2.5V TO 3.3V HIGH PERFORMANCE CLOCK BUFFER

FEATURES:

- **High performance 1:10 clock driver for general purpose applications**
- **Operates up to 200MHz at V_{DD} = 3.3V**
- **Pin-to-pin skew < 100ps**
- **V_{DD} range: 2.3V to 3.6V**
- **Output enable glitch suppression**
- **Distributes one clock input to two banks of five outputs**
- **25Ω on-chip series dampening resistors**
- **Available in TSSOP package**

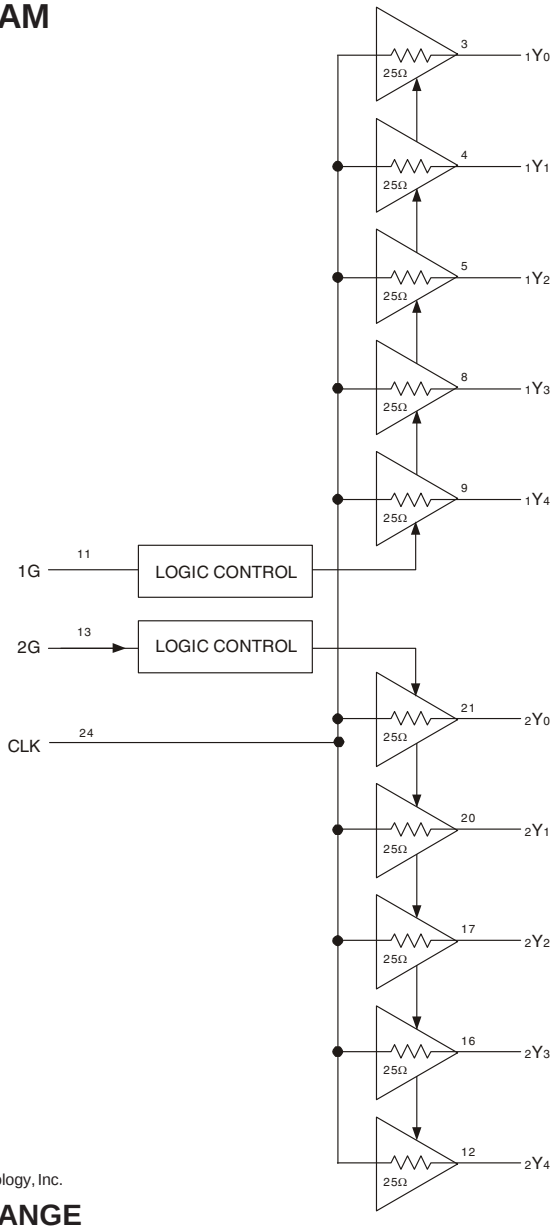
NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

DESCRIPTION:

The IDT5V2310 is a high performance, low skew clock buffer that operates up to 200MHz. Two banks of five outputs each provide low skew copies of CLK. Through the use of control pins 1G and 2G, the outputs of banks 1Y(0:4) and 2Y(0:4) can be placed in a low state regardless of CLK input. The device operates in 2.5V and 3.3V environments. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The IDT5V2310 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



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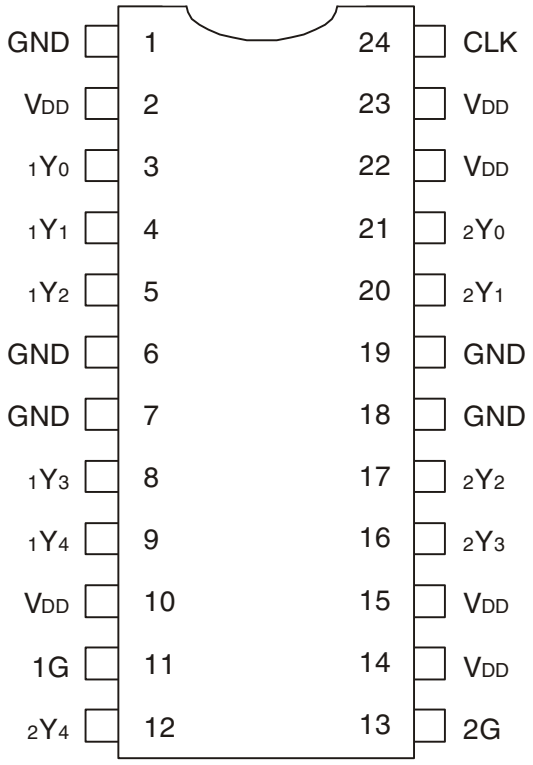
PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	–0.5 to +4.6	V
V_I	Input Voltage(2)	–0.5 to V_{DD} +0.5	V
V_O	Output Voltage(2)	–0.5 to V_{DD} +0.5	V
I_{IK}	Input Clamp Current $V_I < 0$ or $V_I > V_{DD}$	±50	mA
I_{OK}	Output Clamp Current $V_O < 0$ or $V_O > V_{DD}$	±50	mA
I_O	Continuous Total Output Current $V_O < 0$ to V_{DD}	±50	mA
T_{STG}	Storage Temperature	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Not to exceed 4.6V.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = 0V or V_{DD}	—	2.5	—	pF

FUNCTION TABLE(1)

Inputs			Outputs	
1G	2G	CLK	1Y(0:4)	2Y(0:4)
L	L	X	L	L
H	L	H	H	L
L	H	H	L	H
H	H	H	H	H

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

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PIN DESCRIPTION

TERMINAL		Description
Symbol	I/O	
1G	I	Output Enable Control for $_1Y_{(0:4)}$ Outputs. This output enable is active HIGH. If this pin is Logic HIGH, the $_1Y_{(0:4)}$ clock outputs will follow the input clock (CLK). If this pin is logic LOW, the $_1Y_{(0:4)}$ outputs will drive low independent of the state of CLK.
2G	I	Output Enable Control for $_2Y_{(0:4)}$ Outputs. This output enable is active HIGH. If this pin is Logic HIGH, the $_2Y_{(0:4)}$ clock outputs will follow the input clock (CLK). If this pin is logic LOW, the $_2Y_{(0:4)}$ outputs will drive low independent of the state of CLK.
$_1Y_{(0:4)}$	O	Buffered Output Clocks
$_2Y_{(0:4)}$	O	Buffered Output Clocks
CLK	I	Input Reference Frequency
GND		Ground
V_{DD}	PWR	DC Power Supply, 2.3V to 3.6V

RECOMMENDED OPERATING RANGE

Symbol	Description		Min.	Typ.	Max.	Unit
V_{DD}	Internal Power Supply Voltage		2.3	2.5		V
				3.3	3.6	
V_{IL}	Input Voltage LOW	V_{DD} = 3V to 3.6V			0.8	V
		V_{DD} = 2.3V to 2.7V			0.7	
V_{IH}	Input Voltage HIGH	V_{DD} = 3V to 3.6V	2			V
		V_{DD} = 2.3V to 2.7V	1.7			
V_I	Input Voltage		0		V_{DD}	V
I_{OH}	Output Current HIGH	V_{DD} = 3V to 3.6V			-12	mA
		V_{DD} = 2.3V to 2.7V			-6	
I_{OL}	Output Current LOW	V_{DD} = 3V to 3.6V			12	mA
		V_{DD} = 2.3V to 2.7V			6	
T_A	Ambient Operating Temperature		-40		+85	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V_{IK}	Input Voltage	V_{DD} = 3V, I_{IN} = -18mA			- 1.2	V
I_{IN}	Input Current	V_I = 0V or V_{DD}			±5	µA
I_{DD}	Static Device Current[1]	CLK = 0V or V_{DD}, I_O = 0mA, V_{DD} = 3.3V			25	µA

NOTE:

1. For I_{DD} over frequency, see TEST CIRCUIT AND WAVEFORMS.

DC ELECTRICAL CHARACTERISTICS - V_{DD} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max	Unit
V_{OH}	HIGH level Output Voltage	V_{DD} = Min. to Max.	I_{OH} = -100µA	V_{DD} - 0.2			V
		V_{DD} = 3V	I_{OH} = -12mA	2.1			
			I_{OH} = -6mA	2.4			
V_{OL}	LOW level Output Voltage	V_{DD} = Min. to Max.	I_{OL} = 100µA			0.2	V
		V_{DD} = 3V	I_{OL} = 12mA			0.8	
			I_{OL} = 6mA			0.55	
I_{OH}	HIGH level Output Current	V_{DD} = 3V	V_O = 1V	-28			mA
		V_{DD} = 3.3V	V_O = 1.65V		-36		
		V_{DD} = 3.6V	V_O = 3.135V			-14	
I_{OL}	LOW level Output Current	V_{DD} = 3V	V_O = 1.95V	28			mA
		V_{DD} = 3.3V	V_O = 1.65V		36		
		V_{DD} = 3.6V	V_O = 0.4V			14	

NOTE:

1. All typical values are at respective nominal V_{DD}.

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DC ELECTRICAL CHARACTERISTICS - V_{DD} = 2.5V ± 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max	Unit
V_{OH}	HIGH level Output Voltage	V_{DD} = Min. to Max.	I_{OH} = -100µA	V_{DD} - 0.2			V
		V_{DD} = 2.3V	I_{OH} = -6mA	1.8			
V_{OL}	LOW level Output Voltage	V_{DD} = Min. to Max.	I_{OL} = 100µA			0.2	V
		V_{DD} = 2.3V	I_{OL} = 6mA			0.55	
I_{OH}	HIGH level Output Current	V_{DD} = 2.3V	V_O = 1V	-17			mA
		V_{DD} = 2.5V	V_O = 1.25V		-25		
		V_{DD} = 2.7V	V_O = 2.375V			-10	
I_{OL}	LOW level Output Current	V_{DD} = 2.3V	V_O = 1.2V	17			mA
		V_{DD} = 2.5V	V_O = 1.25V		25		
		V_{DD} = 2.7V	V_O = 0.3V			10	

NOTE:

1. All typical values are at respective nominal V_{DD}.

TIMING REQUIREMENTS OVER RECOMMENDED RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
f_{CLK}	Clock Frequency	V_{DD} = 3V to 3.6V	0		200	MHz
		V_{DD} = 2.3V to 2.7V	0		170	

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE - V_{DD} = 3.3V ± 0.3V(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max	Unit
t_{PLH} t_{PHL}	CLK to Yx	f = 0MHz to 200MHz	1.3		2.8	ns
$t_{SK(O)}$(2)	Output Skew, Yx to Yx				100	ps
$t_{SK(P)}$	Pulse Skew				250	ps
$t_{SK(PP)}$	Part-to-Part Skew				500	ps
t_R	Rise Time	V_O = 0.4V to 2V(3)	0.7		2	V/ns
t_F	Fall Time	V_O = 2V to 0.4V(3)	0.7		2	V/ns
t_{SU}	G before CLK↓	$V_{(THRESHOLD)} = V_{DD}/2$	0.1			ns
t_H	G after CLK↓		0.4			

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.
3. Measured at 100MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - V_{DD} = 2.5V ± 0.2V(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max	Unit
t_{PLH} t_{PHL}	CLK to Yx	f = 0MHz to 170MHz	1.5		3.5	ns
$t_{SK(O)}$(2)	Output Skew, Yx to Yx				100	ps
$t_{SK(P)}$	Pulse Skew				400	ps
$t_{SK(PP)}$	Part-to-Part Skew				600	ps
t_R	Rise Time	V_O = 0.4V to 1.7V(3)	0.5		1.4	V/ns
t_F	Fall Time	V_O = 1.7V to 0.4V(3)	0.5		1.4	V/ns
t_{SU}	G before CLK↓	$V_{(THRESHOLD)} = V_{DD}/2$	0.1			ns
t_H	G after CLK↓		0.4			

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.
3. Measured at 100MHz.

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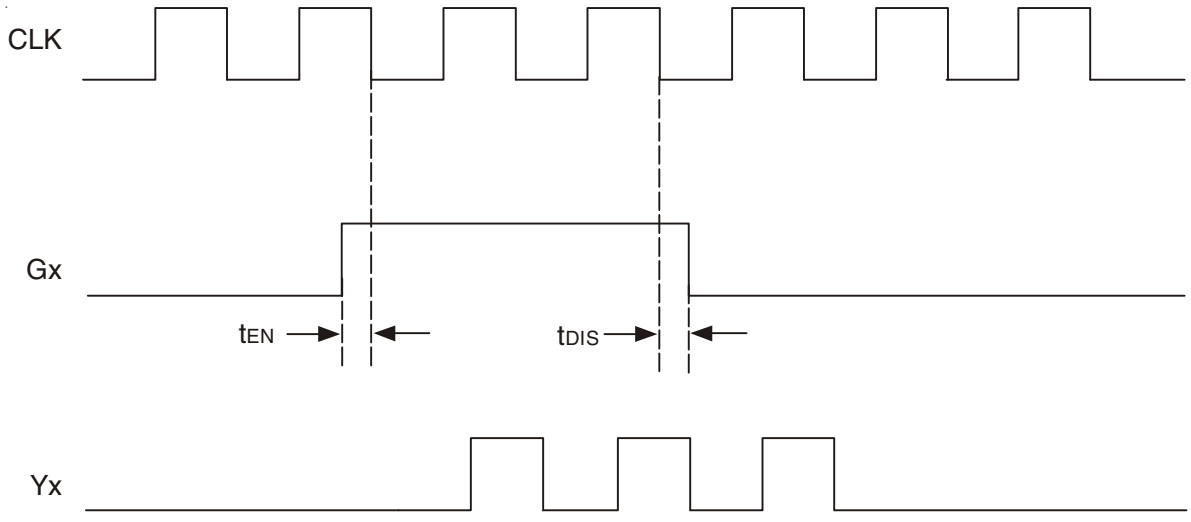
OUTPUT ENABLE GLITCH SUPPRESSION CIRCUIT

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer will be enabled on the next full period of the input clock (negative edge triggered by the input clock). The G input must be stable one t_{EN} - time prior to the falling edge of the CLK for predictable operation.



G (t_{EN}, t_{DIS}) Relative to CLK↓

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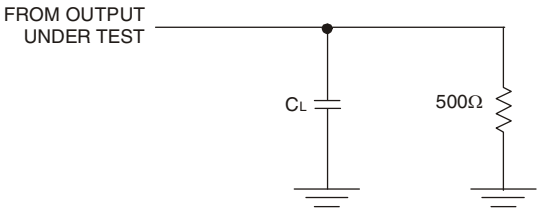
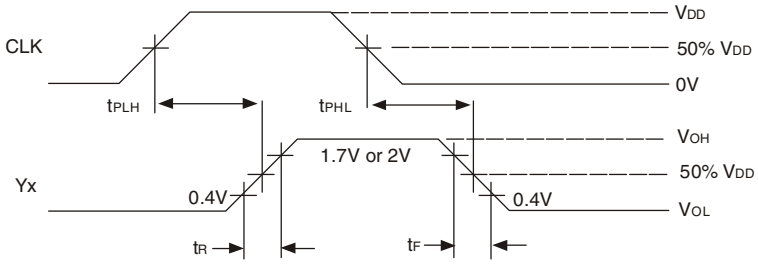
TEST CIRCUITS AND WAVEFORMS

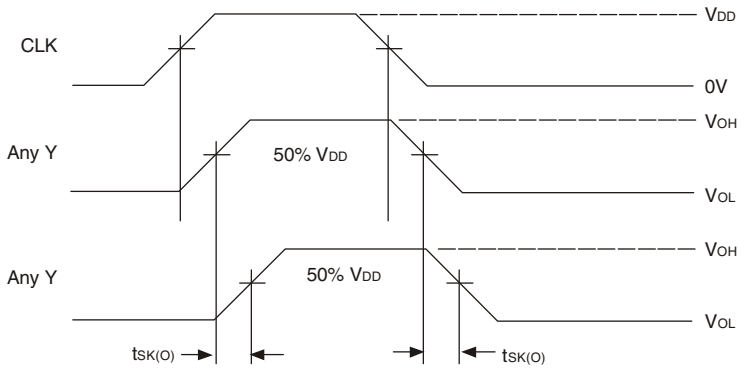


NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤200MHz; Z_O = 50Ω; t_R < 1.2ns; t_F < 1.2ns.

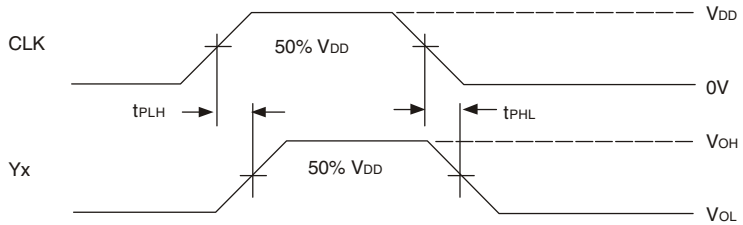
Test Load Circuit



Voltage Waveforms Propagation Delay Times



Output Skew



$$t_{SK(P)} = \left| t_{PLH} - t_{PHL} \right|$$

Pulse Skew

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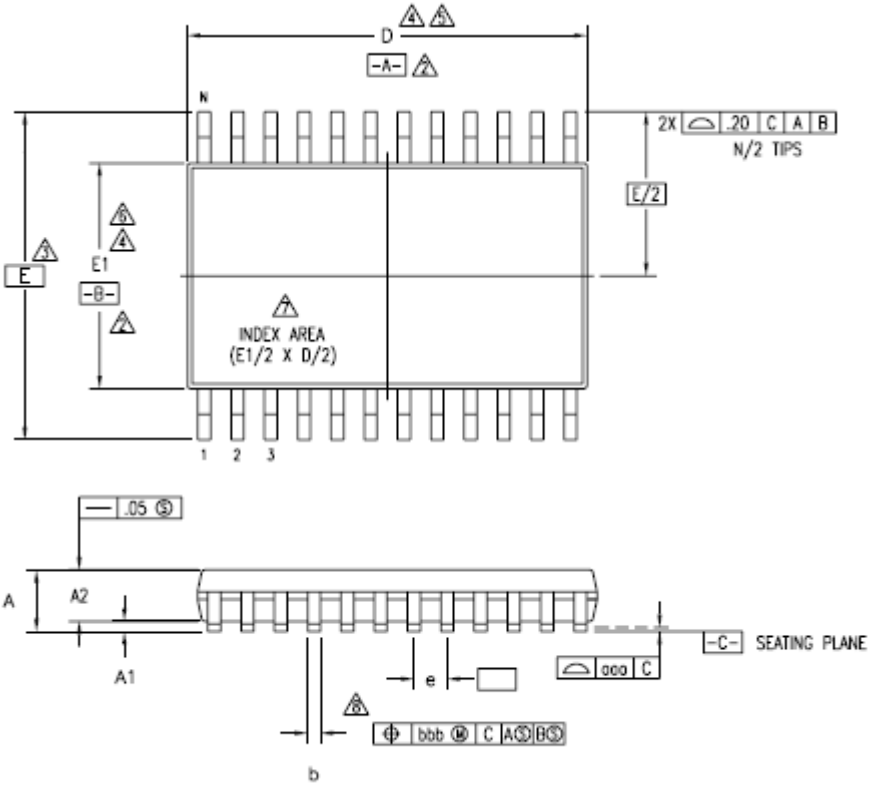
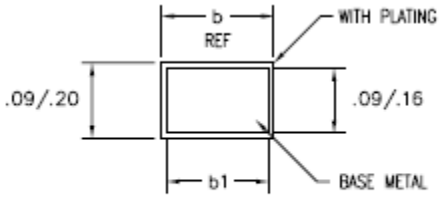
PACKAGE DRAWING AND DIMENSIONS (24-PIN TSSOP)



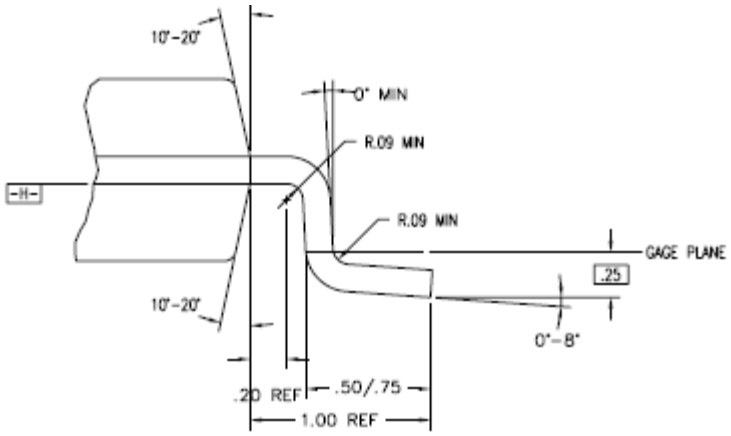


SECTION A-A

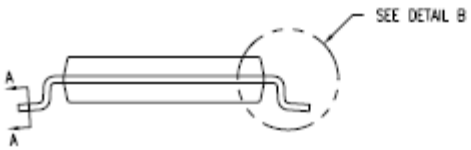
JEDEC VARIATION AD			NOTE
MIN	NOM	MAX	
–	–	1.20	
.05	–	.15	
.80	1.00	1.05	
7.70	7.80	7.90	4,5
6.40 BSC			3
4.30	4.40	4.50	4,6
.65 BSC			
.19	–	.30	
.19	.22	.25	
–	–	.10	
–	–	.10	
24			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE



DETAIL B



MARKING DIAGRAM

IDT5V231
0PGGI
YYWW$
●

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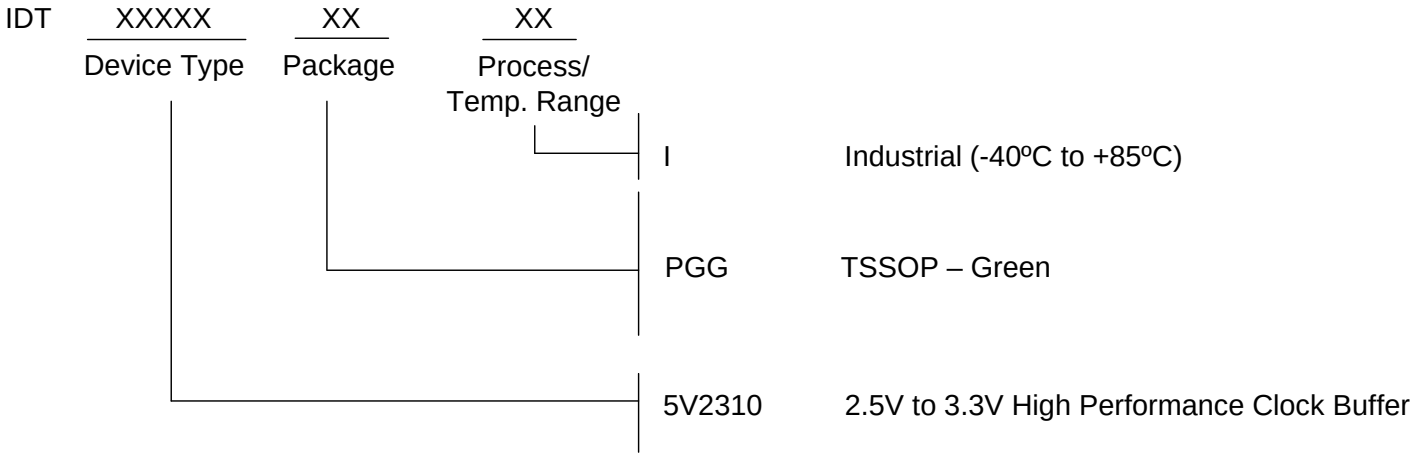
ORDERING INFORMATION



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