

LOW SKEW PCI/PCI-X BUFFER

ICS2304NZ-1

Description

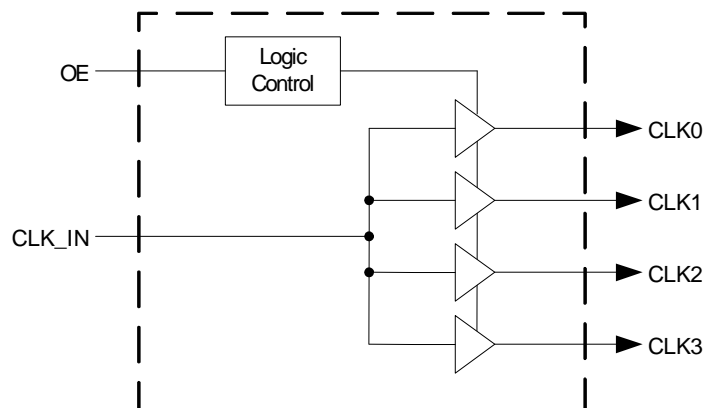
The ICS2304NZ-1 is a high-performance, low skew, low jitter PCI/PCI-X clock driver. It is designed to distribute high-speed signals in PCI/PCI-X applications operating at speeds from 0 to 140 MHz.

The ICS2304NZ-1 is characterized for operation from -40°C to +85°C for automotive and industrial applications.

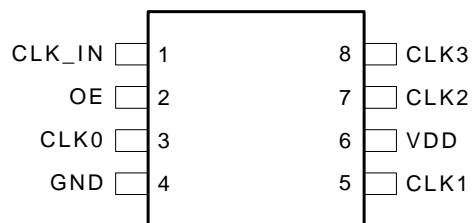
Features

- Packaged in 8-pin TSSOP (4.4 mm body)
- Frequency range of 0 to 140 MHz
- Less than 100 ps skew between outputs
- Distribute one clock input to one bank of four outputs
- Operating voltage of 3.3 V $\pm 10\%$
- Available in commercial and industrial temperature ranges

Block Diagram



Pin Assignment



Functionality Table

Inputs		Outputs
CLK_IN	OE	CLK(3:0)
0	0	Tristate
0	1	0
1	0	Tristate
1	1	1

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK_IN	Input	Input reference frequency.
2	OE	Input	Output Enable. When OE is low, it tri-states clock outputs.
3	CLK0	Output	Buffered clock output.
4	GND	Power	Connect to ground.
5	CLK1	Output	Buffered clock output.
6	VDD	Power	Power supply for 3.3 V.
7	CLK2	Output	Buffered clock output.
8	CLK3	Output	Buffered clock output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS2304NZ-1. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage Range, V_{DD}	-0.5 V to 4.3 V
Input Voltage Range, V_I (see notes 1 and 2)	-0.5 V to $V_{DD} + 0.5$ V
Output Voltage Range, V_O (see notes 1 and 2)	-0.5 V to $V_{DD} + 0.5$ V
Input Clamp Current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 50 mA
Output Clamp Current, I_{IK} ($V_O < 0$ or V_O)	± 50 mA
Continuous Total Output Current, I_O ($V_O = 0$ to V_{DD})	± 50 mA
Package Thermal Impedance, θ_{JA} (see note 3): PW Package	230.5° C/W
Storage Temperature Range, T_{stg}	-65° C to 150° C

Notes:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	3	3.3	3.6	V
High-level Input Voltage, V_{IH}	$0.7 \times V_{DD}$			V
Low-level Input Voltage, V_{IL}			$0.3 \times V_{DD}$	V
Input Voltage, V_I	0		V_{DD}	V
High-level Output Current, I_{OH}			-24	mA
Low-level Output Current, I_{OL}			24	mA
Operating Free-air Temperature, T_A	-40	—	+85	°C

Timing Requirements Over Recommended Ranges of Supply Voltage and Operating Free-air Temperature

	Min.	Typ.	Max.	Units
Clock Frequency, f_{CLK}	0		140	MHz

Electrical Characteristics at 3.3 V over Recommended Free-air Temperature Range

VDD = 3.3 V \pm 10%, T_A = -40°C to +85°C (unless stated otherwise)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage	V _{IK}	V _{DD} at 3.3 V, I _I = -18 mA			-1.2	V
High-level Output Voltage	V _{OH}	V _{DD} = min to max, I _{OH} = -1 mA	V _{DD} -0.2	3.3		V
		V _{DD} = 3 V, I _{OH} = -24 mA	2	2.3		
		V _{DD} = 3 V, I _{OH} = -12 mA	2.4	2.7		
Low-level Output Voltage	V _{OL}	V _{DD} = min to max, I _{OH} = 1 mA		0.222	0.2	V
		V _{DD} = 3 V, I _{OL} = 24 mA		0.61	0.8	
		V _{DD} = 3 V, I _{OL} = 12 mA		0.31	0.55	
High-level Output Current	I _{OH}	V _{DD} = 3 V, V _O = 1 V		-53	-40	mA
		V _{DD} = 3.3 V, V _O = 1.65 V		-54		
Low-level Output Current	I _{OL}	V _{DD} = 3 V, V _O = 2 V	40	53		mA
		V _{DD} = 3.3 V, V _O = 1.65 V		57		
Input Current	I _I	V = V _{DD} or V _O	0.1		50	μA
Dynamic Supply Current	I _{DD}	Unloaded outputs at 66.67 MHz		13	37	mA
Input Capacitance (Note 1)	C _I	V _{DD} = 3.3 V, V _I = 0V or 3.3 V		3	5	pF
Output Capacitance (Note 1)	C _O	V _{DD} = 3.3 V, V _I = 0V or 3.3 V		3.2		pF

Note 1: Guaranteed by design, not 100% tested in production.

Switching Characteristics at 3.3 V over Recommended Ranges of Supply Voltage and Operating Free-air Temperature

VDD = 3.3 V \pm 10%, T_A = -40°C to 85°C (unless stated otherwise)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
High-to-Low Propagation Delay (Note 1)	t _{PLH}	V _O = V _{DD} /2	1.8	3.1	3.8	ns
Low-to-High Propagation Delay (Note 1)	t _{PHL}	V _O = V _{DD} /2	1.8	2.9	3.8	ns
Output Skew Window (Note 1)	T _{SK(o)}	V _O = V _{DD} /2		50	100	ps
Pulse Skew = t _{PLH} - t _{PHL} (Note 1)	T _{SK(p)}	V _O = V _{DD} /2			300	ps
Process Skew (Note 1)	T _{SK(pr)}	V _O = V _{DD} /2			500	ps
CLKIN High Time (Note1)	T _{high}	66 MHz	6			ns
		140 MHz	3			ns
CLKIN Low Time (Note1)	T _{low}	66 MHz	6			ns
		140 MHz	3			ns
Rise Time (Note 1)	T _r	V _{OL} =0.8 V, V _{OH} =2.0 V		1.2	2.0	ns
Fall Time (Note 1)	T _f	V _{OH} =2.0 V, V _{OL} =0.8 V		1.2	2.0	ns
Cycle-to-Cycle Jitter	T _{cyc-cyc}	Loaded outputs			200	ps
Jitter, 1-Sigma	T _{j1s}	10,000 cycles		14	40	ps

Note 1: Guaranteed by design, not 100% tested in production.

Parameter Measurement Information

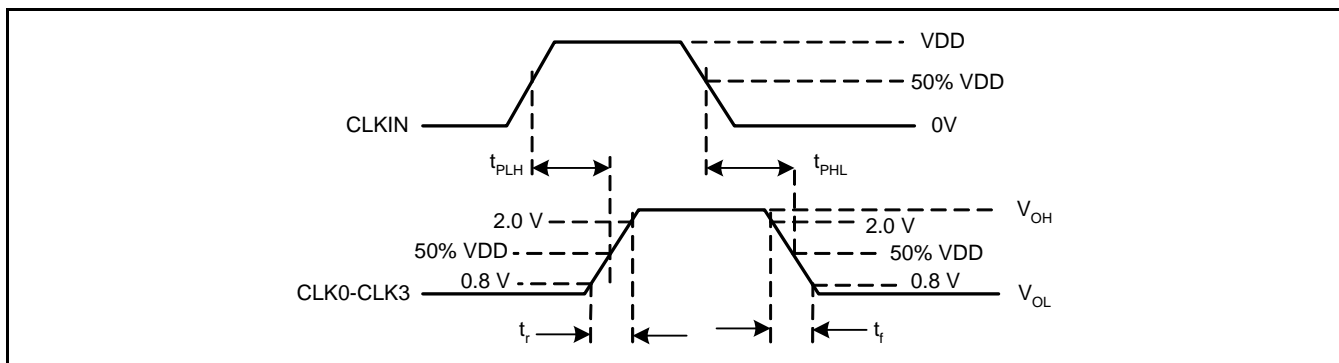


Figure 2. Voltage Thresholds for Propagation Delay (t_{pd}) Measurements

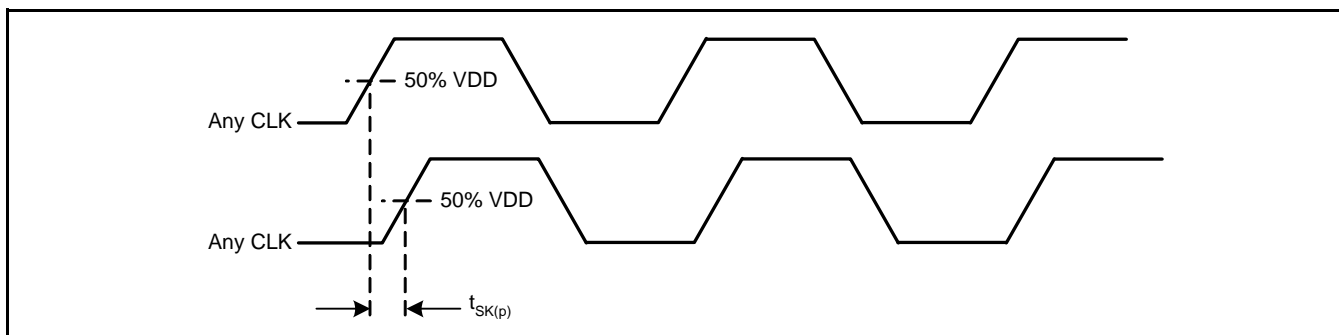


Figure 3. Output Skew

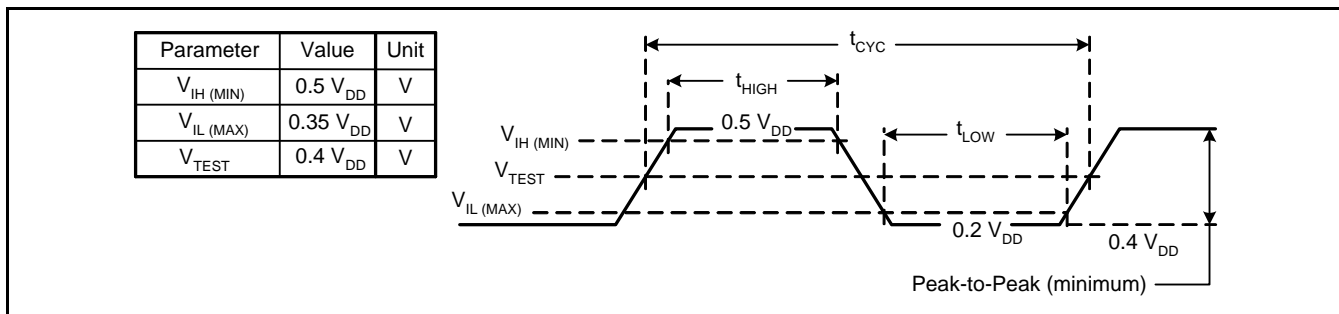


Figure 4. Clock Waveform

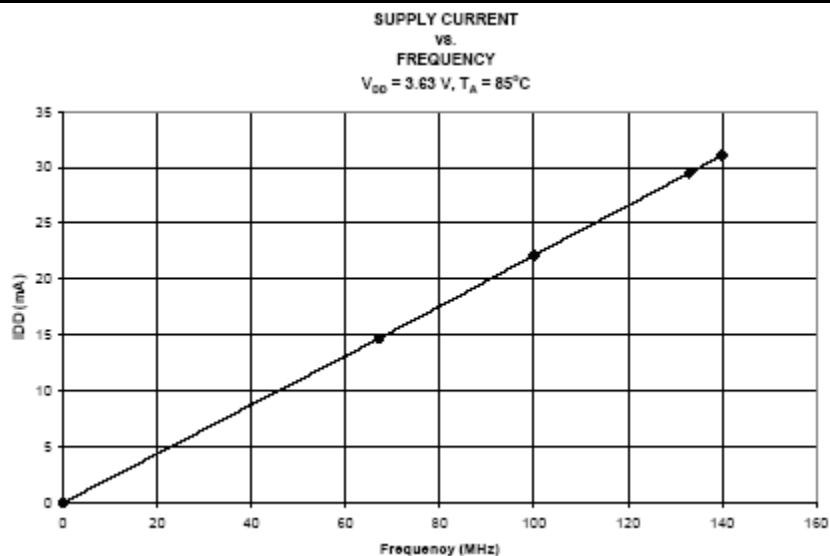


Figure 5. Supply Current vs. Frequency

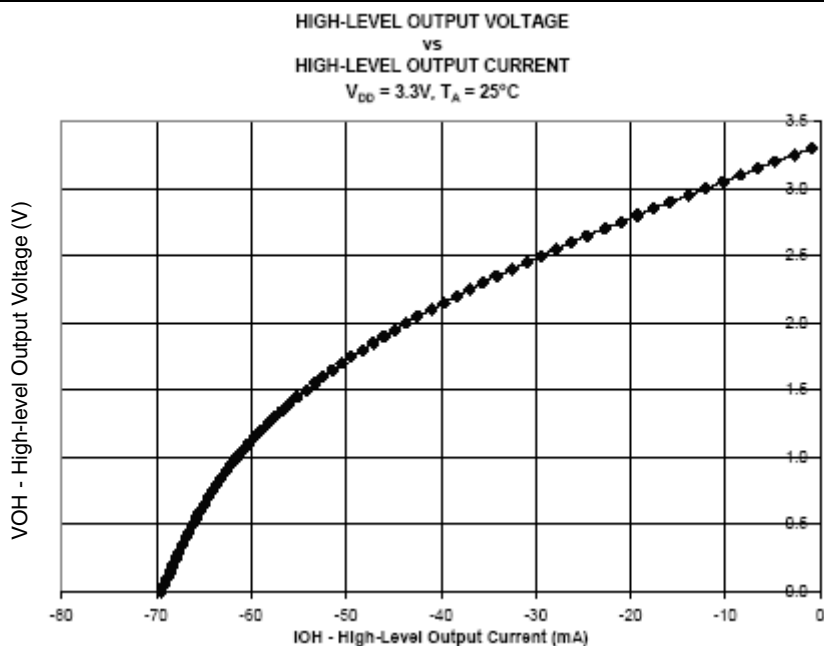


Figure 6. High-level Output Voltage vs. High-level Output Current

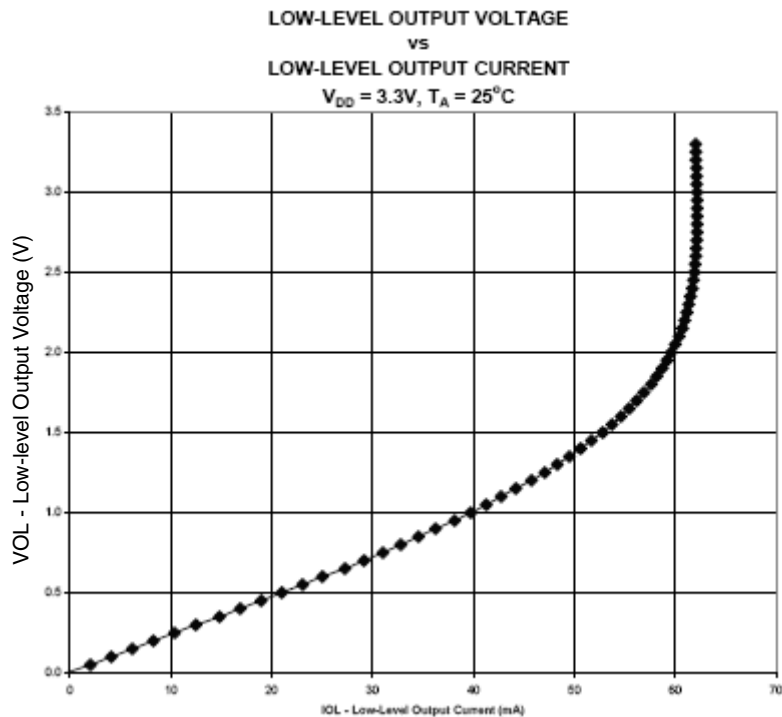
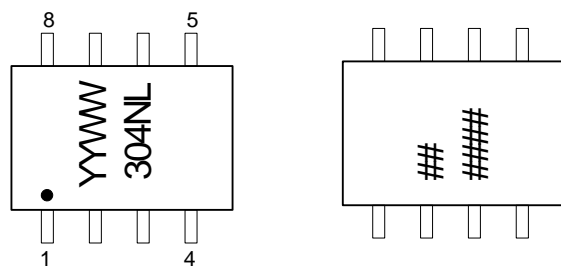


Figure 7. Low-level Output Voltage vs. Low-level Output Current

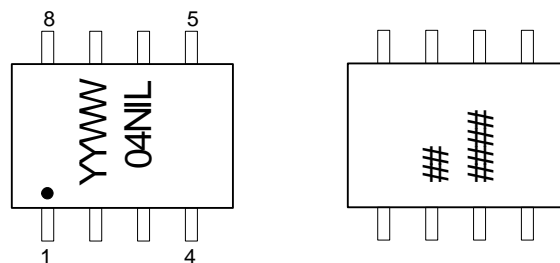
Marking Diagram (commercial)



TOP

BOTTOM

Marking Diagram (industrial)



TOP

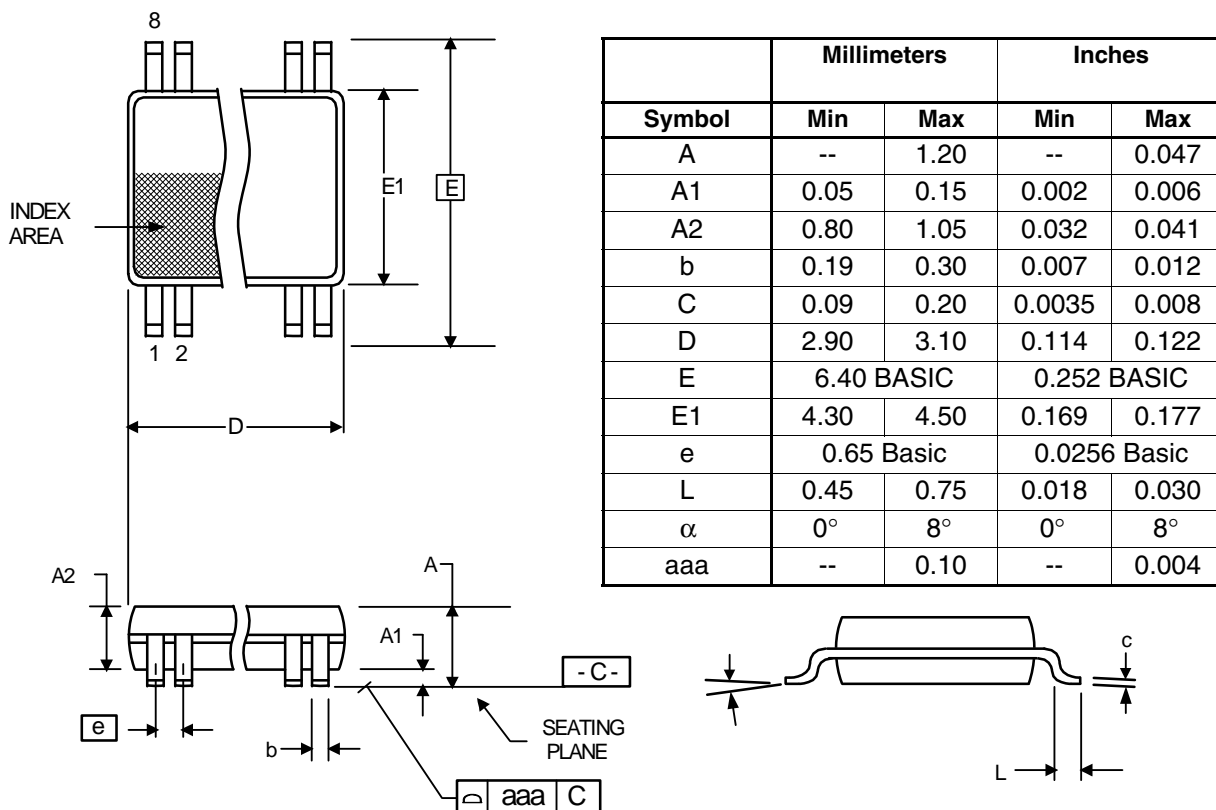
BOTTOM

Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "L" denotes Pb (lead) free package.

Package Outline and Package Dimensions (8-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
2304NZG-1LF	see page 9	Tubes	8-pin TSSOP	0 to +70° C
2304NZG-1LFT		Tape and Reel	8-pin TSSOP	0 to +70° C
2304NZGI-1LF		Tubes	8-pin TSSOP	-40 to +85° C
2304NZGI-1LFT		Tape and Reel	8-pin TSSOP	-40 to +85° C

“LF” suffix to the part number are the Pb-Free configuration, RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, IDT assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Renesas Electronics:](#)

[2304NZGI-1LF](#) [2304NZGI-1LFT](#) [2304NZG-1LF](#) [2304NZG-1LFT](#)