Data Brief
PTX105R NFC Reader IC

Product Description

The PTX105R is a highly integrated NFC reader IC for contactless communication, which is optimized for reader performance and interoperability (Vcc current up to 500mA). While eliminating EMC filter and matching components, the PTX105R enables simple integration and compact design without the complexity associated with existing solutions (dual resonating circuits composed by EMC filter and antenna).

Due to its modular Soft Controller architecture, the NFC functionalities are integrated into a split stack solution where time-critical operations are running on the on-chip MCU, and the rest of the NFC logic is in the host controller to carry out applications such as IOT reader and POS.

Features

The architecture enables:

- Efficient power transmission with accurate digital programmability of RF carrier and modulation shape
- EMC filter removal due to sinewave output driver and Direct Antenna Connection (DiRAC)
- -80dBc RX sensitivity with full dynamic range due to DiRAC
- SDK composed of FW and SW integrated in a Split Stack architecture with Over-The-Air firmware update on the host processor:
  - Modular SW stack running on the Host architecture
  - Integrated FW running on the on-chip MCU for timing critical operations
- Fractional-N PLL to support any reference input clock frequency from 13.15MHz to 52MHz
- Low Power Card Detection (LPCD)
- ISO/IEC14443-A reader/writer mode up to 848kBit/s
- ISO/IEC14443-B reader/writer mode up to 848kBit/s
- NFC Forum Poller mode
- Supports reading of NFC Tag Type 2, 3, 4A/4B and 5
- FeliCa reader/writer mode 212&424kBit/s
- ISO/IEC 15693 reader/writer mode
- NFC Forum P2P Passive Initiator
- NFC Card Emulation Mode for Tag Type 4A (106kBit/s)
- Low Power Field Detection (LPFD)
- EMVCo® 3.0/3.1 PCD L1 compliancy[1]
- Supported host interfaces: I2C, SPI, UART

PTX105R reader IC enables key improvements in customer care-about such as:

RF performance: Patented groundbreaking architecture enables efficient power transmission and -80dBc RX sensitivity, state of the art reader performance even in challenging and complex integration environments.

Interoperability:

- Digitized architecture enables accurate shape control of the modulated signal.
- Elimination of the EMC filter results in well-behaved signal shape avoiding overshoot and undershoot
- DiRAC allows minimum output power loss on matching structure with high input sensitivity, which translates to substantially larger operating volume.

[1] *Depending on the Software Stack, full NFC Forum Poller functionality or EMVCo® L1 is supported by PTX105R.*

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Order information
sales@panthronics.com
Panthronics AG
Sternaeckerweg 16
8041 Graz, Austria
+43 316 269 259-0
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www.panthronics.com

Manufacturability:

- No need for bulky and performance-limiting external components of the EMC filter (no tolerances issue introduced) minimizing the performance variation between final devices.
- Reduced number of matching components allow lower antenna matching impedance, resulting in higher output power.
- Accurate adjustment of transmitter and receiver parameters due to digital architecture enabling tighter production control giving more margin for new use cases.

PTX105R is optimized for applications such as IoT Reader, Access Control, Gaming, Transportation, Wearables, POS etc.

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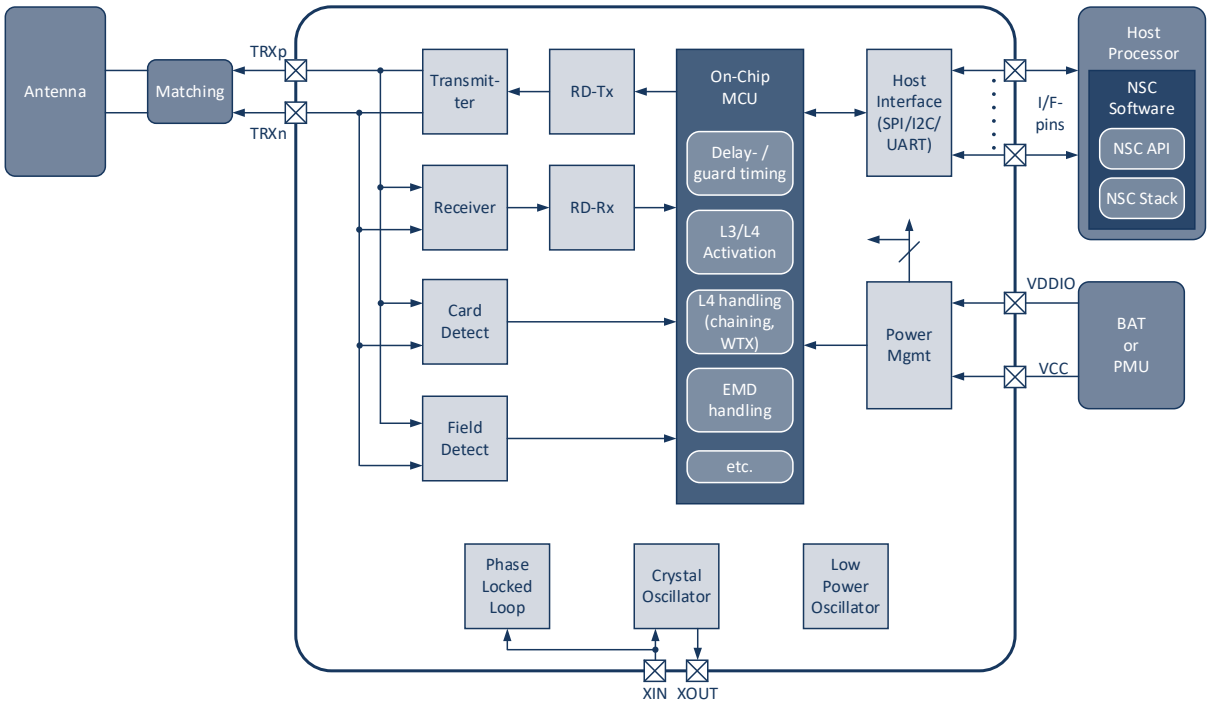

Figure 1: PTX105R Block Diagram

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1 Pinning Information

1.1 Pin Diagram

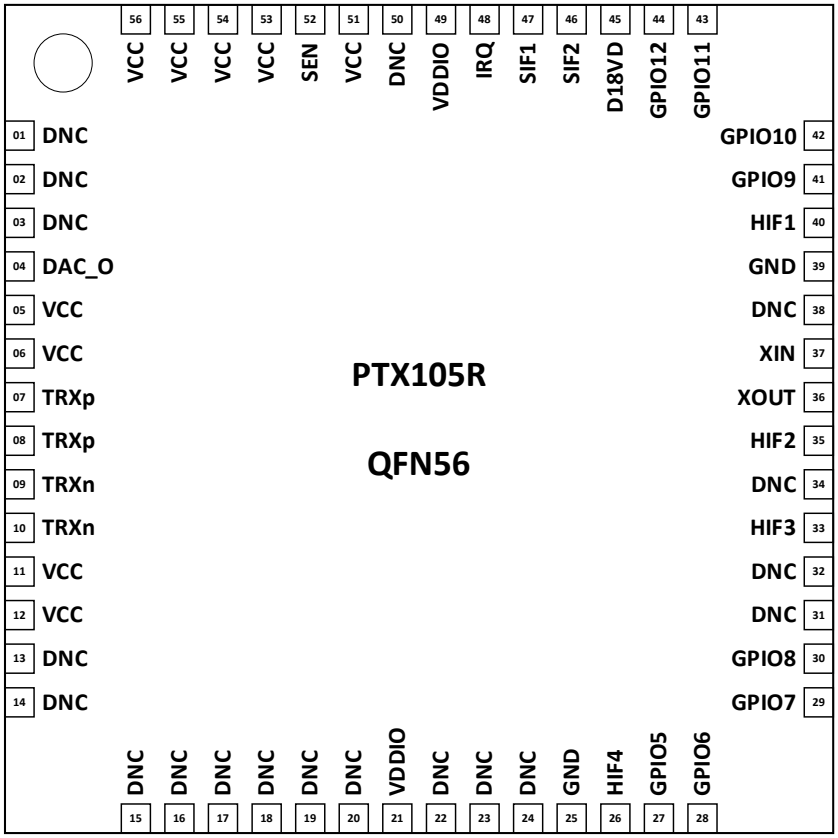

Figure 2: Pin Diagram

1.2 Pin Description

Signal Name	Signal Type	QFN56 Pin	Description
DNC	-	1	Do not connect
DNC	-	2	Do not connect
DNC	-	3	Do not connect
DAC_O	Analog out	4	AUX-DAC output voltage
VCC	Supply	5	NFC IC supply
VCC	Supply	6	NFC IC supply
TRXp	Analog inout	7	Transmitter/Receiver pin p
TRXp	Analog inout	8	Transmitter/Receiver pin p
TRXn	Analog inout	9	Transmitter/Receiver pin n
TRXn	Analog inout	10	Transmitter/Receiver pin n
VCC	Supply	11	NFC IC supply
VCC	Supply	12	NFC IC supply
DNC	-	13	Do not connect
DNC	-	14	Do not connect
DNC	-	15	Do not connect
DNC	-	16	Do not connect
DNC	-	17	Do not connect
DNC	-	18	Do not connect
DNC	-	19	Do not connect
DNC	-	20	Do not connect
VDDIO	Supply	21	IO Pad supply

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DNC	-	22	Do not connect
DNC	-	23	Do not connect
DNC	-	24	Do not connect
GND	Supply	25	Ground
HIF4	Digital inout	26	SPI: MISO, I2C: SCL, UART: TXD
GPIO5	Digital inout	27	General purpose digital IO pin
GPIO6	Digital inout	28	General purpose digital IO pin
GPIO7	Digital inout	29	General purpose digital IO pin
GPIO8	Digital inout	30	General purpose digital IO pin
DNC	-	31	Do not connect
DNC	-	32	Do not connect
HIF3	Digital inout	33	SPI: MOSI, I2C: SDA, UART: RXD
DNC	-	34	Do not connect
HIF2	Digital inout	35	SPI: SCK, I2C: ADDR1, UART: RTS
XOUT	Analog out	36	Xtal oscillator output
XIN	Analog in	37	Xtal oscillator input / Reference clock input
DNC	-	38	Do not connect
GND	Supply	39	Ground
HIF1	Digital inout	40	SPI: NSS, I2C: ADDR0, UART: CTS
GPIO9	Digital inout	41	General purpose digital IO pin
GPIO10	Digital inout	42	General purpose digital IO pin
GPIO11	Digital inout	43	General purpose digital IO pin
GPIO12	Digital inout	44	General purpose digital IO pin
D18VD	Supply	45	Decoupling of core supply
SIF2	Digital in	46	Select interface type bit 2
SIF1	Digital in	47	Select interface type bit 1
IRQ	Digital out	48	Interrupt request to host
VDDIO	Supply	49	IO Pad supply
DNC	-	50	Do not connect
VCC	Supply	51	NFC IC supply
SEN	Analog in	52	System enable input
VCC	Supply	53	NFC IC supply
VCC	Supply	54	NFC IC supply
VCC	Supply	55	NFC IC supply
VCC	Supply	56	NFC IC supply
GND	Supply	-	The exposed pad at the back of QFN is used as GND Requires good thermal connection to ensure low thermal resistance for power dissipation

Table 1: Pin Description

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Sternaeckerweg 16
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2 Functional Description

2.1 System Architecture

PTX105R is a highly integrated reader IC using a split-stack SW architecture, allowing flexible adaption of SW to the needs of the application system such as IoT/NFC Reader, POS etc. This flexibility is achieved by an optimized software interface and ready to use SW-stack for the host-controller. The portable SW stack written in C, implements high level NFC functionality and provides easy to use APIs for integration into the Host system.

The PTX solution is modular and runs on different platforms, providing additional facilities for custom features in case needed.

2.2 Power Management

The power management unit is the central circuit of the PTX105R responsible for providing all necessary reference voltages and currents, generating the internal supply domains, implementing the power-up sequence, and controlling the transitions between different energy states. PTX105R has 3 externally accessible supply domains: VCC, D18VD and VDDIO.

To support the implementation of flexible system power consumption profiles, PTX105R offers different energy states such as Full-Power mode as main operating mode, Power Down mode with maximum power saving on PTX105R as well as standby mode for low power applications.

2.3 Clock Concept

In PTX105R a low-power oscillator (LPO), a crystal oscillator (XO) and a phase-locked loop (PLL) are the main blocks responsible for generating the necessary internal clocks in the various modes.

The reference clock for PTX105R can either be provided from an external clock source or the internal crystal oscillator can be employed. Out of this clock, the PLL subsequently derives the system frequency of 13.56MHz.

2.4 Contactless Interface

PTX105R device has an innovative and patented architecture for the NFC-RF-System in place, that improves performance compared to conventional NFC architectures. Both transmitter and receiver, follow new approaches to bring NFC to the next performance level.

2.5 Host Interface

PTX105R supports the most used industry standard host interfaces, namely SPI, I2C and UART.

The host interface is designed for typical interface supply voltages used by micro-controllers in the range of 1.8V to 5V which must be supplied by the host via the VDDIO pin.

2.6 SW Split Stack

Panthronics provides additional SW-stacks to further ease the integration of the PTX105R into the target application. The SW stacks manage all interactions with the PTX105R, by setting up and configuring the device, consolidating status information, handling error messages, and establishing a data channel between the host and the NFC controller.

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3 Reference Schematic

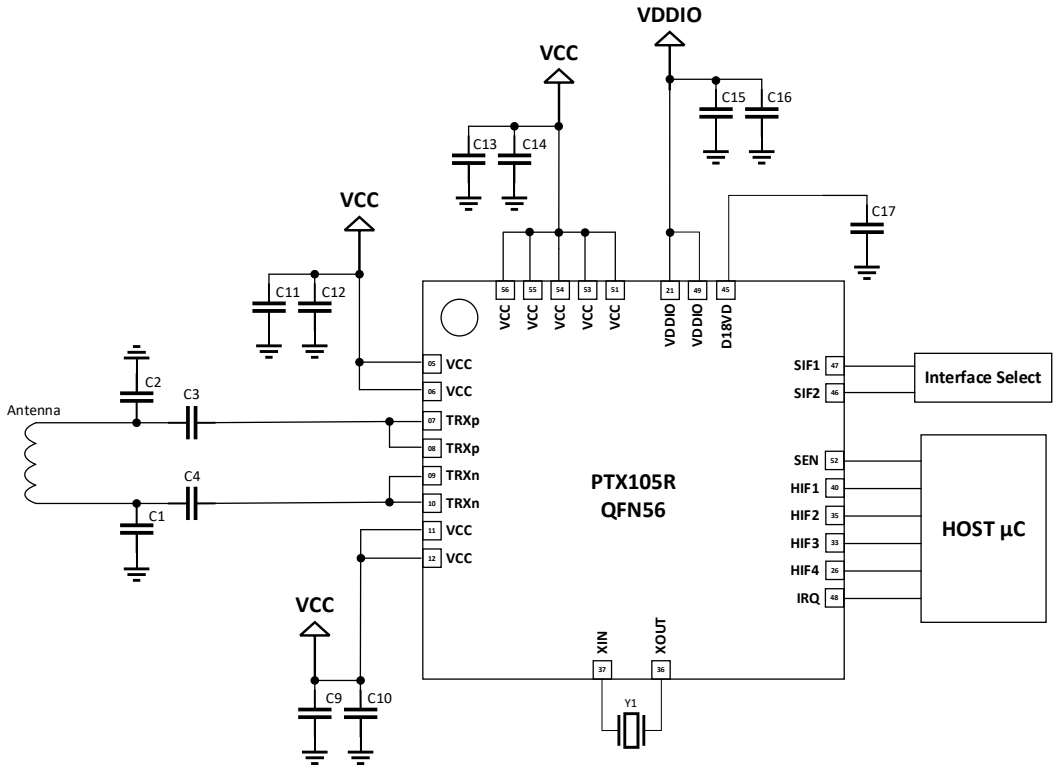

Figure 3: Exemplary Reference Schematic

Designator	Component type	Component value	Description
C1, C2, C3, C4	Ceramic capacitor, C0G type	-	Matching capacitors
C9, C11, C13	Ceramic capacitor, C0G type	10µF	Note that capacitor shall have at least 2.2µF effective capacitance at applied voltage
C10, C12, C14, C15, C17	Ceramic capacitor, C0G type	100nF	
C16	Ceramic capacitor, C0G type	10µF	Optional, depending upon VDDIO supply noise/impedance
Y1	Crystal oscillator	27.12MHz	According to Crystal Requirements in PTX105R Datasheet

Table 2 Reference Schematic Components

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8041 Graz, Austria
+43 316 269 259-0
office@panthronics.com
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4 Package Information

4.1 Package Marking

Figure 4 Package Marking Drawing

Symbol	Description
PTX105R	Device Name
XXXXXX.X	Wafer Lot No.
YYWW	Production year/week

Table 3 Marking Code HVQFN56

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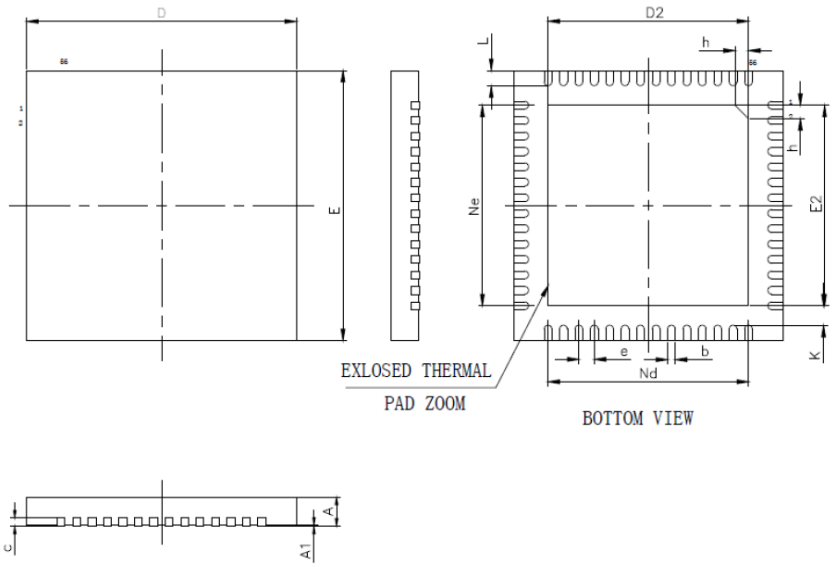
4.2 Package Drawing and Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
e	0.40BSC		
Nd	5.20BSC		
Ne	5.20BSC		
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
K	0.20	—	—
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	217*217		

Figure 5: Package Drawings and Dimensions

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