

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Available in TSSOP package

## DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$  (A port)
- High Output Drivers:  $\pm 24mA$  (B port)

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

This 16-bit bus transceiver is built using advanced dual metal CMOS technology. This high-speed, low power transceiver is ideal for asynchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (DIR) controls the direction of data flow. The output enable pin ( $\overline{OE}$ ) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

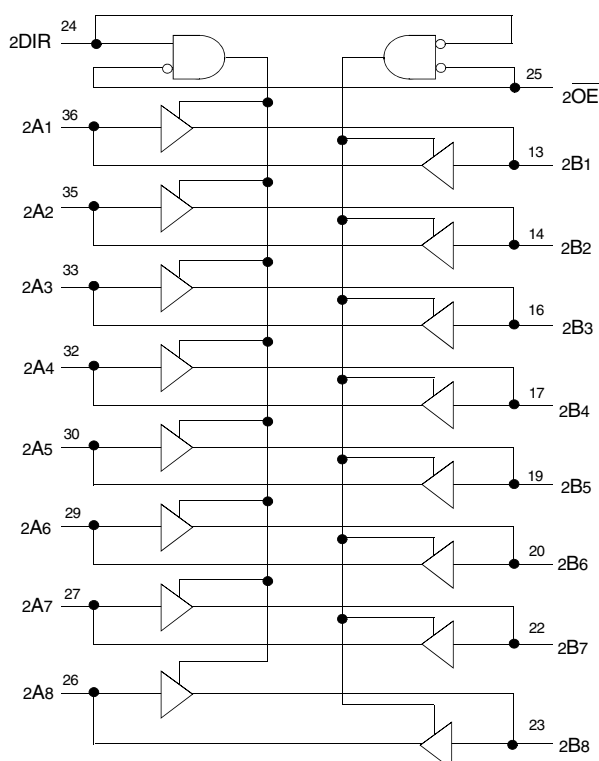
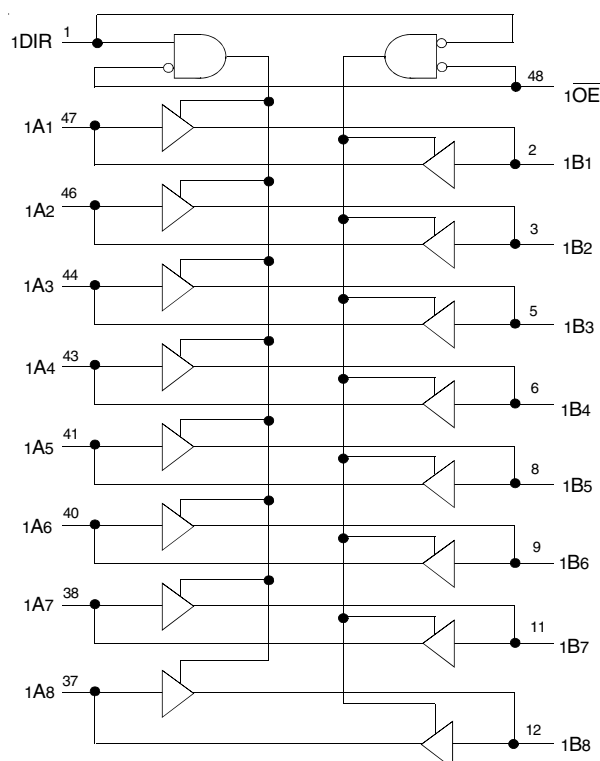
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH162245A (B port) has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

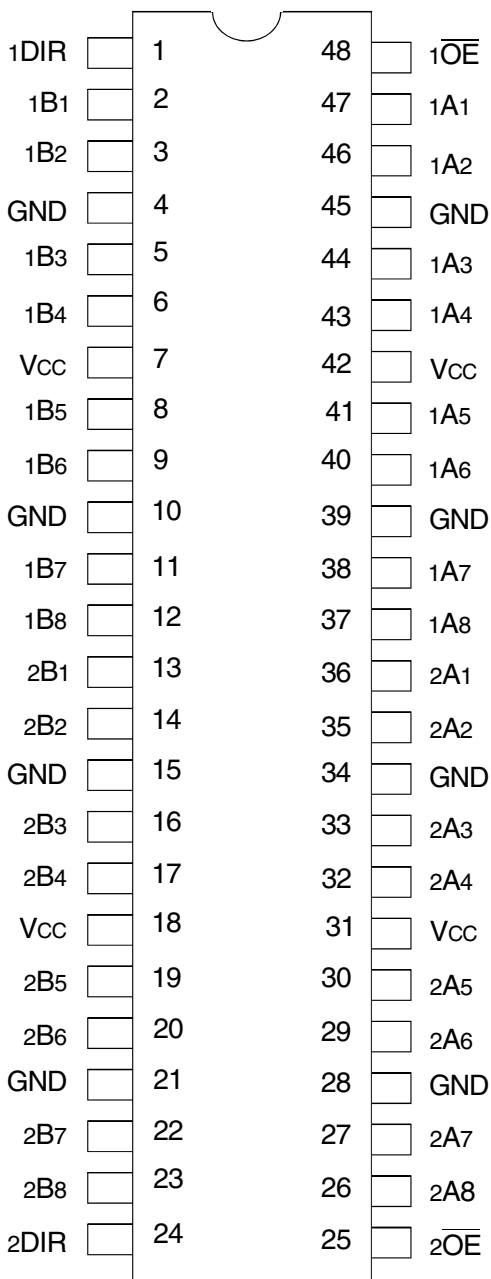
The LVCH162245 (A port) has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been designed to drive  $\pm 12mA$  at the designated threshold levels.

The LVCH162245A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
x $\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Output
x A x	Side A Inputs or 3-State Outputs <sup>(1)</sup>
x B x	Side B Inputs or 3-State Outputs <sup>(1)</sup>

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1)</sup>

Inputs		Outputs
x $\overline{OE}$	xDIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Z State

### NOTE:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

### NOTES:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	—	—	—	
$I_{BHHO}$ $I_{BHLO}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

### NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS (A PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -4mA	1.9	—	
			IOH = -6mA	1.7	—	
		VCC = 2.7V	IOH = -4mA	2.2	—	
			IOH = -8mA	2	—	
		VCC = 3V	IOH = -6mA	2.4	—	
			IOH = -12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.  
TA = -40°C to +85°C.

## OUTPUT DRIVE CHARACTERISTICS (B PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -6mA	2	—	
		VCC = 2.3V	IOH = -12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = -24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.  
TA = -40°C to +85°C.

## OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$ , $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0pF$ , $f = 10MHz$	39	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		4	

## SWITCHING CHARACTERISTICS (A PORT)<sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay xBx to xAx	1.5	5.7	1.5	4.8	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xAx	1.5	7.9	1.5	6.3	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xAx	1.5	8.3	2.2	7.4	ns
$t_{SK(o)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

### NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- Skew between any two outputs of the same package and switching in the same direction.

## SWITCHING CHARACTERISTICS (B PORT)<sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay xAx to xBx	1.5	4.7	1	4	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xBx	1.5	6.7	1.5	5.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xBx	1.5	7.1	1.5	6.6	ns
$t_{SK(o)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

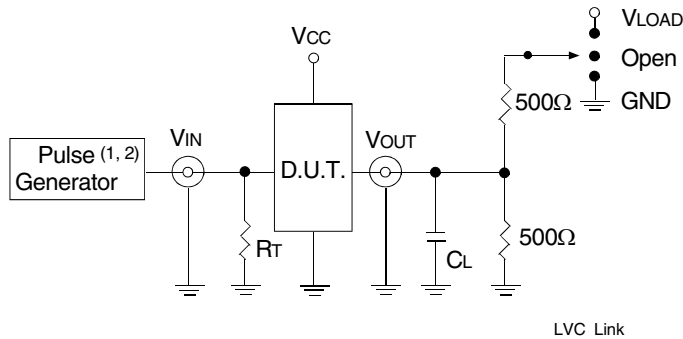
### NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> =2.7V	V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.

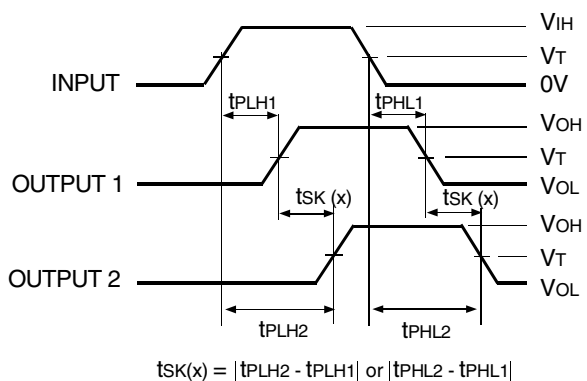
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>f</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>f</sub> ≤ 2ns.

### SWITCH POSITION

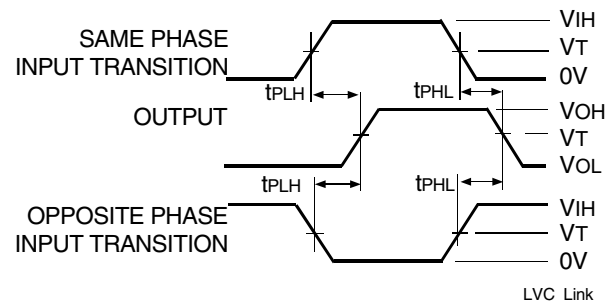
Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open



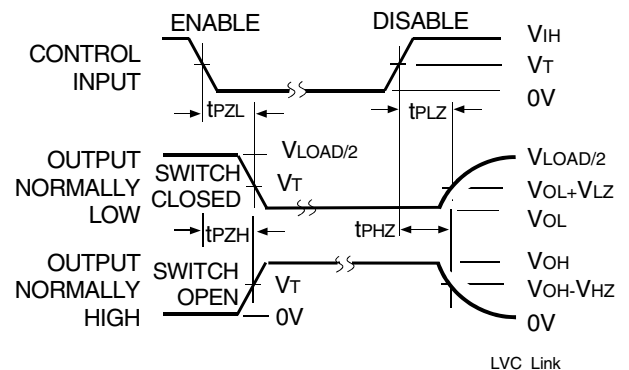
Output Skew - tsK(x)

#### NOTES:

1. For tsK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsK(b) OUTPUT1 and OUTPUT2 are in the same bank.



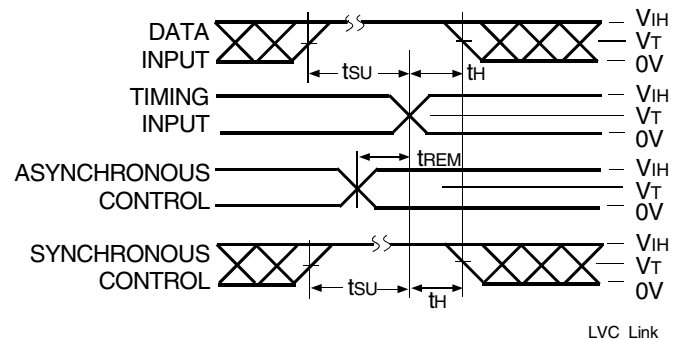
Propagation Delay



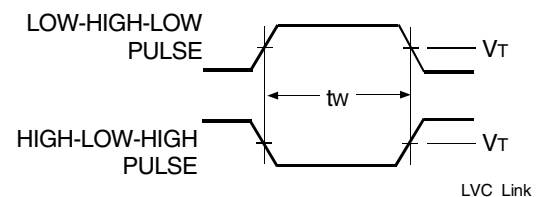
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

XX	LVC	X	XX	XXXX	XX	X		
Temp. Range	Bus-Hold	Family	Device Type	Package				
							Blank 8	Tube or Tray Tape and Reel
							PAG PFG	Thin Shrink Small Outline Package - Green Thin Very Small Outline Package - Green
							245A	16-Bit Bus Transceiver
							162	Double-Density with Resistors, $\pm 24\text{mA}$ (B Port) $\pm 12\text{mA}$ (A Port)
							H	Bus-hold
							74	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

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