

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### General Description

DA9132 is a power management IC (PMIC) suitable for supplying CPUs, GPUs, DDR memory rails in single in-line pin package (SIPP) modules, mobile, portable and consumer applications.

DA9132 integrates two single-phase buck converters, each phase requiring a small external 0.22  $\mu$ H inductor. Each buck is capable of delivering up to 3 A output current at a 0.3 V to 1.9 V output voltage range. The 2.8 V to 5.5 V input voltage range is suitable for a wide variety of low-voltage systems.

With remote sensing, the DA9132 guarantees the highest accuracy and supports multiple PCB routing scenarios without loss of performance.

The pass devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope-controlled rail activation.

The dynamic voltage control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via either a direct register write using the communication interface (I<sup>2</sup>C-compatible) or with a programmable input pin.

A configurable GPI allows multiple I<sup>2</sup>C address selection for multiple instances of DA9132 in the same application.

DA9132 has integrated over-temperature and over-current protection for increased system reliability, without the need for external sensing components.

### Key Features

- 2.8 V to 5.5 V input voltage
- 0.3 V to 1.9 V output voltage
- Up to 3 A output current per channel
- 4 MHz nominal switching frequency
- Dual-channel
- 220 nH inductor per channel
- 20  $\mu$ F output capacitor
- $\pm 1$  % output voltage accuracy (static)
- $\pm 5$  % load transient (dynamic)
- Programmable GPIOs
- Programmable soft-start
- I<sup>2</sup>C-compatible interface (FM+)
- Voltage, current, and temperature supervision
- 24-pin FCQFN package, wettable flanks (nom. 3.3 mm x 4.8 mm)
- 218 mm<sup>2</sup> total solution area
- -40 °C to +105 °C ambient temperature range
- AEC-Q100 Grade 2 qualified version also available for Automotive applications (DA9132-A)

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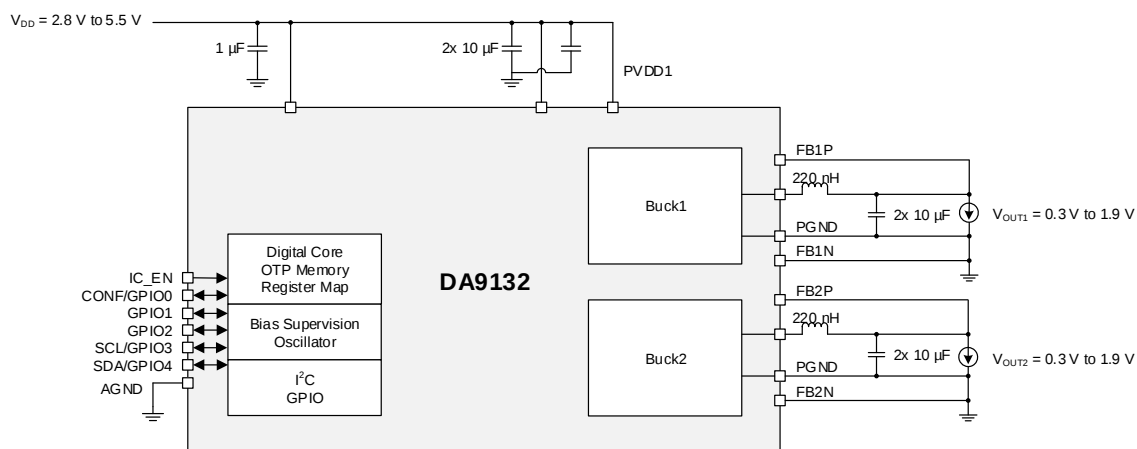
### Benefits

- High Efficiency buck converters deliver outstanding thermal performance
- Fully integrated switching FET's means no external FETs or Schottky diodes are required
- Remote sensing guarantees the highest accuracy and supports multiple PCB routing scenarios without loss of performance.
- Fully programmable soft-start limits the inrush current from the input to give a slope-controlled output voltage.
- Dynamic voltage control (DVC) enables adaptive adjustment of the device output voltage depending on the load. This increases efficiency when the downstream circuitry enters low power or idle mode, resulting in power savings.
- Configurable GPIOs support a range of features including I<sup>2</sup>C, DVC and Power-Good indicator.
- Optimized BoM cost and footprint: Each output requires a very small inductor and capacitor delivering parts and cost savings
- Cycle by cycle current limiting for superior over-current protection

### Applications

- Switches and routers
- Smart metering
- Industrial automation
- Wireless
- Consumer products
- SoC/FPGA based, high performance, automotive Electronic Control unit (ECU) requiring efficient, high current, power delivery
- SIPP modules (SoC, DRAM)

## System Diagrams



## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

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## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 1 Terms and Definitions

|       |                                                    |
|-------|----------------------------------------------------|
| ATE   | Automated Test Equipment                           |
| CPU   | Central Processing Unit                            |
| DDR   | Dual Data Rate                                     |
| DVC   | Dynamic Voltage Control                            |
| FET   | Field Effect Transistor                            |
| FM+   | Fast Mode Plus                                     |
| GBD   | Guaranteed By Design                               |
| GBQ   | Guaranteed By Qualification                        |
| GBSPC | Guaranteed By Statistical Process Characterization |
| GPI   | General Purpose Input                              |
| GPIO  | General Purpose Input/Output                       |
| GPU   | Graphics Processing Unit                           |
| IC    | Integrated Circuit                                 |
| HW    | Hardware                                           |
| OTP   | One Time Programmable                              |
| PCB   | Printed Circuit Board                              |
| PRS   | Product Requirements Specification                 |
| SCL   | Serial Clock                                       |
| SDA   | Serial Data                                        |
| SIPP  | Single In-Line Pin Package                         |
| SW    | Software                                           |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 2 Pinout

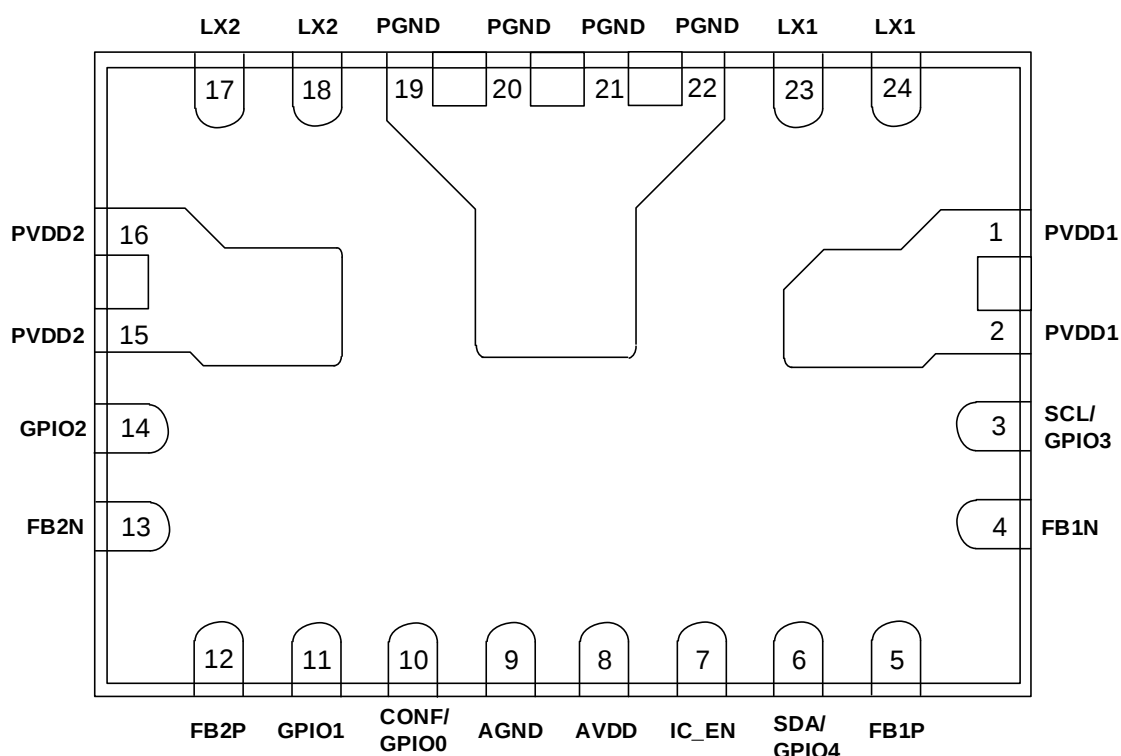


Figure 4: DA9132 Pinout Diagram (Bottom View)

Table 1: Pin Description

| Pin #          | Pin Name   | Type (Table 2) | Drive (mA) | Description               |
|----------------|------------|----------------|------------|---------------------------|
| 1, 2           | PVDD1      | PS             | 5000       | Supply for Ch1            |
| 3              | SCL/GPIO3  | DIO            | 15         | SCL                       |
| 4              | FB1N       | AI             | 10         | Negative feedback for Ch1 |
| 5              | FB1P       | AI             | 10         | Positive feedback for Ch1 |
| 6              | SDA/GPIO4  | DIO            | 15         | SDA                       |
| 7              | IC_EN      | DI             | 10         | IC enable.                |
| 8              | AVDD       | PS             | 10         | Analog supply             |
| 9              | AGND       | PS             | 10         | Analog ground             |
| 10             | CONF/GPIO0 | DIO            | 10         | GPIO                      |
| 11             | GPIO1      | DIO            | 10         | GPIO                      |
| 12             | FB2P       | AI             | 10         | Positive feedback for Ch2 |
| 13             | FB2N       | AI             | 10         | Negative feedback for Ch2 |
| 14             | GPIO2      | DIO            | 10         | GPIO                      |
| 15, 16         | PVDD2      | PS             | 5000       | Supply for Ch2            |
| 17, 18         | LX2        | AO             | 5000       | Buck output of Ch2        |
| 19, 20, 21, 22 | PGND       | PS             | 5000       | Power ground              |
| 23, 24         | LX1        | AO             | 5000       | Buck output of Ch1        |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 2: Pin Type Definition**

| Pin Type | Description          | Pin Type | Description   |
|----------|----------------------|----------|---------------|
| DI       | Digital input        | AI       | Analog input  |
| DIO      | Digital input/output | AO       | Analog output |
| PS       | Power supply         |          |               |

## 3 Characteristics

### 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 3: Absolute Maximum Ratings**

| Parameter        | Description           | Conditions | Min  | Max | Unit |
|------------------|-----------------------|------------|------|-----|------|
| T <sub>STG</sub> | Storage temperature   |            | -65  | 150 | °C   |
| T <sub>J</sub>   | Junction temperature  |            | -40  | 150 | °C   |
| V <sub>SYS</sub> | System supply voltage |            | -0.3 | 6.0 | V    |
| V <sub>PIN</sub> | Voltage on pins       |            | -0.3 | 6.0 | V    |

### 3.2 Recommended Operating Conditions

**Table 4: Recommended Operating Conditions**

| Parameter        | Description (Note 2)  | Conditions (Note 1) | Min  | Typ | Max                    | Unit |
|------------------|-----------------------|---------------------|------|-----|------------------------|------|
| V <sub>SYS</sub> | System supply voltage |                     | 2.8  |     | 5.5                    | V    |
| V <sub>PIN</sub> | Voltage on pins       |                     | -0.3 |     | V <sub>SYS</sub> + 0.3 | V    |
| T <sub>J</sub>   | Junction temperature  |                     | -40  |     | 125                    | °C   |
| T <sub>A</sub>   | Ambient temperature   |                     | -40  |     | 105                    | °C   |

**Note 1** Within the specified limits, a lifetime of 10 years is guaranteed. If operating outside of these recommended conditions, please consult with Dialog Semiconductor.

**Note 2** V<sub>SYS</sub>, V<sub>IN</sub>, P<sub>VDD</sub>, A<sub>VDD</sub> should be connected together. The pin names are different for routing purposes.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.3 Thermal Characteristics

#### 3.3.1 Thermal Ratings

Table 5: Package Ratings

| Parameter     | Description                          | Conditions  | Min | Typ   | Max | Unit |
|---------------|--------------------------------------|-------------|-----|-------|-----|------|
| $\theta_{JA}$ | Package thermal resistance           | Note 1      |     | 21.21 |     | °C/W |
| $\theta_{JB}$ | Thermal resistance junction to board | Note 1      |     | 12.37 |     | °C/W |
| $\theta_{JC}$ | Thermal resistance junction to case  | Without PCB |     | 32    |     | °C/W |

**Note 1** Obtained from package thermal simulations, JEDEC 2S2P four layer board (76.2 mm x 114 mm x 1.6 mm), 70  $\mu$ m (2 oz) copper thickness power planes, 35  $\mu$ m (1 oz) copper thickness signal layer traces, natural convection (still air), see Section 6.1.

#### 3.3.2 Power Dissipation

Table 6: Power Dissipation

| Parameter      | Description       | Conditions                     | Min  | Typ  | Max | Unit |
|----------------|-------------------|--------------------------------|------|------|-----|------|
| $P_{D\_Twarn}$ | Power dissipation | @105 °C ambient, $T_{J\_WARN}$ |      | 0.94 |     | W    |
| $P_{D\_Tcrit}$ | Power dissipation | @105 °C ambient, $T_{CRIT}$    | 1.41 | 1.65 |     | W    |
| $P_{D\_70}$    | Power dissipation | @70°C ambient                  |      | 2.43 |     | W    |

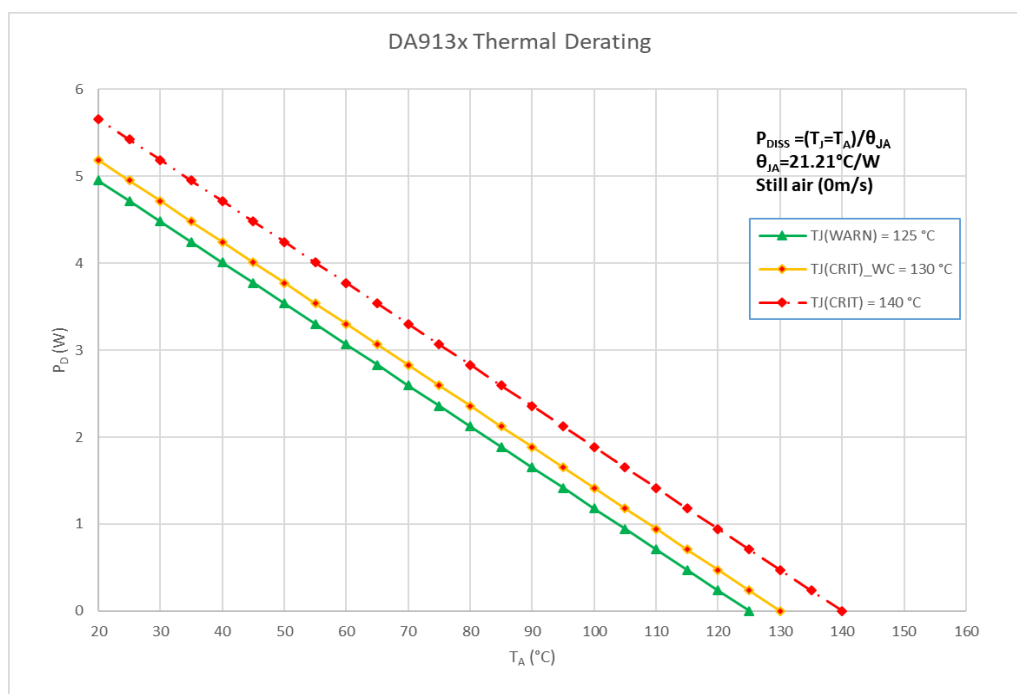


Figure 5: Power Derating Curve

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.3.3 ESD Characteristics

Table 7: ESD Characteristics

| Parameter            | Description                            | Conditions                 | Value | Unit |
|----------------------|----------------------------------------|----------------------------|-------|------|
| V <sub>ESD_HBM</sub> | ESD protection, human body model (HBM) |                            | 2     | kV   |
| V <sub>ESD_CDM</sub> | Maximum ESD protection                 | Charged device model (CDM) | 500   | V    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.4 Buck Characteristics

Unless otherwise noted, the following is valid for  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{SYS} = 2.8\text{ V}$  to  $5.5\text{ V}$ .

**Table 8: Buck Electrical Characteristics**

| Parameter                             | Description                                                                               | Conditions                                                                                                                                       | Min   | Typ  | Max   | Unit             |
|---------------------------------------|-------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------------------|
| <b>External Electrical Conditions</b> |                                                                                           |                                                                                                                                                  |       |      |       |                  |
| $V_{IN}$                              | Input voltage                                                                             | $V_{IN} = V_{SYS}$                                                                                                                               | 2.8   |      | 5.5   | V                |
| $C_{OUT}$                             | Output capacitance, including voltage and temperature coefficient                         |                                                                                                                                                  | -40 % | 20   | +30 % | $\mu\text{F}$    |
| $ESR_{COUT}$                          | Output capacitor series resistance                                                        | $f > 100\text{ kHz}$                                                                                                                             |       | 1    |       | $\text{m}\Omega$ |
| $L$                                   | Inductor value, including current and temperature dependence                              |                                                                                                                                                  | -50 % | 220  | +20 % | nH               |
| $DCR_L$                               | Inductor DC resistance                                                                    |                                                                                                                                                  |       | 8    | 13    | $\text{m}\Omega$ |
| <b>Electrical Performance</b>         |                                                                                           |                                                                                                                                                  |       |      |       |                  |
| $V_{OUT}$                             | Output voltage, configurable in 10 mV steps                                               | $I_{OUT} = 0\text{ mA}$ to $I_{MAX}$ at $25\text{ }^{\circ}\text{C}$ ambient<br>$2.8\text{ V} < V_{OUT} + 1\text{ V} < V_{IN} \leq 5.5\text{ V}$ | 0.3   |      | 1.9   | V                |
| $I_{LIM}$                             | Current limit, configurable per phase<br><a href="#">Note 1</a><br><a href="#">Note 2</a> | $CHx\_ILIM = 0100$                                                                                                                               | -20 % | 5    | +20 % | A                |
| $I_{MAX}$                             | Output current<br><a href="#">Note 3</a>                                                  | $V_{IN} \geq V_{OUT} + 1.0\text{ V}$                                                                                                             | 3     |      |       | A                |
| $V_{OUT\_ACC}$                        | Output voltage accuracy, including static line and load regulation                        | $V_{OUT} < 1\text{ V}$                                                                                                                           | -10   |      | 10    | mV               |
| $V_{OUT\_ACC}$                        | Output voltage accuracy, including static line and load regulation                        | $V_{OUT} \geq 1\text{ V}$                                                                                                                        | -1    |      | 1     | %                |
| $V_{THR\_PG\_HYS}$                    | Power-good voltage threshold hysteresis                                                   | $V_{OUT} = V_{THR\_PG\_DWN}$                                                                                                                     | 60    | 80   | 100   | mV               |
| $V_{THR\_PG\_DWN}$                    | Power-good voltage threshold for falling                                                  | $V_{OUT} = V_{BUCK}$                                                                                                                             | -160  | -130 | -80   | mV               |
| $V_{THR\_HV}$                         | High $V_{OUT}$ voltage threshold                                                          | $V_{OUT} = V_{BUCK}$                                                                                                                             | 100   | 150  | 200   | mV               |
| $V_{OUT\_TR\_LINE}$                   | Line transient response                                                                   | $V_{IN} = 3\text{ V}$ to $3.6\text{ V}$<br>$I_{OUT} = 0.5 * I_{MAX}$<br>$dt = 10\text{ }\mu\text{s}$                                             |       | 15   |       | mV               |
| $f_{SW}$                              | Switching frequency                                                                       |                                                                                                                                                  |       | 4    |       | MHz              |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Parameter         | Description                                                | Conditions                                                                                                                        | Min | Typ | Max | Unit |
|-------------------|------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{ON\_MIN}$     | Minimum turn-on pulse<br>0 % duty is also supported        |                                                                                                                                   | 5   | 7   | 11  | ns   |
| $t_{BUCK\_EN}$    | Turn-on time                                               | CHx_EN = high                                                                                                                     |     |     | 20  | μs   |
| $R_{PD}$          | Output pull-down resistance at the LX node, see CHx_PD_DIS | $V_{IN} = 3.7\text{ V}$<br>$V_{OUT} = 0.5\text{ V}$                                                                               | 145 | 150 | 161 | Ω    |
| $R_{ON\_PMOS}$    | On resistance of switching PMOS                            | $V_{IN} = 3.7\text{ V}$                                                                                                           | 17  | 25  | 37  | mΩ   |
| $R_{ON\_NMOS}$    | On resistance of switching NMOS                            | $V_{IN} = 3.7\text{ V}$                                                                                                           | 6   | 10  | 16  | mΩ   |
| <b>PWM Mode</b>   |                                                            |                                                                                                                                   |     |     |     |      |
| $I_{Q\_PWM}$      | Quiescent current                                          | $V_{IN} = 3.7\text{ V}$<br>No load                                                                                                |     | 16  |     | mA   |
| $\eta_{PWM}$      | Efficiency                                                 | $V_{IN} = 3.6\text{ V}$<br>$V_{OUT} = 1\text{ V}$<br>$I_{OUT} = 10\% (I_{MAX})$ to $80\% (I_{MAX})$                               |     | 85  |     | %    |
| <b>AUTO Mode</b>  |                                                            |                                                                                                                                   |     |     |     |      |
| $V_{OUT\_TR\_LD}$ | Load transient response                                    | $V_{OUT} = 1\text{ V}$<br>$I_{OUT} = 1.25$ to $3.75\text{ A}$ at $25^\circ\text{C}$ ambient<br>$dl/dt = 2.5\text{ A}/\mu\text{s}$ | -30 |     | 55  | mV   |
| <b>PFM Mode</b>   |                                                            |                                                                                                                                   |     |     |     |      |
| $I_{Q\_PFM}$      | Quiescent current in PFM                                   | 1-phase<br>$V_{IN} = 3.7\text{ V}$<br>No load<br>No switching                                                                     |     | 88  |     | μA   |
| $\eta_{PFM}$      | Efficiency                                                 | $V_{IN} = 3.6\text{ V}$<br>$V_{OUT} = 1\text{ V}$<br>$I_{OUT} = 10\text{ mA}$                                                     |     | 80  |     | %    |

**Note 1**  $t_{ON} > 40\text{ ns}$

**Note 2** The value is configured by OTP and should not be modified while the buck is active.

**Note 3** For short durations to meet peak current requirements,  $I_{OUT}$  can be operated at up to 10 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.5 Performance and Supervision Characteristics

Table 9: Electrical Characteristics

| Parameter                     | Description                            | Conditions                                                  | Min | Typ | Max  | Unit |
|-------------------------------|----------------------------------------|-------------------------------------------------------------|-----|-----|------|------|
| <b>Electrical Performance</b> |                                        |                                                             |     |     |      |      |
| V <sub>THR_POR</sub>          | Power-on-reset threshold               | Threshold for AVDD falling                                  |     | 2.1 | 2.25 | V    |
| V <sub>THR_POR_HYS</sub>      | Power-on-reset hysteresis              |                                                             |     | 200 |      | mV   |
| T <sub>WARN</sub>             | Thermal warning temperature threshold  |                                                             | 115 | 125 | 135  | °C   |
| T <sub>CRIT</sub>             | Thermal shutdown temperature threshold |                                                             | 130 | 140 | 150  | °C   |
| I <sub>IN_OFF</sub>           | Supply current                         | OFF state<br>T <sub>A</sub> = 27 °C<br>IC_EN = 0            |     | 0.1 | 1    | μA   |
| I <sub>IN_ON</sub>            | Supply current                         | ON state<br>T <sub>A</sub> = 27 °C<br>IC_EN = 1<br>Buck off | 5   | 10  | 20   | μA   |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.6 Digital I/O Characteristics

Table 10: Digital I/O Electrical Characteristics

| Parameter                     | Description                       | Conditions                                  | Min                 | Typ  | Max                 | Unit       |
|-------------------------------|-----------------------------------|---------------------------------------------|---------------------|------|---------------------|------------|
| <b>Electrical Performance</b> |                                   |                                             |                     |      |                     |            |
| $V_{IH\_EN}$                  | Input high voltage, IC enable     |                                             | 1.2                 |      | AVDD                | V          |
| $V_{IL\_EN}$                  | Input low voltage, IC enable      |                                             |                     |      | 0.4                 | V          |
| $t_{IC\_EN}$                  | IC enable time                    |                                             |                     |      | 1000                | $\mu$ s    |
| $V_{IH\_GPIO\_SCL\_SDA}$      | Input high voltage GPIO, SCL, SDA |                                             | 1.2                 |      | AVDD                | V          |
| $V_{IL\_GPIO\_SCL\_SDA}$      | Input low voltage GPIO, SCL, SDA  |                                             |                     |      | 0.4                 | V          |
| $V_{OH\_GPIO}$                | Output high voltage GPIO          | Push-pull mode<br>$I_{OUT} = 1$ mA          | $0.8 \cdot AV_{DD}$ |      | AVDD                | V          |
| $V_{OL\_GPIO}$                | Output low voltage GPIO           | Push-pull mode<br>$I_{OUT} = 1$ mA          |                     |      | $0.2 \cdot AV_{DD}$ | V          |
| $V_{OL\_SDA}$                 | Output low voltage SDA            | $I_{OUT} = 3$ mA                            |                     | 0.24 |                     | V          |
| $R_{PD}$                      | GPIO pull-down resistor           | $V_{SYS} = 3.7$ V<br><a href="#">Note 1</a> | 9                   | 15   | 24                  | k $\Omega$ |
| $R_{PU}$                      | GPIO pull-up resistor             | $V_{SYS} = 3.7$ V<br><a href="#">Note 1</a> | 28                  | 45   | 70                  | k $\Omega$ |

**Note 1** Resistance may have greater variation, depending on voltage and temperature.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.7 Timing Characteristics

**Table 11: I2C Electrical Characteristics**

| Parameter                     | Description                                      | Conditions            | Min          | Typ | Max  | Unit |
|-------------------------------|--------------------------------------------------|-----------------------|--------------|-----|------|------|
| <b>Electrical Performance</b> |                                                  |                       |              |     |      |      |
| t <sub>BUS</sub>              | Bus free time between a STOP and START condition |                       | 0.5          |     |      | μs   |
| C <sub>BUS</sub>              | Bus line capacitive load                         |                       |              |     | 150  | pF   |
| f <sub>SCL</sub>              | SCL clock frequency                              |                       | 20<br>Note 1 |     | 1000 | kHz  |
| t <sub>LO_SCL</sub>           | SCL low time                                     |                       | 0.5          |     |      | μs   |
| t <sub>HI_SCL</sub>           | SCL high time                                    |                       | 0.26         |     |      | μs   |
| t <sub>RISE</sub>             | SCL and SDA rise time                            | Requirement for input |              |     | 1000 | ns   |
| t <sub>FALL</sub>             | SCL and SDA fall time                            | Requirement for input |              |     | 300  | ns   |
| t <sub>SETUP_START</sub>      | Start condition setup time                       |                       | 0.26         |     |      | μs   |
| t <sub>HOLD_START</sub>       | Start condition hold time                        |                       | 0.26         |     |      | μs   |
| t <sub>SETUP_STOP</sub>       | Stop condition setup time                        |                       | 0.26         |     |      | μs   |
| t <sub>DATA</sub>             | Data valid time                                  |                       |              |     | 0.45 | μs   |
| t <sub>DATA_ACK</sub>         | Data valid acknowledge time                      |                       |              |     | 0.45 | μs   |
| t <sub>SETUP_DATA</sub>       | Data setup time                                  |                       | 50           |     |      | ns   |
| t <sub>HOLD_DATA</sub>        | Data hold time                                   |                       | 0            |     |      | ns   |

**Note 1** Minimum clock frequency is limited to 20 kHz if I2C\_TIMEOUT is enabled

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 3.8 Typical Performance

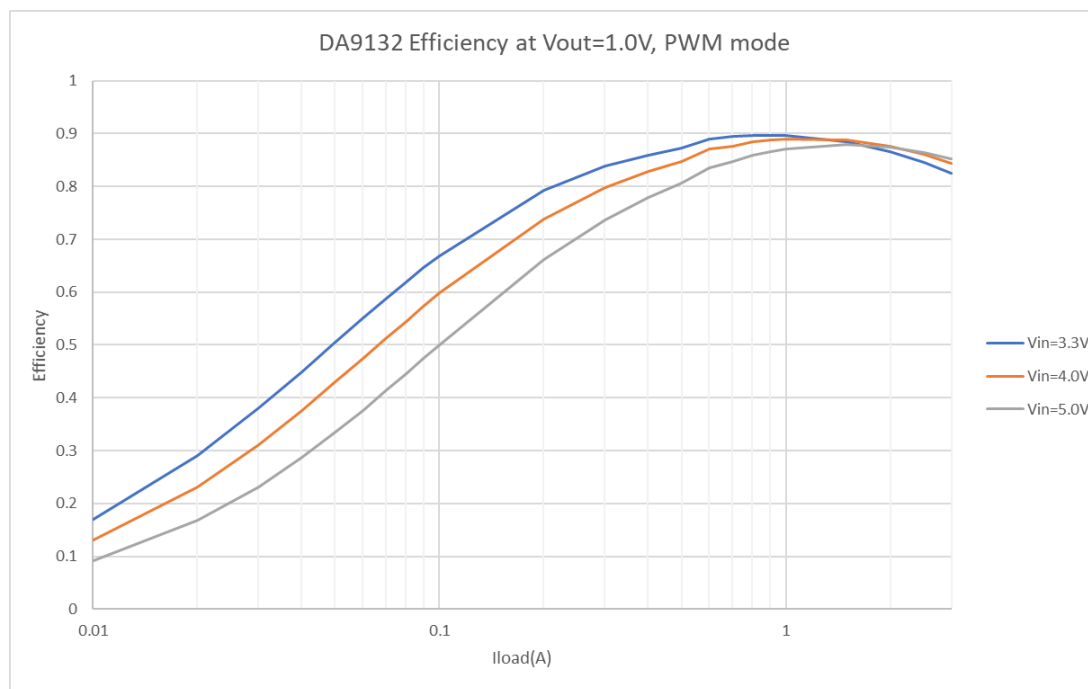


Figure 6: DA9132 Efficiency,  $V_{OUT} = 1.0 V$ , PWM Mode

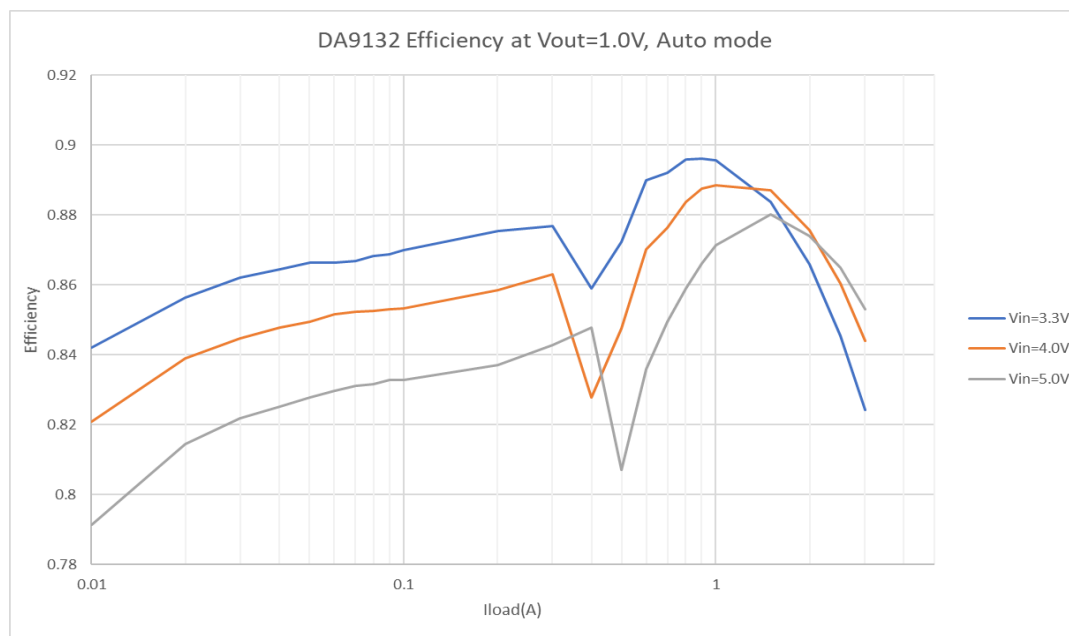


Figure 7: DA9132 Efficiency,  $V_{OUT} = 1.0 V$ , Auto Mode

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4 Functional Description

#### 4.1 DC-DC Buck Converter

DA9132 contains two buck converters, Buck1 and Buck2, each capable of delivering up to 3 A output current at a 0.3 V to 1.9 V output voltage range.

Buck1 and Buck2 have two voltage registers each. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way, different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored and a power-good signal indicates that the buck output voltage has reached a level higher than the  $V_{THR\_PG\_HYS}$  threshold. The power-good status is lost when the voltage drops below  $V_{THR\_PG\_DWN}$  or increases above  $V_{THR\_HV}$ . For each of the buck converters the status of the power-good indicator can be read back via I<sup>2</sup>C from the PG1 and PG2 status bits. It can be also individually assigned to any of the GPIOs by setting the GPIO mode registers to either PG1 or PG2 output.

The buck converters are capable of supporting DVC transitions that occur when:

- the active and selected A- or B-voltage is updated to a new target value
- the voltage selection is changed from the A- to B-voltage (or B- to A-voltage) using CH<x>\_VSEL

The DVC controller operates in pulse width modulation (PWM) mode with synchronous rectification.

The slew rate of the DVC transition is individually programmed for each buck converter at 10 mV per 8  $\mu$ s, 4  $\mu$ s, 2  $\mu$ s, 1  $\mu$ s, or 0.5  $\mu$ s in register bits CH1\_SR\_DVC and CH2\_SR\_DVC.

A pull-down resistor (typically 150  $\Omega$ ) for each phase is always activated unless it is disabled by setting register bits CH<x>\_PD\_DIS to 1.

##### 4.1.1 Switching Frequency

The buck switching frequency, nominally 4 MHz, can be tuned using register bit OSC\_TUNE. The internal 8 MHz oscillator frequency is tuned in  $\pm 160$  kHz steps. This impacts the buck converter frequency in steps of 80 kHz and helps to mitigate possible disturbances to other high frequency systems in the application.

##### 4.1.2 Operation Modes and Phase Selection

The buck converters can operate in PWM and PFM modes. The operating mode is selected using register bits CH1\_<A or B>\_MODE and CH2\_<A or B>\_MODE.

If the automatic operation mode is selected on CH1\_<A or B>\_MODE or CH2\_<A or B>\_MODE, the buck converters automatically change between synchronous PWM mode and PFM depending on the load current. This improves the efficiency across the whole range of output load currents.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4.1.3 Output Voltage Selection

The switching converter can be configured using the I<sup>2</sup>C interface.

For each buck converter two output voltages can be pre-configured in registers CH<x>\_A or B>\_VOUT. The output voltage can be selected by either toggling register bit CH<x>\_VSEL or by re-programming the selected voltage control register. Both changes will result in ramped voltage transitions. After being enabled, the buck converter will, by default, use the register settings in CH<x>\_A\_VOUT unless the output voltage selection is configured via the GPI port.

Registers CH<1 and 2>\_VMAX limit the output voltage that can be set for each of the respective buck converters.

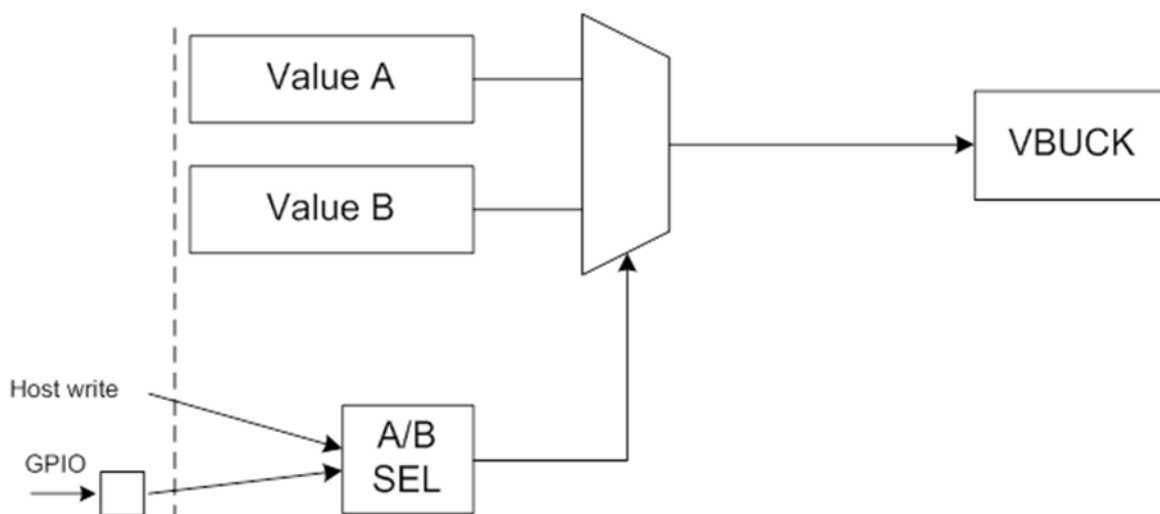


Figure 8: Buck Output Voltage Control Concept

### 4.1.4 Soft Start-Up and Shutdown

To limit in-rush current from V<sub>SY</sub>, the buck converters can perform a soft-start after being enabled. The start-up behavior is a compromise between acceptable inrush current from the battery and turn-on time. Individual ramp times can be configured for each buck converter in registers CH<1 and 2>\_SR\_STARTUP respectively. Rates higher than 20 mV/μs may produce overshoot during the start-up phase, so they should be considered carefully.

A ramped power down can be selected in register bits CH<1 and 2>\_SR\_SHDN. When no ramp is selected (immediate power down), the output node will be discharged only by the pull-down resistor, if enabled in registers CH<1 and 2>\_PD\_DIS.

### 4.1.5 Current Limit

The integrated current limit protects the power stages and external coil from excessive current. The buck current limit should be configured to at least 40 % higher than the required maximum output current.

When the current limit is reached, each buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using register M\_OC<x> in SYS\_MASK\_1. Register bits OC\_DVC\_MASK is used to mask over-current events during DVC transitions.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4.1.6 Resistive Divider

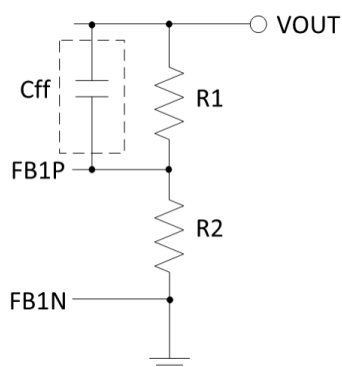
DA9132 can support output voltages higher than 1.9 V using an external resistive divider shown in Figure 9.

To calculate the output voltage with an external divider, use the following equation

$$V_{OUT} = V_{SEL} \times \left(1 + \frac{R1}{R2}\right)$$

**Equation 1**

$V_{SEL}$  is the device buck output voltage setting.



**Figure 9: Resistive Divider**

For example, to program the output voltage to 3.3 V, set  $V_{SEL}$  to 1.65 V, and use a 2.2 k $\Omega$  resistor for both R1 and R2, with  $C_{ff} = 1$  nF.

#### NOTE

The resistors need to be properly selected since the output voltage accuracy will be directly affected by any errors on the resistors. The voltage across FB1P and FB1N ( $V_{SEL}$ ) is guaranteed, but not the output voltage accuracy.



#### CAUTION

- The followings are important notes that need to be considered before using resistive divider on DA9132:
1. Please contact your region's Dialog representative when adopting the resistive divider technique. Dialog need to prepare a special OTP because incorrect OTP settings may result in a different output voltage than expected.
  2. The total resistance ( $R1+R2$ ) is less than 40 k $\Omega$ .
  3. It is recommended that the device is operated in PWM mode only.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

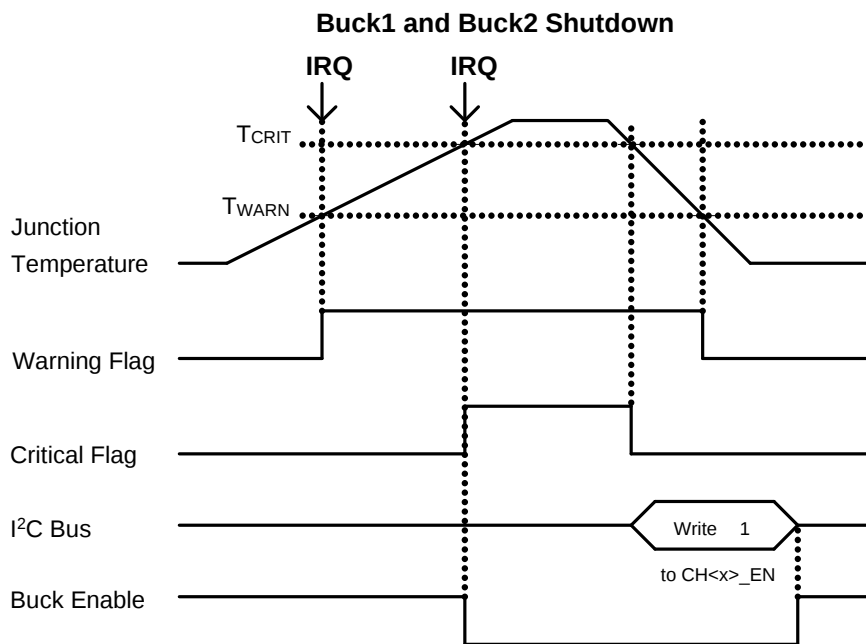
### 4.1.7 Thermal Protection

DA9132 is protected from internal overheating by thermal shutdown.

There are two kinds of flags concerning thermal protection, thermal warning and thermal critical. The warning flag is asserted when  $T_J > T_{WARN}$  and the critical flag is asserted when  $T_J > T_{CRIT}$ . When the critical flag is asserted, Buck1 and Buck2 are shut down immediately.

**Table 12: Thermal Protection Control Registers**

| Category  | Register name | Description                                                   |
|-----------|---------------|---------------------------------------------------------------|
| Status    | TEMP_WARN     | Asserted as long as the thermal warning threshold is reached  |
|           | TEMP_CRIT     | Asserted as long as the thermal shutdown threshold is reached |
| IRQ event | E_TEMP_WARN   | TEMP_WARN caused event                                        |
|           | E_TEMP_CRIT   | TEMP_CRIT caused event                                        |
| IRQ mask  | M_TEMP_WARN   | TEMP_WARN event IRQ mask                                      |
|           | M_TEMP_CRIT   | TEMP_CRIT event IRQ mask                                      |
|           | M_VR_HOT      | TEMP_WARN status IRQ mask                                     |



**Figure 10: Thermal Protection Operation**

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4.2 Internal Circuits

#### 4.2.1 IC\_EN/Chip Enable/Disable

IC\_EN is chip enable/disable control input. When IC\_EN = 0, all blocks except for low I<sub>Q</sub> POR are powered-down and buck output is pulled-down.

#### 4.2.2 nIRQ/Interrupt

The interrupt triggers events. Trigger conditions and control registers for each interrupt event are listed in Table 13.

Some of these events are categorized as fault events and affect device operation (for example, buck disable), see Section 4.1.7.

**Table 13: Interrupt List**

| Name                        | Polarity<br>(Note 1) | Trigger                                                                                             | IRQ Status Register | IRQ Mask Register | Deglitch Period        |
|-----------------------------|----------------------|-----------------------------------------------------------------------------------------------------|---------------------|-------------------|------------------------|
| Thermal warning (event)     | N                    | T <sub>J</sub> rising above T <sub>WARN</sub>                                                       | E_TEMP_WARN         | M_TEMP_WARN       | 0 s                    |
| Thermal critical (event)    | N                    | T <sub>J</sub> rising above T <sub>CRIT</sub>                                                       | E_TEMP_CRIT         | M_TEMP_CRIT       | 0 s                    |
| System good (event)         | P                    | Buck1 PG or Buck2 PG event                                                                          | E_SG                | M_SG              | 0 s                    |
| Buck1 power-good (event)    | P                    | Buck1 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage)                  | E_PG1               | M_PG1             | 0 s                    |
| Buck2 power-good (event)    | P                    | Buck2 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage)                  | E_PG2               | M_PG2             | 0 s                    |
| Buck1 over-voltage (event)  | N                    | Buck1 V <sub>OUT</sub> rising above over-voltage threshold (target voltage + 150 mV)                | E_OV1               | M_OV1             | Rise:8 μs<br>Fall:8 μs |
| Buck2 over-voltage (event)  | N                    | Buck2 V <sub>OUT</sub> rising above over-voltage threshold (target voltage + 150 mV)                | E_OV2               | M_OV2             | Rise:8 μs<br>Fall:8 μs |
| Buck1 under-voltage (event) | N                    | Buck1 V <sub>OUT</sub> falling below under-voltage threshold (target voltage - V <sub>TH_PG</sub> ) | E_UV1               | M_UV1             | 0 s                    |
| Buck2 under-voltage (event) | N                    | Buck2 V <sub>OUT</sub> falling below under-voltage threshold (target voltage - V <sub>TH_PG</sub> ) | E_UV2               | M_UV2             | 0 s                    |
| Buck1 over-current (event)  | N                    | Buck1 current rising above over-current threshold                                                   | E_OC1               | M_OC1             | 0 s                    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Name                                  | Polarity<br>(Note 1) | Trigger                                                                     | IRQ Status Register | IRQ Mask Register      | Deglintch Period                          |
|---------------------------------------|----------------------|-----------------------------------------------------------------------------|---------------------|------------------------|-------------------------------------------|
| Buck2 over-current (event)            | N                    | Buck2 current rising above over-current threshold                           | E_OC2               | M_OC2                  | 0 s                                       |
| Buck1 power-good (status)<br>(Note 2) | P                    | Buck1 $V_{OUT}$ is in power-good voltage range (not under- or over-voltage) | PG1                 | M_PG1_STAT<br>(Note 3) | 0 s                                       |
| Buck2 power-good (status)<br>(Note 2) | P                    | Buck2 $V_{OUT}$ is in power-good voltage range (not under- or over-voltage) | PG2                 | M_PG2_STAT<br>(Note 3) | 0 s                                       |
| System good (status)<br>(Note 2)      | P                    | Buck1 PG or Buck2 PG is active                                              | SG                  | M_SG_STAT<br>(Note 3)  | 0 s                                       |
| Thermal warning (status)<br>(Note 2)  | N                    | $T_J$ rising above $T_{WARN}$                                               | TEMP_WARN           | M_VR_HOT<br>(Note 3)   | 0 s                                       |
| GPIO0 change (event)                  | N                    | Detect GPIO0 change for active trigger<br>selected GPIO0_TRIG register      | E_GPIO0             | M_GPIO0                | 100 $\mu$ s/<br>1 ms/<br>10 ms/<br>100 ms |
| GPIO1 change (event)                  | N                    | Detect GPIO1 change for active trigger<br>selected GPIO1_TRIG register      | E_GPIO1             | M_GPIO1                |                                           |
| GPIO2 change (event)                  | N                    | Detect GPIO2 change for active trigger<br>selected GPIO2_TRIG register      | E_GPIO2             | M_GPIO2                |                                           |

**Note 1** Polarity at the source of the flag: P = active-high, N = active-low.  
General rule is: normal system state is high, and abnormal system state is low (for example, PG = high means power-good, TEMP\_CRIT = low when TEMP critical state).

**Note 2** Interrupt outputs the status as is. I<sup>2</sup>C write is not required for interrupt clear.

**Note 3** OTP load value defined by CONF pin setting if CONF\_EN = 1.

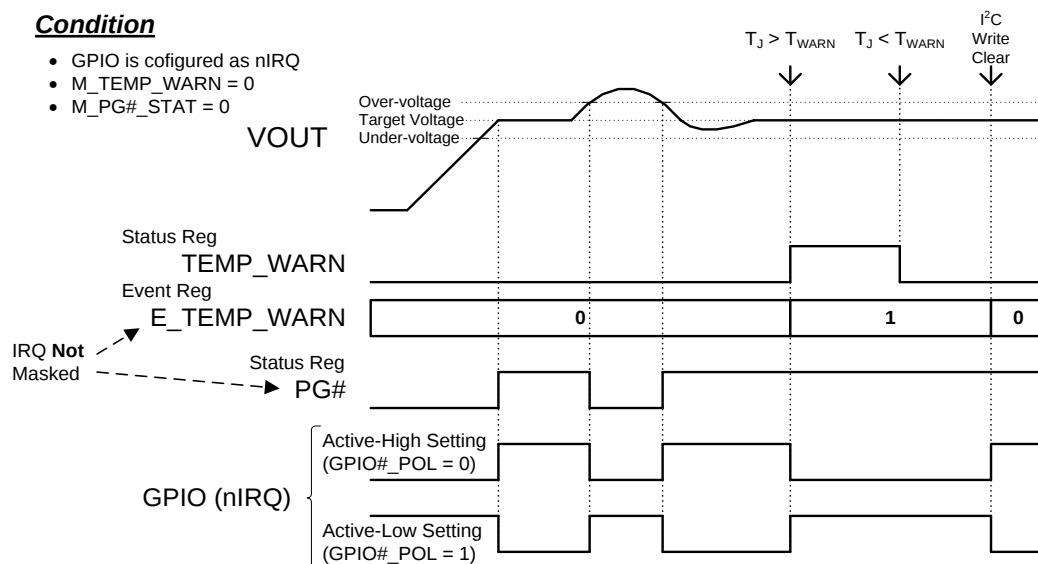
**Table 14: Interrupt Registers Except for Power-Good Status**

| Register | Description                                                                                                                                                       |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E_<name> | Read-only interrupt event register<br>0: No interrupt<br>1: Interrupt occurred<br><b>Cleared after being written to I<sup>2</sup>C. Set until IRQ is removed.</b> |
| M_<name> | Interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Event register (E_<name>) is updated.                                                  |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 15: Interrupt Registers for Power-Good, System Good, and Temp Warning Status**

| Register     | Description                                                                                                                                                                                          |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PG<x>        | Buck<x> power-good status. Asserted as long as the buck<x> output voltage is in range (under-voltage threshold < buck output voltage < over-voltage threshold)<br>0: Not power-good<br>1: Power-good |
| M_PG<x>_STAT | Power-good status interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Power-good status register (PG<x>) is updated                                                           |
| SG           | System good status<br>0: Not system good<br>1: System good                                                                                                                                           |
| M_SG_STAT    | System good status (SG) interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. System good status register (SG) is updated                                                       |
| TEMP_WARN    | Asserted as long as the thermal warning threshold ( $T_{WARN}$ ) is reached<br>0: Junction temperature is below $T_{WARN}$<br>1: Junction temperature is above $T_{WARN}$                            |
| M_VR_HOT     | Temperature warning status (TEMP_WARN) interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Temperature warning status register (TEMP_WARN) is updated                         |



**Figure 11: Interrupt Operation Example**

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### Condition

- GPIO is configured as nIRQ
- **M\_VR\_HOT = 0**
- M\_PG1\_STAT = 0
- M\_PG2\_STAT = 0

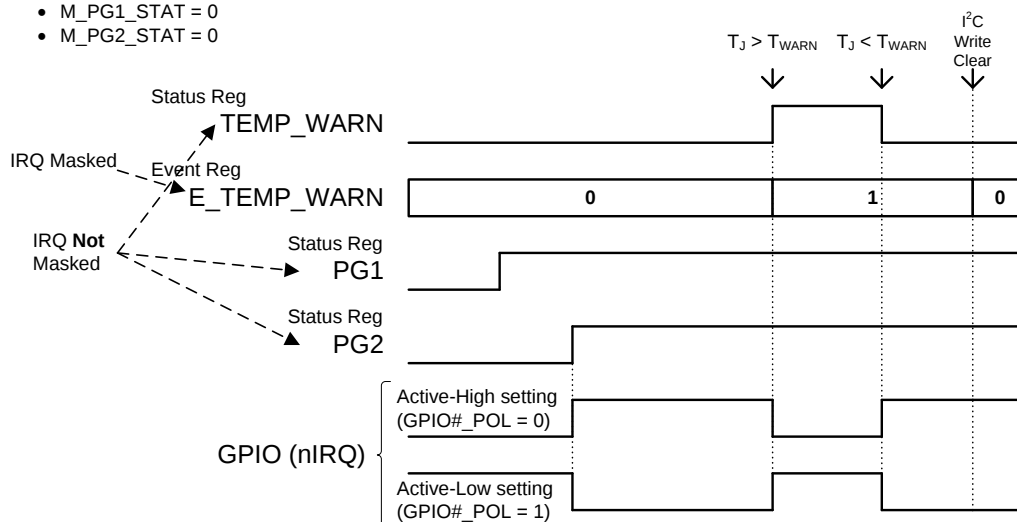


Figure 12: Interrupt Operation Example 2

### Condition

- GPIO is configured as nIRQ
- **M\_SG = 0**

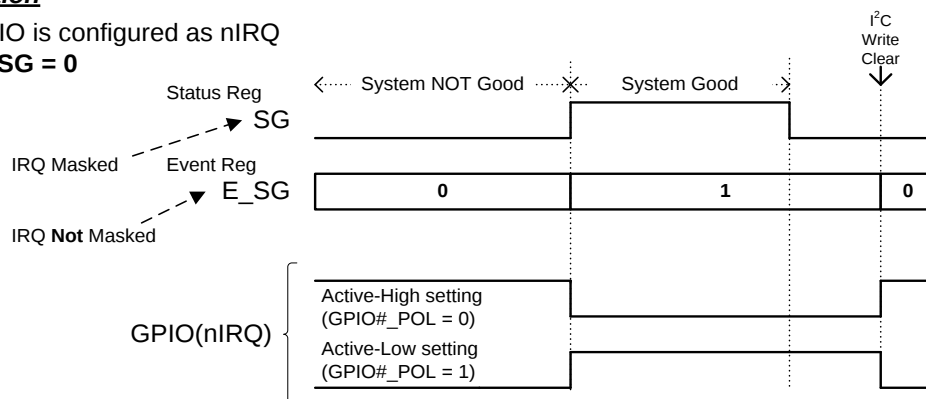


Figure 13: Interrupt Operation Example 3

### Condition

- GPIO is configured as nIRQ
- **M\_SG\_STAT = 0**

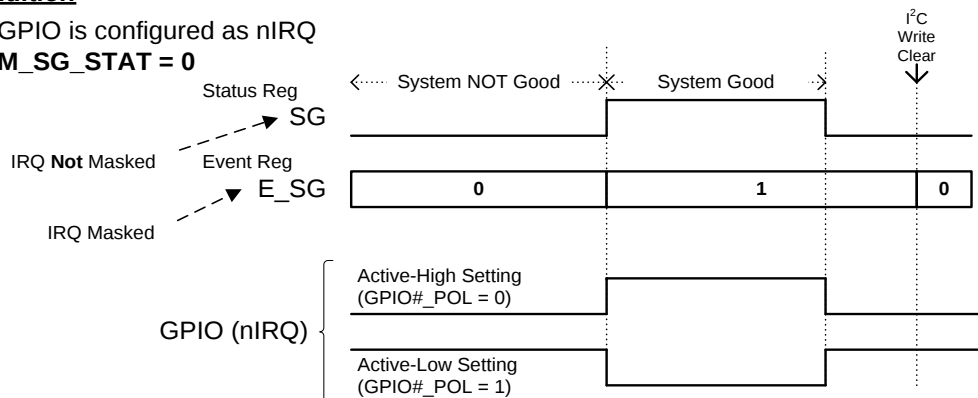


Figure 14: Interrupt Operation Example 4

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4.2.3 GPIO

#### 4.2.3.1 GPIO Pin Assignment

The DA9132 provides up to five GPIO pins, three if the I<sup>2</sup>C is enabled, see [Table 16](#). These registers are OTP programmable. When CONF\_EN = 1 GPIO0 can be used for chip configuration.

Any register settings for GPIO3 and GPIO4 are ignored and GPIO3 and GPIO4 function as SCL and SDA respectively if I2C\_EN = 1.

**Table 16: GPIO Pin Assignment**

| OTP Option |         | GPIO Pin       |       |       |               |               | Available GPIOs |
|------------|---------|----------------|-------|-------|---------------|---------------|-----------------|
| I2C_EN     | CONF_EN | CONF/<br>GPIO0 | GPIO1 | GPIO2 | SCL/<br>GPIO3 | SDA/<br>GPIO4 |                 |
| 1'b0       | 1'b0    | GPIO0          | GPIO1 | GPIO2 | GPIO3         | GPIO4         | 5               |
|            | 1'b1    | CONF           | GPIO1 | GPIO2 | GPIO3         | GPIO4         | 4               |
| 1'b1       | 1'b0    | GPIO0          | GPIO1 | GPIO2 | SCL           | SDA           | 3               |
|            | 1'b1    | CONF           | GPIO1 | GPIO2 | SCL           | SDA           | 2               |

#### 4.2.3.2 GPIO Function

The GPIOs pins are configurable as the following functions in register GPIO<x>\_MODE (x = 0 to 4):

- Buck1 enable input (EN1)
- Buck2 enable input (EN2)
- Buck1 and Buck2 enable input (EN1 & EN2)
- Buck1 DVC control input (DVC1)
- Buck2 DVC control input (DVC2)
- Buck1 and Buck2 DVC control input (DVC1 & DVC2)
- Buck1 and Buck2 OTP setting reload input (RELOAD)
- Buck1 power-good output (PG1)
- Buck2 power-good output (PG2)
- Buck1 and Buck2 power-good output (PG1 & PG2)
- System good output (SG)
- Interrupt output (nIRQ)

**Table 17: GPIO Function Configuration**

| GPIO<x>_MODE[3:0] | Function     | IO Condition |
|-------------------|--------------|--------------|
| 4'h0              | GPIO disable | HiZ          |
| 4'h1              | EN1          | In           |
| 4'h2              | EN2          | In           |
| 4'h3              | EN1 & EN2    | In           |
| 4'h4              | DVC1         | In           |
| 4'h5              | DVC2         | In           |
| 4'h6              | DVC1 & DVC2  | In           |
| 4'h7              | RELOAD       | In           |
| 4'h8              | PG1          | Out          |
| 4'h9              | PG2          | Out          |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| GPIO<x>_MODE[3:0] | Function   | IO Condition |
|-------------------|------------|--------------|
| 4'hA              | PG1 & PG2  | Out          |
| 4'hB              | SG         | Out          |
| 4'hC              | nIRQ       | Out          |
| 4'hD              | Reserved   | HiZ          |
| 4'hE              | Low level  | Out          |
| 4'hF              | High level | Out          |

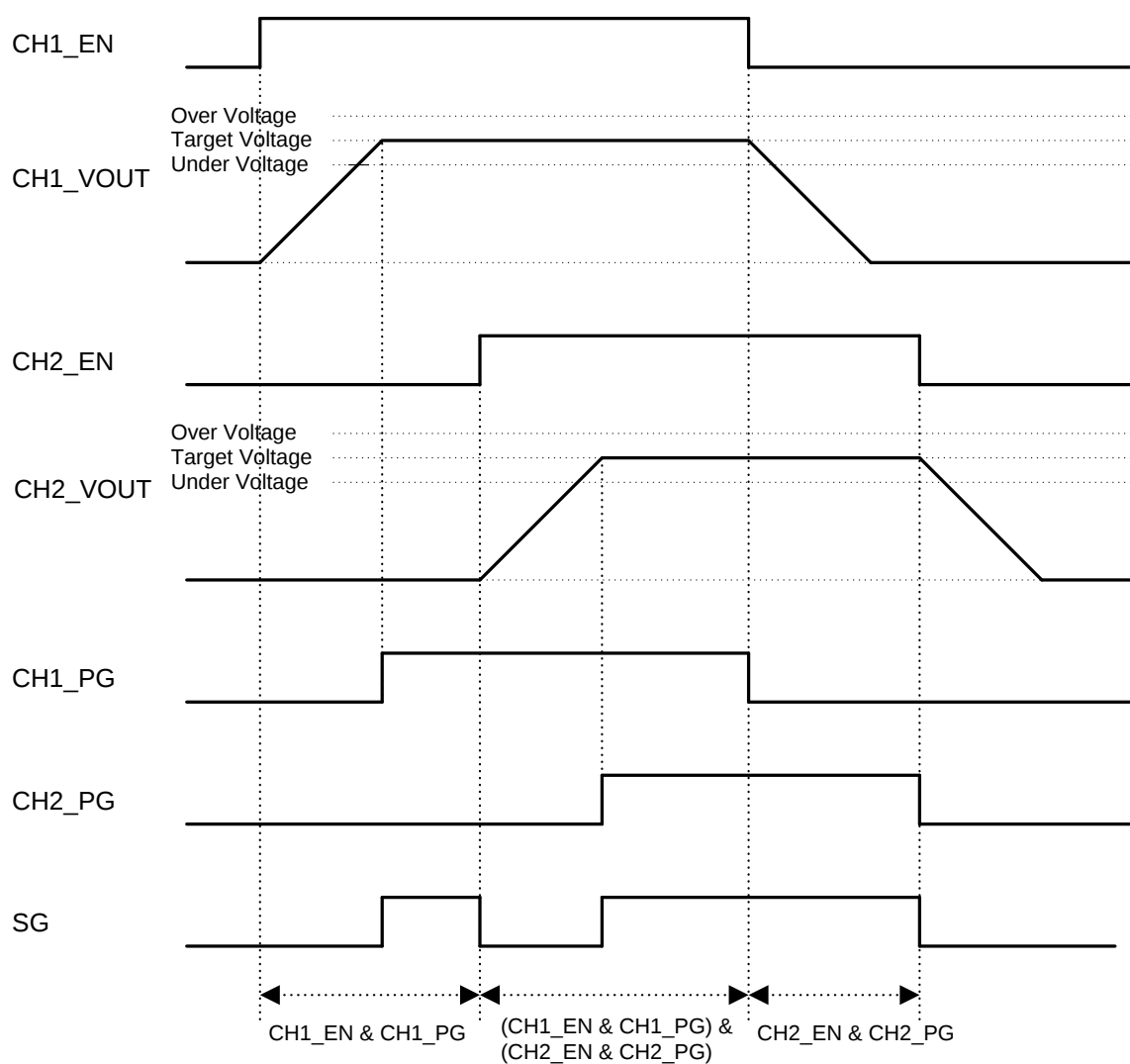


Figure 15: Power-Good (PG) and System Good (SG)

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 4.2.3.3 Chip Configuration Select (CONF)

GPIO0 functions as chip configuration select (CONF) input when CONF\_EN = 1.

Three different chip configurations can be selected according to the CONF pin level, whether it is HIGH, LOW, or Hi-Z. [Table 18](#) lists the device configurations can be modified if CONF\_EN = 1.

**Table 18: GPIO0-Configurable Registers when CONF\_EN = 1**

| Register Name      | Description                                |
|--------------------|--------------------------------------------|
| IF_SLAVE_ADDR[6:0] | I <sup>2</sup> C slave address             |
| CH1_A_MODE[1:0]    | CH1_A Operation mode select                |
| CH1_B_MODE[1:0]    | CH1_B Operation mode select                |
| CH1_VSEL           | CH1 output voltage and operation selection |
| CH1_EN             | CH1 enable                                 |
| CH1_A_VOUT[7:0]    | CH1 output voltage setting A               |
| CH1_B_VOUT[7:0]    | CH1 output voltage setting B               |
| CH2_A_MODE[1:0]    | CH2_A Operation mode select                |
| CH2_B_MODE[1:0]    | CH2_B Operation mode select                |
| CH2_VSEL           | CH2 output voltage and operation selection |
| CH2_EN             | CH2 enable                                 |
| CH2_A_VOUT[7:0]    | CH2 output voltage setting A               |
| CH2_B_VOUT[7:0]    | CH2 output voltage setting B               |
| M_PG1_STAT         | IRQ mask setting for CH1 power-good status |
| M_PG2_STAT         | IRQ mask setting for CH2 power-good status |
| M_SG_STAT          | IRQ mask setting for system good status    |
| M_VR_HOT           | IRQ mask setting for temp warning status   |
| CH1_EN_DLY[3:0]    | Delay setting for CH1 enable               |
| CH1_DIS_DLY[3:0]   | Delay setting for CH1 disable              |
| CH2_EN_DLY[3:0]    | Delay setting for CH2 enable               |
| CH2_DIS_DLY[3:0]   | Delay setting for CH2 disable              |
| GPIO1_MODE[3:0]    | GPIO1 mode setting                         |
| GPIO2_MODE[3:0]    | GPIO2 mode setting                         |
| GPIO1_OBUF         | GPIO1 output buffer select                 |
| GPIO2_OBUF         | GPIO2 output buffer select                 |
| GPIO1_TRIG[1:0]    | GPIO1 input trigger select                 |
| GPIO1_POL          | GPIO1 polarity select                      |
| GPIO1_PUPD         | GPIO1 pull-up/pull-down enable             |
| GPIO1_DEB[1:0]     | GPIO1 input debounce time setting          |
| GPIO1_DEB_RISE     | GPIO1 input debounce rising edge enable    |
| GPIO1_DEB_FALL     | GPIO1 input debounce falling edge enable   |
| GPIO2_TRIG[1:0]    | GPIO2 input trigger select                 |
| GPIO2_POL          | GPIO2 polarity select                      |
| GPIO2_PUPD         | GPIO2 pull-up/pull-down enable             |

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| Register Name  | Description                              |
|----------------|------------------------------------------|
| GPIO2_DEB[1:0] | GPIO2 input debounce time setting        |
| GPIO2_DEB_RISE | GPIO2 input debounce rising edge enable  |
| GPIO2_DEB_FALL | GPIO2 input debounce falling edge enable |

### 4.3 Operating Modes

#### 4.3.1 ON

DA9132 is ON when the IC\_EN port is higher than  $V_{IH\_EN}$  and the supply voltage is higher than  $V_{THR\_POR}$ . Once enabled, the host processor can start communicating with DA9132 using the control interface, after the  $t_{IC\_EN}$  delay.

#### 4.3.2 OFF

DA9132 is OFF when the IC\_EN port is lower than  $V_{IL\_EN}$ . In OFF, the bucks are always disabled and LX nodes are pulled down by (typically 150  $\Omega$ ) internal pull-down resistors.

### 4.4 I<sup>2</sup>C Communication

All features of DA9132 can be controlled with the I<sup>2</sup>C interface which is enabled or disabled in register I2C\_EN.

| I2C_EN | Description                                                                                                                            |
|--------|----------------------------------------------------------------------------------------------------------------------------------------|
| 0      | I <sup>2</sup> C disable: SCL/GPIO3 and SDA/GPIO4 pins can be used as GPIO                                                             |
| 1      | I <sup>2</sup> C enable: SCL/GPIO3 and SDA/GPIO4 pins are used as I <sup>2</sup> C clock input and I <sup>2</sup> C data input/output. |

GPIO3 functions as the I<sup>2</sup>C clock and GPIO4 carries all the power manager bidirectional I<sup>2</sup>C data. The I<sup>2</sup>C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 k $\Omega$  to 20 k $\Omega$ ). The standard frequency of the I<sup>2</sup>C bus is 1 MHz in fast-mode plus (FM+), 400 kHz in fast-mode, or 100 kHz in standard mode.

#### 4.4.1 I<sup>2</sup>C Protocol

All data is transmitted across the I<sup>2</sup>C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).

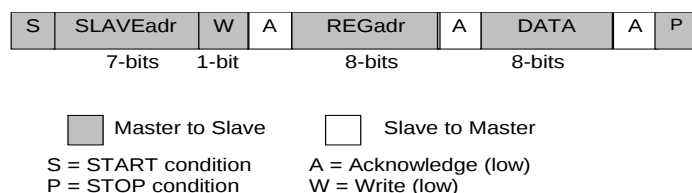
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**Figure 16: I²C START and STOP Condition Timing**

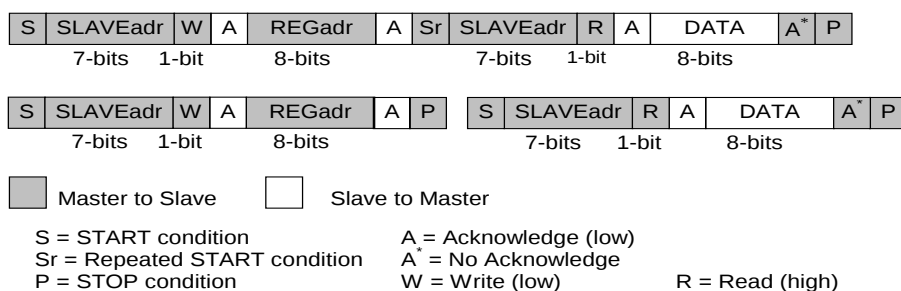
The I²C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in [Figure 17](#) and [Figure 18](#)).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9132 responds to all bytes with acknowledge (A), see [Figure 17](#).



**Figure 17: I²C Byte Write (SDA Line)**

When the host reads data from a register it first has to write to DA9132 with the target register address and then read from DA9132 with a repeated START, or alternatively a second START, condition. After receiving the data, the host sends no acknowledge (A\*) and terminates the transmission with a STOP condition, see [Figure 18](#).



**Figure 18: I²C Byte Read (SDA Line) Examples**

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### 5 Register Definitions

#### 5.1 Register Map

Table 19: Register Map

| Addr                 | Register                     | 7                | 6                | 5              | 4               | 3                | 2          | 1               | 0           |
|----------------------|------------------------------|------------------|------------------|----------------|-----------------|------------------|------------|-----------------|-------------|
| <b>System Module</b> |                              |                  |                  |                |                 |                  |            |                 |             |
| <b>System</b>        |                              |                  |                  |                |                 |                  |            |                 |             |
| 0x0001               | <a href="#">SYS_STATUS_0</a> | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | SG         | TEMP_CRIT       | TEMP_WARN   |
| 0x0002               | <a href="#">SYS_STATUS_1</a> | PG2              | OV2              | UV2            | OC2             | PG1              | OV1        | UV1             | OC1         |
| 0x0003               | <a href="#">SYS_STATUS_2</a> | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | GPIO2      | GPIO1           | GPIO0       |
| 0x0004               | <a href="#">SYS_EVENT_0</a>  | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | E_SG       | E_TEMP_CRIT     | E_TEMP_WARN |
| 0x0005               | <a href="#">SYS_EVENT_1</a>  | E_PG2            | E_OV2            | E_UV2          | E_OC2           | E_PG1            | E_OV1      | E_UV1           | E_OC1       |
| 0x0006               | <a href="#">SYS_EVENT_2</a>  | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | E_GPIO2    | E_GPIO1         | E_GPIO0     |
| 0x0007               | <a href="#">SYS_MASK_0</a>   | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | M_SG       | M_TEMP_CRIT     | M_TEMP_WARN |
| 0x0008               | <a href="#">SYS_MASK_1</a>   | M_PG2            | M_OV2            | M_UV2          | M_OC2           | M_PG1            | M_OV1      | M_UV1           | M_OC1       |
| 0x0009               | <a href="#">SYS_MASK_2</a>   | Reserved         | Reserved         | Reserved       | Reserved        | Reserved         | M_GPIO2    | M_GPIO1         | M_GPIO0     |
| 0x000A               | <a href="#">SYS_MASK_3</a>   | Reserved         | Reserved         | Reserved       | Reserved        | M_VR_HOT         | M_SG_STAT  | M_PG2_STAT      | M_PG1_STAT  |
| 0x000B               | <a href="#">SYS_CONFIG_0</a> | CH1_DIS_DLY<3:0> |                  |                |                 | CH1_EN_DLY<3:0>  |            |                 |             |
| 0x000C               | <a href="#">SYS_CONFIG_1</a> | CH2_DIS_DLY<3:0> |                  |                |                 | CH2_EN_DLY<3:0>  |            |                 |             |
| 0x000D               | <a href="#">SYS_CONFIG_2</a> | Reserved         | OC_LATCHOFF<1:0> |                | OC_DVC_MASK     | PG_DVC_MASK<1:0> |            | Reserved        | Reserved    |
| 0x000E               | <a href="#">SYS_CONFIG_3</a> | Reserved         | OSC_TUNE<2:0>    |                |                 | Reserved         | Reserved   | I2C_TIMEOUT     | Reserved    |
| 0x0010               | <a href="#">SYS_GPIO0_0</a>  | Reserved         | Reserved         | Reserved       | GPIO0_MODE<3:0> |                  |            |                 | GPIO0_OBUF  |
| 0x0011               | <a href="#">SYS_GPIO0_1</a>  | GPIO0_DEB_FALL   | GPIO0_DEB_RISE   | GPIO0_DEB<1:0> |                 | GPIO0_PUPD       | GPIO0_PO L | GPIO0_TRIG<1:0> |             |
| 0x0012               | <a href="#">SYS_GPIO1_0</a>  | Reserved         | Reserved         | Reserved       | GPIO1_MODE<3:0> |                  |            |                 | GPIO1_OBUF  |
| 0x0013               | <a href="#">SYS_GPIO1_1</a>  | GPIO1_DEB_FALL   | GPIO1_DEB_RISE   | GPIO1_DEB<1:0> |                 | GPIO1_PUPD       | GPIO1_PO L | GPIO1_TRIG<1:0> |             |
| 0x0014               | <a href="#">SYS_GPIO2_0</a>  | Reserved         | Reserved         | Reserved       | GPIO2_MODE<3:0> |                  |            |                 | GPIO2_OBUF  |
| 0x0015               | <a href="#">SYS_GPIO2_1</a>  | GPIO2_DEB_FALL   | GPIO2_DEB_RISE   | GPIO2_DEB<1:0> |                 | GPIO2_PUPD       | GPIO2_PO L | GPIO2_TRIG<1:0> |             |

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| Addr          | Register            | 7               | 6                   | 5        | 4            | 3                   | 2 | 1               | 0          |
|---------------|---------------------|-----------------|---------------------|----------|--------------|---------------------|---|-----------------|------------|
| Buck Control  |                     |                 |                     |          |              |                     |   |                 |            |
| Buck1         |                     |                 |                     |          |              |                     |   |                 |            |
| 0x0020        | BUCK_BUCK1_0        | Reserved        | CH1_SR_DVC_DWN<2:0> |          |              | CH1_SR_DVC_UP<2:0>  |   |                 | CH1_EN     |
| 0x0021        | BUCK_BUCK1_1        | Reserved        | CH1_SR_SHDN<2:0>    |          |              | CH1_SR_STARTUP<2:0> |   |                 | CH1_PD_DIS |
| 0x0022        | BUCK_BUCK1_2        | Reserved        | Reserved            | Reserved | Reserved     | CH1_ILIM<3:0>       |   |                 |            |
| 0x0023        | BUCK_BUCK1_3        | CH1_VMAX<7:0>   |                     |          |              |                     |   |                 |            |
| 0x0024        | BUCK_BUCK1_4        | Reserved        | Reserved            | Reserved | CH1_VSE<br>L | CH1_B_MODE<1:0>     |   | CH1_A_MODE<1:0> |            |
| 0x0025        | BUCK_BUCK1_5        | CH1_A_VOUT<7:0> |                     |          |              |                     |   |                 |            |
| 0x0026        | BUCK_BUCK1_6        | CH1_B_VOUT<7:0> |                     |          |              |                     |   |                 |            |
| Buck2         |                     |                 |                     |          |              |                     |   |                 |            |
| 0x0028        | BUCK_BUCK2_0        | Reserved        | CH2_SR_DVC_DWN<2:0> |          |              | CH2_SR_DVC_UP<2:0>  |   |                 | CH2_EN     |
| 0x0029        | BUCK_BUCK2_1        | Reserved        | CH2_SR_SHDN<2:0>    |          |              | CH2_SR_STARTUP<2:0> |   |                 | CH2_PD_DIS |
| 0x002A        | BUCK_BUCK2_2        | Reserved        | Reserved            | Reserved | Reserved     | CH2_ILIM<3:0>       |   |                 |            |
| 0x002B        | BUCK_BUCK2_3        | CH2_VMAX<7:0>   |                     |          |              |                     |   |                 |            |
| 0x002C        | BUCK_BUCK2_4        | Reserved        | Reserved            | Reserved | CH2_VSE<br>L | CH2_B_MODE<1:0>     |   | CH2_A_MODE<1:0> |            |
| 0x002D        | BUCK_BUCK1_5        | CH2_A_VOUT<7:0> |                     |          |              |                     |   |                 |            |
| 0x002E        | BUCK_BUCK1_6        | CH2_B_VOUT<7:0> |                     |          |              |                     |   |                 |            |
| Serialization |                     |                 |                     |          |              |                     |   |                 |            |
| 0x0048        | OTP_DEVICE_ID       | DEV_ID<7:0>     |                     |          |              |                     |   |                 |            |
| 0x0049        | OTP_VARIANT_ID      | MRC<3:0>        |                     |          |              | VRC<3:0>            |   |                 |            |
| 0x004A        | OTP_CUSTOMER_I<br>D | CUST_ID<7:0>    |                     |          |              |                     |   |                 |            |
| 0x004B        | OTP_CONFIG_ID       | CONFIG_REV<7:0> |                     |          |              |                     |   |                 |            |

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### 5.1.1 System

**Table 20: SYS\_STATUS\_0 (0x0001)**

| Bit | Type | Symbol    | Description                                                            |
|-----|------|-----------|------------------------------------------------------------------------|
| [2] | R    | SG        | Asserted as long as the output voltage of the enabled buck is in range |
| [1] | R    | TEMP_CRIT | Asserted whilst the thermal shutdown threshold is exceeded             |
| [0] | R    | TEMP_WARN | Asserted whilst the thermal warning threshold is exceeded              |

**Table 21: SYS\_STATUS\_1 (0x0002)**

| Bit | Type | Symbol | Description                                      |
|-----|------|--------|--------------------------------------------------|
| [7] | R    | PG2    | Asserted whilst Buck2 output voltage is in range |
| [6] | R    | OV2    | Asserted whilst Buck2 output is over-voltage     |
| [5] | R    | UV2    | Asserted whilst Buck2 output is under-voltage    |
| [4] | R    | OC2    | Asserted whilst Buck2 output is over-current     |
| [3] | R    | PG1    | Asserted whilst Buck1 output voltage is in range |
| [2] | R    | OV1    | Asserted whilst Buck1 output is over-voltage     |
| [1] | R    | UV1    | Asserted whilst Buck1 output is under-voltage    |
| [0] | R    | OC1    | Asserted whilst Buck1 output is over-current     |

**Table 22: SYS\_STATUS\_2 (0x0003)**

| Bit | Type | Symbol | Description  |
|-----|------|--------|--------------|
| [2] | R    | GPIO2  | GPIO2 status |
| [1] | R    | GPIO1  | GPIO1 status |
| [0] | R    | GPIO0  | GPIO0 status |

**Table 23: SYS\_EVENT\_0 (0x0004)**

| Bit | Type | Symbol      | Description                                                                          |
|-----|------|-------------|--------------------------------------------------------------------------------------|
| [2] | R    | E_SG        | SG caused event. Write 1 to clear this bit after the event source has been released. |
| [1] | R    | E_TEMP_CRIT | TEMP_CRIT event. Write 1 to clear this bit after the event source has been released. |
| [0] | R    | E_TEMP_WARN | TEMP_WARN event. Write 1 to clear this bit after the event source has been released. |

**Table 24: SYS\_EVENT\_1 (0x0005)**

| Bit | Type | Symbol | Description                                                                           |
|-----|------|--------|---------------------------------------------------------------------------------------|
| [7] | RW   | E_PG2  | PG2 caused event. Write 1 to clear this bit after the event source has been released. |
| [6] | RW   | E_OV2  | OV2 caused event. Write 1 to clear this bit after the event source has been released. |
| [5] | RW   | E_UV2  | UV2 caused event. Write 1 to clear this bit after the event source has been released. |
| [4] | RW   | E_OC2  | OC2 caused event. Write 1 to clear this bit after the event source has been released. |

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| Bit | Type | Symbol | Description                                                                           |
|-----|------|--------|---------------------------------------------------------------------------------------|
| [3] | RW   | E_PG1  | PG1 caused event. Write 1 to clear this bit after the event source has been released. |
| [2] | RW   | E_OV1  | OV1 caused event. Write 1 to clear this bit after the event source has been released. |
| [1] | RW   | E_UV1  | UV1 caused event. Write 1 to clear this bit after the event source has been released. |
| [0] | RW   | E_OC1  | OC1 caused event. Write 1 to clear this bit after the event source has been released. |

**Table 25: SYS\_EVENT\_2 (0x0006)**

| Bit | Type | Symbol  | Description                                                                      |
|-----|------|---------|----------------------------------------------------------------------------------|
| [2] | RW   | E_GPIO2 | GPIO2 event. Write 1 to clear this bit after the event source has been released. |
| [1] | RW   | E_GPIO1 | GPIO1 event. Write 1 to clear this bit after the event source has been released. |
| [0] | RW   | E_GPIO0 | GPIO0 event. Write 1 to clear this bit after the event source has been released. |

**Table 26: SYS\_MASK\_0 (0x0007)**

| Bit | Type | Symbol      | Description        |
|-----|------|-------------|--------------------|
| [2] | RW   | M_SG        | SG IRQ mask        |
| [1] | RW   | M_TEMP_CRIT | TEMP_CRIT IRQ mask |
| [0] | RW   | M_TEMP_WARN | TEMP_WARN IRQ mask |

**Table 27: SYS\_MASK\_1 (0x0008)**

| Bit | Type | Symbol | Description        |
|-----|------|--------|--------------------|
| [7] | RW   | M_PG2  | PG2 event IRQ mask |
| [6] | RW   | M_OV2  | OV2 event IRQ mask |
| [5] | RW   | M_UV2  | UV2 event IRQ mask |
| [4] | RW   | M_OC2  | OC2 event IRQ mask |
| [3] | RW   | M_PG1  | PG1 event IRQ mask |
| [2] | RW   | M_OV1  | OV1 event IRQ mask |
| [1] | RW   | M_UV1  | UV1 event IRQ mask |
| [0] | RW   | M_OC1  | OC1 event IRQ mask |

**Table 28: SYS\_MASK\_2 (0x0009)**

| Bit | Type | Symbol  | Description    |
|-----|------|---------|----------------|
| [2] | RW   | M_GPIO2 | GPIO2 IRQ mask |
| [1] | RW   | M_GPIO1 | GPIO1 IRQ mask |
| [0] | RW   | M_GPIO0 | GPIO0 IRQ mask |

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**Table 29: SYS\_MASK\_3 (0x000A)**

| Bit | Type | Symbol     | Description                                                                                                                        |
|-----|------|------------|------------------------------------------------------------------------------------------------------------------------------------|
| [3] | RW   | M_VR_HOT   | Temp warning status IRQ mask. Initial value is determined by CONF pin setting at the start-up if CONF_EN = 1, see Section 4.2.3.3. |
| [2] | RW   | M_SG_STAT  | SG status IRQ mask. Initial value is determined by CONF pin setting at the start-up if CONF_EN = 1, see Section 4.2.3.3.           |
| [1] | RW   | M_PG2_STAT | PG2 status IRQ mask. Initial value is determined by CONF pin setting at the start-up if CONF_EN = 1, see Section 4.2.3.3.          |
| [0] | RW   | M_PG1_STAT | PG1 status IRQ mask. Initial value is determined by CONF pin setting at the start-up if CONF_EN = 1, see Section 4.2.3.3.          |

**Table 30: SYS\_CONFIG\_0 (0x000B)**

| Bit   | Type | Symbol      | Description                                                                                                                                                             |         |
|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| [7:4] | RW   | CH1_DIS_DLY | Delay for CH1 disable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |         |
|       |      |             | <b>Value</b> <b>Description</b>                                                                                                                                         |         |
|       |      |             | 0x00                                                                                                                                                                    | 0       |
|       |      |             | 0x01                                                                                                                                                                    | 1.0 ms  |
|       |      |             | 0x02                                                                                                                                                                    | 2.0 ms  |
|       |      |             | 0x03                                                                                                                                                                    | 3.0 ms  |
|       |      |             | 0x04                                                                                                                                                                    | 4.0 ms  |
|       |      |             | 0x05                                                                                                                                                                    | 5.0 ms  |
|       |      |             | 0x06                                                                                                                                                                    | 6.0 ms  |
|       |      |             | 0x07                                                                                                                                                                    | 7.0 ms  |
|       |      |             | 0x08                                                                                                                                                                    | 8.0 ms  |
|       |      |             | 0x09                                                                                                                                                                    | 9.0 ms  |
|       |      |             | 0x0A                                                                                                                                                                    | 10.0 ms |
|       |      |             | 0x0B                                                                                                                                                                    | 11.0 ms |
|       |      |             | 0x0C                                                                                                                                                                    | 12.0 ms |
|       |      |             | 0x0D                                                                                                                                                                    | 13.0 ms |
|       |      |             | 0x0E                                                                                                                                                                    | 14.0 ms |
|       |      |             | 0x0F                                                                                                                                                                    | 15.0 ms |
| [3:0] | RW   | CH1_EN_DLY  | Delay for CH1 enable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1  |         |
|       |      |             | <b>Value</b> <b>Description</b>                                                                                                                                         |         |
|       |      |             | 0x00                                                                                                                                                                    | 0       |
|       |      |             | 0x01                                                                                                                                                                    | 0.5 ms  |
|       |      |             | 0x02                                                                                                                                                                    | 1.0 ms  |
|       |      |             | 0x03                                                                                                                                                                    | 1.5 ms  |

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| Bit | Type | Symbol | Description |
|-----|------|--------|-------------|
|     |      |        | 0x4 2.0 ms  |
|     |      |        | 0x5 2.5 ms  |
|     |      |        | 0x6 3.0 ms  |
|     |      |        | 0x7 3.5 ms  |
|     |      |        | 0x8 4.0 ms  |
|     |      |        | 0x9 4.5 ms  |
|     |      |        | 0xA 5.0 ms  |
|     |      |        | 0xB 5.5 ms  |
|     |      |        | 0xC 6.0 ms  |
|     |      |        | 0xD 6.5 ms  |
|     |      |        | 0xE 7.0 ms  |
|     |      |        | 0xF 7.5 ms  |

**Table 31: SYS\_CONFIG\_1 (0x000C)**

| Bit   | Type        | Symbol      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|-------|-------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|-----|---|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|
| [7:4] | RW          | CH2_DIS_DLY | Delay for CH2 disable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>0</td></tr><tr><td>0x1</td><td>1.0 ms</td></tr><tr><td>0x2</td><td>2.0 ms</td></tr><tr><td>0x3</td><td>3.0 ms</td></tr><tr><td>0x4</td><td>4.0 ms</td></tr><tr><td>0x5</td><td>5.0 ms</td></tr><tr><td>0x6</td><td>6.0 ms</td></tr><tr><td>0x7</td><td>7.0 ms</td></tr><tr><td>0x8</td><td>8.0 ms</td></tr><tr><td>0x9</td><td>9.0 ms</td></tr><tr><td>0xA</td><td>10.0 ms</td></tr><tr><td>0xB</td><td>11.0 ms</td></tr><tr><td>0xC</td><td>12.0 ms</td></tr><tr><td>0xD</td><td>13.0 ms</td></tr><tr><td>0xE</td><td>14.0 ms</td></tr><tr><td>0xF</td><td>15.0 ms</td></tr></table> | Value       | Description | 0x0 | 0 | 0x1 | 1.0 ms | 0x2 | 2.0 ms | 0x3 | 3.0 ms | 0x4 | 4.0 ms | 0x5 | 5.0 ms | 0x6 | 6.0 ms | 0x7 | 7.0 ms | 0x8 | 8.0 ms | 0x9 | 9.0 ms | 0xA | 10.0 ms | 0xB | 11.0 ms | 0xC | 12.0 ms | 0xD | 13.0 ms | 0xE | 14.0 ms | 0xF | 15.0 ms |
|       |             |             | Value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Description |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0           |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 2.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 3.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 4.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 5.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 6.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 7.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 8.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0x9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 9.0 ms      |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0xA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 10.0 ms     |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0xB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 11.0 ms     |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0xC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 12.0 ms     |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | 0xD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 13.0 ms     |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xE   | 14.0 ms     |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xF   | 15.0 ms     |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| [3:0] | RW          | CH2_EN_DLY  | Delay for CH2 enable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|       |             |             | <table><tr><th>Value</th><th>Description</th></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Value       | Description |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| Value | Description |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Bit | Type | Symbol | Description |
|-----|------|--------|-------------|
|     |      |        | 0x0 0       |
|     |      |        | 0x1 0.5 ms  |
|     |      |        | 0x2 1.0 ms  |
|     |      |        | 0x3 1.5 ms  |
|     |      |        | 0x4 2.0 ms  |
|     |      |        | 0x5 2.5 ms  |
|     |      |        | 0x6 3.0 ms  |
|     |      |        | 0x7 3.5 ms  |
|     |      |        | 0x8 4.0 ms  |
|     |      |        | 0x9 4.5 ms  |
|     |      |        | 0xA 5.0 ms  |
|     |      |        | 0xB 5.5 ms  |
|     |      |        | 0xC 6.0 ms  |
|     |      |        | 0xD 6.5 ms  |
|     |      |        | 0xE 7.0 ms  |
|     |      |        | 0xF 7.5 ms  |

Table 32: SYS\_CONFIG\_2 (0x000D)

| Bit                                  | Type | Symbol      | Description                                                                                                                                     |                                 |
|--------------------------------------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|
| [6:5]                                | RW   | OC_LATCHOFF | Over-current latch-off setting. BUCK shut-down after OCP for 8 $\mu$ s/1 ms/3 ms unless disable setting. IRQ is generated unless IRQ is masked. |                                 |
|                                      |      |             | <b>Value</b> <b>Description</b>                                                                                                                 |                                 |
|                                      |      |             | 0x0Latch off disable                                                                                                                            |                                 |
|                                      |      |             | 0x1Latch off after 8 $\mu$ s of OCP signal                                                                                                      |                                 |
|                                      |      |             | 0x2Latch off after 1 ms of OCP signal                                                                                                           |                                 |
| [4]                                  | RW   | OC_DVC_MASK | 0x3Latch off after 3 ms of OCP signal                                                                                                           |                                 |
|                                      |      |             | Over-current event (IRQ and latch-off feature) mask during DVC ramp-up and ramp-down for both CH1 and CH2                                       |                                 |
|                                      |      |             | Power-good mask during DVC for both CH1 and CH2                                                                                                 |                                 |
|                                      |      |             |                                                                                                                                                 | <b>Value</b> <b>Description</b> |
|                                      |      |             |                                                                                                                                                 | 0x0No mask                      |
| 0x1Mask as not power-good during DVC |      |             |                                                                                                                                                 |                                 |
| 0x2Mask as power-good during DVC     |      |             |                                                                                                                                                 |                                 |
| [3:2]                                | RW   | PG_DVC_MASK | 0x3Reserved                                                                                                                                     |                                 |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 33: SYS\_CONFIG\_3 (0x000E)**

| Bit   | Type | Symbol      | Description                                                               |
|-------|------|-------------|---------------------------------------------------------------------------|
| [6:4] | RW   | OSC_TUNE    | Tune oscillator frequency, tuned frequency = Current + OSC_TUNE * 160 kHz |
|       |      |             | <div><div>Value</div><div>Description</div></div>                         |
|       |      |             | 0x33                                                                      |
|       |      |             | 0x22                                                                      |
|       |      |             | 0x11                                                                      |
|       |      |             | 0x00                                                                      |
|       |      |             | 0x77                                                                      |
|       |      |             | 0x66                                                                      |
|       |      |             | 0x55                                                                      |
|       |      |             | 0x44                                                                      |
| [1]   | RW   | I2C_TIMEOUT | Enable automatic reset of 2-wire interface (if SDA stays low for >50 ms). |

**Table 34: SYS\_GPIO0\_0 (0x0010)**

| Bit   | Type             | Symbol     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|-------|------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|-----|-------------------|-----|------------------|-----|-----------|-----|-----------------|-----|------------|-----|------------|-----|-------------------|-----|--------------|-----|------------|-----|------------|-----|------------------|-----|-----------|-----|-------------|-----|----------|-----|------------|-----|-------------|
| [4:1] | RW               | GPIO0_MODE | GPIO function mode select                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>GPIO disable</td></tr><tr><td>0x1</td><td>EN1 input</td></tr><tr><td>0x2</td><td>EN2 input</td></tr><tr><td>0x3</td><td>EN1 &amp; EN2 input</td></tr><tr><td>0x4</td><td>DVC1 input</td></tr><tr><td>0x5</td><td>DVC2 input</td></tr><tr><td>0x6</td><td>DVC1 &amp; DVC2 input</td></tr><tr><td>0x7</td><td>RELOAD input</td></tr><tr><td>0x8</td><td>PG1 output</td></tr><tr><td>0x9</td><td>PG2 output</td></tr><tr><td>0xA</td><td>PG1 &amp; PG2 output</td></tr><tr><td>0xB</td><td>SG output</td></tr><tr><td>0xC</td><td>nIRQ output</td></tr><tr><td>0xD</td><td>Reserved</td></tr><tr><td>0xE</td><td>Low output</td></tr><tr><td>0xF</td><td>High output</td></tr></table> | Value             | Description | 0x0 | GPIO disable      | 0x1 | EN1 input        | 0x2 | EN2 input | 0x3 | EN1 & EN2 input | 0x4 | DVC1 input | 0x5 | DVC2 input | 0x6 | DVC1 & DVC2 input | 0x7 | RELOAD input | 0x8 | PG1 output | 0x9 | PG2 output | 0xA | PG1 & PG2 output | 0xB | SG output | 0xC | nIRQ output | 0xD | Reserved | 0xE | Low output | 0xF | High output |
|       |                  |            | Value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Description       |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | GPIO disable      |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | EN1 input         |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | EN2 input         |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | EN1 & EN2 input   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | DVC1 input        |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | DVC2 input        |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | DVC1 & DVC2 input |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | RELOAD input      |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | PG1 output        |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | PG2 output        |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0xA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | PG1 & PG2 output  |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0xB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | SG output         |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0xC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | nIRQ output       |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0xD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Reserved          |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xE   | Low output       |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xF   | High output      |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| [0]   | RW               | GPIO0_OBUF | GPIO output buffer select                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>open-drain output</td></tr><tr><td>0x1</td><td>push-pull output</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Value             | Description | 0x0 | open-drain output | 0x1 | push-pull output |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | Value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Description       |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            | 0x0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | open-drain output |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x1   | push-pull output |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|       |                  |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |             |     |                   |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 35: SYS\_GPIO0\_1 (0x0011)**

| Bit                                                     | Type | Symbol         | Description                                               |
|---------------------------------------------------------|------|----------------|-----------------------------------------------------------|
| [7]                                                     | RW   | GPIO0_DEB_FALL | GPI debouce falling edge                                  |
| [6]                                                     | RW   | GPIO0_DEB_RISE | GPI debounce rising edge                                  |
| [5:4]                                                   | RW   | GPIO0_DEB      | GPI debounce time                                         |
|                                                         |      |                | <b>Value</b> <b>Description</b>                           |
|                                                         |      |                | 0x0100 μs debouce                                         |
|                                                         |      |                | 0x11 ms debouce                                           |
|                                                         |      |                | 0x210 ms debounce                                         |
| 0x3100 ms debounce                                      |      |                |                                                           |
| [3]                                                     | RW   | GPIO0_PUPD     | GPIO pull-up/pull-down enable                             |
|                                                         |      |                | <b>Value</b> <b>Description</b>                           |
|                                                         |      |                | 0x0GPI: pull-down disabled, GPO: pull-up to AVDD disabled |
| 0x1GPI: pull-down enabled, GPO: pull-up to AVDD enabled |      |                |                                                           |
| [2]                                                     | RW   | GPIO0_POL      | GPIO polarity                                             |
|                                                         |      |                | <b>Value</b> <b>Description</b>                           |
|                                                         |      |                | 0x0GPIO is active-high                                    |
| 0x1GPIO is active-low                                   |      |                |                                                           |
| [1:0]                                                   | RW   | GPIO0_TRIG     | GPI trigger type                                          |
|                                                         |      |                | <b>Value</b> <b>Description</b>                           |
|                                                         |      |                | 0x0Dual-edge triggered                                    |
|                                                         |      |                | 0x1Pos-edge triggered                                     |
|                                                         |      |                | 0x2Neg-edge triggered                                     |
| 0x3Reserved (No trigger)                                |      |                |                                                           |

**Table 36: SYS\_GPIO1\_0 (0x0012)**

| Bit   | Type              | Symbol     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |                 |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|-------|-------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------------|-----|--------------|-----|-----------|-----|-----------|-----|-----------------|-----|------------|-----|------------|-----|-------------------|-----|--------------|
| [4:1] | RW                | GPIO1_MODE | GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                                                                                                                      |                 |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x0</td><td>GPIO disable</td></tr><tr><td>0x1</td><td>EN1 input</td></tr><tr><td>0x2</td><td>EN2 input</td></tr><tr><td>0x3</td><td>EN1 &amp; EN2 input</td></tr><tr><td>0x4</td><td>DVC1 input</td></tr><tr><td>0x5</td><td>DVC2 input</td></tr><tr><td>0x6</td><td>DVC1 &amp; DVC2 input</td></tr><tr><td>0x7</td><td>RELOAD input</td></tr></tbody></table> | Value           | Description | 0x0 | GPIO disable | 0x1 | EN1 input | 0x2 | EN2 input | 0x3 | EN1 & EN2 input | 0x4 | DVC1 input | 0x5 | DVC2 input | 0x6 | DVC1 & DVC2 input | 0x7 | RELOAD input |
|       |                   |            | Value                                                                                                                                                                                                                                                                                                                                                                                                                                          | Description     |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x0                                                                                                                                                                                                                                                                                                                                                                                                                                            | GPIO disable    |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x1                                                                                                                                                                                                                                                                                                                                                                                                                                            | EN1 input       |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x2                                                                                                                                                                                                                                                                                                                                                                                                                                            | EN2 input       |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x3                                                                                                                                                                                                                                                                                                                                                                                                                                            | EN1 & EN2 input |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x4                                                                                                                                                                                                                                                                                                                                                                                                                                            | DVC1 input      |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
|       |                   |            | 0x5                                                                                                                                                                                                                                                                                                                                                                                                                                            | DVC2 input      |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
| 0x6   | DVC1 & DVC2 input |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |
| 0x7   | RELOAD input      |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 |             |     |              |     |           |     |           |     |                 |     |            |     |            |     |                   |     |              |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Bit | Type | Symbol     | Description                                                                                                                                                                     |
|-----|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |      |            | 0x8 PG1 output<br>0x9 PG2 output<br>0xA PG1 & PG2 output<br>0xB SG output<br>0xC nIRQ output<br>0xD Reserved<br>0xE Low output<br>0xF High output                               |
| [0] | RW   | GPIO1_OBUF | GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>Value Description<br>0x0 open-drain output<br>0x1 push-pull output |

**Table 37: SYS\_GPIO1\_1 (0x0013)**

| Bit   | Type | Symbol         | Description                                                                                                                                                                                                                                                  |
|-------|------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7]   | RW   | GPIO1_DEB_FALL | GPI debounce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                    |
| [6]   | RW   | GPIO1_DEB_RISE | GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                     |
| [5:4] | RW   | GPIO1_DEB      | GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>Value Description<br>0x0 100 $\mu$ s debounce<br>0x1 1 ms debounce<br>0x2 10 ms debounce<br>0x3 100 ms debounce                                         |
| [3]   | RW   | GPIO1_PUPD     | GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>Value Description<br>0x0 GPI: pull-down disabled, GPO: pull-up to AVDD disabled<br>0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled |
| [2]   | RW   | GPIO1_POL      | GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>Value Description<br>0x0 GPIO is active-high<br>0x1 GPIO is active-low                                                                                      |
| [1:0] | RW   | GPIO1_TRIG     | GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                             |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Bit | Type | Symbol | Description |                       |
|-----|------|--------|-------------|-----------------------|
|     |      |        | Value       | Description           |
|     |      |        | 0x0         | Dual-edge triggered   |
|     |      |        | 0x1         | Pos-edge triggered    |
|     |      |        | 0x2         | Neg-edge triggered    |
|     |      |        | 0x3         | Reserved (No trigger) |

**Table 38: SYS\_GPIO2\_0 (0x0014)**

| Bit             | Type | Symbol     | Description                                                                                               |
|-----------------|------|------------|-----------------------------------------------------------------------------------------------------------|
| [4:1]           | RW   | GPIO2_MODE | GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |
|                 |      |            | <b>Value</b> <b>Description</b>                                                                           |
|                 |      |            | 0x0GPIO disable                                                                                           |
|                 |      |            | 0x1EN1 input                                                                                              |
|                 |      |            | 0x2EN2 input                                                                                              |
|                 |      |            | 0x3EN1 & EN2 input                                                                                        |
|                 |      |            | 0x4DVC1 input                                                                                             |
|                 |      |            | 0x5DVC2 input                                                                                             |
|                 |      |            | 0x6DVC1 & DVC2 input                                                                                      |
|                 |      |            | 0x7RELOAD input                                                                                           |
|                 |      |            | 0x8PG1 output                                                                                             |
|                 |      |            | 0x9PG2 output                                                                                             |
|                 |      |            | 0xA PG1 & PG2 output                                                                                      |
|                 |      |            | 0xB SG output                                                                                             |
|                 |      |            | 0xC nIRQ output                                                                                           |
|                 |      |            | 0xD Reserved                                                                                              |
|                 |      |            | 0xE Low output                                                                                            |
| 0xF High output |      |            |                                                                                                           |
| [0]             | RW   | GPIO2_OBUF | GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |
|                 |      |            | <b>Value</b> <b>Description</b>                                                                           |
|                 |      |            | 0x0open-drain output                                                                                      |
|                 |      |            | 0x1push-pull output                                                                                       |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 39: SYS\_GPIO2\_1 (0x0015)**

| Bit   | Type                                                   | Symbol         | Description                                                                                                                                                                                                                                                                                                                                                                |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
|-------|--------------------------------------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------------|-----|--------------------------------------------------------|-----|------------------------------------------------------|-----|--------------------|-----|-----------------------|
| [7]   | RW                                                     | GPIO2_DEB_FALL | GPI debouce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                                                   |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| [6]   | RW                                                     | GPIO2_DEB_RISE | GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                                                   |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| [5:4] | RW                                                     | GPIO2_DEB      | <div>GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>100 μs debounce</td></tr><tr><td>0x1</td><td>1 ms debounce</td></tr><tr><td>0x2</td><td>10 ms debounce</td></tr><tr><td>0x3</td><td>100 ms debounce</td></tr></table>                   | Value | Description | 0x0 | 100 μs debounce                                        | 0x1 | 1 ms debounce                                        | 0x2 | 10 ms debounce     | 0x3 | 100 ms debounce       |
| Value | Description                                            |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x0   | 100 μs debounce                                        |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x1   | 1 ms debounce                                          |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x2   | 10 ms debounce                                         |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x3   | 100 ms debounce                                        |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| [3]   | RW                                                     | GPIO2_PUPD     | <div>GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</td></tr><tr><td>0x1</td><td>GPI: pull-down enabled, GPO: pull-up to AVDD enabled</td></tr></table>                  | Value | Description | 0x0 | GPI: pull-down disabled, GPO: pull-up to AVDD disabled | 0x1 | GPI: pull-down enabled, GPO: pull-up to AVDD enabled |     |                    |     |                       |
| Value | Description                                            |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x0   | GPI: pull-down disabled, GPO: pull-up to AVDD disabled |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x1   | GPI: pull-down enabled, GPO: pull-up to AVDD enabled   |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| [2]   | RW                                                     | GPIO2_POL      | <div>GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>GPIO is active-high</td></tr><tr><td>0x1</td><td>GPIO is active-low</td></tr></table>                                                                                                       | Value | Description | 0x0 | GPIO is active-high                                    | 0x1 | GPIO is active-low                                   |     |                    |     |                       |
| Value | Description                                            |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x0   | GPIO is active-high                                    |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x1   | GPIO is active-low                                     |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| [1:0] | RW                                                     | GPIO2_TRIG     | <div>GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Dual-edge triggered</td></tr><tr><td>0x1</td><td>Pos-edge triggered</td></tr><tr><td>0x2</td><td>Neg-edge triggered</td></tr><tr><td>0x3</td><td>Reserved (No trigger)</td></tr></table> | Value | Description | 0x0 | Dual-edge triggered                                    | 0x1 | Pos-edge triggered                                   | 0x2 | Neg-edge triggered | 0x3 | Reserved (No trigger) |
| Value | Description                                            |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x0   | Dual-edge triggered                                    |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x1   | Pos-edge triggered                                     |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x2   | Neg-edge triggered                                     |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |
| 0x3   | Reserved (No trigger)                                  |                |                                                                                                                                                                                                                                                                                                                                                                            |       |             |     |                                                        |     |                                                      |     |                    |     |                       |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 5.1.2 Buck1

Table 40: BUCK\_BUCK1\_0 (0x0020)

| Bit   | Type | Symbol         | Description                                                                                    |
|-------|------|----------------|------------------------------------------------------------------------------------------------|
| [6:4] | RW   | CH1_SR_DVC_DWN | Voltage slew-rate for DVC ramp-down                                                            |
|       |      |                | <b>Value</b> <b>Description</b>                                                                |
|       |      |                | 0x0      10 mV/8 $\mu$ s                                                                       |
|       |      |                | 0x1      10 mV/4 $\mu$ s                                                                       |
|       |      |                | 0x2      10 mV/2 $\mu$ s                                                                       |
|       |      |                | 0x3      10 mV/ $\mu$ s                                                                        |
|       |      |                | 0x4      20 mV/ $\mu$ s                                                                        |
|       |      |                | 0x5      Reserved                                                                              |
| [3:1] | RW   | CH1_SR_DVC_UP  | Voltage slew-rate for DVC ramp-up                                                              |
|       |      |                | <b>Value</b> <b>Description</b>                                                                |
|       |      |                | 0x0      10 mV/8 $\mu$ s                                                                       |
|       |      |                | 0x1      10 mV/4 $\mu$ s                                                                       |
|       |      |                | 0x2      10 mV/2 $\mu$ s                                                                       |
|       |      |                | 0x3      10 mV/ $\mu$ s                                                                        |
|       |      |                | 0x4      20 mV/ $\mu$ s                                                                        |
|       |      |                | 0x5      40 mV/ $\mu$ s                                                                        |
| [0]   | RW   | CH1_EN         | Channel enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |
|       |      |                |                                                                                                |

Table 41: BUCK\_BUCK1\_1 (0x0021)

| Bit   | Type | Symbol         | Description                        |
|-------|------|----------------|------------------------------------|
| [6:4] | RW   | CH1_SR_SHDN    | Voltage slew-rate during shut-down |
|       |      |                | <b>Value</b> <b>Description</b>    |
|       |      |                | 0x0      10 mV/8 $\mu$ s           |
|       |      |                | 0x1      10 mV/4 $\mu$ s           |
|       |      |                | 0x2      10 mV/2 $\mu$ s           |
|       |      |                | 0x3      10 mV/ $\mu$ s            |
|       |      |                | 0x4      20 mV/ $\mu$ s            |
|       |      |                | 0x5      Reserved                  |
| [3:1] | RW   | CH1_SR_STARTUP | Voltage slew-rate during startup   |
|       |      |                |                                    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Bit | Type | Symbol     | Description                                                                                                                                                                                                                                    |
|-----|------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |      |            | <b>Value</b> <b>Description</b><br>0x0      10 mV/8 $\mu$ s<br>0x1      10 mV/4 $\mu$ s<br>0x2      10 mV/2 $\mu$ s<br>0x3      10 mV/ $\mu$ s<br>0x4      20 mV/ $\mu$ s<br>0x5      40 mV/ $\mu$ s<br>0x6      Reserved<br>0x7      Reserved |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
|     |      |            |                                                                                                                                                                                                                                                |
| [0] | RW   | CH1_PD_DIS | Pull-down while buck is disabled. 0: enable, 1: disable                                                                                                                                                                                        |

**Table 42: BUCK\_BUCK1\_2 (0x0022)**

| Bit   | Type | Symbol   | Description                                                                                                                                                                                                                                                                                               |
|-------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | RW   | CH1_ILIM | Select OCP threshold (A). The value is configured by OTP and should not be modified while the buck is active.                                                                                                                                                                                             |
|       |      |          | <b>Value</b> <b>Description</b><br>0x0      Reserved<br>0x1      3.5<br>0x2      4.0<br>0x3      4.5<br>0x4      5.0<br>0x5      5.5<br>0x6      6.0<br>0x7      6.5<br>0x8      7.0<br>0x9      7.5<br>0xA      8.0<br>0xB      8.5<br>0xC      9.0<br>0xD      9.5<br>0xE      10.0<br>0xF      Disable |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |
|       |      |          |                                                                                                                                                                                                                                                                                                           |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 43: BUCK\_BUCK1\_3 (0x0023)**

| Bit   | Type | Symbol   | Description                                                                                                   |
|-------|------|----------|---------------------------------------------------------------------------------------------------------------|
| [7:0] | RW   | CH1_VMAX | VOUT max setting (V):<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in 10 mV steps.<br>This is a read-only register. |
|       |      |          | <b>Value</b> <b>Description</b>                                                                               |
|       |      |          | 0x1E      0.3                                                                                                 |
|       |      |          | 0x1F      0.31                                                                                                |
|       |      |          | 0x20      0.32                                                                                                |
|       |      |          | Continuing through...                                                                                         |
|       |      |          | 0x99      1.53                                                                                                |
|       |      |          | To...                                                                                                         |
|       |      |          | 0xBD      1.89                                                                                                |
|       |      |          | 0xBE      1.9                                                                                                 |

**Table 44: BUCK\_BUCK1\_4 (0x0024)**

| Bit   | Type | Symbol     | Description                                                                                                                           |
|-------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| [4]   | RW   | CH1_VSEL   | Output voltage and operation selection: 0: A, 1: B.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |
| [3:2] | RW   | CH1_B_MODE | Operation mode selection.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |
|       |      |            | <b>Value</b> <b>Description</b>                                                                                                       |
|       |      |            | 0x0      Force PFM operation                                                                                                          |
|       |      |            | 0x1      Force PWM operation                                                                                                          |
|       |      |            | 0x2      Force PWM operation                                                                                                          |
|       |      |            | 0x3      Auto mode                                                                                                                    |
| [1:0] | RW   | CH1_A_MODE | Operation mode selection.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |
|       |      |            | <b>Value</b> <b>Description</b>                                                                                                       |
|       |      |            | 0x0      Force PFM operation                                                                                                          |
|       |      |            | 0x1      Force PWM operation                                                                                                          |
|       |      |            | 0x2      Force PWM operation                                                                                                          |
|       |      |            | 0x3      Auto mode                                                                                                                    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 45: BUCK\_BUCK1\_5 (0x0025)**

| Bit   | Type | Symbol     | Description                                                                                                                                                                                                                                             |
|-------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | RW   | CH1_A_VOUT | Output voltage setting A: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br>Write-protected when value is written below 0.30 V or above 1.90 V |
|       |      |            | <b>Value</b> <b>Description</b>                                                                                                                                                                                                                         |
|       |      |            | 0x1E      0.3                                                                                                                                                                                                                                           |
|       |      |            | 0x1F      0.31                                                                                                                                                                                                                                          |
|       |      |            | 0x20      0.32                                                                                                                                                                                                                                          |
|       |      |            | Continuing through...                                                                                                                                                                                                                                   |
|       |      |            | 0x64      1                                                                                                                                                                                                                                             |
|       |      |            | To...                                                                                                                                                                                                                                                   |
|       |      |            | 0xBC      1.88                                                                                                                                                                                                                                          |
|       |      |            | 0xBD      1.89                                                                                                                                                                                                                                          |
|       |      |            | 0xBE      1.9                                                                                                                                                                                                                                           |

**Table 46: BUCK\_BUCK1\_6 (0x0026)**

| Bit   | Type | Symbol     | Description                                                                                                                                                                                                                                             |
|-------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | RW   | CH1_B_VOUT | Output voltage setting B: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br>Write-protected when value is written below 0.30 V or above 1.90 V |
|       |      |            | <b>Value</b> <b>Description</b>                                                                                                                                                                                                                         |
|       |      |            | 0x1E      0.3                                                                                                                                                                                                                                           |
|       |      |            | 0x1F      0.31                                                                                                                                                                                                                                          |
|       |      |            | 0x20      0.32                                                                                                                                                                                                                                          |
|       |      |            | Continuing through...                                                                                                                                                                                                                                   |
|       |      |            | 0x64      1                                                                                                                                                                                                                                             |
|       |      |            | To...                                                                                                                                                                                                                                                   |
|       |      |            | 0xBC      1.88                                                                                                                                                                                                                                          |
|       |      |            | 0xBD      1.89                                                                                                                                                                                                                                          |
|       |      |            | 0xBE      1.9                                                                                                                                                                                                                                           |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 5.1.3 Buck2

Table 47: BUCK\_BUCK2\_0 (0x0028)

| Bit   | Type | Symbol         | Description                                                                                    |
|-------|------|----------------|------------------------------------------------------------------------------------------------|
| [6:4] | RW   | CH2_SR_DVC_DWN | Voltage slew-rate for DVC ramp-down                                                            |
|       |      |                | <b>Value</b> <b>Description</b>                                                                |
|       |      |                | 0x0          10 mV/8 $\mu$ s                                                                   |
|       |      |                | 0x1          10 mV/4 $\mu$ s                                                                   |
|       |      |                | 0x2          10 mV/2 $\mu$ s                                                                   |
|       |      |                | 0x3          10 mV/ $\mu$ s                                                                    |
|       |      |                | 0x4          20 mV/ $\mu$ s                                                                    |
|       |      |                | 0x5          Reserved                                                                          |
|       |      |                | 0x6          Reserved                                                                          |
|       |      |                | 0x7          Reserved                                                                          |
| [3:1] | RW   | CH2_SR_DVC_UP  | Voltage slew-rate for DVC ramp-up                                                              |
|       |      |                | <b>Value</b> <b>Description</b>                                                                |
|       |      |                | 0x0          10 mV/8 $\mu$ s                                                                   |
|       |      |                | 0x1          10 mV/4 $\mu$ s                                                                   |
|       |      |                | 0x2          10 mV/2 $\mu$ s                                                                   |
|       |      |                | 0x3          10 mV/ $\mu$ s                                                                    |
|       |      |                | 0x4          20 mV/ $\mu$ s                                                                    |
|       |      |                | 0x5          40 mV/ $\mu$ s                                                                    |
|       |      |                | 0x6          Reserved                                                                          |
|       |      |                | 0x7          Reserved                                                                          |
| [0]   | RW   | CH2_EN         | Channel enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |

Table 48: BUCK\_BUCK2\_1 (0x0029)

| Bit   | Type | Symbol         | Description                         |
|-------|------|----------------|-------------------------------------|
| [6:4] | RW   | CH2_SR_SHDN    | Voltage slew-rate during power-down |
|       |      |                | <b>Value</b> <b>Description</b>     |
|       |      |                | 0x0          10 mV/8 $\mu$ s        |
|       |      |                | 0x1          10 mV/4 $\mu$ s        |
|       |      |                | 0x2          10 mV/2 $\mu$ s        |
|       |      |                | 0x3          10 mV/ $\mu$ s         |
|       |      |                | 0x4          20 mV/ $\mu$ s         |
|       |      |                | 0x5          Reserved               |
|       |      |                | 0x6          Reserved               |
|       |      |                | 0x7          Immediate power-down   |
| [3:1] | RW   | CH2_SR_STARTUP | Voltage slew-rate during startup    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

| Bit | Type | Symbol     | Description                                             |                    |
|-----|------|------------|---------------------------------------------------------|--------------------|
|     |      |            | <b>Value</b>                                            | <b>Description</b> |
|     |      |            | 0x0                                                     | 10 mV/8 μs         |
|     |      |            | 0x1                                                     | 10 mV/4 μs         |
|     |      |            | 0x2                                                     | 10 mV/2 μs         |
|     |      |            | 0x3                                                     | 10 mV/μs           |
|     |      |            | 0x4                                                     | 20 mV/μs           |
|     |      |            | 0x5                                                     | 40 mV/μs           |
|     |      |            | 0x6                                                     | Reserved           |
|     |      |            | 0x7                                                     | Reserved           |
| [0] | RW   | CH2_PD_DIS | Pull-down while BUCK is disabled. 0: enable, 1: disable |                    |

**Table 49: BUCK\_BUCK2\_2 (0x002A)**

| Bit   | Type    | Symbol   | Description          |                    |
|-------|---------|----------|----------------------|--------------------|
| [3:0] | RW      | CH2_ILIM | Select OCP threshold |                    |
|       |         |          | <b>Value</b>         | <b>Description</b> |
|       |         |          | 0x0                  | Reserved           |
|       |         |          | 0x1                  | 3.5                |
|       |         |          | 0x2                  | 4.0                |
|       |         |          | 0x3                  | 4.5                |
|       |         |          | 0x4                  | 5.0                |
|       |         |          | 0x5                  | 5.5                |
|       |         |          | 0x6                  | 6.0                |
|       |         |          | 0x7                  | 6.5                |
|       |         |          | 0x8                  | 7.0                |
|       |         |          | 0x9                  | 7.5                |
|       |         |          | 0xA                  | 8.0                |
|       |         |          | 0xB                  | 8.5                |
|       |         |          | 0xC                  | 9.0                |
|       |         |          | 0xD                  | 9.5                |
|       |         |          | 0xE                  | 10.0               |
| 0xF   | Disable |          |                      |                    |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

**Table 50: BUCK\_BUCK2\_3 (0x002B)**

| Bit   | Type | Symbol   | Description                                                                                                                                                                                                                                                                                                                                                                                      |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|-------|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|------|-----|------|------|------|------|-----------------------|--|------|---|-------|--|------|------|------|------|------|-----|
| [7:0] | RW   | CH2_VMAX | VOUT max setting (V):<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV<br>This is a read-only register.                                                                                                                                                                                                                                                                                  |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x1E</td><td>0.3</td></tr><tr><td>0x1F</td><td>0.31</td></tr><tr><td>0x20</td><td>0.32</td></tr><tr><td colspan="2">Continuing through...</td></tr><tr><td>0x64</td><td>1</td></tr><tr><td colspan="2">To...</td></tr><tr><td>0xBC</td><td>1.88</td></tr><tr><td>0xBD</td><td>1.89</td></tr><tr><td>0xBE</td><td>1.9</td></tr></table> | Value       | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | 0x64 | 1 | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
|       |      |          | Value                                                                                                                                                                                                                                                                                                                                                                                            | Description |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | 0x1E                                                                                                                                                                                                                                                                                                                                                                                             | 0.3         |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | 0x1F                                                                                                                                                                                                                                                                                                                                                                                             | 0.31        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | 0x20                                                                                                                                                                                                                                                                                                                                                                                             | 0.32        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | Continuing through...                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | 0x64                                                                                                                                                                                                                                                                                                                                                                                             | 1           |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | To...                                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |          | 0xBC                                                                                                                                                                                                                                                                                                                                                                                             | 1.88        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
| 0xBD  | 1.89 |          |                                                                                                                                                                                                                                                                                                                                                                                                  |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
| 0xBE  | 1.9  |          |                                                                                                                                                                                                                                                                                                                                                                                                  |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |

**Table 51: BUCK\_BUCK2\_4 (0x002C)**

| Bit   | Type                | Symbol     | Description                                                                                                                                                                                                                                                                                                                                                              |       |             |     |                     |     |                     |     |                     |     |           |
|-------|---------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|-----------|
| [4]   | RW                  | CH2_VSEL   | Output voltage and operation selection: 0: A, 1: B. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                                                                                                                                                                                                                                       |       |             |     |                     |     |                     |     |                     |     |           |
| [3:2] | RW                  | CH2_B_MODE | <div>Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Force PFM operation</td></tr><tr><td>0x1</td><td>Force PWM operation</td></tr><tr><td>0x2</td><td>Force PWM operation</td></tr><tr><td>0x3</td><td>Auto mode</td></tr></table> | Value | Description | 0x0 | Force PFM operation | 0x1 | Force PWM operation | 0x2 | Force PWM operation | 0x3 | Auto mode |
| Value | Description         |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x0   | Force PFM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x1   | Force PWM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x2   | Force PWM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x3   | Auto mode           |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| [1:0] | RW                  | CH2_A_MODE | <div>Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</div> <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Force PFM operation</td></tr><tr><td>0x1</td><td>Force PWM operation</td></tr><tr><td>0x2</td><td>Force PWM operation</td></tr><tr><td>0x3</td><td>Auto mode</td></tr></table> | Value | Description | 0x0 | Force PFM operation | 0x1 | Force PWM operation | 0x2 | Force PWM operation | 0x3 | Auto mode |
| Value | Description         |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x0   | Force PFM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x1   | Force PWM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x2   | Force PWM operation |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |
| 0x3   | Auto mode           |            |                                                                                                                                                                                                                                                                                                                                                                          |       |             |     |                     |     |                     |     |                     |     |           |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

Table 52: BUCK\_BUCK2\_5 (0x002D)

| Bit   | Type | Symbol     | Description                                                                                                                                                                                                                                                                                                                                                                                      |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|-------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|------|-----|------|------|------|------|-----------------------|--|------|---|-------|--|------|------|------|------|------|-----|
| [7:0] | RW   | CH2_A_VOUT | Output voltage setting A: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br>Write-protected when value is written below 0.30 V or above 1.90 V                                                                                                                                          |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x1E</td><td>0.3</td></tr><tr><td>0x1F</td><td>0.31</td></tr><tr><td>0x20</td><td>0.32</td></tr><tr><td colspan="2">Continuing through...</td></tr><tr><td>0x64</td><td>1</td></tr><tr><td colspan="2">To...</td></tr><tr><td>0xBC</td><td>1.88</td></tr><tr><td>0xBD</td><td>1.89</td></tr><tr><td>0xBE</td><td>1.9</td></tr></table> | Value       | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | 0x64 | 1 | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
|       |      |            | Value                                                                                                                                                                                                                                                                                                                                                                                            | Description |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x1E                                                                                                                                                                                                                                                                                                                                                                                             | 0.3         |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x1F                                                                                                                                                                                                                                                                                                                                                                                             | 0.31        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x20                                                                                                                                                                                                                                                                                                                                                                                             | 0.32        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | Continuing through...                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x64                                                                                                                                                                                                                                                                                                                                                                                             | 1           |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | To...                                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBC                                                                                                                                                                                                                                                                                                                                                                                             | 1.88        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBD                                                                                                                                                                                                                                                                                                                                                                                             | 1.89        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBE                                                                                                                                                                                                                                                                                                                                                                                             | 1.9         |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |

Table 53: BUCK\_BUCK2\_6 (0x002E)

| Bit   | Type | Symbol     | Description                                                                                                                                                                                                                                                                                                                                                                                      |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|-------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|------|-----|------|------|------|------|-----------------------|--|------|---|-------|--|------|------|------|------|------|-----|
| [7:0] | RW   | CH2_B_VOUT | Output voltage setting B: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br>Write-protected when value is written below 0.30 V or above 1.90 V                                                                                                                                          |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x1E</td><td>0.3</td></tr><tr><td>0x1F</td><td>0.31</td></tr><tr><td>0x20</td><td>0.32</td></tr><tr><td colspan="2">Continuing through...</td></tr><tr><td>0x64</td><td>1</td></tr><tr><td colspan="2">To...</td></tr><tr><td>0xBC</td><td>1.88</td></tr><tr><td>0xBD</td><td>1.89</td></tr><tr><td>0xBE</td><td>1.9</td></tr></table> | Value       | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | 0x64 | 1 | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
|       |      |            | Value                                                                                                                                                                                                                                                                                                                                                                                            | Description |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x1E                                                                                                                                                                                                                                                                                                                                                                                             | 0.3         |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x1F                                                                                                                                                                                                                                                                                                                                                                                             | 0.31        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x20                                                                                                                                                                                                                                                                                                                                                                                             | 0.32        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | Continuing through...                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0x64                                                                                                                                                                                                                                                                                                                                                                                             | 1           |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | To...                                                                                                                                                                                                                                                                                                                                                                                            |             |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBC                                                                                                                                                                                                                                                                                                                                                                                             | 1.88        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBD                                                                                                                                                                                                                                                                                                                                                                                             | 1.89        |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |
|       |      |            | 0xBE                                                                                                                                                                                                                                                                                                                                                                                             | 1.9         |             |      |     |      |      |      |      |                       |  |      |   |       |  |      |      |      |      |      |     |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 5.1.4 Serialization

Table 54: OTP\_DEVICE\_ID (0x0048)

| Bit   | Type | Symbol | Description |
|-------|------|--------|-------------|
| [7:0] | R    | DEV_ID | Device ID   |

Table 55: OTP\_VARIANT\_ID (0x0049)

| Bit   | Type | Symbol | Description        |
|-------|------|--------|--------------------|
| [7:4] | R    | MRC    | Mask Revision Code |
| [3:0] | R    | VRC    | Chip Variant Code  |

Table 56: OTP\_CUSTOMER\_ID (0x004A)

| Bit   | Type | Symbol  | Description |
|-------|------|---------|-------------|
| [7:0] | R    | CUST_ID | Customer ID |

Table 57: OTP\_CONFIG\_ID (0x004B)

| Bit   | Type | Symbol     | Description |
|-------|------|------------|-------------|
| [7:0] | R    | CONFIG_REV | OTP Variant |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 6 Package Information

#### 6.1 Package Outlines

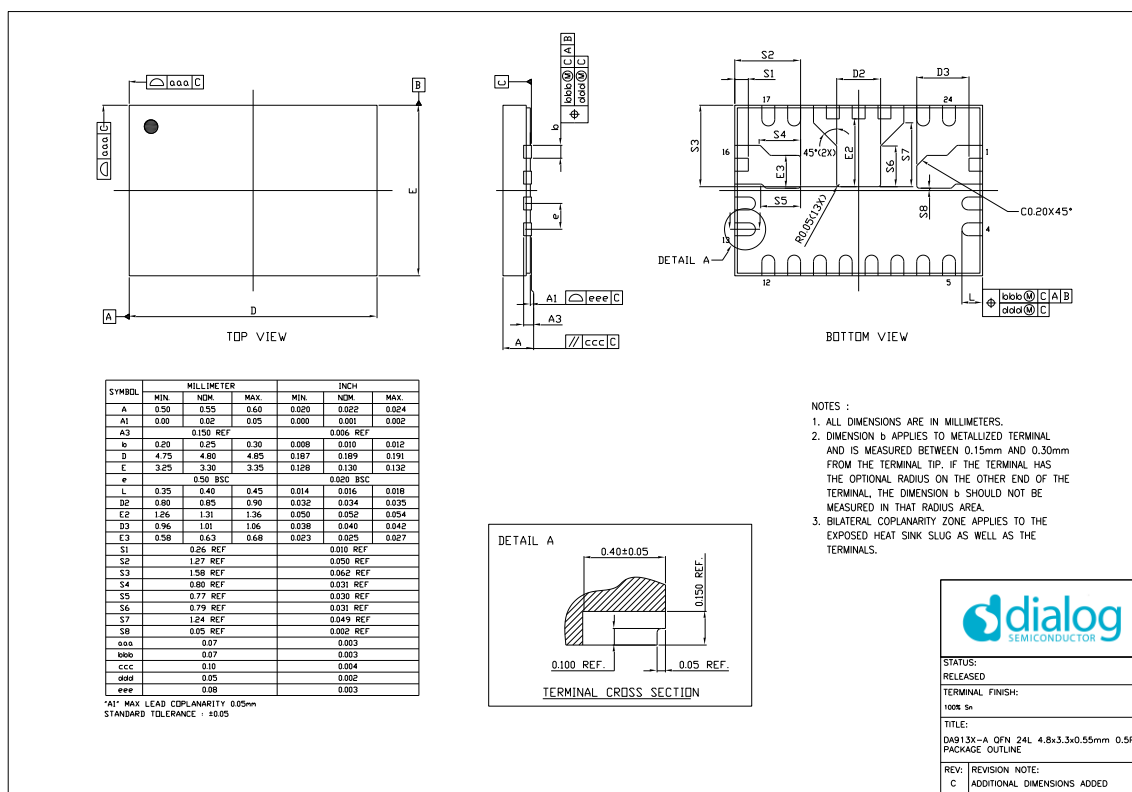


Figure 19: Package Outline Drawing

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 6.2 Package Marking

| Package Marking                                                                   |                 |                      |
|-----------------------------------------------------------------------------------|-----------------|----------------------|
| A1 Corner >                                                                       | Marking Content | Format               |
| 1st                                                                               | •               | Pin 1 ID             |
| 2nd                                                                               | D A 9 1 3 2     | Orientation/Part No. |
| 3rd                                                                               | x x A T y y     | OTP/Option/Year      |
| 4th                                                                               | W W Z Z Z Z     | Date Code            |
|                                                                                   |                 |                      |
| Date Code Format: yy = Year, ww = Week, zzzz = Traceability                       |                 |                      |
| xx identifies the OTP Variant                                                     |                 |                      |
| A or AT optionally indicate the Automotive and Automotive high temp test options. |                 |                      |

### 6.3 Moisture Sensitivity Level

The moisture sensitivity level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in The FCQFN package is qualified for MSL 3.

Table 58.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The FCQFN package is qualified for MSL 3.

**Table 58: MSL Classification**

| MSL Level | Floor Lifetime | Conditions      |
|-----------|----------------|-----------------|
| MSL 4     | 72 hours       | 30 °C / 60 % RH |
| MSL 3     | 168 hours      | 30 °C / 60 % RH |
| MSL 2A    | 4 weeks        | 30 °C / 60 % RH |
| MSL 2     | 1 year         | 30 °C / 60 % RH |
| MSL 1     | Unlimited      | 30 °C / 60 % RH |

### 6.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 7 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Dialog Semiconductor [local sales representative](#).

**Table 59: Ordering Information**

| Part Number | Package                             | Package Description | MOQ                  |
|-------------|-------------------------------------|---------------------|----------------------|
| DA9132xxRT2 | 24 FCQFN wettable flanks, 3.3 x 4.8 | T&R, 4800 pcs       | 3 Reels - 14400      |
| DA9132xxRT1 | 24 FCQFN wettable flanks            | Tray, 490 pcs       | 30 Trays - 14700 pcs |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### 8 Application Information

The following recommended components are examples selected from requirements of a typical application.

#### 8.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

**Table 60: Recommended Consumer Grade Capacitor Types**

| Application        | Value (μF) | Size | Temp. Char. | Tol. (%) | V-Rate (V) | Type                     |
|--------------------|------------|------|-------------|----------|------------|--------------------------|
| VOUT output bypass | 10         | 0402 | X5R         | 20       | 6.3        | Murata GRM155R60J106ME15 |
| PVDDx bypass       | 10         | 0603 | X5R         | 20       | 25         | Murata GRM188R61E106MA73 |
| AVDD bypass        | 1          | 0402 | X5R         | 10       | 10         | Murata GRM155R61A105KE15 |

**Table 61: Recommended Automotive Grade Capacitor Types**

| Application        | Value (μF) | Size | Temp. Char. | Tol. (%) | V-Rate (V) | Type                      |
|--------------------|------------|------|-------------|----------|------------|---------------------------|
| VOUT output bypass | 10         | 0805 | X7R ±15%    | ±10      | 6.3        | TDK CGA4J1X7R0J106K125AC  |
| PVDDx bypass       | 10         | 3216 | X7R ±15%    | ±10      | 16         | Murata GCM31CR71C106KA64L |
| AVDD bypass        | 1          | 0805 | X7R ±15%    | ±10      | 50         | Murata GCM21BR71H105KA03L |

#### 8.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current  
Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance  
Critical for the converter efficiency and should therefore be minimized.

**Table 62: Recommended Inductor Types**

| Value (μH) | Size (mm)       | IMAX (DC) (A) | ISAT (A) | Tol. (%) | DC Resistance (mΩ) | Type                     |
|------------|-----------------|---------------|----------|----------|--------------------|--------------------------|
| 0.22       | 2.5 x 2.0 x 1.2 | 6.7           | 8        | 20       | 8                  | TDK TFM252012ALMAR22MTAA |
| 0.47       | 2.5 x 2.0 x 1.2 | 4.9           | 5.8      | 20       | 8                  | TDK TFM252012ALMAR47MTAA |

## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

### Status Definitions

| Revision | Datasheet Status | Product Status | Definition                                                                                                                                                                                                                                                                                                                                                                                           |
|----------|------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.<n>    | Target           | Development    | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.                                                                                                                                                                                                                                                               |
| 2.<n>    | Preliminary      | Qualification  | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.                                                                                                                                                                                            |
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| 4.<n>    | Obsolete         | Archived       | This datasheet contains the specifications for discontinued products. The information is provided for reference only.                                                                                                                                                                                                                                                                                |

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## High-Performance, Dual-Channel DC-DC Converter for Mobile and Portable Applications

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