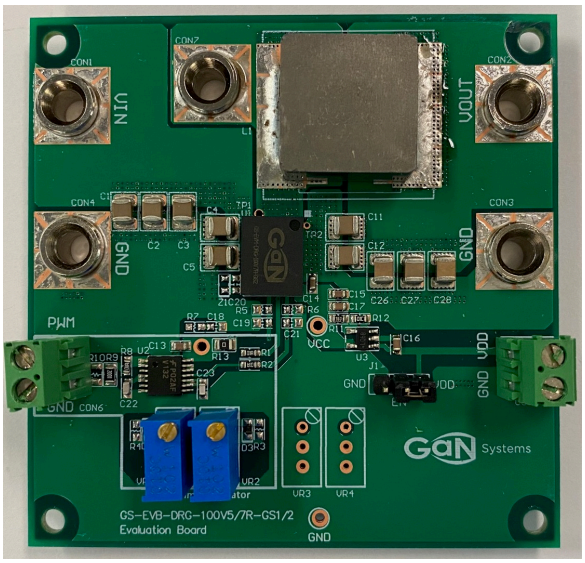
GS-EVB-DRG-100V7R-GS2

100 V Driver GaN Open Loop Buck/Boost Evaluation Board

Technical Manual



Visit www.gansystems.com for the latest version of this technical manual.

WARNING:
PCB surface can become hot. Contact may cause burns. Do not touch!

CAUTION!
This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

Overview

GS-EVB-DRG-100V7R-GS2 Evaluation Board with 100V DrGaN SMT power stage provides a complete 48V step down converter which can be used to evaluate efficiency & power density for use in applications such as CPU/GPU/DDR, high-performance Class D audio systems, and forward converters, ZVS, and buck / boost topologies. GS-EVB-DRG-100V7R-GS2 is intended and made available for testing and evaluation purposes only.

Features

- Integrated board for easy evaluation of GS-EVM-DRG-100VR-GS2
- 100 V Driver GaN Open loop Buck/Boost Board
- 7mΩ Half-Bridge power stage
- Dual PWM DrGaN input
- Ultra-fast rise/fall time
- High power density at 1MHz+ f_{SW} operation
- High efficiency for 48V board power

Applications

- 48 V Step Down Converters
- CPU/GPU/DDR
- High-performance Class D Audio systems
- Forward Converter, ZVS, Buck/Boost topologies

Contents and Requirements

Kit Contents

The GS-EVB-DRG-100V7R-GS2 includes the following hardware.

Table 1 GS-EVB-DRG-100V7R-GS2 Evaluation Kit Contents

Quantity	Description
1	GS-EVB-DRG-100V7R-GS2 100 V Open Loop Buck/Boost Evaluation Board with Driver GaN Power Stage

Hardware Requirements

In order to evaluate the performance of the evaluation board, the following equipment is required:

- High speed digital oscilloscope
- DC load (power resistor or electrical load)
- 48V & 5V DC power supplies
- Signal generator for PWM input (0-5V)
- DC test leads

Electrical Specifications

Table 2 Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ.	Max
V_{IN}	Input Voltage [V]			48	
V_{OUT}	Output Voltage [V]	Duty Cycle=25%		12	
I_{OUT}	Output current [A]			10	
F_{SW}	Switching frequency [kHz]		300	500	1000
	Efficiency [%]	F_{SW}=500kHz			96.4

Block Diagram and schematics

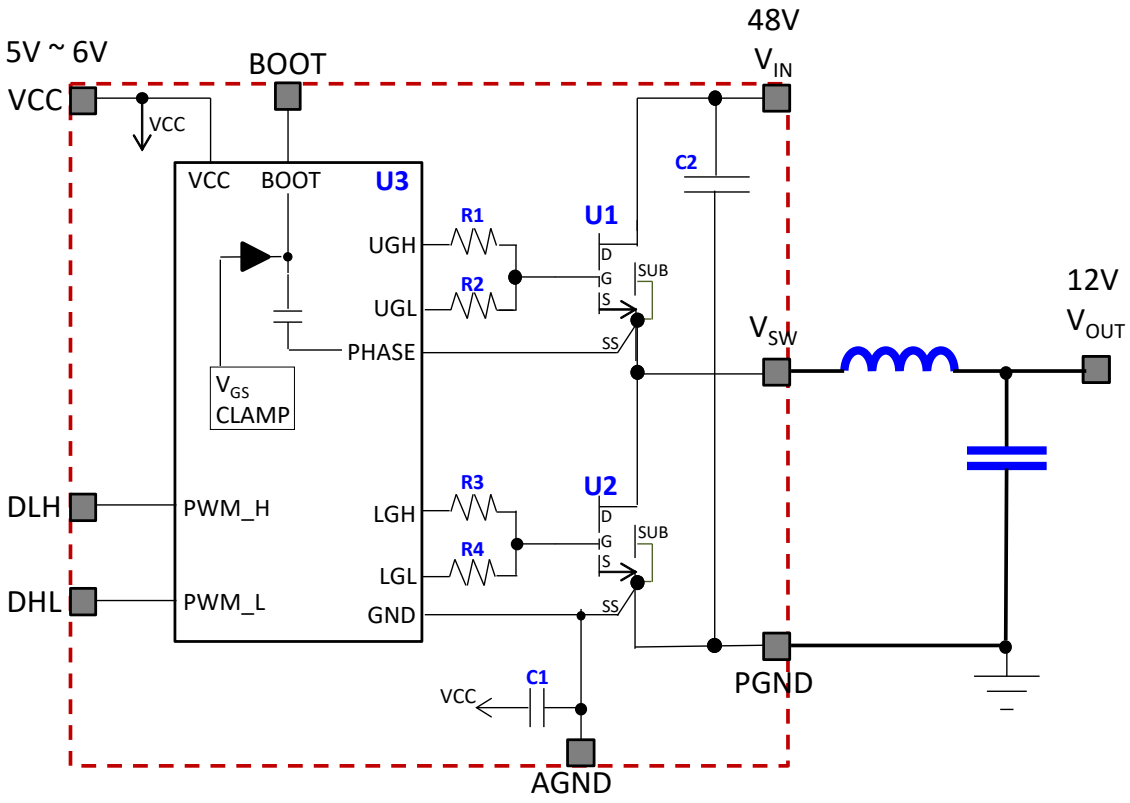


Figure 1 DrGaN Module Block Diagram

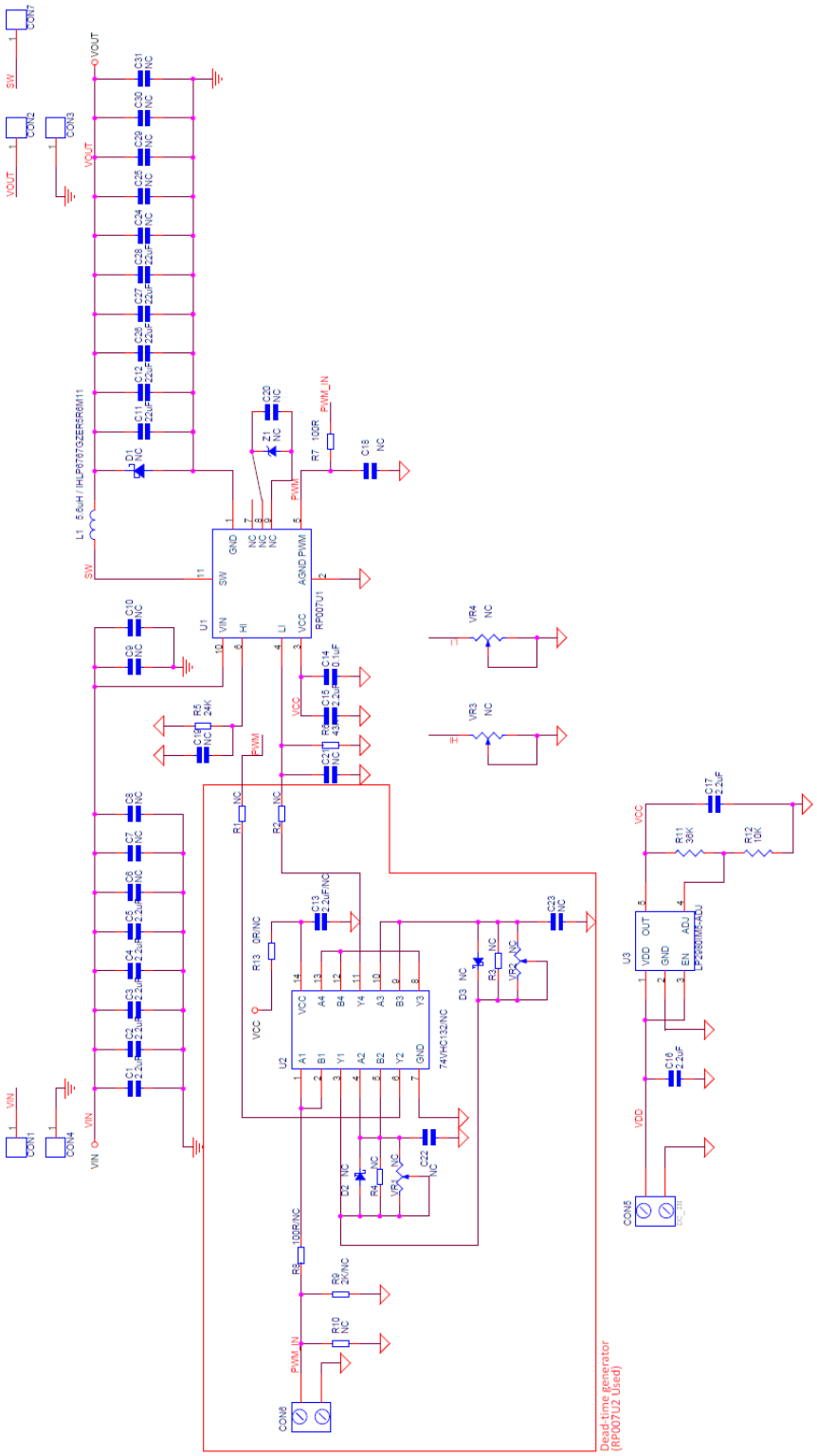


Figure 2 Evaluation Board Schematics

Please refer to the Evaluation Board/Kit Important Notice on page 10

Quick Start Guide

Pin Description

Figure 3 Pinout definition

Board Setup

Below is an example of board connection setup for 150W Open Loop Buck DC/DC Converter.

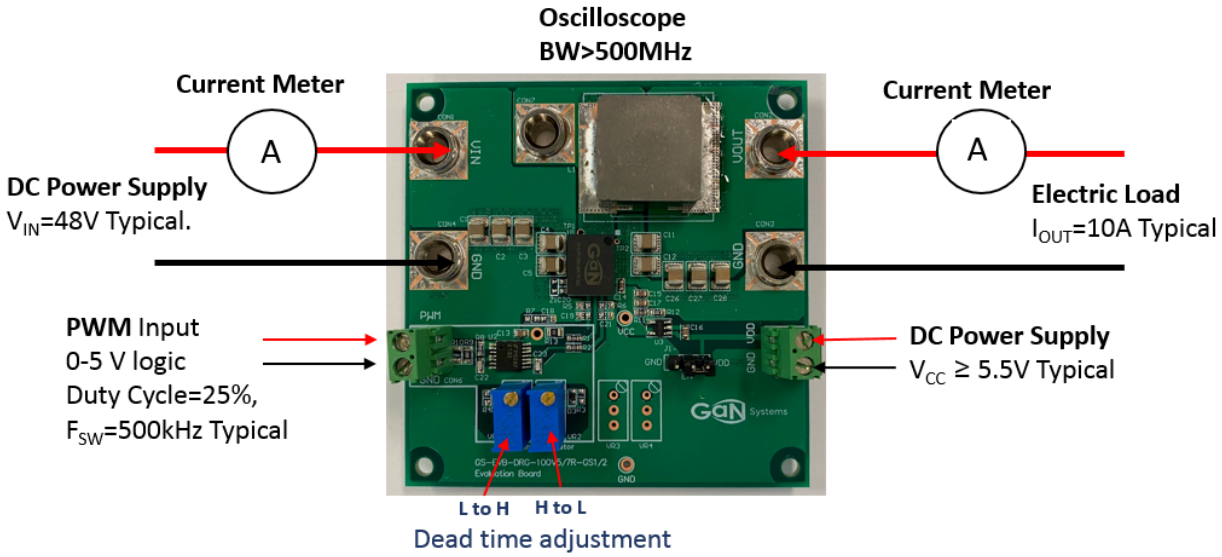


Figure 4 Board Connection for Open Loop Buck DC/DC Converter

Test Results

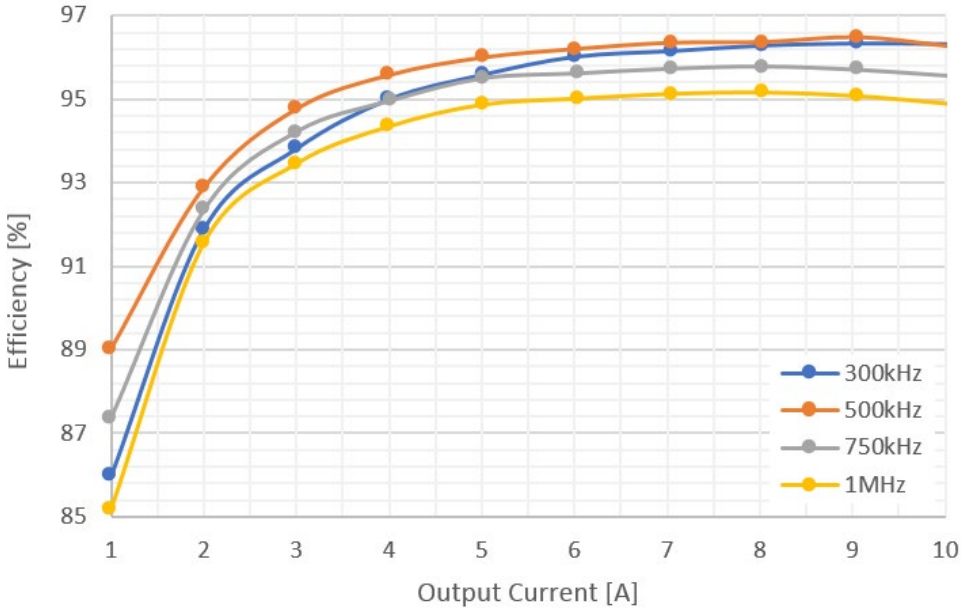


Figure 5 Efficiency (not including driver loss)

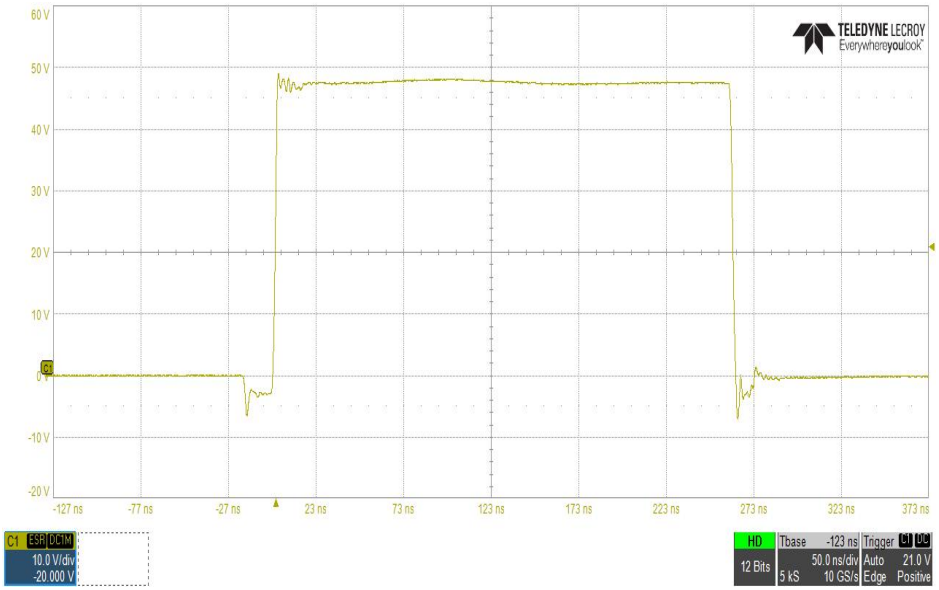


Figure 6 Switching Waveform: F_{SW} = 1 MHz

Bill of Materials (BOM)

Table 3 Bill of Materials

100V GaN Module EVB BOM LIST						
Designator	Value	Package Reference	Description	Manufacturer	Part Number	Quanity
U1		QFN	100V GaN Module, QFN 8 x 10		GS-EVM-DRG-100V7R-GS2	1
U2		TSSOP-14	IC GATE NAND 4CH 2-INP 14-TSSOP	FAIRCHILD	74VHC132MTCX	1
U3		SOT-235	IC REG LDO 16Vin, 0.2A, Adj, SOT23-5	TI	LP2980IM5-ADJ	1
C1, C2, C3, C4, C5	2.2µF	1210	CAP, Ceramic, 2.2µF, 100V, +-/10%	MuRata	GCJ32DR72A225KA01	5
C11, C12, C26, C27, C28	22uF	1210	CAP, Ceramic, 22µF, 25V, +-/10%	MuRata	GRM32ER71E226KE15	5
C14	0.1uF	0603	CAP, Ceramic, 0.1µF, 50V, +-/10%	MuRata	GCM188L81H104KA57	1
C13, C15, C16, C17	2.2uF	0603	CAP, Ceramic, 2.2µF, 16V, +-/10%	MuRata	GRM188Z71C225KE43	4
C22, C23	100pF	0603	CAP, Ceramic, 100pF, 50V, +-/5%	MuRata	GCH1555C1H101JE01	2
R1, R2, R8	100R	0603	RES, 100R ohm, 1%, 0603			3
R9	2.2K	0805	RES, 2.2K ohm, 1%, 0805			1
R11	39K	0603	RES, 36K ohm, 1%, 0603			1
R12	10K	0603	RES, 10K ohm, 1%, 0603			1
R13	0R	0805	RES, 0 ohm, 1%, 0805			1
VR1, VR2	1K		TRIMMER 1K OHM 0.5W TH	MuRata	PV36W102C01B00	2
D2, D3	20V	SOD-523	DIODE SCHOTTKY 20V 500MA SOD523	NXP	PMEG2005EB	2
L1	5.6uH		Inductor, 5.6uH, 4.23mR	Vishay	IHLP6767GZER5R6M11	1
CON1,CON2,CON3,CON4			JACK NON-INSULATED .218"	Keystone	575-4	4
CON5,CON6		PBT 381	PCB Terminal Block Series 381		PBT 381-2	2

PCB Layout

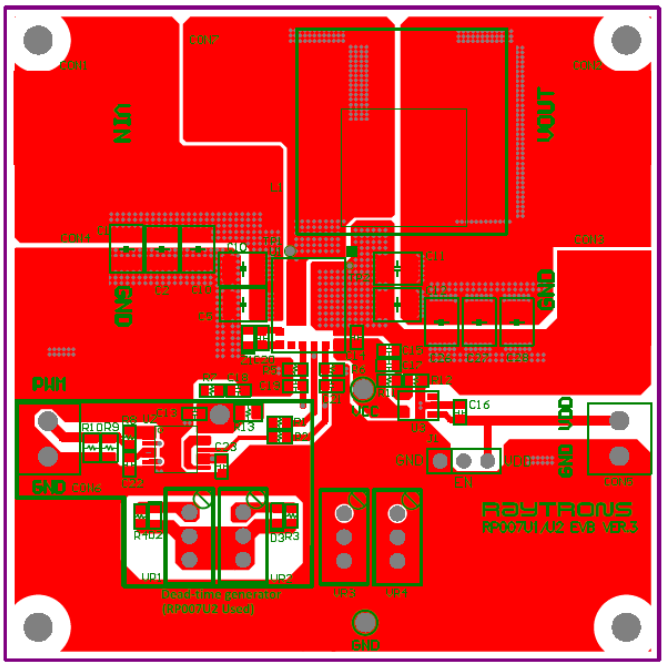


Figure 7 PCB Layout - Top Layer (L1)

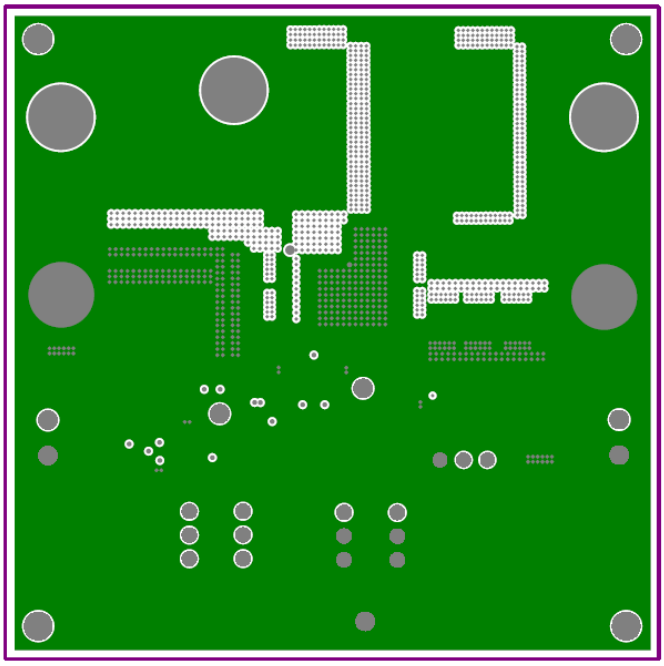


Figure 8 PCB Layout - Mid Layer 1 (L2)

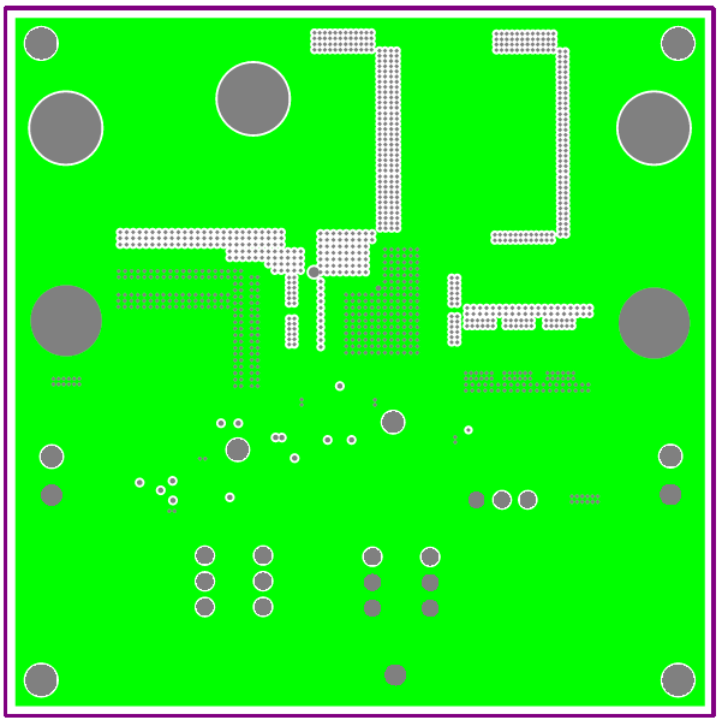


Figure 9 PCB Layout - Mid Layer 2 (L3)

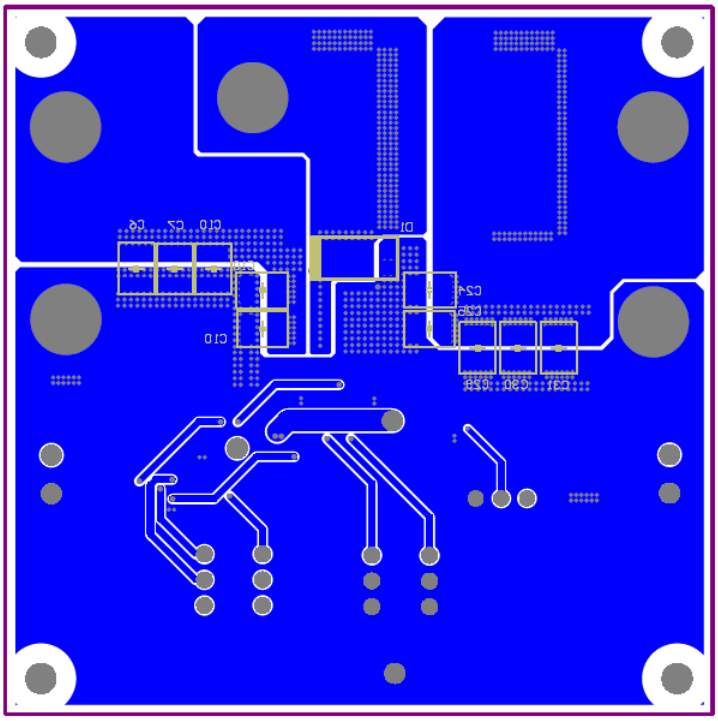


Figure 10 PCB Layout – Bottom Layer (L4)

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