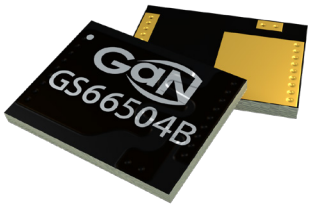
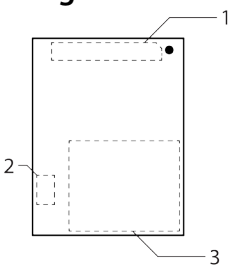
Features

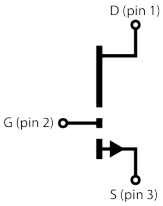
- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 100 mΩ
- $I_{DS(max)}$ = 15 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*™ package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 5.0 x 6.6 mm^2 PCB footprint
- RoHS 6 compliant



Package Outline



Circuit Symbol



The thermal pad is internally connected to Source, S (pin 3) and substrate

Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- Class D Audio amplifiers
- 400 V input DC-DC converters
- On Board Battery Chargers
- Traction Drive

Description

The GS66504B is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*™** packaging enables low inductance & low thermal resistance in a small package. The GS66504B is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	15	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	12.5	A

(1) Pulse $\leq$ 1 µs

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$		1.0		°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$		17		°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$		28		°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}			260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Part number	Package type	Ordering code	Packing method	Quantity
GS66504B	GaN*PX*™ Bottom-Side Cooled	GS66504B-TR	Tape-and-reel	3000
GS66504B	GaN*PX*™ Bottom-Side Cooled	GS66504B-MR	Mini-reel	250

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 25 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		100	130	mΩ	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 4.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		258		mΩ	V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 4.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_{DS} = 3.5 mA
Gate-to-Source Current	I_{GS}		80		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V, I_{DS} = 15 A
Drain-to-Source Leakage Current	I_{DSS}		1	25	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		200		µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 150 °C
Internal Gate Resistance	R_G		1.5		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		130		pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{OSS}		33		pF	
Reverse Transfer Capacitance	C_{RSS}		1		pF	
Effective Output Capacitance, Energy Related (Note 3)	$C_{O(ER)}$		44		pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (Note 4)	$C_{O(TR)}$		71		pF	
Total Gate Charge	Q_G		3.0		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		1.1		nC	
Gate-to-Drain Charge	Q_{GD}		0.84		nC	
Output Charge	Q_{OSS}		28.3		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Performance Graphs

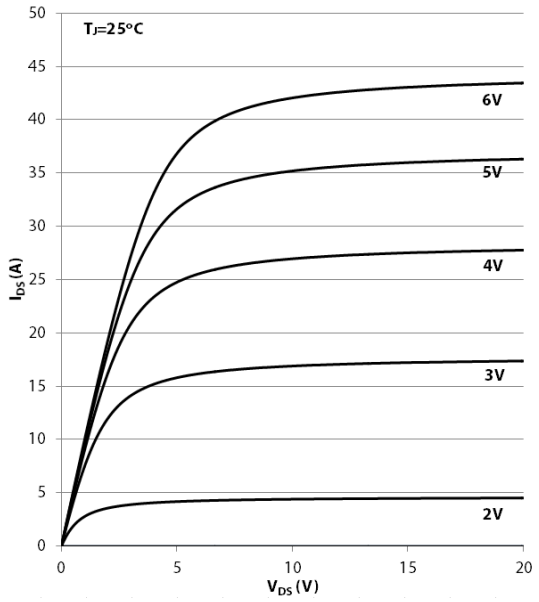


Figure 1 : Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

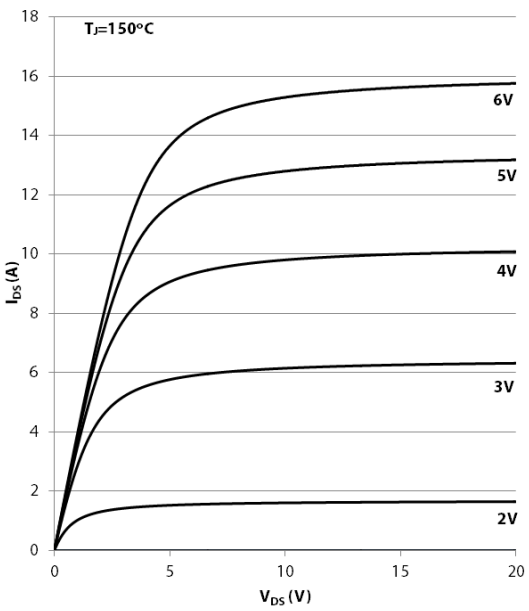


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

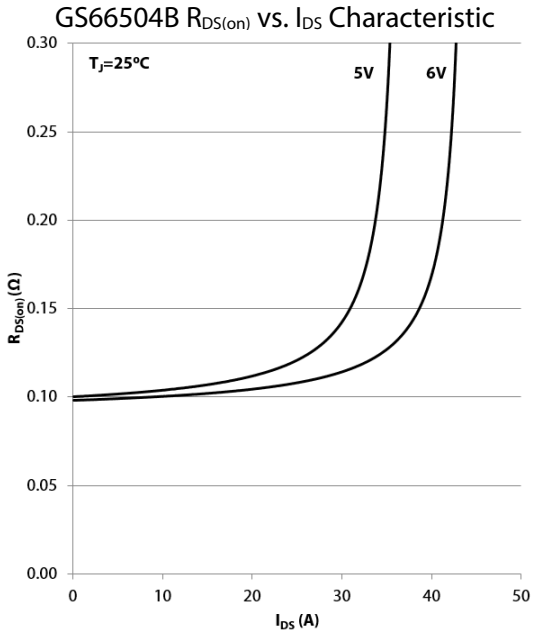


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

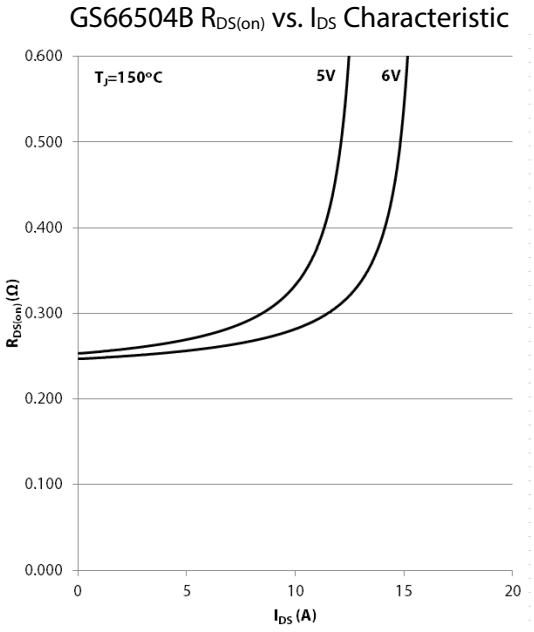


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

GS66504B I_{DS} vs. V_{DS} , T_J dependence

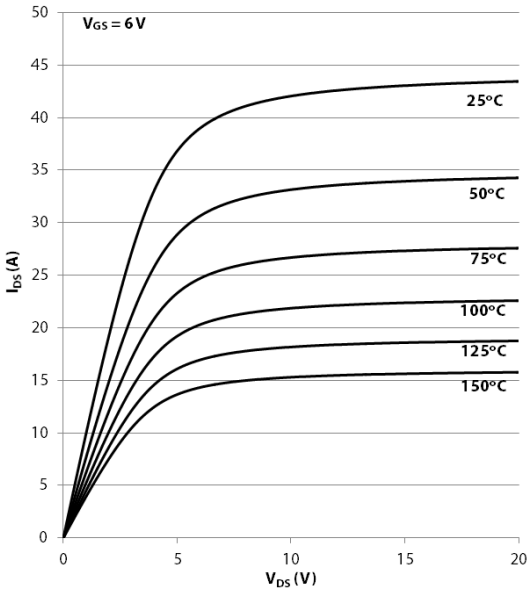


Figure 5 : Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

GS66504B Gate Charge, Q_G Characteristic

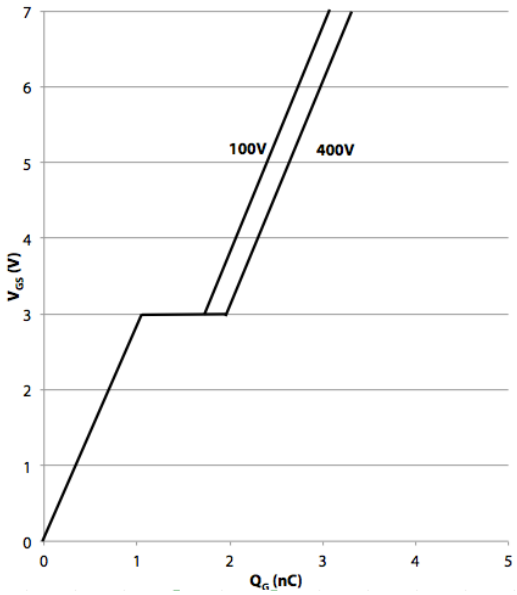


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

GS66504B Capacitance Characteristics

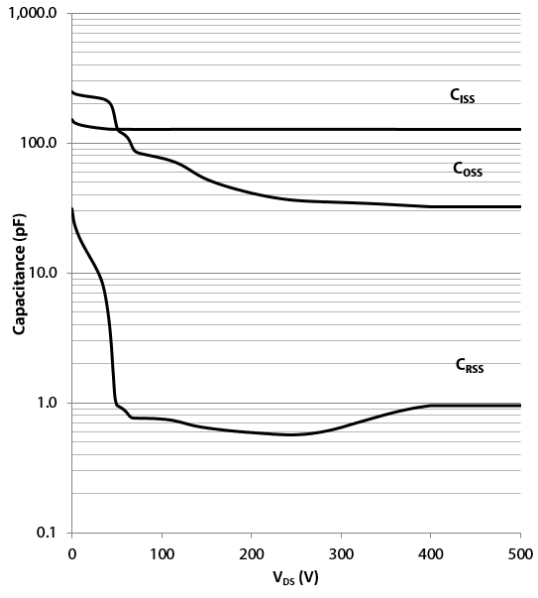


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS66504B Stored Energy Characteristic

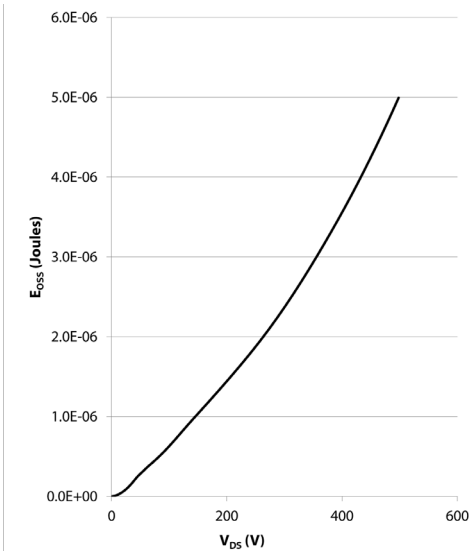


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

GS66504B Reverse Conduction Characteristics

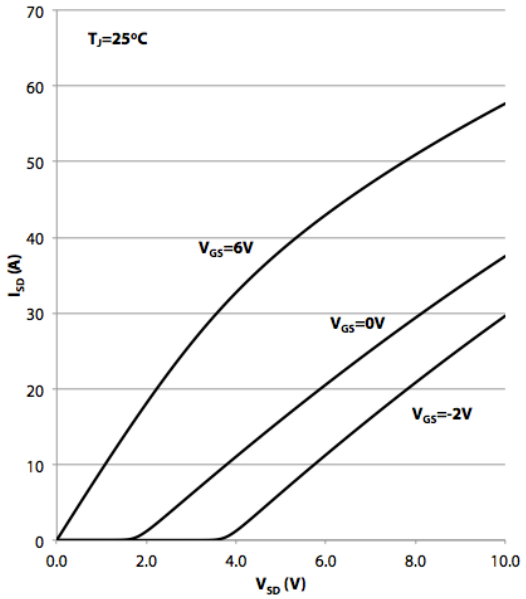


Figure 9 : Typical I_{SD} vs. V_{SD}

GS66504B I_{DS} vs. V_{GS} Characteristic

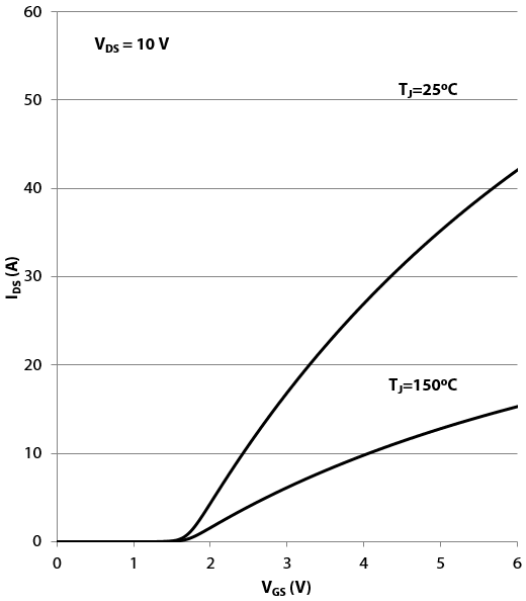


Figure 10 : Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

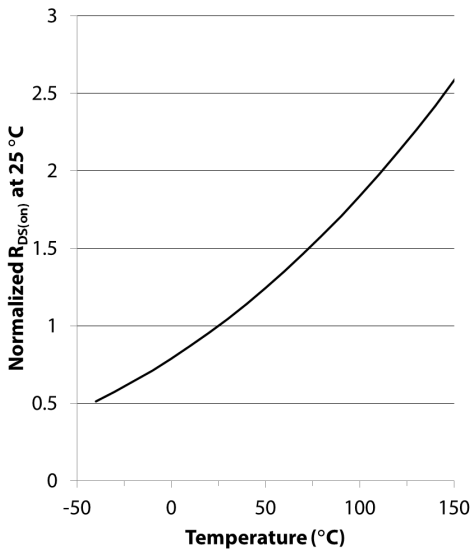


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

GS66504B I_{DS} - V_{DS} SOA

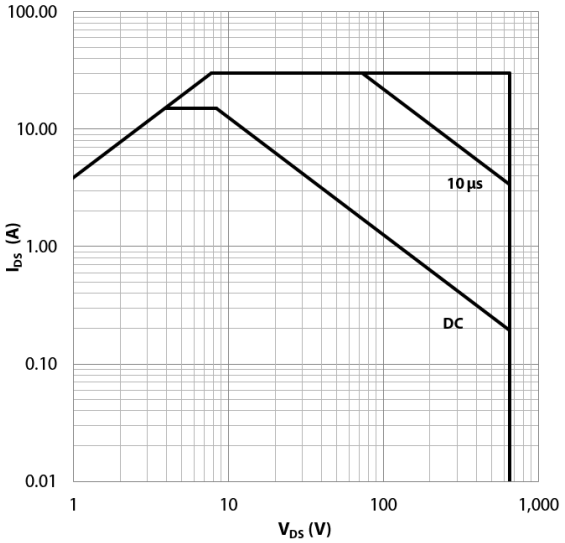


Figure 14: Safe Operating Area @ T_{case} = 25 °C

GS66504B Power Dissipation – Temperature Derating

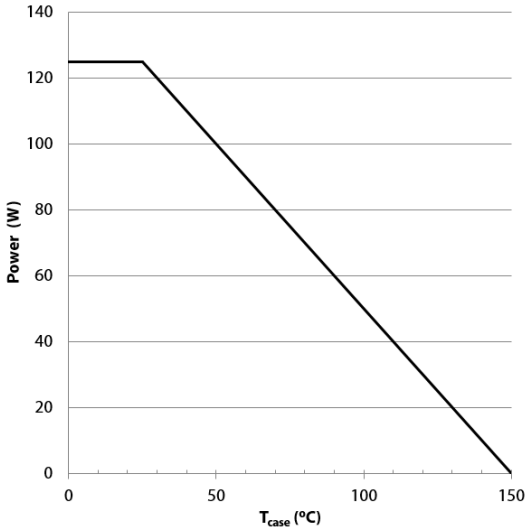


Figure 15: Power Derating vs. T_{case}

GS66504B Transient $R_{\theta JC}$

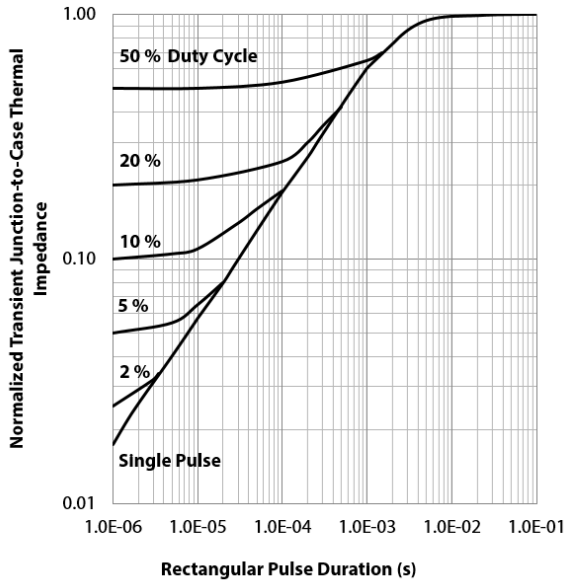


Figure 16: Transient Thermal Impedance

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" which can be found at www.gansystems.com.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note GN001 for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

Although the GS66504B does not have a dedicated source sense pin, the GaNPX™ packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the GS66504B. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However adding more copper under this pad will improve thermal performance by reducing the package temperature.

Reverse Conduction

GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for up to 1 µs is acceptable.

Packaging and Soldering

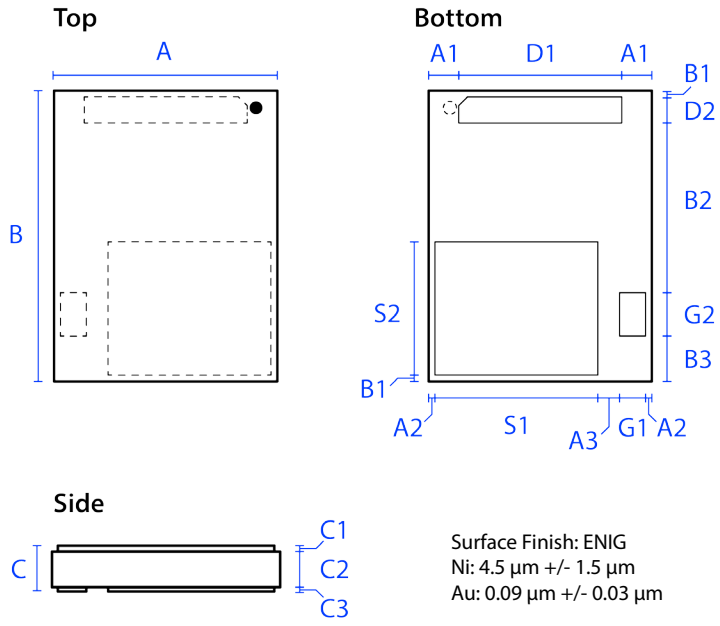
The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66504B device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Package Dimensions

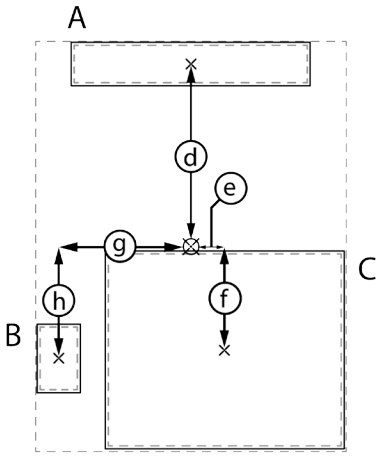


Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

	mm	Inches	
A	5.01	0.197	± 0.10 mm (0.004″)
A1	0.625	0.025	± 0.05 mm (0.002″)
A2	0.075	0.003	± 0.05 mm (0.002″)
A3	0.50	0.020	
B	6.56	0.258	± 0.10 mm (0.004″)
B1	0.075	0.003	± 0.05 mm (0.002″)
B2	3.91	0.154	
B3	0.975	0.038	± 0.05 mm (0.002″)
C	0.51	0.0201	± 0.05 mm (0.002″)
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	3.76	0.148	
D2	0.60	0.024	
G1	0.60	0.024	
G2	1.00	0.039	
S1	3.76	0.148	
S2	3.07	0.121	

Note: Inch measurements are approximate values

Recommended PCB Footprint



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.86	0.70	0.152	0.028
B	0.70	1.10	0.028	0.043
C	3.86	3.17	0.152	0.125

Dimensions

	mm	Inches
d	2.91	0.115
e	0.55	0.022
f	1.67	0.066
g	2.13	0.084
h	1.81	0.071

PCB pad openings
Package outline

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

GaN Systems:

GS66504B-E01-TY GS66504B-E01-MR