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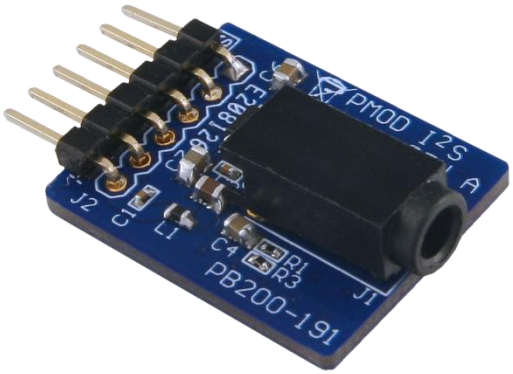
PmodI²S™ Reference Manual

Revised April 12, 2016
This manual applies to the PmodI²S rev. A

Overview

The Digilent PmodI2S is a stereo audio module that accepts all major audio data interface formats and sample rates.



The PmodI²S.

Features include:

- Stereo 24-bit D/A converter
- Output converted audio signals through standard headphone jack
- Supports all major audio data interface formats
- Accepts 16-24 bits of audio data
- Small PCB size for flexible designs 1.0 in × 0.8 in (2.5 cm × 2.0 cm)
- 6-pin Pmod port with GPIO interface

1 Functional Description

The PmodI2S utilizes a Cirrus Logic CS4344 Stereo D/A converter to take digital audio data and output the corresponding analog signal through a standard stereo headphone jack. It is designed to work at standard audio rates, although the master clock can run anywhere from 512 kHz to 50 MHz.

2 Interfacing with the Pmod

The PmodI2S communicates with the host board via the GPIO protocol. As this module uses the Integrated Interchip Sound (I²S) protocol, several different clock lines are required.

The fastest clock signal will be the Master Clock (MCLK); as the name implies, this signal will keep everything nicely synchronized. The sample rate (Fs) clock, also known as the Left-Right Clock (LRCK) or the Word Select (WS) clock, indicates when a particular set of data is to be placed on the left or right audio channel for stereo sound.

The final clock is the bit clock, labeled as the Serial Clock (SCK) on the Pmod. This clock can either be provided as a signal from the host board, or can be internally derived by the Pmod itself by providing at least two consecutive

frames of the LRCK without providing any SCK signals. The on-board chip will then measure the Master Clock rate and the LRCK rate and determine an appropriate bit clock rate. However, the MCLK/LRCK ratio must meet a set ratio in order to generate an internal SCK, as outlined in the table below from the CS4344 datasheet.

Internal SCK Mode	External SCK Mode
16-bit data and SCK = 32*Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64	Up to 24-bit data with data valid on the rising edge of SCK
Up to 24-bit data and SCK = 48*Fs if MCLK/LRCK = 768, 384, 192, or 96	
Up to 24-bit data and SCK = 72*Fs if MCLK/LRCK = 1152	

Table 1. MCLK/LRCK ratio.

The ratio between the MCLK and the LRCK rates must be an integer ratio so that the internal clock dividers can determine an appropriate bit rate. A table of commonly used sample rates and their corresponding MCLK rates from the CS4344 datasheet is provided below:

LRCK (kHz)	MCLK (MHz)									
	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.9120	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
Mode	QSM				DSM		SSM			

Table 2. Sample rates and corresponding MCLK rates.

The I²S protocol requires that data is clocked in on the falling edge of the bit clock. The first bit of data (MSB) is not clocked in on the falling edge until a first complete bit clock cycle has passed after the LRCK has changed state. The rising edge of the bit clock clock informs the on board chip that the next bit of data can be read.

The delay of one bit clock cycle before transferring data at each LRCK change also implies that the least significant bit (LSB) of data will be transferred after the LRCK change has occurred. No particular phase relationship must be followed with this on-board chip, although the phase relationship must stay consistent throughout audio session. An example timing diagram of I²S from Texas Instruments is shown below:

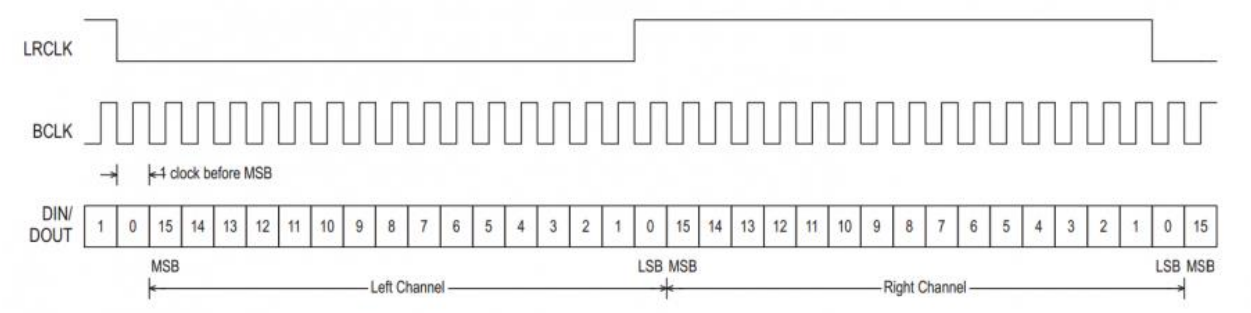


Figure 1. PmodI2S timing diagram.

Pin	Signal	Description
1	MCLK	Master Clock
2	LRCK	Left-right Clock
3	SCK	Serial Clock
4	SDIN	Serial Data input
5	GND	Power Supply Ground
6	VCC	Positive Power Supply

Table 3. Pinout description table.

Any external power applied to the PmodI2S must be within 3V and 5.25V; however, it is recommended that Pmod is operated at 3.3V.

3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 1 inch long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular to the pin header.

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