



BCM® Bus Converter

BCM384y120x800AC0



Fixed Ratio DC-DC Converter

Features

- Up to 800 W continuous output power
- 1177 W/in³ power density
- 97.4% peak efficiency
- 4242 Vdc isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 2361 through-hole ChiP package
 - 2.402" x 0.990" x 0.286"
(61.00 mm x 25.14 mm x 7.26 mm)

Typical Applications

- 380 DC Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

Product Ratings

| | |
|--|--------------------------------|
| $V_{IN} = 384 \text{ V (260 – 410 V)}$ | $P_{OUT} = \text{up to 800 W}$ |
| $V_{OUT} = 12 \text{ V (8.1 – 12.8 V)}$ (NO LOAD) | $K = 1/32$ |

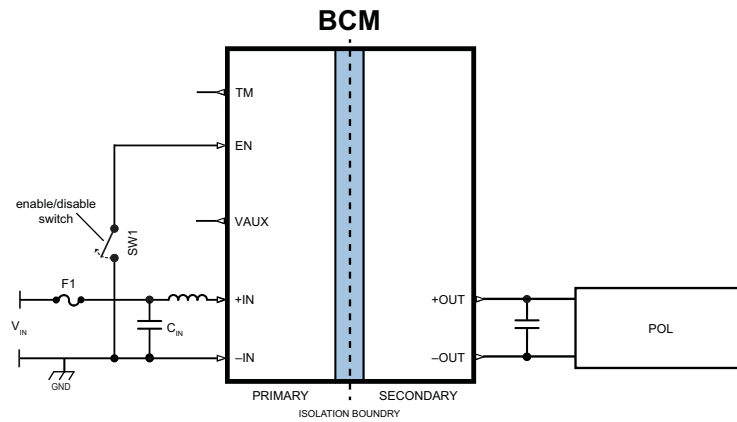
Product Description

The VI Chip® Bus Converter (BCM®) is a high efficiency Sine Amplitude Converter™ (SAC™), operating from a 260 to 410 VDC primary bus to deliver an isolated ratiometric output from 8.1 to 12.8 VDC.

The BCM384y120x800AC0 offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the input of the BCM module. With a K factor of 1/32, that capacitance value can be reduced by a factor of 1024x, resulting in savings of board area, material and total system cost.

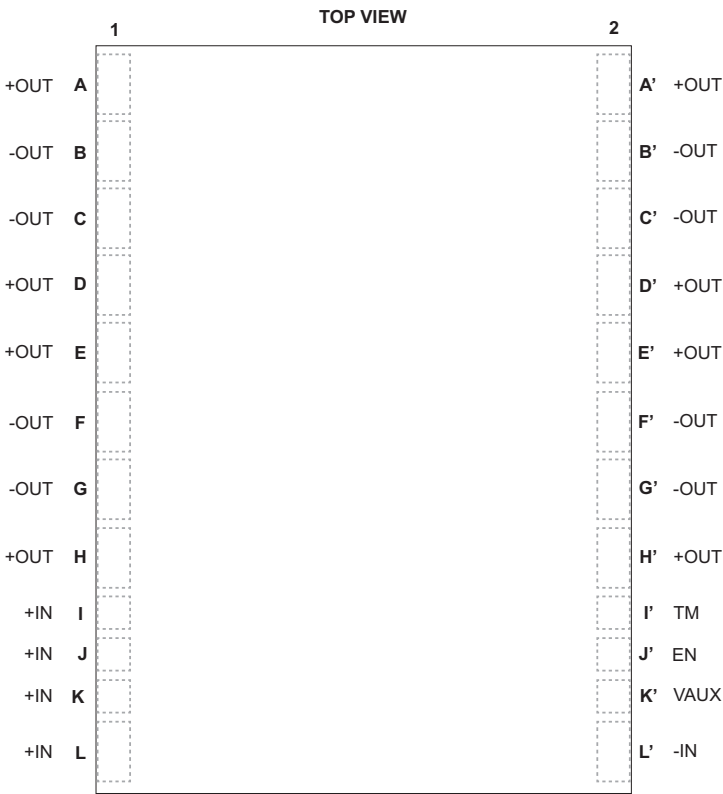
Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

Typical Application



BCM384y120x800AC0 + Point of load

Pin Configuration



2361 ChiP Package and Through hole device

Part Ordering Information

| Device | Input Voltage Range | Package Type | Output Voltage x 10 | Temperature Grade | Output Power | Revision | Package Size | Version |
|-----------|---------------------|-----------------------|---------------------|--------------------------------------|--------------|----------|--------------|---------|
| BCM | 384 | y | 120 | x | 800 | A | C | 0 |
| BCM = BCM | 384 = 260 to 410 V | P = ChiP Through Hole | 120 = 12 V | T = -40 to 125°C M = -55 to 125°C | 800 = 800 W | A | C = 2361 | 0 |

All products shipped in JEDEC compliant trays.

Standard Models

| Part Number | V _{IN} | Package Type | V _{OUT} | Temperature | Power | Package Size |
|-------------------------------------|-----------------|--|-----------------------|----------------|-------|--------------|
| BCM384 P 120 T 800AC0 | 260 to 410 V | ChiP Through Hole | 12 V 8.1 to 12.8 V | -40°C to 125°C | 800 W | 2361 |
| BCM384 P 120 M 800AC0 | 260 to 410 V | ChiP Through Hole ChiP Through Hole | 12 V 8.1 to 12.8 V | -55°C to 125°C | 800 W | 2361 |

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|---|--|-------|------|------|
| +IN to -IN | | -1 | 480 | V |
| V _{IN} slew rate (operational) | | -1000 | 1000 | V/ms |
| Isolation voltage, input to output | Dielectric test applied to 100% production units | | 4242 | V |
| +OUT to -OUT | | -1 | 15 | V |
| TM to -IN | | -0.3 | 4.6 | V |
| EN to -IN | | -0.3 | 5.5 | V |
| VAUX to -IN | | -0.3 | 4.6 | V |

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---------------------------|---|--------------|------|-------------|---------------|
| Powertrain | | | | | | |
| Input voltage range, continuous | $V_{\text{IN_DC}}$ | | 260 | | 410 | V |
| Input voltage range, transient | $V_{\text{IN_TRANS}}$ | Full current or power supported, 50 ms max, 10% duty cycle max | 260 | | 410 | V |
| V_{IN} μ Controller Active | $V_{\mu\text{C_ACTIVE}}$ | V_{IN} voltage where μC is initialized, (ie VAUX = Low, powertrain inactive) | | | 130 | V |
| Input Voltage Slew Rate | dV_{IN}/dt | $V_{\text{IN_UVLO-}} \leq V_{\text{IN}} \leq V_{\text{IN_OVLO+}}$ | 0.001 | | 1000 | V/ms |
| Quiescent current | I_{Q} | Disabled, EN Low, $V_{\text{IN}} = 384\text{ V}$ | | 2 | | mA |
| | | $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 4 | |
| No load power dissipation | P_{NL} | $V_{\text{IN}} = 384\text{ V}$, $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ | | 9.3 | 13 | W |
| | | $V_{\text{IN}} = 384\text{ V}$ | 5 | | 20 | |
| | | $V_{\text{IN}} = 260\text{ V}$ to 410 V , $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ | | | 16 | |
| | | $V_{\text{IN}} = 260\text{ V}$ to 410 V | | | 22 | |
| Inrush current peak | $I_{\text{INR_P}}$ | $V_{\text{IN}} = 410\text{ V}$, $C_{\text{OUT}} = 1000\text{ }\mu\text{F}$, $R_{\text{LOAD}} = 25\%$ of full load current | | 10 | | A |
| | | $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 15 | |
| DC input current | $I_{\text{IN_DC}}$ | At $P_{\text{OUT}} = 800\text{ W}$, $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 2.2 | A |
| Transformation ratio | K | $K = V_{\text{OUT}}/V_{\text{IN}}$, at no load | | 1/32 | | V/V |
| Output power (average) | $P_{\text{OUT_AVG}}$ | See Figure 1 | | | 800 | W |
| Output power (peak) | $P_{\text{OUT_PK}}$ | 10 ms max, $P_{\text{OUT}} \leq 50\% P_{\text{OUT_AVG}}$ | | | 1100 | W |
| Output current (average) | $I_{\text{OUT_AVG}}$ | | | | 68 | A |
| Output current (peak) | $I_{\text{OUT_PK}}$ | 10 ms max, $I_{\text{OUT}} \leq 50\% I_{\text{OUT_AVG}}$ | | | 91 | A |
| Efficiency (ambient) | η_{AMB} | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 68\text{ A}$ | 96.2 | 97.2 | | % |
| | | $V_{\text{IN}} = 260\text{ V}$ to 410 V , $I_{\text{OUT}} = 68\text{ A}$ | 95.7 | | | |
| | | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 34\text{ A}$ | 96.3 | 97 | | |
| Efficiency (hot) | η_{HOT} | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 68\text{ A}$; $T_{\text{INTERNAL}} = 100^{\circ}\text{C}$ | 96 | 97 | | % |
| Efficiency (over load range) | $\eta_{20\%}$ | $14\text{ A} < I_{\text{OUT}} < 68\text{ A}$, $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | 90 | | | % |
| Output resistance | $R_{\text{OUT_COLD}}$ | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 68\text{ A}$, $T_{\text{INTERNAL}} = -40^{\circ}\text{C}$ | 1.0 | 1.65 | 2.2 | m Ω |
| | $R_{\text{OUT_AMB}}$ | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 68\text{ A}$ | 1.6 | 2.3 | 2.9 | |
| | $R_{\text{OUT_HOT}}$ | $V_{\text{IN}} = 384\text{ V}$, $I_{\text{OUT}} = 68\text{ A}$, $T_{\text{INTERNAL}} = 100^{\circ}\text{C}$ | 2.3 | 2.9 | 3.4 | |
| Switching frequency | F_{SW} | Frequency of the Output Voltage Ripple = $2x F_{\text{SW}}$ | 0.97 | 1.03 | 1.09 | MHz |
| Output voltage ripple | $V_{\text{OUT_PP}}$ | $C_{\text{OUT}} = 0\text{ F}$, $I_{\text{OUT}} = 68\text{ A}$, $V_{\text{IN}} = 384\text{ V}$, 20 MHz BW | | 210 | | mV |
| | | $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 300 | |
| Input inductance (parasitic) | $L_{\text{IN_PAR}}$ | Frequency 2.5 MHz (double switching frequency), Simulated lead model | | 7 | | nH |
| Output inductance (parasitic) | $L_{\text{OUT_PAR}}$ | Frequency 2.5 MHz (double switching frequency), Simulated lead model | | 0.64 | | nH |
| Input Series inductance (internal) | $L_{\text{IN_INT}}$ | Reduces the need for input decoupling inductance in BCM arrays | | 0.56 | | μH |
| Effective Input capacitance (internal) | $C_{\text{IN_INT}}$ | Effective value at 384 V_{IN} | | 0.25 | | μF |

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|-----------------------------|--|--------------|-------|--------------|--------------------|
| Powertrain (Cont.) | | | | | | |
| Effective Output capacitance (internal) | $C_{\text{OUT_INT}}$ | Effective value at 12 V_{OUT} | | 104 | | μF |
| Effective Output capacitance (external) | $C_{\text{OUT_EXT}}$ | Excessive capacitance may drive module into SC protection | 0 | | 1000 | μF |
| Array Maximum external output capacitance | $C_{\text{OUT_AEXT}}$ | $C_{\text{OUT_AEXT Max}} = N * 0.5 * C_{\text{OUT_EXT Max}}$ | | | | |
| Protection | | | | | | |
| Auto Restart Time | $t_{\text{AUTO_RESTART}}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{\text{IN}} > V_{\text{IN_UVLO+}}$ | 292.5 | | 357.5 | ms |
| Input overvoltage lockout threshold | $V_{\text{IN_OVLO+}}$ | | 420 | 434.5 | 450 | V |
| Input overvoltage recovery threshold | $V_{\text{IN_OVLO-}}$ | | 410 | 424 | 440 | V |
| Input overvoltage lockout hysteresis | $V_{\text{IN_OVLO_HYST}}$ | | | 10.5 | | V |
| Overvoltage lockout response time | t_{OVLO} | | | 100 | | μs |
| Input undervoltage lockout threshold | $V_{\text{IN_UVLO-}}$ | | 195 | 221 | 250 | V |
| Input undervoltage recovery threshold | $V_{\text{IN_UVLO+}}$ | | 225 | 243 | 255 | V |
| Input undervoltage lockout hysteresis | $V_{\text{IN_UVLO_HYST}}$ | | | 15 | | V |
| Undervoltage lockout response time | t_{UVLO} | | | 100 | | μs |
| Undervoltage startup delay | $t_{\text{UVLO+_DELAY}}$ | From $V_{\text{IN}} = V_{\text{IN_UVLO+}}$ to powertrain active, EN floating (i.e One time Startup delay from application of V_{IN} to V_{OUT}) | | 20 | | ms |
| Soft-Start time | $t_{\text{SOFT-START}}$ | From powertrain active Fast Current limit protection disabled during Soft-Start | | 1 | | ms |
| Output overcurrent trip threshold | I_{OCP} | | 75 | 85 | 110 | A |
| Output overcurrent response time constant | t_{OCP} | Effective internal RC filter | | 3 | | ms |
| Short circuit protection trip threshold | I_{SCP} | | 105 | | | A |
| Short circuit protection response time | t_{SCP} | | | 1 | | μs |
| Overtemperature shutdown threshold | t_{OTP} | Temperature sensor located inside controller IC | 125 | | | $^{\circ}\text{C}$ |
| Undertemperature shutdown threshold | t_{UTP} | Temperature sensor located inside controller IC | | | -45 | $^{\circ}\text{C}$ |
| Undertemperature Restart time | $t_{\text{UTP_RESTART}}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{\text{IN}} > V_{\text{IN_UVLO+}}$ | | 3 | | s |

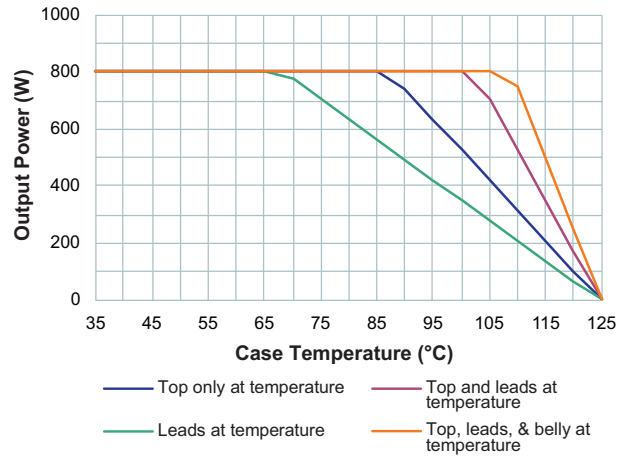


Figure 1 — Specified thermal operating area

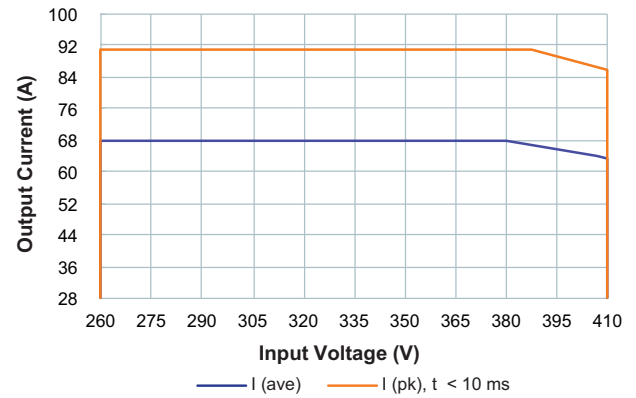
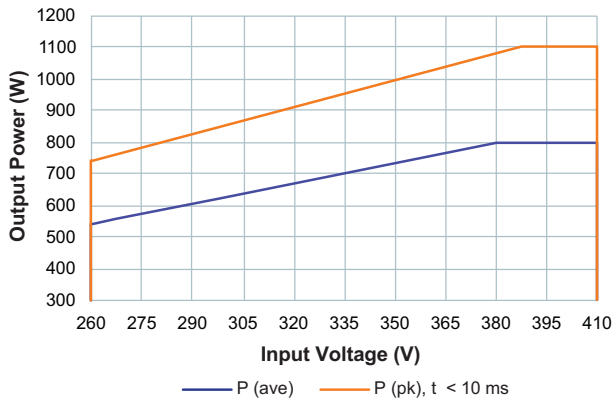


Figure 2 — Specified electrical operating area

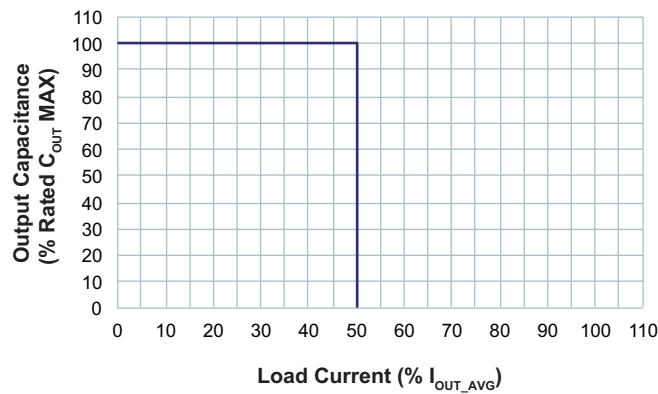


Figure 3 — Safe operating area; start up load current vs. output capacitance

Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Temperature Monitor | | | | | | | | |
|---|-------------------|--|----------------------|---|--------------|------------|--------------|------------------------|
| <ul style="list-style-type: none"> The TM pin is a standard analog I/O configured as an output from an internal μC. μC 250 kHz PWM output internally pulled high to 3.3 V. The TM pin monitors the internal temperature of the controller IC within an accuracy of $\pm 5^{\circ}\text{C}$. | | | | | | | | |
| SIGNAL TYPE | STATE | ATTRIBUTE | SYMBOL | CONDITIONS / NOTES | MIN | TYP | MAX | UNIT |
| DIGITAL OUTPUT | Start Up | Powertrain active to TM time | t_{VAUX} | Powertrain active to TM PWM | | 100 | | μs |
| | Regular Operation | TM Duty Cycle | V_{TM} | | 18.18 | | 68.18 | % |
| | | TM Current | I_{TM} | | | | 4 | mA |
| | | Recommended External filtering: | | | | | | |
| | | TM Capacitance (External) | $C_{\text{TM_EXT}}$ | Recommended External filtering | | 0.01 | | μF |
| | | TM Resistance (External) | $R_{\text{TM_EXT}}$ | Recommended External filtering | | 1 | | k Ω |
| | | Specifications using recommended filter: | | | | | | |
| | | TM Gain | A_{TM} | | | 10 | | mV/ $^{\circ}\text{C}$ |
| | | TM Voltage Reference | $V_{\text{TM_AMB}}$ | Controller $T_{\text{INTERNAL}} = 27^{\circ}\text{C}$ | | 1.27 | | V |
| | | TM Voltage Ripple | $V_{\text{TM_PP}}$ | $R_{\text{TM_EXT}} = 1 \text{ K}\Omega$, $C_{\text{TM_EXT}} = 0.01 \mu\text{F}$, $V_{\text{IN}} = 384 \text{ V}$, $I_{\text{OUT}} = 68 \text{ A}$ | | 28 | | mV |
| | | | | $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 40 | mV |

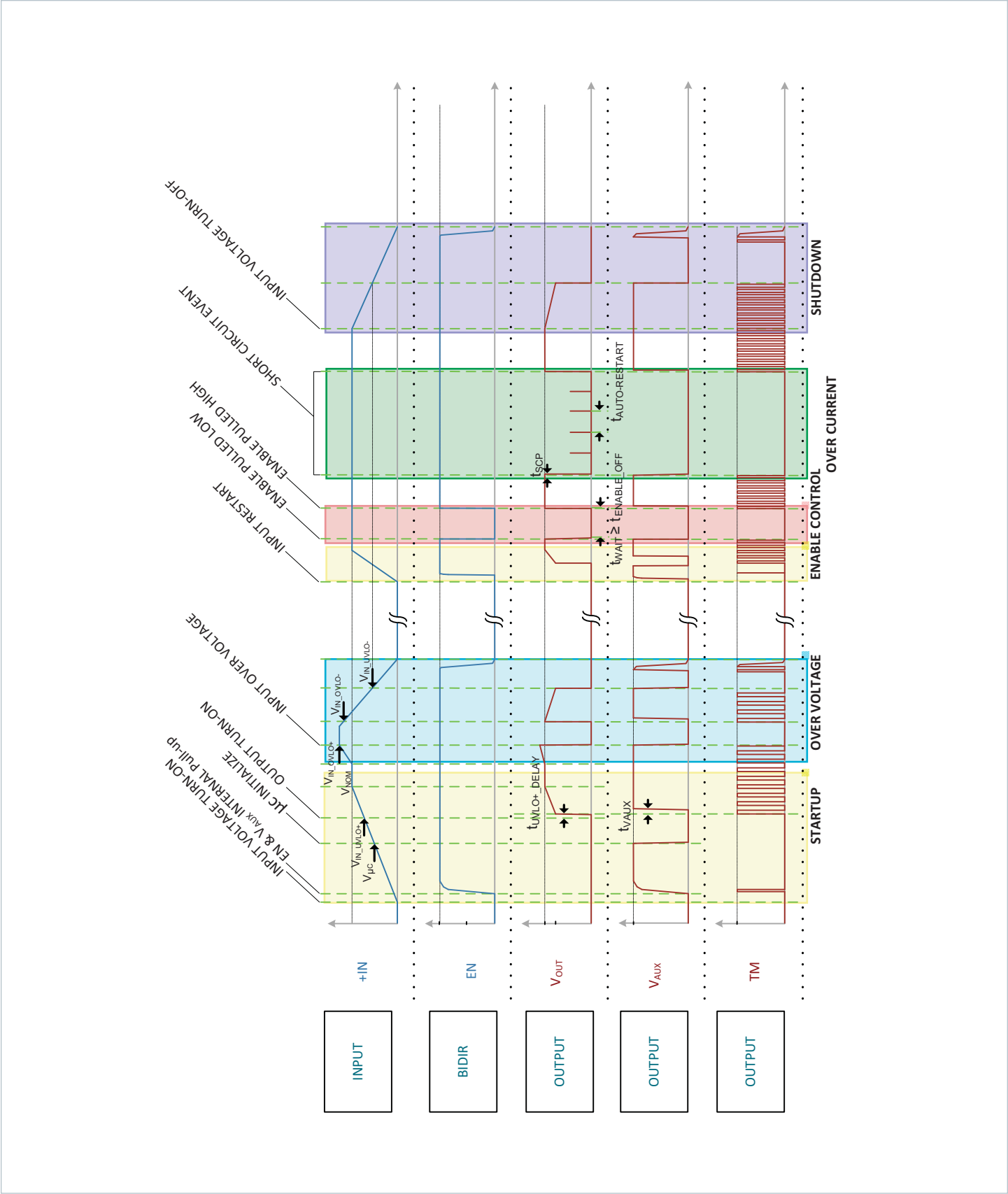
| ENABLE Control | | | | | | | | |
|--|-------------------|------------------------------|------------------------------|--|--------------|------------|--------------|---------------|
| <ul style="list-style-type: none"> The EN pin is a standard analog I/O configured as an input to an internal μC. It is internally pulled high to 3.3 V. When held low the BCM[®] internal bias will be disabled and the powertrain will be inactive. In an array of BCMs, EN pins should be interconnected to synchronize startup and permit startup into full load conditions. | | | | | | | | |
| SIGNAL TYPE | STATE | ATTRIBUTE | SYMBOL | CONDITIONS / NOTES | MIN | TYP | MAX | UNIT |
| ANALOG INPUT | Start Up | EN to Powertrain active time | $t_{\text{EN_START}}$ | $V_{\text{IN}} > V_{\text{IN_UVLO+}}$, EN held low both conditions satisfied for $t > t_{\text{UVLO+_DELAY}}$ | | 250 | | μs |
| | Regular Operation | EN Voltage Threshold | $V_{\text{EN_TH}}$ | | 2.3 | | | V |
| | | EN Resistance (Internal) | $R_{\text{EN_INT}}$ | Internal pull up resistor | | 1.5 | | k Ω |
| | | EN Disable Threshold | $V_{\text{EN_DISABLE_TH}}$ | | | | 1 | V |
| | Fault | Time off | $t_{\text{ENABLE_OFF}}$ | Module will ignore attempts to re-enable during time off | 292.5 | | 357.5 | ms |

Signal Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

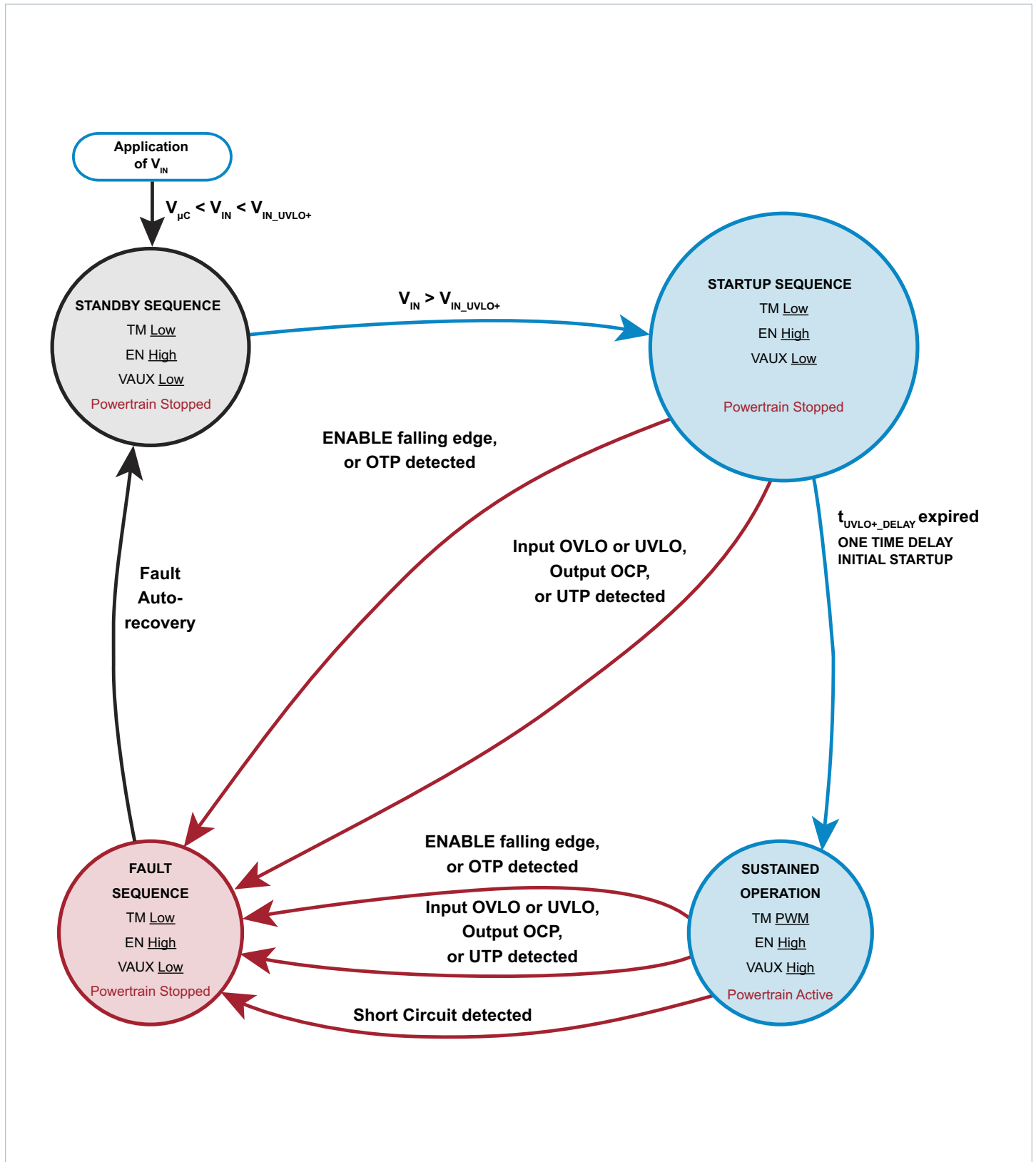
| Auxiliary Voltage Source | | | | | | | | |
|---|-------------------|--------------------------------|------------------------|---|------------|----------|------------|---------------|
| <ul style="list-style-type: none"> The VAUX pin is a standard analog I/O configured as an output from an internal μC. VAUX is internally connected to μC output as internally pulled high to a 3.3 V regulator with 2% tolerance, a 1% resistor of 1.5 kΩ. VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2 ms delay from the start of powertrain activating, signaling the end of softstart. VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected. | | | | | | | | |
| SIGNAL TYPE | STATE | ATTRIBUTE | SYMBOL | CONDITIONS / NOTES | MIN | TYP | MAX | UNIT |
| ANALOG OUTPUT | Start Up | Powertrain active to VAUX time | t_{VAUX} | Powertrain active to VAUX high | | 2 | | ms |
| | Regular Operation | VAUX Voltage | V_{VAUX} | $0 < I_{\text{VAUX}} < 4 \text{ mA}$ | 2.8 | | 3.3 | V |
| | | VAUX Available Current | I_{VAUX} | | | | 4 | mA |
| | | VAUX Voltage Ripple | $V_{\text{VAUX_PP}}$ | | | 50 | | mV |
| | | | | $T_{\text{INTERNAL}} \leq 100^{\circ}\text{C}$ | | | 100 | mV |
| | | VAUX Capacitance (External) | $C_{\text{VAUX_EXT}}$ | | | | 0.01 | μF |
| | | VAUX Resistance (External) | $R_{\text{VAUX_EXT}}$ | $V_{\text{IN}} < V_{\mu\text{C_ACTIVE}}$ | 1.5 | | | k Ω |
| | Fault | VAUX Fault Response Time | $t_{\text{FR_TM}}$ | From fault detection to VAUX = 2.8 V, $C_{\text{VAUX}} = 0 \text{ pF}$ | | 10 | | μs |

BCM Module Timing diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. See associated figures for general trend data.

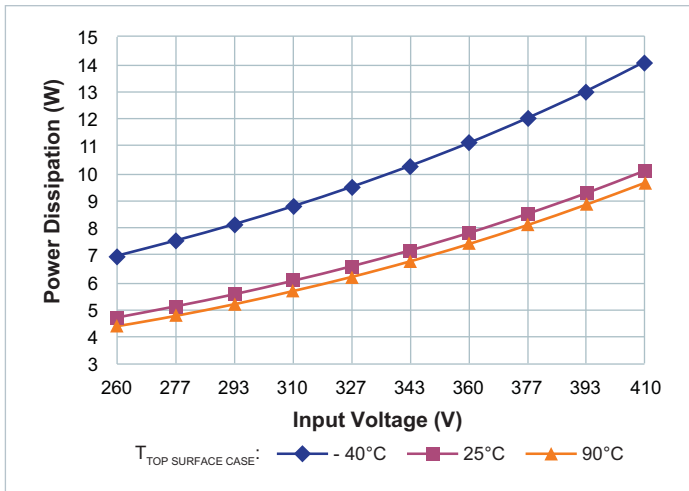


Figure 4 — No load power dissipation vs. V_{IN}

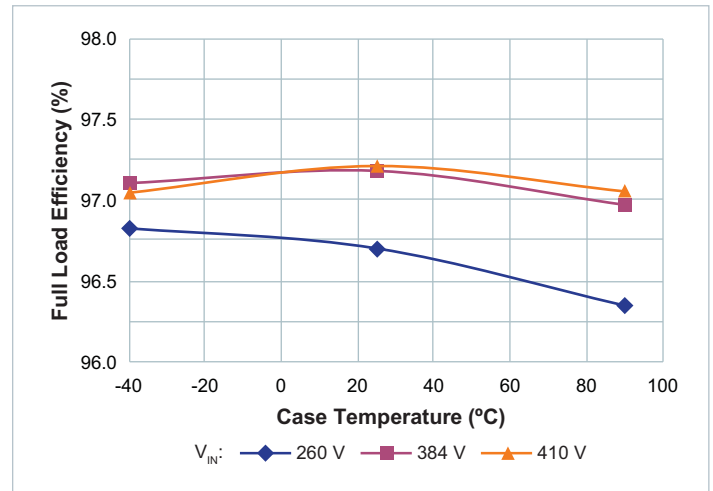


Figure 5 — Full load efficiency vs. temperature; V_{IN}

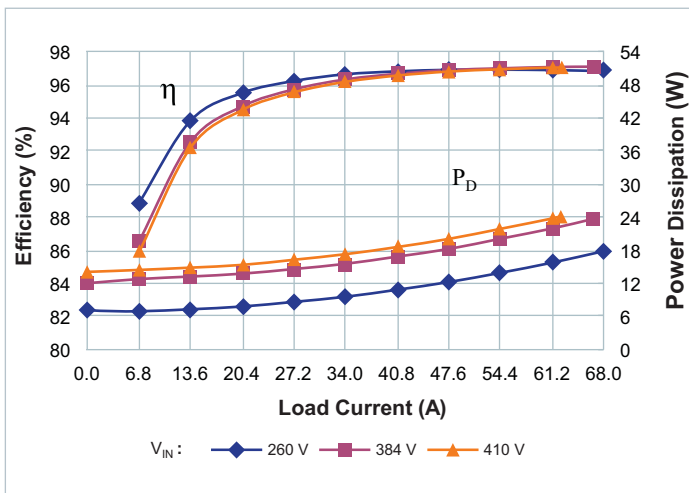


Figure 6 — Efficiency and power dissipation at $T_{CASE} = -40^{\circ}\text{C}$

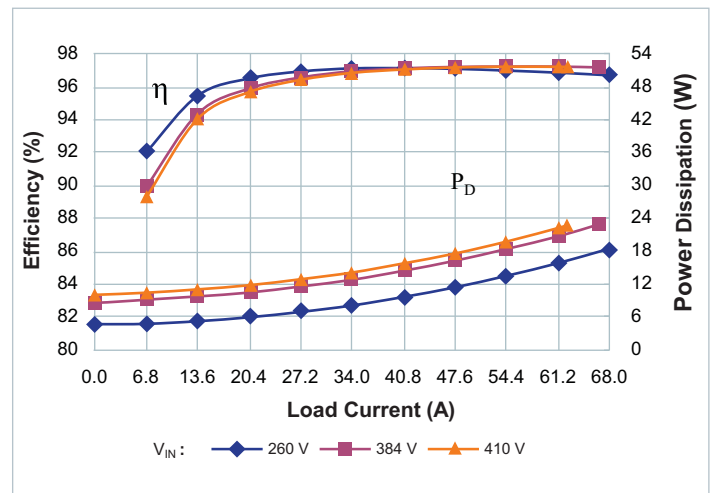


Figure 7 — Efficiency and power dissipation at $T_{CASE} = 25^{\circ}\text{C}$

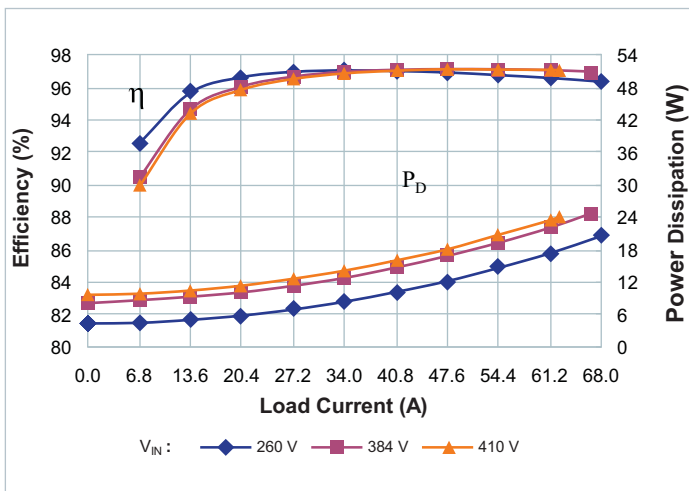


Figure 8 — Efficiency and power dissipation at $T_{CASE} = 90^{\circ}\text{C}$

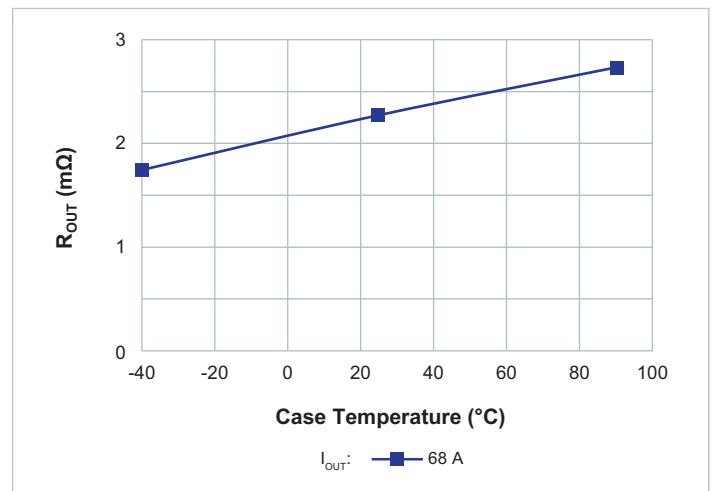


Figure 9 — R_{OUT} vs. temperature; Nominal V_{IN}

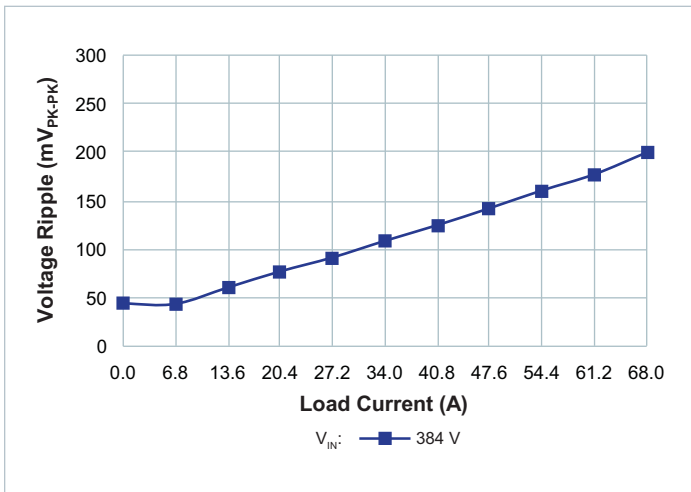


Figure 10 — V_{RIPPLE} VS. I_{OUT} ; No external C_{OUT} . Board mounted module, scope setting : 20 MHz analog BW

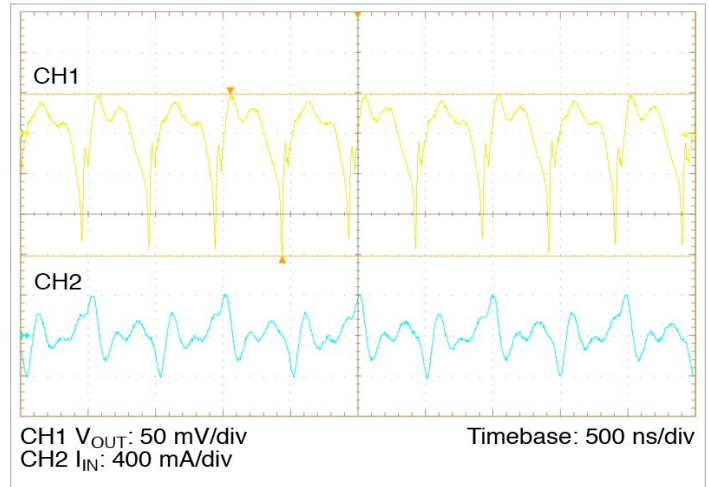


Figure 11 — Full load ripple, 270 μ F C_{IN} ; No external C_{OUT} . Board mounted module, scope setting : 20 MHz analog BW

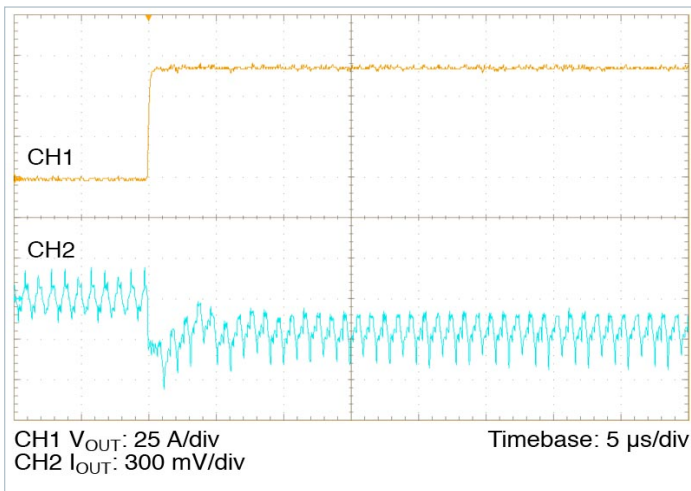


Figure 12 — 0 A – 68 A transient response: $C_{IN} = 270 \mu$ F, no external C_{OUT}

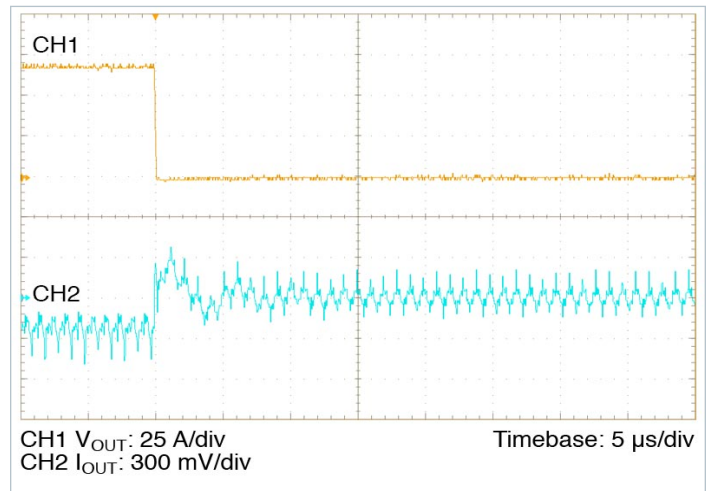


Figure 13 — 68 A – 0 A transient response: $C_{IN} = 270 \mu$ F, no external C_{OUT}

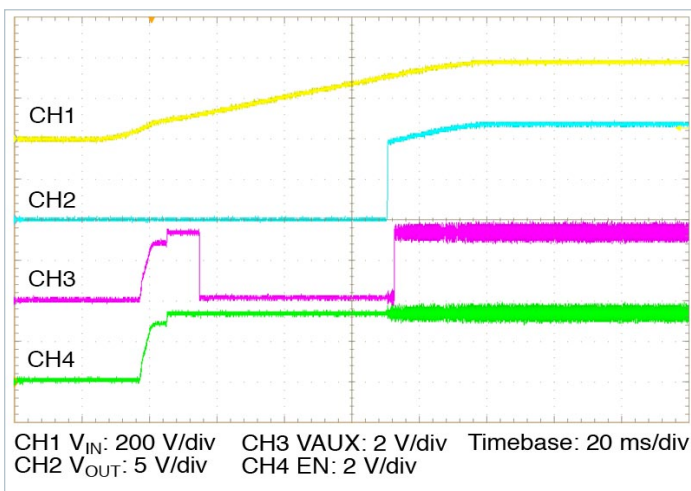


Figure 14 — Start up from application of $V_{IN} = 384$ V, 50% I_{OUT} , 100% C_{OUT}

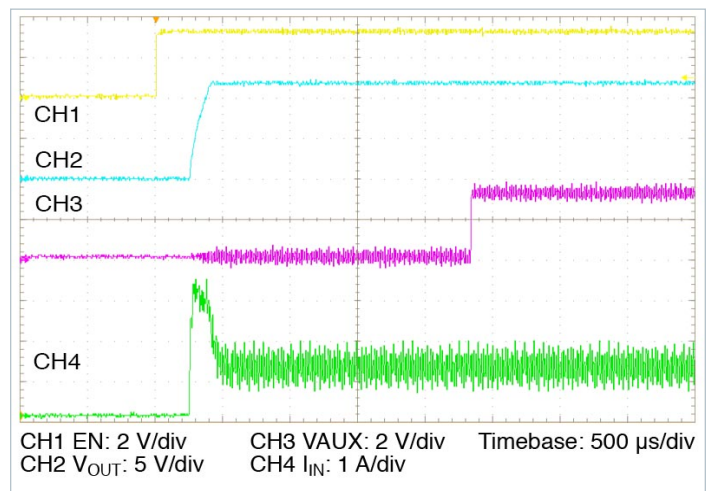


Figure 15 — Start up from application of EN with pre-applied $V_{IN} = 384$ V, 50% I_{OUT} , 100% C_{OUT}

General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|--------------------------------|-------------------------|---|-----------------|-----------------|-----------------|------------|
| | | | | | | |
| | | Mechanical | | | | |
| Length | L | | 60.87 / [2.396] | 61.00 / [2.402] | 61.13 / [2.407] | mm / [in] |
| Width | W | | 24.76 / [0.975] | 25.14 / [0.990] | 25.52 / [1.005] | mm / [in] |
| Height | H | | 7.21 / [0.284] | 7.26 / [0.286] | 7.31 / [0.288] | mm / [in] |
| Volume | Vol | Without heatsink | | 11.13 / [0.679] | | cm³/ [in³] |
| Weight | W | | | 41 / [1.45] | | g / [oz] |
| Lead finish | | Nickel | 0.51 | | 2.03 | µm |
| | | Palladium | 0.02 | | 0.15 | |
| | | Gold | 0.003 | | 0.051 | |
| | | | | | | |
| | | Thermal | | | | |
| Operating temperature | T _{INTERNAL} | BCM384P120T800AC0 (T-Grade) | -40 | | 125 | °C |
| | | BCM384P120M800AC0 (M-Grade) | -55 | | 125 | °C |
| Thermal resistance top side | ϕ _{INT-TOP} | Estimated thermal resistance to maximum temperature internal component from isothermal top | | 1.35 | | °C/W |
| Thermal resistance leads | ϕ _{INT-LEADS} | Estimated thermal resistance to maximum temperature internal component from isothermal leads | | 2 | | °C/W |
| Thermal resistance bottom side | ϕ _{INT-BOTTOM} | Estimated thermal resistance to maximum temperature internal component from isothermal bottom | | 1.91 | | °C/W |
| Thermal capacity | | | | 34 | | Ws /°C |
| | | | | | | |
| | | Assembly | | | | |
| Storage Temperature | T _{ST} | BCM384P120T800AC0 (T-Grade) | -55 | | 125 | °C |
| | | BCM384P120M800AC0 (M-Grade) | -65 | | 125 | °C |
| ESD Withstand | ESD _{HBM} | Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV) | | | | |
| | ESD _{CDM} | Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V) | | | | |

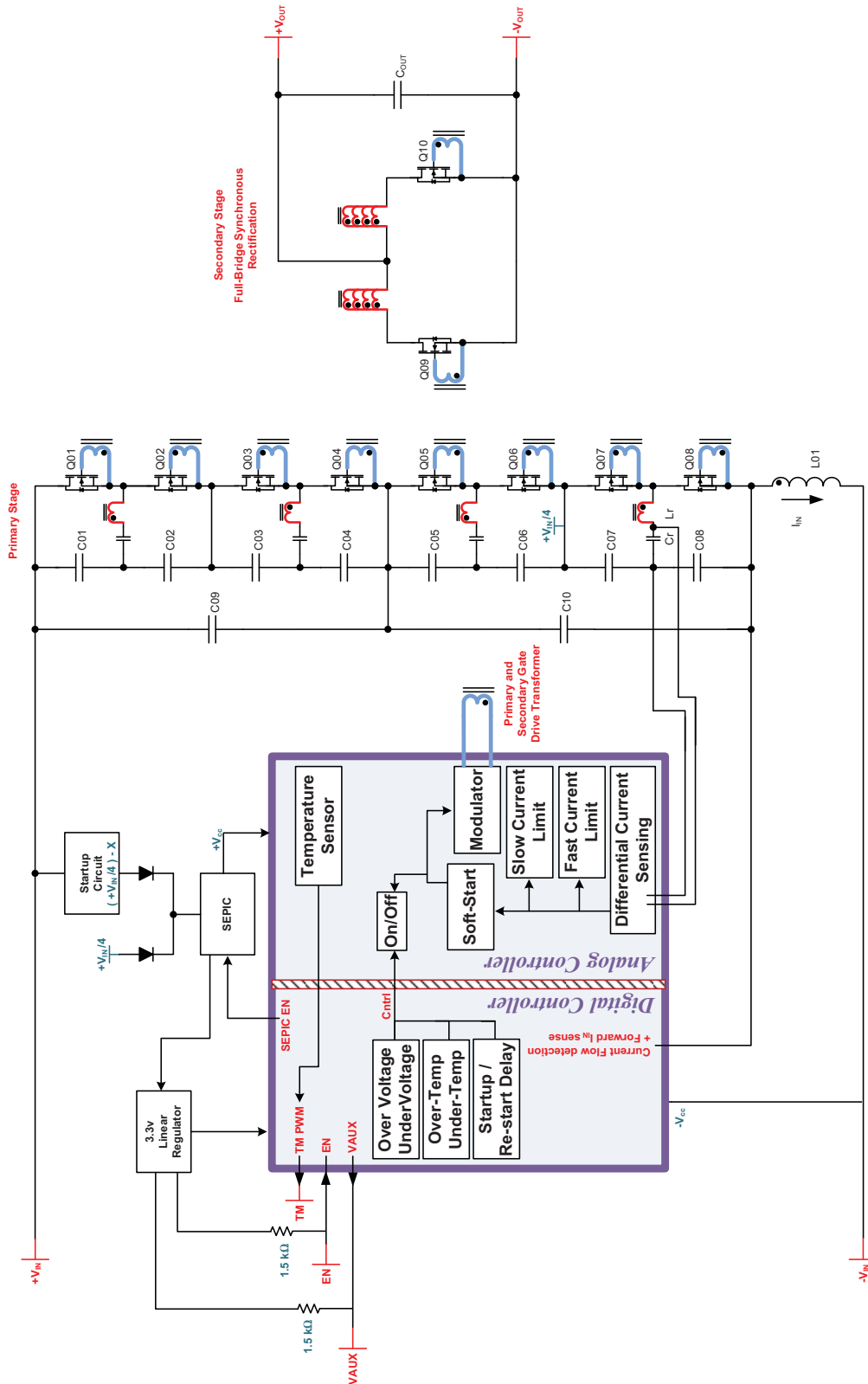
General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{INTERNAL}} \leq 125^{\circ}\text{C}$ (T-Grade); All other specifications are at $T_{\text{INTERNAL}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|-------------------------------------|----------------------|---|--------------|------------|------------|--------------------|
| | | Soldering ^[1] | | | | |
| Peak temperature Top case | | | | | 135 | $^{\circ}\text{C}$ |
| | | Safety | | | | |
| Isolation voltage / Dielectric test | V_{HIPOT} | IN to OUT | 4,242 | | | Vdc |
| | | IN to CASE | 2,121 | | | |
| | | OUT to CASE | 2,121 | | | |
| Isolation capacitance | $C_{\text{IN_OUT}}$ | Unpowered unit | 620 | 780 | 940 | pF |
| Isolation resistance | $R_{\text{IN_OUT}}$ | At 500 Vdc | 10 | | | M Ω |
| MTBF | | MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer | | 5.61 | | MHrs |
| | | Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled | | 1.73 | | MHrs |
| Agency approvals / standards | | cTÜVus "EN 60950-1 " cURus "UL 60950-1 " CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | | |

^[1] Product is not intended for reflow solder attach.

BCM Module Block Diagram



Sine Amplitude Converter™ Point of Load Conversion

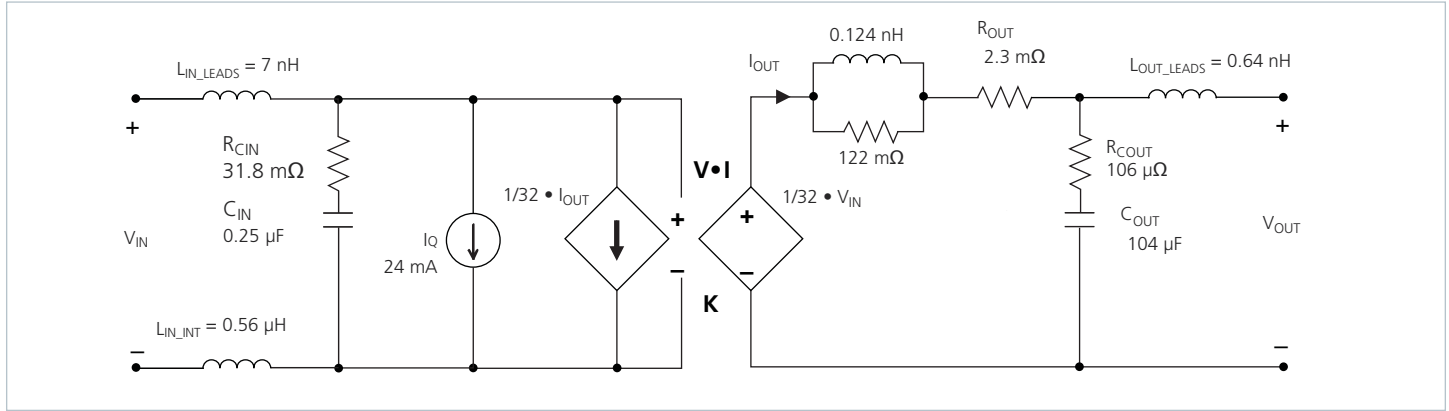


Figure 16 — BCM module AC model

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the BCM module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM384y120x800AC0 SAC can be simplified into the preceding model.

At no load:

$$V_{OUT} = V_{IN} \cdot K \quad (1)$$

K represents the “turns ratio” of the SAC.

Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT} \quad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \quad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the $R_{DS(on)}$ of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0 \Omega$ and $I_Q = 0 A$, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{IN} .

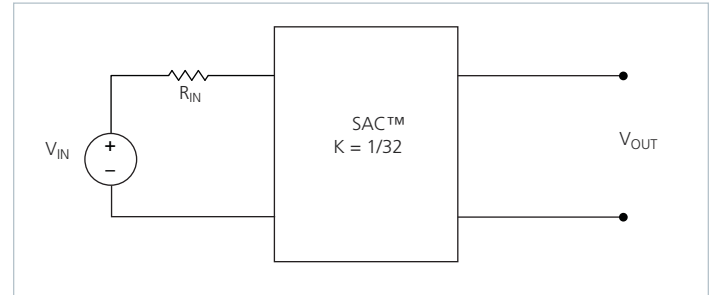


Figure 17 — $K = 1/32$ Sine Amplitude Converter with series input resistor

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \cdot R_{IN}) \cdot K \quad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{IN} \cdot K^2 \quad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that $R = 1 \Omega$, the effective R as seen from the secondary side is $1 \text{ m}\Omega$, with $K = 1/32$.

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 18.

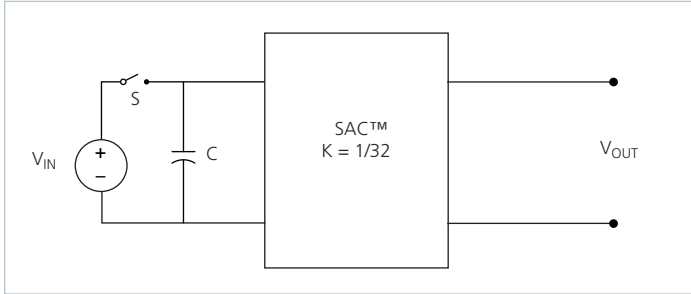


Figure 18 — Sine Amplitude Converter with input capacitor

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{IN} , the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \cdot K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \cdot \frac{dV_{OUT}}{dt} \quad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a $K = 1/32$ as shown in Figure 18, $C = 1 \mu\text{F}$ would appear as $C = 1024 \mu\text{F}$ when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the BCM® module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \cdot I_{IN} - P_{NL} - (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}} \right)$$

Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:
To take full advantage of the BCM module's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 1 μ F in series with 0.3 Ω . A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.
- Further reduce input and/or output voltage ripple without sacrificing dynamic response:
Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.
- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:
The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the output of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500 kHz the module appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. (13).

$$C_{OUT} = \frac{C_{IN}}{K^2} \quad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 19 shows the "thermal circuit" for a VI Chip® BCM module 2361 in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP} , T_{CASE_BOTTOM} , and T_{LEADS} . This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

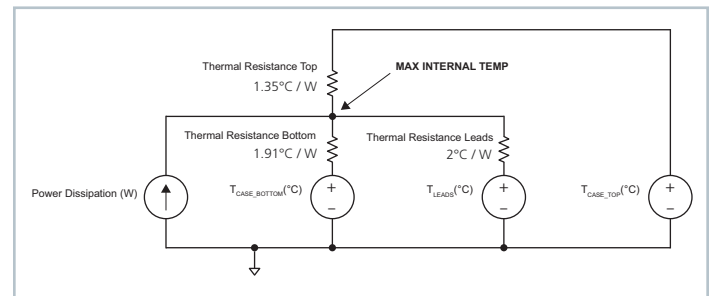


Figure 19 — Double side cooling and leads thermal model

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \cdot 1.24 = T_{CASE_TOP}$$

$$T_{INT} - PD_2 \cdot 1.24 = T_{CASE_BOTTOM}$$

$$T_{INT} - PD_3 \cdot 7 = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where T_{INT} represents the internal temperature and PD_1 , PD_2 , and PD_3 represent the heat flow through the top side, bottom side, and leads respectively.

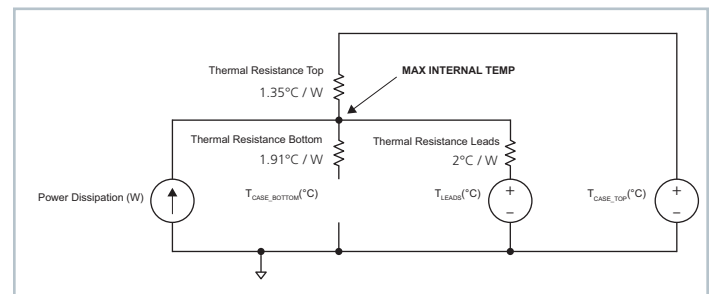


Figure 20 — One side cooling and leads thermal model

Figure 20 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \cdot 1.24 = T_{CASE_TOP}$$

$$T_{INT} - PD_3 \cdot 7 = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

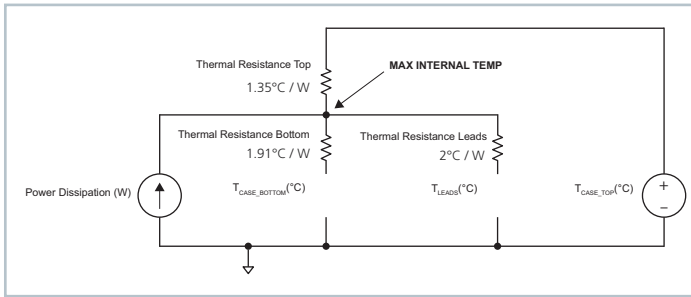


Figure 21 — One side cooling thermal model

Figure 21 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \cdot 1.24 = T_{CASE_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at:

<http://www.vicorpower.com/powerbench>.

Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of BCMs in order to prevent circulating currents.

For further details see [AN:016 Using BCM Bus Converters in High Power Arrays](#).

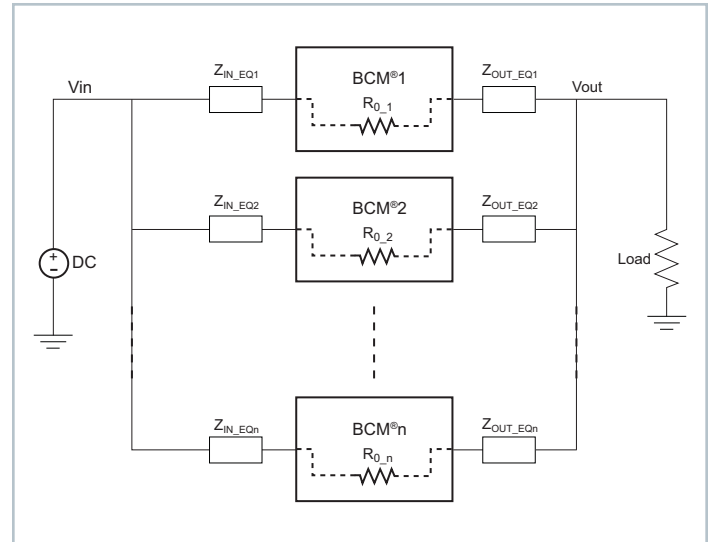


Figure 22 — BCM module array

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
(usually greater than maximum current of BCM module)
- Maximum voltage rating
(usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤ 5 A Bussmann PC-Tron

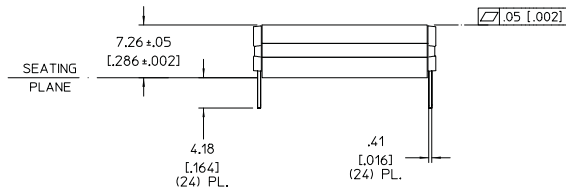
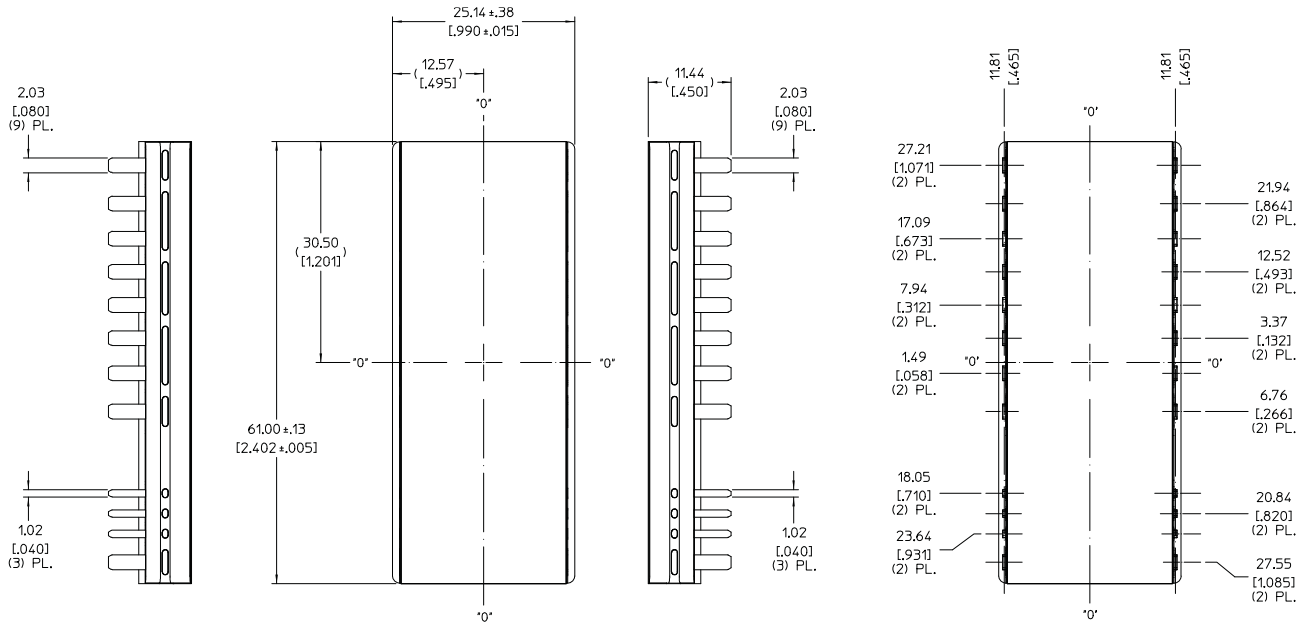
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{IN} \cdot K$. The module will continue operation in this fashion for as long as no faults occur.

The BCM384y120x800AC0 has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

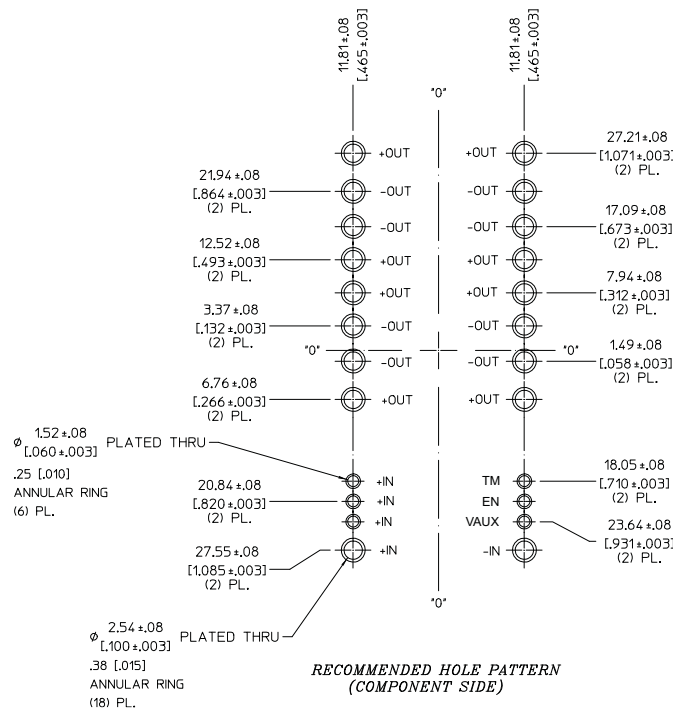
Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10 ms, 10% duty cycle is permitted and has been qualified to cover these cases.

BCM Module Through Hole Package Mechanical Drawing and Recommended Land Pattern



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.



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