AC Front End
FE175D480x033FP-00

Complete AC-DC PCB-Mounted Solution

Features & Benefits

- Complete AC-DC PCB-mounted solution
- Active Power Factor Correction (PFC)
- Rectification
- Filtering
- Transient protection
- Low-profile package, 9.55mm height above board
- Power density: 121W/in^3, 330W in 7.2in^2 footprint
- Consistent high efficiency over world-wide AC mains (85 – 264V_{AC})
- Secondary-side energy storage
- SELV 48V Output
  - Efficient power distribution to PoL converters
- 3,000V_{AC} / 4,242V_{DC} isolation
- PFC (THD) exceeds EN61000-3-2 requirements
- Conducted emissions EN55022, Class B (with a few external components)
- Surge immunity EN61000-4-5
- ZVS high-frequency (MHz) switching
- Low-profile, high-density filtering
- 100°C baseplate operation

Typical Applications

- LED – Lighting, display, signage
- Telecom (WiMAX, Power Amplifiers, Optical Switches)
- Automatic Test Equipment (ATE)
- High-Efficiency Server Power
- Office Equipment (Printers, Copiers, Projectors)
- Industrial Equipment (Process Controllers, Material Handling, Factory Automation)

Product Ratings	
V_{IN} = 85 – 264V_{AC}	P_{OUT} = 330W
V_{OUT} = 48V_{DC} (Isolated)	

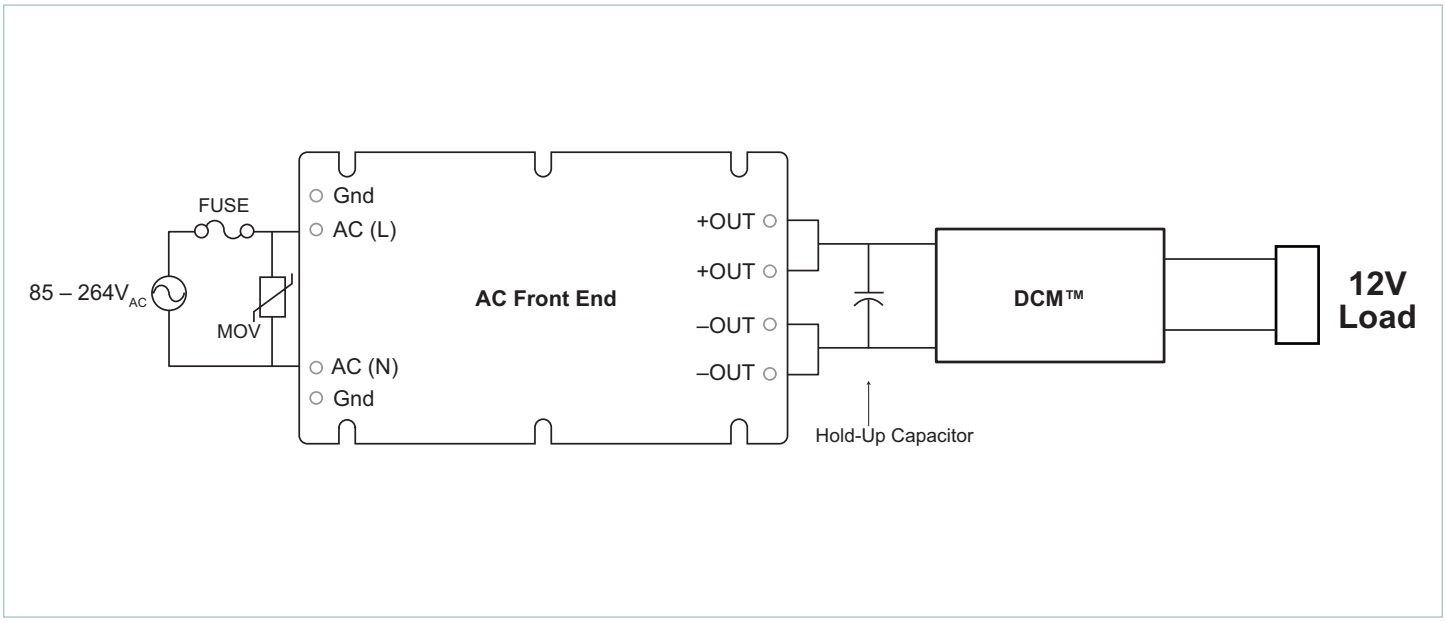
Product Description

The AC Front End is an AC-to-DC converter, operating from a universal AC input to generate an isolated and regulated 48V_{DC} output with power factor correction. The module incorporates rectification, transient and surge suppression and AC to DC conversion to provide a complete AC to DC solution in a thin-profile package. With its ZVS high-frequency Adaptive Cell™ topology, the AC Front End module consistently delivers high efficiency across worldwide AC mains. Downstream DC-DC converters support secondary-side energy storage and efficient power distribution, providing superior power system performance and connectivity from the wall plug to the point-of-load.

Part Ordering Information

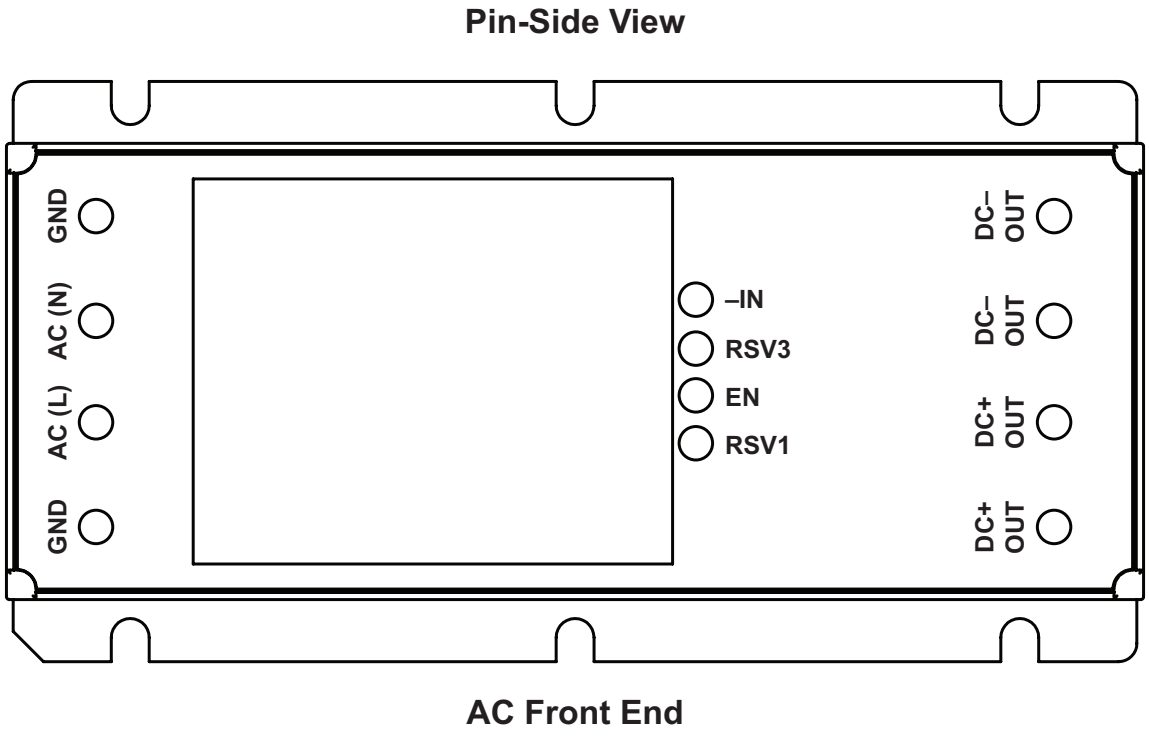
Part Number	Temperature Grade	Revision
FE175D480**C**033FP-00	**C** = –20 to 100°C	00
FE175D480**T**033FP-00	**T** = –40 to 100°C	

Typical Application



Vicor recommends the following PRM™ modules: PRM48JF480T500A00, PRM48JH480T250A00, PR036A480x012xP, PR045A480X040xP

Pin Configuration



Pin Descriptions

Signal Name	Type	Description
GND	PE Ground	Protective Earth Ground; two pins plus six grounded standoffs between PCB and baseplate
AC (N)	AC Power Input	AC Neutral Input
AC (L)	AC Power Input	AC Line Input
EN	Signal Input	Open drain with internal pullup. Leave open to enable, pull to –IN to disable
–IN	Signal Reference	EN pin reference pin
RSV3	No Connect	Do not connect to this pin
RSV1	No Connect	Do not connect to this pin
DC +OUT	Power Output	+48V Output
DC –OUT	Power Return	+48V Return Pin

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Positive pin current represents current flowing out of the pin

Parameter	Comments	Min	Max	Unit
Input voltage AC (L) to AC (N)	Continuous		275	V_{AC}
Input voltage AC (L) to AC (N)	1ms	0	600	V_{PK}
RSV1 to –IN	Do not connect to this pin	–0.3	5.3	V_{DC}
EN to –IN	5V tolerant 3.3V logic	–0.3	5.3	V_{DC}
RSV3 to –IN	Do not connect to this pin	–0.3	5.3	V_{DC}
Output voltage (+OUT to –OUT)		–0.3	57.0	V_{DC}
Output Current		0.0	10.2	A
Operating Temperature	C-Grade; baseplate	–20	100	°C
	T-Grade; baseplate	–40	100	
	M-Grade; baseplate	–55	100	
Storage Temperature	C-Grade	–40	125	°C
	T-Grade	–40	125	
	M-Grade	–65	125	
Dielectric Withstand	Input – Output	3000		V_{RMS}
	Input – Base	1500		
	Output – Base	1500		

Electrical Specifications

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_C = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade. C_{OUT} is 6800µF ±20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input Voltage Range	V_{IN}	Continuous operation	**85**		**264**	V_{RMS}
Input Voltage Cell Reconfiguration Low-to-High Threshold	V_{IN-CR+}			145	**148**	V_{RMS}
Input Voltage Cell Reconfiguration High-to-Low Threshold	$V_{IN-CR–}$		**132**	135		V_{RMS}
Input Current (Peak)	I_{INRP}				12	A
Source Line Frequency Range	F_{LINE}		47		63	Hz
Power Factor	PF	Input power >100W		0.9		–
Input Inductance (External)	L_{IN}	Differential-mode inductance; common-mode inductance may be higher; see “Source Inductance Considerations” on page 19			1	mH
No-Load Specification						
Input Power – No Load, Maximum	P_{NL}	EN floating, see Figure 3		1.1	1.5	W
Input Power – Disabled, Maximum	P_Q	EN pulled low, see Figure 4			1.6	W

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_{CASE} = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade. C_{OUT} is 6800µF ±20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specification						
Output Voltage Set Point	V_{OUT}	V_{IN} = 230V_{RMS}, 10% load	47.5	49	50.5	V
Output Voltage, No Load	V_{OUT-NL}	Over all operating stead-state line conditions	**46**	51.5	**55**	V
Output Voltage Range (Transient)	V_{OUT}	Non-faulting abnormal line and load transient conditions	**30**		**55**	V
Output Power	P_{OUT}	See Figure 1, safe operating area			**330**	W
Efficiency	η	V_{IN} = 230V, full load	91		94	%
		85V < V_{IN} < 264V, full load, see Figure 2	**88.5**			
		85V < V_{IN} < 264V, 75% load	89			
Output Voltage Ripple, Switching Frequency	$V_{OUT-PP-HF}$	Over all opearting steady-state line and load conditions, 20MHz BW, measured at C_3, Figure 28		100	**300**	mV
Output Voltage Ripple, Line Frequency	$V_{OUT-PP-LF}$	Over all opearting steady-state line and load conditions, 20MHz BW		3.8	5	V
Output Capacitance (External)	$C_{OUT-EXT}$		**6000**		**12,000**	µF
Output Turn-On Delay	t_{ON}	From V_{IN} applied, EN floating		400	**1000**	ms
		From EN pin release, V_{IN} applied				
Start-Up Set-Point Acquisition Time	t_{SS}	Full load		400	500	ms
Cell Reconfiguration Response Time	t_{CR}	Full load		5.5	11	ms
Voltage Deviation (Load Transient)	$\%V_{OUT-TRANS}$	C_{OUT} = max			8	%
Recovery Time	t_{TRANS}			250	500	ms
Line Regulation	$\%V_{OUT-LINE}$	Full load		0.5	1	%
Load Regulation	$\%V_{OUT-LOAD}$	10 – 100% load		0.5	1	%
Output Current (Continuous)	I_{OUT}	See Figure 1, SOA			**6.9**	A
Output Current (Transient)	I_{OUT-PK}	20ms duration, max			**10.2**	A
Output Switching Cycle Charge	Q_{TOT}				**13.5**	µC
Output Inductance (Parasitic)	$L_{OUT-PAR}$	Frequency at 1MHz		1		nH
Output Capacitance (Internal)	$C_{OUT-INT}$	Effective value at nominal output voltage		7		µF
Output Cpacitance (Internal ESR)	R_{COUT}			0.5		mΩ

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_{CASE} = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade. C_{OUT} is 6800µF ±20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Turn-On	$V_{IN-UVLO+}$	See timing diagram		74	**83**	V_{RMS}
Intput Undervoltage Turn-Off	$V_{IN-UVLO-}$		**65**	71		V_{RMS}
Input Overvoltage Turn-On	$V_{IN-OVLO+}$	See timing diagram	**265**	270		V_{RMS}
Input Overvoltage Turn-Off	$V_{IN-OVLO-}$			273	**283**	V_{RMS}
Output Overvoltage Threshold	$V_{OUT-OVLO+}$	Instantaneous, latched shut down	**55.3**	56.6	**59.0**	V
Upper Start/Restart Temperature Threshold (Case)	$T_{CASE-OTP-}$		**100**			°C
Overtemperature Shut-Down Threshold (Junction)	T_{J-OTP+}		**130**			°C
Overtemperature Shut-Down Threshold (Case)	$T_{CASE-OTP+}$			**110**		°C
Undertemperature Shut-Down Threshold (Case)	$T_{CASE-UTP-}$	C-Grade			**–25**	°C
Lower Start/Restart Temperature Threshold (Case)	$T_{CASE-UTP+}$	C-Grade			**–20**	°C
Overcurrent Blanking Time	t_{OC}	Based on line frequency	**400**	460	**550**	ms
Input Overvoltage Response Time	t_{POVP}				**6**	µs
Input Undervoltage Response Time	t_{UVLO}	Based on line frequency	**27**	39	**51**	ms
Output Overvoltage Response Time	t_{SOVP}	Powertrain on	**60**	120	**180**	µs
Short-Circuit Response Time	t_{SC}	Powertrain on, operational state		60	**120**	µs
Fault Retry Delay Time	t_{OFF}	See timing diagram		10		s
Output Power Limit	P_{PROT}		**330**			W

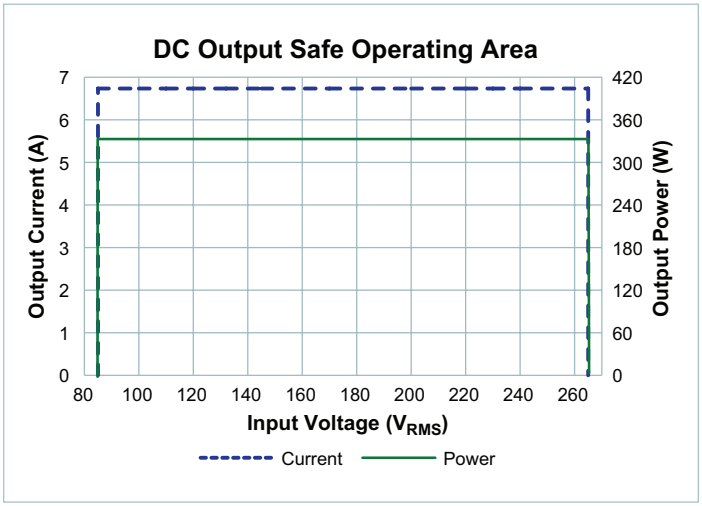


Figure 1 — *DC output safe opearating area*

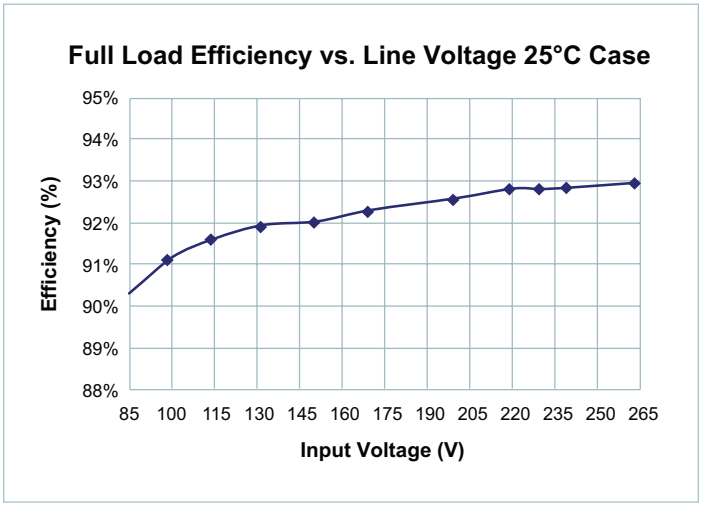


Figure 2 — *Full-load efficiency vs. line voltage*

Signal Characteristics

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_{CASE} = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade.

Enable: EN

- The EN pin enables and disables the AC Front End; when held below 0.8V the unit will be disabled.
- The EN pin can reset the AC Front End after a latching OVP event.
- The EN pin voltage is 3.3V during normal operation.
- The EN pin is referenced to the –IN pin of the module.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Start Up	En Enable Threshold	V_{EN_EN}				**2.00**	V
	Standby	En Disable Time	t_{EN_DIS}	From any point in line cycle		9	**16**	ms
		En Disable Threshold	V_{EN_DIS}		**0.80**			V
		En Resistance To Disable	R_{EN_EXT}	Max allowable resistance to –IN required to disable the moducle			**14**	kΩ

Reserved: RSV1, RSV3

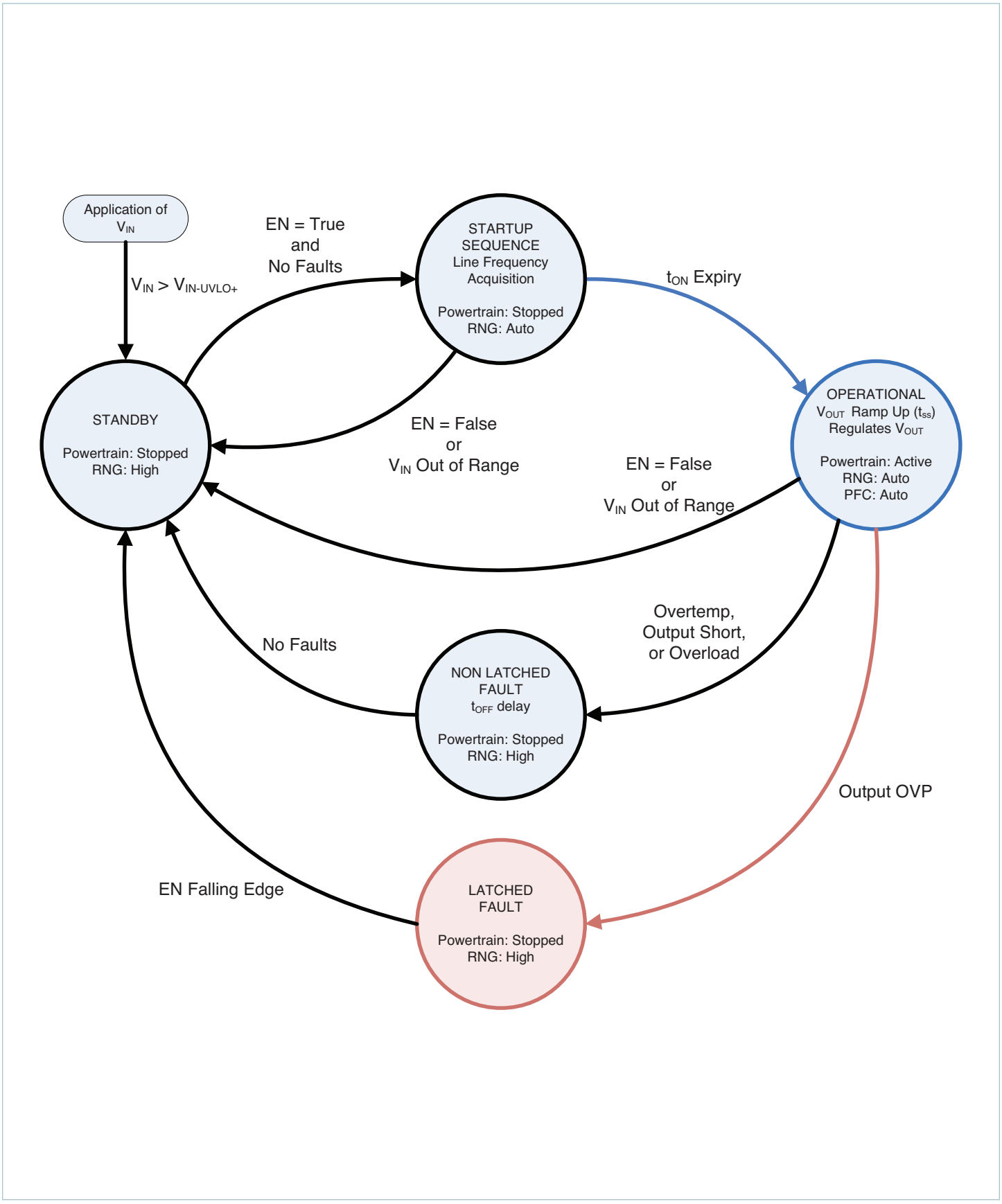
- No connections are required to these pins. In noisy environments, it is beneficial to add a 0.1µF capacitor between each reserved pin and –IN.

–IN

- **Warning:** –IN and N are not at the same potential and must not be connected together.
- The –IN pin is the signal reference ground for the EN pin.
- The –IN pin also serves as an access point for the common mode bypass filter to comply with EN55022 Class B for Conducted Emissions.

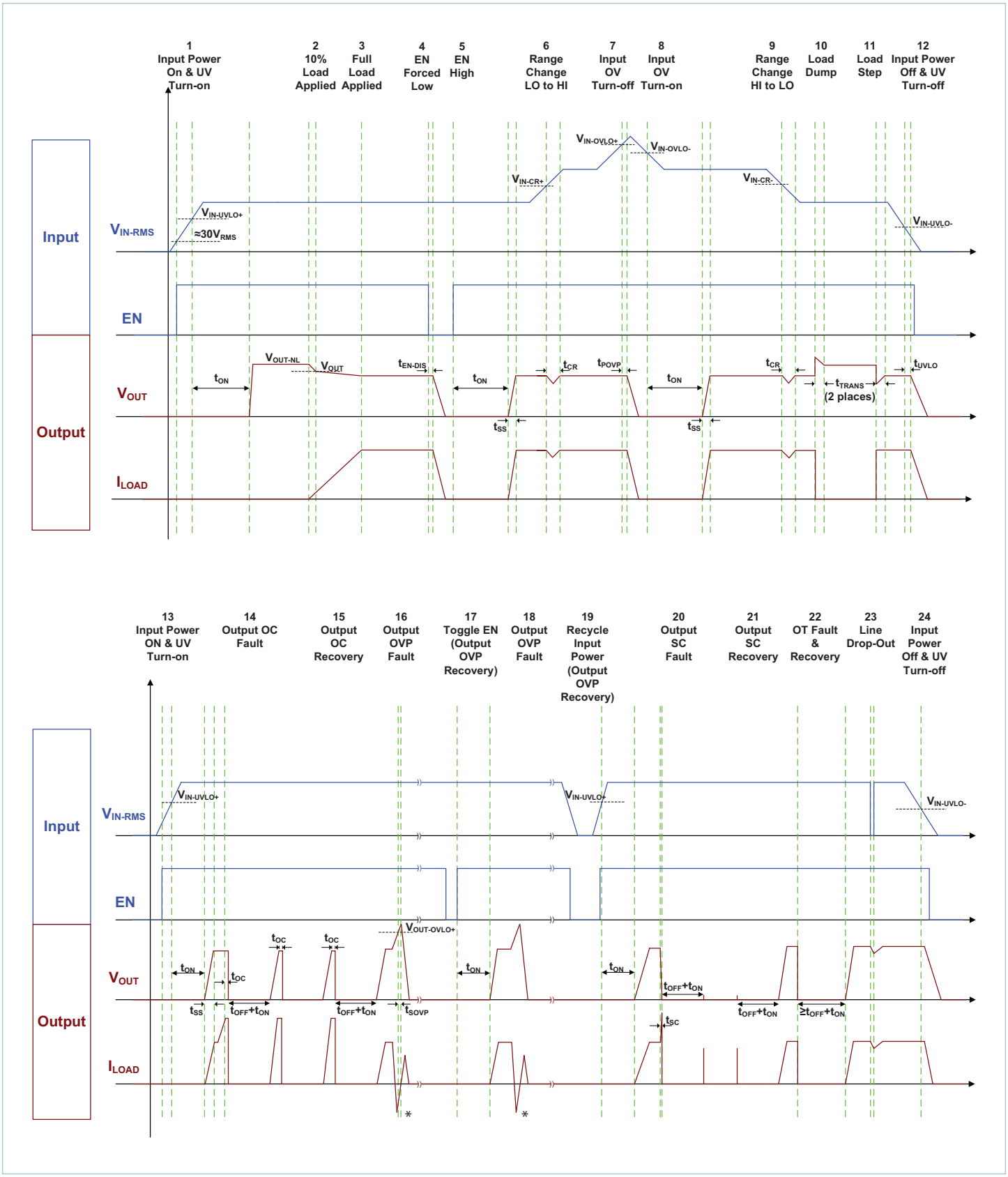
High-Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities are listed inside the state bubbles.



Functional Block Diagram

Module inputs are shown in blue; module outputs are shown in brown.
Note: Negative current is externally forced and shown for the purpose of OVP protection scenario.



Application Characteristics

The following figures present typical performance at T_{CASE} = 25ºC, unless otherwise noted. See associated figures for general trend data.

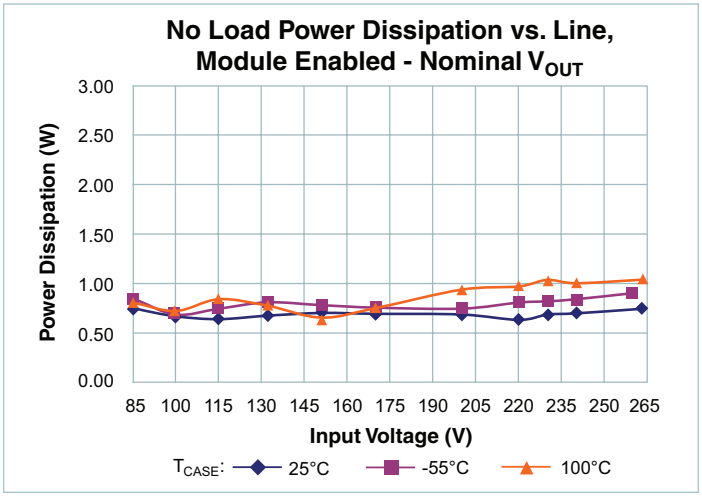


Figure 3 — *Typical no-load power dissipation vs. V_{IN}, module enabled*

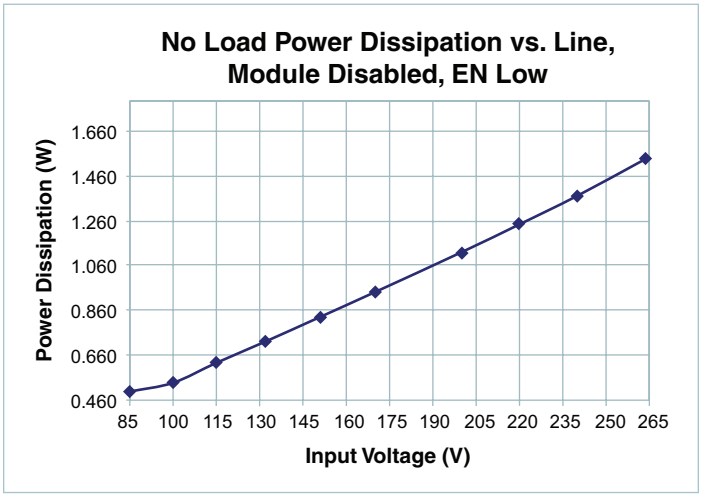


Figure 4 — *No-load power dissipation trend vs. V_{IN}, module disabled*

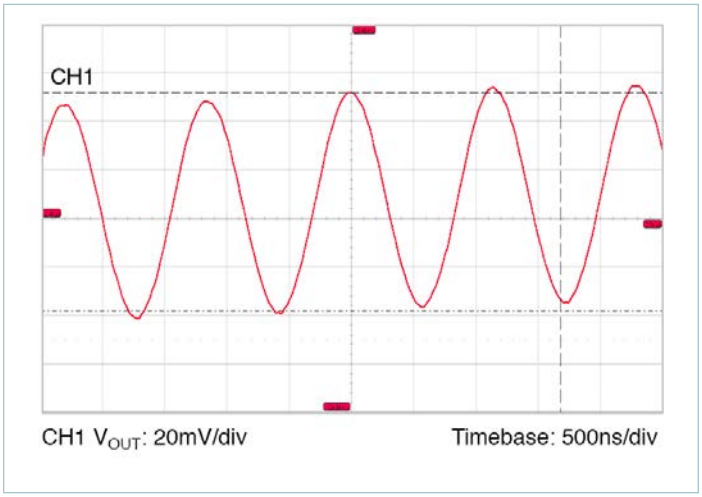


Figure 5 — *Typical switching frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 6.9A, no external ceramic capacitance*

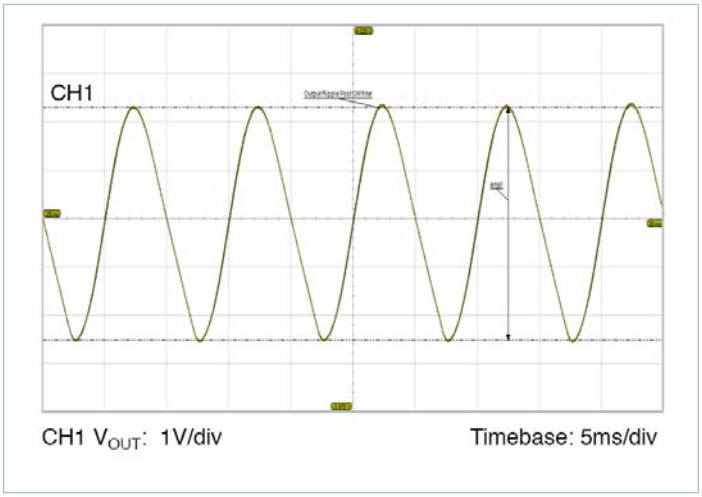


Figure 6 — *Typical line frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 6.9A, C_{OUT} = 6,800µF. Measured at C3, Figure 25*

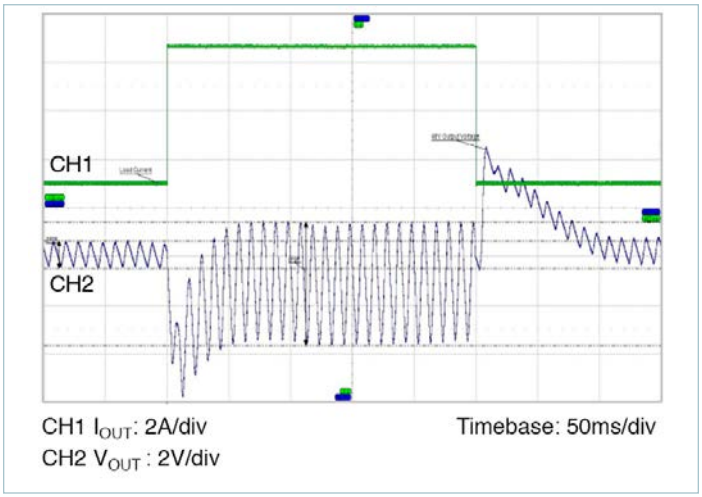


Figure 7 — *Typical output voltage transient response, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 6.9A, C_{OUT} = 6,800µF*

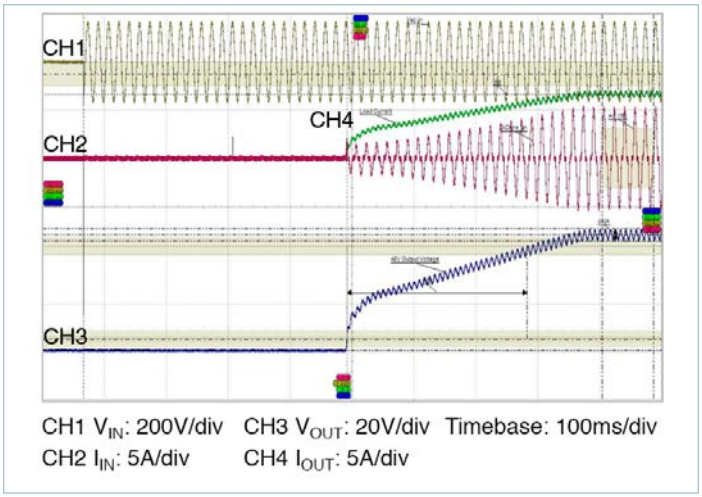


Figure 8 — *Typical start-up waveform, application of V_{IN}, R_{LOAD} = 7.1Ω, C_{OUT} = 6,800µF*

Application Characteristics (Cont.)

The following figures present typical performance at T_{CASE} = 25ºC, unless otherwise noted. See associated figures for general trend data.

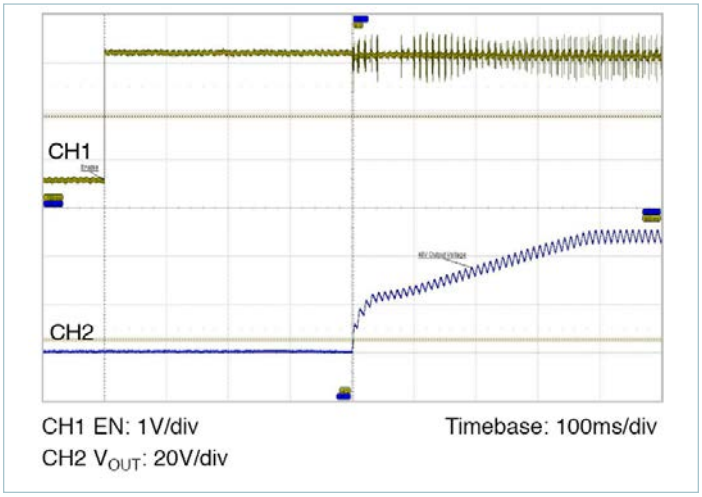


Figure 9 *— Typical start-up waveform, EN pin release, V_{IN} = 230V, R_{LOAD} = 7.1Ω, C_{OUT} = 6,800µF*

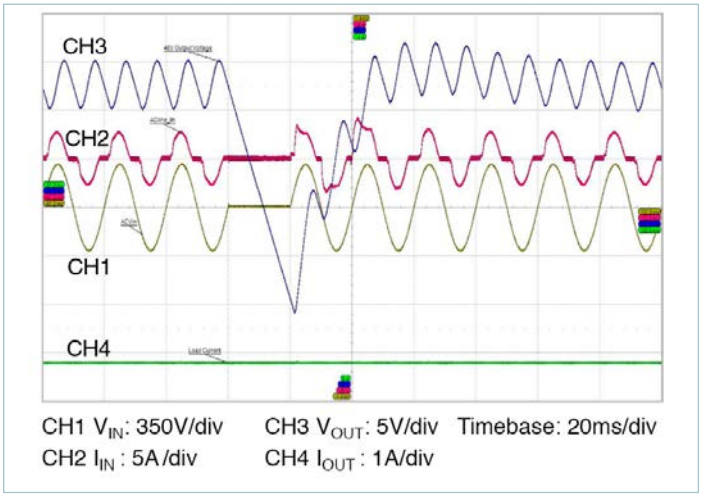


Figure 10 *— Line drop out, 50Hz, 0° phase, P_{LOAD} = 330W, C_{OUT} = 6,800µF*

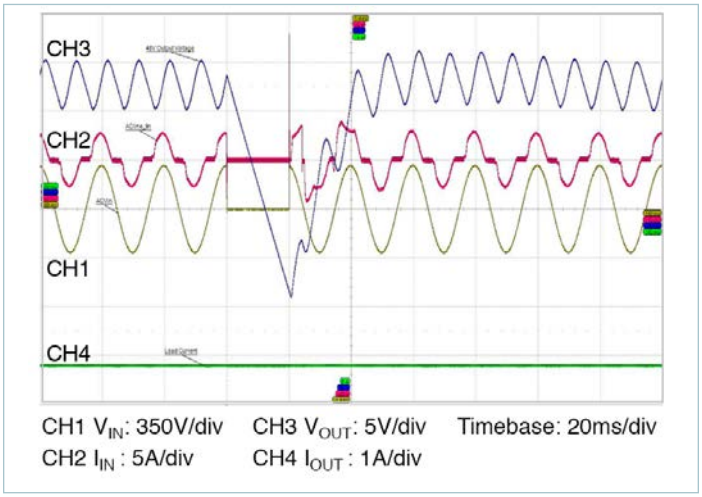


Figure 11 *— Line drop out, 50Hz, 90° phase, V_{IN} = 230V, P_{LOAD} = 330W, C_{OUT} = 6,800µF*

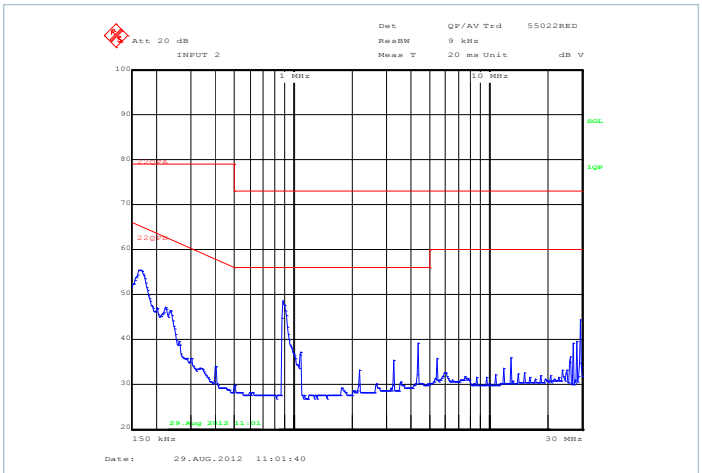


Figure 12 *— Typical EMI spectrum, quasi-peak scan, 90% load, 230V_{IN}, C_{OUT} = 6,800µF; test circuit – Figure 25*

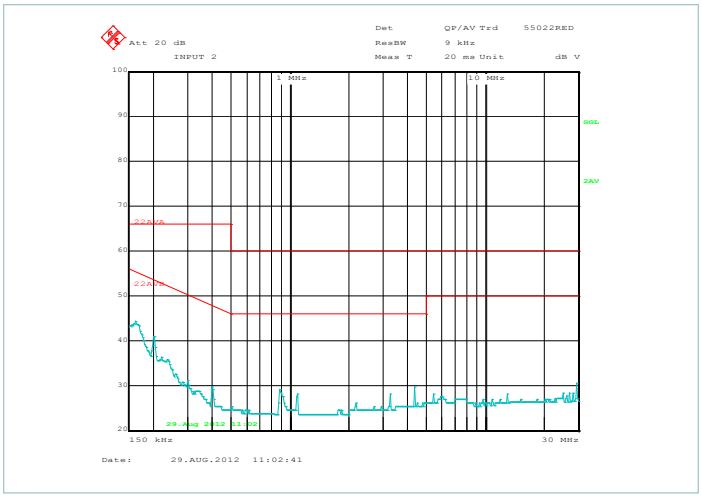


Figure 13 *— Typical EMI spectrum, average scan, 90% load, 230V_{IN}, C_{OUT} = 6,800µF; test circuit – Figure 28*

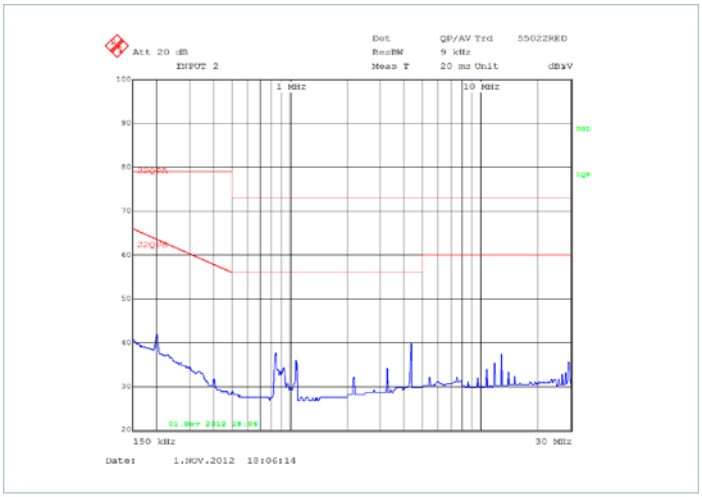


Figure 14 *— Typical EMI spectrum, quasi-peak scan, 90% load, 115V_{IN}, C_{OUT} = 6,800µF; test circuit – Figure 25*

Application Characteristics (Cont.)

The following figures present typical performance at T_{CASE} = 25°C, unless otherwise noted. See associated figures for general trend data.

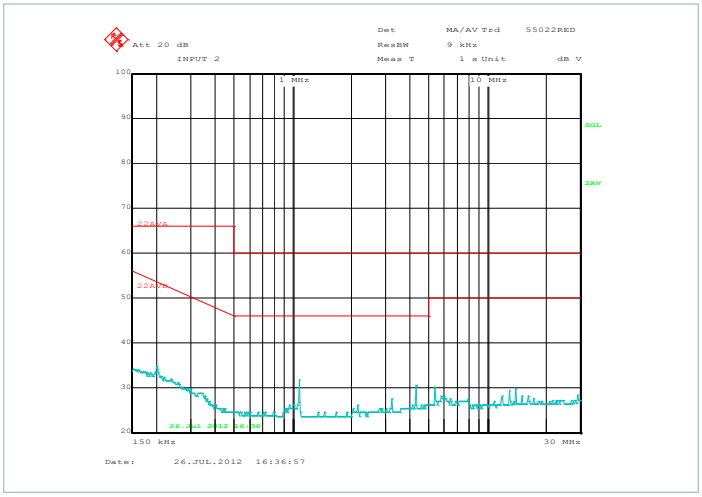


Figure 15 *— Typical EMI spectrum, average scan, 90% load, 115V_{IN}, C_{OUT} = 6,800µF; test circuit – Figure 25*

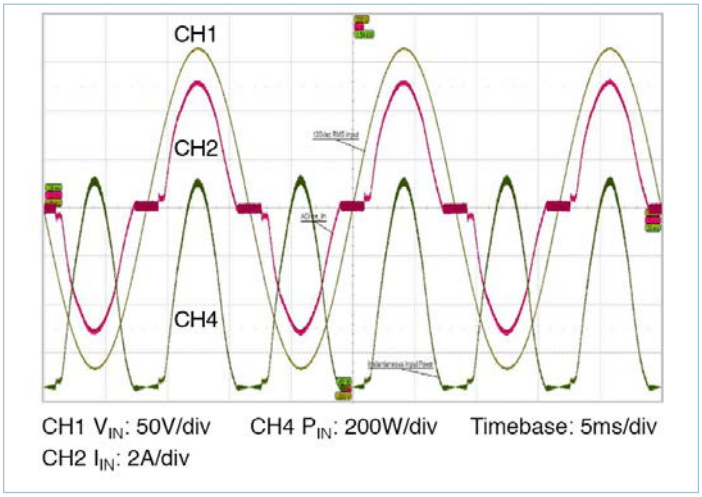


Figure 16 *— Typical line current waveform, 60Hz, V_{IN} = 120V, P_{LOAD} = 330W; C_{OUT} = 6,800µF*

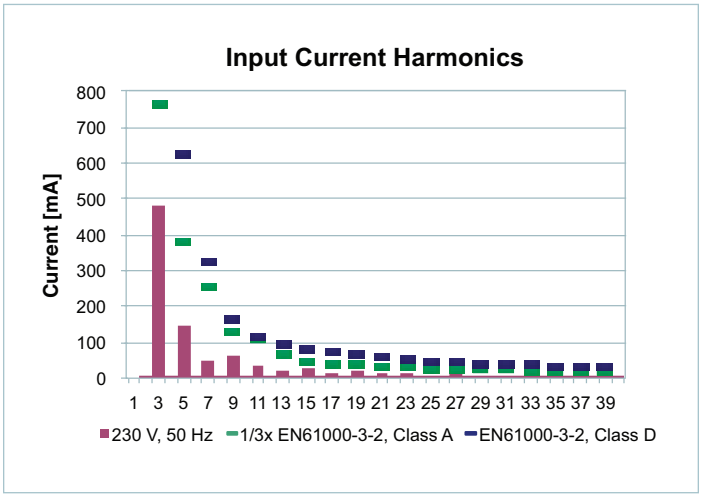


Figure 17 *— Typical input current harmonics, full load vs. V_{IN}*

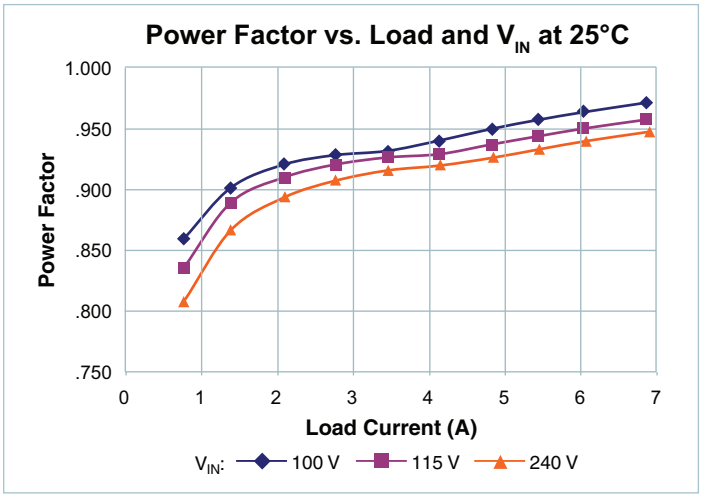


Figure 18 *— Typical power factor vs. V_{IN} and I_{OUT}*

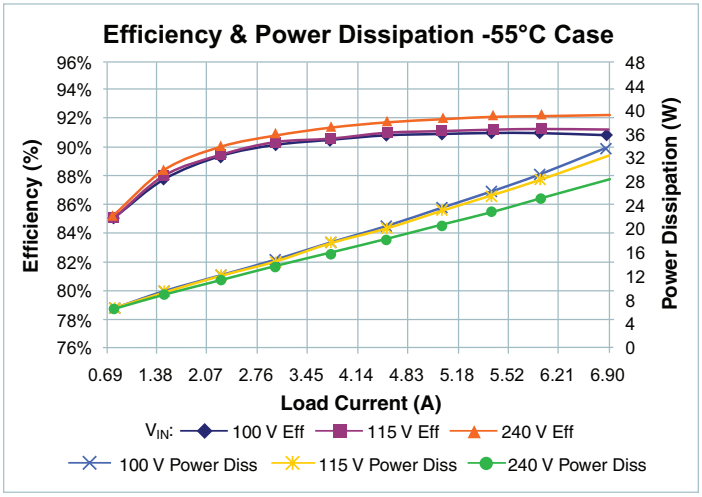


Figure 19 *— V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = –55°C*

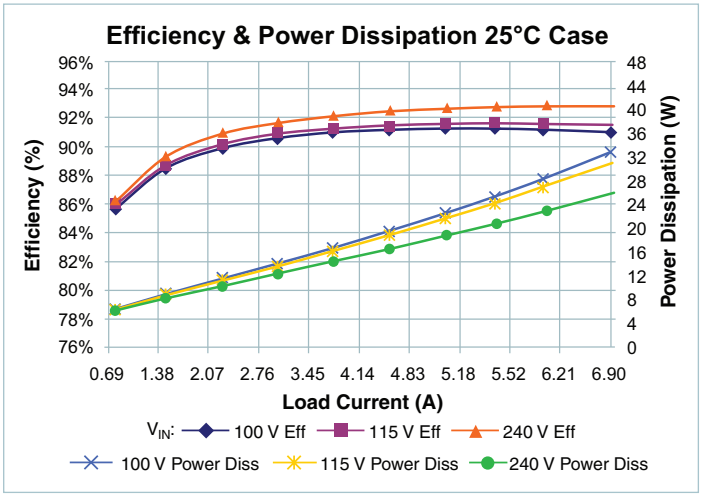


Figure 20 *— V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 25°C*

Application Characteristics (Cont.)

The following figures present typical performance at T_{CASE} = 25ºC, unless otherwise noted. See associated figures for general trend data.

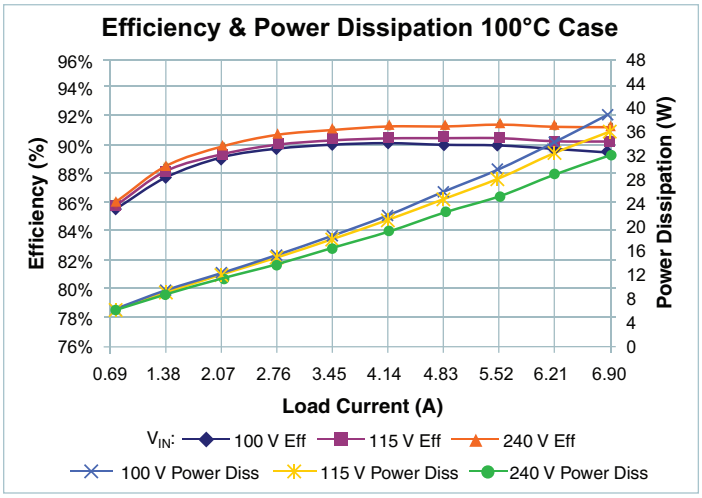


Figure 21 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 100ºC*

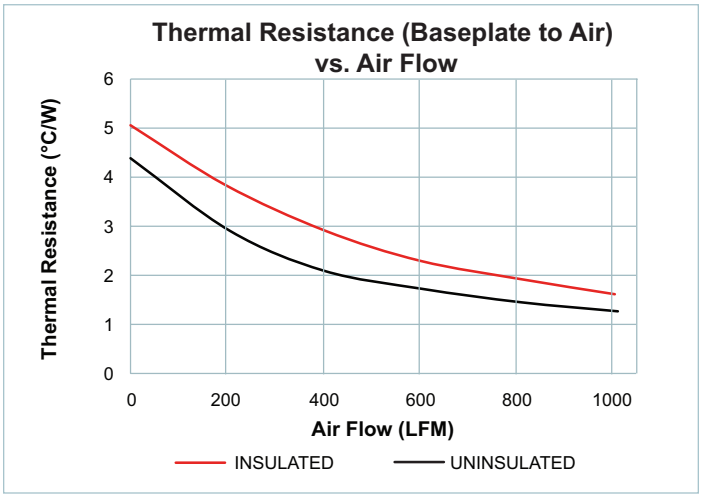


Figure 22 — *Baseplate-to-air thermal resistance; Insulated: minimal thermal dissipation through pins to PCB; Uninsulated: thermal dissipation to typical PCB*

General Characteristics

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_C = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified product grade.

Attribute	Symbol	Conditions / Notes		Min	Typ	Max	Unit
Mechanical							
Length	L				95.3 [3.75]		mm [in]
Width	W				48.6 [1.91]		mm [in]
Height	H				9.55 [0.38]		mm [in]
Volume	Vol				44.2 [2.69]		cm^3 [in^3]
Weight	W				111 [3.9]		g [oz]
Pin Material		C10200 copper, full hard					
Underplate		Nickel		100		150	µin
Pin Finish		Pure matte tin, whisker-resistant chemistry		200		300	µin
Thermal							
Operating Baseplate (Case) Temperature	T_C	Any operating condition	C-Grade	–20		100	°C
			T-Grade	–40		100	°C
			M-Grade	–55		100	°C
Thermal Resistance		Baseplate-to-sink, flat greased surface			0.13		°C / W
		Baseplate-to-sink, thermal pad (PN 36967)			0.17		°C / W
Thermal Capacity					84.5		Ws / °C
Assembly							
ESD Rating	ESD_{HBM}	Human Body Model, (JEDEC JESD 22-A114C.01)		1000			V
	ESD_{MM}	Machine Model, (JEDEC JESD 22-A115B)		N/A			V
	ESD_{CDM}	Charged Device Model, (JEDEC JESD 22-C101D)		200			V
Soldering							
See Application Note: Soldering Methods and Procedure for Vicor Power Modules							
Safety & Reliability							
Touch Current		Measured in accordance with IEC 60990 using measuring network Figure 28			0.56	0.68	mA
Agency Approvals / Standards		cURus UL/CSA 60950-1					
		cTÜVus EN 60950-1					
		CE, Low Voltage Directive 2006/95/EC					

General Characteristics (Cont.)

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_C = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified product grade.

Attribute	Symbol	Conditions / Notes
EMI/EMC Compliance		
FCC Part 15, EN55022, CISPR22: 2006 + A1: 2007, Conducted Emissions		Class B Limits – with components connected as shown in Figure 28
EN61000-3-2: 2009, Harmonic Current Emissions		Class A
EN61000-3-3: 2005, Voltage Changes & Flicker		P_{ST} < 1.0; P_{LT} < 0.65; dc < 3.3%; dmax < 6%
EN61000-4-4: 2004, Electrical Fast Transients		Level 2, Performance criteria A
EN61000-4-5: 2006, Surge Immunity		Level 3, Immunity Criteria B, external TMOV required
EN61000-4-6: 2009, Conducted RF Immunity		Level 2, 130dBµV ($3.0V_{RMS}$)
EN61000-4-8: 1993 + A1 2001, Power Frequency H-Field 10A/m, continuous field		Level 3, Performance Criteria A
EN61000-4-11: 2004, Voltage Dips & Interrupts		Class 2, Performance Criteria A Dips, Performance Criteria B Interrupts

Product Details and Design Guidelines

Building Blocks and System Designs

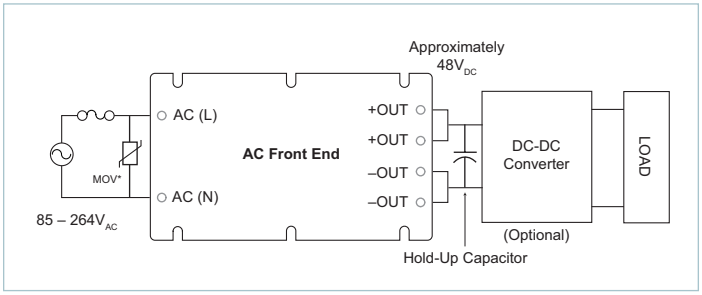


Figure 23 — *300W universal AC-to-DC supply*

The AC Front End is a high efficiency AC-to-DC converter, operating from a universal AC input to generate an isolated SELV $48V_{DC}$ output bus with power factor correction. It is the key component of an AC-to-DC power supply system such as the one shown in Figure 23 above.

The input to the AC Front End is a sinusoidal AC source with a power factor maintained by the module with harmonics conforming to IEC 61000-3-2. Internal filtering enables compliance with the standards relevant to the application (Surge, EMI, etc.). See EMI/EMC Compliance standards on page 16.

The module uses secondary-side energy storage (at the SELV 48V bus) and optional PRM™ regulators to maintain output hold up through line dropouts and brownouts. Downstream regulators also provide tighter voltage regulation, if required.

The FE175D480C033FP-00 is designed for standalone operation; however, it may be part of a system that is paralleled by downstream DC-DC converters. Contact Vicor Sales or refer to our www.vicorpower.com, regarding new models that can be paralleled directly for higher power applications.

Traditional PFC Topology

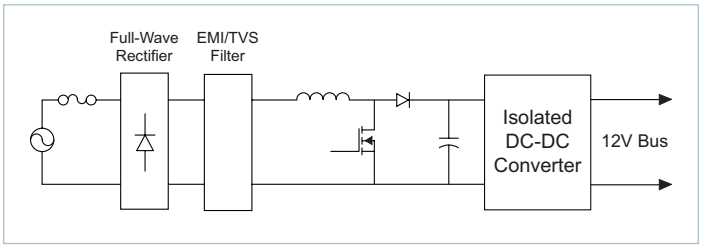


Figure 24 — *Traditional PFC AC-to-DC supply*

To cope with input voltages across worldwide AC mains ($85 – 264V_{AC}$), traditional AC-DC power supplies (Figure 24) use two power conversion stages: 1) a PFC boost stage to step up from a rectified input as low as $85V_{AC}$ to ~$380V_{DC}$; and 2) a DC-DC down converter from $380V_{DC}$ to a 12V bus. The efficiency of the boost stage and of traditional power supplies is significantly compromised operating from worldwide AC lines as low as $85V_{AC}$.

Adaptive Cell™ Topology

With its single-stage Adaptive Cell topology, the AC Front End enables consistently high-efficiency conversion from worldwide AC mains to a 48V bus and efficient secondary-side power distribution.

Power Factor Correction

The module provides power factor correction over worldwide AC mains. For most static loads, PFC approaches unity, see Figure 18. Load transients that approach the line frequency should be filtered or avoided as these may reduce PFC.

Input Fuse Selection

The AC Front End is not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Recommended fuse: 5A, 216 Series Littelfuse
- Current rating
  (usually greater than the AC Front End maximum current)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t

Fault Handling

Input Undervoltage (UV) Fault Protection

The AC Front End's input voltage is monitored by the microcontroller to detect an input undervoltage condition. When the input voltage is less than the $V_{IN\text{-}UVLO–}$, a fault is detected, the fault latch and reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the unit falls. After a time t_{UVLO}, the unit shuts down. Faults lasting less than t_{UVLO} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage rises above $V_{IN\text{-}UVLO+}$, the unit recovers from the input UV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage of the unit reaches the set-point voltage within a time t_{SS}.

Overcurrent (OC) Fault Protection

The unit's output current, determined by V_{EAO}, $V_{IN\text{-}B}$ and the primary-side-sensed output voltage is monitored by the microcontroller to detect an output OC condition. If the output current exceeds its current limit, a fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time t_{OC}. As long as the fault persists, the module goes through an auto-restart cycle with off time equal to $t_{OFF} + t_{ON}$ and on time equal to t_{OC}. Faults shorter than a time t_{OC} may not be detected. Once the fault is cleared, the module follows its normal start up sequence after a time t_{OFF}.

Short Circuit (SC) Fault Protection

The microcontroller determines a short circuit on the output of the unit by measuring its primary sensed output voltage. Most commonly, a drop in the primary-sensed output voltage triggers a short circuit event. The module responds to a short circuit event within a time t_{SC}. The module then goes through an auto restart cycle, with an off time equal to $t_{OFF} + t_{ON}$ and an on time equal to t_{SC}, for as long as the short circuit fault condition persists. Once the fault is cleared, the unit follows its normal start up sequence after a time toff. Faults shorter than a time t_{SC} may not be detected.

Temperature Fault Protection

The microcontroller monitors the temperature within the AC Front End. If this temperature exceeds $T_{J\text{-}OTP+}$, an overtemperature fault is detected, the reset logic block disables the modulator, the modulator stops the powertrain switching and the output voltage of the AC Front End falls. Once the case temperature falls below $T_{CASE\text{-}OTP-}$, after a time greater than or equal to toff, the converter recovers and undergoes a normal restart. For the C-Grade version of the converter, this temperature is 75°C. Faults shorter than a time totp may not be detected. If the temperature falls below $T_{CASE\text{-}UTP-}$, an undertemperature fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching and the output voltage of the unit falls. Once the case temperature rises above $T_{CASE\text{-}UTP}$, after a time greater than or equal to t_{OFF}, the unit recovers and undergoes a normal restart.

Output Overvoltage Protection (OVP)

The microcontroller monitors the primary sensed output voltage to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT\text{-}OVLO+}$, a fault is latched, the logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time tsovp. Faults shorter than a time t_{SOVP} may not be detected. This type of fault is a latched fault and requires that 1) the EN pin be toggled or 2) the input power be recycled to recover from the fault.

Hold-Up Capacitance

The AC Front End uses secondary-side energy storage (at the SELV 48V bus) and optional PRM™ regulators to maintain output hold up through line dropouts and brownouts. The module's output bulk capacitance can be sized to achieve the required hold up functionality.

Hold-up time depends upon the output power drawn from the AC-Front-End-based AC-to-DC front end and the input voltage range of downstream DC-to-DC converters.

The following formula can be used to calculate hold-up capacitance

$$C = 2 \bullet P_{OUT} \bullet \frac{(0.005 + t_d)}{(V_2^2 - V_1^2)} \qquad (1)$$

for a system comprised of AC Front End and a PRM regulator:

Where:

- **C** = AC Front End's output bulk capacitance in farads
- **t_d** = Hold-up time in seconds
- **P_{OUT}** = AC Front End's output power in watts
- **V_2** = Output voltage of AC Front end's converter in volts
- **V_1** = PRM regulator undervoltage turn off (volts) **or** $P_{OUT}/I_{OUT\text{-}PK}$, whichever is greater

Output Filtering

The AC Front End module requires an output bulk capacitor in the range of 6,000 – 12,000µF for proper operation of the PFC front end.

The output voltage has the following two components of voltage ripple:

1) Line frequency voltage ripple: 2 • f_{LINE} Hz component
2) Switching frequency voltage ripple: 1MHz module switching frequency component

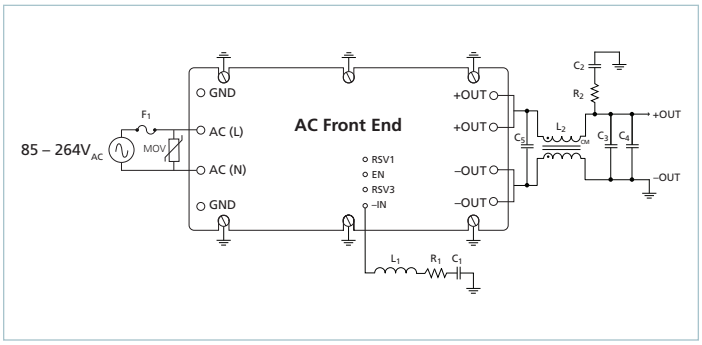


Figure 25 — *Typical application for EN55022 Class B EMI*

Where, in the schematic:

- **C_1** = 2.2nF (Murata GA355DR7GF222KW01L)
- **C_2** = 4.7nF (Murata GA355DR7GF472KW01L)
- **C_3** = 3.3µF (TDK C4532X7R1H335MT)
- **C_4** = 6800µF 63V (Panasonic UVR1J682MRD)
- **C_5** = 100µF 63V (Nichicon UVY1J101MPD)
- **F_1** = 5A, 216 Series Littlefuse
- **L_1** = 15µH (TDK MLF2012C150KT)
- **L_2** = 600µH (Vicor 37052-601)
- **MOV** = 300V, 10kA, 20mm dia (Littlefuse TMOV20RP300E)
- **R_1** = 6.8Ω
- **R_2** = 2.2Ω

Line Frequency Filtering

Output line frequency ripple depends upon output bulk capacitance. Output bulk capacitor values should be calculated based on line frequency voltage ripple. High-grade electrolytic capacitors with adequate ripple current ratings, low ESR and a minimum voltage rating of 63V are recommended.

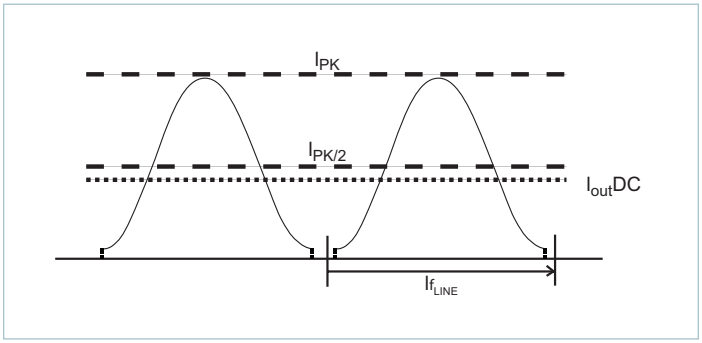


Figure 26 — *Output current waveform*

Based on the output current waveform, as seen in Figure 26, the following formula can be used to determine peak-to-peak line frequency output voltage ripple:

$$VPP_{LINE} = 0.2 \bullet \frac{P_{OUT}}{(V_{OUT} \bullet f_{LINE} \bullet C)} \quad (2)$$

Where:

VPP_{LINE} = Output voltage ripple peak-to-peak line frequency

P_{OUT} = Average output power

V_{OUT} = Output voltage set point, nominally 48V

f_{LINE} = Frequency of line voltage

C = Output bulk capacitance

I_{DC} = Maximum average output current

I_{PK} = Peak-to-peak line frequency output current ripple

In certain applications, the choice of bulk capacitance may be determined by hold-up requirements and low frequency output voltage filtering requirements. Such applications may use the greater capacitance value determined from these requirements. The ripple current rating for the bulk capacitors can be determined from the following equation:

$$I_{RIPPLE} \approx 0.8 \bullet \frac{P_{OUT}}{V_{OUT}} \quad (3)$$

Switching Frequency Filtering

Some applications require the output filtering shown in Figure 25 to meet radiated emissions limits. In such a situation, the output switching ripple shown in Figure 5 should be expected at the output of the filter. In cases where other means are used to control radiated emissions, and more ripple can be tolerated, the output filter can be simplified by removal of the common mode inductor, and C5, which is used to reduce the Q of the LC resonant tank.

Output switching frequency voltage ripple is the function of the output bypass ceramic capacitor. Output bypass ceramic capacitor values should be calculated based on switching frequency voltage ripple. Normally bypass capacitors with low ESR are used with a sufficient voltage rating.

Output bypass ceramic capacitor value for allowable peak-to-peak switching frequency voltage ripple can be determined by:

$$C_3 = \frac{Q_{TOT}}{V_{OUT\text{-}PP\text{-}HF}} - C_{OUT\text{-}INT} \quad (4)$$

Where:

$V_{OUT\text{-}PP\text{-}HF}$ = Allowable peak-to-peak output switching frequency voltage ripple in volts

Q_{TOT} = The total output charge per switching cycle at full load, maximum 13.5µC

$C_{OUT\text{-}INT}$ = The module internal effective capacitance

C_3 = Required output bypass ceramic capacitor

EMI Filtering and Transient Voltage Suppression

EMI Filtering

The AC Front End with PFC is designed such that it will comply with EN55022 Class B for Conducted Emissions with the filter connected across –IN and GND as shown in Figure 25. The emissions spectrum is shown in Figures 12 – 15. If one of the outputs is connected to earth ground, a small (single turn) output common mode choke is also required.

EMI performance is subject to a wide variety of external influences such as PCB construction, circuit layout etc. As such, external components in addition to those listed herein may be required in specific instances to gain full compliance to the standards specified.

Transient Voltage Suppression

The AC Front End contains line transient suppression circuitry to meet specifications for surge (i.e., EN61000-4-5) and fast transient conditions (i.e., EN61000-4-4 fast transient/"burst").

Thermal Design

Thermal management of internally dissipated heat should maximize heat removed from the baseplate surface, since the baseplate represents the lowest aggregate thermal impedance to internal components. The baseplate temperature should be maintained below 100°C. Cooling of the system PCB should be provided to keep the leads below 100°C, and to control maximum PCB temperatures in the area of the module.

Powering a Constant Power Load

When the output voltage of the AC Front End module is applied to the input of the PRM™ regulator, the regulator turns on and acts as a constant-power load. When the module's output voltage reaches the input undervoltage turn on of the regulator, the regulator will attempt to start. However, the current demand of the PRM regulator at the undervoltage turn-on point and the hold-up capacitor charging current may force the AC Front End into current limit. In this case, the unit may shut down and restart repeatedly. In order to prevent this multiple restart scenario, it is necessary to delay enabling a constant-power load when powered up by the upstream AC to 48V front end until after the output set point of the AC Front End is reached.

This can be achieved by

1) Keeping the downstream constant-power load off during power up sequence

and

2) Turning the downstream constant-power load on after the output voltage of the module reaches 48V steady state.

After the initial start up, the output of the AC Front End can be allowed to fall to 30V during a line dropout at full load. In this case, the circuit should not disable the PRM regulator if the input voltage falls after it is turned on; therefore, some form of hysteresis or latching is needed on the enable signal for the constant power load. The output capacitance of the AC Front End should also be sized appropriately for a constant power load to prevent collapse of the output voltage of the module during line dropout (see Hold-Up Capacitance on page 18). A constant-power load can be turned off after completion of the required hold up time during the power-down sequence or can be allowed to turn off when it reaches its own undervoltage shut-down point.

The timing diagram in Figure 27 shows the output voltage of the AC Front End module and the PRM™ PC pin voltage and output voltage of the PRM regulator for the power up and power down sequence. It is recommended to keep the time delay approximately 10 – 20ms.

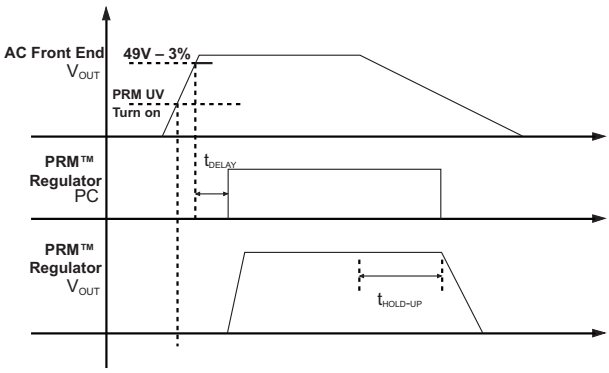


Figure 27 — *PRM enable hold-off waveforms*

Special care should be taken when enabling the constant-power load near the auto-ranger threshold, especially with an inductive source upstream of the AC Front End. A load current spike may cause a large input voltage transient, resulting in a range change which could temporarily reduce the available power (see Adaptive Cell™ Topology below).

Adaptive Cell™ Topology

The Adaptive Cell topology utilizes magnetically coupled "top" and "bottom" primary cells that are adaptively configured in series or parallel by a configuration controller comprised of an array of switches. A microcontroller monitors operating conditions and defines the configuration of the top and bottom cells through a range control signal.

A comparator inside the microcontroller monitors the line voltage and compares it to an internal voltage reference.
If the input voltage of the AC Front End crosses above the positive going cell reconfiguration threshold voltage, the output of the comparator transitions, causing switches S_1 and S_2 to open and switch S_3 to close (see Functional Block Diagram on page 8). With the top cell and bottom cell configured in series, the unit operates in "high" range and input capacitances C_{IN-T} and C_{IN-B} are in series.

If the peak of input voltage of the unit falls below the negative-going range threshold voltage for two line cycles, the cell configuration controller opens switch S_3 and closes switches S_1 and S_2. With the top cell and bottom cells configured in parallel, the unit operates in "low" range and input capacitances C_{IN-T} and C_{IN-B} are in parallel.

Power processing is held off while transitioning between ranges and the output voltage of the unit may temporarily droop. External output hold up capacitance should be sized to support power delivery to the load during cell reconfiguration. The minimum specified external output capacitance of 6,000µF is sufficient to provide adequate ride-through during cell reconfiguration for typical applications.

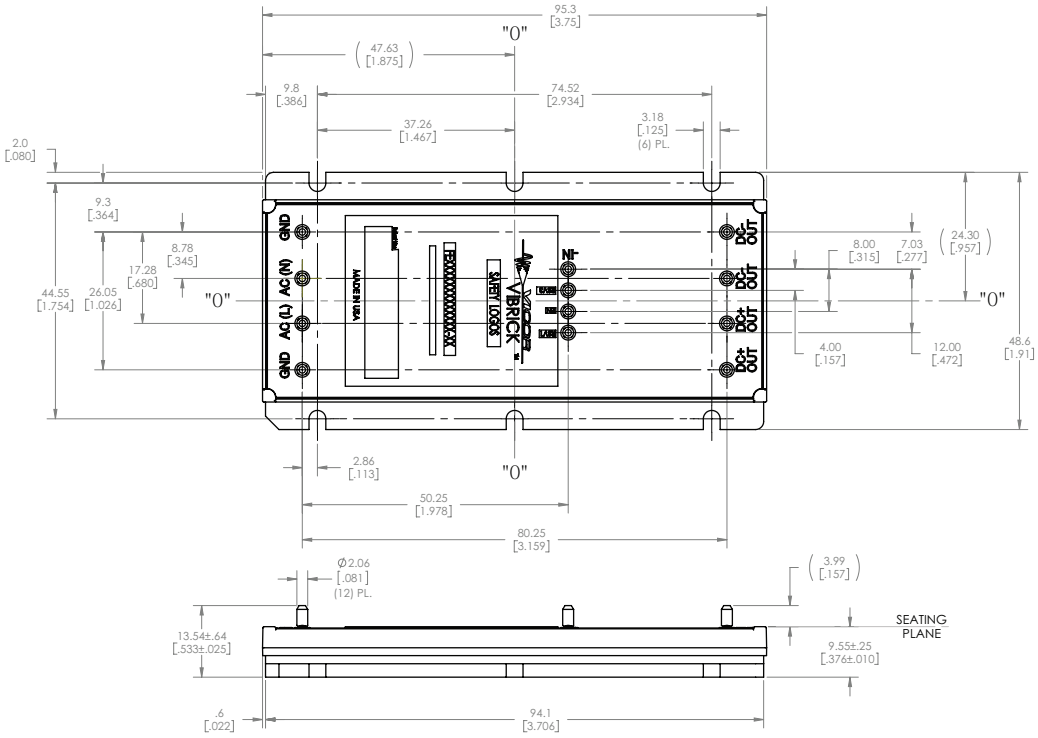
Source Inductance Considerations

The AC Front End powertrain uses a unique Adaptive Cell Topology that dynamically matches the powertrain architecture to the AC line voltage. In addition the AC Front End uses a unique control algorithm to reduce the AC line harmonics yet still achieve rapid response to dynamic load conditions presented to it at the DC output terminals. Given these unique power processing features, the AC Front End can expose deficiencies in the AC line source impedance that may result in unstable operation if ignored.

It is recommended that for a single AC Front End, the line source inductance should be no greater than 1mH for a universal AC input of 100 – 240V. If the AC Front End will be operated at 240V nominal only, the source impedance may be increased to 2mH. For either of the preceding operating conditions it is best to be conservative and stay below the maximum source inductance values. When multiple AC Front End's are used on a single AC line, the inductance should be no greater than 1mH/N, where N is the number of AC Front End's on the AC branch circuit, or 2mH/N for $240V_{AC}$ operation. It is important to consider all potential sources of series inductance including and not limited to, AC power distribution transformers, structure wiring inductance, AC line reactors, and additional line filters. Non-linear behavior of power distribution devices ahead of the AC Front End may further reduce the maximum inductance and require testing to ensure optimal performance.

If the AC Front End is to be utilized in large arrays, the AC Front Ends should be spread across multiple phases or sources thereby minimizing the source inductance requirements, or be operated at a line voltage close to $240V_{AC}$. Vicor Applications should be contacted to assist in the review of the application when multiple devices are to be used in arrays.

Product Outline Drawing



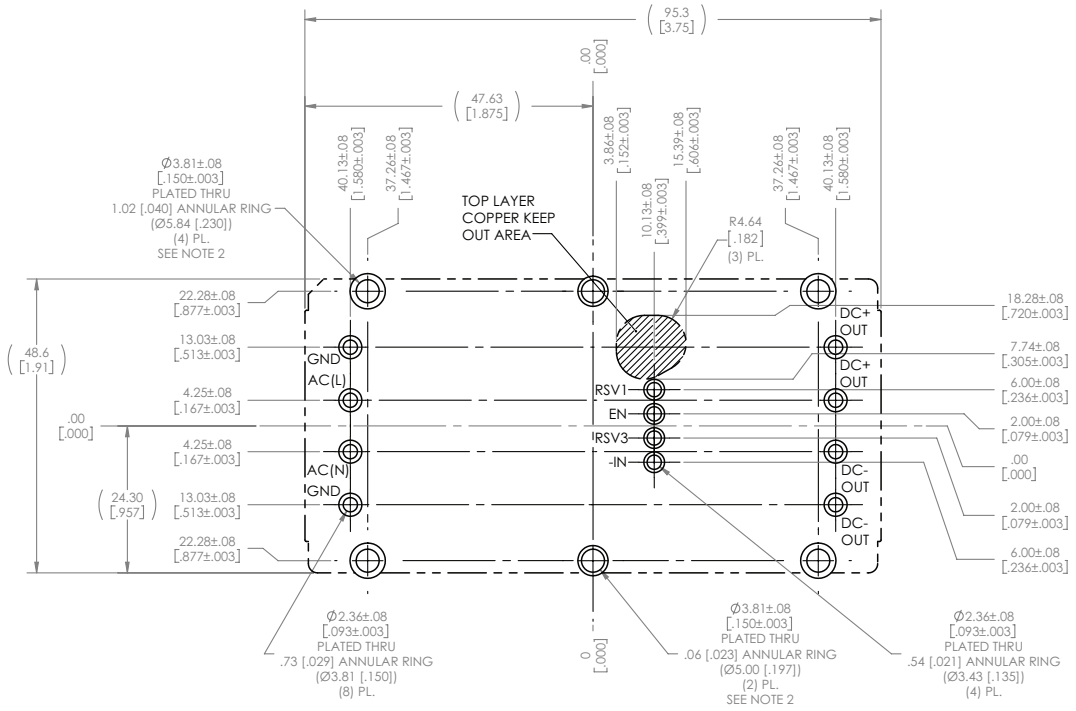
NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

2- PLATED THROUGH HOLES SHALL BE USED WITH VIBRICK STANDOFF KITS TO GROUND THE BASEPLATE TO THE CUSTOMERS PCB AND/OR COLD PLATE.

Product outline drawings are available in .pdf and .dxf formats. 3D mechanical models are available in .pdf and .step formats. See the AC Front End family page for more details.

Recommended PCB Footprint



RECOMMENDED PCB PATTERN
(COMPONENT SIDE SHOWN)

Product outline drawings are available in .pdf and .dxf formats. 3D mechanical models are available in .pdf and .step formats. See the AC Front End family page for more details.

Revision History

Revision	Date	Description	Page Number(s)
2.1	03/19/19	First release with updated formatting	n/a
2.2	04/24/20	Corrections to pin configuration image	3

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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
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