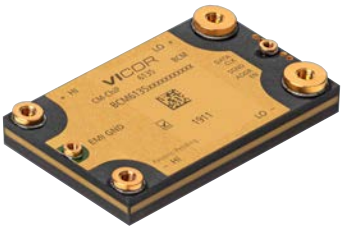


BCM® Bus Converter
BCM6135CD1E5165yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 65A continuous low-voltage-side current
- Up to 3.4kW/in^3 power density
- 97.9% peak efficiency
- 4,242V_{DC} isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short-circuit and thermal protection
- PMBus® management interface

Typical Applications

- 380V_{DC} Power Distribution
- High-End Computing Systems
- High-Density Power Supplies

Product Ratings	
V_{HI} = 384V (260 – 410V)	I_{LO} = up to 65A
V_{LO} = 48V (32.5 – 51.3V) (NO LOAD)	K = 1/8

Product Description

The CM-ChiP BCM is a high-efficiency Bus Converter, operating from a 260 – 410V_{DC} high-voltage bus to create an isolated ratiometric 32.5 – 51.3V_{DC} low-side bus. This ultra-low-profile module is available in a chassis-mount form factor, incorporates a fixed-ratio DC-DC converter and PMBus commands and controls. The BCM provides low output impedance, low noise, fast transient response, high efficiency and high power density. A low-voltage-side-referenced PMBus-compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring and other telemetry functions.

Owing to its megahertz bandwidth and low series impedance, the BCM performs as an efficient capacitance multiplier, enabling bulk capacitance across the 48V bus to be scaled down by a factor of 1/64 across the 384V bus. Capacitance multiplication cuts down the size and number of capacitors required by 48V PoL regulators while freeing up real estate at the point-of-load.

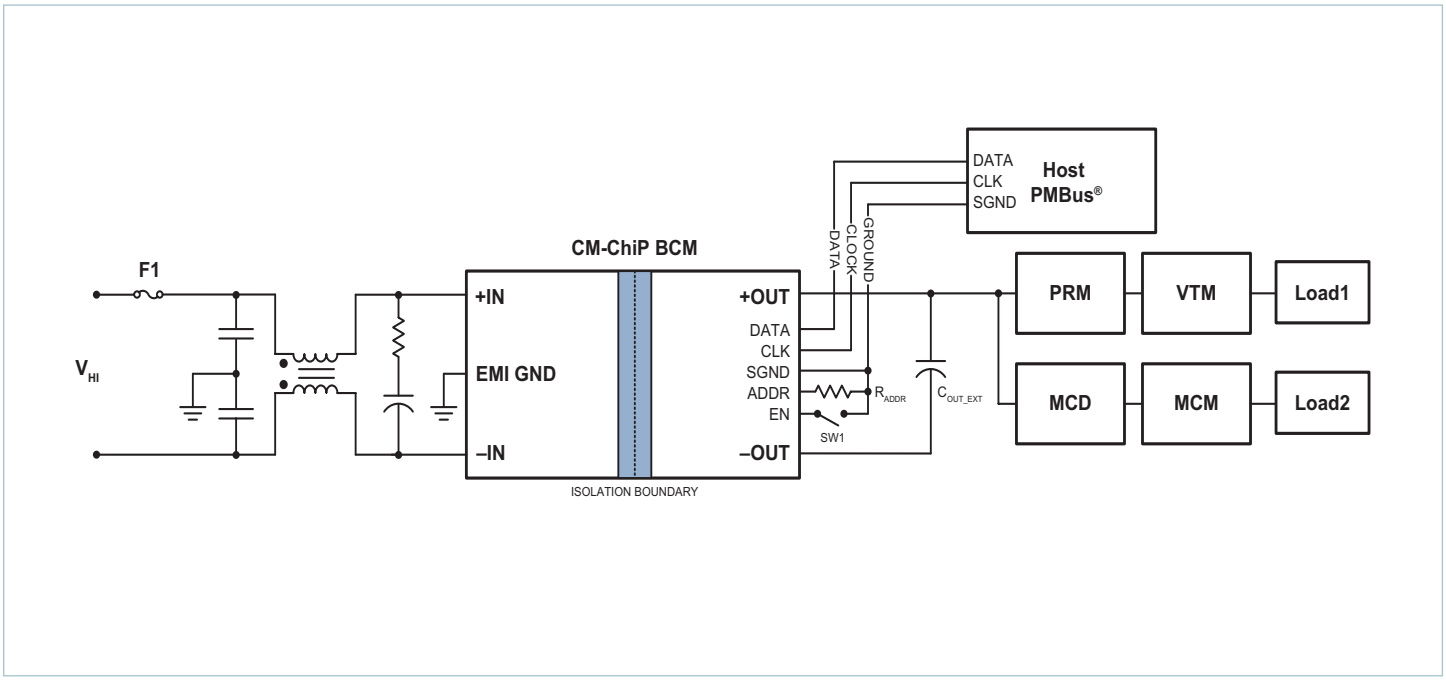
The CM-ChiP BCM module offers flexible thermal management options, with very low top- and bottom-side thermal impedances. Thermally-adept CM-ChiP-based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes.

Package Information

- Chassis-Mount CM-ChiP™ Package
  2.415 x 1.392 x 0.292in
  [61.33 x 35.35 x 7.42mm]
- Weight: 68g

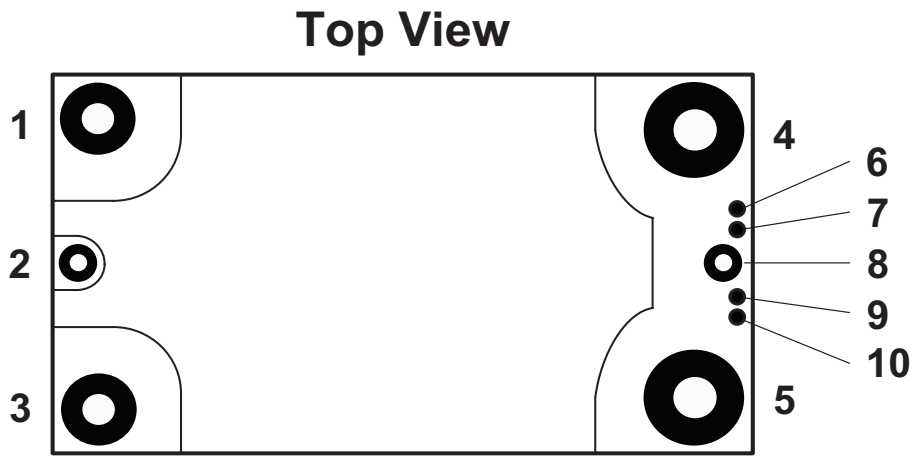
Note: Product images may not highlight current product markings.

Typical Applications



BCM6135CD1E5165yzz with PRM™ + VTM™ and MCD + MCM™

Pin Configuration



BCM6135 in a CM-ChiP Package
Chassis Mount

Pin Descriptions

Power Pins			
Pin Number	**Signal Name**	**Type**	**Function**
1	+HI	HIGH SIDE POWER	High-voltage-side positive power terminal
2	EMI GND	EMI GROUND	EMI ground terminal
3	–HI	HIGH SIDE POWER RETURN	High-voltage-side negative power terminal
4	+LO	LOW SIDE POWER	Low-voltage-side positive power terminal
5	–LO	LOW SIDE POWER RETURN	Low-voltage-side negative power terminal
Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
6	DATA	INPUT / OUTPUT	I²C™ data, PMBus® compatible
7	CLK	INPUT	I²C clock, PMBus compatible
8	SGND	SIGNAL GROUND	Signal ground
9	ADDR	INPUT	Address assignment, resistor based
10	EN	INPUT	Active-low enable pin, enables and disables the powertrain

Part Ordering Information

Part Number	Package Type	Product Grade	Option Field
BCM6135**C**D1E5165**T00**	**C** = CM-ChiP Chassis-Mount	**T** = –40 to 125°C	**00** = Step-Down

Storage and Handling Information

Attribute	Comments	Specification
Storage Temperature Range	T-Grade	–40 to 125°C
Operating Internal Temperature Range (T_{INT})	T-Grade	–40 to 125°C
Weight		68g
Terminal Finish	C145 Copper	
	Nickel	200µin
	Palladium	30µin
	Hard Gold	3 – 5µin
Package Plating		75µm copper with ENiG surface finish
ESD Rating	Human Body Model JEDEC JS-001-2017	Class 2, 2000V to < 4000V
	Charged Device Model JS-002-2018	Class C2b, 750V to < 1000V

Reliability and Agency Approvals

Attribute	Comments	Value	Unit
MTBF	Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled	19.8	MHrs
	MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer	8.52	
Agency Approvals/Standards	cTÜVus, UL 62368-1, CAN/CSA No. C22.2 62368-1, EN 62368-1		
	cTÜVus, UL 60950-1, CAN/CSA No. C22.2 60950-1, EN 60950-1		
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI	Powertrain disabled	–1	960	V
	Powertrain enabled		480	V
+LO to –LO		–1	60	V
DATA to SGND		–0.3	5.5	V
CLK to SGND		–0.3	5.5	V
ADDR to SGND		–0.3	3.6	V
Isolation Voltage / Dielectric Withstand	Basic insulation (high-voltage side to case)	2250		V_{DC}
	Reinforced insulation (high-voltage side to low-voltage side)	4242		
	Basic insulation (low-voltage side to case)	707		

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward-Direction Operation (High-Voltage Side to Low-Voltage Side)						
HI-Side Voltage Range, Continuous	V_{HI_DC}		260	384	410	V
HI-Side Voltage Range, Transient	V_{IN_TRANS}		260		410	V
HI-Side Voltage Initialization Threshold	$V_{\mu C\_ACTIVE}$	HI-side voltage where internal bias and controller are initialized (powertrain inactive)		150		V
HI-Side Quiescent Current	I_{HI_Q}	Disabled, EN inactive state, V_{HI_DC} = 384V		2		mA
No-Load Power Dissipation	$P_{HI\text{-}NL}$	V_{HI_DC} = 384V		14	42	W
		V_{HI_DC} = 260 – 410V			62	
Transformation Ratio	K	High voltage to low voltage K = V_{LO_DC} / V_{HI_DC}, at no load		1/8		V / V
LO-Side Current, Continuous	$I_{LO\_OUT\_DC}$				65	A
LO-Side Current, Pulsed	$I_{LO\_OUT\_PULSE}$	20ms pulse, 25% duty cycle			78	A
LO-Side Peak Overload Current	$I_{LO\_OUT\_OVLD}$	5ms			97.5	A
		1ms			104	
		500µs			110.5	
		200µs			123.5	
Efficiency, Ambient	η_{AMB}	V_{HI_DC} = 384V, $I_{LO\_OUT\_DC}$ = 65A	96.1	97.1		%
		V_{HI_DC} = 260 – 410V, $I_{LO\_OUT\_DC}$ = 65A	95.0			%
		V_{HI_DC} = 384V, $I_{LO\_OUT\_DC}$ = 32.5A	96.8	97.8		%
LO-Side Output Resistance	R_{LO_AMB}	V_{HI_DC} = 384V, $I_{LO\_OUT\_DC}$ = 65A	9.8	16.5	22.2	mΩ
Switching Frequency	F_{SW}	V_{HI_DC} = 384V, $I_{LO\_OUT\_DC}$ = 65A	1.1	1.2	1.3	MHz
		Over rated line, continuous load range, temperature	1.1		1.5	
LO-Side Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 65A, V_{HI_DC} = 384V, 20MHz BW		425		mV
Effective HI-Side Capacitance	C_{HI_INT}	Effective value at V_{HI_DC} = 384V		0.188		µF
Effective LO-Side Capacitance	C_{LO_INT}	Effective value at V_{LO_DC} = 48V		37.7		µF
Rated LO-Side Capacitance (External)	C_{LO_OUT}	Rated LO-side connected capacitance at start up, $I_{LO\_OUT\_DC}$ = 0A. Excessive capacitance may prevent module start up.			100	µF
Rated LO-Side Capacitance (External), Parallel Array Operation	$C_{LO\_OUT\_AEXT}$	C_{LO_EXT} Max = N • 0.5 • $C_{LO\_EXT\ MAX}$, where N = number of units in parallel				

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Protection Specification – Forward-Direction Operation (High-Voltage Side to Low-Voltage Side)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{HI\_DC} > V_{HI\_UVLO+}$		2000		ms
HI-Side Undervoltage Lockout Threshold	$V_{HI\_UVLO–}$		160	190		V
HI-Side Undervoltage Recovery Threshold	V_{HI_UVLO+}			230	260	V
HI-Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			10		V
HI-Side Undervoltage Lockout Response Time	t_{HI_UVLO}			200		µs
HI-Side Overvoltage Lockout Threshold	V_{HI_OVLO+}			435	445	V
HI-Side Overvoltage Recovery Threshold	$V_{HI\_OVLO–}$		410	425		V
HI-Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			10		V
HI-Side Overvoltage Lockout Response Time	t_{HI_OVLO}			200		µs
HI-Side Undervoltage/Overvoltage Retry Time	$t_{UVLO\_OVLO\_RETRY}$	Start up into persistent fault condition; Non-latching fault detection given: $V_{HI\_DC} > V_{\mu C\_ACTIVE}$		350		ms
HI-Side Undervoltage Start-Up Delay	$t_{HI\_UVLO+\_DELAY}$	From $V_{HI\_DC} = V_{HI\_UVLO+}$ to powertrain active, EN held in active state, (i.e., one-time start-up delay from application of V_{HI_DC} to V_{LO_DC})		440		ms
LO-Side Soft-Start Time	$t_{LO\_SOFT\_START}$	From powertrain active, no load; fast current limit protection disabled during soft-start		300		µs
LO-Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		79	94	100	A
LO-Side Output Overcurrent Response Time	$t_{LO\_OUT\_OCP}$			8		ms
LO-Side Output Short-Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$			145		A
LO-Side Output Short-Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shut-Down Threshold	T_{OTP+}	Temperature sensor located inside controller IC	100			°C
Overtemperature Recovery Threshold	$T_{OTP–}$	Temperature sensor located inside controller IC		90		°C

Operating Area

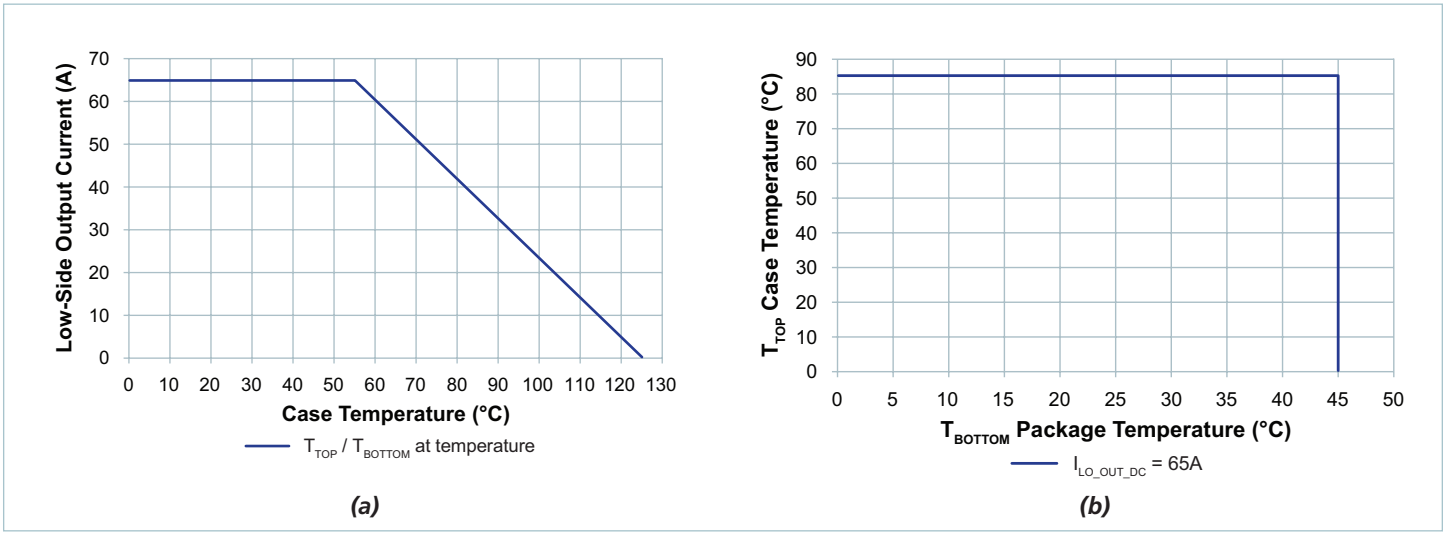


Figure 1 — *Specified thermal operating area: (a) equal top and bottom surface temperatures; (b) unequal top and bottom package surface temperatures.*

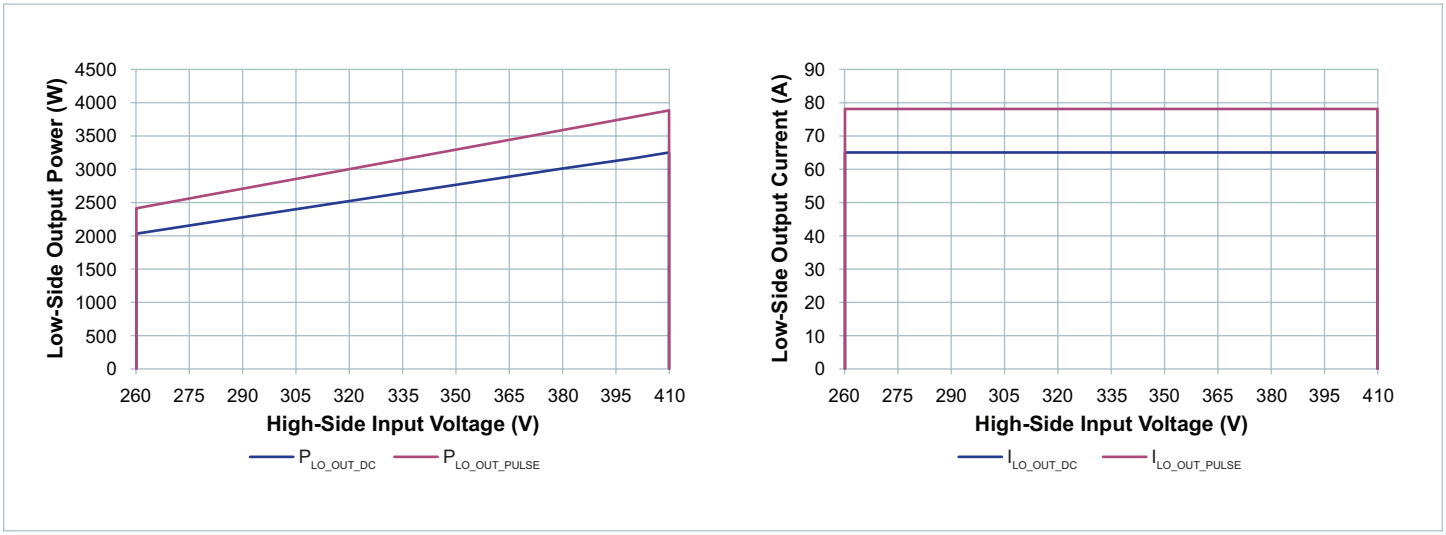


Figure 2 — *Specified electrical operating area using rated R_{LO_AMB}*

PMBus® Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Monitored Telemetry					
Attribute	**PMBus Read Command**	**Accuracy (Rated Range)**	**Functional Reporting Range**	**Update Rate**	**Reported Units**
HI-Side Voltage	(88h) READ_VIN	±2% (Powertrain Enabled)	160 – 480V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO-Side Voltage	(8Bh) READ_VOUT	±1%	0 – 60V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO-Side Current	(8Ch) READ_IOUT	–5%, +10%	0 – 95A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
Temperature	(8Dh) READ_TEMPERATURE_1	±7°C (Full Range)	–55 to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

Variable Parameters

- Variables can be written only when module is disabled with V_{HI} or $V_{HI\_DC} < V_{HI\_UVLO–}$.
- Module must remain in a disabled mode for 3ms after any changes to the variables below to allow sufficient time to commit changes to EEPROM.

Attribute	PMBus Command	Conditions / Notes	Accuracy (Rated Range)	Functional Reporting Range	Default Value
Turn-On Delay	(60h) TON_DELAY	Additional time delay to the undervoltage start-up delay	±50µs	0 – 100ms	0ms
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal temperature monitor	±7°C (Full Range)	0 – 100°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal temperature monitor	±7°C (Full Range)	0 – 100°C	100%

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.
Please note: For chassis mount model, Vicor part number 48705-3001R7 or equivalent will be needed for applications requiring the use of the signal pins. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

Enable (EN) Pin

- The EN pin is a standard analog I/O configured as an input to an internal µC.
- It is internally pulled high to 3.3V.
- When pulled high, the BCM internal bias will be disabled and the powertrain will be inactive.
- In an array of BCMs, EN pins should be interconnected to synchronize start up.
- PMBus® ON/OFF command has no effect if the BCM EN pin is not in the active state. This BCM has active low EN pin logic.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input	Start Up	EN to Powertrain Active Time	t_{EN_START}	V_{HI_DC} > V_{HI_UVLO+}, EN active, both conditions satisfied for t > $t_{HI\_UVLO+DELAY}$		**2**		ms
	Regular Operation	EN Voltage Threshold	V_{ENABLE}				**1**	V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull-up resistor		10		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$		**2.3**			V

SGND Pin

- All PMBus interface signals (CLK, DATA, ADDR, EN) are referenced to SGND pin.
- SGND pin and low-voltage-side power-return terminal (–LO) are common.
  To avoid noise interference, keep SGND signal separated from –LO in electrical design.

Address (ADDR) Pin

- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during start up and is stored until power is reset. This pin programs only a fixed and persistent address.
- This pin has an internal 10kΩ pullup resistor to 3.3V.
- 16 addresses are available. The range of each address is 206.25mV (total range for all 16 addresses is 0 – 3.3V).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Multi-Level Input	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR Leakage Current	I_{SADDR}	Leakage current			1	µA
	Start Up	ADDR Registration Time	t_{SADDR}	From V_{VDDB_MIN}		1		ms

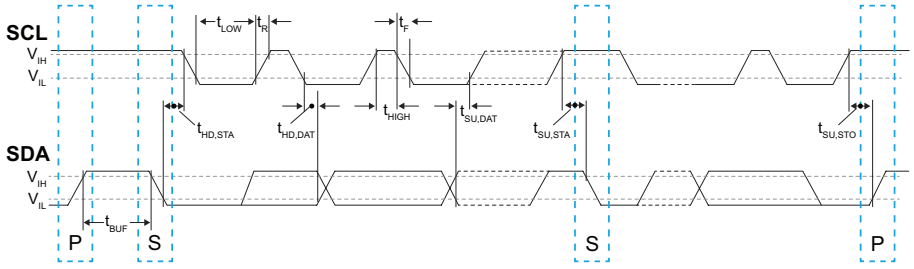
Signal Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.
Please note: For chassis mount model, Vicor part number 48705-3001R7 or equivalent will be needed for applications requiring the use of the signal pins. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

Serial Clock input (CLK) and Serial Data (DATA) Pins

- High-power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is not supported.
- PMBus® command compatible.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input / Output	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.1			V
			V_{IL}				0.8	V
		Output Voltage Threshold	V_{OH}		3			V
			V_{OL}				0.4	V
		Leakage Current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10 – 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Set-Up Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Set-Up Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Set-Up Time	$t_{SU:DAT}$		100			ns
		Clock Low Time Out	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F		20		300	ns
		Clock or Data Rise Time	t_R		20		300	ns



Application Characteristics

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high side to low side). See associated figures for general trend data.

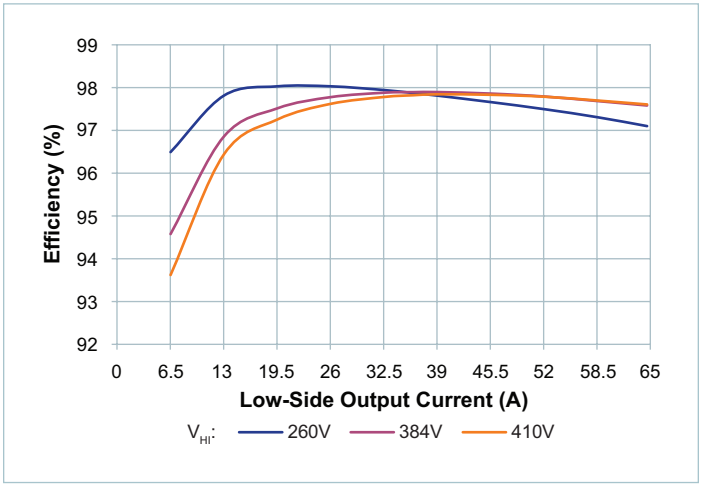


Figure 3 — *Efficiency at T_{TOP}, T_{BOTTOM} = –40°C*

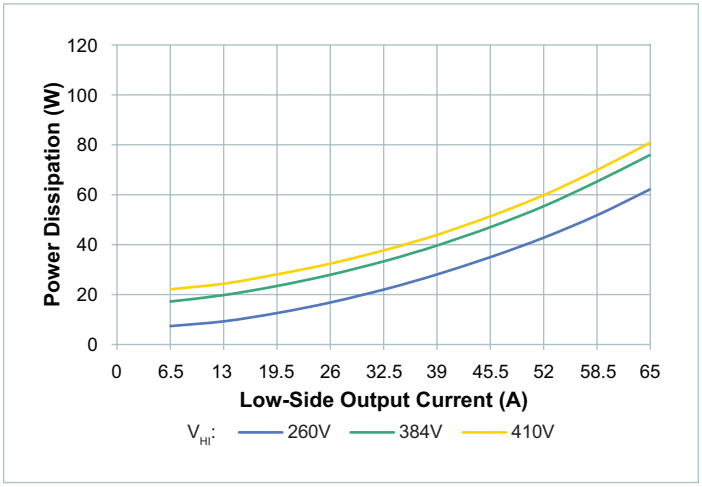


Figure 4 — *Power dissipation at T_{TOP}, T_{BOTTOM} = –40°C*

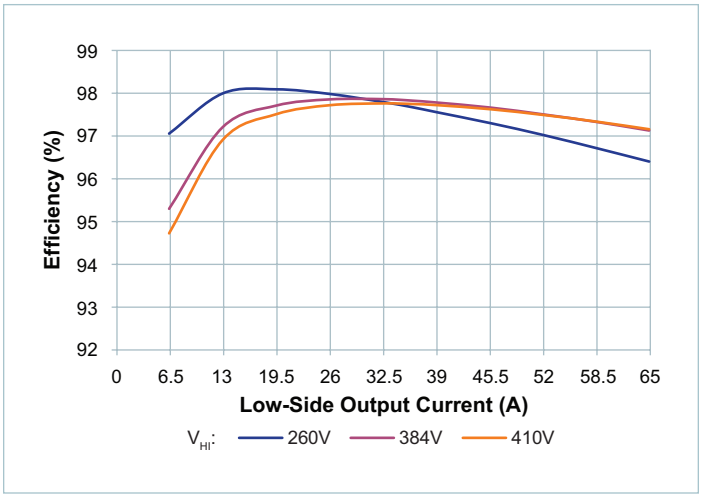


Figure 5 — *Efficiency at T_{TOP}, T_{BOTTOM} = 25°C*

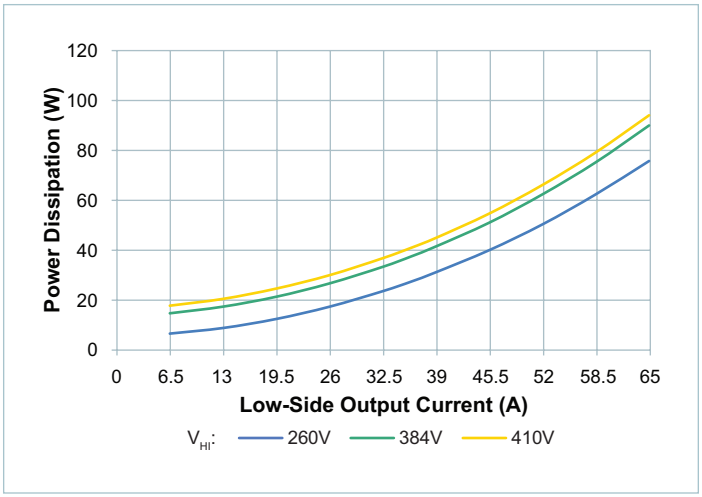


Figure 6 — *Power dissipation at T_{TOP}, T_{BOTTOM} = 25°C*

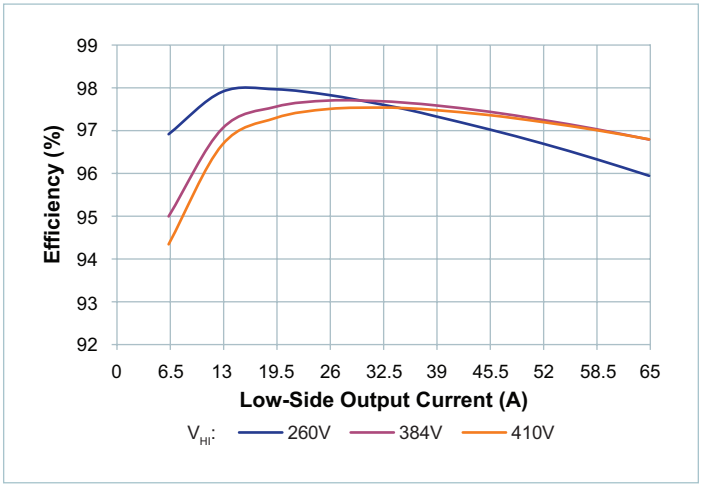


Figure 7 — *Efficiency at T_{TOP} = 85°C, T_{BOTTOM} = 45°C*

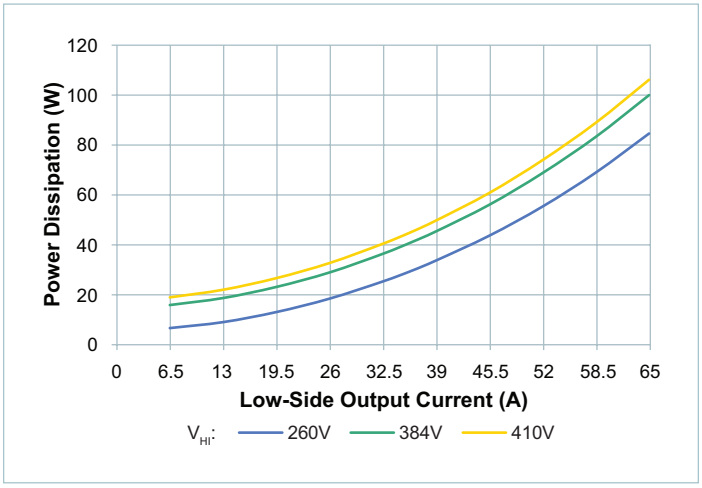


Figure 8 — *Power dissipation at T_{TOP} = 85°C, T_{BOTTOM} = 45°C*

Application Characteristics (Cont.)

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (primary side to secondary side). See associated figures for general trend data.

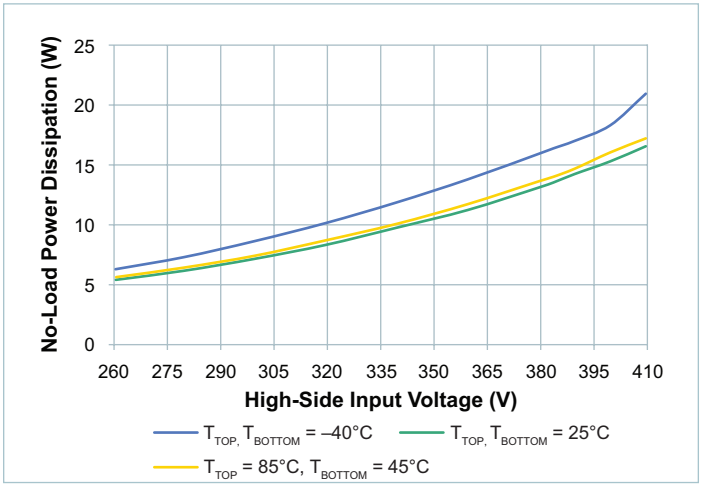


Figure 9 — *No-load power dissipation vs. V_{HI_DC}*

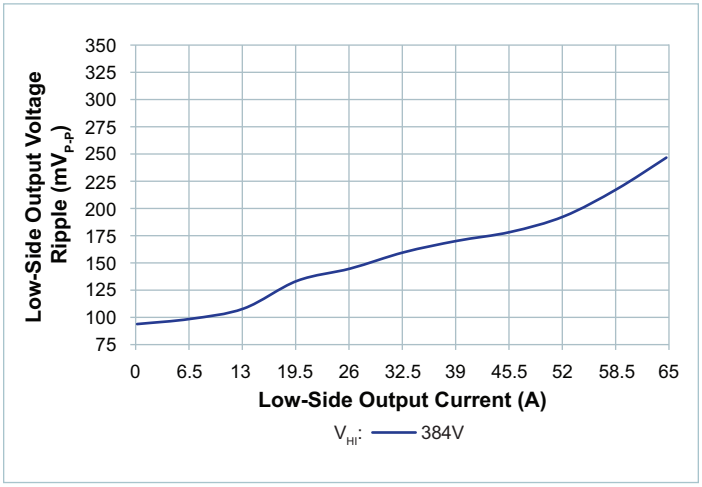


Figure 10 — *$V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; no external $C_{LO\_OUT\_EXT}$; board-mounted module, scope setting: 20MHz analog BW*

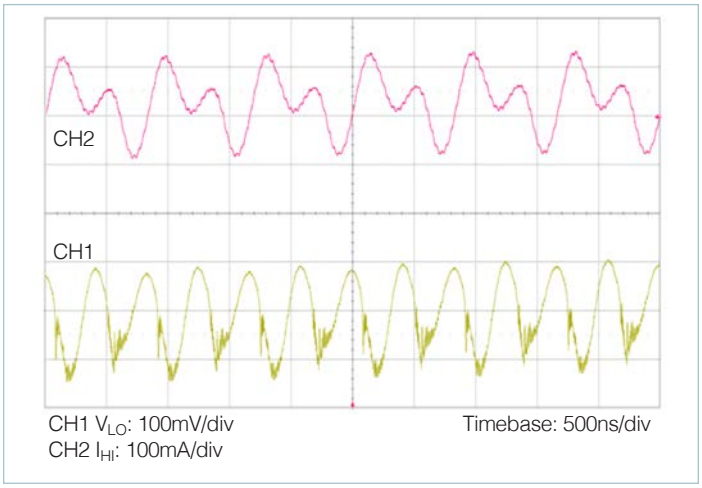


Figure 11 — *Full-load low-side voltage and high-side current ripple; no external $C_{LO\_OUT\_EXT}$*

Application Characteristics (Cont.)

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (primary side to secondary side). See associated figures for general trend data.

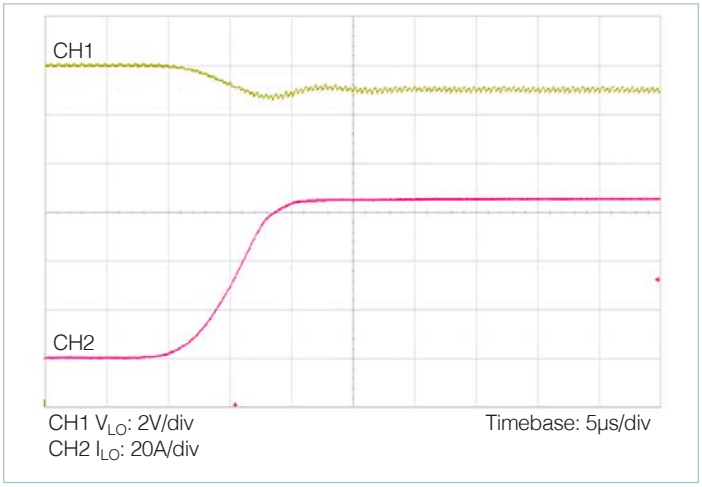


Figure 12 — *0 – 65A transient response, V_{HI} = 384V, $C_{LO\_OUT\_EXT}$ = 0µF*

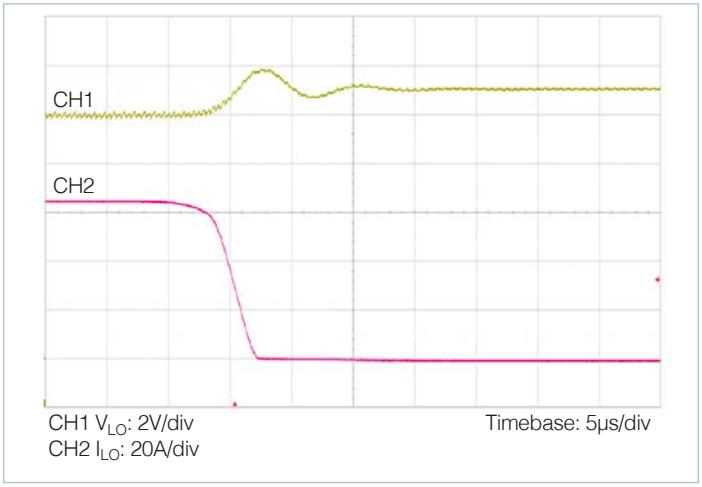


Figure 13 — *65 – 0A transient response, V_{HI} = 384V, $C_{LO\_OUT\_EXT}$ = 0µF*

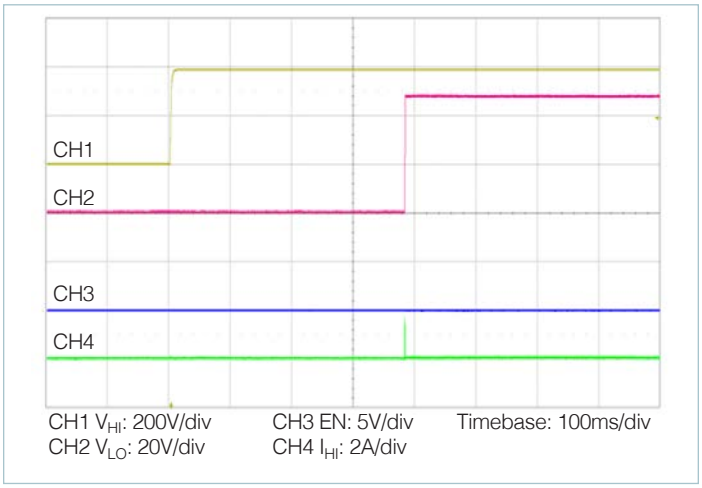


Figure 14 — *Start up from application of V_{HI} = 384V, 0% $I_{LO\_OUT\_DG}$, 100% $C_{LO\_OUT\_EXT}$*

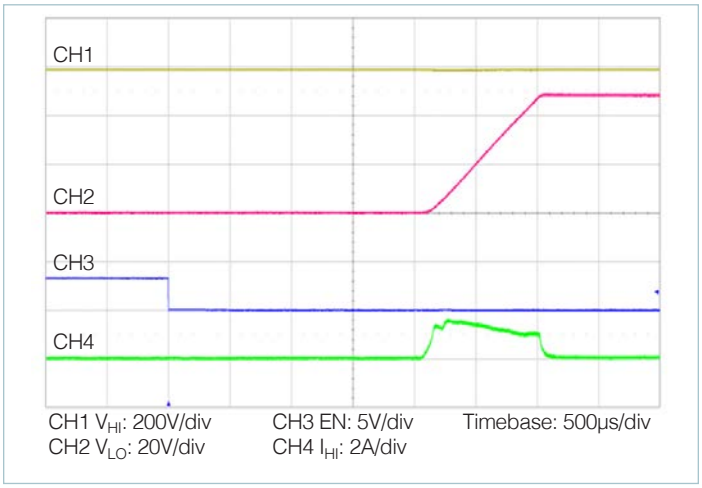


Figure 15 — *Start up from application of EN with pre-applied V_{HI} = 384V, 0% $I_{LO\_OUT\_DG}$, 100% $C_{LO\_OUT\_EXT}$*

BCM in a CM-ChiP™

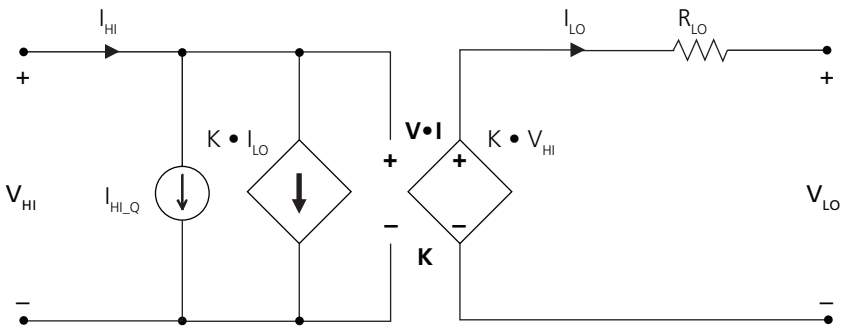


Figure 16 — *BCM DC model*

The BCM uses a high-frequency resonant tank to move energy from the high-voltage side to low-voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the high-side voltage and the low-side current. A small amount of capacitance embedded in the high-voltage-side and low-voltage stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM6135CD1E5165Yzz can be simplified into the model shown in Figure 16.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM. Rearranging Equation 1:

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM, and is a function of the R_{DS_ON} of the high-voltage-side and low-voltage-side MOSFETs and the winding resistance of the power transformer. I_{HI_Q} represents the quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI}.

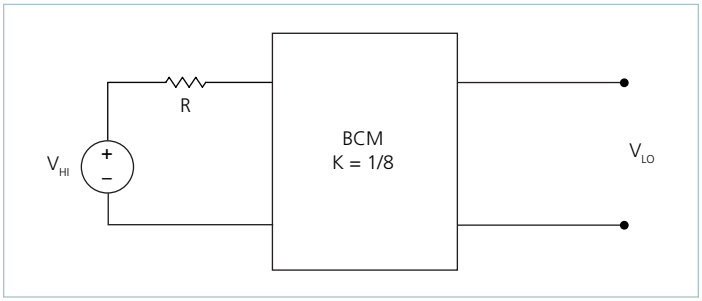


Figure 17 — *K = 1/8 BCM with series high-voltage-side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R on the high-voltage side of the BCM is effectively scaled by K^2 with respect to the low-voltage side.

Assuming that R = 1Ω, the effective R as seen from the low-voltage side is 16mΩ, with K = 1/8.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the high-voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 18.

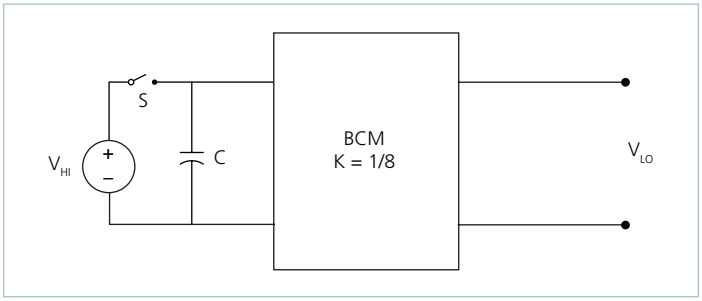


Figure 18 — *BCM with high-voltage-side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \quad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \quad (9)$$

The equation in terms of the low-voltage side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low-voltage side when expressed in terms of the high-voltage side. With K = 1/8 as shown in Figure 18, C = 1µF would appear as C = 64µF when viewed from the low-voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low-loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \quad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \quad (11)$$

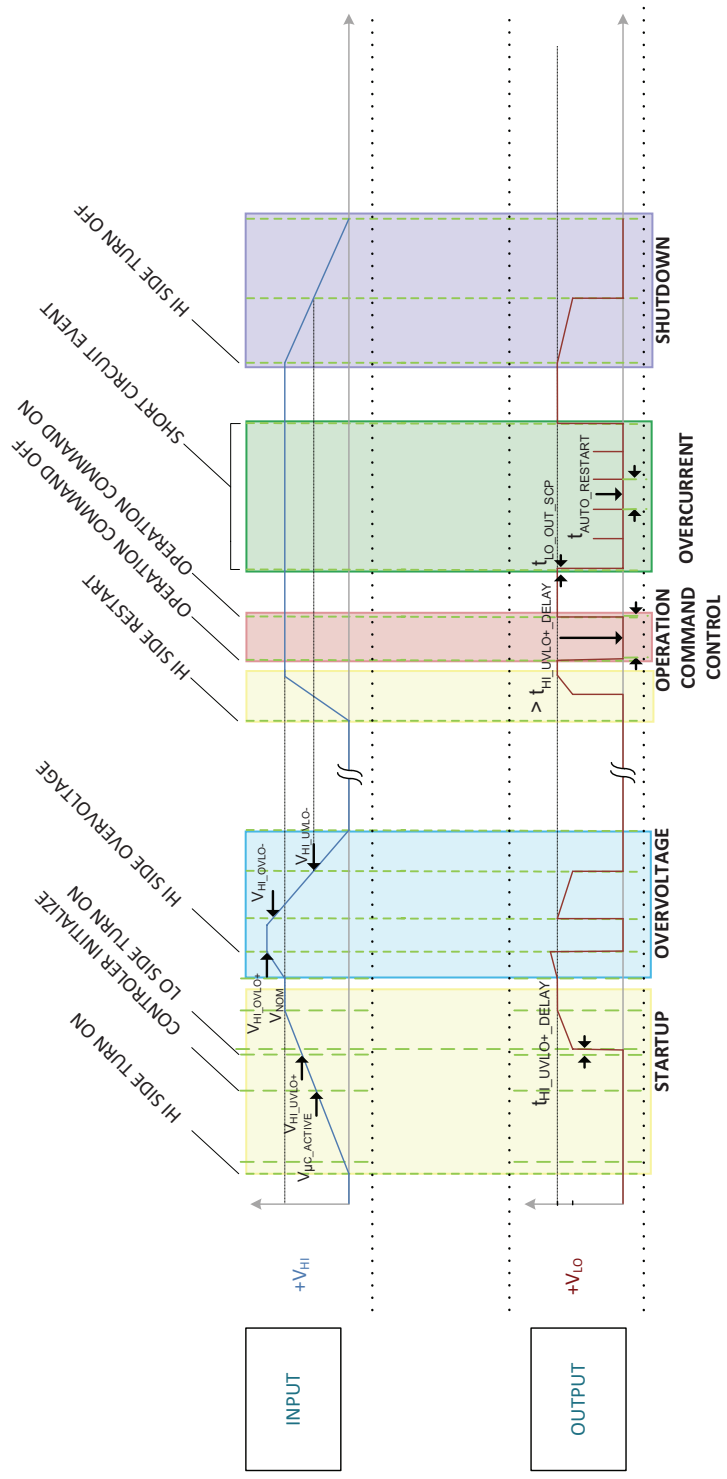
The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \quad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Timing Diagram (Forward Direction)



Input and Output Filter Design

A major advantage of BCM systems versus conventional PWM converters is that the transformer based BCM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of high-voltage-side voltage and low-voltage-side current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the high-voltage-side and low-voltage-side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the BCM's dynamic response, the impedance presented to its high-voltage-side terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- *Further reduce high-voltage-side and/or low-voltage-side voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the high-voltage-side source will appear at the low-voltage side of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module high- and low-voltage-side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating high-voltage-side range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Total load capacitance at the low-voltage side of the BCM shall not exceed the specified maximum. Owing to the wide bandwidth and minimal low-voltage-side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the high-voltage side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the high-voltage side appears as effective capacitance on the low-voltage side per the relationship defined in Equation 13.

$$C_{LO} = \frac{C_{HI}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Current Sharing

The performance of the BCM topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each BCM in an array is required to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays.

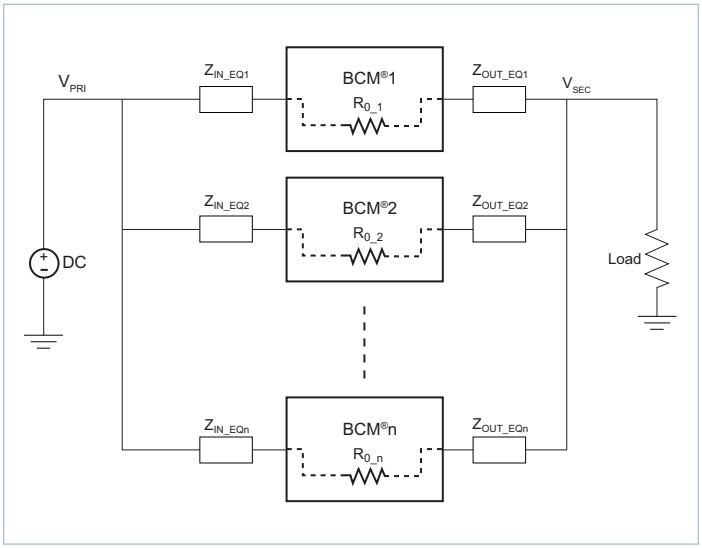


Figure 19 — *BCM parallel array*

Fuse Selection

In order to provide flexibility in configuring power systems, CM-ChiP™ modules are not internally fused. Input line fusing of CM-ChiP products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: See safety agency approvals.

Thermal Considerations

The CM-ChiP™ module provides a high degree of flexibility in that it presents several pathways to remove heat from the internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the high- and low-voltage-side power terminals. The extent to which these surfaces are cooled is a key component in determining the maximum current that is available from a CM-ChiP.

Since the CM-ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are multiple pathways to remove heat from the CM-ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors.

Figure 20 shows the "thermal circuit" for a BCM6135 CM-ChiP in a two-sided cooling application, where the product is cooled through a heat sink at the bottom and a separate heat sink at the top. In this case, the BCM top and bottom (each heat sink) surface temperatures are represented as T_{TOP} and T_{BOTTOM}. This thermal system can now be very easily analyzed as an electrical network with simple resistors, voltage sources and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

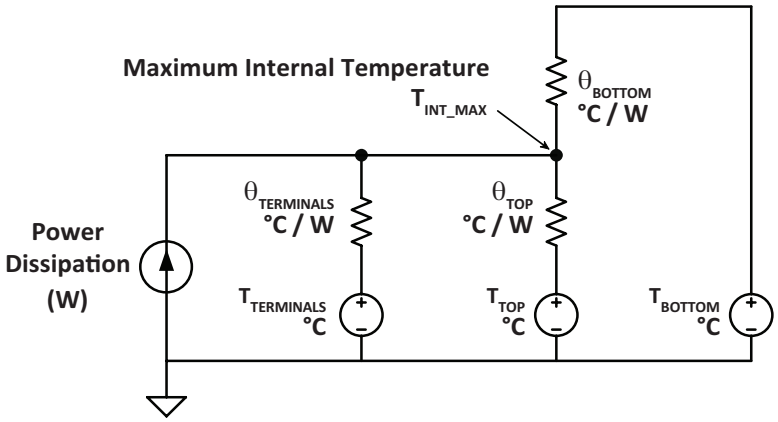


Figure 20 — *Two-sided cooling thermal model*

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
$\theta_{TERMINALS}$	3.6	From the hottest component inside the BCM to the high- and low-voltage-side terminals
θ_{TOP}	1.1	From the hottest component inside the BCM to the top package surface
θ_{BOTTOM}	0.85	From the hottest component inside the BCM to the bottom package surface

Table 1 — *Thermal impedances*

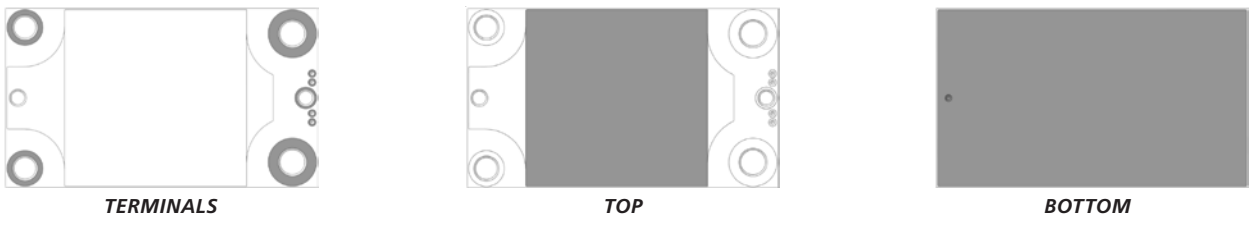
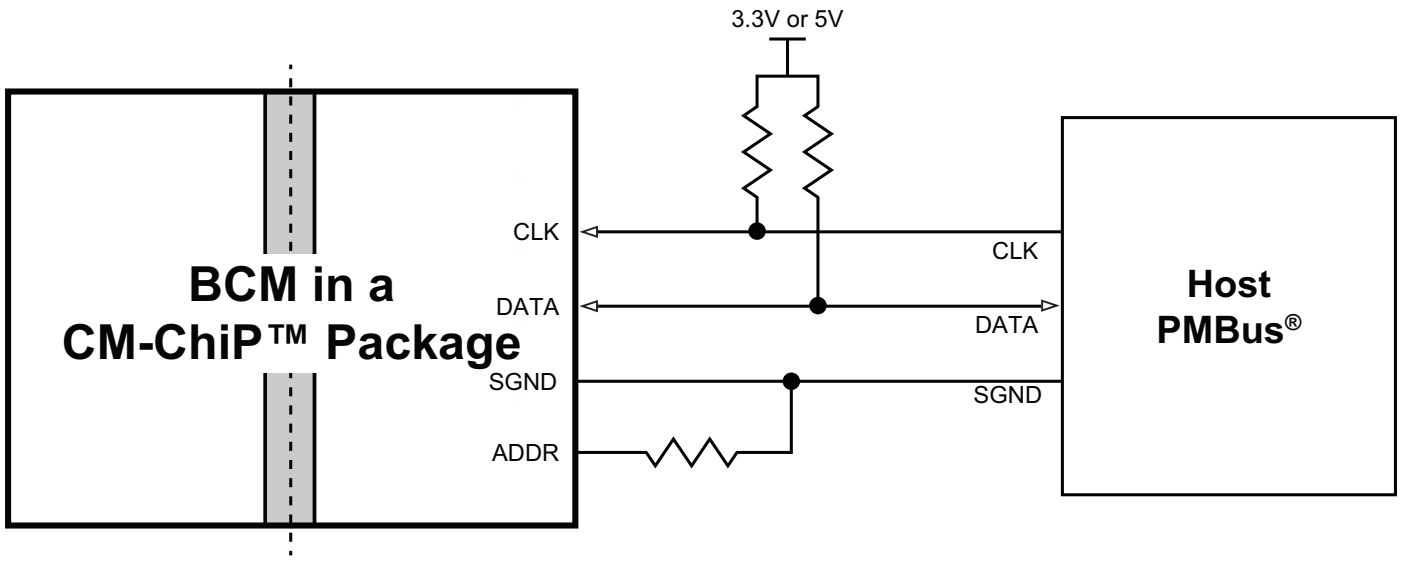


Figure 21 — *Thermal model boundary conditions; area defined as shaded*

System Diagram for PMBus Interface



The controller of the CM-ChiP BCM is referenced to the low-voltage-side signal ground (SGND).

The CM-ChiP BCM provides the Host PMBus system with accurate telemetry monitoring and reporting, in addition to corresponding status flags. The BCM is periodically polled for status by the Host PMBus.

The BCM enables the PMBus compatible Host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.

PMBus Interface

Refer to "PMBus® Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus specifications details at http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of the predetermined 16 possible addresses shown in the table below using a resistor between the ADDR pin and SGND pin.

The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power up, the BCM controller will sample the address pin voltage and will keep this address until device power is removed.

ID	Child Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The BCM controller employs a direct data format where all reported measurements are in volts, amperes, degrees Celsius or seconds. The Host uses the following PMBus specification to interpret received values metric prefixes. Note that the COEFFICIENTS command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the BCM controller

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
OT_FAULT_LIMIT	4Fh	1	2	0
OT_WARN_LIMIT	50h	1	2	0
TON_DELAY	60h	1	3	0
READ_EOUT	87h	1	0	0
READ_VIN	88h	1	1	0
READ_VOUT	8Bh	1	2	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0

No special formatting is required when modifying the supervisory limits and warnings.

Supported Command List

Command	Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Data Bytes
OPERATION	01h	Turn BCM on or off	80h	Write Byte	Read Byte	1
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the BCM	1Dh	N/A	Read Byte	1
CLEAR_FAULTS	03h	Clear all faults	N/A	Send Byte	N/A	None
CAPABILITY	19h	PMBus® key capabilities set by factory	A0h	N/A	Read Byte	1
OT_FAULT_LIMIT	4Fh [g]	Overtemperature protection	64h	Write Word	Read Word	2
OT_WARN_LIMIT	51h [g]	Overtemperature warning	64h	Write Word	Read Word	2
TON_DELAY	60h [g]	Startup delay in addition to fixed delay	01h	Write Word	Read Word	2
STATUS_BYTE	78h	Summary of faults	00h	Write Byte	Read Byte	1
STATUS_WORD	79h	Summary of fault conditions	00h	Write Word	Read Word	2
STATUS_IOUT	7Bh	Overcurrent fault status	00h	N/A	Read Byte	1
STATUS_INPUT	7Ch	Overvoltage and undervoltage fault status	00h	N/A	Read Byte	1
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	N/A	Read Byte	1
STATUS_CML	7Eh	PMBus communication fault	00h	Write Byte	Read Byte	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	Write Byte	Read Byte	1
READ_EOUT	87h	Output energy meter data	00h	N/A	Block Read	6
READ_VIN	88h	Reads high side voltage	FFFFh	N/A	Read Word	2
READ_VOUT	8Bh	Reads low side voltage	FFFFh	N/A	Read Word	2
READ_IOUT	8Ch	Reads low side current	FFFFh	N/A	Read Word	2
READ_TEMPERATURE_1	8Dh	Reads internal temperature	FFFFh	N/A	Read Word	2
READ_POUT	96h	Reads low side power	FFFFh	N/A	Read Word	2
PMBUS_REVISION	98h	PMBus-compatible revision	33h	N/A	Read Byte	1
MFR_ID	99h	Internal controller ID	"VI"	N/A	Block Read	2
MFR_MODEL	9Ah	Internal controller or BCM model	Part Number	N/A	Block Read	18
MFR_REVISION	9Bh	Internal controller or BCM revision	FW and HW revision	N/A	Block Read	18
MFR_LOCATION	9Ch	Internal controller or BCM factory location	"AP"	N/A	Block Read	2
MFR_DATE	9Dh	Internal controller or BCM manufacturing date	"YYWW"	N/A	Block Read	4
MFR_SERIAL	9Eh	Internal controller or BCM serial number	Serial Number	N/A	Block Read	16
MFR_VIN_MIN	A0h	Minimum rated high side voltage	Varies per BCM	N/A	Read Word	2
MFR_VIN_MAX	A1h	Maximum rated high side voltage	Varies per BCM	N/A	Read Word	2
MFR_VOUT_MIN	A4h	Minimum rated low side voltage	Varies per BCM	N/A	Read Word	2
MFR_VOUT_MAX	A5h	Maximum rated low side voltage	Varies per BCM	N/A	Read Word	2
MFR_IOUT_MAX	A6h	Maximum rated low side current	Varies per BCM	N/A	Read Word	2
MFR_POUT_MAX	A7h	Maximum rated low side power	Varies per BCM	N/A	Read Word	2
READ/WRITE USER DATA_00	B0h	Custom user data space	00h	Block Write	Block Read	29
READ/WRITE USER DATA_01	B1h	Custom user data space	00h	Block Write	Block Read	29
READ/WRITE USER DATA_02	B2h	Custom user data space	00h	Block Write	Block Read	255
READ/WRITE USER DATA_03	B3h	Custom user data space	00h	Block Write	Block Read	255
BCM_EN_POLARITY	D0h [g]	Set BCM EN pin polarity	00h	Write Byte	Read Byte	1
READ_K_FACTOR	D1h	Reads K factor	Varies per BCM	N/A	Read Word	2

[g] The BCM must be in a disabled state by either EN pin control or OPERATION (01h) off command during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus® communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the parent sends the child device address followed by a write bit. Once the child acknowledges, the parent proceeds with the command code and then similarly the data byte.

1	7	1	1	8	1	8	1	1
S	Child Address	Wr	A	Command Code	A	Data Byte	A	P
		x = 0	x = 0		x = 0		x = 0	

S Start Condition

Sr Repeated Start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Parent to Child

From Child to Parent

... Continued next line

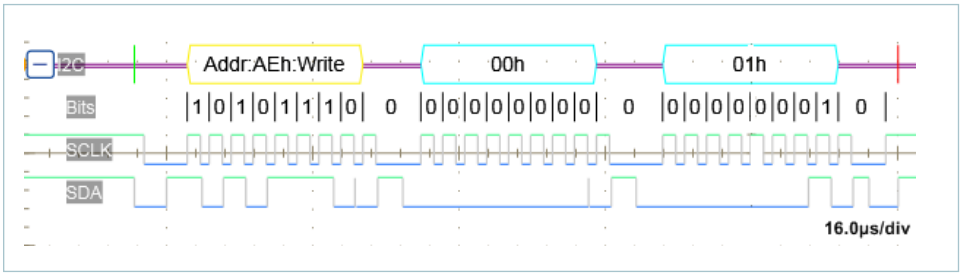


Figure 22 — *PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Write Byte with PEC (Packet Error Checking) Protocol:

1	7	1	1	8	1	8	1	8	1	1
S	Child Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P
		x = 0	x = 0		x = 0		x = 0		x = 0	

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a child Address. After receiving the READ bit, the BCM controller begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Child Address	Wr	A	Command Code	A	Sr	Child Address	Rd	A	Data Byte	A	P
		x = 0	x = 0		x = 0			x = 1	x = 0		x = 1	

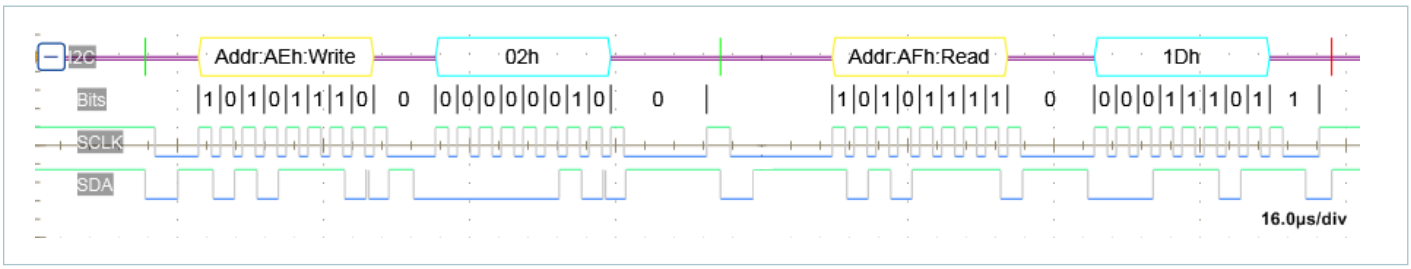
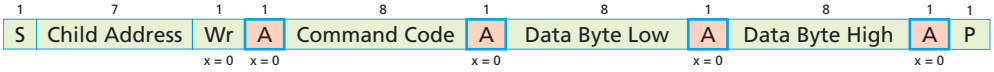


Figure 23 — *ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.



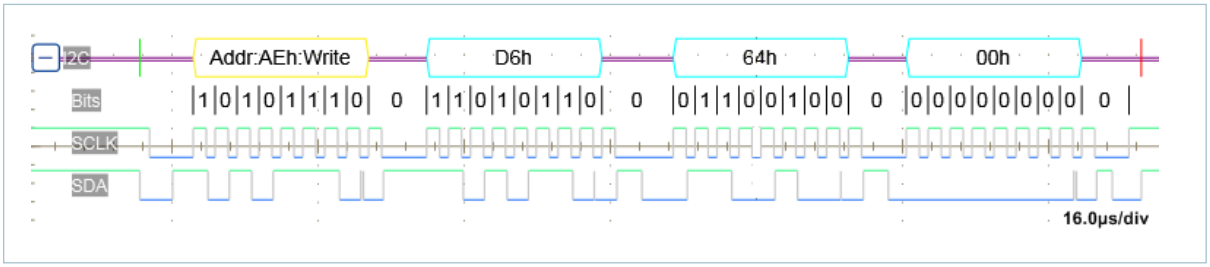
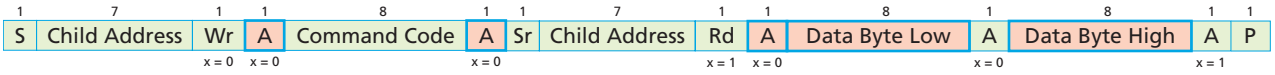


Figure 24 — *TON_DELAY COMMAND (D6h)_WRITE WORD PROTOCOL*

Read Word protocol:



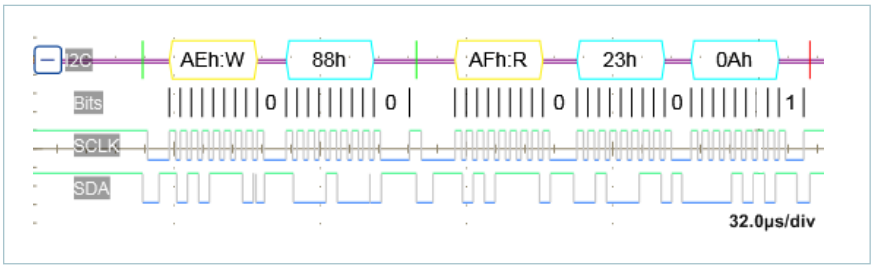
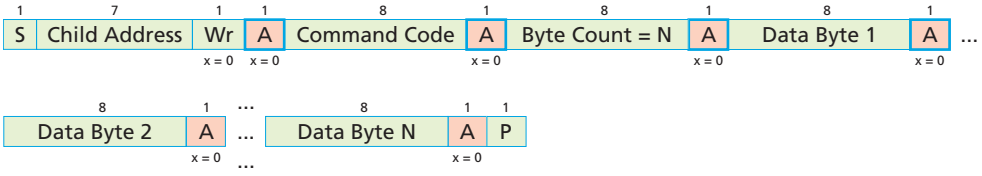


Figure 25 — *MFR_VIN_MIN COMMAND (88h)_READ WORD PROTOCOL*

Write Block protocol:



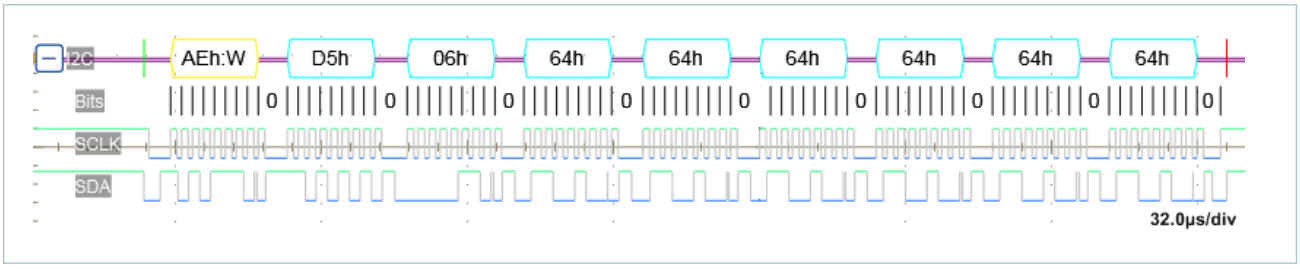
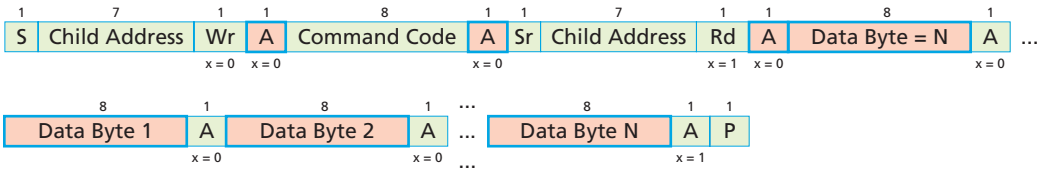


Figure 26 — *SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



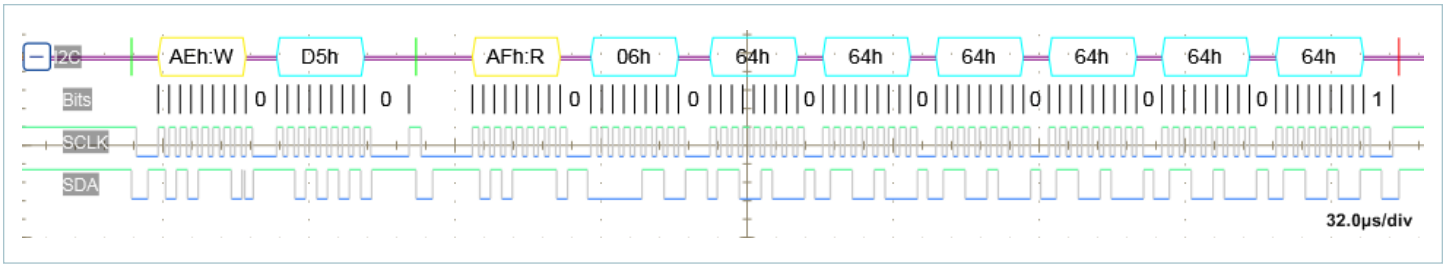
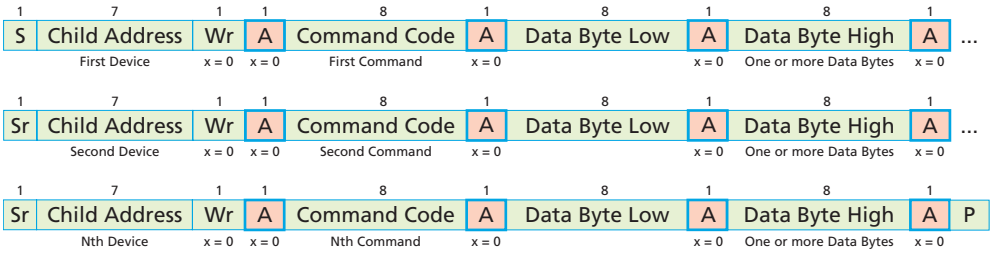


Figure 27 — *SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:



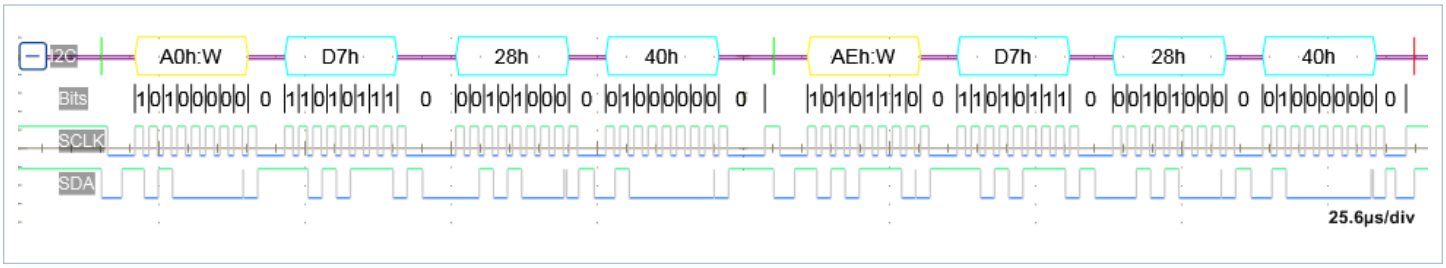


Figure 28 — *DISABLE_FAULT COMMAND (D7h)_WRITE*

Note that only one command per device is allowed in a group command.

Supported Commands Transaction Type

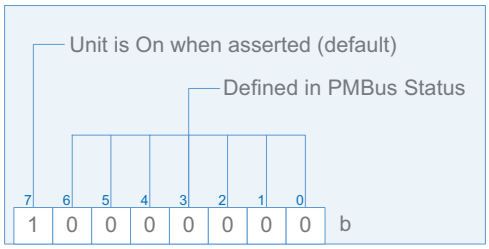
Supported command access privileges are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type
OPERATION	01h	R/W
ON_OFF_CONFIG	02h	R
CLEAR_FAULTS	03h	W
CAPABILITY	19h	R
OT_FAULT_LIMIT	4Fh	R/W
OT_WARN_LIMIT	51h	R/W
TON_DELAY	60h	R/W
STATUS_BYTE	78h	R/W
STATUS_WORD	79h	R/W
STATUS_IOUT	7Bh	R
STATUS_INPUT	7Ch	R
STATUS_TEMPERATURE	7Dh	R
STATUS_CML	7Eh	R/W
STATUS_MFR_SPECIFIC	80h	R/W
READ_EOUT	87h	R
READ_VIN	88h	R
READ_VOUT	8Bh	R
READ_IOUT	8Ch	R
READ_TEMPERATURE_1	8Dh	R
READ_POUT	96h	R
PMBUS_REVISION	98h	R
MFR_ID	99h	R
MFR_MODEL	9Ah	R
MFR_REVISION	9Bh	R
MFR_LOCATION	9Ch	R
MFR_DATE	9Dh	R
MFR_SERIAL	9Eh	R
MFR_VIN_MIN	A0h	R
MFR_VIN_MAX	A1h	R
MFR_VOUT_MIN	A4h	R
MFR_VOUT_MAX	A5h	R
MFR_IOUT_MAX	A6h	R
MFR_POUT_MAX	A7h	R
READ/WRITE USER DATA_00	B0h	R/W
READ/WRITE USER DATA_01	B1h	R/W
READ/WRITE USER DATA_02	B2h	R/W
READ/WRITE USER DATA_03	B3h	R/W
BCM_EN_POLARITY	D0h	R/W

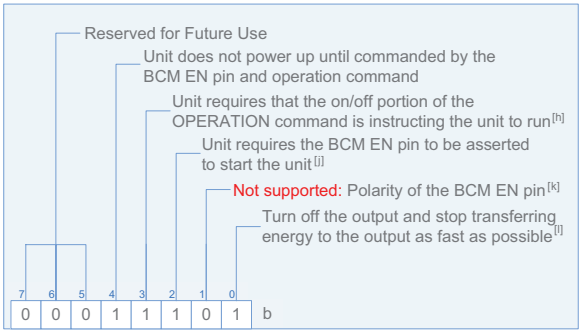
OPERATION Command (01h)

The OPERATION command and the BCM EN pin can both be used to turn on and off the connected BCM. Note that the Host OPERATION command will not enable the BCM if the BCM EN pin is disabled in hardware with respect to the pre-set pin polarity. The OPERATION command provides ON/OFF control only with the BCM EN pin active.

If synchronous start up is required in the system, it is recommended to use the command from Host PMBus® or the BCM EN pin in order to achieve simultaneous array start up.



ON_OFF_CONFIG Command (02h

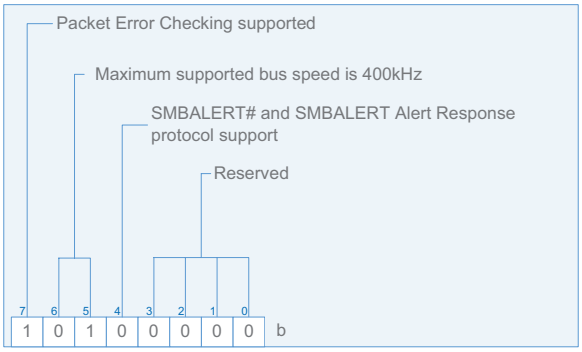


[h] The BCM EN pin is ALWAYS to be asserted for power up. The BCM_EN_POLARITY command (D0h) bit[1] defines the logic level required for the control pin (i.e., BCM Enable pin) to be asserted.
[j] With respect to the BCM EN pin if used in system.
[k] See MFR_SPECIFIC_00 / BCM_EN_POLARITY to change the Polarity of the BCM Enable Pin.
[l] The BCM powertrain once disabled cannot sink current.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared. All faults are latched once asserted in the BCM. Registered faults will not be cleared when disabling the BCM powertrain by the EN pin, sending the OPERATION command, or by lowering the high side voltage below the undervoltage protection threshold.

CAPABILITY Command (19h)



The BCM returns a default value of A0h. This value indicates that the PMBus® frequency supported is up to 400kHz and that Packet Error Checking (PEC) is supported. SMBALERT# is not supported.

OT_FAULT_LIMIT Command (4Fh), OT_WARN_ LIMIT Command (51h),

The values of these registers are set in non-volatile memory and can only be written when the BCM is disabled.

The values of the above mentioned faults and warnings are set by default to 100% of the respective BCM model supervisory limits. However, these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80%, one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a Host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the Electrical Specifications. In general, once a fault is detected, the BCM powertrain will shut down and attempt to auto-restart after a predetermined delay.

TON_DELAY Command (60h)

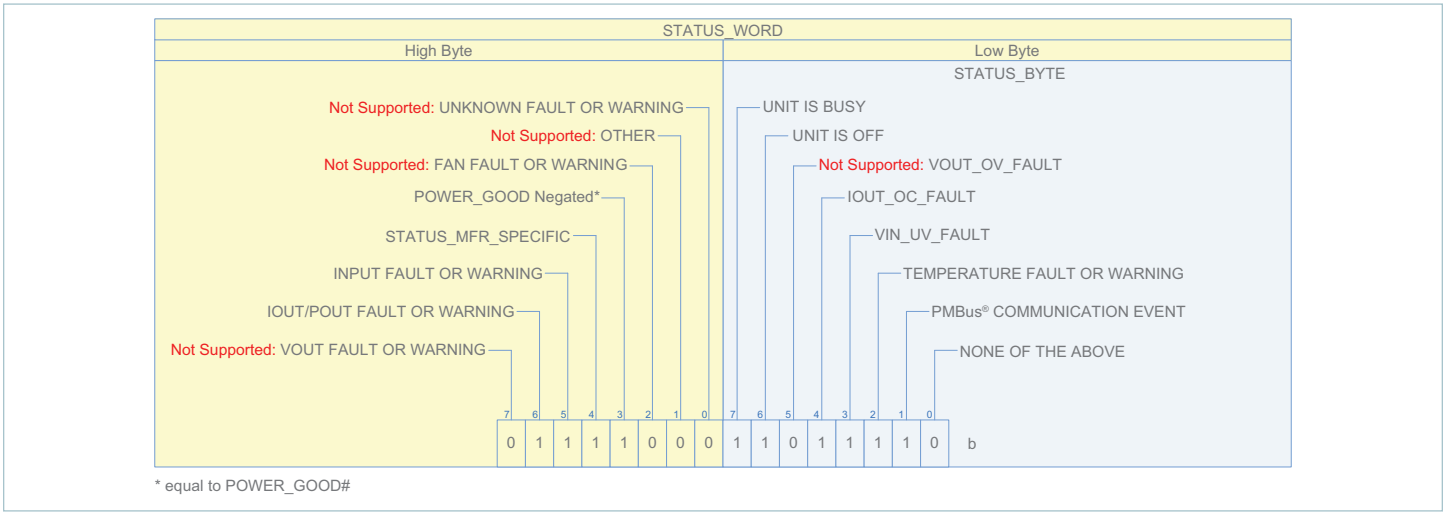
The value of this register word is set in non-volatile memory and can only be written when the BCM is disabled.

The maximum possible delay is 100ms. Default value is set to (01h). The reported value can be interpreted using the following equation.

$$TON\_DELAY_{ACTUAL} = t_{REPORTED} \bullet 10^{-3}(s)$$

Staggering start up in an array is possible with the TON_DELAY Command. This delay will be in addition to any start-up delay inherent in the BCM module. For example: start-up delay from application of V_{IN} is typically 20ms. When TON_DELAY is greater than zero, the set delay will be added to it.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the Host or once the BCM input power is removed.

This includes undervoltage fault, overvoltage fault, overtemperature fault, overtemperature warning, undertemperature fault and communication faults.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus® Power System Management Protocol Specification – Part II – Revision 1.3 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set, when the BCM is not in the active state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared, when the BCM is in the active state, 5ms after the powertrain is activated allowing for soft start to elapse.

POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

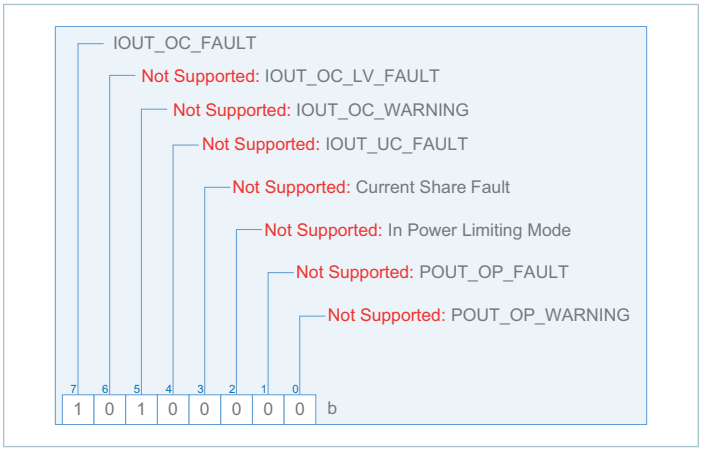
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (80h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and Host notification by temporarily acquiring bus parent status is not supported.

If the BCM is powered by $V_{HI} \geq V_{\mu C\text{-}ACTIVE}$, it will retain the last telemetry data and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard, which requires that status bits remain set until specifically cleared. Note that in the case where the BCM V_{IN} is lost, i.e., $V_{\mu C\text{-}ACTIVE} \leq V_{HI} \leq V_{HI\_UVLO+}$, the status will always indicate an undervoltage fault, in addition to any other fault that occurred.

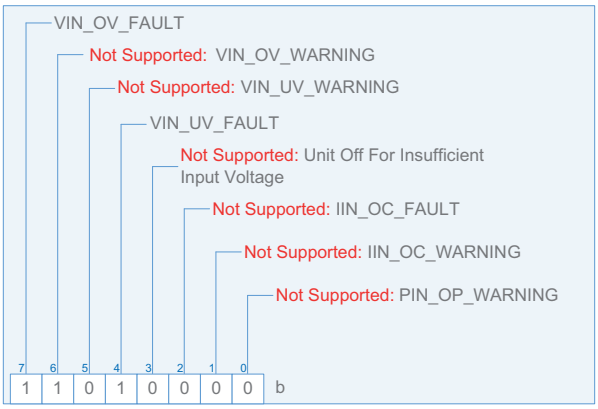
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



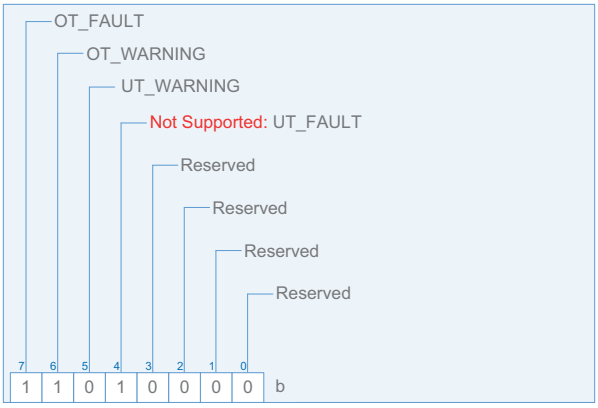
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



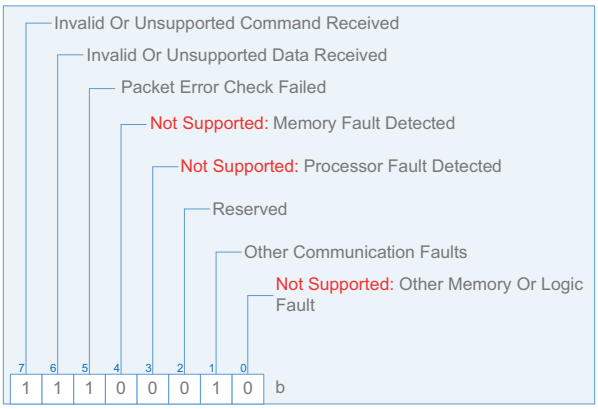
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

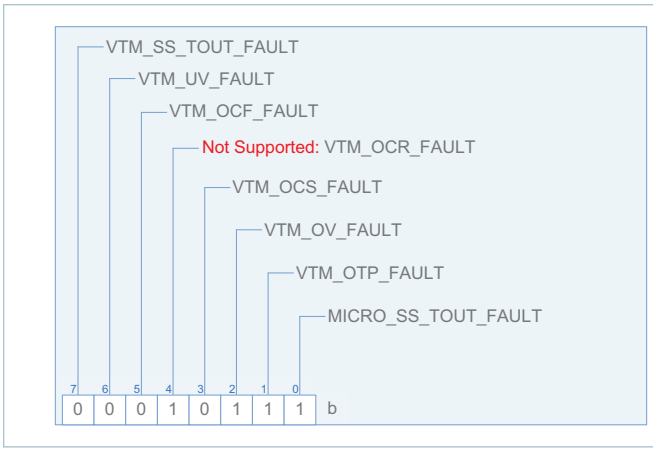
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus® command or data or other communication fault occurs.

STATUS_MFR_SPECIFIC (80h)



The BCM consists of a supervisory microcontroller and a powertrain controller. This register reports powertrain controller faults. The VTM_SS_TOUT_FAULT, if asserted, indicates a soft-start timeout fault. VTM_UV_FAULT and VTM_OV_FAULT report undervoltage and overvoltage fault conditions reported by the powertrain controller. In the event of an short circuit condition, the VTM_OCF_FAULT will be asserted. An overcurrent condition is indicated by the VTM_OCS_FAULT bit. The powertrain controller monitors the BCM internal temperature. An overtemperature shut-down condition is indicated by assertion of the VTM_OTP_FAULT bit.

The MICRO_SS_TOUT_FAULT bit, if asserted, refers to a soft-start time-out condition detected by the supervisory controller.

Unsupported bits are indicated above. A one indicates a fault.

READ_EOUT (87h)

This command returns output (LO side) energy metering data for computation of average output power delivery. A read will return 6 bytes of data as defined in the following table. The user shall use the BLOCK READ command structure specified in SMBus specification and also listed as an example in this document. Deviation from this table generates a communication error in STATUS_CML register.

Byte	Description
0	Instantaneous power accumulator low byte
1	Instantaneous power accumulator high byte
2	Accumulator rollover counter
3	Sample count low byte
4	Sample count mid byte
5	Sample count high byte

The two-byte accumulator holds the cumulative sum of the BCM instantaneous low-voltage-side output power computed by multiplying the LO-side output voltage by the LO-side output current at a regular sampling interval. The two bytes of the accumulator are encoded in DIRECT FORMAT as defined in the PMBus® Specification v1.3. The accumulator rollover counter is one byte and increments each time the two-byte accumulator overflows. The sample count (three bytes) increments each time the LO-side output power is sampled and summed into the accumulator. Overflow events of the accumulator rollover-counter byte and sample-count bytes must be accounted for by the Host for correct data interpretation.

Average output power is computed by the Host from two readings of the READ_EOUT command. Each read of the READ_EOUT command requires that the total LO-side output energy count be calculated based on the returned power accumulator reading and the rollover count.

$$Energy\_Count = Rollover\_Count \bullet Maximum\_Direct\_Format\_Value(m,b,R) + Accumulator\_Value$$

Where:

The maximum DIRECT FORMAT value is a function of the values of m, b and R:

$$Maximum\_Direct\_Format\_Value(m,b,R) = \frac{1}{m} \bullet \left(Y_{MAX} \bullet 10^{-R} - b\right)$$

and

$$Y_{MAX} = 2^{15} - 1 = 32{,}767$$

The average LO-side output power can be computed based on the above calculations performed on each set of READ_EOUT data and the returned sample count.

$$Average\_Power = \frac{Current\_Energy\_Count - Last\_Energy\_Count}{Current\_Sample\_Count - Last\_Sample\_Count}\ (W)$$

Information provided by this command is independent of the BCM specific averaging period and sampling frequency. The sample count update rate is 102400µs.

Example

Where:

V_{LO} = 48V
I_{LO} = 65A

Last-read EOUT_COMMAND data:

Accumulator count = 28080
Rollover count = 0
Sample count = 9

Calculations on last read:

$$Energy\_Count = 28080 + \left(0 \bullet 32767\right) = 28080$$

Current-read EOUT_COMMAND data:

Accumulator count = 2868
Rollover count = 36
Sample count = 379

Calculations on current read:

$$Energy\_Count = 2868 + \left(36 \bullet 32767\right) = 1182480$$

Average Power Calculation:

$$Average\_Power = \frac{\left(1182480 - 28080\right)}{\left(379 - 9\right)} = 3120W$$

READ_VOUT Command (8Bh)

Returns the BCM's low-side voltage V_{LO} in the following format:

$$V_{OUT\_ACTUAL} = V_{OUT\_REPORTED} \bullet 10^{-2}(V)$$

READ_IOUT Command (8Ch)

Returns the BCM's low-side current I_{LO} in the following format:

$$I_{OUT\_ACTUAL} = I_{OUT\_REPORTED} \bullet 10^{-2}(A)$$

READ_TEMPERATURE_1 Command (8Dh)

Returns the BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (°C)$$

READ_POUT Command (96h)

Returns the BCM's low-side power P_{LO} in the following format:

$$P_{OUT\_ACTUAL} = P_{OUT\_REPORTED}\ (W)$$

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

These values are set by the factory and indicate the device input-side/output-side voltage and output-side current range and output-side power capacity.

These commands report the rated BCM input-side (HI) voltage minimum and maximum in volts, output-side (LO) voltage minimum and maximum in volts, output-side (LO) current maximum in amperes and output-side (LO) power maximum in watts.

READ/WRITE USER DATA_00 (B0h) and READ/WRITE USER DATA_01 (B1h) Commands

A direct communication to the BCM controller for access of User Data by the B0h – B3h commands is supported.

The supported commands B0h and B1h allow write and read of 28 bytes of data to and from non-volatile memory when the BCM is disabled, as defined in the following tables. A write stores a fixed length data payload of 28 bytes in EEPROM. A read will return the same 28 byte fixed length payload. The user shall use the BLOCK READ/WRITE command structure specified in SMBus™ specification also listed as an example in this document. Deviation from this table generates a communication error in STATUS_CML register.

READ/WRITE USER DATA_00 Command (B0h)

Byte	Description	Values
0	See table below	Action Description Byte
1:28	Data (28 user-programmable bytes)	Data_1, Data_2, ..., Data_28

Byte	Values	Description
0	0	Reserved
	1	**Write:** Write the 28-byte password protected user data
	2	Reserved
	3	**Set WR Protection:** Byte 1:28 – 0xff **Remove WR Protection:** Byte 1:28 – 0x00

READ/WRITE USER DATA_01 Command (B1h)

Byte	Description	Values
0	Write	1 – Write
1:28	Data (28 user-programmable bytes)	Data_1, Data_2, ..., Data_28

The supported commands B2h and B3h allow write and read of 255 bytes of data to and from non-volatile memory when the BCM is disabled, as defined in the following tables. A write stores a fixed length data payload of 255 bytes in EEPROM. A read will return the same 255 byte fixed length payload. The user shall use the BLOCK READ/WRITE command structure specified in SMBus™ specification also listed as an example in this document. Deviation from this table generates a communication error in STATUS_CML register.

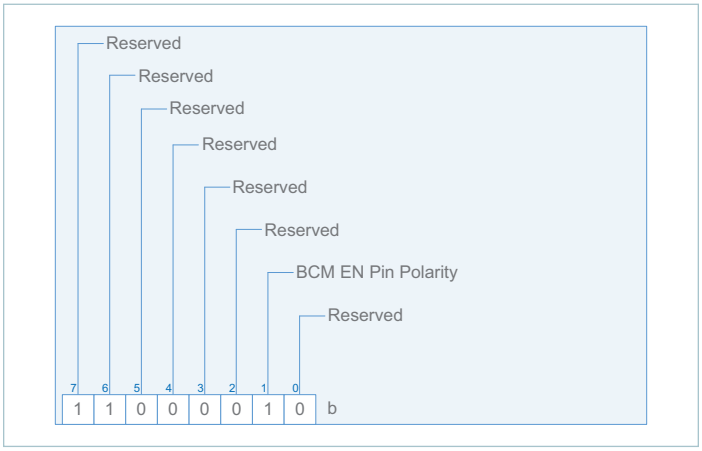
READ/WRITE USER DATA_02 Command (B2h)

Byte	Description	Values
0:254	Data (255 user programmable bytes)	Data_0, Data_1, ..., Data_254

READ/WRITE USER DATA_03 Command (B3h)

Byte	Description	Values
0:254	Data (255 user programmable bytes)	Data_0, Data_1, ..., Data_254

BCM_EN_POLARITY Command (D0h)



The value of this register is set in non-volatile memory and can only be written when the BCM is disabled. This command defines the polarity of the EN pin. If BCM_EN_POLARITY is set, the BCM will start up once V_{HI} is greater than the undervoltage threshold. The BCM EN pin is internally pulled up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull-down is then required. In this case, applying V_{HI} greater than the undervoltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

Returns the BCM's K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16}(V/V)$$

The K factor is defined in the BCM to represent the ratio of the transformer winding and hence is equal to V_{OUT} / V_{IN}.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the BCM.

Section	Description	Response to Host		STATUS_BYTE	STATUS_CML			Notes
		NACK	FFh	CML	Other Fault	Unsupported Data	PEC Failed	
10.8.1	Corrupted data						X	
10.8.2	Sending too few bits			X	X			
10.8.3	Reading too few bits			X	X			
10.8.4	Host sends or reads too few bytes			X	X			
10.8.5	Host sends too many bytes	X		X				
10.8.6	Reading too many bytes		X	X	X			
10.8.7	Device busy	X	X					Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

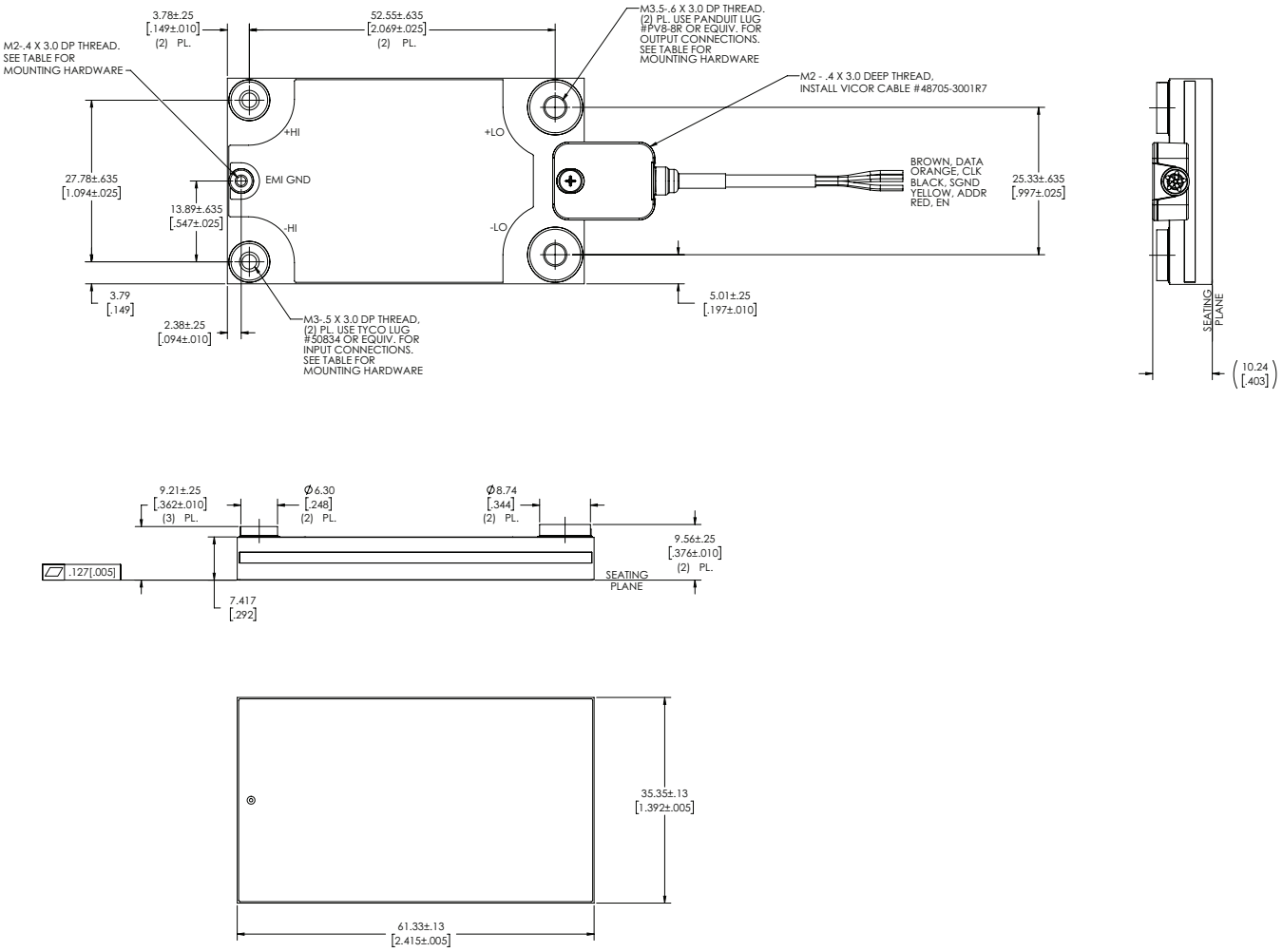
Data Content Faults Implementation

This section describes data content fault as implemented in the BCM.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NACK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly set read bit in the address byte	X	X	X			No response
10.9.2	Unsupported command code	X	X		X		
10.9.3	Invalid or unsupported data		X			X	
10.9.4	Data out of range		X			X	
10.9.5	Reserved bits						No response; not a fault

Mechanical Drawing

6135 BCM TC7_5
(Reference DWG# 48382 rev 2)



NOTES:

1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM / [INCH]
2- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

Fastener Assemblies Per BCM for use with recommended ring lugs (Input Tyco 50834, output Panduit PV8-8R)					
Fastener Size	Qty	Screw	Belleville	Flat	Torque
M2 screw/Belleville/flat	1	M2 x 4 (McMaster 92000A011)	Maryland Prec. Spring SSP-52203	Vicor 43985	0.8 in-lb
M3 screw/Belleville/flat	2	M3 x 4 (McMaster 92000A113)	Vicor 43440	Vicor 43985	6 in-lb
M3.5 screw/Belleville/flat	2	M3.5 x 5 (McMaster 92000A150)	Vicor 43441	McMaster 98017A615	8.5 in-lb

Revision History

Revision	Date	Description	Page Number(s)
1.0	06/08/21	Initial release	n/a

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

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