BCM53101M

Six-/Seven-Port Managed 10/100 Ehternet Switches

GENERAL DESCRIPTION

The Broadcom® BCM53101M is a highly integrated, cost-effective seven-port 10/100BASE-T/TX managed switch. The switch design is based on the field-proven, industry-leading ROBO architecture. This device combines all the functions of a high-speed switch system including packet buffers, PHY transceivers, media access controllers (MACs), address management, port-based rate control, and a non-blocking switch fabric into a single 65 nm CMOS device. Designed to be fully compliant with the IEEE 802.3 and IEEE 802.3x specifications, including the MAC-control PAUSE frame, the BCM53101M provides compatibility with all industry-standard Ethernet and fast Ethernet devices.

The BCM53101M has a rich feature set suitable for applications not only for next-generation cable, xDSL and EPON/GPON gateways, but also for SOHO/SMB routers. It is also specifically designed for next generation set-top boxes.

The BCM53101M contains five full-duplex 10/100 BASE-TX Ethernet transceivers. In addition, the BCM53101M has one RGMII/MII/RvMII/RMII/TMII/RvTMII interface for the CPU or a router chip, providing flexible 10/100/1000 Mbps connectivity. There is another MII/RvMII/RMII/TMII/RvTMII interface for the WAN port or configurable as the dual IMP port.

The BCM53101M provides 70+ on-chip MIB counters to collect receive and transmit statistics for each port.

The BCM53101M is available in industrial temperature (I-Temp) and commercial temperature (C-Temp) rated packages.

FEATURES

- Six 10/100 media access controllers
- One 10/100/1000 media access controller
- Five-port 10/100 transceivers for TX
- One RGMII/MII/RvMII/RMII/TMII/RvTMII interface for an inband management port (IMP) for connection to a CPU/management entity without PHY
- One MII/RvMII/RMII/TMII/RvTMII interface for a WAN port
- Dual IMP ports support, WAN port to be IMP port-capable
- IEEE 802.1p, MAC Port, TOS, and DiffServ QoS for four queues, plus two time-sensitive queues
- Port-based VLAN
- VLAN-based ingress rate limit: 64 kbps granularity
- IEEE 802.1Q-based VLAN with 4K entries
- Port-based ingress rate control and egress rate shaping with 64 kbps granularity
- MAC-based trunking with automatic link failover
- Protected port
- Broadcast storm control - per port based
- Port mirroring and storm suppression
- BroadSync HD
- Timestamp tagging at MAC interface
- Time-aware egress scheduler
- IGMP Snooping, MLD snooping support
- Spanning tree support (802.1D/1s/1w)
  - Multiple Spanning trees–up to eight
- Double-tagging tolerant
- IEEE 802.3as support
- IEEE 802.3x programmable per port flow control and back pressure
- IEEE 802.1x support for secure user authentication
- EEPROM, MDC/MDIO, and SPI interface
- Parallel/serial LED support
- 2K entry MAC address table with automatic learning and aging
- 64 KB packet buffer
- 128 multicast group support
- Maximum frame size support up to 9720 bytes
- 1.2V for core and 2.5V/3.3V for I/O
- Trap reserved multicast MAC addresses to IMP port
- JTAG support
- 132-pin DRQFN package (10 mm x 10 mm)

53101M-DS05-R

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December 2, 2011

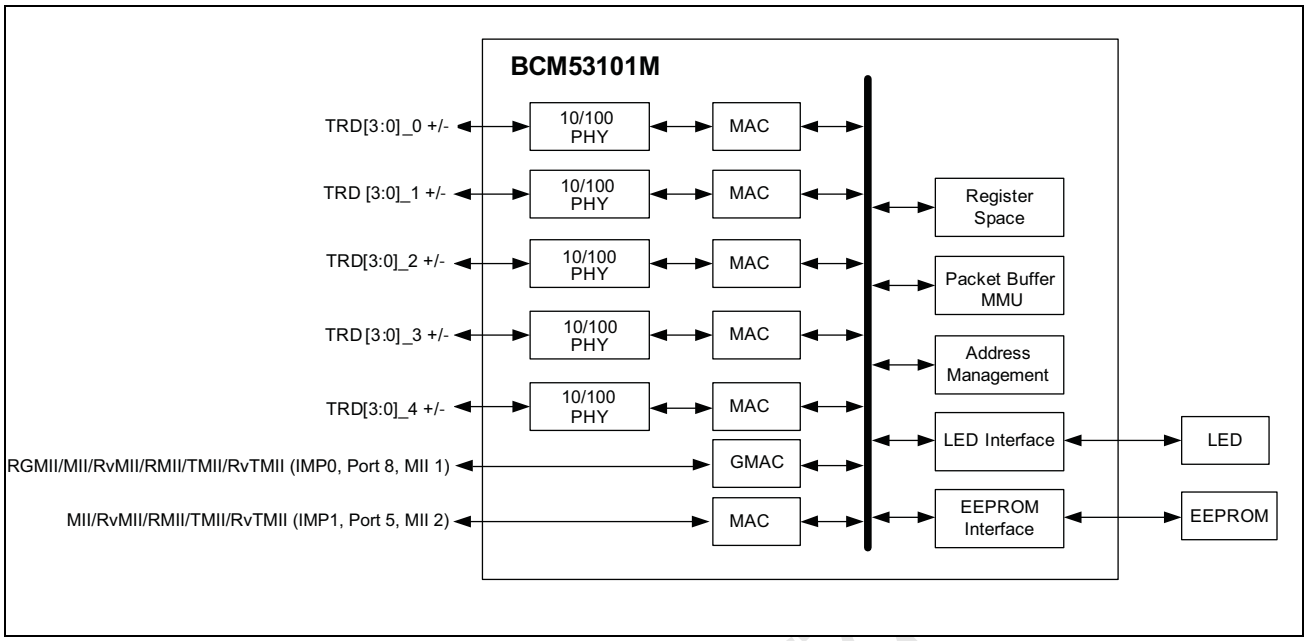

Figure 1: BCM53101M Functional Block Diagram

Revision History

Revision: 53101M-DS05-R

Date: December 2, 2011

Note: Cross-reference page numbers are valid for this revision of the document only.

Updated:		
• Spanning tree support available on page 1	Added (802.1D/1s/1w)	Feature
• Figure 1: "BCM53101M Functional Block Diagram," on page 2	Added an arrow to connect	No action required
• "Overview" on page 30	Corrected edit error to 2K unicast address	No action required
• "SCK: Serial Clock" on page 85	Changed max frequency to 12.5 MHz	No action required
• "Pseudo-PHY" on page 103	Added a warning note	No action required
• Figure 45: "LED Interface Register Structure Diagram," on page 111	Corrected edit error	No action required
• Table 29: "Signal Description," on page 114	Corrected edit error	No action required
• Table 70: "Pause Frame Detection Control Register (Page 00h: Address 80h)," on page 152	Corrected edit error	No action required
• Table 209: "Port Suppressed Packet Drop Count Register (Page 41h: Address 50h–73h)," on page 243	Corrected edit error	No action required
• Table 212: "IMP Port Egress Rate Control Configuration Registers Bit Definitions," on page 244	Corrected edit error	No action required
• Table 59: "BCM53101M Mechanical Drawing," on page 279	Updated dimensions D2 and E2	Update thermal pad dimensions

Revision: 53101M-DS04-R

Date: August 12, 2010

Updated:		
• "Overview" on page 34	Changed maximum frame size to 9720	New feature available
• Bulleted list in "Address Learning" on page 55	Corrected editing errors	No action required
• Notes under "Reserved Multicast Addresses" on page 58	Corrected editing errors	No action required
• Steps in "100BASE-FX Fiber Mode" on page 71	Clarified register/page information and removed final step	Suggest a review of the EFX programming setup
• "SPI-Compatible Programming Interface" on page 89	Max operating speed from 2 MHz to 12.5 MHz	New feature available

• Figure 48: “LED Interface Block Diagram,” on page 116	4A changed to 4C; 4C changed to 4A	Suggest a review of the schematics
• Table 43: “LED Function 0 Control Register (Page 00h: Address 10h–11h),” on page 146	Renamed bit 15 function description to BroadSync HD	No action required
• Table 44: “LED Function 1 Control Register (Page 00h: Address 12h–13h),” on page 147	Renamed bit 15 function description to BroadSync HD	No action required
• Table 113: “Aging Time Control Register (Page 02h: Address 06h–09h),” on page 184	0 value description update for bit 20	Typo correction
• Table 250: “TC_To_CoS Mapping Register (Page 30h: Address 62h–63h),” on page 268	Corrected editing errors bits 15:14	No action required
• Table 318: “BroadSync HD Timestamp Report Control Register (Page 90h, Address 14h–17h),” on page 310	Bit 5:0 description and default update	Suggest a review of the timestamp control programming
• Table 338: “Absolute Maximum Ratings,” on page 318	Added T_J symbol	Suggest a review of the thermal characteristic of the system design
• Table 340: “IDD for 10BASE-T (A0 Silicon),” on page 319	Added note for 2.5V center tap current	Center tap current for B0 silicon is slightly higher. Suggest a review of the power budget if B0 is used instead of the A0 silicon.
• Table 341: “IDD for 100BASE-TX (A0 Silicon),” on page 320	Added note for 2.5V center tap current	Center tap current for B0 silicon is slightly higher. Suggest a review of the power budget if B0 is used instead of the A0 silicon.
• Table 352: “Reverse TMII Input Timing,” on page 328	Added “10 (Port 8)” to Min value to rising setup time	New feature available
Added:		
• Table 281: “Page 40h Jumbo Frame Control Registers,” on page 288	None	New feature available
Revision: 53101M-DS03-R Date: March 12, 2010		
Updated:		
• Broadcom header (see “Broadcom Header Control Register (Page 02h: Address 03h)” on page 180	None to existing design	Be aware of new option when coding for new design
• “Broadcom Tag Format for Egress Packet Transfer” on page 73	Management CPU programming	Suggest a review of the management CPU programming setup
• “Broadcom Tag Format for Ingress Packet Transfer” on page 74		
• “Dual-Input Configuration/LED Output Function” on page 116	Schematics design	Suggest a review of the schematics

• Current consumption (see “Electrical Characteristics” on page 314)	Power supply requirement	Suggest a review of the schematics
• RESET rise time maximum in Table 344: “Reset and Clock Timing,” on page 319 (t105) • “MDC/MDIO Interface” on page 105 • MDIO input setup/hold time minimum in Table 362: “MDC/MDIO Timing (Master Mode),” on page 331 (t403/t404) • SCK high/low time minimum in Table 364: “SPI Timings,” on page 333 (t602) • “EEPROM Timing” on page 334 (t701, t702, t703, t704, t705, t706)	Schematics design	Suggest a review of related timing
• Figure 68: “BCM53101XCT Mechanical Drawing,” on page 336	Layout	Suggest a review of the layout file
Added:		
• “Power-Saving Modes” on page 61	None	Suggest a review of the initial configuration codes
• Enhanced FX support (B0 silicon)	None	New feature option available
• IMP port (port 8) TMII/RvTMII support	None	New feature option available

53101M-DS02-R	09/29/09	**Updated:** • General Description on cover page. • "Overview" on page 1. • "Programming the VLAN Table" on page 9. • "Rate Control" on page 11. • "Media Access Controller" on page 26. • "Frame Management" on page 30. • "In-Band Management Port" on page 30. • Table 19: "Signal Description," on page 73. • Table 39: "Switch Control Register (Page 00h: Address 20h)," on page 95. • Table 54, "IMP RGMII Control Register (Page 00h: Address 60h)," on page 104. • Table 76: "Broadcom Header Control Register (Page 02h: Address 03h)," on page 112. • Table 159: "TX Queue Control Register (Page 30h: Address 80h)," on page 168. • Table 196: "Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)," on page 192. • Table 219: "ResE Max AV Packet Size Register (Page 90h, Address 04h-05h)," on page 202. • Figure 55, "RGMII Input Timing (Normal Mode)," on page 221. • Figure 56, "RGMII Input Timing (Delayed Mode)," on page 222. • Table 220: "ResE Time Base Register (Page 90h, Address 10h-13h)," on page 202. • Table 223: "ResE Slot Adjustment Register (Page 90h, Address 1Ch-1Fh)," on page 204. • Table 225: "ResE Class 5 Bandwidth Control Register (Page 90h, Address 30h-39h)," on page 205. • Table 227: "ResE Class 4 Bandwidth Control Register (Page 90h, Address 60h-69h)," on page 205. **Added:** • Section 9: "Electrical Characteristics," on page 210.
53101M-DS01-R	07/31/09	**Updated:** • General Description • "Overview" on page 1. • Table 3: "Bucket Bit Rate," on page 12. • Table 8: "Behavior for Reserved Multicast Addresses," on page 23. • Section 5: "Hardware Signal Definition Table," on page 73. • Section 6: "Pin Assignment," on page 80 with new pin assignment. **Added:** • Section 8: "Register Definitions," on page 84. • Section 10: "Timing Characteristics," on page 212.
53101M-DS00-R	05/08/09	Initial release

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the BCM53101E, BCM53101M, and BCM53101P.

This document is for design engineers interested in integrating the BCM53101E, BCM53101M, or BCM53101P into their hardware designs and others who need specific data about the physical characteristics and operation of the devices.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

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The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

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In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

The BCM53101M is a single-chip, seven-port Gigabit/Fast Ethernet switch device that provides the following features:

- One Gigabit Media Access Controller (GMAC)
- Six full-duplex capable Media Access Controllers (MACs)
- Five ports with 10/100BASE-TX-compatible transceivers
- One RGMII/MII/RvMII/RMII/TMII/RvTMII port for PHY-less connection to the management agent
- One MII/RvMII/RMII/TMII/RVTMII interface for WAN port
- An integrated Motorola® SPI-compatible interface
- High performance, integrated packet buffer memory
- An address resolution engine
- A set of Management Information Base (MIB) statistics registers

The integrated 10BASE-T/100BASE-TX transceivers perform all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT-5 twisted pair cable, and 10BASE-T full-duplex or half-duplex Ethernet on CAT-3, -4, or -5 cable.

The device provides six internal MACs. Each MAC is dual-speed and both half- and full-duplex capable. The GMAC supports full-duplex and half-duplex modes for 10 Mbps and 100 Mbps, and full-duplex for 1000 Mbps. Flow control is provided in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is provided. The MAC is IEEE 802.3-compliant and supports a maximum frame size of 9720 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 2K unicast addresses. Addresses are added to the table after receiving an error-free packet.

The MIB statistics registers collect receive and transmit statistics for each port and provide direct hardware support for the Ether-like MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface Port by an external microcontroller.

Audience

This document is for designers interested in integrating the BCM53101M switches into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM53101M switches.

Data Sheet Information

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active low (such as $\overline{CE}$).
- In register and signal descriptions, [*n*:*m*] indicates a range from bit *n* to bit *m* (such as [7:0] indicates bits 7 through 0, inclusive).
- The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage (for example, 1 KB means 1,024 bytes, 100 Mbps [referring to Fast Ethernet speed] means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).

Section 2: Features and Operation

Overview

The BCM53101M switches include the following features:

Quality of Service

The Quality of Service (QoS) feature provides up to six internal queues per port to support six different traffic classes (TC). The traffic classes can be programmed so that higher-priority TC in the switch experiences less delay than lower-priority TC under congested conditions. This can be important in minimizing latency for delay-sensitive traffic. The BCM53101M switches can assign the packet to one of the six egress transmit queues according to information in the following sections:

- "Port-Based QoS" on page 34 (ingress port ID)
- "IEEE 802.1p QoS" on page 34
- "MACDA-Based QoS" on page 34
- "TOS/DSCP QoS" on page 35

The "TC Decision Tree" on page 35 decides which priority system is used based on three programmable register bits detailed in Table 1: "TC Decision Tree Summary," on page 35. The corresponding traffic class is then assigned to one of the six queues on a port-by-port basis.

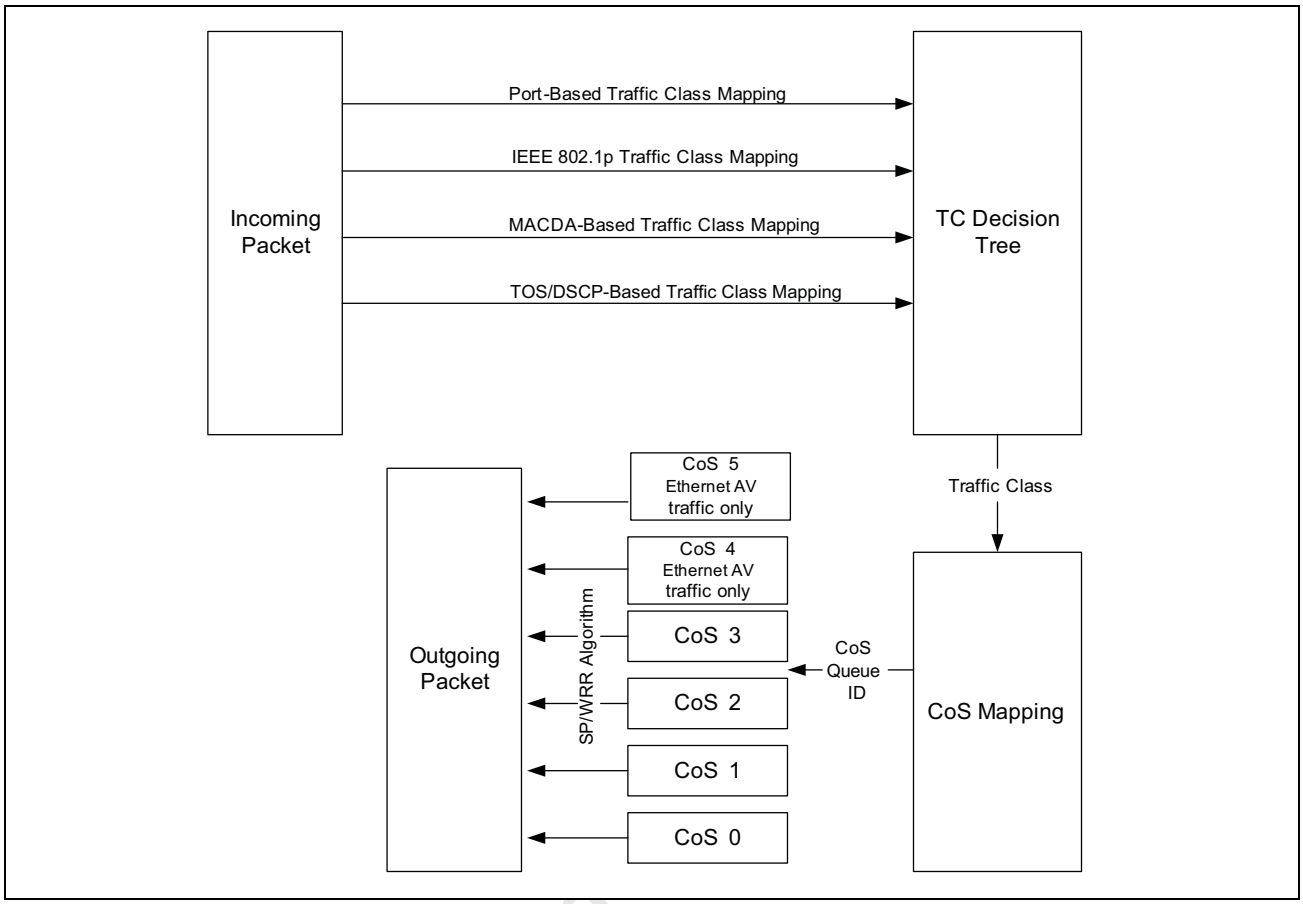


Figure 2: QoS Program Flow

Egress Transmit Queues

Each Ethernet egress port has six transmit queues (CoS 0–CoS 5). The CoS 4 and CoS 5 queues are dedicated to BroadSync™ HD traffic only and cannot be shared with other traffic. Each CoS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. Every Ethernet (ingress) port has its own set of counters to measure the buffer occupancy and the arrival rate related to the traffic received from the port.

The IMP (egress) port serves four queues (CoS 0–CoS 3) and the traffic generated by the Local Management Packet Generator, which generates management report messages back to the CPU such as the Time Sync TX timestamp packets.

Each CoS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. The IMP (ingress) port also has its own set of counters to measure the buffer occupancy and the arrival rated to the traffic received from the port. The IMP port should be used only if it is configured as a regular Ethernet port.

All incoming frames are assigned to an egress transmit queue depending on their assigned TC. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher TC queues being given greater access than the lower TC queues. Queue 0 is the lowest-TC queue.

The CoS 0–CoS 3 queues are dedicated to non-BroadSync traffic only and as programmed in the "TX Queue Control Register (Page 30h: Address 80h)" on page 222. The BCM53101M uses Strict Priority (SP) and the Weighted Round Robin (WRR) algorithm for queue scheduling on CoS 0–CoS 3. The scheduling is configurable in the TX Queue Control register as one of the following combinations of SP and WRR: 4SP and 4WRR, 1SP and 3WRR, 2SP and 2WRR. The WRR algorithm weights for each queue can be programmed using the "TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)" on page 223.

Port-Based QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with the TC configured for the corresponding port. The mapping mechanism is globally enabled/disabled by programming the "QoS Global Control Register (Page 30h: Address 00h)" on page 216. The mapping entry is also per-port configured using the "Port N (N = 0–5, 8) PCP_To_TC Map Register (Page 30h: Address 10h–2Bh)" on page 217. When disabled, the TC that results from this mapping is 000.

IEEE 802.1p QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC-configured for the corresponding IEEE 802.1p Priority Code Point (PCP). The mapping mechanism is per-port enabled/disabled using the "QoS IEEE 802.1p Enable Register (Page 30h: Address 04h–05h)" on page 217. The mapping entries are per-port configured using the "Port N (N = 0–5, 8) PCP_To_TC Map Register (Page 30h: Address 10h–2Bh)" on page 217. When disabled or if the incoming packet is not tagged, the TC that results from this mapping is 000.

MACDA-Based QoS

MACDA-Based QoS is enabled when the IEEE 802.1p QoS is disabled using the 802_1P_EN bit in the "QoS IEEE 802.1p Enable Register (Page 30h: Address 04h–05h)" on page 217. When using MACDA-based QoS, the destination address and VLAN ID are used to index the ARL table as described in "Address Management" on page 50. The matching ARL entry contains a 3-bit TC field as shown in Table 5 on page 52. These bits set the MACDA-based TC for the frame. The MACDA-based TC is assigned to the TC bits depending upon the result shown in Table 1 on page 35. The TC for the frame is mapped to one of the egress transmit queues base on the ingress port using the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221. The TC bits for a learned ARL entry default to 0. To change the default, an ARL entry is written to the ARL table as described in the "Writing an ARL Entry" on page 56. For more information about the egress transmit queues, see "Egress Transmit Queues" on page 33.

TOS/DSCP QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC configured for the corresponding IP TOS/DSCP. The mapping mechanism is per-port enabled/disabled using the "QoS DiffServ Enable Register (Page 30h: Address 06h–07h)" on page 217. The mapping entries are globally configured using the "DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)" on page 218 through the "DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)" on page 220. When disabled or the incoming packet is not of the IPv4/v6 type, the TC that results from this mapping is 000.

TC Decision Tree

Non-BroadSync™ Frame

The TC decision tree determines which priority system is assigned to TC-mapping bits for the given frame. As summarized above, the TC bits for the frame can be determined according to the ingress port-based TC, IEEE 802.1p TC, MACDA-based TC, DiffServ TC, or MACSA-based TC information. The decision on which TC mapping to use is based on the Port_QoS_En bit and the QoS_Layer_Sel bits of the "QoS Global Control Register (Page 30h: Address 00h)" on page 216. Table 1 on page 35 summarizes how these programmable bits affect the derived TC. The DiffServ and IEEE 802.1p QoS TC are only available if the respective QoS is enabled and the received packet has the appropriate tagging.

Table 1: TC Decision Tree Summary

Port_QoS_En	*QoS_Layer_Sel*	*Value of TC Bits*
0	00	IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping
0	01	DiffServ TC mapping if available; otherwise, TC = 000
0	10	DiffServ TC mapping for IP frame; otherwise, IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping
0	11	Highest available TC of the following: IEEE 802.1p TC mapping, DiffServ TC mapping, MACDA-based TC mapping, or MACSA-based TC mapping
1	00	MACSA-based TC mapping if available; otherwise, port-based TC mapping
1	01	MACSA-based TC mapping if available; otherwise, port-based TC mapping
1	10	MACSA-based TC mapping if available; otherwise, port-based TC mapping
1	11	Highest available TC of the following: Port-based TC mapping, MACSA-based TC mapping, IEEE 802.1p TC mapping, DiffServ TC mapping, or MACDA-based TC mapping

For the packets received from an Ethernet port when the ACL rules generate a TC change request, the ACL-derived TC overwrites the priority generated by the Table 1 TC-mapping mechanisms.

BroadSync HD Frame

For the BroadSync HD packet from an Ethernet port, the TC is determined directly from the explicit IEEE 802.1Q/P tag carried in the BroadSync HD packets (BroadSync HD packets are expected to be always tagged), which is independent of Table 1 TC mapping (including ACL-based mapping).

The conditions used to decided whether an incoming packet is BroadSync HD are as follows:

- The port from which the packet is received is configured as AV-enabled.
- The packet received is either VLAN tagged or priority tagged, with PCP = 4 or 5.
- The MACDA is of multicast type and can be found through ARL table search.

Note: BroadSync HD cannot be received from the IMP port.

Queuing Class (CoS) Determination

The BCM53101M supports CoS mapping using the following mapping mechanisms:

- TC-to-CoS mapping: The queuing class to forward a packet to an Ethernet port is mapped from the TC determined for the packet. The mapping entries are globally configured.
- BroadSync HD-to-CoS mapping: The queuing class to forward a BroadSync HD packet to an AV-enabled Ethernet port is mapped from the PCP carried by the packet. PCP5 is mapped to CoS 5 and PCP4 is mapped to CoS 4.
- CPU-to-CoS mapping: The queuing class to forward a packet to the external CPU through the IMP port is determined based on the reasons to forward (copy or trap) the packet to the CPU. The mapping entries are globally configured.

Note: When the BCM53101M is configured in the aggregation mode where the IMP operates as the uplink port to the upstream network processor, the CoS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU and the CoS is decided based on the reasons for forwarding the packet to the CPU.

Table 2 shows the reasons for forwarding a packet to the CPU.

Table 2: Reasons to Forward a Packet to the CPU

ToCPU Reason	*Description*	*ToCPU CoS*
Mirroring	Packet is forwarded (copied) through the IMP port because it needs to be mirrored to the CPU as the capturing device.	0
SA Learning	Packet is forwarded (copied) through the IMP port because its SA needs to be learned by the CPU.	0
Switching/Flooding	Packet is forwarded through the IMP port either because the CPU is one of the intended destination hosts of the packet or because the switch makes the flooding decision to reach all potential destinations.	0

Table 2: Reasons to Forward a Packet to the CPU (Cont.)

ToCPU Reason	*Description*	*ToCPU CoS*
Protocol Termination	Packet is forwarded (trapped) through the IMP port because it implies an IEEE 802.1™ defined L2 protocol that needs to be terminated by the CPU.	0
Protocol Snooping	Packet is forwarded (copied) through the IMP port because it implies an L3 or application level protocol that needs to be monitored by the CPU for network security or operation efficiency.	0
Exception Processing	Packet is forwarded (trapped) through the IMP port for some special processing even though the CPU is not the intended destination.	0

The ToCPU CoS values listed in Table 2 are the default settings and are configurable. In order to prevent out of order delivery of the same packet flow to the CPU, the CoS for the mirroring and SA learning reasons must be programmed with a value that is lower than or equal to the value of the other reasons.

A packet could be forwarded to the CPU for more than one reason, therefore, the CoS selection is based on the highest CoS values among all the reasons for the packet.

Port-Based VLAN

The port-based Virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per-port basis. Data switching outside of the port's private domain is not allowed. The BCM53101M provides flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to nonprivate domain ports. The private domain ports are selected for each ingress port using the Port-Based VLAN Control register. For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame will be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the nonprivate domain ports. The frame is only forwarded to those ports that meet both the ARL table criteria and the port-based VLAN criteria.

IEEE 802.1Q VLAN

The BCM53101M supports IEEE 802.1Q VLAN and up to approximately 4000 VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM53101M autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN and MAC L2 lookups.

IEEE 802.1Q VLAN Table Organization

Each VLAN table entry consists of a VLAN ID, an Untag map, and a Forward map. The Untag map controls whether the egress packet is tagged or untagged. The Forward map defines the membership within a VLAN domain. The Untag map and Forward map include a bit-wise representation of all the ports. Also:

- The FWD_MODE indicates whether the packet forwarding should be based on VLAN membership or on ARL flow.
- Policing_EN enables the VLAN rate-limiting function.
- Policing_ID controls whether Bucket 0 or Bucket 1 is used in the VLAN rate-liming function.

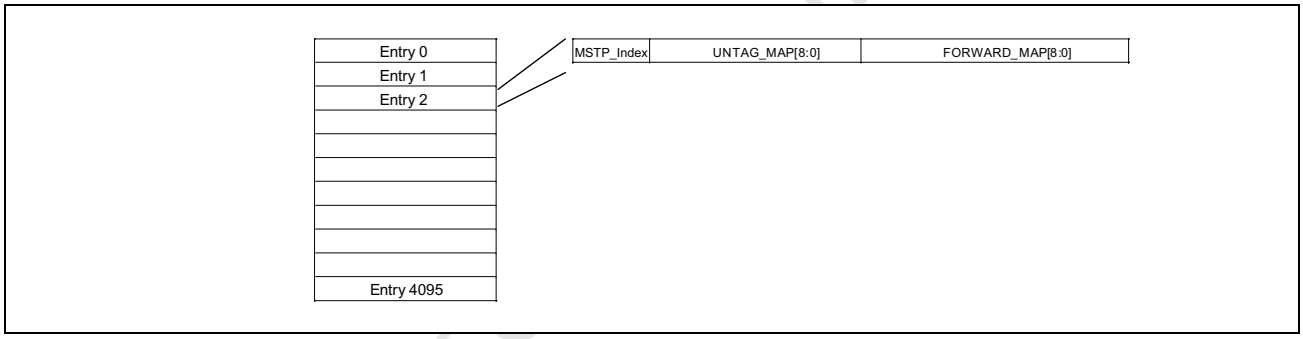


Figure 3: VLAN Table Organization

Note: When the IEEE 802.1Q feature is enabled, frames sent from the CPU must be tagged. If the MII port is configured as a management port, the tag is not stripped even if the untag bit is set.

Programming the VLAN Table

The IEEE 802.1Q VLAN feature can be enabled by writing to the Enable IEEE 802.1Q bit in the "Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 227. The default priority and VID can be assigned to each port in the "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)" on page 234. These are necessary when tagging a previously untagged frame. The Hashing algorithm uses either [VID, MAC] or [MAC] for the ARL index key, depending on the VLAN Learning Mode bits in the "Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 227. If both the VID and MAC address are used, a single MAC address is able to be a member of multiple VLANs simultaneously.

The VLAN table can be written using the following steps:

1. Use the "VLAN Table Entry Register (Page 05h: Address 83h–86h)" on page 186 to define the ports that are part of the VLAN group and the ports that should be untagged.
2. Use the "VLAN Table Address Index Register (Page 05h: Address 81h–82h)" on page 186 to define the VLAN ID of the VLAN group.

Note: FFFh is not a valid VID number.

3. Set bits [1:0] = 00 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" on page 186 to indicate a write operation.
4. Set bit 7 of the VLAN Table Read/Write/Clear Control register to 1, starting the write operation. This bit returns to 0 when the write is complete.

The VLAN table can be read using the following steps:

1. Use the "VLAN Table Address Index Register (Page 05h: Address 81h–82h)" on page 186 to define from which VLAN group to read the data.
2. Set bits [1:0] = 01 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" on page 186 to indicate a read operation.
3. Set bit 7 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" to 1 to start the read operation. This bit returns to 0 when the read is complete.
4. Read the VLAN Table Entry register to obtain the VLAN table entry information.

Maximum Frame Size Support

The BCM53101M can receive and transmit frames of extended length on all ports. The maximum frame size support is configurable by register and supports up to a total length of 9720 bytes.

Port Trunking/Aggregation

The BCM53101M supports MAC-based trunking. The trunking feature allows up to four ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM53101M allows up to two trunk groups. Trunks are composed of predetermined ports and can be enabled using the Trunking Group 0 register. Ports within a trunk group must be of the same linked speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other port within the trunk automatically assumes all traffic designated for the trunk, thus allowing for a seamless and automatic redundancy scheme. This hashing function can be performed on either the DA, SA, or DA/SA, depending on the Trunk Hash Selector bit of MAC Trunking Control register.

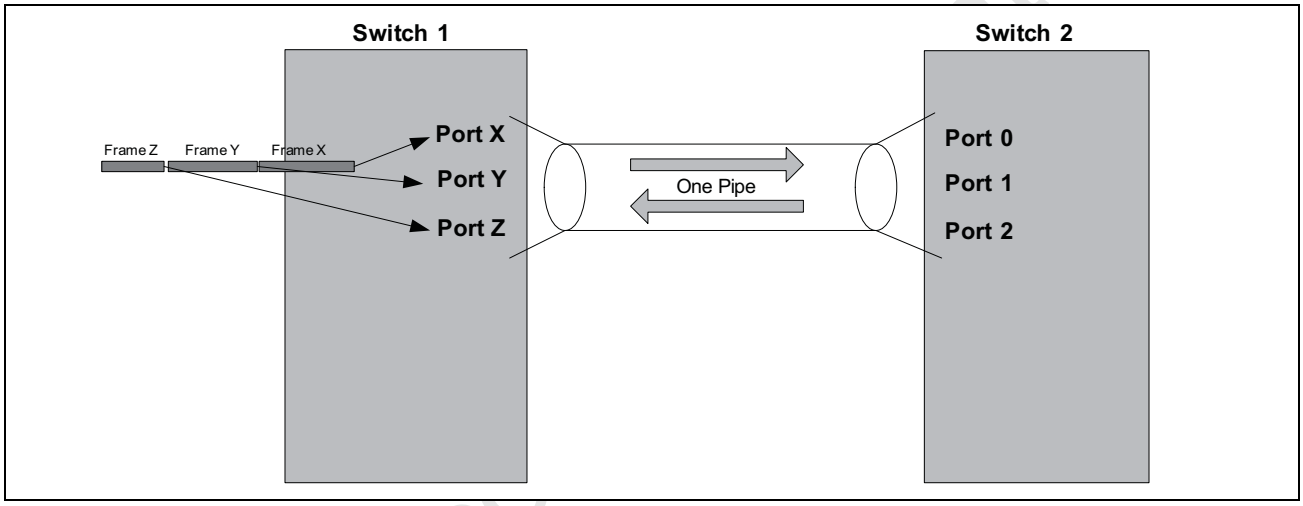


Figure 4: Trunking

WAN Port

The BCM53101M offers a programmable WAN port feature: It has a WAN Port Select register (page 00h, address 26h). When a port is selected as a WAN port, all that port's traffic is forwarded to the CPU port only. The non-WAN port traffic from all other local ports does not flood to the WAN port. To avoid CPU-originated Multicast, Broadcast, and DLF packets from flooding to the WAN port, the BCM53101M limits the CPU traffic to the WAN port by setting the EN_MAN_TO_WAN bit in the WAN Port Select register. When the EN_MAN_TO_WAN bit is 0, only egress-directed frames (from the CPU) are forwarded to the WAN port.

Rate Control

Ingress Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types and the policing of VLAN traffic. If the rates of these packet types or the VLAN traffic exceeds the programmable maximum rate, the packets are dropped. Broadcast Storm Suppression can be activated using the "Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243.

The broadcast storm suppression mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 5). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types or the VLAN traffic is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the bucket bit rate (the rate at which credit is added to the bucket). At this point, excess packets are either dropped or deterred using flow control, depending on the Suppression Drop mode in the Ingress Rate Control Configuration register.

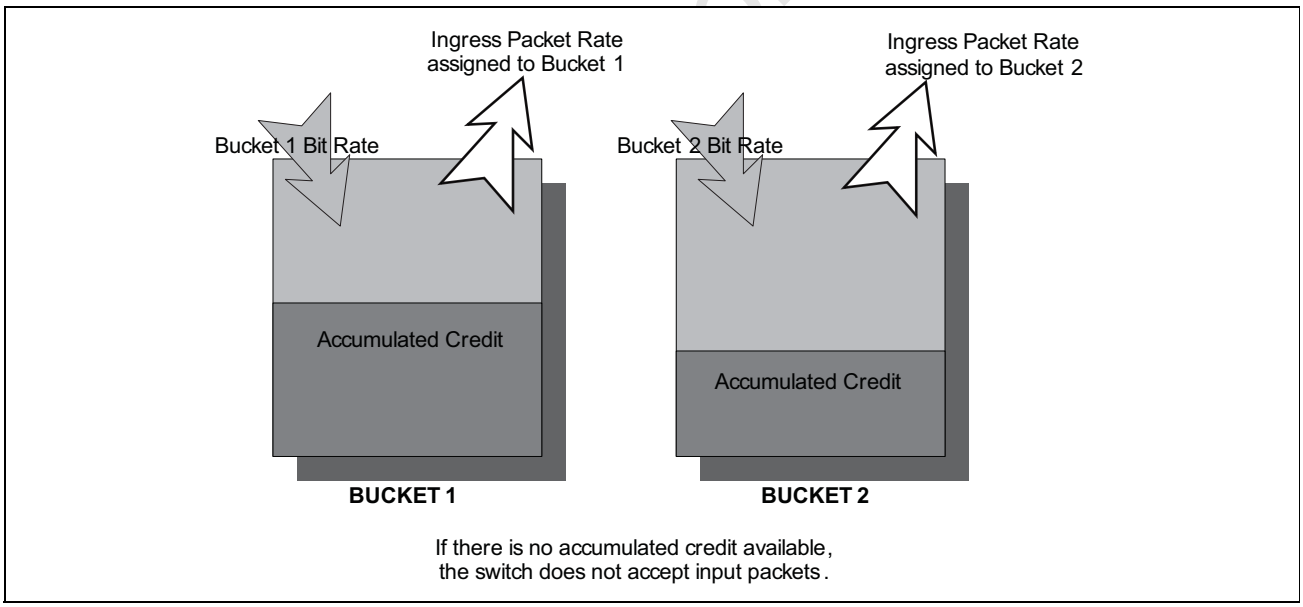


Figure 5: Bucket Flow

Two-Bucket System

For added flexibility, the BCM53101M employ two buckets to track the rate of ingressed packets. Each of the two buckets (Bucket 0 and Bucket 1) can be programmed to monitor different packet types or VLAN traffic. For example, Bucket 0 could monitor broadcast packets while Bucket 1 monitors multicast packets. Multiple packet types or VLAN traffic can be monitored by each bucket, and a packet type or VLAN traffic can be monitored by both buckets.

The rates of each bucket can be individually programmed (see "Bucket Bit Rate"). For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed using the Suppressed Packet Type Mask of the Ingress Rate Control Configuration register. This determines the maximum credit that can accumulate in each bucket. The Rate Count and Bucket Size can be individually programmed for each port, providing another level of flexibility. Suppression control can be enabled or disabled on a per-port basis Ingress Rate Control Configuration register. This system allows the user to control dual packet-type and VLAN traffic rates on a per-port basis.

Egress Rate Control

The BCM53101M monitors the rate of egress traffic per port. Unlike the ingress traffic rate control, egress rate control provides only the per-port rate control, regardless of traffic types. This feature uses only one bucket to track the rate of egressed packets. The Egress Rate Control feature can be enabled in the Port Egress Rate Control Configuration register, and the output rate per port can be controlled by setting the bucket size and Refresh Count in the same register. The Egress Rate Control feature supports only absolute bit rate mode (Bit Rate Mode = 0) and the bucket bit rate calculation is shown in Table 3.

Bucket Bit Rate

The relative ingress rates of each bucket can be programmed Port Receive Rate Control register on a per-port basis. Each port has a programmable Rate Count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed using the Ingress Rate Control Configuration register on a chip basis. If this bit is 1, the packet rate is automatically scaled according to the port link speed. Ports operating at 1000 Mbps are allotted a 100-times higher ingress rate than ports linked at 10 Mbps. Together, the Rate Count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The Rate Count values are specified in Table 3. Values outside these ranges are not valid entries.

Table 3: Bucket Bit Rate

Rate Count (RC)	*Bit Rate Mode*	*Link Speed*	*Bucket Bit Rate Equation*	*Approximate Computed Bucket Bit Rate Values (As a Function of RC)*
1–28	0	Any	= (RC x 8 x 1M) / 125	64 KB, 128 KB, 192 KB,..., 1.792 MB
29–127	0	Any	= (RC – 27) x 1M	2 MB, 3 MB, 4 MB,..., 100 MB
128–240	0	Any	= (RC – 115) x 1M x 8	104 MB, 112 MB, 120 MB,..., 1000 MB
1–125	1	10 Mbps	= (RC x 8 x 1M) / 100	0.08 MB, 0.16 MB, 0.24 MB,... 10 MB
1–125	1	100 Mbps	= (RC x 8 x 1M) / 10	0.8 MB, 1.6 MB, 2.4 MB,..., 100 MB

Table 3: Bucket Bit Rate (Cont.)

Rate Count (RC)	*Bit Rate Mode*	*Link Speed*	*Bucket Bit Rate Equation*	*Approximate Computed Bucket Bit Rate Values (As a Function of RC)*
1–125	1	200 Mbps	= (RC x 8 x 1M) / 5	1.6 Mb, 3.2 Mb, 4.8 Mb ..... 200 Mb
1–125	1	1000 Mbps	= RC x 8 x 1M	8 MB, 16 MB, 24 MB,... 1000 MB

Note: 1M represents 1 x 10^6.

IMP Port Egress Rate Control

The IMP port egress can be configured for rate limiting at either packets-per-second (pps) or bits-per-second (BPS) granularity.

Protected Ports

The Protected Ports feature allows certain ports to be designated as protected using the Protected Port Selection register. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. Some benefits of protected ports include the following:

- If all available ports are designated as protected ports except a single aggregator port, no incoming traffic to the protected ports is sent within the protected ports group. Any flooded traffic is forwarded to the aggregator port only.
- The server port and nonsecured ports are designated as protected to prevent nonsecured ports from monitoring important information on a server port. The nonsecured ports are not able to receive traffic from the server port.

Port Mirroring

The BCM53101M supports port mirroring, allowing ingress and egress traffic to be monitored by a single port designated as the mirror capture port. The BCM53101M can be configured to mirror the ingress or egress traffic of any other ports. Mirroring multiple ports is possible but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

Enabling Port Mirroring

Port mirroring is enabled by setting the Mirror Enable bit in the Mirror Capture Control register.

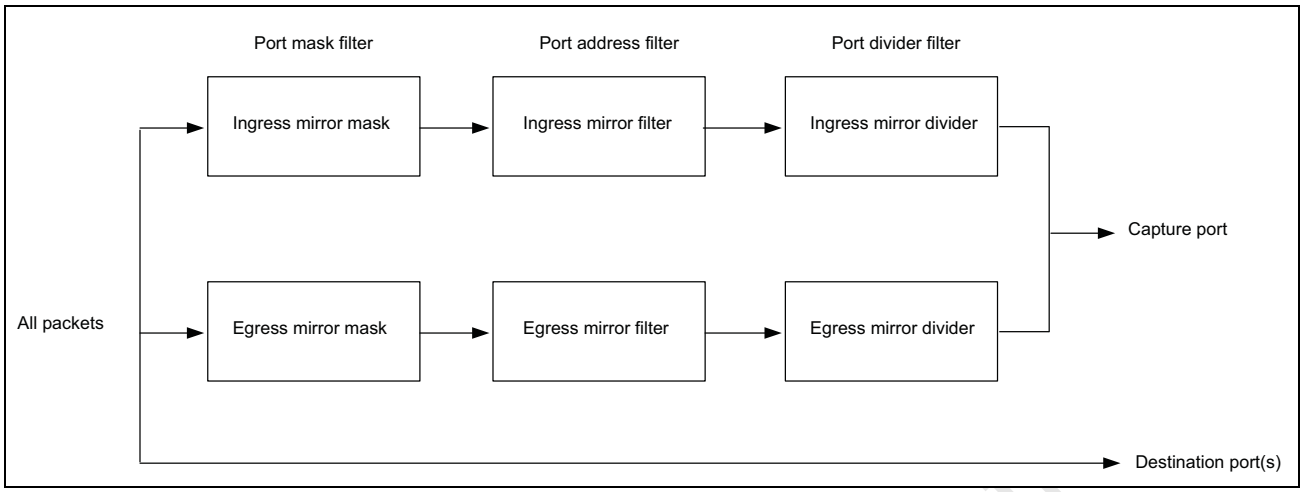


Figure 6: Mirror Filter Flow

Capture Port

The capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the capture port according to the Mirror Filtering Rules. The Capture port is specified by the Capture Port bits of the Mirror Capture Control register.

Mirror Filtering Rules

Mirror filtering rules consist of a set of three filter operations applied to traffic ingressed or egressed at a switch port: Port Mask, Packet Address, and Packet Divider.

Port Mask Filter

The IN_MIRROR_MASK bits in the Ingress Mirror Control register define the receive ports that are monitored. The OUT_MIRROR_MASK bits in the Ingress Mirror Divider register define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one-mirror capture port should be taken into account to avoid congestion or packet loss.

Packet Address Filter

The Ingress Mirror Control register is used to set the type of filtering applied to frames received on the mirrored ports. The IN_MIRROR_FILTER bits select from the following actions:

- Mirror all received frames
- Mirror received frames with DA = *x*
- Mirror received frames with SA = *x*

where *x* is the 48-bit MAC address programmed into the Ingress Mirror MAC Address register. Likewise, the Egress Mirror Control register is used to set the type of filtering that is applied to frames transmitted on the egressed mirrored ports. The filtering MAC address is specified in the Egress Mirror MAC Address register.

Packet Divider Filter

The IN_DIV_EN bit in the Ingress Mirror Control register allows further statistical sampling. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the Ingress Mirror Divider register. Only one out of every *n* frames is forwarded to the mirror capture port, where *n* = IN_MIRROR_DIV + 1. This allows the following additional capabilities:

- Mirror every n^{th} received frame
- Mirror every n^{th} received frame with DA = *x*
- Mirror every n^{th} received frame with SA = *x*

Similarly, the Egress Mirror Divide function is controlled by the Egress Mirror Control register and the Egress Mirror Divider register.

Note: When multiple ingress ports have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN_MIRROR_DIV to deliver the n^{th} receive frame to the mirror capture port. Egressed frames are governed by the OUT_MIRROR_MASK and OUT_MIRROR_DIV bits.

IGMP Snooping

The BCM53101M supports IP layer IGMP Snooping. When IGMP is enabled, the BCM53101M forwards IGMP frames to the frame management port. The external management entity programs the multicast membership information to the ARL table.

When the IGMP_IP_EN in the High-Level Protocol Control register is enabled, a frame with a value of 2 in the IP header protocol field, IGMP frames are forwarded to the CPU port. The management CPU determines which port should participate in the multigroup session from the IGMP control packets. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. If the IGMP_FWD_EN in the High-Level Protocol Control register is enabled, IGMP frames are trapped to the CPU port only.

MLD Snooping

Multicast Listener Discovery (MLD) is the protocol used by an IPv6 router to discover the presence of multicast listeners (nodes wishing to receive multicast packets) on its directly attached links, and to discover specifically which multicast addresses are of interest to those neighboring nodes. One important difference to note is that MLD uses ICMPv6 message types rather than IGMP message types.

The BCM53101M supports IP layer MLD Snooping.

When the ICMPv6_EN in the High-Level Protocol Control register is enabled, a frame with a value of 58 and 0 in the IP next header field is forwarded to the CPU port. The management CPU determines which port should participate in the multigroup session from the ICMPv6 control packets. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. If the ICMPv6_FWD_EN in the High-Level Protocol Control register is enabled, ICMPv6 frames are trapped to the CPU port only.

IEEE 802.1x Port-Based Security

IEEE 802.1x is a port-based authentication protocol. By receiving and extracting special frames, the CPU controls whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM53101M detects EAPOL frames by checking the destination address of the frame. The destination address should be either a multicast address as defined in IEEE 802.1x (01-80-C2-00-00-03) or a user-predefined MAC (unicast or multicast) address. Once EAPOL frames are detected, the frames are forwarded to the CPU so it can send the frames to the authenticator server. Eventually, the CPU determines whether the requestor is qualified or not based on its MAC_Source addresses, and frames are either accepted or dropped. The per-port EAP can be programmed in the register.

The BCM53101M provides three modes for implementing the IEEE 802.1x feature. Each mode can be selected by setting the appropriate bits in the register.

The Basic Mode (when EAP Mode = 00'b) is the standard mode. The EAP_BLK_MODE bit is set prior to authentication to block all incoming packets. Upon authentication, the EAP_BLK_MODE bit is cleared to allow incoming packets. In this mode, the Source Address of incoming packets is not checked.

The second mode is Extended Mode (when EAP Mode = 10'b), where an extra filtering mechanism is implemented after the port is authenticated. If the Source MAC address is unknown, the incoming packets are dropped and the unknown SA are not learned. However, if the incoming packet is an IEEE 802.1x packet or a special frame, the incoming packets are forwarded. The definition of the Unknown SA in this case is when the switch cannot match the incoming Source MAC address to any of the addresses in ARL table, or the incoming Source MAC address matches the address in ARL table but the port number is mismatched.

The third mode is Simplified Mode (when EAP Mode = 11'b). In this mode, the unknown Source MAC address packets are forwarded to the CPU rather than dropped. Otherwise, it is same as Extended Mode operation.

Note: The BCM53101M check only the destination addresses to qualify EAPOL frames. Ethernet type fields, packet type fields, or non-IEEE 802.1Q frames are not checked.

MSTP Multiple Spanning Tree

The BCM53101M supports up to eight multiple spanning trees. When the EN_RX_BPDU bit (page 02h, address 00h, bit 1) = 0 (default state), the BCM53101M floods BPDU packets to all local ports. When the EN_RX_BPDU bit = 1, the BCM53101M forwards BPDU packets to the management port only.

Software Reset

Software resets of the BCM53101M are triggered by programming the SW_RST bit (see "Watch Dog Control 0 Register (Page 00h: Address 79h)" on page 154).

BroadSync™ HD

BroadSync HD is the enhancement to IEEE 802.3 MAC and IEEE 802.1D bridges to support the kind of low-latency isochronous services and guaranteed quality of service required for many consumer electronics applications.

The BCM53101M provides the BroadSync HD feature through the BroadSync HD Enable Control register. The BCM53101M always forwards BPDU MRP packets to the CPU for BroadSync HD applications and handles IEEE 802.1 Time Sync Protocol.

The BCM53101M can identify a packet as a BroadSync HD packet if the MAC DA matches a multicast group (configured based on MRP protocols). PCP = 4 or 5 and the ingress port is AV-enabled. There are two dedicated queues for BroadSync HD Class 5 and Class 4 traffic per egress port. The BCM53101M enhances shaping and scheduling for BroadSync HD operation.

Time Base and Slot Generation

For BroadSync HD applications, the BCM53101M maintains a time base (32-bit counter) running at a granularity of 1 ns, which can be adjusted by the CPU for synchronization with the BroadSync HD time master unit (Switch or Host) through the IEEE 802.1 Time Synchronized (TS) protocol (to be standardized). The TS protocol is implemented by the CPU, which requires the BCM53101M to perform the following operations:

- A received TS protocol packet is timestamped at the ingress port when the first byte (of MACDA) arrives and is transferred along with the receiving timestamp to the CPU.
- A TS protocol packet initiated by the CPU (to be transmitted at an egress port) is timestamped at the egress port when the first byte (of MACDA) is transmitted. The transmit timestamp recorded at the egress port is reported back to CPU.

The time synchronization point peers over an Ethernet link must be chosen such that the link delay is perceived as constant and the protocol exchange occurs at least every 10 ms over every link.

The CPU may be required to speed up or slow down the time base maintained in the BCM53101M based on the TS protocol execution. The BCM53101M provides the time base adjustment mechanism for graceful time changes based on CPU instructions.

In addition, the BCM53101M maintains a counter mechanism to generate a slot for BroadSync HD traffic scheduling:

- A slot—defined as 125 µs—is used to pace BroadSync HD Class 5 traffic, which has tight jitter requirements.

- A macroslot — configurable as 1 ms, 2 ms, or 4 ms (binary number of slots) using the BroadSync HD Slot Adjustment register — is used to pace the BroadSync HD Class 4 traffic, which has relaxed jitter requirements.

The CPU may be required to make the slot wider or narrower based on the TS protocol execution. The BCM53101M provides a slot adjustment mechanism for graceful slot width changes based on CPU instructions.

Transmission Shaping and Scheduling

Packets queued at each Ethernet (egress) port is subject to scheduling behavior as shown in Figure 7.

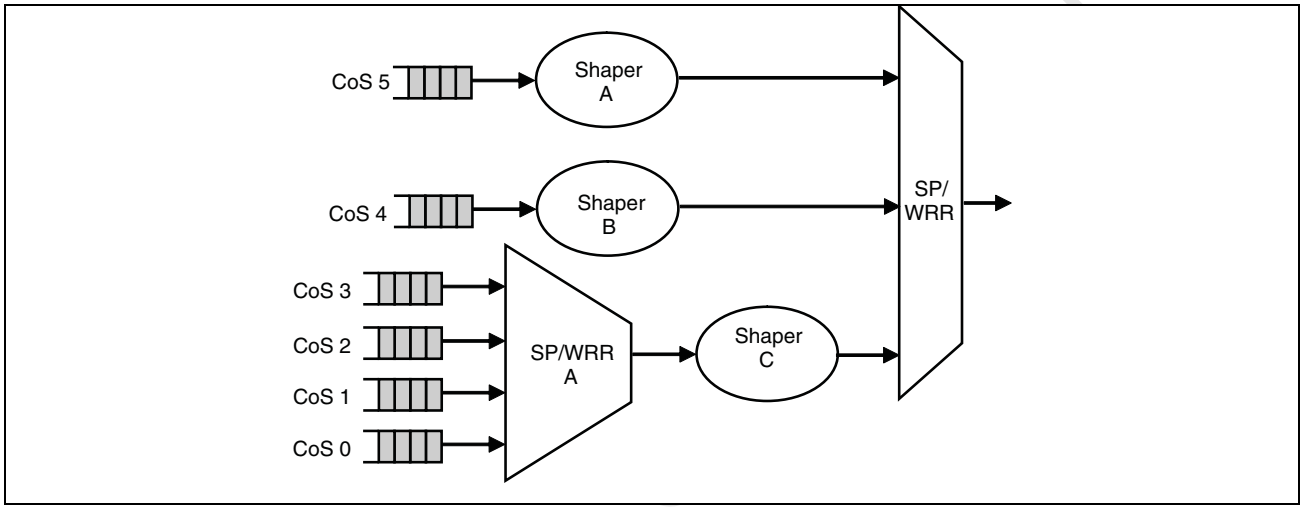


Figure 7: BroadSync HD Shaping and Scheduling

BroadSync HD Class 5 Media Traffic

The CoS 5 queue is dedicated for BroadSync HD Class 5 traffic only, and a CoS 5 packet is always the highest priority to be scheduled for transmission if it is allowed by the Shaper A that operates as follows:

- Shaper A is an emulation of fixed bandwidth pipe for Class 5 BroadSync HD traffic with tight jitter that handles interference from non-BroadSync HD or Class 4 BroadSync HD traffic adaptively. The preamble and IPG transmission are not taken into account for pipe operation.
- Tunable parameters for Shaper A include the following:
  - MaxAVPacketSize is a global setting (set using the BroadSync HD Maximum Packet Size register) that indicates the maximum packet size allowed on an AV-enabled port.
  - Class5_BW is a per-port setting (set using the BroadSync HD Class 5 Bandwidth Control register) that indicates the reserved bandwidth for Class 5 BroadSync HD traffic at a granularity of bytes (per slot, 125 µs).
  - Class5_Window is a per-port setting (set using the BroadSync HD Class 5 Bandwidth Control register) that indicates jitter control for Class 5 BroadSync HD transmission.
- At the start of each slot:
  a. If the queue is empty, reset the credit in the shaping bucket to Class5_BW.

b. If the queue is not empty and Class5_Window is set to 0, reset the credit in the shaping bucket to Class5_BW.
c. If the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is greater than MaxAVPacketSize, reset the credit in the shaping bucket to Class5_BW.
d. If the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is less than or equal to MaxAVPacketSize, add Class5_BW to the credit in the shaping bucket.

- The credit in the shaping bucket decrements for each byte transmitted for Class 5 BroadSync HD traffic through the port.
  - If the credit reaches 0 before the end of the current slot while transmitting a Class 5 BroadSync HD packet, the ongoing packet transmission is not interrupted and the credit stays at 0 until being reset at the start of next slot.
  - The credit decrements resumes at the next slot if the ongoing transmission continues.
- As long as the credit in the shaping bucket is greater than 0, a Class 5 BroadSync HD packet is allowed to be scheduled for transmission.

BroadSync HD Class 4 Media Traffic

The CoS 4 queue is dedicated for BroadSync HD Class 4 traffic only. A CoS 4 packet always yields to CoS 5 traffic (if allowed to be scheduled) but takes precedence over the traffic from CoS 0–CoS 3 queues or follows the weight ratio between CoS 4 and CoS 0–CoS 3 for transmission scheduling, if it is allowed by Shaper B which operates as follows:

- Shaper B is an emulation of fixed bandwidth pipe for Class 4 BroadSync HD traffic with relaxed jitter that handles interference from non-BroadSync HD or Class 5 BroadSync HD traffic adaptively. Shaper B statistically levels the Class 4 BroadSync HD transmission bursts towards the next hop switch to reduce the buffering requirements by using the slot (instead of the macroslot) as the pacing mechanism. The preamble and IPG transmission are not accounted for in pipe operation.
- Tunable parameters for the Shaper B include the following:
  - MacroSlot_Period is a global setting (set using the BroadSync HD Slot Adjustment register to indicate 1 ms, 2 ms, or 4 ms) that indicates the periodic cycle time to shape the Class 4 traffic.
  - MaxAVPacketSize is a global setting that indicates the maximum packet size allowed on an AV-enabled port (same as for BroadSync HD Class 5 setting).
  - Class4_BW is a per-port setting (set using the BroadSync HD Class 4 Bandwidth Control register) that indicates the evenly divided bandwidth share per slot, which is derived by dividing the reserved bandwidth for Class 4 BroadSync HD traffic at a granularity of bytes (per macroslot) by the number of slots within a macroslot.
- At the start of each slot:
  - If the slot is the first one for the current macroslot, reset the credit bucket to Class4_BW + MaxAVPacketSize (MaxAVPacketSize is used as the deficit base);
  - Otherwise, add Class4_BW to the credit in the shaping bucket.
- The shaping credit bucket decrements for every byte transmitted for Class 4 BroadSync HD traffic.

As long as the credit in the shaping bucket is greater than or equal to MaxAVPacketSize, a Class 4 BroadSync HD packet is allowed to be scheduled for transmission.

Address Management

The BCM53101M Address Resolution Logic contains the following features:

- Four bins per bucket address table configuration
- Hashing of the MAC/VID address to generate the address table point

The address management unit of the BCM53101M provides wire-speed learning and recognition functions. The address table supports 2K unicast/multicast addresses using on-chip memory.

Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains four entries or bins. The address table has 512 buckets with four entries in each bucket, thus allowing up to four different MAC addresses with the same hashed index bits to be mapped simultaneously into the address table. In the ARL DA/SA lookup process, it hashes a 10-bit search index and reads from bin 0 and bin 1 in the first cycle, and reads from bin 2 and bin 3 in the second cycle. These four entries are used for ARL routing and learning.

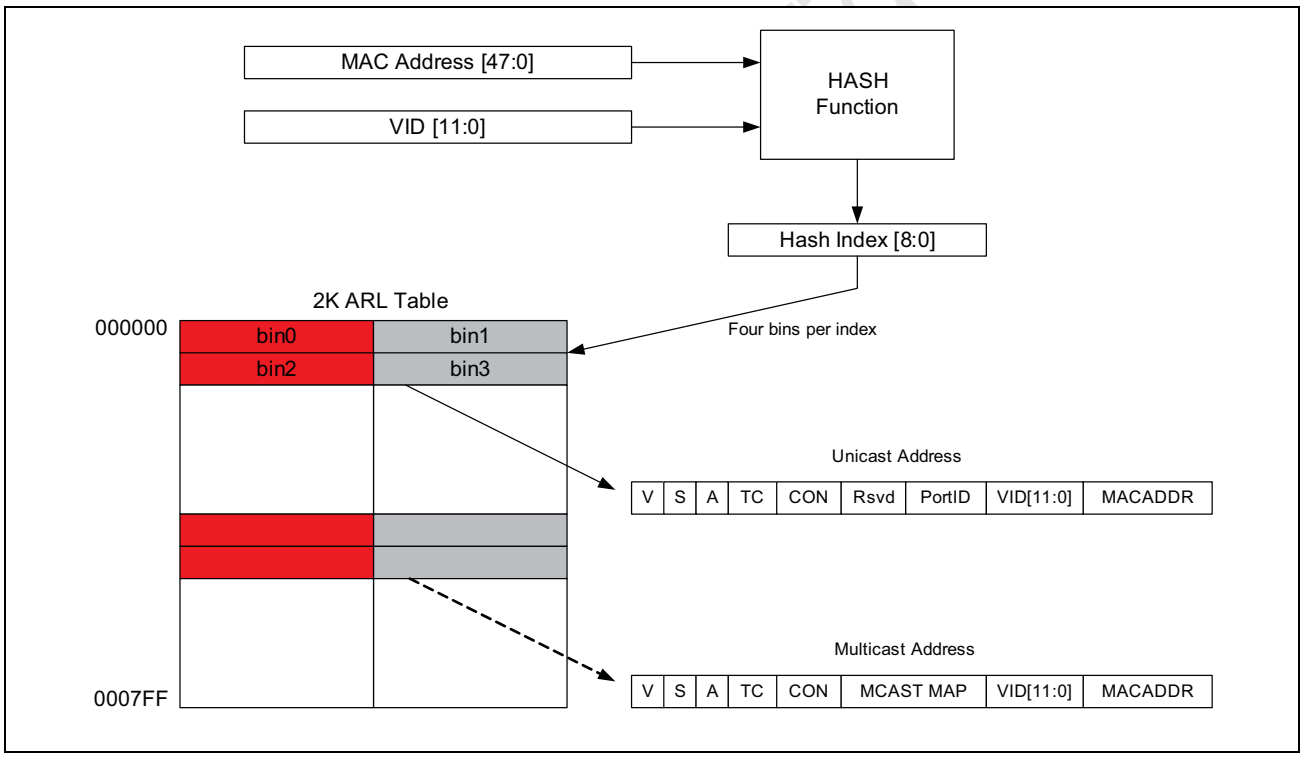


Figure 8: Address Table Organization

The index to the address table is computed using a hash algorithm based on the MAC address and the VLAN ID (VID), if enabled.

Note: In the Enable IEEE 802.1Q and VLAN Learning Mode both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See "IEEE 802.1Q VLAN" on page 38 for more information.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits [9:0] of the hash are used as an index to the approximately 4K locations of the address table.

The CRC-CCITT polynomial is $x^{16}+x^{12}+x^5+1$.

Address Learning

Information is gathered from received unicast packets and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.
- The packet does not have a reserved multicast destination address.
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 5 on page 52 for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table. They must be written using one of the "Programming Interfaces" on page 85. See "Writing an ARL Entry" on page 56 and Table 7 on page 53 for more information.

Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The destination address (DA) and VID of the received packet are used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for "Unicast Addresses" on page 52 and "Multicast Addresses" on page 53.

Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. The unicast address-resolution algorithm is as follows:

- If the multiport addressing feature is enabled and the DA matches one of the programmed multiport addresses, it is forwarded accordingly. See "Using the Multiport Addresses" on page 57.
- The lower nine bits of the hashed index key are used as a pointer into the address table memory and the entry is retrieved.
- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the unicast DLF forward bit is set, the frame is forwarded according to the port map in the Unicast Lookup Failed Forward Map register.
- Otherwise, the packet is flooded to all appropriate ports.

See Table 4 for definitions of the unicast index key and the assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See Table 5 for a description of a unicast ARL entry.

Table 4: Unicast Forward Field Definitions

EN_1QVLAN	*Index Key*	*Forwarding Field*
1	DA and VID	Port ID
0	DA	Port ID

Table 5: Address Table Entry for Unicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address
VALID	1 = Entry is valid 0 = Entry is empty
STATIC	1 = Entry is static—Should not be aged out and is written and updated by software 0 = Entry is dynamically learned and aged
AGE	1 = Entry has been accessed or learned since last aging process 0 = Entry has not been accessed since last aging process
TC	MACDA-based TC (valid for static entries only). See "Quality of Service" on page 32 for more information.
Reserved	–
Reserved	Only 00 is valid.
PORTID	Port identifier. The port associated with the MAC address.
MAC ADDRESS	48-bit MAC address

Note: The fields described in Table 5 can be written using the ARL Table MAC/VID Entry N (N = 0–3) and ARL Table Data Entry N (N = 0–3) registers.

Multicast ARL table entries are described in Table 7 on page 53.

Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP_MULTICAST bit is set, multicast frames are assigned a forwarding field corresponding to a multicast port map from the matching ARL entry (see "Address Management" on page 50). If no matching ARL entry is found, the packet is flooded to all appropriate ports.

The multicast address resolution algorithm is as follows:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 8 on page 54.
- If the multiport addressing feature is enabled and the DA matches one of the programmed multiport addresses, it is forwarded accordingly. See "Using the Multiport Addresses" on page 57.
- Otherwise, the lower nine bits of the hashed index key are used as a pointer into the ARL table memory and the entry is retrieved.
- If the valid indicator is set and the address stored at the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the multicast DLF forward bit is set (see "Address Management" on page 50), the frame is forwarded according to the port map in the Multicast Lookup Failed Forward Map register.
- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

See Table 6 for definitions of the multicast index key and the assigned forwarding field. The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See Table 7 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 55 for more information.

Table 6: Multicast Forward Field Definitions

EN_1QVLAN	*IP_MULTICAST*	*Index Key*	*Forwarding Field*
1	0	DA and VID	Port ID
0	0	DA	Port ID
1	1	DA and VID	IPMC0
0	1	DA	IPMC0

Table 7: Address Table Entry for Multicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address

Table 7: Address Table Entry for Multicast Address (Cont.)

Field	Description
VALID	1 = Entry is valid 0 = Entry is empty
STATIC	1 = Entry is static—This entry is not aged out and is written and updated by software. 0 = Not defined
AGE	Ignored for static ARL table entries
TC	MACDA-based TC (valid for static entries only). See "Quality of Service" on page 32 for more information.
Reserved	–
IPMC0 [8:0]	Multicast forwarding mask 1 = Forwarding enable 0 = Forwarding disable
MAC ADDRESS	48-bit MAC address

Note: The fields described in Table 7 can be written using the ARL Table MAC/VID Entry N (N = 0–3) and ARL Table Data Entry N (N = 0–3) registers.

Unicast ARL table entries are described in Table 5 on page 52.

Reserved Multicast Addresses

Table 8 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions.

Table 8: Behavior for Reserved Multicast Addresses

MAC Address	Function	IEEE 802.1 Specified Action	Unmanaged Mode Action	Managed Mode Action
01-80-C2-00-00-00	Bridge group address	Drop frame	Flood frame	Forwards frame to IMP only
01-80-C2-00-00-01	IEEE 802.3x MAC control frame	Drop frame	Receive MAC determines if valid pause frame and acts accordingly	Receive MAC determines if valid pause frame and acts accordingly.
01-80-C2-00-00-02	Reserved	Drop frame	Drop frame	Forwards to frame management port only
01-80-C2-00-00-03	IEEE 802.1x port-based network access control	Drop frame	Drop frame	Forwards frame to management port only
01-80-C2-00-00-04–01-80-C2-00-00-0F	Reserved	Drop frame	Drop frame	Forwards frame to management port only

Table 8: Behavior for Reserved Multicast Addresses (Cont.)

MAC Address	Function	IEEE 802.1 Specified Action	Unmanaged Mode Action	Managed Mode Action
01-80-C2-00-00-10	All LANs bridge management group address	Forward frame	Flood frame	Forwards frame to all ports including management port
01-80-C2-00-00-11– 01-80-C2-00-00-1F	Reserved	Forward frame	Flood frame	Forwards frame to all ports excluding management port[a]
01-80-C2-00-00-20	GMRP address	Forward frame	Flood frame	Forwards frame to all ports excluding management port
01-80-C2-00-00-21	GVRP address	Forward frame	Flood frame	Forwards frame to all ports excluding management port
01-80-C2-00-00-22– 01-80-C2-00-00-2F	Reserved	Forward frame	Flood frame[b]	Forwards frame to all ports excluding management port[b]

a. Can also be programmed to forward frame to management port.
b. Frames flood to all ports. Certain exclusions apply, such as VLAN restrictions.

Static Address Entries

The BCM53101M supports static ARL table entries that are created and updated using one of the "Programming Interfaces" on page 85. These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location using the ARL/VTBL Access register and setting the STATIC bit. The AGE bit is ignored. Static entries do not automatically learn MAC addresses or port associations and are not aged out by the automatic internal aging process. See "Writing an ARL Entry" on page 56 for details.

Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL read/write control which allows an address-entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

Reading an ARL Entry

To read an ARL entry, do the following:

1. Set the MAC address in the MAC Address Index register.
2. Set the VLAN ID in the VLAN ID Index register.

   This step is necessary only if the VID is used in the index key.

3. Set the ARL_R/W bit to 1 in the ARL Table Read/Write Control register.
4. Set the START/DONE bit to 1 in the ARL Table Read/Write Control register.
   This initiates the read operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. The matching ARL entry is read. The contents of entry are stored in the ARL Table MAC/VID Entry N (N = 0–3) and ARL Table Data Entry N (N = 0–3) registers.

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. An entry that does not match might be a valid entry but is not a valid match for the index key. All other read entries are considered valid ARL entries.

Writing an ARL Entry

To write an ARL entry, do the following:

1. Follow the steps in "Reading an ARL Entry" (above) to read the ARL entry matching the MAC address and VID that are written to the table.
2. Keep the values that remain from the previous read operation:
   - MAC Address Index register
   - VLAN ID Index register
   - ARL Table MAC/VID Entry N (N = 0–3) register
   - ARL Table Data Entry N (N = 0–3) register
3. Modify the correct entry as necessary. Set the STATIC bit so that the entry is not aged out.
4. Set the ARL_R/W bit to 0 in the ARL Table Read/Write Control register.
5. Set the START/DONE bit to 1 in the ARL Table Read/Write Control register. This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table.

Searching the ARL Table

The second method to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the Start/Done bit in the ARL Table Search Control register begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the Search Valid bit indicates when a found valid entry is available in the ARL Table Search MAC/VID Result N (N = 0–1) and ARL Table Search Data Result N (N = 0–1) registers. When the host reads the contents of the ARL Table Search Data Result 1 register (page 05h: address 78h), the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write, or search process and then read/write other registers, returning periodically to see if the operation has completed.

Address Aging

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous one to two aging intervals. The aging interval is programmable using the Age_Change_En and AGE_TIME bits in the Aging Time Control register.

Entries that are written and updated using one of the "Programming Interfaces" on page 85 should have the STATIC bit set. Thus, they are not affected by the aging process.

For each entry in the ARL table, the aging process performs the following:

- If the VALID bit is not set, no further action is required.
- If the VALID bit is set and the STATIC is set, no further action is required.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is set, then clear the AGE bit. This keeps the entry in the table, but marks it so that it is removed if it is not accessed before the subsequent aging scan.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is reset, then reset the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

Fast Aging

The fast aging function can be enabled per port or VLAN ID.

The port fast aging can be enabled by setting the Start/Done bit of the Fast-Aging Control register, the Fast Age All Ports bit of the Fast-Aging Port Control register, and the appropriate port bits in the Fast-Aging Port Control register.

The VLAN ID fast aging can be enabled by setting the Start/Done bit of the Fast-Aging Control register, the Fast Age All VID bit of the Fast-Aging VID Control register, and the appropriate VLAN ID bits of the Fast-Aging VID Control register.

Using the Multiport Addresses

The Multiport Address N (N = 0–5) register can be used to forward a given MAC address and Ether Type to multiple ports. Packets with a corresponding DA are forwarded to the port map contained in the Multiport Vector N (N = 0–5) register. These registers must be controlled using the Multiport Control register.

Note: The Multiport Address N (N = 0–5) register is the only mechanism for TS Protocol qualification for the BroadSync HD application. It can be enabled using the Multiport Control register.

Power-Saving Modes

The BCM53101M can be configured to operate in different power-saving modes. See Table 9.

Table 9: Power-Saving Modes of the BCM53101M

Mode	*Description*
Normal	Normal operating mode after BCM53101M is reset. In this state, there is no power-saving scheme being turned on.
Auto power-down (APD)	When a PHY is configured in auto power-down mode, it can nap for a few seconds and then wakes up for a few milliseconds to check if there is any chance to link up. The nap and wake up intervals are programmable. This mode is recommended for the default operating configuration. See also "Auto Power-Down Mode Programming Guide" on page 60.
Sleep	The most power-saving mode. The BCM53101M can be configured to enter sleep mode when all the ports are in a link down state for an extended period of time. In this state, software can respectively shut down the PHY, the PLL, and the MAC clocks to save power. In addition, the system clock can also be slowed down to 12.5 MHz to save even more power. Because there is a time delay between link down and signal-detect deassertion, the software needs to check all the ports for Signal Detect to be low before entering sleep mode. This is to prevent the device from waking up immediately by any false detection of Signal Detect. While in sleep mode, the Signal Detect capability of the PHY is still functioning. Hence, the software can poll for the PHY status to determine whether it is the time to leave sleep mode. When energy is detected at any port, the software initiates the BCM53101M to exit sleep mode. In sleep mode, the switch registers are still accessible, but the internal PHY registers are not. ***Note:*** While the system clock is operating at 12.5 MHz, the SPI clock is running at 3.125 MHz. See also "Sleep Mode Programming Guide" on page 61.

Power State Diagram

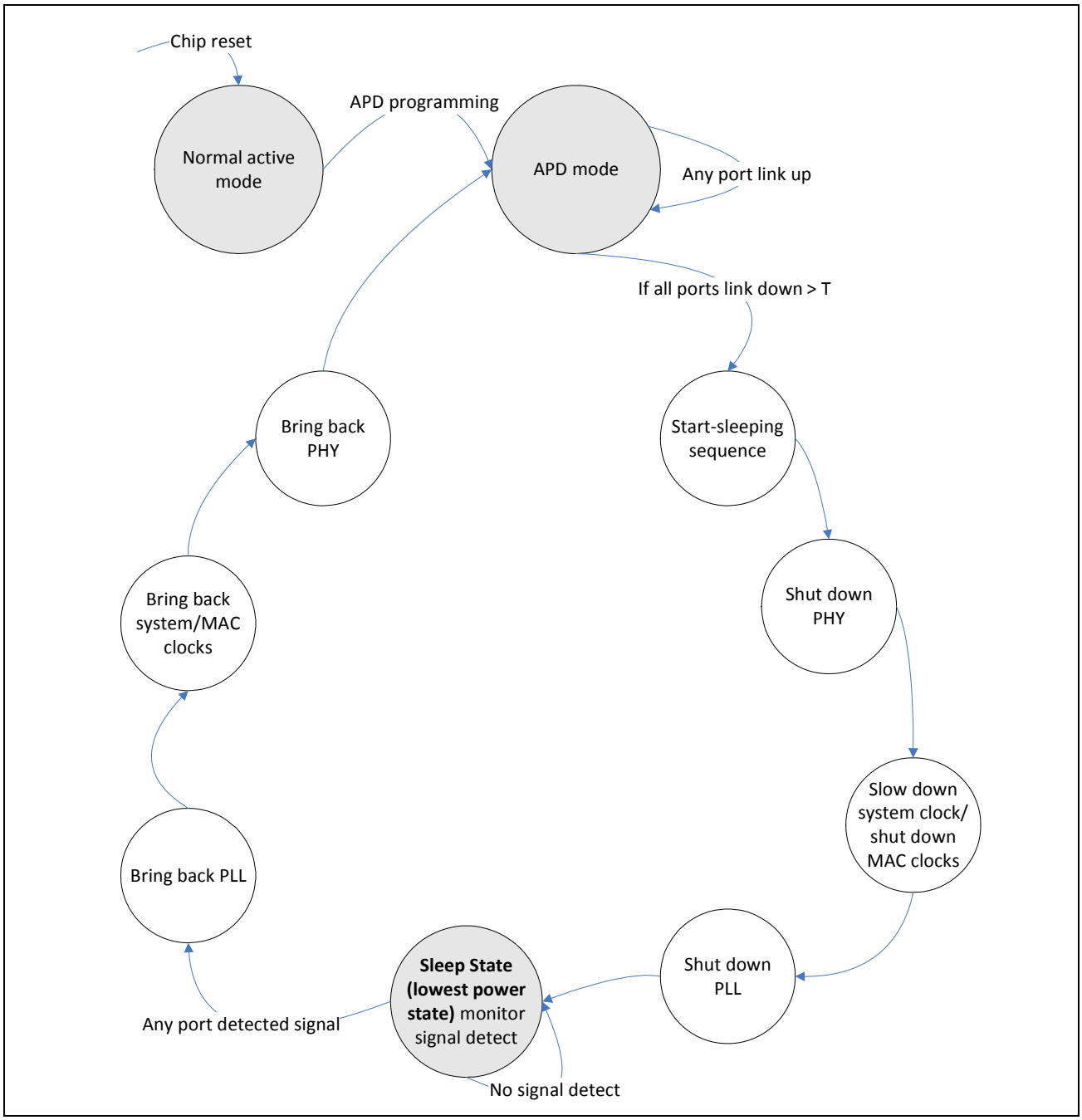


Figure 9: Power State Diagram

Auto Power-Down Mode Programming Guide

Set nap timer to 5s and wake-up timer to 40 ms.

Table 10: Enable EPHY Shadow Registers

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*
10	3e	2	0x008b
11	3e	2	0x008b
12	3e	2	0x008b
13	3e	2	0x008b
14	3e	2	0x008b

Table 11: Enable Auto Power-Down

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*
10	36	2	0x0031
11	36	2	0x0031
12	36	2	0x0031
13	36	2	0x0031
14	36	2	0x0031

Table 12: Disable EPHY Shadow Registers

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*
10	3e	2	0x000b
11	3e	2	0x000b
12	3e	2	0x000b
13	3e	2	0x000b
14	3e	2	0x000b

Sleep Mode Programming Guide

1. Verify that Signal Detect is low before entering sleep mode (read).

Check page 00, offset 4e, bits [4:0] for signal detect of EPHY ports 4–0.

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	4e	2	0x8000	// Signal Detect of all ports is low

2. Shut down the PHY (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	4a	4	0x0000001f	// Enable PHY power-down.
00	4a	4	0x01f0001f	// Power down PHY TX.
00	4a	4	0x01ff801f	// Power down PHY RX and keep Reset Divider and Signal Detect enabled.

3. Slow down system clock and shut down MAC clocks (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	df	1	0xa0	// Slow system clock down to 12.5 MHz and stop port 5/port 8 MAC clocks.

4. Shut down the PLL (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	dc	1	0x1f	// Power down the PLL.

5. Monitor signal detection (read).

Check page 00, offset 4e, bits [4:0] for signal detect of EPHY ports 4–0.

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	4e	2	0x8001	// For example, port 0 has detected signal

6. Bring back PLL (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	dc	1	0xc0	// Reset PLL.
00	dc	1	0x00	// PLL reset completed.

7. Bring back system clocks and MAC clocks (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*
00	df	1	0x00 // Resume normal system clock and port 5/port 8 MAC clocks.

8. Bring back PHY (write).

Page	*SPI Offset*	*Register Size (Bytes)*	*Data*	
00	4a	4	0x00000000	// Disable PHY power-down mode.
00	48	2	0x001f	// Reset PHY and wait for 400 ns.
00	48	2	0x0000	// PHY reset. Refrain from any PHY activity for 100 µs.

Section 3: System Functional Blocks

Overview

The BCM53101M includes the following blocks:

Media Access Controller

The BCM53101M contains six 10/100 MACs and one GMAC.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3-, IEEE 802.3u-, and IEEE 802.3x-compliant.

Receive Function

The MAC initiates frame reception following the assertion of a receive-data-valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1,536 bytes or 2048 bytes for jumbo-enabled ports.

Note: Frames longer than 1,518 (untagged) and frames longer than 1,522 (tagged) are considered oversized frames. However, only frames over 1,536 bytes are treated as bad frames and dropped. When jumbo-frame mode is enabled, only frames longer than 2048 bytes are bad frames and dropped.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled by writing to the Port Traffic Control register.

Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and interpacket gap enforcement.

In 10/100 Mbps half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If a collision is observed during frame transmission and the collision window timer has not expired, the transmit controller asserts jam and executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit-times of IPG have been observed. Transmit functions can be disabled by writing to the Port Traffic Control register.

Flow Control

The BCM53101M implements an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53101M initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full- and half-duplex modes.

Half-Duplex

In half-duplex mode, the MAC backpressures a receiving port by transmitting a 96 bit-time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

Integrated 10/100 PHY

The PHY is the ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface and performs the reverse process on data received at the MDI interface. The registers of the PHY are read/written to using the programming interface. The following sections describe the operations of the internal PHY block.

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs preequalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the PHY transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start-of-stream delimiter (/J/K/ codes) and appending an end-of-stream delimiter (/T/R/ codes) to the end of the packet. The transmitter repeatedly sends the idle (/i/ code) between packets. The encoded data stream is serialized and then scrambled by the stream cipher block. The scrambled data is then encoded into MLT3 signal levels.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn-to-zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the internal MAC interface. When an invalid code group is detected in the data stream, the PHY asserts the internal MII receive error signal. This signal is also asserted when the link fails or when the descrambler loses lock during packet reception.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD± pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch-detect circuits. When no signal is detected on the receive pair, the link monitor enters the link-fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters link-pass state and the transmit and receive functions are enabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The PHY achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design drives high noise-tolerant performance. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise-rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 100BASE-TX and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input and the receive clock is locked to the incoming data stream.

Baseline Wander Correction

100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as *baseline wander*, can greatly reduce the noise immunity of the receiver. The PHY automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced and, therefore, produces very low-noise transmit signals.

Stream Cipher

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive-ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

The receiver descrambles the incoming data stream by exclusive-ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53101M enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that interpacket gaps containing idles or frame extensions are received at expected intervals.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

PHY Registers

Each transceiver within the BCM53101M contains a complete set of PHY registers. The 5-bit transceiver address is assigned correspondingly to the internal port ID. All PHY registers can be accessed either through the MDC and MDIO signals or through the Serial Peripheral Interface.

100BASE-FX Fiber Mode[1]

The 10/100 port can be configured to operate in 100BASE-FX compatible mode. The following sequence is required for configuring the preferred PHY ports to 100BASE-FX compatible operation using register write from the CPU. Each port's register can be programmed through pages 10h–14h, respectively.

1. Write 2100h to register (pages 10h–14h, address 00h–01h) to force the port to 100M full-duplex without auto-negotiation. Most FX applications require configuration for full-duplex.

1. 100BASE-FX fiber mode is supported starting with B0 silicon only.

2. Set bits 9 and 5 of register (pages 10h–14h, address 20h–21h) to bypass the scrambler and descrambler blocks (these scrambling functions are not required for 100BASE-FX operation). Other bits within this register may be set, so it is best to perform a read-modified write to ensure proper setting of this register.
3. Set bit 5 of hidden register (pages 10h–14h, address 2Eh–2Fh). This changes the three-level MLT-3 code transmitted by the PHY to two-level binary suitable for driving standard fiber transceivers. Additionally, the PHY receiver is configured to recognize binary signaling. This register access must also be in the form of a read-modified write.
4. Enable the internal EFX signal detect function by doing the following:
   a. Write 008Bh to register (pages 10h–14h, address 3Eh–3Fh).
   b. Write 0200h to register (pages 10h–14h, address 32h–33h).
   c. Write 0084h to register (pages 10h–14h, address 3Ah–3Bh).
   d. Write 000Bh to register (pages 10h–14h, address 3Eh–3Fh).

Refer to the 53101-AN10x-R, *Layout and Design Guide*, for the FX termination requirement.

Frame Management

The BCM53101M provides a frame management block that works in conjunction with a selectable port interface to receive forwarded management frames directed to the switch. The frame management block is configured using the En_IMP_Port bits as shown in Table 91: "Global Management Configuration Register (Page 02h: Address 00h)," on page 164.

An external CPU connects using the selected port interface to process the forwarded frames and respond appropriately. When the selected port is defined as the Frame Management Port, it is referred to as the In-band Management Port (IMP).

In-Band Management Port

The BCM53101M supports dual IMP ports. Either one or both RGMII and MII ports can be configured as the In-band Management Port (IMP).

The IMP can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system.

As the IMP is defined as the frame management port, normal frame data is forwarded to the port based on the state of the RX_UCST_EN, RX_MCST_EN, and RX_BCST_EN bits in the IMP Port Control register. If these bits are cleared, no frame data is forwarded to the Frame Management Port with the exception that frames meeting the mirror ingress/egress rules criteria are always forwarded to the designated frame management port.

Packets transferred over the IMP port are tagged with the Broadcom proprietary header to carry the necessary information that is of interest to the management entity running on the CPU, as shown in Figure 10, except for the PAUSE frame. The IMP port must support the normal Ethernet pause-based flow control mechanism.

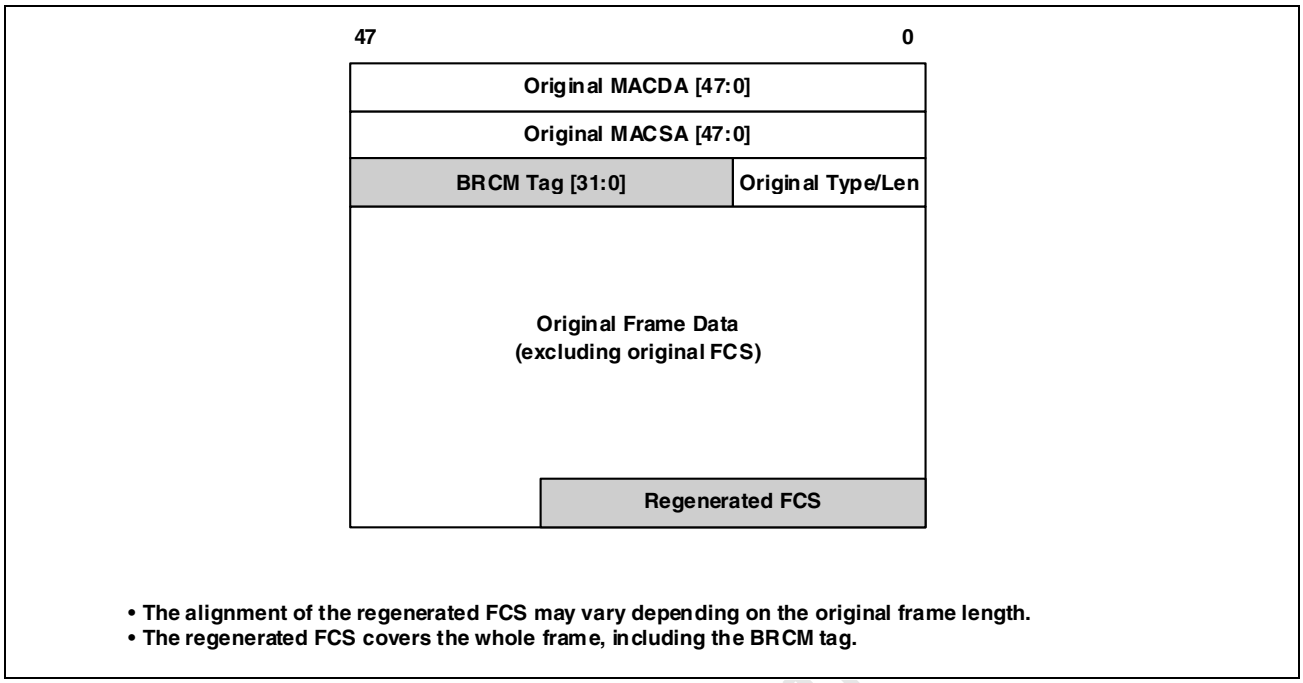


Figure 10: IMP Packet Encapsulation Format

The BRCM tag is designed for asymmetric operation across the IMP port. The information carried from the switching device to the CPU is different from the information carried from the CPU to the switching device.

Similarly, the host system must insert the BRCM tag fields into frames intending to be sent into the management port, to be routed to specific egress ports. The opcode within the tag field determines how the frame is handled and allows frames to be forwarded using the normal address lookup using a port ID designation within the tag.

Note: The IMP link supports the standard PAUSE flow control protocols, so the coding of the first two bytes of the BRCM tag must not be the same as that of the Ethertype field indicating the PAUSE frame.

The BRCM tag are transmitted with the convention of highest significant octet first, followed by the next lowest significant octet, and so on, with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM tag field in Table 14 on page 70, the most significant octet would be transmitted first (bits [24:31]), with bit 24 being the first bit transmitted.

Note: The BCM53101M introduces a new option to disable the BRCM header. When disabled, the IMP port no longer looks for the BRCM header in ingress packets and no longer inserts the BRCM header in egress packets.

Broadcom Tag Format for Egress Packet Transfer

When a packet is forwarded by the switching device to the external CPU for processing, the BRCM tag is formatted as shown in Table 13 and Table 14.

Table 13: Egress Broadcom Tag Format for Opcode = 000 (IMP to CPU)

31–29	*28–16*	*15–8*	*7–5*	*4–0*
Opcode = 000	Reserved = 0x0	REASON_CODE[7:0]	TC[2:0]	SRC_PID[4:0]

Opcode 000 indicates the packet transfer with explicit reasons to help the external CPU to direct the packet for the appropriate packet processing entities as follows:

- REASON_CODE [7:0]

  This indicates the reasons why the packet is forwarded to the external CPU so that the CPU can identify the appropriate software routines for packet processing.
  - Bit [0] indicates mirroring
  - Bit [1] indicates SA learning
  - Bit [2] indicates switching
  - Bit [3] indicates protocol termination
  - Bit [4] indicates protocol snooping
  - Bit [5] indicates flooding/exception processing
  - Bit [6] and Bit[7] are reserved. Default = 0.
- TC [2:0]

  This indicates the traffic class classified by the switching device when forwarding the packet to the CPU.
- SRC_PID [4:0]

  This indicates the ingress port of the switching device where the packet is received.

Table 14: Egress Broadcom Tag Format for Opcode = 001 (IMP to CPU)

63–61	*60–38*	*37*	*36–32*
Opcode = 001	Reserved = 0x0	T/R	T/R_PID[4:0]
31–0			
TIME_STAMP[31:0]			

Opcode 001 indicates a packet transfer with explicit timestamp recorded at the port where it was transmitted or received (indicated by the T/R_PID) for IEEE 802.1AS protocol implementation as follows:

- T/R

  This indicates the type of timestamp recorded through the port (indicated by T/R_PID) for packet:
  - 0 = Received
  - 1 = Transmitted

- T/R_PID[4:0]

  This indicates the port through which the packet was transmitted when T/R = 1, or received when T/R = 0.
- TIME_STAMP [31:0]

  This carries the timestamp value recorded at the port through which the packet was transmitted when T/R = 1 or received when T/R = 0.

Broadcom Tag Format for Ingress Packet Transfer

For packet transfer from the external CPU to the switching device, the BRCM tag is formatted as shown in Table 15 and Table 16.

Table 15: Ingress Broadcom Tag for Opcode = 000 (CPU to IMP)

31–29	*28–26*	*25–24*	*23–0*
Opcode = 000	TC[2:0]	TE[1:0]	Reserved

Opcode 000 indicates that the external CPU is not dictating how the packet is forwarded and the packet is forwarded by the switching device based on the original Ethernet packet information as follows:

- TC [2:0]

  This indicates the traffic class with which the external CPU intends to forward the packet.
- TE (tag enforcement)

  This indicates the 802.1Q/P tagging/untagging encapsulation enforcement for the packet transmission.

  00 = No enforcement (follow VLAN untag mask rules)

  01 = Untag enforcement

  10 = Tag enforcement

  11 = Reserved

Table 16: Ingress Broadcom Tag for Opcode = 001 (CPU to IMP)

31–29	*28–26*	*25–24*	*23*	*22–9*	*8–0*
Opcode = 001	TC[2:0]	TE[1:0]	TS	Reserved	DST_MAP[8:0]

Opcode 001 indicates the packet is forwarded to multiple (or single) egress ports by the switching device based on the explicit direction of the external CPU as follows:

- TC [2:0]

  This indicates the traffic class with which the external CPU intends to forward the packet.
- TE (tag enforcement)

  This indicates the 802.1Q/P tagging/untagging encapsulation enforcement for the packet transmission.

  00 = No enforcement (follow VLAN untag mask rules)

  01 = Untag enforcement

  10 = Tag enforcement

  11 = Reserved

- TS (timestamp request)

  This indicates whether the transmit timestamped at the egress port should be reported back to the external CPU.
- DST_MAP [8:0]

  This indicates the egress port bit map to which the external CPU intends to forward the packet.
  - Bit [8] = Port 8/IMP
  - Bits [5:0] = Ports 5–0

MIB Engine

The MIB engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53101M implement 70-plus MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. As a group, this latter group can be steered selectively to the receive or transmit process on a per-port basis. The section below describes each individual counter.

The BCM53101M offers the MIB snapshot feature per port using the enabled MIB Snapshot Control register. A snapshot of a selected port MIB registers can be captured and available to the users while MIB counters are continuing to count.

If bits [7:6] = 10 of MIB Snapshot Control register, the captured snapshot MIB counters can be read from the Port Snapshot MIB Control register after bit 7 of the MIB Snapshot Control register is cleared to 0. Registers in the Port MIB registers can be read for a live counter.

If bits [7:6] = 11 of MIB Snapshot Control register, the captured snapshot MIB counters can be read from the Port Snapshot MIB Control or Port MIB registers (depending on which port is captured) after bit 7 of the MIB Snapshot Control register is cleared to 0. The live counters cannot be read.

MIB Counters Per Port

The total number of counters per port is 43.

Table 17: Receive-Only Counters

Receive-Only Counters (19)	*Description of Counter*
RxDropPkts (32 bit)	Number of good packets received by a port that were dropped due to a lack of resources (such as lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters.
RxOctets (64 bit)	Number of data bytes received by a port (excluding preamble, but including FCS), including bad packets.

Table 17: Receive-Only Counters (Cont.)

Receive-Only Counters (19)	*Description of Counter*
RxBroadcastPkts (32 bit)	Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed.
RxMulticastPkts (32 bit)	Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed.
RxSAChanges (32 bit)	Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed.
RxUndersizePkts (32 bit)	Number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).
RxOversizePkts (32 bit)	Number of good packets received by a port that are greater than 1522 bytes (tagged) and 1518 bytes (untagged). This counter alone is incremented for packets in the range 1523–1536 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter are incremented for packets of 1537 bytes and higher. The maximum packet size can be programmed.
RxFragments (32 bit)	Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
RxJabbers (32 bit)	Number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.
RxUnicastPkts (32 bit)	Number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed.
RxAlignmentErrors (32 bit)	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes, inclusive, and have a bad FCS with a nonintegral number of bytes.
RxFCSErrors (32 bit)	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets (64 bit)	Total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed.
JumboPktCount (32 bit)	Number of good packets received by a port that are greater than the standard maximum size and less than or equal to the jumbo packet size, regardless of CRC or alignment errors.
RxPausePkts (32 bit)	Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88–08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00–01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.

Table 17: Receive-Only Counters (Cont.)

Receive-Only Counters (19)	*Description of Counter*
RxSymbolErrors (32 bit)	Total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event.
RxDiscard (32 bit)	Number of good packets received by a port that were discarded by the Forwarding Process.
InRangeErrors (32 bit)	Number of packets received with good CRC and one of the following: (1) The value of length/type field is between 46 and 1500 inclusive, and does not match the number of (MAC client data + PAD) data octets received, OR (2) The value of length/type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).
OutOfRangeErrors (32 bit)	Number of packets received with good CRC and the value of length/type field is greater than 1500 and less than 1536.

Table 18: Transmit-Only Counters

Transmit-Only Counters (19)	*Description of Counter*
TxDropPkts (32 bit)	This counter is incremented every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by the TxLateCollision counter.
TxOctets (64 bit)	Total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts (32 bit)	Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts (32 bit)	Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions (32 bit)	Number of collisions experienced by a port during packet transmissions.
TxUnicastPkts (32 bit)	Number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision (32 bit)	Number of packets successfully transmitted by a port that have experienced exactly one collision.
TxMultipleCollision (32 bit)	Number of packets successfully transmitted by a port that have experienced more than one collision.
TxDeferredTransmit (32 bit)	Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. This only applies to the Half Duplex mode, while the Carrier Sensor Busy.
TxLateCollision (32 bit)	Number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxPausePkts (32 bit)	Number of PAUSE events at each port.

Table 18: Transmit-Only Counters (Cont.)

Transmit-Only Counters (19)	*Description of Counter*
TxFrameInDisc (32 bit)	Number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM53101M internal flow-control/buffering scheme has been configured incorrectly.
TXQ0PKT(32 bit)	Total number of good packets transmitted on CoS 0, which is specified in MIB queue select register when QoS is enabled.
TXQ1PKT(32 bit)	Total number of good packets transmitted on CoS 1, which is specified in MIB queue select register when QoS is enabled.
TXQ2PKT(32 bit)	Total number of good packets transmitted on CoS 2, which is specified in MIB queue select register when QoS is enabled.
TXQ3PKT(32 bit)	Total number of good packets transmitted on CoS 3, which is specified in MIB queue select register when QoS is enabled.
TXQ4PKT(32 bit)	Total number of good packets transmitted on CoS 4, which is specified in MIB queue select register when QoS is enabled.
TXQ5PKT(32 bit)	Total number of good packets transmitted on CoS 5, which is specified in MIB queue select register when QoS is enabled.

Table 19: Transmit/Receive Counters

Transmit/Receive Counters (6)	*Description of Counter*
Pkts64Octets (32 bit)	Number of packets (including error packets) that are 64 bytes long.
Pkts65to127Octets (32 bit)	Number of packets (including error packets) that are between 65 and 127 bytes long.
Pkts128to255Octets (32 bit)	Number of packets (including error packets) that are between 128 and 255 bytes long.
Pkts256to511Octets (32 bit)	Number of packets (including error packets) that are between 256 and 511 bytes long.
Pkts512to1023Octets (32 bit)	Number of packets (including error packets) that are between 512 and 1023 bytes long.
Pkts1024toMaxPktOctets (32 bit)	Number of packets that (include error packets) are between 1024 and the standard maximum packet size inclusive.

Table 20 on page 76 identifies the mapping of the BCM53101M MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs that are supported. Direct mappings are defined. However, there are several additional indirectly supported statistics counters that make up the full complement of counters required to support each MIB fully. These are shown in Table 21 on page 78.

Finally, Table 22 on page 79 identifies the additional counters supported by the BCM53101M and references the specific standard or reason for the inclusion of the counter.

Table 20: Directly Supported MIB Counters

BCM53101M MIB	*Ethernet-like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxDropPkts	dot3StatsInternalMACReceiveErrors	dot1dTpPortInDiscards	ifInDiscards	–
RxOctets	–	–	ifInOctets	etherStatsOctets
RxBroadcastPkts	–	–	ifInBroadcastPkts	etherStatsBroadcastPkts
RxMulticastPkts	–	–	ifInMulticastPkts	etherStatsMulticastPkts
RxSAChanges	Note 2	Note 2	Note 2	Note 2
RxUndersizePkts	–	–	–	etherStatsUndersizePkts
RxOversizePkts	dot3StatsFrameTooLongs	–	–	etherStatsOverrsizePkts
RxFragments	–	–	–	eytherStatsFragments
RxJabbers	–	–	–	etherStatsJabbers
RxUnicastPkts	–	–	ifInUcastPkts	–
RxAlignmentErrors	dot3StatsAlignmentErrors	–	–	–
RxFCSErrors	dot3StatsFCSErrors	–	–	–
RxGoodOctets	–	–	–	–
RxExcessSizeDisc	Note 2	Note 2	Note 2	Note 2
RxPausePkts	Note 2	Note 2	Note 2	Note 2
RxSymbolErrors	Note 2	Note 2	Note 2	Note 2
Note 1	–	–	ifInErrors	–
Note 1	–	–	ifInUnknownProtos	–
Note 1	–	dot1dTpPortInFrames	–	–
TxDropPkts	dot3StatsInternalMACTransmitErrors	–	ifOutDiscards	–
TxOctets	–	–	ifOutOctets Note 3	–
Note 1	–	dot1dTpPortOutFrames	–	–
TxBroadcastPkts	–	–	ifOutBroadcastPkts	–
TxMulticastPkts	–	–	ifOutMulticastPkts	–
TxCollisions	–	–	–	etherStatsCollisions
TxUnicastPkts	–	–	ifOutUcastPkts	–
TxSingleCollision	dot3StatsSingleCollisionFrames	–	–	–

Table 20: Directly Supported MIB Counters (Cont.)

BCM53101M MIB	*Ethernet-like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
TxMultipleCollision	dot3StatsMultiple CollisionFrames	–	–	–
TxDeferredTransmit	dot3StatsDeferred Transmissions	–	–	–
TxLateCollision	dot3StatsLate Collision	–	–	–
TxFrameInDisc	Note 2	Note 2	Note 2	Note 2
TxPausePkts	Note 2	Note 2	Note 2	Note 2
Note 4	dot3StatsCarrier SenseErrors	–	–	–
Note 1	–	–	ifOutErrors	–
Pkts64Octets	–	–	–	etherStatsPkt64 Octets
Pkts65to127Octets	–	–	–	etherStatsPkt65to 127Octets
Pkts128to255Octets	–	–	–	etherStatsPkt128to 255Octets
Pkts256to511Octets	–	–	–	etherStatsPkt256to 511Octets
Pkts512to1023Octets	–	–	–	etherStatsPkt512to 1023Octets
Pkts1024toMaxPkt Octets	–	–	–	etherStatsPkt1024to MaxPktOctets
Note 1	–	–	–	etherStatsDrop Events
Note 1	–	–	–	etherStatsPkts
Note 1	–	–	–	etherStatsCRCAlign Errors
Note 4	dot3StatsSQETest Errors	–	–	–

Note 1: Derived by summing two or more of the supported counters. See Table 21 on page 78 for specific details.
Note 2: Extensions required by recent standards developments or BCM53101M operation specifics.
Note 3: The MIB II interfaces specification for ifOutOctets includes preamble/SFD and errored bytes. Because IEEE 802.3-compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets counter maintained by the BCM53101M is consistent with good bytes transmitted, excluding preamble but including FCS. The count can be adjusted to match the ifOutOctets definition more closely by adding the preamble for TxGoodPkts and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.
Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM53101M. These attributes were originally defined to support coax-based AUI transceivers. The BCM53101M integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 (not supported).

Table 21: Indirectly Supported MIB Counters

BCM53101M MIB	*Ethernet-like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers	–	–	ifInErrors	–
	–	–	ifInUnknownProtos	–
RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts	–	dot1dTpPortIn Frames	–	–
DropEvents = RxDropPkts + TxDropPkts	–	–	–	etherStatsDrop Events
RxTotalPkts = RxGoodPkts + RxErrorPkts	–	–	–	etherStatsPkts
RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors	–	–	–	etherStatsCRCAlign Errors
–	dot3StatsSQETest Errors	–	–	–
RxFramesTooLong = RxOversizePkts + RxJabber	dot3StatsFrameToo Longs	–	–	–
TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts	–	dot1dTpPortOut Frames	–	–
TxErrorPkts = TxLateCollision[a]	–	–	ifOutErrors	–

a. The number of packets transmitted from a port that experienced a late collision or excessive collisions. While some media types operate in half-duplex mode, frames that experience carrier sense errors are also summed in this counter. The BCM53101M integrated design means this error condition is eliminated.

Table 22: BCM53101M Supported MIB Extensions

BCM53101M MIB	*Appropriate Standards Reference*
RxSAChanges	IEEE 802.3u Clause 30 — Repeater Port Managed Object Class aSourceAddressChanges
RxExcessSizeDisc	The BCM53101M cannot store packets in excess of 1536 bytes (excluding preamble/SFD, but inclusive of FCS). This counter indicates packets that were discarded by the BCM53101M due to excessive length.
RxPausePkts	IEEE 802.3x Clause 30 — PAUSE Entity Managed Object Class aPAUSEMACCtrlFramesReceived
RxSymbolErrors	IEEE 802.3u Clause 30 — Repeater Port Managed Object Class aSymbolErrorDuringPacket
TxFrameInDisc	Internal diagnostic use for optimization of flow control and buffer allocation algorithm
TxPausePkts	Number of PAUSE events at a given port

Integrated High-Performance Memory

The BCM53101M embeds a 128 KB high-performance SRAM for storing the following:

- Packet data
- The ARL table
- The VLAN table
- The TX queues
- Descriptors

This eliminates the need for external memory and allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves nonblocking performance for stand-alone 5-port applications.

Switch Controller

The core of the BCM53101M device is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store-and-forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully nonblocking solution.

Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see Figure 11). The first level is the TXQ linked list; the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame TC order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to six transmit queues for servicing QoS. All six transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as a linked list and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 2048-byte jumbo frame requires eight buffer tags for handling the frame.

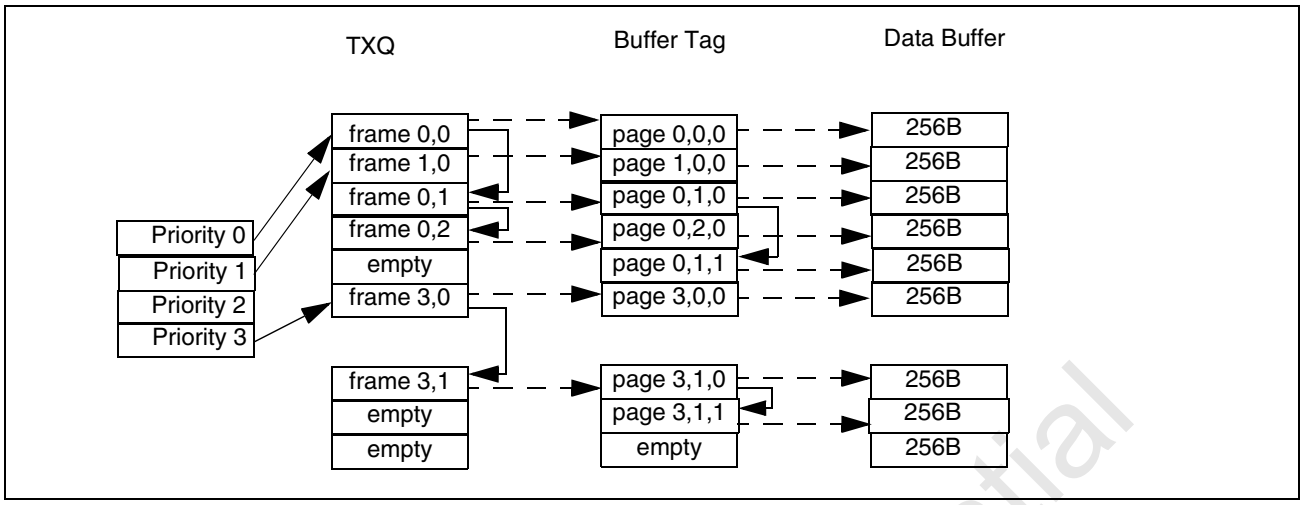


Figure 11: TXQ and Buffer Tag Structure

Section 4: System Interfaces

Overview

The BCM53101M includes the following interfaces:

Copper Interface

The internal PHYs transmit and receive data using the analog copper interface. See the following topics for additional information:

Auto-Negotiation

The BCM53101M negotiates its mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u specification. When the auto-negotiation function is enabled, the BCM53101M automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53101M can be configured to advertise the following modes:

- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD).

Automatic MDI Crossover

During auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53101M internal PHY can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports.

During auto-negotiation, the BCM53101M internal PHY normally transmits on the TD± pin and receives on the RD± pin. When connecting to another device that does not perform MDI crossover, the BCM53101M internal PHY automatically switches its RD±/TD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function. During 100BASE-TX operation, pair swaps automatically occur within the device and do not require user intervention.

10/100BASE-T Forced Mode Auto-MDIX

The Forced Mode Auto-MDIX feature allows the copper auto-negotiation to be disabled in either 10BASE-T or 100BASE-T and still takes advantage of the automatic MDI crossover function. Whenever the forced link is down for at least four seconds, auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100BASE-TX idles are detected. Once detected, the internal PHY returns to the forced mode operation.

Frame Management/WAN Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see "Frame Management" on page 68. The port is configurable to RGMII, MII, RvMII, RMII, TMII, or RvTMII.

BCM53101M also provides one MII/RvMII/RMII/TMII/RvTMII interface for a WAN port or an integrated gateways application.

MII/Reverse MII

The media independent interface (MII) serves as a digital data interface between the BCM53101M and an external 10/100 Mbps management entity. Reverse MII notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 100 Mbps and 10 Mbps for both full-duplex and half-duplex operation. See Figure 12 on page 84 for connection information.

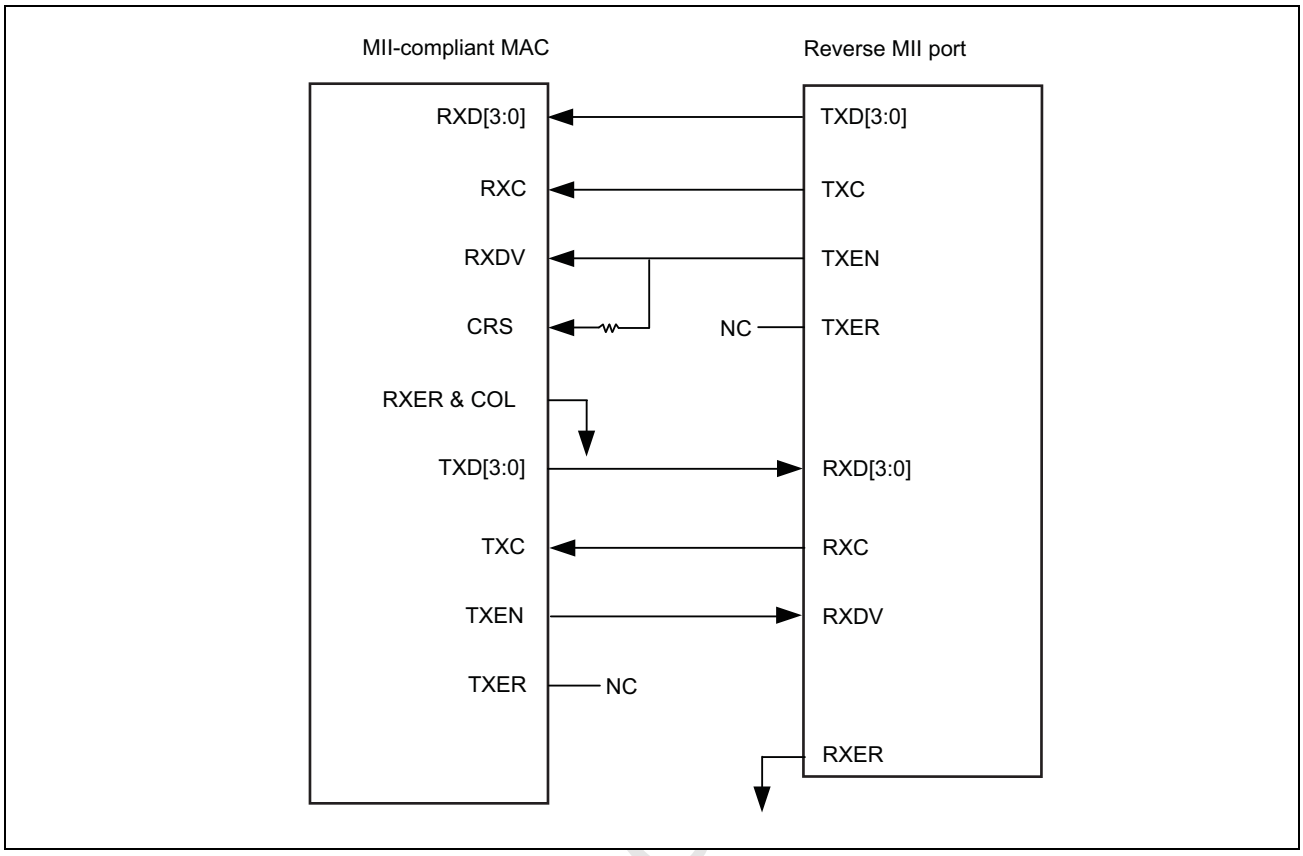


Figure 12: MII/RvMII Port Connection

TMII

The MII interface can be configured to operate at Turbo Mode. In turbo mode, the MII port runs at speeds of up to 50 MHz and sustains transfer rates of up to 200 Mbps.

RMII

The Reduced Media Independent Interface (RMII) serves as a digital data interface between the BCM53101M and an external management entity. Transmit and receive data is clocked on the rising edge of the clocks. The RMII transmits data synchronously using the TXD[1:0] and RXD[1:0] data signals.

RGMII

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM53101M and an external gigabit management entity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits data synchronously using the TXD[3:0] and RXD[3:0] data signals.

Configuration Pins

Initial configuration of the BCM53101M takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration. See "Hardware Signal Definitions" on page 115 for more information.

Programming Interfaces

The BCM53101M can be programmed using the SPI or EEPROM interface. These interfaces share a common pin set that is configured using the CPU_EPROM_SEL strap pin. The "SPI-Compatible Programming Interface" on page 85 provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM53101M register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the "EEPROM Interface" on page 100 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM53101M devices is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is used.

An explanation follows for using the serial interface with an SPI-compatible CPU ("SPI-Compatible Programming Interface" on page 85) or an EEPROM ("EEPROM Interface" on page 100). Either mode can be selected using the CPU_EPROM_SEL strap pin. Either mode has access to the same register space.

SPI-Compatible Programming Interface

One way to access the BCM53101M internal registers is to use the serial peripheral interconnect (SPI) compatible interface. This four-pin interface is designed to support a fully functional, bidirectional Motorola® serial peripheral interface (SPI) for register read/write accesses. The maximum speed of operation is 12.5 MHz. The SPI interface shares pins with the EEPROM interface. To select the SPI interface, pull up or float the CPU_EPROM_SEL pin. (The internal pull-up resistor defaults to SPI interface over EEPROM interface.)

The SPI is a four-pin interface consisting of the following:

- Device select ($\overline{SS}$ = Slave select, input to the BCM53101M)
- Device clock (SCK, which operates at speeds up to 12.5 MHz, input to the BCM53101M)
- Data write line (MOSI = Master Out/Slave In, input to the BCM53101M)
- Data read line (MISO = Master In/Slave Out, output from the BCM53101M)

Note: All the RoboSwitch™ SPI interfaces are designed to operate in slave mode. Therefore, the SCK and SS signals are driven by the external master host device when accessing the BCM53101M registers. For more detailed descriptions, refer to the *Motorola SPI spec MC68HC08AS20-Rev. 4.0*.

$\overline{SS}$: Slave Select

The $\overline{SS}$ signal is used to select a slave device and to indicate the beginning of transmission. The BCM53101M SPI interface operates in the clock phase one (CPHA = 1) transmission format. In this format, the SS signal is driven active low while the SCK signal is high, and remains low throughout the transmission including multiple-byte transfers. The minimum time requirement between $\overline{SS}$ operation is 200 ns.

SCK: Serial Clock

The serial clock SCK maximum operating frequency is 12.5 MHz for the BCM53101M family of devices. The SCK is used to clock data into and out of the Slave ROBO device. The SCK signal is expected to remain high when the interface is idle because the BCM53101M SPI design is based on CPOL = 1 (Clock Polarity = 1). The clock polarity is not programmable on the BCM53101M. The BCM53101M is designed so that data is driven by the falling edge and sampled by the rising edge of the SCK clock. This clock is not a free-running clock: It is generated only during a data transaction and remains high when the clock is idle.

MOSI: Master Output Slave Input

The MOSI signal is used by the master device to transmit the data to the slave device. The data is put on the bus and is expected to be clocked in by a rising edge of the SCK clock signal. This line is used to issue a command and to set the register page and address value of read/write operations.

MISO: Master Input Slave Output

The MISO signal is used by the Slave device to output the data to the master device. The data is put on the bus and is expected to be clocked out by a rising edge of the SCK clock signal. This line is used to transmit the status and the content of the register of read operation.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM53101M. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM53101M slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms determined by the content of the command byte: normal SPI and fast SPI. Figure 13 shows the normal SPI command byte; Figure 14 shows the fast SPI command byte. These two mechanisms should not be mixed in an implementation: The CPU should always initiate transfers consistently with only one of the two mechanisms.

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 13: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 14: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits [7:5]. If bit 4 is a 0, it is a normal SPI command byte and bits [7:5] should be defined as 011b. If bit 4 is a 1, bits [7:5] indicate a fast SPI command byte and bits [7:5] indicate the byte offset into the register that the BCM53101M starts to read from (byte offsets are not supported for write operations).

In command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM53101M operates as a single-chip system, the CHIP ID is 000.

Note: The SS# signal must also be active for any BCM53101M device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits [7:5] of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Noncontiguous blocks are also stored/read through the use of multiple transmissions which allow a new command byte and register base address to be specified. The SS signal must remain low for the entire read or write transaction, as shown in Figure 15 and Figure 16, with the transaction terminated by the deassertion of the SS line by the master.

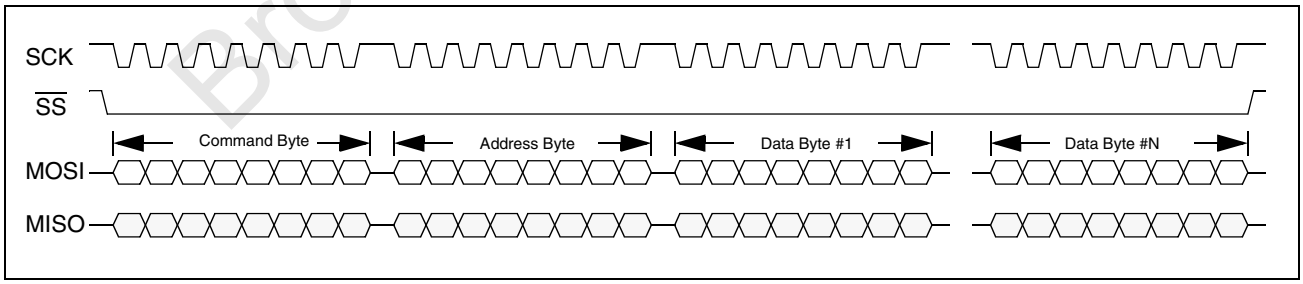


Figure 15: SPI Serial Interface Write Operation

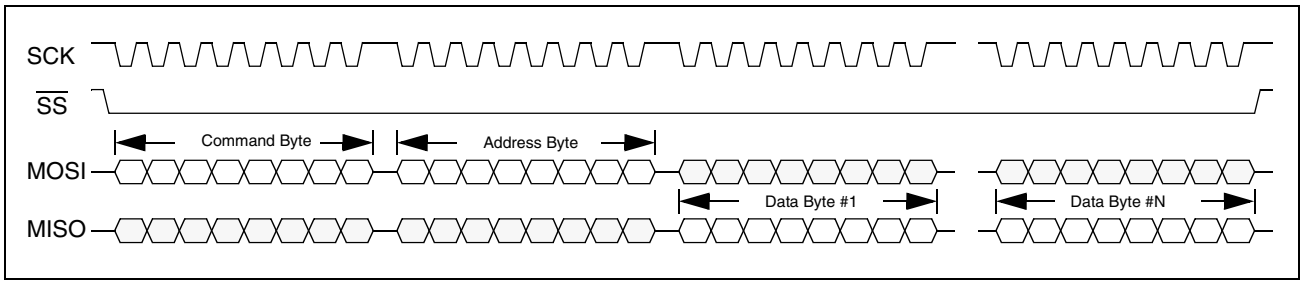


Figure 16: SPI Serial Interface Read Operation

Figure 17 shows the typical connection block diagram for SPI interface with/without external PHY devices.

Without External PHY

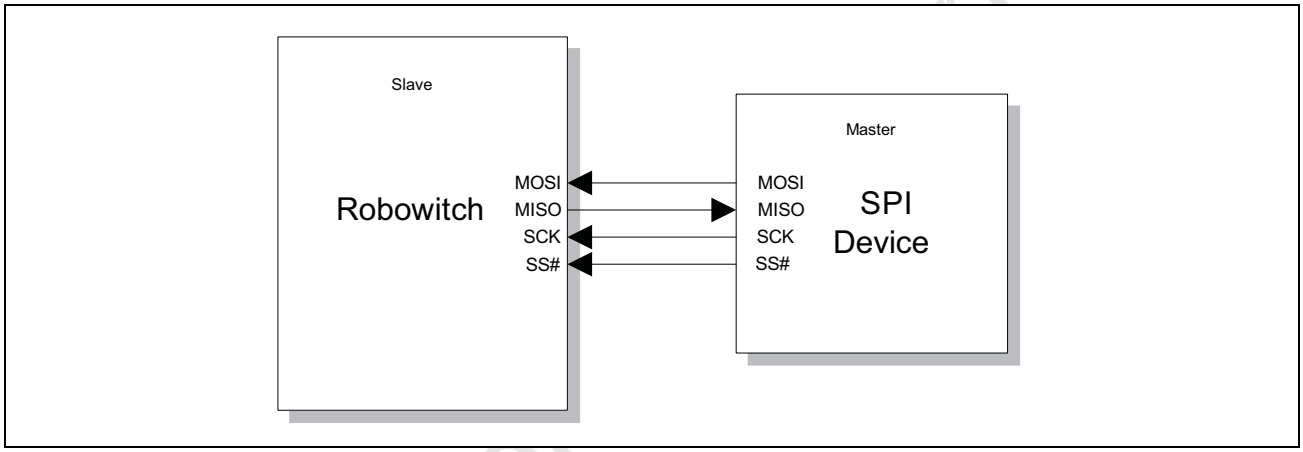


Figure 17: SPI Interface Without External PHY Device

External PHY Registers

The BCM53101M also uses the MDIO/MDC interface for polling registers of an external PHY. In this case, the MDIO/MDC interface polls the external PHY registers pulling the data internal to the BCM53101M. Then, the external PHY registers are retrieved from the register data using the SPI interface. The SPI interface rather than the MDIO/MDC interface is used to access internal PHY registers.

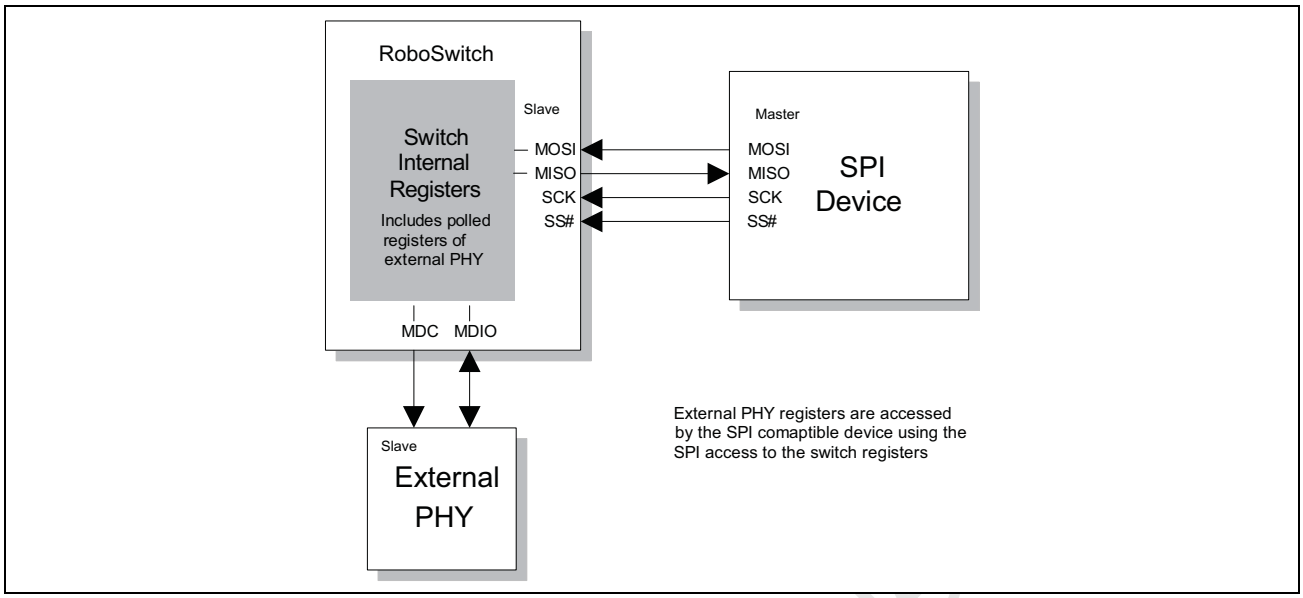


Figure 18: Accessing External PHY Registers

Reading and Writing BCM53101M Registers Using SPI

The BCM53101M internal register read and write operations are executed by issuing a command followed by multiple accesses of the SPI registers in the BCM53101M. There are three SPI interface registers in the BCM53101M that are used by the master device to access the internal switch registers. The SPI interface registers are as follows:

- SPI Page register (page: global, address: FFh): Used to specify the value of the specific register pages.
- SPI Data I/O register (page: global, address: F0h): Used to write and read the specific register's content.
- SPI Status register (page: global, address: FEh): Used to check for an operation completion.
  - Bit 7 = SPIF, SPI read/write complete flag
  - Bit 6 = Reserved
  - Bit 5 = RACK, SPI read data ready acknowledgement
  - Bits [4:3] = Reserved
  - Bit 2 = MDIO_Start, Start/Done MDC/MDIO operation
  - Bit 1 = Reserved
  - Bit 0 = Reserved

The BCM53101M SPI interface supports the following operating modes:

- Normal read mode (see "Normal Read Operation")
- Fast read mode (see "Fast Read Operation" on page 94)
- Normal write mode (see "Normal Write Operation" on page 97)

Note: The RoboSwitch family does not support fast-write mode.

Normal Read Operation

A normal write operation consists of five transactions (five $\overline{SS}$ operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine whether the operation can start.
2. Issue a normal write command (opcode = 0x61) to write the register page value into the SPI Page register 0xFF.
3. Issue a normal read command (opcode = 0x60) to setup the required RoboSwitch register address.
4. Issue a normal read command (opcode = 0x60) to poll the RACK bit in the SPI status register(0xFE) to determine the completion of read (register content gets loaded in SPI Data I/O register).
5. Issue a normal read command (opcode = 0x60) to read the specific registers' content placed in the SPI Data I/O register (0xF0).

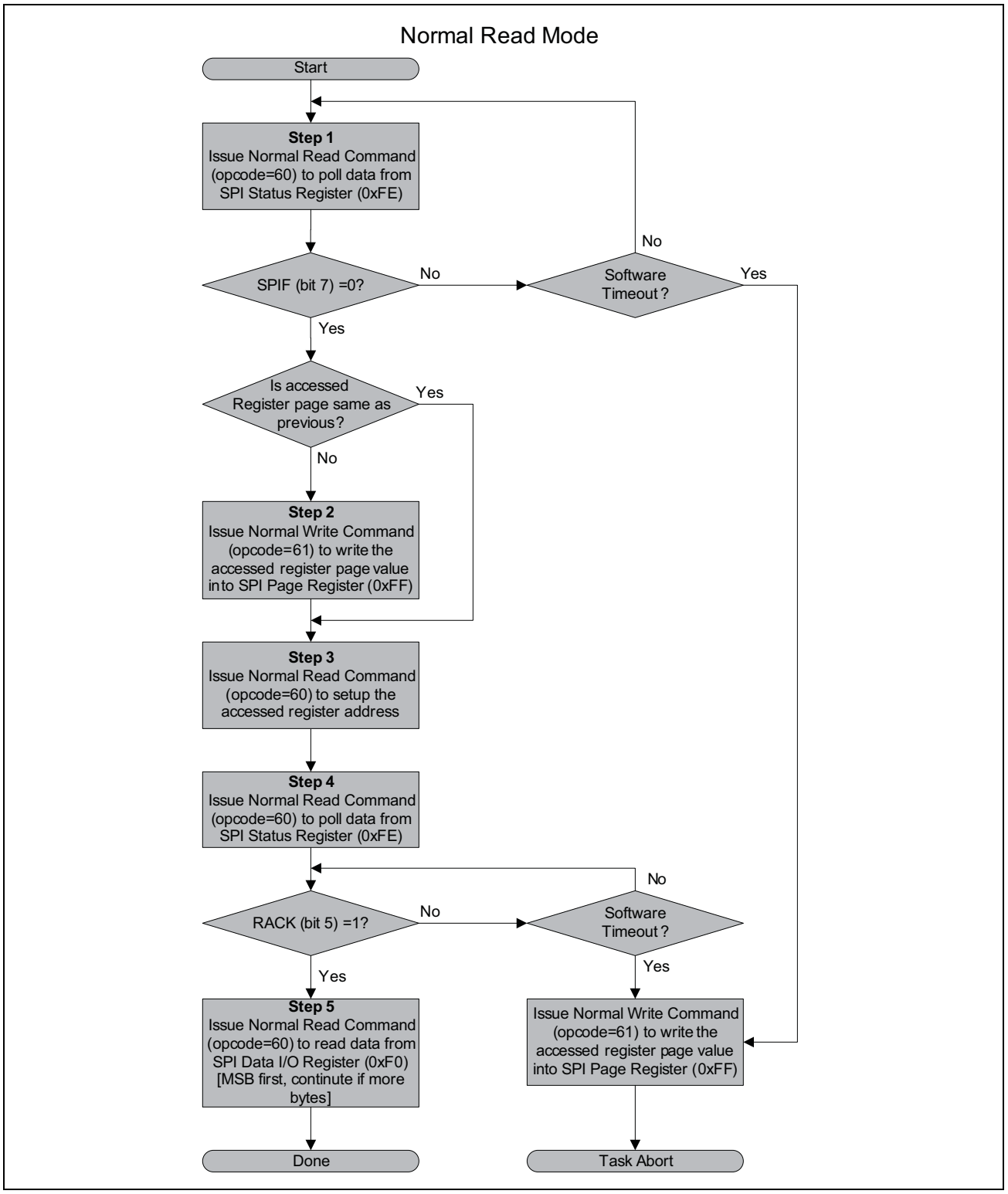


Figure 19: Normal Read Operation

Example: Read from 1000BASE-T Control register (page 10h, offset 12h).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a normal read command byte = 0 1 1 0 0 0 0 0 (opcode = 0x60)
   - Clock in the SPI Status register address (0xFE)
   - Clock out the SPI Status register value = 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
   - Deassert $\overline{SS}$ while SCK is high idle state

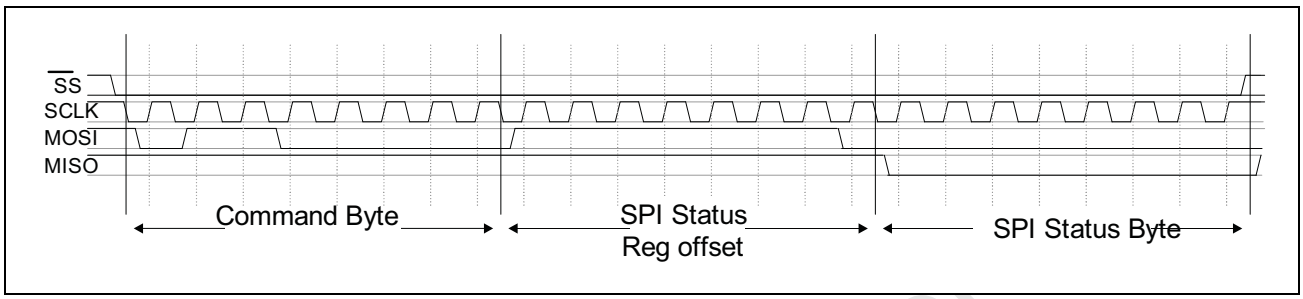


Figure 20: Normal Read Mode to Check the SPIF Bit of SPI Status Register

2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI page register (0xFF) —this step is required only if previous read/write was not to/from Page 10h.
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a normal write command byte = 0 1 1 0 0 0 0 1 (opcode = 0x61)
   - Clock in offset of Page register (0xFF)
   - Clock in the accessed register page value = 0 0 0 1 0 0 0 0 (page register = 0x10)
   - Deassert $\overline{SS}$ while SCK is high idle state

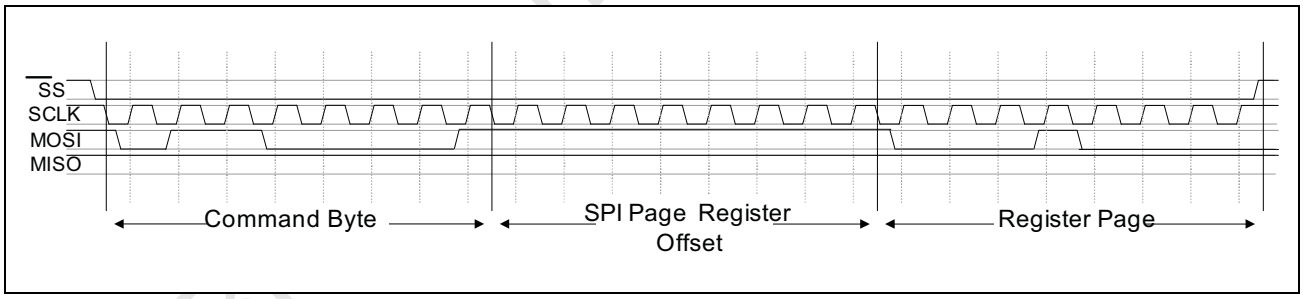


Figure 21: Normal Read Mode to Setup the Accessed Register Page Value

3. Issue a normal read command (opcode = 0x60) and write the accessed register address value 0x12, and clock out 8 bits to complete the read cycle, but discard result (this is where the state machine triggers a internal data transfer from Address 0x12 to the SPI Data I/O register)
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a normal read command byte = 0 1 1 0 0 0 0 0 (opcode = 0x60)
   - Clock in the address of accessed register address value (0x12)
   - Clock out eight clocks for the dummy read, and discard results on MISO
   - Deassert $\overline{SS}$ while SCK is high idle state

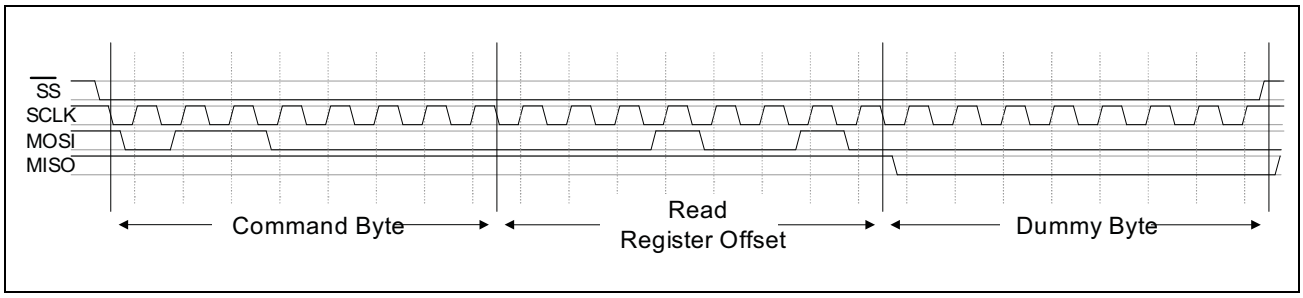


Figure 22: Normal Read Mode to Set Up the Accessed Register Address Value (Dummy Read)

Note: This dummy read is always eight clock cycles, whether or not it is an 8-bit register.

4. Issue a normal read command (opcode = 0x60) to read the SPI Status to check the RACK bit for completion of the register content transfer to the SPI Data I/O register.(this step may be repeated until the proper bit set is read.)
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a normal read command byte = 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in offset for SPI Status register (0xFE) = 1 1 1 1 1 1 1 0
- Clock out the content of SPI Status bits
- Repeat the polling until the content of SPI Status register value = 0 0 1 0 0 0 0 0 (RACK bit 5= 1)
- Deassert $\overline{SS}$ while SCK is high idle state

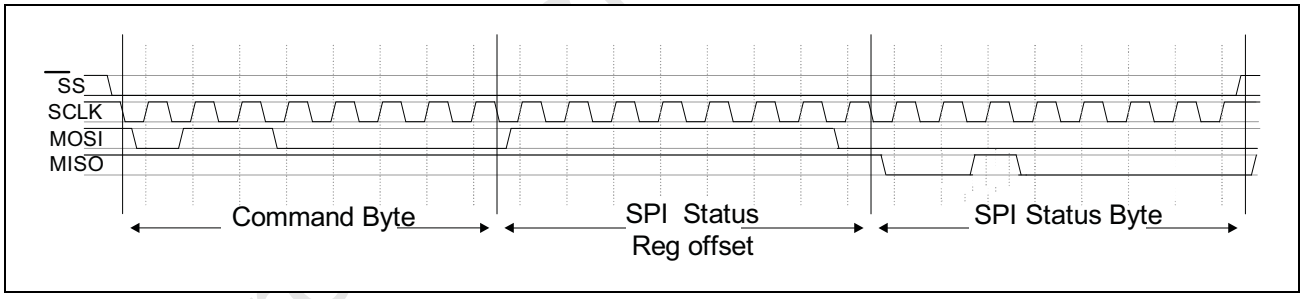


Figure 23: Normal Read Mode to Check the SPI Status for Completion of Read

5. Issue a normal read command (opcode = 0x60) to read the data from the SPI Data I/O register:
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in Command Byte = 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in offset of SPI Data I/O Register (0xF0)
- Clock out first data byte on MISO line = 0 0 0 0 0 0 0 0 (byte 0 = bit 7 to bit 0 = MSB to LSB)
- Clock out next byte (in this case, last) on MISO line = 0 0 0 0 1 1 1 0 (byte 1 = bit 15 to bit 8)
- [Continue if more bytes]
- Deassert $\overline{SS}$ while SCK is high idle state

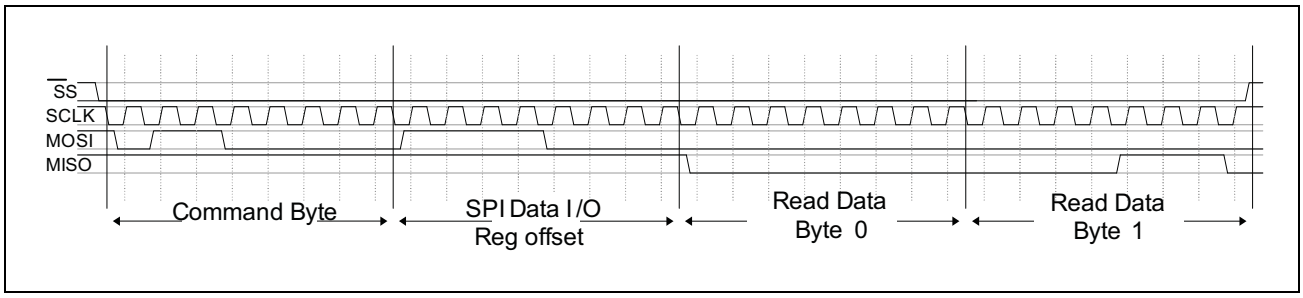


Figure 24: Normal Read Mode to Obtain the Register Content

Fast Read Operation

Fast read operation consists of three transactions (three $\overline{SS}$ operations)

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status Register (0xFE) to determine the operation can start.
2. Issue a fast read command (opcode = 0x10) to setup the accessed Register Page value into the Page register (0xFF).
3. Issue a fast read command (opcode = 0x10) to setup the accessed register address value, to trigger an actual read, and retrieve the accessed register content till the completion

The fast read mode process is different from the normal read mode: Once the switch receives a fast read command followed by the register page and address information, the status and the data (register content) is put on the MISO line without going through the SPI Status register or the SPI Data I/O register. Once the RACK bit of the bytes following the fast read command with address information is recognized, the register content is put on the MISO line immediately following the byte with the RACK bit set. The fast read process is described in the following paragraphs with a flowchart followed by a step-by-step description.

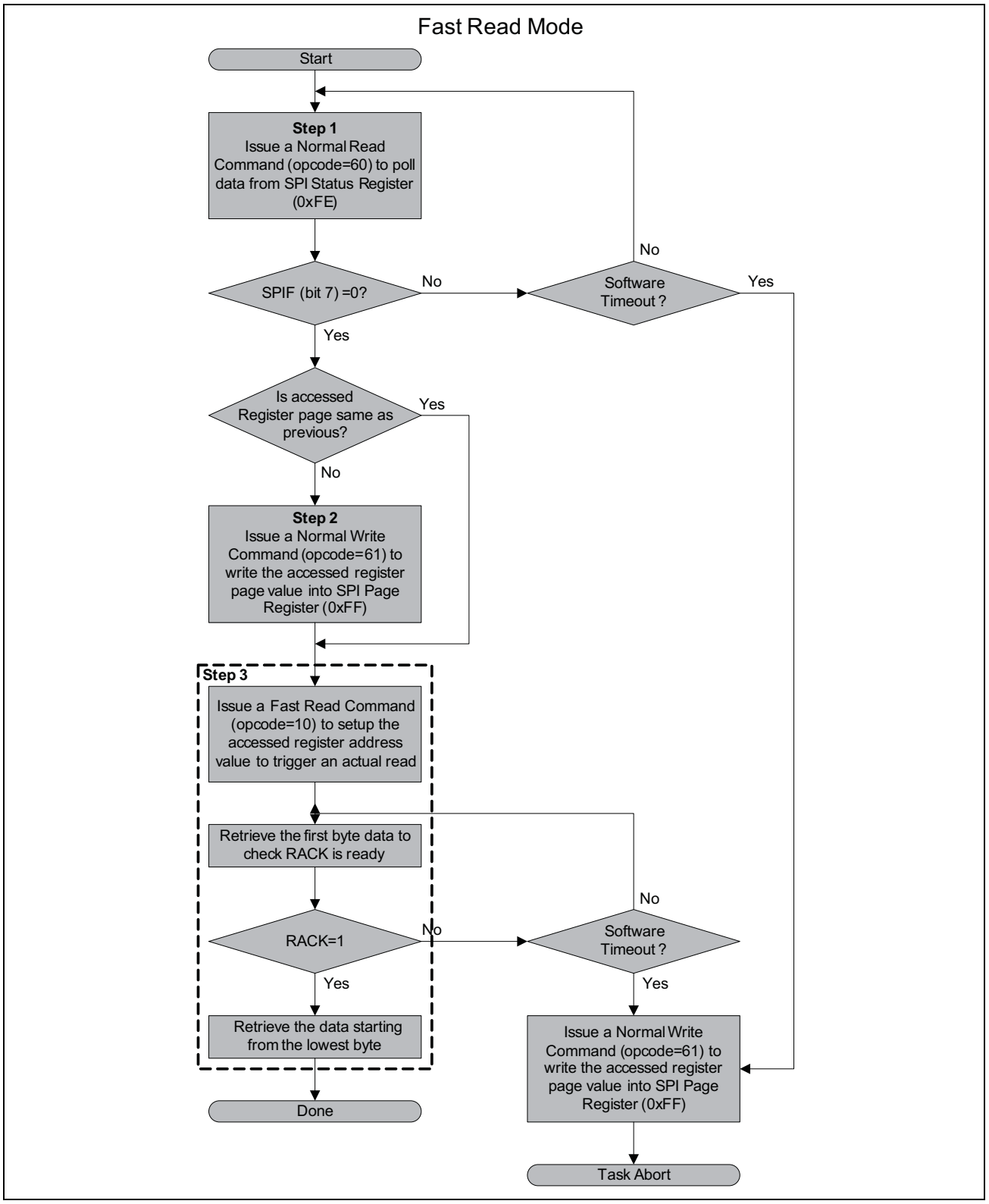


Figure 25: Fast Read Operation

Example: Read from 1000BASE-T Control register (page 10h, offset 12h).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a normal read command byte = 0 1 1 0 0 0 0 0(opcode = 0x60)
- Clock in the SPI Status register address (0xFE)
- Clock in the accessed register page value = 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
- Deassert $\overline{SS}$ while SCK is high idle state

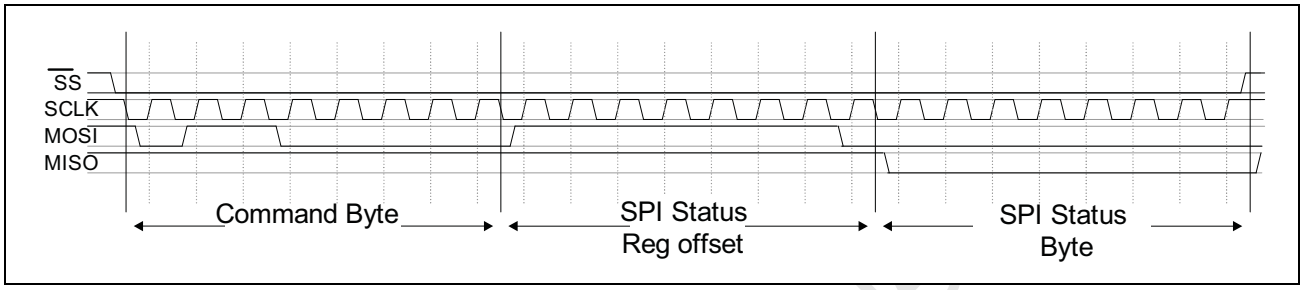


Figure 26: Normal Read Mode to Check the SPIF Bit of SPI Status Register

2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into the SPI Page register (0xFF)—this step is required only if previous read/write was not to/from Page 10h.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Fast Read Command Byte = 0 11 0 0 0 0 0 1 (opcode = 0x61)
- Clock in offset of Page register (0xFF)
- Clock in the accessed register page value = 0 0 0 1 0 0 0 0 (page register = 0x10)
- Deassert $\overline{SS}$ while SCK is high idle state

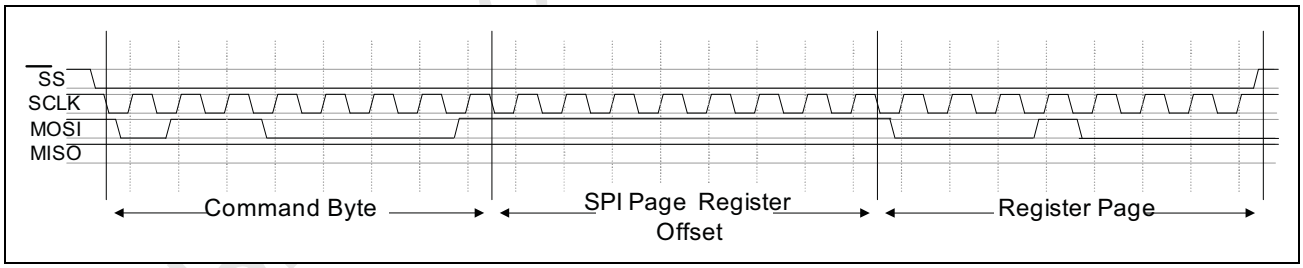


Figure 27: Fast Read Mode to Set Up New Page Value

3. Issue a fast read command (opcode = 0x10), followed by the address of the accessed register (0x12), check for a read completion by checking the RACK bit in the SPI Status register, and finally clock out the read data.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Fast Read Command Byte = 0 0 0 1 0 0 0 0 0 (opcode = 0x10)
- Clock in the Address of accessed register (0x12)
- Clock out Bytes Until Bit 0 or Bit 1 = 1 = 0 0 0 0 0 0 0 1 (RACK bit 0=1)
- Clock out first data byte = 0 0 0 0 0 0 0 0 (byte 0 = bit 7 to bit 0)

– Clock out next data (in this case, last) byte = 0 0 0 0 1 1 1 0 (byte 1 = bit 15 to bit 8)
– [Continue if more bytes]
– Deassert $\overline{SS}$ while SCK is high idle state

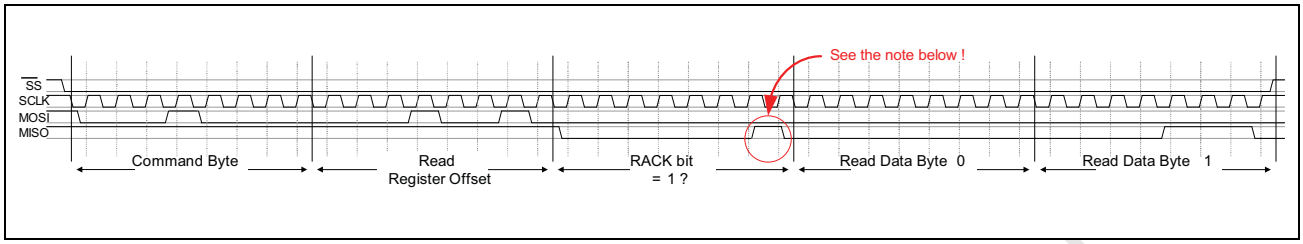


Figure 28: Fast Read to Read the Register

Note: There is an errata on the RACK output timing in fast read mode. The RACK (bit 0) must be sampled prior to toggling the clock to shift out the bit 0.

Normal Write Operation

A normal write operation consists of three transactions (three $\overline{SS}$ operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a normal write command (opcode = 0x61) to setup the accessed register page value into the page register (0xFF).
3. Issue a normal write command (opcode = 0x61) to setup the accessed register address value, followed by the write content starting from a lower byte.

The normal write mode process is described in the following paragraphs with a flowchart followed by a step-by-step description.

Note: The RoboSwitch does not support fast write mode.

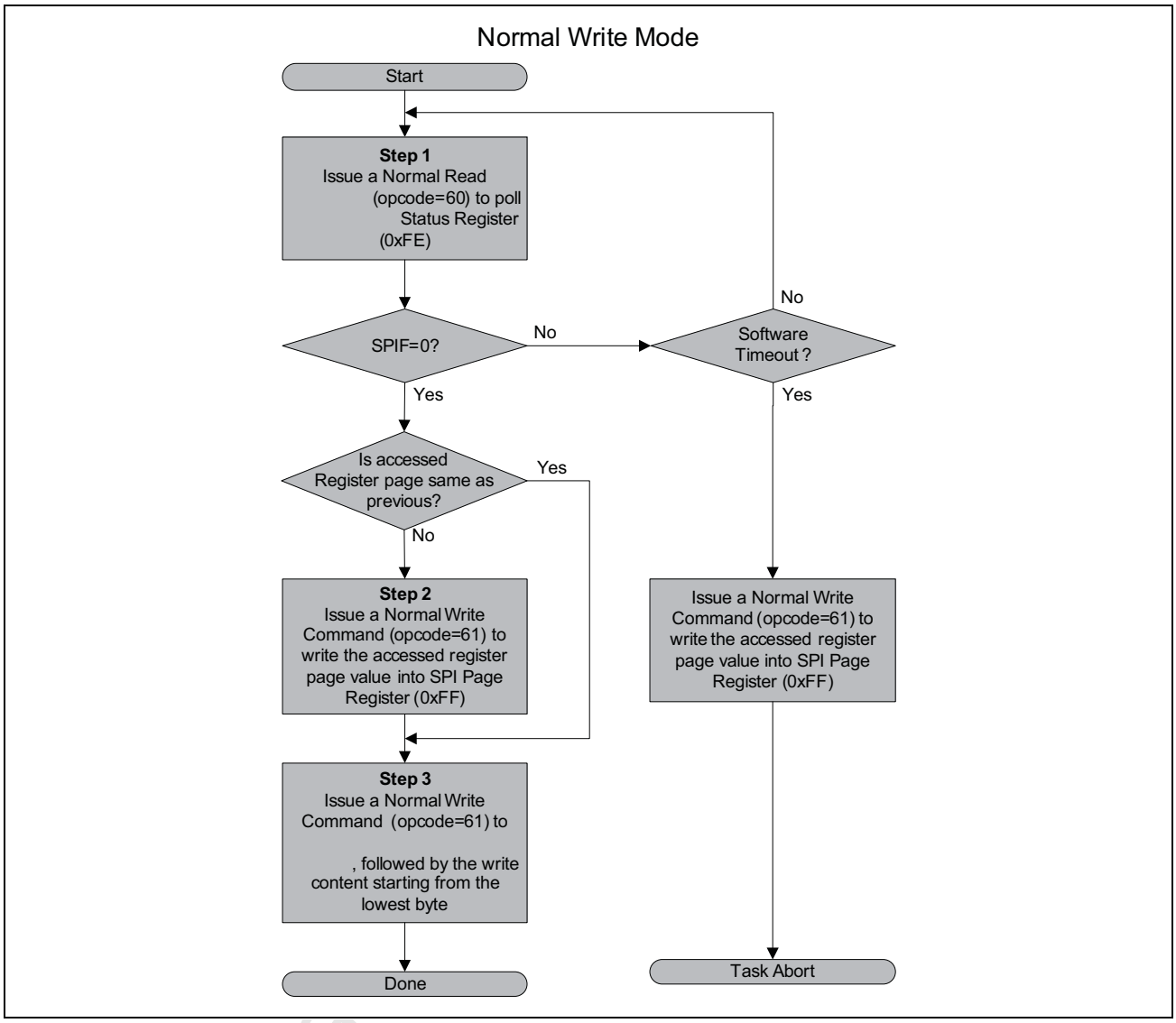


Figure 29: Normal Write Operation

Example: 0x1600h is written to 1000BASE-T Control register (page 0x10, offset 0x12).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a normal read command byte = 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in the SPI Status register address (0xFE)
- Clock in the accessed register page value = 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
- Deassert $\overline{SS}$ while SCK is high idle state

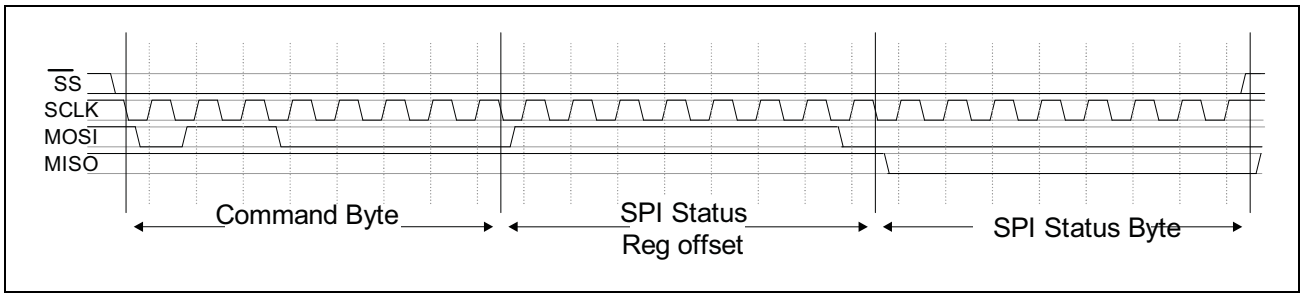


Figure 30: Normal Read Mode to Check the SPIF Bit of SPI Status Register

2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI Page register (0xFF)—this step is required only if previous read/write was not from/to Page 0x10.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a normal write command byte = 0 1 1 0 0 0 0 1 (opcode = 0x61)
- Clock in offset of Page register (0xFF)
- Clock in 1 byte of the accessed register page value (page register 0x10)
- Deassert $\overline{SS}$ while SCK is high idle state

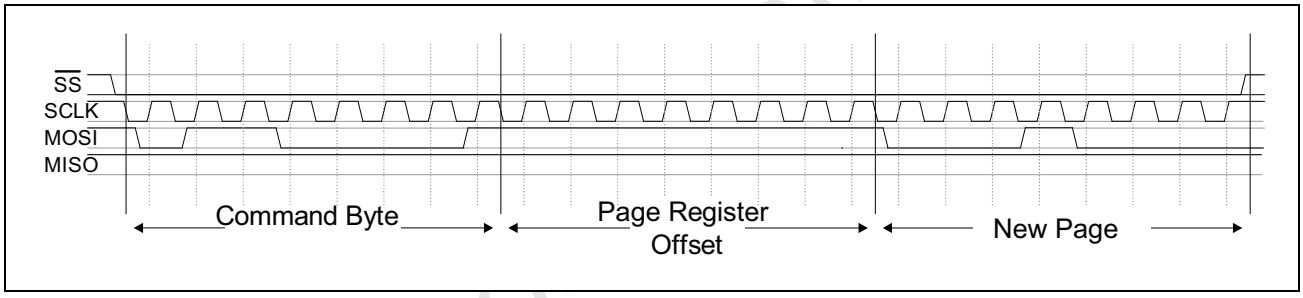


Figure 31: Normal Write to Set Up the Register Page Value

3. Issue a normal write command (opcode = 0x61) and write the address of the accessed register followed by the write content starting from a lower byte.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a normal write command byte = 0 1 1 0 0 0 0 1 (opcode = 0x61)
- Clock in Offset of Address of accessed register (0x12)
- Clock in lower data byte first = 0 0 0 0 0 0 0 0 (byte 0 = bit 7 to bit 0)
- Clock in upper data byte next = 0 0 0 1 0 1 1 0 (byte 1 = bit 15 to bit 8)
- [Continue if more bytes]
- Deassert $\overline{SS}$ while SCK is high idle state

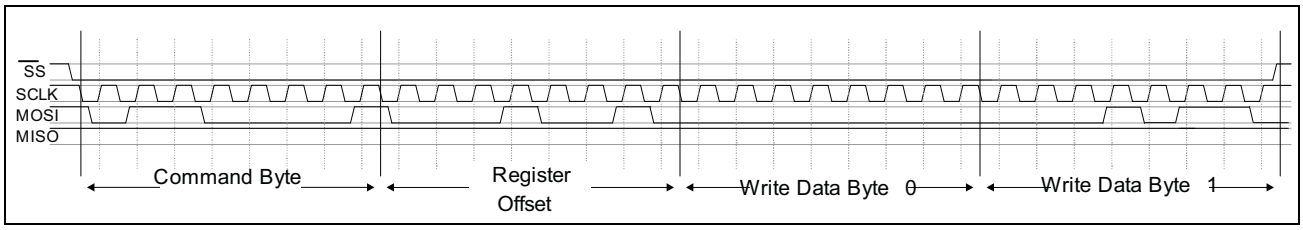


Figure 32: Normal Write to Write the Register Address Followed by Written Data

EEPROM Interface

The BCM53101M can be connected using the serial interface to a low-cost external serial EEPROM, enabling it to download register-programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

During the chip-initialization phase, the data is read-in from the EEPROM sequentially after the internal memory has been cleared. The first data read in is the header and it matches a predefined magic code. In the case where the header data does not match the instruction fetch, the process stops and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the header.

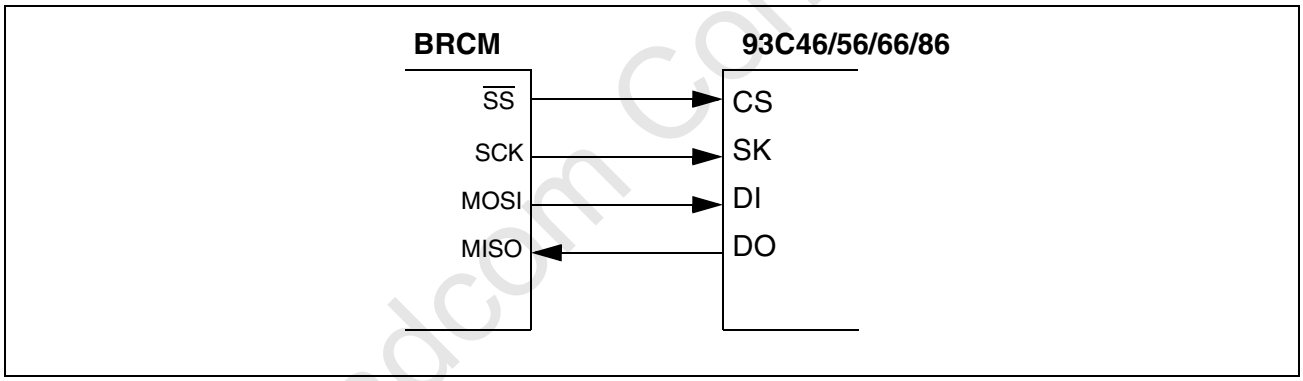


Figure 33: Serial EEPROM Connection

EEPROM Format

The EEPROM should be configured to x16 word format. The header contains key and length information as shown in Table 23 on page 101. The actual data stored in the EEPROM is byte-swapped as shown in Table 24 on page 101.

- Upper 5 bits are magic code 15h, which indicates that valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speedup. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words

– 93C86 up to 1024 words

Table 23: EEPROM Header Format

Bits [15:11}	***Bit 10***	***Bits [9:0]***
Magic code, 15h	Speed	Total entry number 93C46 = 0–63 93C56 = 0–127 93C66 = 0–255 93C86 = 0–1023

Table 24: EEPROM Contents

Bits [7:0]	***Bits [15:11]***	***Bit 10***	***Bits [9:8]***
Total entry number	Magic code, 15h	Speed	Total entry number

Figure 34 shows an EEPROM programming example.

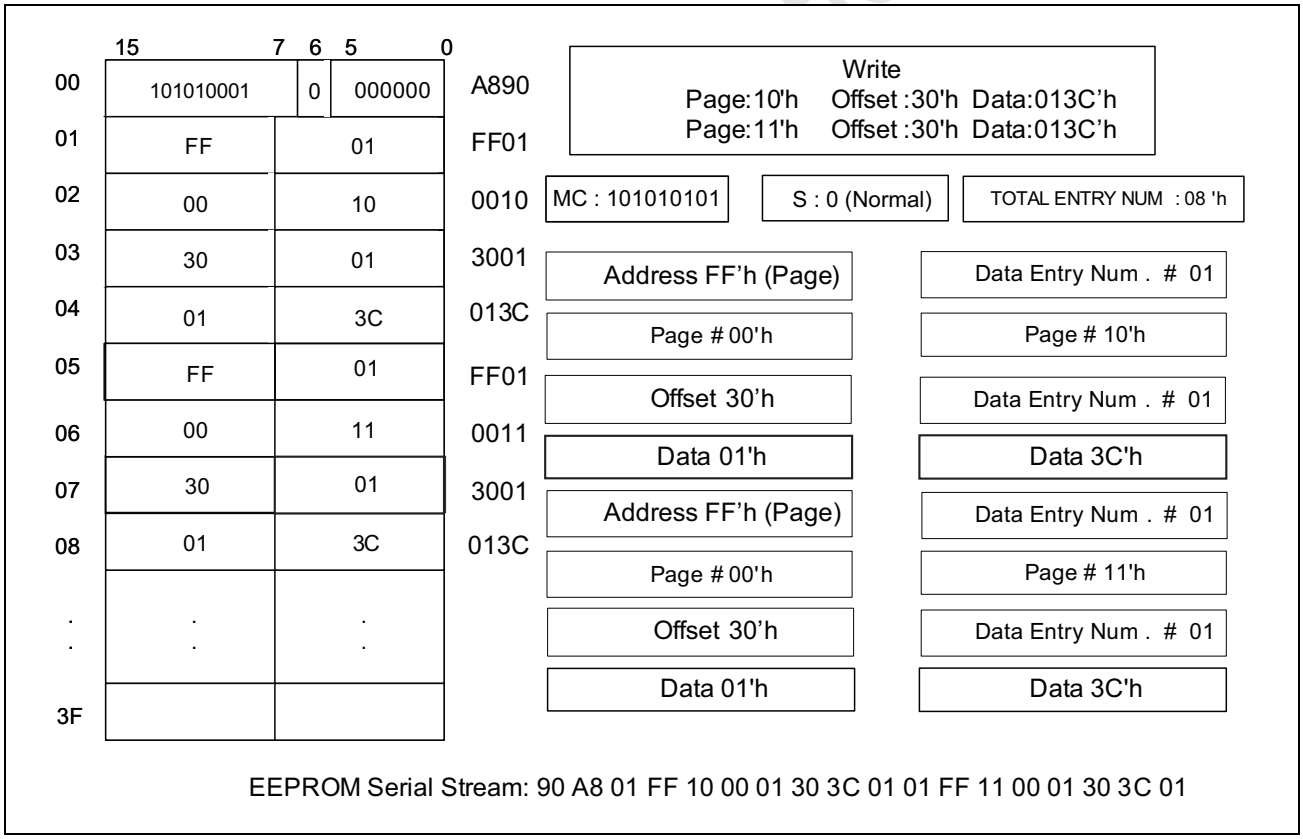


Figure 34: EEPROM Programming Example

MDC/MDIO Interface

The BCM53101M offers an MDC/MDIO interface for accessing the switch registers as well as the PHY registers. An external management entity can access the switch registers through this interface when the SPI interface is not used (that is, when the SPI clock is in idle mode). The switch registers are accessed through the pseudo-PHY interface; the PHY registers are accessed directly using PHY addresses.

Each internal transceiver in the BCM53101M is assigned a unique hardware PHY address.

Transceiver 0 has address 00000. Transceivers 1–4 have addresses 1 through 4h, respectively.

Each internal PHY checks that the PHY address of the initiated command matches its own address before executing the command.

The external PHY can be connected to the GMII interface of the IMP port. The external PHY MII registers can be accessed through the SPI interface by accessing page 88h. The actual PHY address can be assigned using the MDIO IMP PORT Address register.

Note: The PHY registers are not accessible using the pseudo-PHY operation.

MDC/MDIO Interface Register Programming

The BCM53101M is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM53101M sources a 2.5 MHz clock. Serial bidirectional data transmitted using the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM53101M and contains the following:

- **Preamble (PRE)**. To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- **Start of Frame** (**ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code** (**OP)**. A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address** (**PHYAD)**. A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address** (**REGAD)**. A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround** (**TA).** The next bit-times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM53101M chip during these two bit-times. When a read operation is being performed, the MDIO pin of the BCM53101M must be put in a high-impedance state during these bit-times. The external PHY drives the MDIO pin to 0 during the second bit-time.
- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM53101M. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Master

Each serial port of the BCM53101M is assigned a unique PHY address. The address by default is set to ascending order.

Pseudo-PHY

Note: Pseudo-PHY mode requires the SPI interface to be enabled (CPU_EEPROM_SEL=1) to function properly.

The MDC/MDIO can be used by an external management entity to read/write register values internal to the BCM53101M. This mode offers an alternative programming interface to the chip. The BCM53101M operates in slave mode with a PHY address of 30d. The following figures show the register setup flowchart for accessing the registers using the MDC/MDIO interface.

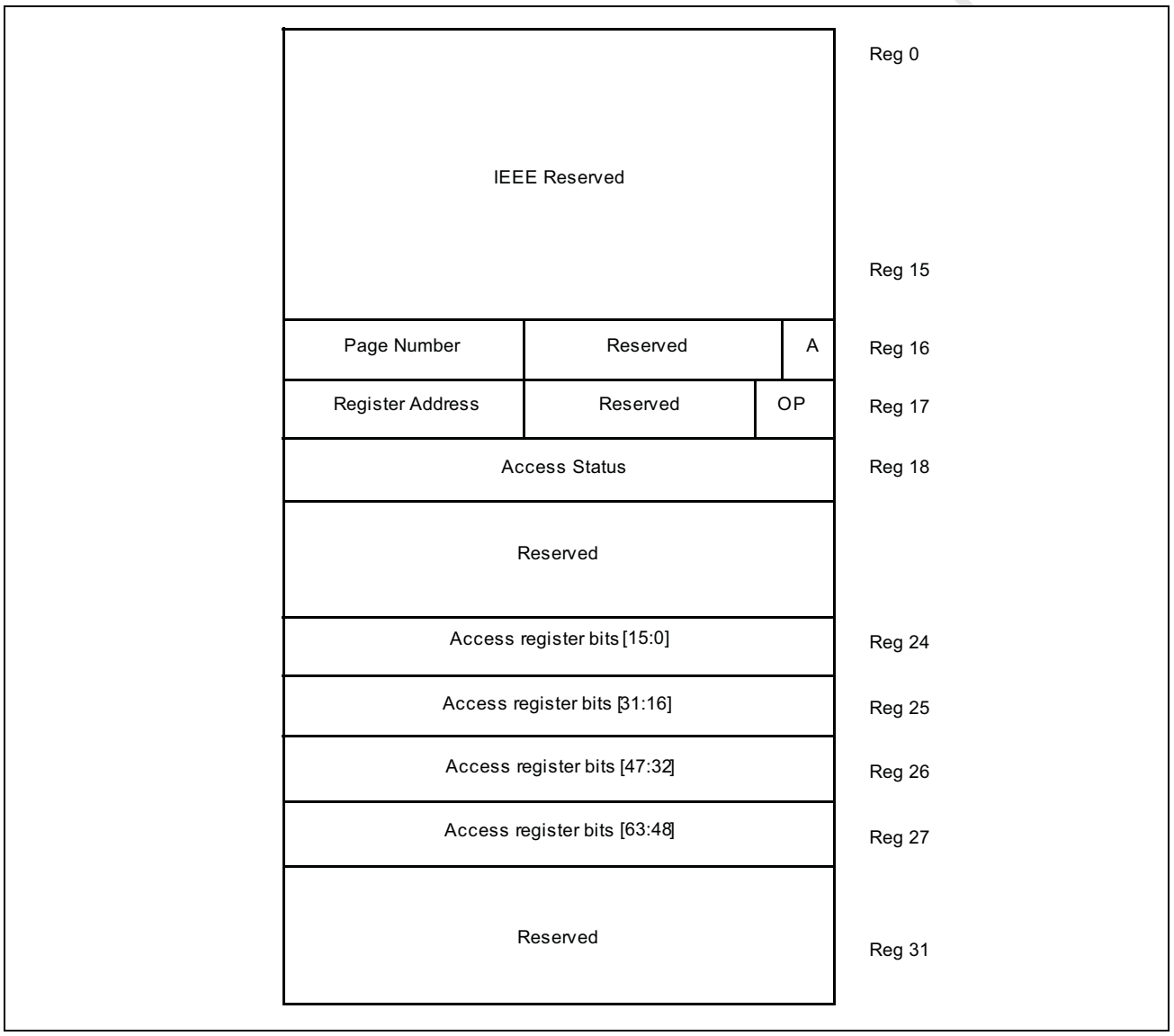


Figure 35: Pseudo-PHY MII Register Definitions

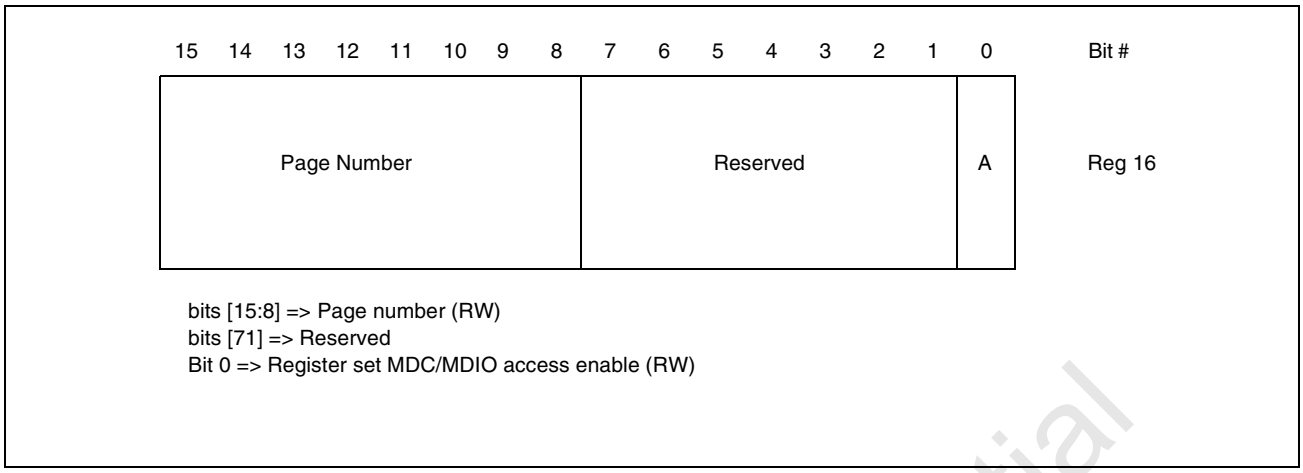


Figure 36: Pseudo-PHY MII Register 16: Register Set Access Control Bit Definition

Note: The bit 0 (MDC/MDIO Access Enable) in register 16 should be released (set to 0) after a transaction is completed. This allows the SPI interface to access the switch register if required.

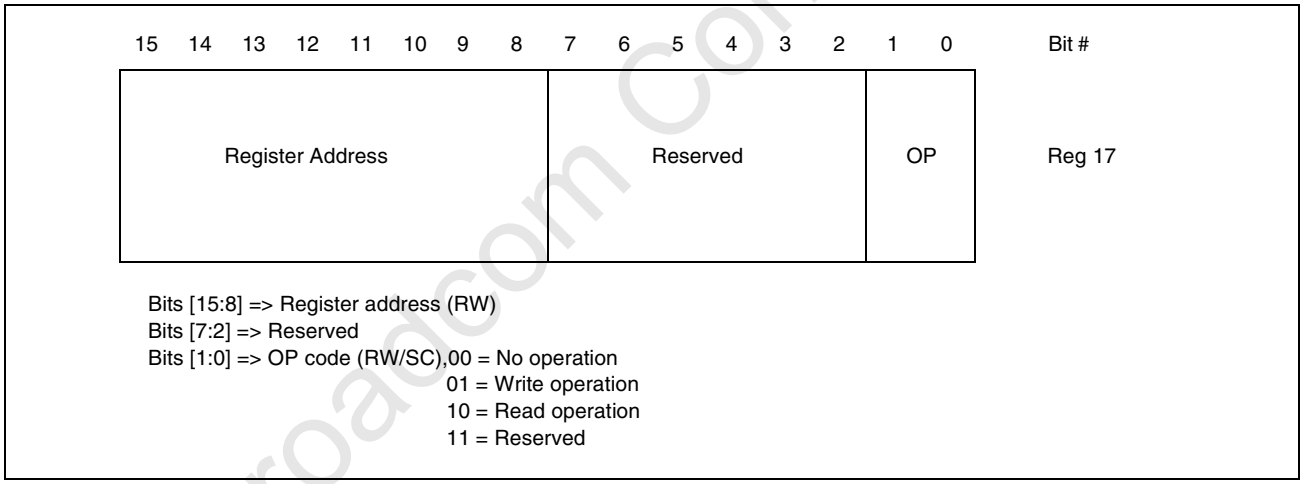


Figure 37: Pseudo-PHY MII Register 17: Register Set Read/Write Control Bit Definition

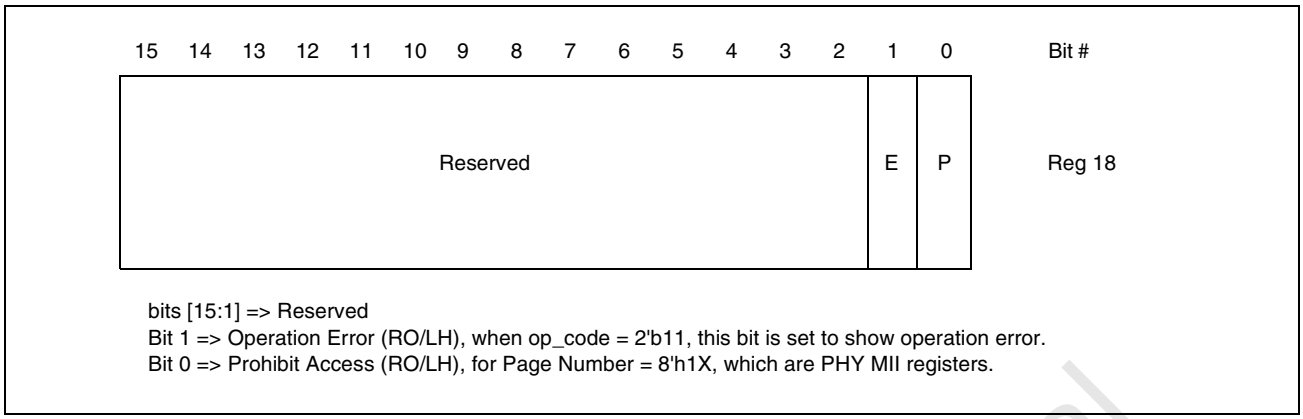


Figure 38: Pseudo-PHY MII Register 18: Register Access Status Bit Definition

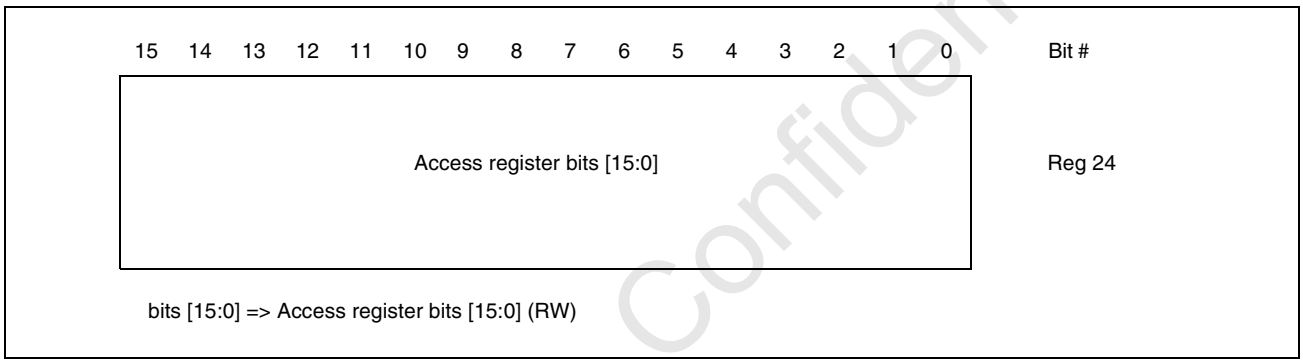


Figure 39: Pseudo-PHY MII Register 24: Access Register Bit Definition

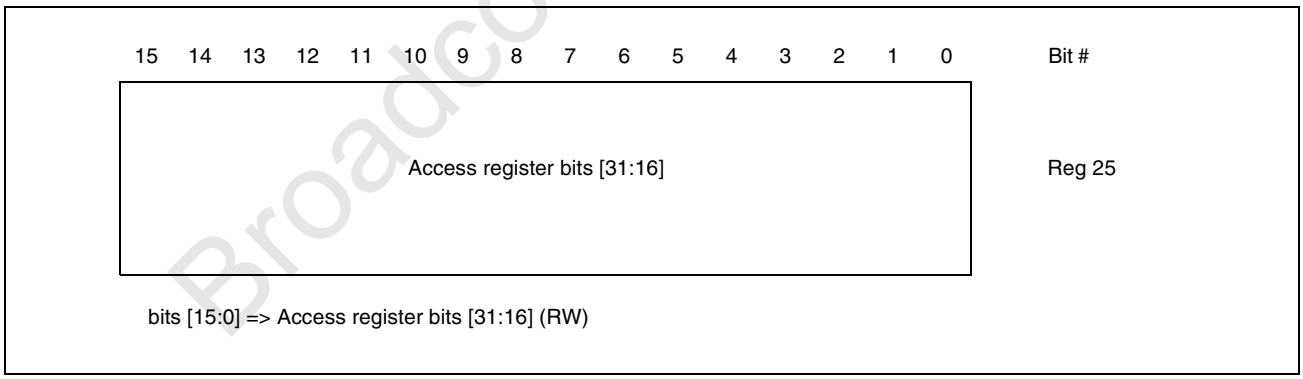


Figure 40: Pseudo-PHY MII Register 25: Access Register Bit Definition

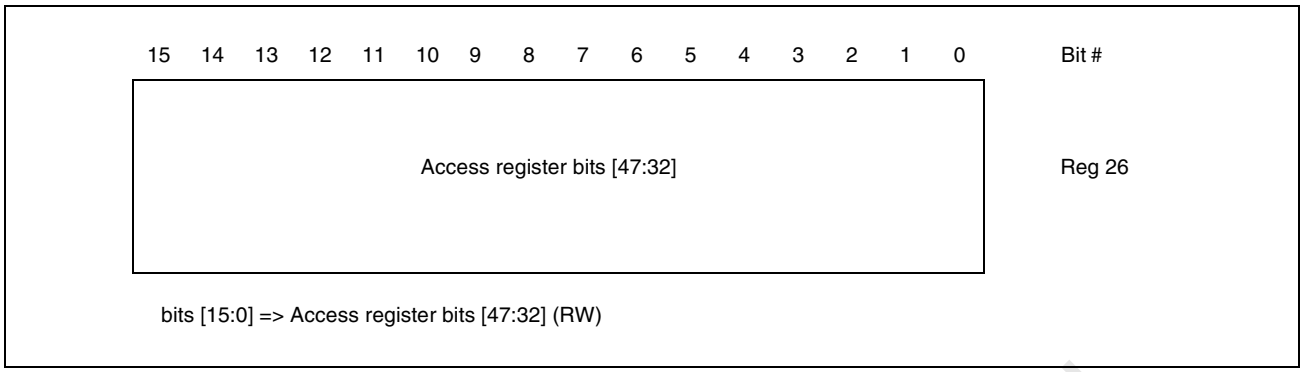


Figure 41: Pseudo-PHY MII Register 26: Access Register Bit Definition

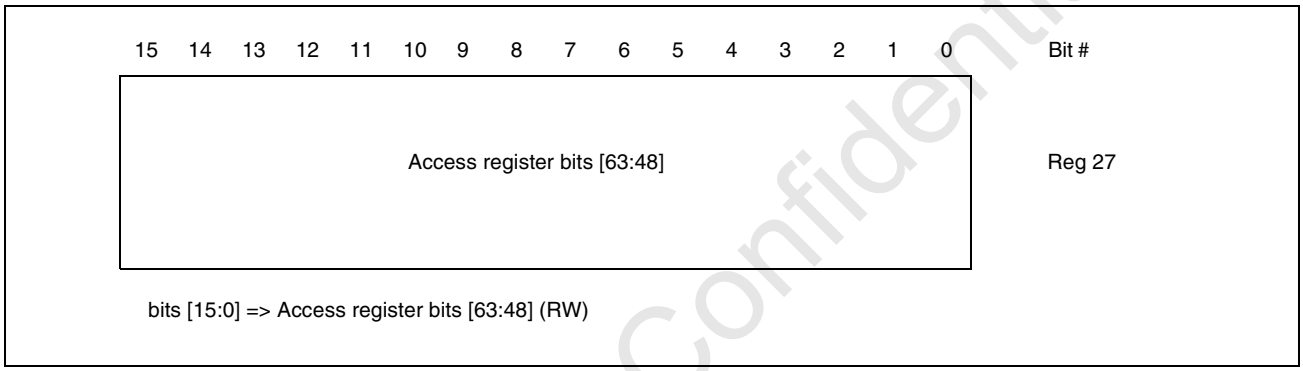


Figure 42: Pseudo-PHY MII Register 27: Access Register Bit Definition

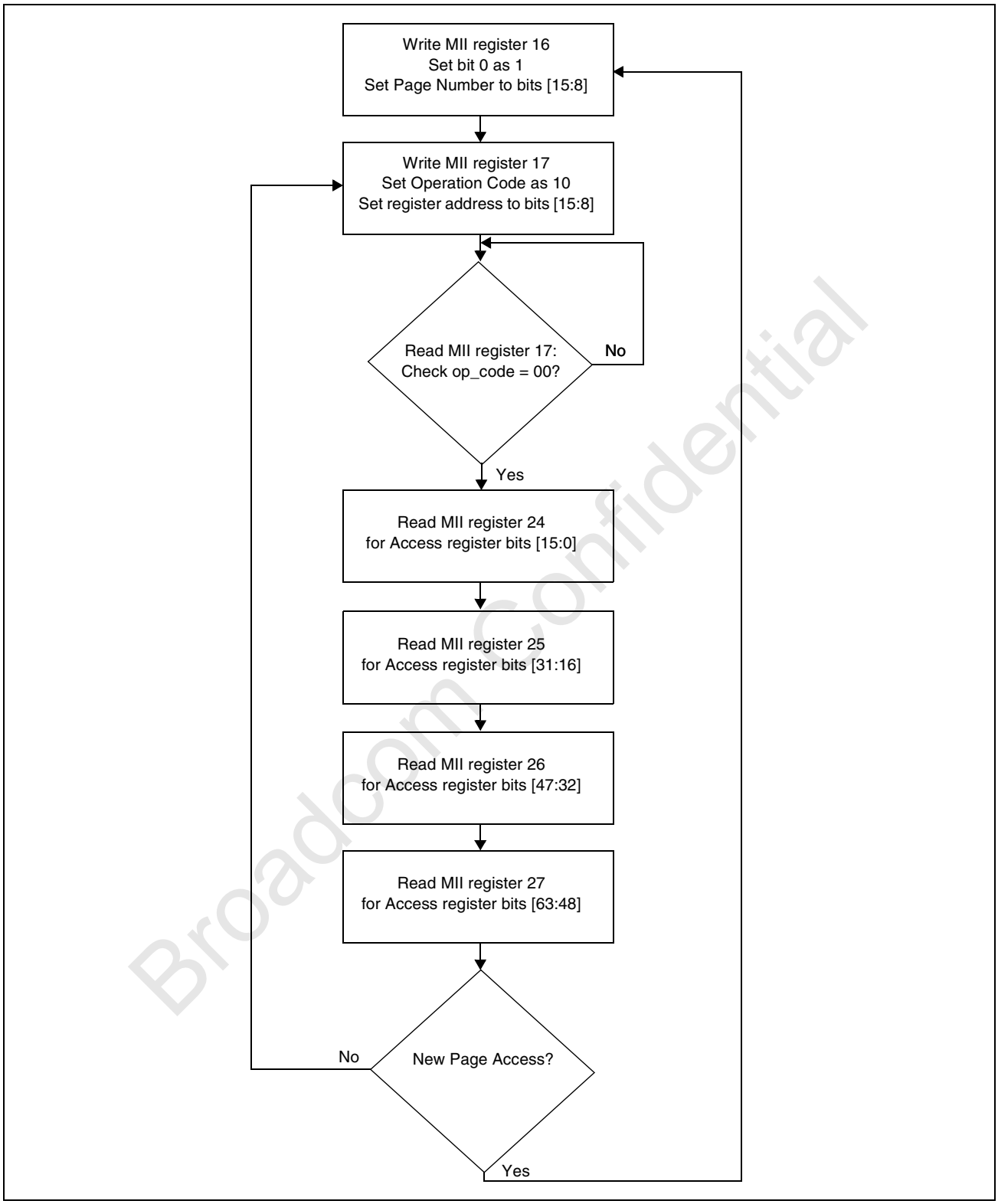


Figure 43: Read Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

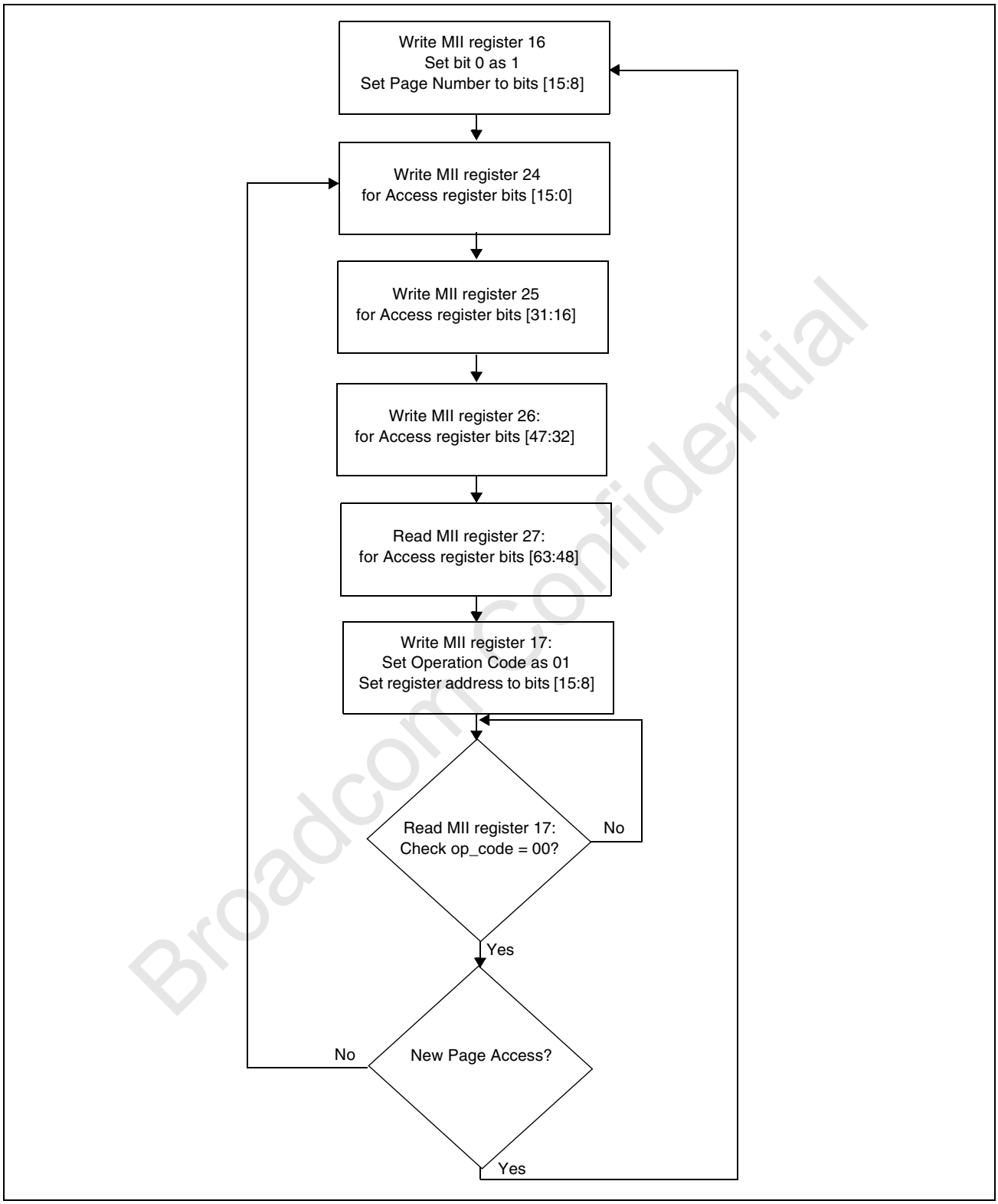


Figure 44: Write Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

Table 25 summarizes the complete management frame format.

Table 25: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven by master Driven by slave
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to master

See "MDC/MDIO Interface" on page 102 for more information regarding the timing requirements.

LED Interfaces

The BCM53101M provides flexible visibility per-port status of various functions. The LED interface offers an option to display different functions for each port given the number of LED bits available. The BCM53101M provides a total of 15 LED pins. In a 5-port switch application, these are dedicated as three LED pins per port as shown in Table 26 on page 111. If one or more ports are not used in an application and are disabled using the "LED Enable Map Register (Page 00h: Address 16h–17h)" and no more than three LED pins are to be used per port, the locations of the pins for the enabled ports are the same as if all five ports were used, with three pins reserved per port, regardless of whether the port is enabled.

To set up the LED interface, configure strap pins LEDMODE[1:0] or select the desired display functions in the "LED Function 0 Control Register (Page 00h: Address 10h–11h)" and "LED Function 1 Control Register (Page 00h: Address 12h–13h)". The per-port LED display has three fixed functions.

- To configure the strap pins, set the predefined functions to be displayed by setting the strap pins LEDMODE[1:0]. Per-port LED display has three fixed functions and occupies three LED pins.
- To configure LED display function in the two LED Function Control registers, assign each port to one of "LED Function 0 Control Register (Page 00h: Address 10h–11h)" and "LED Function 1 Control Register (Page 00h: Address 12h–13h)" by enabling the bits in the "LED Function Map Register (Page 00h: Address 14h–15h)". The LED interface shifts out the status of the selected functions for ports enabled in the "LED Enable Map Register (Page 00h: Address 16h–17h)".

Only three or less than three functions can be selected, and the per-port LED display occupies three LED pins (three fixed functions). For example, if the LED display function using the "LED Function 1 Control Register (Page 00h: Address 12h–13h)" is configured and the value is set to 2024h (three LED functions), the per-port LED display has three fixed functions and occupies three LED pins per port: port 4 LED[A:C], port 3 LED[A:C], ..., port 0 LED[A:C].

The status of enabled ports is sent out from a higher port number to the lowest port number. The output order in the shift out is from LED4A, LED4B, LED4C, LED3A, ..., LED0B, LED0C. The output port order for LED is from high port number to low port number, and the output bit order within the port LED is from A to C.

The LED MODE MAP 0 and 1 (page 00h: addresses 18h and 1Ah) can be set to select the following:

- LED to blinking
- LED on or off
- LED auto mode

Bit 7 of the "LED Configuration Register (Page 00h: Address 0Fh)" (LED_EN) is enabled by default. When bit 7 is enabled, the LED display of each port status is normal and truly reflects each port's link-up/link-down status. If bit 7 is disabled, the LED status is latched in its current state.

LED signals are active low. For the dual-function LEDs, LNK, DPX, and speed state are active low. The ACT (activity) indicator is indicated by blinking.

Table 26: LED Output Pins Per Port

Port	***LED Output Pins***
Port 4	$\overline{\text{LED4A}}$, $\overline{\text{LED4B}}$, $\overline{\text{LED4C}}$
Port 3	$\overline{\text{LED3A}}$, $\overline{\text{LED3B}}$, $\overline{\text{LED3C}}$
Port 2	$\overline{\text{LED2A}}$, $\overline{\text{LED2B}}$, $\overline{\text{LED2C}}$
Port 1	$\overline{\text{LED1A}}$, $\overline{\text{LED1B}}$, $\overline{\text{LED1C}}$
Port 0	$\overline{\text{LED0A}}$, $\overline{\text{LED0B}}$, $\overline{\text{LED0C}}$

Figure 45 shows the LED Interface register structure.

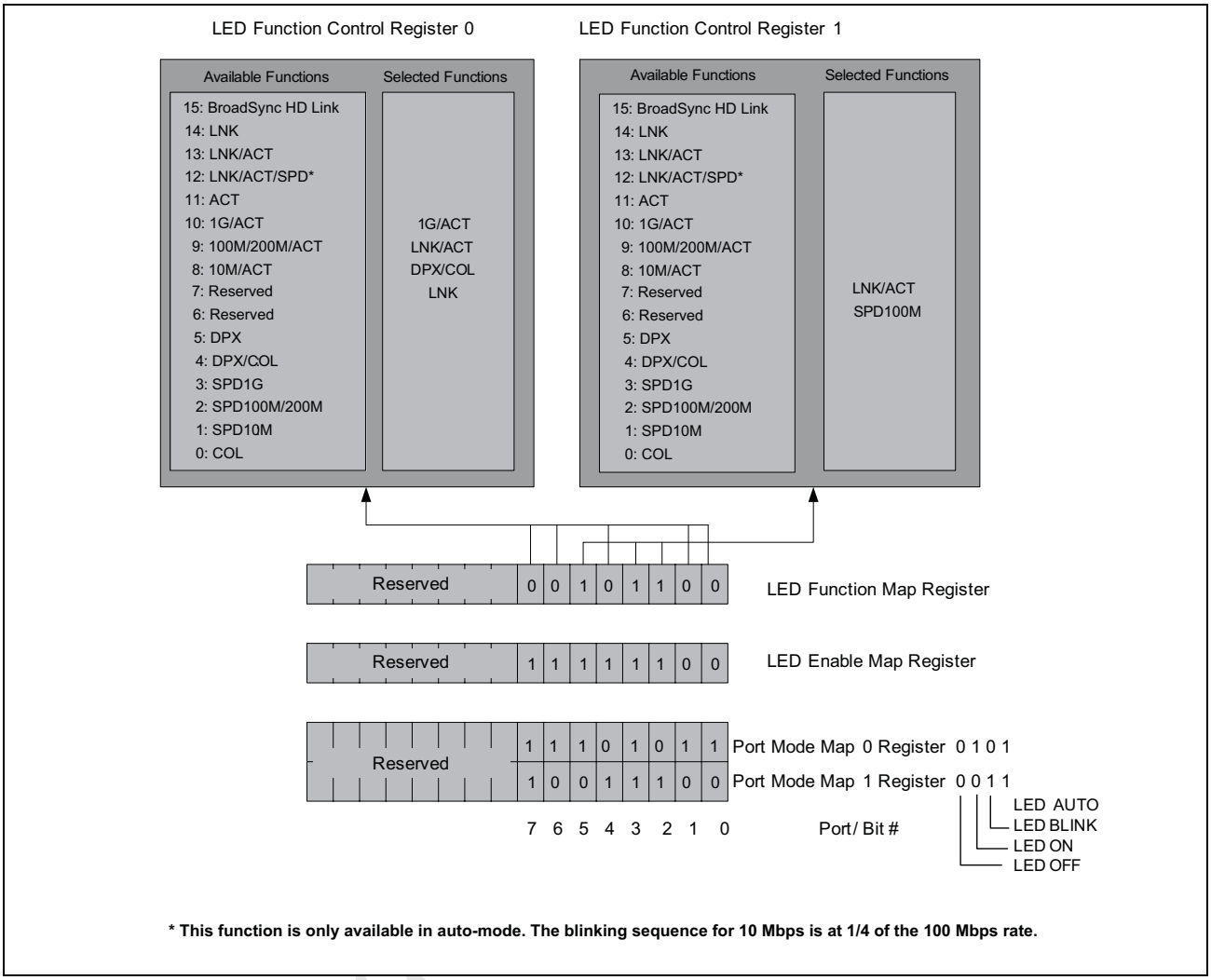


Figure 45: LED Interface Register Structure Diagram

The BCM53101M offers two LED interfaces: parallel LED and serial. As shown in Figure 46, the source of the LED status stream is the same for both interfaces. The status bit stream is based on the programmed register settings. The parallel LED interface provides all the shifting and storing of status internally and does not require any external shift registers; however, it requires more I/O pins to be connected on the part.

The serial LED interface is output through two pins (LEDDATA, LEDCLK). This interface saves the number of I/O pins but requires the user to design in the external shift registers.

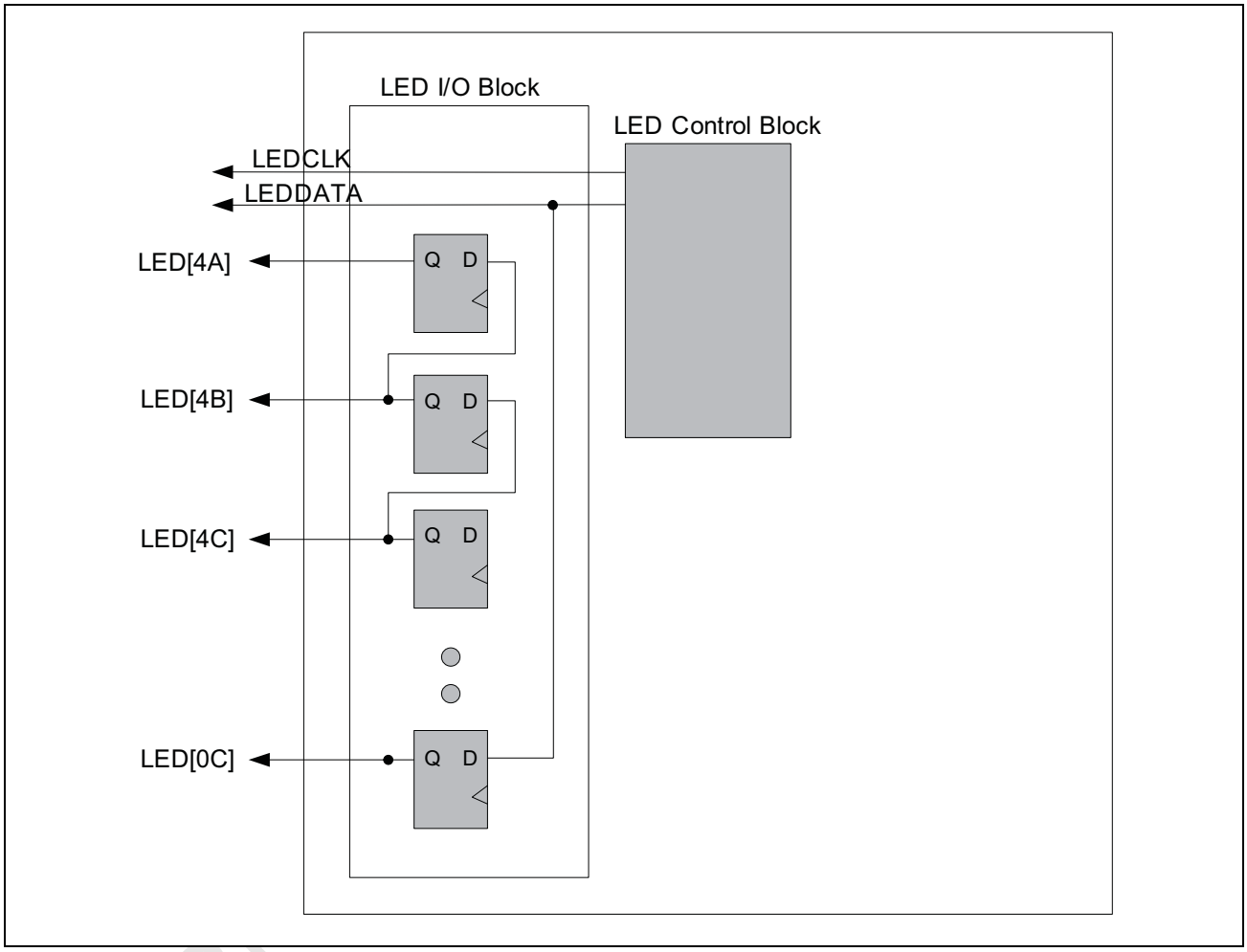


Figure 46: LED Interface Block Diagram

Dual-Input Configuration/LED Output Function

There are four LED pins that have secondary functions. These pins serve as input pins during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active-low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 27 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or an active-high LED output (see Figure 47).

Table 27: Dual-Input Configuration/LED Outputs

LED Output Pins (Normal Operation)	*Input Configuration Pin (Latched During Reset)*
$\overline{\text{LED4C}}$	CPU_EEPROM_SEL
$\overline{\text{LED3C}}$	$\overline{\text{HW\_FWDG\_EN}}$
$\overline{\text{LED2C}}$	FREQ[1]
$\overline{\text{LED1C}}$	FREQ[0]

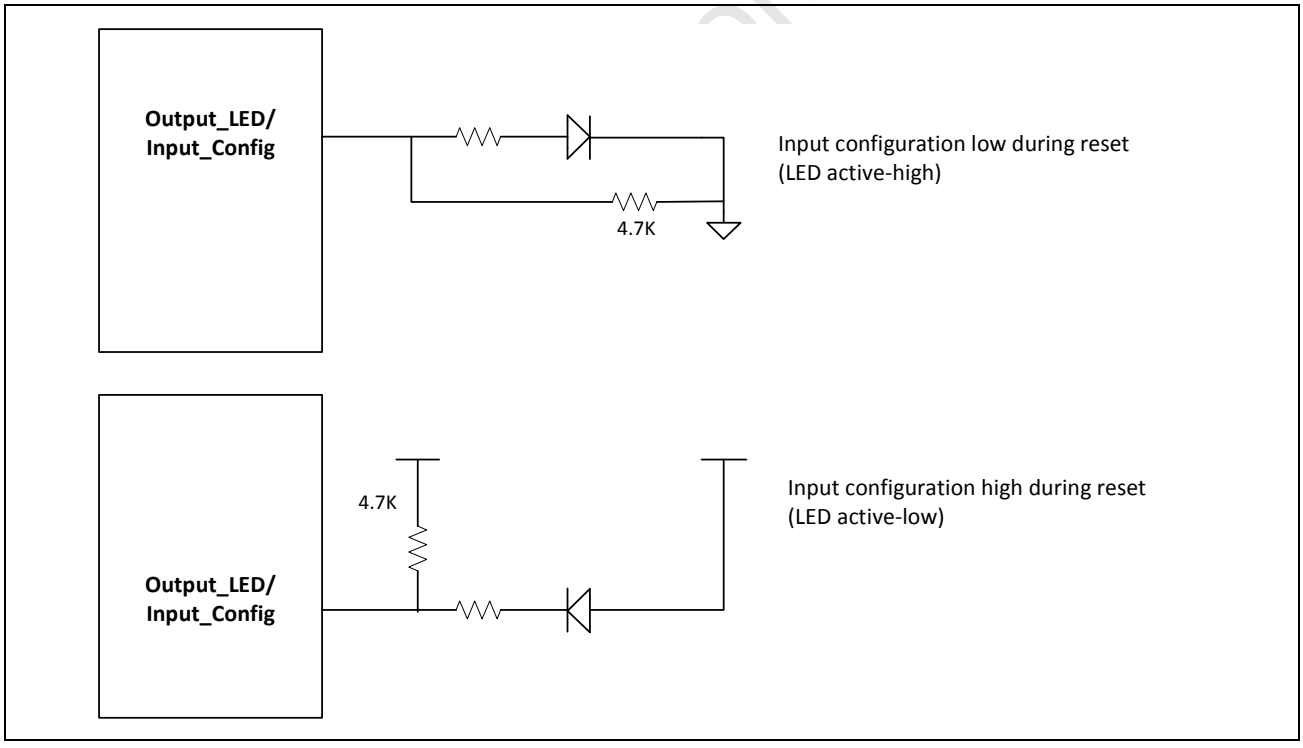


Figure 47: LED Circuit for Dual-Input Configuration/LED Output Pins

Section 5: Hardware Signal Definition Table

Hardware Signal Definitions

Table 28 lists the conventions are used to identify the I/O types.

Table 28: I/O Signal Type Definitions

Type	*Description*	*Type*	*Description*
I	Input	O	Output
I/O	Bidirectional	I/O_{PD}	Bidirectional with internal pull-down
I_{PD}	Input with internal pull-down	O_{OD}	Open drain output
I_{PU}	Input with internal pull-up	O_{ODPM}	Open drain power management output
I_S	Input with Schmidt trigger	O_{3S}	Tristated signal
GND	Ground	B	Bias
PWR	Power supply	A	Analog
OVERLINE	Active-low signal	–	–

Configuration of the BCM53101M takes place during reset by loading device control values from hardware strapping pins. Some of the strapping pins are I/O pins and have secondary functions during normal device operation. They should be configured with external pull-up or pull-down resistors. The strapping value is loaded during the reset sequence and the I/O pin returns to output operation upon completion of reset. Attaching a pull-up or pull-down resistor to these pins other than the intended default value can have an adverse effect on the function of the device.

Table 29: Signal Description

Signal Name	*Pin Number*	*Type*	*Description*
Media Connections			
RD4+/– RD3+/– RD2+/– RD1+/– RD0+/–	B45/A52 B41/A49 B38/A45 B34/A42 A41/B33	I/O_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
TD4+/– TD3+/– TD2+/– TD1+/– TD0+/–	A51/B44 A50/B42 A44/B37 A43/B35 B32/A40	I/O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.

Table 29: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
Note: The signal level of all the digital pins in this table must not exceed VDD + 0.5V except where noted.			
Clock/Reset			
XTALI XTALO	A29 B25	I O	**25 MHz Crystal/Clock Input.** For a single-ended clock signal input, connect a 25 MHz (±50 ppm) reference clock to the XTALI pin. This pin must be driven with a continuous clock. Leave XTALO unconnected for this mode of operation. Alternatively, a 25 MHz parallel-resonant crystal can be connected between the XTALI and XTALO pins, with a 27 pF capacitor from each pin to GND. ***Note:*** XTALI/ATALO signal level must not exceed 2.5V.
RESET	B60	$I_{S, PU}$	**Reset.** Active low. Resets the BCM53101M.
MII1 Interface (RGMII/MII/RvMII/RMII/TMII/RvTMII)[a] (Port 8, IMP 0)			
MII1_TXC	A10	I/O_{PD}	**MII1 Transmit Clock.** • RGMII = 2.5/25/125 MHz output • MII = 2.5/25 MHz input • RvMII = 2.5/25 MHz output • RMII (external clock) = 50 MHz input • RMII (internal clock) = 50 MHz output
MII1_TXD[3] MII1_TXD[2] MII1_TXD[1] MII1_TXD[0]	B5 A7 A8 B7	I/O_{PD}	**MII1 Transmit Data Output**. Nibble-wide transmit data is output on these pins synchronously to MII1_TXC. MII1_TXD[3] is the most significant bit. In RMII mode, only MII1_TXD[1:0] are used.
MII1_TXEN	A9	I/O_{PD}	**MII1 Transmit Enable**. Indicates that the data nibble is valid on MII1_TXD[3:0].
MII1_RXC	A11	I/O_{PD}	**MII1 Receive Clock.** • RGMII = 2.5/25/125 MHz input • MII = 2.5/25 MHz input • RvMII = 2.5/25 MHz output • RMII = Not used
MII1_RXD[3] MII1_RXD[2] MII1_RXD[1] MII1_RXD[0]	A13 B11 A12 B10	I/O_{PD}	**MII1 Receive Data Inputs.** Nibble-wide receive data. MII1_RXD[3] is the most significant bit. In RMII mode, only MII2_RXD[1:0] are used.
MII1_RXER	A14	I/O_{PD}	**MII1 Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame. An illegal code or some other coding violation has been detected in the data received from the twisted-pair medium when both MII1_RXDV and MII1_RXER are high.

Table 29: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
MII1_RXDV	A15	I/O_{PD}	**MII1 Receive Data Valid.** Active high. MII1_RXDV indicates that a receive frame is in progress and the data present on the MII1_RXD input pins is valid.
MII2 Interface (MII/RvMII/RMII/TMII/RvTMII)[a] (Port 5, IMP 1, WAN PORT)			
MII2_TXC	A21	I/O_{PD}	**MII2 Transmit Clock.** • MII = 2.5/25 MHz input • RvMII = 2.5/25 MHz output • RMII (external clock) = 50 MHz input • RMII (internal clock) = 50 MHz output • TMII = 50 MHz input • RvTMII = 50 MHz output
MII2_TXD[3] MII2_TXD[2] MII2_TXD[1] MII2_TXD[0]	A22 B17 A16 B14	I/O_{PD}	**MII2 Transmit Data Output.** Nibble-wide transmit data is output on these pins synchronously to MII2_TXC. MII2_TXD[3] is the most significant bit. In RMII mode, only MII2_TXD[1:0] are used.
MII2_TXEN	B15	I/O_{PD}	**MII2 Transmit Enable.** Indicates that the data nibble is valid on MII2_TXD[3:0].
MII2_RXC	A24	I/O_{PD}	**MII2 Receive Clock.** • MII = 2.5/25 MHz input • RvMII = 2.5/25 MHz output • RMII = Not used • TMII = 50 MHz input • RvTMII = 50 MHz output
MII2_RXD[3] MII2_RXD[2] MII2_RXD[1] MII2_RXD[0]	B21 A25 B19 A23	I/O_{PD}	**MII2 Receive Data Inputs.** Nibble-wide receive data. MII2_RXD[3] is the most significant bit. In RMII mode, only MII2_RXD[1:0] are used.
MII2_RXDV	A26	I/O_{PD}	**MII2 Receive Data Valid.** Active high. MII2_RXDV indicates that a receive frame is in progress and the data present on the MII2_RXD input pins is valid.
MII2_RXER	A27	I/O_{PD}	**MII2 Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame. An illegal code or some other coding violation has been detected in the data received from the twisted-pair medium when both MII2_RXDV and MII2_RXER are high.
Serial MII Interface			
MDIO	A3	I/O_{PD}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of the internal transceivers. The input data value on the MDIO pin is valid and latched on the rising edge of MDC.

Table 29: Signal Description (Cont.)

Signal Name	*Pin Number*	*Type*	*Description*
MDC	B1	I/O_{PD}	**Management Data Clock.** MDC must be provided to the BCM53101M as an input to allow MII management functions. Clock frequencies up to 12.5 MHz are supported. If the BCM53101M detects SCK activity on the SPI interface, the BCM53101M sources a 2.5 MHz clock to the external PHY device.
Bias			
RDAC	A48	B	**DAC Bias Resistor.** Adjusts the drive level of the transmit DAC. A 1.24 kΩ 1% precision resistor must be connected between the RDAC pin and GND.
LEDs			
$\overline{\text{LED4A}}$ $\overline{\text{LED4B}}$ LED4C	B57 A68 A69	I/O_{PU}	**Per Port Parallel LED Indicators.**
$\overline{\text{LED3A}}$ $\overline{\text{LED3B}}$ LED3C	A65 A66 A67		
$\overline{\text{LED2A}}$ $\overline{\text{LED2B}}$ LED2C	B53 A64 B54		
$\overline{\text{LED1A}}$ $\overline{\text{LED1B}}$ LED1C	B51 A62 A63		
$\overline{\text{LED0A}}$ $\overline{\text{LED0B}}$ LED0C	B49 A60 A61		
Note: The LED pins are active low. However, for those pins that have a multiplexed strap function, the polarity of the LED pins may change. The LED pin active state is the inverse of the state of the strap pin. On power-up/reset, if the shared strap pin is in a low state, then the LED pin is active high, and vice versa: • $\overline{\text{LED4C}}$ shares with $\overline{\text{CPU\_EEPROM\_SEL}}$ • $\overline{\text{LED3C}}$ shares with HW_FWDG_EN • $\overline{\text{LED1C}}$ shares with FREQ[1] • $\overline{\text{LED0C}}$ shares with FREQ[0]			
LEDCLK	B59	I/O_{PD}	**Serial LED Shift Clock**. Periodically active. Enables shift of LEDDATA into external registers. *Shared with LEDMODE[1].*
LEDDATA	A70	I/O_{PD}	**Serial LED Data Output.** Serial LED data is shifted out when LEDCLK is active. *Shared with LEDMODE[0].*

Table 29: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
Serial Port Interface			
SCK	B4	I/O_{PD}	**Serial Clock.** Clock input to the serial port interface supplied by the SPI master. Supports up to 2 MHz. *Shared with EEPROM's SCK.*
$\overline{SS}$	A6	I/O_{PU}	**Slave Select.** Active low signal that enables a serial port interface Read or Write operation. *Shared with EEPROM's CS.*
MOSI	A5	I/O_{PU}	**Master-Out/Slave-In.** Input signal which receives control and address information for the serial port interface, as well as serial data during Write operations. *Shared with EEPROM's DI.*
MISO	A4	I/O_{PU}	**Master-In/Slave-Out.** Output signal from the BCM53101M driven with serial data during a serial port interface Read operation. *Shared with EEPROM's DO.*
EEPROM Interface			
SCK	B4	I/O_{PD}	**Serial Data Clock.** Clock output to the EEPROM supplied by the BCM53101M. *Shared with SPI's SCK pin.*
CS	A6	I/O_{PU}	**Chip Select.** Active high signal that enables an EEPROM Read operation. *Shared with SPI's SS pin.*
DO	A4	I/O_{PU}	**Data Out.** Serial data output from the external EEPROM. *Share with SPI's MISO pin.*
DI	A5	I/O_{PU}	**Data In.** Serial data input to the external EEPROM. *Shared with SPI's MOSI pin.*
Configuration			
MII1_MODE[2] MII1_MODE[1] MII1_MODE[0]	B29 A33 A32	I/O_{PD}	**MII1 Mode.** Used to configure MII1 port. • 100 = Reserved • 101 = RGMII • 000 = MII/TMII • 001 = RvMII/RvTMII • 010 = RMII with external clock • 011 = RMII with internal clock
MII2_MODE[1] MII2_MODE[0]	A34 B31	I/O_{PD}	**MII2 Mode**. Used to configure MII2 port. • 00 = MII/TMII • 01 = RvMII/RvTMII • 10 = RMII with external clock • 11 = RMII with internal clock

Table 29: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
FREQ[1:0]	A63 A61	I/O_{PU} I/O_{PU}	**Clock Frequency Select.** Selects internal operational clock speed. • 00 = 71.42 MHz • 01 = 76 MHz • 10 = 50 MHz • 11 = 66 MHz (default) • *FREQ[1:0] shared with LED1C and LED0C*
HW_FWDG_EN	A67	I/O_{PU}	**Forwarding Enable** HW_FWDG_EN = 1: Frame forwarding is disabled at power-up. Typically implemented to support compliant IEEE 802.1 Spanning Tree Protocol in a managed application. HW_FWDG_EN = 0: Frame forwarding is enabled (typical for unmanaged applications). *Shared with LED3C.*
LEDMODE[1] LEDMODE[0]	B59 A70	I/O_{PD} I/O_{PD}	**LED Mode Selection.** LEDMODE[1] share with LEDCLK. LEDMODE[0] share with LEDDATA.
CPU_EEPROM_SEL	A69	I_{PU}	**CPU or EEPROM Interface Selection** • CPU_EEPROM_SEL = 0: Disables SPI interface, and allows for connection to EEPROM. • CPU_EEPROM_SEL = 1: Configures SPI interface to connect to CPU. • *Shared with LED4C.* ***Note:*** The SPI interface has to be enabled (CPU_EEPROM_SEL = 1) for Pseudo-PHY accesses through the MDC/MDIO interface to function properly.
JTAG Controller			
TCK	B46	I/O_{PU}	**JTAG Test Clock Input.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	A57	I/O_{PU}	**JTAG Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
TDO	B47	I/O_{PU}	**JTAG Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; otherwise, high impedance.
TMS	A58	I/O_{PU}	**JTAG Mode Select Input.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.

Table 29: Signal Description (Cont.)

Signal Name	*Pin Number*	*Type*	*Description*
$\overline{\text{TRST}}$	A59	I_{PU}	**JTAG Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. This reset controls the JTAG state machine. The TRST input must be driven low to insure the TAP controller initializes to the proper state. ***Note:*** A 4.7K external pull-down resistor is required on this pin to ensure proper initialization.
Power			
VDDC	B3, B9, B13, B22, B27, B50, B56	PWR	**1.2V Digital Core VDD**
VSSC	ePAD	GND	**Digital Core GND**
VDDO	B2, B48, B52, B55, B58	PWR	**3.3V/2.5V Digital Periphery (Output Buffer) VDD**. LEDs, SPI, EEPROM, JTAG, and MDC/MDIO
VDDO1	B26, B28, B30	PWR	**3.3V/2.5V Digital Periphery (Output Buffer) VDD**. MII1 and MII2 mode configuration pins
VDDO2	B6, B8, B12	PWR	**3.3V/2.5V Digital Periphery (Output Buffer) VDD**. MII1 Interface RGMII = 2.5V MII = 3.3V RvMII = 3.3V RMII = 3.3V
VDDO3	B16, B18, B20	PWR	**3.3V/2.5V Digital Periphery (Output Buffer) VDD** MII2 Interface MII = 3.3V RvMII = 3.3V RMII = 3.3V TMII = 3.3V RvTMII = 3.3V
VSSO	ePAD	GND	**Digital Periphery (Output Buffer) GND**
VDDA	A39, B36, B43	PWR	**1.2V Analog VDD**
VSSA	ePAD	GND	**Analog GND**
VDDBIAS	A47, B40	PWR	**2.5V Bias Circuit VDD**
VSSBIAS	ePAD	GND	**Bias Circuit GND**
PLLAVDD	B23	PWR	**1.2V Analog PLL Circuit VDD**
PLLAVSS	ePAD	GND	**PLL Analog Circuit GND**
PLLDVDD	B39	PWR	**1.2V Digital PLL Circuit VDD**
PLLDVSS	ePAD	GND	**PLL Digital Circuit GND**
VDDXTAL	B24	PWR	**2.5V XTAL VDD**
VSSXTAL	ePAD	GND	**XTAL Circuit GND**

Table 29: Signal Description (Cont.)

Signal Name	*Pin Number*	*Type*	*Description*
No Connect			
NC	A1, A2, A17, A18, A19, A20, A35, A36, A37, A38, A53, A54, A55, A56, A71, A72	NC	**No Connect.** These pins are unconnected.
DNC	A28, A30, A31, A46	DNC	**No Connect.** These pins are for test purposes only and should not be connected (float). Do not connect these pins together.
Note: There is a weak internal pull-down resistor at pin A30. This pin must be connected to a stronger 1.0 kΩ external pull-down resistor to ground to enable the LED I/O driver. This is the workaround erratum, LED Blinking Abnormally During Power-on Reset.			

a. MII1 and MII2 interfaces support full-duplex operation only.

Section 6: Pin Assignment

BCM53101 Signals by Ball

Table 30: BCM53101 Signals by Ball

Ball	Signal
A1	NC
A2	NC
A3	MDIO
A4	MISO/DO
A5	MOSI/DI
A6	$\overline{SS}$/CS
A7	MII1_TXD[2]
A8	MII1_TXD[1]
A9	MII1_TXEN
A10	MII1_TXC
A11	MII1_RXC
A12	MII1_RXD[1]
A13	MII1_RXD[3]
A14	MII1_RXER
A15	MII1_RXDV
A16	MII2_TXD[1]
A17	NC
A18	NC
A19	NC
A20	NC
A21	MII2_TXC
A22	MII2_TXD[3]
A23	MII2_RXD[0]
A24	MII2_RXC
A25	MII2_RXD[2]
A26	MII2_RXDV
A27	MII2_RXER
A28	DNC
A29	XTALI
A30	DNC

Ball	*Signal*
A31	DNC
A32	MII1_MODE[0]
A33	MII1_MODE[1]
A34	MII2_MODE[1]
A35	NC
A36	NC
A37	NC
A38	NC
A39	VDDA
A40	TD0–
A41	RD0+
A42	RD1–
A43	TD1+
A44	TD2+
A45	RD2–
A46	DNC
A47	VDDBIAS
A48	RDAC
A49	RD3–
A50	TD3+
A51	TD4+
A52	RD4–
A53	NC
A54	NC
A55	NC
A56	NC
A57	TDI
A58	TMS
A59	TRST
A60	LED0B
A61	LED0C/FREQ[0]
A62	LED1B
A63	LED1C/FREQ[1]
A64	LED2B
A65	LED3A
A66	LED3B
A67	LED3C/$\overline{\text{HW\_FWDG\_EN}}$
A68	LED4B

Ball	*Signal*
A69	LED4C/CPU_EEPROM_SEL
A70	LEDDATA/LEDMODE[0]
A71	NC
A72	NC
B1	MDC
B2	VDDO
B3	VDDC
B4	SCK
B5	MII1_TXD[3]
B6	VDDO2
B7	MII1_TXD[0]
B8	VDDO2
B9	VDDC
B10	MII1_RXD[0]
B11	MII1_RXD[2]
B12	VDDO2
B13	VDDC
B14	MII2_TXD[0]
B15	MII2_TXEN
B16	VDDO3
B17	MII2_TXD[2]
B18	VDDO3
B19	MII2_RXD[1]
B20	VDDO3
B21	MII2_RXD[3]
B22	VDDC
B23	PLLAVDD
B24	VDDXTAL
B25	XTALO
B26	VDDO1
B27	VDDC
B28	VDDO1
B29	MII1_MODE[2]
B30	VDDO1
B31	MII2_MODE[0]
B32	TD0+
B33	RD0–
B34	RD1+

Ball	*Signal*
B35	TD1–
B36	VDDA
B37	TD2–
B38	RD2+
B39	PLLDVDD
B40	VDDBIAS
B41	RD3+
B42	TD3–
B43	VDDA
B44	TD4–
B45	RD4+
B46	TCK
B47	TDO
B48	VDDO
B49	LED0A
B50	VDDC
B51	LED1A
B52	VDDO
B53	LED2A
B54	LED2C
B55	VDDO
B56	VDDC
B57	LED4A
B58	VDDO
B59	LEDCLK/LEDMODE[1]
B60	RESET
ePAD	VSSC
ePAD	VSSO
ePAD	VSSA
ePAD	VSSBIAS
ePAD	PLLAVSS
ePAD	PLLDVSS
ePAD	VSSXTAL

BCM53101 Signals by Name

Table 31: BCM53101 Signals by Name

Signal	*Ball*
DNC	A28
DNC	A30
DNC	A31
DNC	A46
LED0A	B49
LED0B	A60
LED0C/FREQ[0]	A61
LED1A	B51
LED1B	A62
LED1C/FREQ[1]	A63
LED2A	B53
LED2B	A64
LED2C	B54
LED3A	A65
LED3B	A66
LED3C/HW_FWDG_EN	A67
LED4A	B57
LED4B	A68
LED4C/CPU_EEPROM_SEL	A69
LEDCLK/LEDMODE[1]	B59
LEDDATA/LEDMODE[0]	A70
MDC	B1
MDIO	A3
MII1_MODE[0]	A32
MII1_MODE[1]	A33
MII1_MODE[2]	B29
MII1_RXC	A11
MII1_RXD[0]	B10
MII1_RXD[1]	A12
MII1_RXD[2]	B11
MII1_RXD[3]	A13
MII1_RXDV	A15
MII1_RXER	A14
MII1_TXC	A10

Signal	*Ball*
MII1_TXD[0]	B7
MII1_TXD[1]	A8
MII1_TXD[2]	A7
MII1_TXD[3]	B5
MII1_TXEN	A9
MII2_MODE[0]	B31
MII2_MODE[1]	A34
MII2_RXC	A24
MII2_RXD[0]	A23
MII2_RXD[1]	B19
MII2_RXD[2]	A25
MII2_RXD[3]	B21
MII2_RXDV	A26
MII2_RXER	A27
MII2_TXC	A21
MII2_TXD[0]	B14
MII2_TXD[1]	A16
MII2_TXD[2]	B17
MII2_TXD[3]	A22
MII2_TXEN	B15
MISO/DO	A4
MOSI/DI	A5
NC	A1
NC	A2
NC	A17
NC	A18
NC	A19
NC	A20
NC	A35
NC	A36
NC	A37
NC	A38
NC	A53
NC	A54
NC	A55
NC	A56
NC	A71
NC	A72

Signal	*Ball*
PLLAVDD	B23
PLLAVSS	ePAD
PLLDVDD	B39
PLLDVSS	ePAD
RD0–	B33
RD0+	A41
RD1–	A42
RD1+	B34
RD2–	A45
RD2+	B38
RD3–	A49
RD3+	B41
RD4–	A52
RD4+	B45
RDAC	A48
RESET	B60
SCK	B4
$\overline{SS}$/CS	A6
TCK	B46
TD0–	A40
TD0+	B32
TD1–	B35
TD1+	A43
TD2–	B37
TD2+	A44
TD3–	B42
TD3+	A50
TD4–	B44
TD4+	A51
TDI	A57
TDO	B47
TMS	A58
TRST	A59
VDDA	A39
VDDA	B36
VDDA	B43
VDDBIAS	A47
VDDBIAS	B40

Signal	*Ball*
VDDC	B3
VDDC	B9
VDDC	B13
VDDC	B22
VDDC	B27
VDDC	B50
VDDC	B56
VDDO	B2
VDDO	B48
VDDO	B52
VDDO	B55
VDDO	B58
VDDO1	B26
VDDO1	B28
VDDO1	B30
VDDO2	B6
VDDO2	B8
VDDO2	B12
VDDO3	B16
VDDO3	B18
VDDO3	B20
VDDXTAL	B24
VSSA	ePAD
VSSBIAS	ePAD
VSSC	ePAD
VSSO	ePAD
VSSXTAL	ePAD
XTALI	A29
XTALO	B25

Section 7: Ball Location Diagram

Figure 48 shows the BCM53101M ball location diagram.

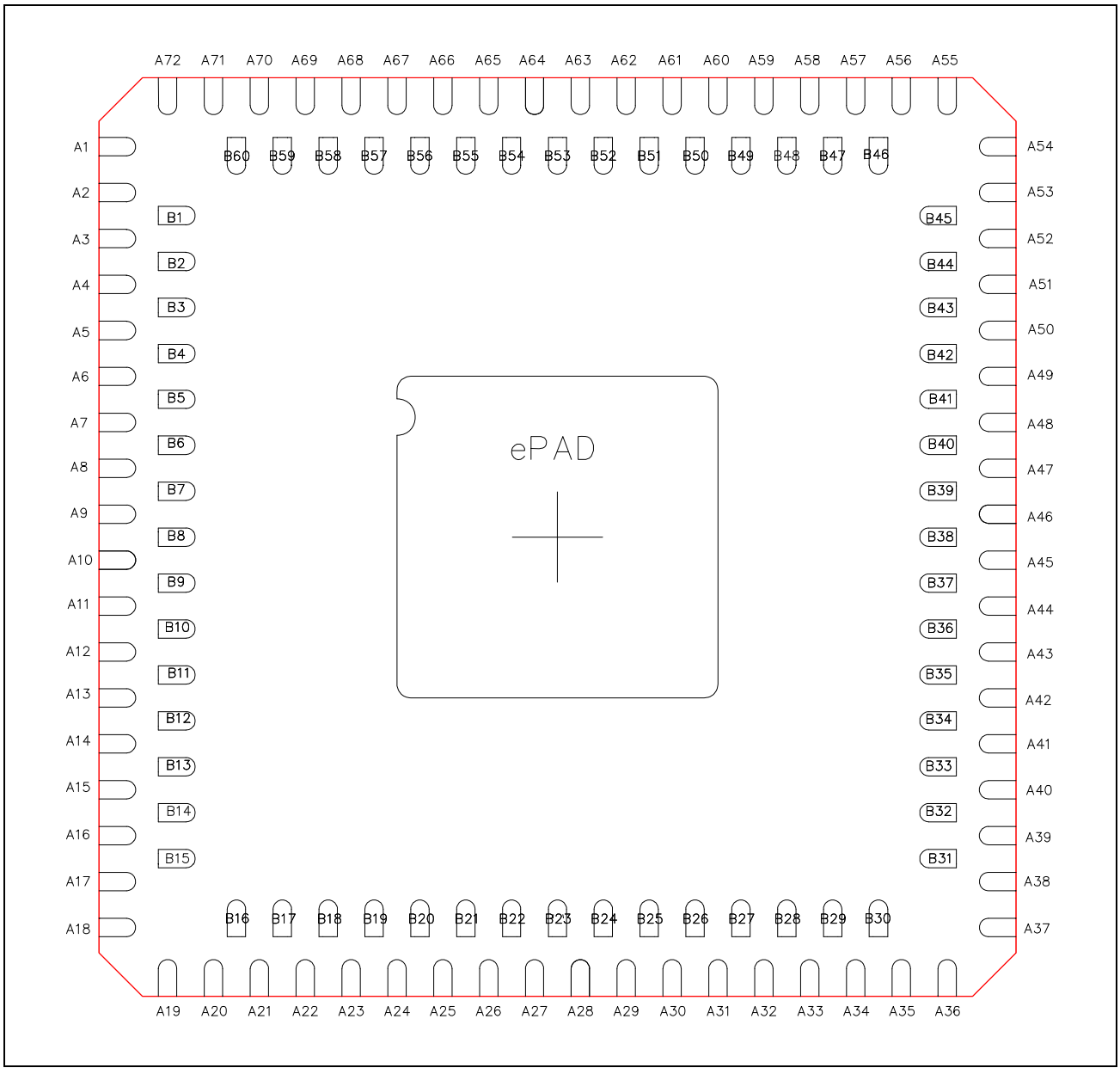


Figure 48: Ball Location Diagram

Section 8: Register Definitions

Register Definition

The BCM53101M register sets can be accessed through the programming interfaces described in "Programming Interfaces" on page 85. The register space is organized into pages, each containing a certain set of registers. Table 32 lists the pages defined in the BCM53101M. To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their addresses. See "Programming Interfaces" on page 85 for more information.

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or to write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Clear on read

Reserved bits must be written as the default value and ignored when read.

Global Page Register

Table 32: Global Page Register Map

Page	*Description*
00h	"Page 00h: Control Registers" on page 134
01h	"Page 01h: Status Registers" on page 159
02h	"Page 02h: Management/Mirroring Registers" on page 163
03h	Reserved
04h	"Page 04h: ARL Control Register" on page 173
05h	"Page 05h: ARL/VTBL Access Registers" on page 178
06h–0Fh	Reserved
10h–14h	"Page 10h–14h: Internal PHY MII Registers" on page 188

Table 32: Global Page Register Map (Cont.)

Page	Description
15h–1Fh	Reserved
20h–28h	"Page 20h–28h: Port MIB Registers" on page 211
29h–2Fh	Reserved
30h	"Page 30h: QoS Registers" on page 215
31h	"Page 31h: Port-Based VLAN Registers" on page 224
32h	"Page 32h: Trunking Registers" on page 225
33h	Reserved
34h	"Page 34h: IEEE 802.1Q VLAN Registers" on page 227
35h	Reserved
36h	"Page 36h: DoS Prevent Register" on page 235
37h–3Fh	Reserved
40h	"Page 40h: Maximum Frame Control Registers" on page 239
41h	"Page 41h: Broadcast Storm Suppression Registers" on page 241
42h	"Page 42h: EAP Registers" on page 249
43h	"Page 43h: MSPT Registers" on page 253
44h–6Fh	Reserved
70h	"Page 70h: MIB Snapshot Control Register" on page 255
71h	"Page 71h: Port MIB Snapshot Register" on page 257
72h–84h	Reserved
85h	"Page 85h: WAN Interface (Port 5) External PHY MII Registers" on page 257
86h–87h	Reserved
88h	"Page 88h: IMP Port External PHY MII Registers Page Summary" on page 257
89h	Reserved
90h	"Page 90h: BroadSync™ HD Registers" on page 258
91h	"Page 91h: Traffic Remarking Registers" on page 264
92h–EFh	Reserved
Maps to all pages	"Global Registers" on page 266

Page 00h: Control Registers

Table 33: Control Registers (Page 00h)

Address	Bits	Register Name
00h–05h	8/port	"Port Traffic Control Register (Page 00h: Address 00h–05h)" on page 136
06h–07h	8	Reserved
08h	8	"IMP Port[8] Control Register (Page 00h: Address 08h)" on page 136
09h–0Ah	8	Reserved
0Bh	8	"Switch Mode Register (Page 00h: Address 0Bh)" on page 137
0Ch–0Dh	16	Reserved
0Eh	8	"IMP Port State Override Register (Page 00h: Address 0Eh)" on page 138
0Fh	8	"LED Configuration Register (Page 00h: Address 0Fh)" on page 139
10h–11h	16	"LED Function 0 Control Register (Page 00h: Address 10h–11h)" on page 140
12h–13h	16	"LED Function 1 Control Register (Page 00h: Address 12h–13h)" on page 141
14h–15h	16	"LED Function Map Register (Page 00h: Address 14h–15h)" on page 141
16h–17h	16	"LED Enable Map Register (Page 00h: Address 16h–17h)" on page 142
18h–19h	16	"LED Mode Map 0 Register (Page 00h: Address 18h–19h)" on page 142
1Ah–1Bh	16	"LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)" on page 143
1Ch–1Eh	–	Reserved
1Fh	8	Reserved
20h	–	"Switch Control Register (Page 00h: Address 20h)" on page 143
21h	8	"Port Forward Control Register (Page 00h: Address 21h)" on page 144
22h–23h	–	Reserved
24h–25h	16	"Protected Port Selection Register (Page 00h: Address 24h–25h)" on page 146
26h–27h	16	"WAN Port Select Register (Page 00h: Address 26h–27h)" on page 146
28h–2Bh	32	"Pause Capability Register (Page 00h: Address 28h–2Bh)" on page 147
2Ch–2Eh	–	Reserved
2Fh–31h	–	Reserved
32h–33h	16	"Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)" on page 147
34h–35h	16	"Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)" on page 148
36h–37h	16	"MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)" on page 148
38h–39h	16	"Pause Pass Through for RX Register (Page 00h: Address 38h–39h)" on page 148
3Ah–3Bh	16	"Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)" on page 149
3Ch–3Dh	16	"Disable Learning Register (Page 00h: Address 3Ch–3Dh)" on page 149
3Eh–3Fh	16	"Software Learning Control Register (Page 00h: Address 3Eh–3Fh)" on page 150
40h–47h	–	Reserved

Table 33: Control Registers (Page 00h) (Cont.)

Address	Bits	Register Name
48h–49h	–	"PHY Control Register (Page 00h: Address 48h–49h)" on page 151
4Ah–4Dh	–	"PHY Power-Down Register (Page 00h: Address 4Ah–4Dh)" on page 151
4Eh–4Fh	–	"PHY Status Register (Page 00h: Address 4Eh–4Fh)" on page 152
50h–57h	–	Reserved
58h–5Dh	8/port	"Port N(0–5) Port State Override Register (Page 00h: Address 58h–5Dh)" on page 153
5Eh–5Fh	–	Reserved
60h	–	"IMP RGMII Control Register (Page 00h: Address 60h)" on page 154
61h–74h	–	Reserved
75h	–	"MDIO WAN Port Address Register (Page 00h: Address 75h)" on page 154
78h	–	"MDIO IMP PORT Address Register (Page 00h: Address 78h)" on page 154
79h	–	"Watch Dog Control 0 Register (Page 00h: Address 79h)" on page 154
7Ah–7Fh	–	Reserved
80h	8	"Pause Frame Detection Control Register (Page 00h: Address 80h)" on page 155
81h–87h	–	Reserved
88h	8	"Fast-Aging Control Register (Page 00h: Address 88h)" on page 155
89h	8	"Fast-Aging Port Control Register (Page 00h: Address 89h)" on page 155
8Ah–8Bh	16	"Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)" on page 156
8Ch–8Fh	–	Reserved
90h–A1h	–	"Port Cross Connect Destination Register (Page 00h: Address 90h–A1h)" on page 156
A2h–EDh	–	Reserved
EEh	–	"Bonding Pad Status Register (Page 00h: Address EEh)" on page 158
EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
8Ch–EFh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Port Traffic Control Register (Page 00h: Address 00h–05h)

Table 34: Port Traffic Control Register Address Summary

Address	Description
00h	Port 0
01h	Port 1
02h	Port 2
03h	Port 3
04h	Port 4
05h	Port 5

Table 35: Port Traffic Control Register (Page 00h: Address 00h–05h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	CPU writes the current computed states of its spanning tree algorithm for a given port. 000 = No spanning tree (default for unmanaged mode) 001 = Disabled state (default for managed mode) 010 = Blocking state 011 = Listening state 100 = Learning state 101 = Forwarding state 110–111 = Reserved	Controlled by HW_FWDG_EN Strap Option HW_FWDG_EN = 0: Unmanaged mode HW_FWDG_EN = 1: Managed mode
4:2	Reserved	R/W	Write as default. Ignore on read.	0
1	TX_DISABLE	R/W	0 = Enables the transmit function of the port at the MAC level. 1 = Disables the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	0 = Enables the receive function of the port at the MAC level. 1 = Disables the receive function of the port at the MAC level.	0

IMP Port[8] Control Register (Page 00h: Address 08h)

Table 36: IMP Port[8] Control Register (Page 00h: Address 08h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	Write as default. Ignore on read.	—

Table 36: IMP Port[8] Control Register (Page 00h: Address 08h) (Cont.)

Bit	Name	R/W	Description	Default
4	RX_UCST_EN	R/W	Receive unicast enable Allow unicast frames to be forwarded to the IMP when the IMP is configured as the frame management port and the frame matches the address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0
3	RX_MCST_EN	R/W	Receive multicast enable Allow multicast frames to be forwarded to the IMP when the IMP is configured as the frame management port and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0
2	RX_BCST_EN	R/W	Receive broadcast enable Allow broadcast frames to be forwarded to the IMP when the IMP is configured as the frame management port. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0
1:0	Reserved	R/W	Write as default. Ignore on read.	0

Switch Mode Register (Page 00h: Address 0Bh)

Table 37: Switch Mode Register (Page 00h: Address 0Bh)

Bit	Name	R/W	Description	Default
7:2	Reserved	R/W	Write as default. Ignore on read.	0
1	SW_FWDG_EN	R/W	Software forwarding enable • 1 = Frame forwarding is enabled. • 0 = Frame forwarding is disabled. Managed switch implementations should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters before frame forwarding is enabled.	Inverse of HW_FWDG_EN

Table 37: Switch Mode Register (Page 00h: Address 0Bh)

Bit	Name	R/W	Description	Default
0	SW_FWDG_MODE	R/W	Software forwarding mode 0 = Unmanaged mode 1 = Managed mode ARL treats reserved multicast addresses differently, depending on this selection.	HW_FWDG_EN

Pause Quanta Register (Page 00h: Address 0Ch–0Dh)

Table 38: Pause Quanta Register (Page 00h: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:0	PAUSE_QUANTA	RO	Number of slot times for which the transmitter wants the link partner to suspend its transmission. The same value is common to all ports that have auto-negotiated to full duplex with flow control enabled.	FFFFh

IMP Port State Override Register (Page 00h: Address 0Eh)

Table 39: IMP Port State Override Register (Page 00h: Address 0Eh)

Bit	Name	R/W	Description	Default
7	MII_SW_OR	R/W	MII software override 0 = Use MII hardware pin status. 1 = Use contents of this register.	0
6	Reserved	R/W	Write as default. Ignore on read.	0
5	TX Flow Control Capability	R/W	Link partner flow control capability 0 = Not PAUSE capable 1 = PAUSE capable	0
4	RX Flow Control Capability	R/W	Link partner flow control capability 0 = Not PAUSE-capable 1 = PAUSE-capable	0
3:2	SPEED	R/W	Speed 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = 200 Mbps (this enables TMII function on port 8)	10
1	FDX	R/W	Full duplex 0 = Half duplex 1 = Full duplex	1

Table 39: IMP Port State Override Register (Page 00h: Address 0Eh) (Cont.)

Bit	Name	R/W	Description	Default
0	LINK	R/W	Link status 0 = Link fail 1 = Link pass	0

LED Control Registers (Page 00h: Address 0Fh–1Ch)

Table 40: LED Control Register Address Summary

Address	Description
0Fh	LED Configuration register
10h–11h	LED function 0 control register
12h–13h	LED function 1 control register
14h–15h	LED function map register
16h–17h	LED enable map register
18h–19h	LED mode map 0 register
1Ah–1Bh	LED mode map 1 register
1Ch	LED Option register

LED Configuration Register (Page 00h: Address 0Fh)

Table 41: LED Configuration Register (Page 00h: Address 0Fh)

Bit	Name	R/W	Description	Default
7	LED_EN	R/W	Enable LED	1
6	POST_EXEC	R/W	Write 1 to restart POST.	0
5	POST_PSCAN_EN	R/W	When enabled, switch scans the port during the POST period.	0
4:3	Reserved	R/W	Write as default. Ignore on read.	0
2:0	LED_Refresh_rate	R/W	LED refresh count register (LED blinking rate) Refresh time = (N + 1) × 10 ms • 000 = Reserved • 001 = 20 ms/25 Hz • 010 = 30 ms/16 Hz • 011 = 40 ms/12 Hz (Default) • 100 = 50 ms/10 Hz • 101 = 60 ms/8 Hz • 110 = 70 ms/7 Hz • 111 = 80 ms/6 Hz	011

LED Function 0 Control Register (Page 00h: Address 10h–11h)

Table 42: LED Function 0 Control Register (Page 00h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:0	LED_FUNCTION 0	R/W	The following is the list of functions assigned to each bit: 15 = BroadSync HD LINK 14 = LNK 13 = LNK/ACT 12 = LNK/ACT/SPD[a] 11 = ACT 10 = 1G/ACT 9 = 100M/200M/ACT 8 = 10M/ACT 7 = Reserved 6 = Reserved 5 = DPX 4 = DPX/COL 3 = SPD1G 2 = SPD100M/200M 1 = SPD10M 0 = COL	LED MODE[1:0]=00: 16'h2024 LED MODE[1:0]=01: 16'h1021 LED MODE[1:0]=10: 16'h4804 LED MODE[1:0]=11: 16'hA010

a. 10 mbps blinking frequency is 1/4 of 100 mbps blinking frequency and is only available in auto_ mode.

LED Function 1 Control Register (Page 00h: Address 12h–13h)

Table 43: LED Function 1 Control Register (Page 00h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:0	LED_FUNCTION 1	R/W	The following is the list of functions assigned to each bit: 15 = BroadSync HD LINK 14 = LNK 13 = LNK/ACT 12 = LNK/ACT/SPD[a] 11 = ACT 10 = 1G/ACT 9 = 100M/200M/ACT 8 = 10M/ACT 7 = Reserved 6 = Reserved 5 = DPX 4 = DPX/COL 3 = SPD1G 2 = SPD100M/200M 1 = SPD10M 0 = COL	LED MODE[1:0]=00: 16'h2024 LED MODE[1:0]=01: 16'h1021 LED MODE[1:0]=10: 16'h4804 LED MODE[1:0]=11: 16'hA010

a. 10 mbps blinking frequency is 1/4 of 100 mbps blinking frequency and is only available in auto_ mode.

LED Function Map Register (Page 00h: Address 14h–15h)

Table 44: LED Function Map Register (Page 00h: Address 14h–15h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	LED_FUNC_MAP	R/W	Per port select function bit. Each port LED follows the function table specified for each port. 1 = Select function 1. 0 = Select function 0. • Bit 8 corresponds to port 8 in serial LED interface. • Bits [7:6] = Reserved • Bit 5 corresponds to port 5 in serial LED interface. • Bits [4:0] correspond to ports [4:0].	1FFh

LED Enable Map Register (Page 00h: Address 16h–17h)

Table 45: LED Enable Map Register (Page 00h: Address 16h–17h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	LED_EN_MAP	R/W	Per port LED enable bit 1 = Enable 0 = Disable • Bit 8 corresponds to port 8 in serial LED interface. • Bits [7:6] = Reserved • Bit 5 corresponds to port 5 in serial LED interface. • Bits [4:0] correspond to ports [4:0].	1Fh

LED Mode Map 0 Register (Page 00h: Address 18h–19h)

Table 46: LED Mode Map 0 Register (Page 00h: Address 18h–19h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	LED_MODE_MAP0	R/W	Per port LED output control • Bit 8 corresponds to port 8 in serial LED interface. • Bits [7:6] = Reserved • Bit 5 corresponds to port 5 in serial LED interface. • Bits [4:0] correspond to ports [4:0]. LED_MODE_MAP0 is used in conjunction with LED_MODE_MAP1 to determine the LED output. • [LED_MODE_MAP1, LED_MODE_MAP0] = 11: Auto. • [LED_MODE_MAP1, LED_MODE_MAP0] = 10: Blink. • [LED_MODE_MAP1, LED_MODE_MAP0] = 01: On. • [LED_MODE_MAP1, LED_MODE_MAP0] = 00: Off.	1FFh

LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)

Table 47: LED Mode Map 1 Control Register (Page 00h: Address 1Ah–1Bh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	LED_MODE_MAP1	R/W	Per port LED output control • Bit 8 corresponds to port 8 in serial LED interface. • Bits [7:6] = Reserved • Bit 5 corresponds to port 5 in serial LED interface. • Bits [4:0] correspond to ports [4:0]. LED_MODE_MAP1 is used in conjunction with LED_MODE_MAP0 to determine the LED output. • [LED_MODE_MAP1, LED_MODE_MAP0] = 11: Auto. • [LED_MODE_MAP1, LED_MODE_MAP0] = 10: Blink. • [LED_MODE_MAP1, LED_MODE_MAP0] = 01: On. • [LED_MODE_MAP1, LED_MODE_MAP0] = 00: Off.	1FFh

LED Options Register (Page 00h: Address 1Ch)

Table 48: LED Options Register (Page 00h: Address 1Ch)

Bit	Name	R/W	Description	Default
7:2	Reserved	R/W	Write as default. Ignore on read.	0
1	RX_Only_Activity	R/W	Enables RX-only activity indication When enable, TX activities and COL are masked out. ACT only presents RX activity.	0
0	Reserved	R/W	Write as default. Ignore on read.	0

Switch Control Register (Page 00h: Address 20h)

Table 49: Switch Control Register (Page 00h: Address 20h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	Write as default. Ignore on read.	–
4	MII2_INT_Volt_Sel	R/W	MII2 Interface Voltage Select 1 = 2.5V 0 = 3.3V (Default)	0h

Table 49: Switch Control Register (Page 00h: Address 20h) (Cont.)

Bit	Name	R/W	Description	Default
3	MII1_INT_Volt_Sel	R/W	MII1 Interface Voltage Select 1 = 2.5V (When configured as RGMII mode) 0 = 3.3V (Others)	1 (RGMII mode) 0 (Others)
2:1	Reserved	R/W	Write as default. Ignore on read.	0
0	MII_DUMB_FWD_En	R/W	Enables Port[8] to be a destination port in unmanaged mode 1 = Enable 0 = Disable (Default)	0

Port Forward Control Register (Page 00h: Address 21h)

Table 50: Port Forward Control Register (Page 00h: Address 21h)

Bit	Name	R/W	Description	Default
7	MCST_DLF_FWD_EN	R/W	1 = Forward multicast lookup failed frames according to "Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)" 0 = Flood multicast packet if fail ARL table lookup	0
6	UCST_DLF_FWD_EN	R/W	1 = Forward unicast lookup failed frames according to "Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)" 0 = Flood unicast packet if fail ARL table lookup	0h
5:3	Reserved	R/W	Write as default. Ignore on read.	0
2	In_Range_Error_Discard	R/W	In Range Error Discard When enabled, the ingress port discards any frames if the Length field mismatches the frame length. In Range Error Frame is any frame received with good CRC and one of the following: • The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number of (MAC Client Data + Padding) data octets received. • The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding). 1 = Enable 0 = Disable (Default)	0

Table 50: Port Forward Control Register (Page 00h: Address 21h) (Cont.)

Bit	Name	R/W	Description	Default
1	Out_Of_Range_Error_Discard		Out of Range Error Discard When enabled, the ingress port discards any frames if the Length field is between 1500 and 1536 (excluding 1500 and 1536) and with good CRC. ***Note:*** This option only controls the length field checking but not the frame length checking. 1 = Enable 0 = Disable (Default)	0
0	IP_MULTICAST	R/W	1 = Supports new 4K IP_Multicast address scheme. 0 = It is illegal to set this bit to zero.	1

Preserve Ingress Packet Format Control Register (Page 00h: Address 22h–23h)

Table 51: Preserve Ingress Packet Format Control Register (Page 00h: Address 22h–23h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	Preserve_Ingress_Pkt_Format	R/W	Preserve Per Port Ingress Packet Format • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 1 = Enable 0 = Disable This register is a per-port configuration. Users should also set this register for the ingress port, which is in port-cross-connect mode. When enabled, regardless the frame is untagged, 1Q/1p tagged or double-tagged the ingress frame format is preserved without being affected by the ingress logic normalization process and the egress logic tag/untag process. However, the ingress logic can still insert the timestamp if required, and if Broadcom header is enabled, the ingress/egress logic can still remove/insert the Broadcom header, respectively.	0

Protected Port Selection Register (Page 00h: Address 24h–25h)

Table 52: Protected Port Selection Register (Page 00h: Address 24h–25h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	PORT_SELECT	R/W	Protected port selection • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 1 = Port protected. Cannot send/receive to other protected ports. 0 = Port is not protected.	0

See "Protected Ports" on page 43 for more information.

WAN Port Select Register (Page 00h: Address 26h–27h)

Table 53: WAN Port Select Register (Page 00h: Address 26h–27h)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as default. Ignore on read.	0
9	EN_MAN_TO_WAN	R/W	1 = Management port could send nonegress direct frame to WAN port 0 = Management port sends only egress direct frame to WAN port	0
8:6	Reserved	R/W	Write as default. Ignore on read.	0
5:0	WAN_PORT_MAP	R/W	WAN port selection 1 = Corresponding bit when set selects the port as WAN port. Bits [5:0] correspond to ports 5–0, respectively. ***Note:*** Port 5 can be selected as a WAN port only when IMP1 is disabled.	0

Pause Capability Register (Page 00h: Address 28h–2Bh)

Table 54: Pause Capability Register (Page 00h: Address 28h–2Bh)

Bit	Name	R/W	Description	Default
31:24	Reserved	R/W	Write as default. Ignore on read.	0
23	EN_OVERRIDE	R/W	Forces the content of this register setting to be used over the auto negotiation result.	0
22:18	Reserved	R/W	Write as default. Ignore on read.	–
17:9	EN_RX_PAUSE_CAP	–	Enabling the receive pause capability. • Bit 17 = IMP port • Bits [16:15] = Reserved • Bits [14:9] correspond to ports 5–0, respectively	0h
8:0	EN_TX_PAUSE_CAP	–	Enables the transmit pause capability. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0h

Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)

Table 55: Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	UNI_DLF_MAP	R/W	Unicast lookup failed forward map • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. When the UCST_DLF_FWD_EN bit in "Port Forward Control Register (Page 00h: Address 21h)" on page 144 is enabled and a unicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a unicast lookup failure to this port. 1 = Forward a unicast lookup failure to this port.	0

See "Unicast Addresses" on page 52 for more information.

Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Table 56: Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	MCST_DLF_MAP	R/W	Multicast lookup failed forward map • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. When the MCST_DLF_FWD_EN bit in "Port Forward Control Register (Page 00h: Address 21h)" on page 144 is enabled and a multicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a multicast lookup failure to this port. 1 = Forward a multicast lookup failure to this port.	0

See "Multicast Addresses" on page 53 for more information.

MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)

Table 57: MLF IMPC Forward Map Register (Page 00h: Address 36h–37h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	MLF_IPMC_FWD_MAP	R/W	IPMC forward map • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0

Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Table 58: Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 58: Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Bit	Name	R/W	Description	Default
8:0	IGNORE_PAUSE FRAME _RX	R/W	RX pause pass through map 1 = Ignore IEEE 802.3x 0 = Comply with IEEE 802.3x pause frame receiving. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. ***Note:*** There is no support for pause frame pass through over the IMP port. It is illegal to write 1 to bit 8.	0

Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

Table 59: Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	IGNORE_PAUSE FRAME _TX	R/W	TX pause pass through map 1 = Ignore IEEE 802.3x. 0 = Comply with IEEE 802.3x pause frame receiving • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0

Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Table 60: Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 60: Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
8:0	DIS_LEARNING	R/W	Port bit mask to disable learning • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively 1 = Disable learning. When disabled, the BCM53101M does not do the following: • Learn entries to ARL • Refresh entries to ARL • Support software learning 0 = Enable learning	0

Software Learning Control Register (Page 00h: Address 3Eh–3Fh)

Table 61: Software Learning Control Register (Page 00h: Address 3Eh–3Fh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	–
8:0	SW_LEARN_CNTL	R/W	Software Learning Control. 1 = Software learning control enabled. • Forwarding behavior: Incoming packet with unknown SA will be copied to the CPU port. • Learning behavior: Allow S/W to decide whether to learn the incoming packet or not. In S/W learning mode, the H/W learning mechanism is disabled automatically. • Refresh behavior: Allow refresh mechanism to operate properly even though the H/W learning is disabled. ***Note:*** This field has no effect if disable learning is already enabled in "Disable Learning Register (Page 00h: Address 3Ch–3Dh)" on page 149 ***Note:*** It is not allowed to enable software learning for WAN port, since all frames from WAN port are already send to the IMP port. 0 = Software learning control disabled. • Forwarding/Learning/Refresh behavior default to hardware operation. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0

PHY Control Register (Page 00h: Address 48h–49h)

Table 62: PHY Control Register (Page 00h: Address 48h–49h)

Bit	Name	R/W	Description	Default
15:5	Reserved	R/W	Write as default. Ignore on read.	0
4:0	Per PHY Reset	R/W	Per-port PHY reset Set these bits to reset the corresponding PHYs. These bits must be asserted for at least 400 ns while the system clock is running. After deassertion, no PHY activity is allowed for 100 µs. Bits [4:0] corresponds to ports 4–0.	0

PHY Power-Down Register (Page 00h: Address 4Ah–4Dh)

Table 63: PHY Power-Down Register (Page 00h: Address 4Ah–4Dh)

Bit	Name	R/W	Description	Default
31	EXT_PWR_DOWN_DLL	R/W	Power-down DLL When active, the internal PLL is put into power-down mode.	
30	EXT_PWR_DOWN_BIAS	R/W	Power-down bias When active, the internal bias is put into power-down mode. The PHY ENERGY_DET output is not valid when this input is active.	
29:25	Reserved	R/W	Write as default. Ignore on read.	–
24:20	EXT_PWR_DOWN_PHY_TX	R/W	Power-down PHY transmitter When active, these bits put the corresponding PHY transmitters into power-down mode. When power-down mode is revoked, the corresponding PHYs must be reset using the Per PHY Reset bits of the PHY Control Register (Page 00h: Address 48h–49h). Bits [24:20] correspond to ports 4–0.	0
19:15	EXT_PWR_DOWN_PHY_RX	R/W	Power-down PHY receiver When active, these bits put the corresponding PHY receivers into power-down mode. When power-down mode is revoked, the corresponding PHYs must be reset using the Per PHY Reset bits of the PHY Control Register (Page 00h: Address 48h–49h). Bits [19:15] correspond to ports 4–0.	

Table 63: PHY Power-Down Register (Page 00h: Address 4Ah–4Dh) (Cont.)

Bit	Name	R/W	Description	Default
14:10	EXT_PWR_DOWN_PHY_SD	R/W	Power-down PHY signal detect When active, these bits put the corresponding PHY signal detect function into power-down mode. When power-down mode is revoked, the corresponding PHYs must be reset using the Per PHY Reset bits of the PHY Control Register (Page 00h: Address 48h–49h). Bits [14:10] correspond to ports 4–0.	
9:5	EXT_PWR_DOWN_PHY_RD	R/W	Power-down PHY reset divider When active, these bits put the corresponding PHY reset divider into power-down mode. When power-down mode is revoked, the corresponding PHYs must be reset using the Per PHY Reset bits of the PHY Control Register (Page 00h: Address 48h–49h). Bits [9:5] correspond to ports 4–0.	
4:0	EXT_PWR_DOWN_PHY_EN	R/W	Power-down PHY enable When active, these bits put the corresponding PHY into power-down mode. When power-down mode is revoked, the corresponding PHYs must be reset using the Per PHY Reset bits of the PHY Control Register (Page 00h: Address 48h–49h). Bits [4:0] correspond to ports 4–0.	

PHY Status Register (Page 00h: Address 4Eh–4Fh)

Table 64: PHY Status Register (Page 00h: Address 4Eh–4Fh)

Bit	Name	R/W	Description	Default
15	PHY_PLL_LOCK	R/W	PLL Lock Indicator	0
14:5	Reserved	R/W	Write as default. Ignore on read.	0
4:0	PHY ENERGY_DET	R/W	PHY Energy Detect Output When active, this indicates the presence of a signal on the corresponding RD± receive analog pair. Bits [4:0] correspond to ports 4–0.	0

Port N(0–5) Port State Override Register (Page 00h: Address 58h–5Dh)

Table 65: Port N(0–5) Port State Override Register Address Summary

Address	Description
58h	Port 0
59h	Port 1
5Ah	Port 2
5Bh	Port 3
5Ch	Port 4
5Dh	Port 5

Table 66: Port State Override Register (Page 00h: Address 58h–5Dh)

BIt	Name	R/W	Description	Default
7	Reserved	R/W	Write as default. Ignore on read.	0
6	Software Override	R/W	Writing 1 to this bit allows the values of the bits [5:0] to be written to the external PHY. Writing 0 to this bit prevents these values from overriding the present external PHY conditions.	0
5	TX Flow Control Enable	R/W	Value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for transmit traffic. 1 = Flow control enabled for transmit traffic.	0
4	RX Flow Control Enable	R/W	Value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for receive traffic. 1 = Flow control enabled for receive traffic.	0
3:2	Speed	R/W	Value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Illegal state for ports [4–0] 11 = 200 Mbps. This enables TMII function in port 5.	10
1	Duplex Mode	R/W	Value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Half duplex 1 = Full duplex	1
0	Link State	R/W	Value of this bit overrides the existing conditions of the external PHY port if bit 6 is written 1. 1 = Link-up 0 = Link-down	1

IMP RGMII Control Register (Page 00h: Address 60h)

Table 67: IMP RGMII Control Register (Page 00h: Address 60h)

Bit	Name	R/W	Description	Default
7:2	Reserved	R/W	Write as default. Ignore on read.	0
1	RGMII_DLL_RXC_ENABLE	R/W	1 = RGMII RXC clock delay by DLL is enabled (delay mode) 0 = RGMII RXC clock delay by DLL is disabled (normal mode)	0
0	RGMII_DLL_TXC_ENABLE	R/W	1 = RGMII TXC clock delay by DLL is enabled (delay mode) 0 = RGMII TXC clock delay by DLL is disabled (normal mode)	0

MDIO WAN Port Address Register (Page 00h: Address 75h)

Table 68: MDIO WAN Port Address Register (Page 00h: Address 75h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	Write as default. Ignore on read.	0
4:0	WAN_MDIO_ADDRESS	R/W	WAN port MDIO SCAN address	15h

MDIO IMP PORT Address Register (Page 00h: Address 78h)

Table 69: MDIO IMP PORT Address Register (Page 00h: Address 78h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	Write as default. Ignore on read.	0
4:0	IMP_MDIO_ADDRESS	R/W	IMP PORT MDIO address	18h

Watch Dog Control 0 Register (Page 00h: Address 79h)

Table 70: Watch Dog Control 0 Register (Page 00h: Address 79h)

Bit	Name	R/W	Description	Default
7	SW_RST	R/W	Software Reset Write 1 to activate a RESET, 0 to clear the reset state. 1 = Activate reset. 0 = Clear reset. ***Note:*** Bit 4 EN_SW_RST must be enabled as well.	0
6:5	Reserved	R/W	Write as default. Ignore on read.	N/A
4	EN_SW_RST	R/W	Enable global software reset.	0

Table 70: Watch Dog Control 0 Register (Page 00h: Address 79h) (Cont.)

Bit	Name	R/W	Description	Default
3:0	Reserved	R/W	Write as default. Ignore on read.	0

Pause Frame Detection Control Register (Page 00h: Address 80h)

Table 71: Pause Frame Detection Control Register (Page 00h: Address 80h)

Bit	Name	R/W	Description	Default
7:1	Reserved	R/W	Write as default. Ignore on read.	0
0	PAUSE_IGNORE_DA	R/W	0 = Check DA field on pause frame detection. 1 = Ignore DA field on pause frame detection.	0

Fast-Aging Control Register (Page 00h: Address 88h)

Table 72: Fast-Aging Control Register (Page 00h: Address 88h)

Bit	Name	R/W	Description	Default
7	Fast_Age_Start/Done	R/W	1 = Triggers fast-aging process When the fast-aging process is done, this bit is cleared to 0.	0
6	Reserved	R/W	Write as default. Ignore on read.	–
5	EN_AGE_MCAST	R/W	Enable aging multicast entry 1 = Aging multicast entries in ARL table 0 = Disable aging multicast entries in ARL table ***Note:*** EN_AGE_MCAST and EN_AGE_Port cannot be enabled (set to 1) at the same time.	0
4	EN_AGE_SPT	R/W	When set, check spanning tree ID.	0
3	EN_AGE_VLAN	R/W	When set, check VLAN ID.	0
2	EN_AGE_Port	R/W	When set, check port ID.	0
1	EN_AGE_Dynamic	R/W	When set, age out dynamic entry.	1
0	EN_AGE_Static	R/W	When set, age out static entry.	0

Fast-Aging Port Control Register (Page 00h: Address 89h)

Table 73: Fast-Aging Port Control Register (Page 00h: Address 89h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	Write as default. Ignore on read.	0
3:0	AGE_PORT	R/W	Fast-aging source port select Writing bits [3:0] selects the Port ID to be fast-aged.	0

Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Table 74: Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11:0	Fast Age Single VID	R/W	Writing bits [11:0] selects the VID to be fast-aged.	0

Port Cross Connect Destination Register (Page 00h: Address 90h–A1h)

Table 75: Port Cross Connect Destination Register Address Summary

Address	Description
90h–91h	Port 0
92h–93h	Port 1
94h–95h	Port 2
96h–97h	Port 3
98h–99h	Port 4
9Ah–9Bh	Port 5
9Ch–9Dh	Reserved
9Eh–9Fh	Reserved
A0h–A1h	IMP port

Table 76: Port Cross Connect Destination Register (Page 00h: Address 90h–A1h)

Bit	Name	R/W	Description	Default
15	PCC_Enable	R/W	Per-port cross connect enable Setting this field to 1 enables the port to operate in cross connect mode. The port-cross-connect decision overrules all ARL decisions. Therefore MAC-LAND packets (MACDA = MACSA), which are originally dropped by the ARL, pass through in port-cross-connect mode. However, DoS-attack drop still takes effect when enabled. It is recommended that user should also configure disable-learning and preserve-ingress-packet-format.	0
14:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 76: Port Cross Connect Destination Register (Page 00h: Address 90h–A1h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	PCC_Destination[8:0]		Per-bit per-port cross connect destination mask Bit mask corresponding to the physical ports. Setting a bit to 1 indicates that it is the destination port. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. When a receive port is configured to be in the cross connect mode, all received packets are forwarded to the destination ports specified by this register, regardless of the result of the layer 2 lookup operation.	0

PLL Control Register (Page 00h: Address DCh)

Table 77: PLL Control Register (Page 00h: Address DCh)

Bit	Name	R/W	Description	Default
7	PLL_ARESET	R/W	PLL analog reset Software must reset the analog/digital circuit when releasing PLL global power-down or releasing PLL clock comparator power-down.	0
6	PLL_DRESET	R/W	PLL digital reset Software must reset the analog/digital circuit when releasing PLL global power-down or releasing PLL clock comparator power-down.	0
5	Reserved	RO	Write as default. Ignore on read.	0
4:0	PLL_POWER_DOWN_CTRL	R/W	PLL power-down control [4] = PLL global power-down [3] = Clock comparator power-down [2] = Channel 1 power-down [1] = Channel 2 power-down [0] = Channel 3 power-down	0

Low Power Control Register (Page 00h: Address DFh)

Table 78: Low Power Control Register (Page 00h: Address DFh)

Bit	Name	R/W	Description	Default
7	LOW_POWER_ENABLE	R/W	When enabled, the system clock becomes a low-power clock source. $systemClock = \frac{CK25}{2}$	0
6	SLEEP_SYS	R/W	Write as default. Ignore on read.	0
5	SLEEP_MAC	R/W	1 = Stop MAC source clocks for P5 and P8.	
4:0	Reserved	R/W	Write as default. Ignore on read.	0

Bonding Pad Status Register (Page 00h: Address EEh)

Table 79: Bonding Pad Status Register (Page 00h: Address EEh)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Write as default. Ignore on read.	0
1:0	BOND_53101[1:0]	RO	Bonding options	11

Page 01h: Status Registers

Table 80: Status Registers (Page 01h)

Address	Bits	Register Name
00h–01h	16	"Link Status Summary Register (Page 01h: Address 00h–01h)" on page 159
02h–03h	16	"Link Status Change Register (Page 01h: Address 02h–03h)" on page 160
04h–07h	32	"Port Speed Summary Register (Page 01h: Address 04h–07h)" on page 160
08h–09h	16	"Duplex Status Summary Register (Page 01h: Address 08h–09h)" on page 160
0Ah–0Dh	32	"Pause Status Summary Register (Page 01h: Address 0Ah–0Dh)" on page 161
0Eh–0Fh	16	"Source Address Change Register (Page 01h: Address 0Eh–0Fh)" on page 161
10h–45h	48/port	"Last Source Address Register (Page 01h: Address 10h–45h)" on page 162
46h–6Fh	–	Reserved
70h–75h	–	"Strap Pin Status Register (Page 01h: Address 70h–75h)" on page 162
76h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Link Status Summary Register (Page 01h: Address 00h–01h)

Table 81: Link Status Summary Register (Page 01h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Ignore on read	0
8:0	LINK_STATUS	RO	Link status 9-bit field indicates link status for each port: • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Link fail 1 = Link pass	N/A

Link Status Change Register (Page 01h: Address 02h–03h)

Table 82: Link Status Change Register (Page 01h: Address 02h–03h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Ignore on read	0
8:0	LINK_STATUS_CHANGE	RO	Link status change • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link status constant. 1 = Link status change.	1FFh

Port Speed Summary Register (Page 01h: Address 04h–07h)

Table 83: Port Speed Summary Register (Page 01h: Address 04h–07h)

Bit	Name	R/W	Description	Default
31:18	Reserved	R/W	Write as default. Ignore on read.	0
17:0	PORT_SPEED	RO	Port speed Speed of each port is reported based on the mapping below: • Bits [17:16] = IMP port • Bits [15:12] = Reserved • Bits [11:10] = Port 5 • Bits [9:8] = Port 4 • Bits [7:6] = Port 3 • Bits [5:4] = Port 2 • Bits [3:2] = Port 1 • Bits [1:0] = Port 0 Bit values are as follows: • 00 = 10 Mbps • 01 = 100 Mbps • 10 = 1000 Mbps • 11 = 200 Mbps (ports 5 and 8 only, when configured in TMII/RvTMII mode)	N/A

Duplex Status Summary Register (Page 01h: Address 08h–09h)

Table 84: Duplex Status Summary Register (Page 01h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as default. Ignore on read.	0

Table 84: Duplex Status Summary Register (Page 01h: Address 08h–09h)

Bit	Name	R/W	Description	Default
8:0	DUPLEX_STATE	RO	Duplex state • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Half duplex 1 = Full duplex	N/A

Pause Status Summary Register (Page 01h: Address 0Ah–0Dh)

Table 85: PAUSE Status Summary Register (Page 01h: Address 0Ah–0Dh)

Bit	Name	R/W	Description	Default
31:18	Reserved	RO	Write as default. Ignore on read.	0
17:9	RECEIVE_PAUSE_STATE	RO	Pause state. Receive pause capability • Bit 17 = IMP port • Bits [16:15] = Reserved • Bits [14:9] correspond to ports 5–0, respectively. 0 = Disabled 1 = Enabled	N/A
8:0	TRANSMIT_PAUSE_STATE	RO	Transmit pause capability • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Disabled 1 = Enabled	N/A

Source Address Change Register (Page 01h: Address 0Eh–0Fh)

Table 86: Source Address Change Register (Page 01h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 86: Source Address Change Register (Page 01h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
8:0	SRC_ADDR_CHANGE	RC	Source address change • Bit 8 = IMP port • Bits [4:0] correspond to ports [4:0], respectively. Bit value is 1 if a change in the source address is detected on the given port. Bit remains set until cleared by a read operation. 0 = No change in source address since last read 1 = Source address has changed since last read.	0

Last Source Address Register (Page 01h: Address 10h–45h)

Table 87: Last Source Address Register Address Summary

Address	Description
10h–15h	Port 0
16h–1Bh	Port 1
1Ch–21h	Port 2
22h–27h	Port 3
28h–2Dh	Port 4
2Eh–33h	Port 5
34h–39h	Reserved
3Ah–3Fh	Reserved
40h–45h	IMP port

Table 88: Port N Last Source Address (Page 01h: Address 10h–45h)

Bit	Name	R/W	Description	Default
47:0	LAST_SOURCE_ADD	RO	48-bit source address detected on the last packet ingressed	0

Strap Pin Status Register (Page 01h: Address 70h–75h)

Table 89: Strap Pin Status Register (Page 01h: Address 70h–75h)

Bit	Name	R/W	Description	Default
47:21	Reserved	RO	Ignore on read	0
20:19	FINAL_MII2_MODE	RC	Final MII2 mode according to bonding options	Depends on strap pins

Table 89: Strap Pin Status Register (Page 01h: Address 70h–75h) (Cont.)

Bit	Name	R/W	Description	Default
18:16	FINAL_MII1_MODE		Final MII1 mode according to bonding options	Depends on strap pins
15:13	Reserved	RO	Ignore on read	0
12:0	STRAP_VALUE_VECTOR	RO	Display strap pin value Bit 12 = Reserved Bit 11:10 = STRAP_LED_MODE[1:0] Bit 9:8 = STRAP_MII2_MODE[1:0] Bit 7 = Reserved Bit 6:4 = STRAP_MII1_MODE[2:0] Bit 3:2 = STRAP_CLOCK freq[1:0] Bit 1 = STRAP_CPU_EPROM_SEL Bit 0 = STRAP_HW_FWDG_EN	Depends on strap pins

Page 02h: Management/Mirroring Registers

Table 90: Management/Mirroring Registers (Page 02h)

Address	Bits	Register Name
00h	8	"Global Management Configuration Register (Page 02h: Address 00h)" on page 164
01h–02h	–	Reserved
03h	8	"Broadcom Header Control Register (Page 02h: Address 03h)" on page 165
04h–05h	16	"RMON MIB Steering Register (Page 02h: Address 04h–05h)" on page 165
06h–09h	32	"Aging Time Control Register (Page 02h: Address 06h–09h)" on page 166
0Ah–OBh	–	Reserved
0Ch–0Fh	32	"IPG Shrink Control Register (Page 02h: Address 0Ch–0Fh)" on page 166
10h–11h	16	"Mirror Capture Control Register (Page 02h: Address 10h–11h)" on page 166
12h–13h	16	"Ingress Mirror Control Register (Page 02h: Address 12h–13h)" on page 167
14h–15h	16	"Ingress Mirror Divider Register (Page 02h: Address 14h–15h)" on page 168
16h–1Bh	48	"Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)" on page 168
1Ch–1Dh	16	"Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)" on page 169
1Eh–1Fh	16	"Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)" on page 170

Table 90: Management/Mirroring Registers (Page 02h) (Cont.)

Address	Bits	Register Name
20h–25h	48	"Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)" on page 170
26h–3Fh	–	Reserved
30h–33h	32	"Device ID Register (Page 02h: Address 30h–33h)" on page 170
34h–3Fh	–	Reserved
40h	8	"Revision Number Register (Page 02h: Address 40h)" on page 170
41h–4Fh	–	Reserved
50h–53h	32	"High-Level Protocol Control Register (Page 02h: Address 50h–53h)" on page 171
54h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Global Management Configuration Register (Page 02h: Address 00h)

Table 91: Global Management Configuration Register (Page 02h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	En_IMP_Port	R/W	IMP port enable Enables IMP function under management mode. 00 = No frame management port 01 = Reserved 10 = Enable IMP port (IMP0) only. All traffic to CPU from LAN and WAN ports is forwarded to IMP0 port. 11 = Enable Dual-IMP ports (both IMP0 port and IMP1). All traffic to CPU from LAN ports is forwarded to IMP0 port and all traffic from WAN ports is forwarded to IMP1. Bits ignored when SW_FWDG_MODE = Unmanaged in "Switch Mode Register (Page 00h: Address 0Bh)" on page 137. ***Note:*** IMP0 is port 8 and IMP1 is port 5. ***Note:*** When only IMP0 is enabled (En_IMP_Port = 10), IMP0 is also called IMP port.	00
5:2	Reserved	R/W	Write as default. Ignore on read.	0
1	En_Rx_BPDU	R/W	Receive BPDU enable Enables all ports to receive BPDUs and forwards to the IMP port. This bit must be set to allow BPDUs to be received globally.	0

Table 91: Global Management Configuration Register (Page 02h: Address 00h)

Bit	Name	R/W	Description	Default
0	Reset MIB	R/W	Reset MIB counters Resets all MIB counters for all ports to 0 (pages 20h–28h). This bit must be set and then cleared in successive write cycles to activate the reset operation.	0

Broadcom Header Control Register (Page 02h: Address 03h)

Table 92: Broadcom Header Control Register (Page 02h: Address 03h)

Bit	Name	R/W	Description	Default
7:2	Reserved	R/W	Write as default. Ignore on read.	0
1:0	BRCM_HDR_EN	R/W	Broadcom Tag enable for IMP Port Bit 1 = Enable BRCM header for IMP1 port. (Only when IMP1 is enabled). Bit 0 = Enable BRCM header for IMP0 port. • 1 = BRCM header is required. Additional BRCM header information is inserted between the SA and Type/ Length fields for egress frame. Host must insert an appropriate BRCM header on ingress frame. Any ingress frame without a proper BRCM header is discarded. • 0 = BRCM header is not required. IMP port ignores BRCM header on ingress frame and no BRCM header is inserted in the egress frame.	11

RMON MIB Steering Register (Page 02h: Address 04h–05h)

Table 93: RMON MIB Steering Register (Page 02h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	Override RMON Receive	R/W	Forces RMON packet size bucket counters from normal default of snooping on the receive side of the MAC to the transmit side. This setting allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively.	0

Aging Time Control Register (Page 02h: Address 06h–09h)

Table 94: Aging Time Control Register (Page 02h: Address 06h–09h)

Bit	Name	R/W	Description	Default
31:21	Reserved	R/W	Write as default. Ignore on read.	0
20	AGE_CHANGE_EN	R/W	Age change enable 1 = Set age time using bits [19:0] 0 = Age time default 600s	0
19:0	AGE_TIME	R/W	Specifies aging time in 0.5 seconds for dynamically learned addresses. Maximum age time is 524,287s. Setting AGE_TIME to 0 disables the aging process. For more information on ARL table aging, see "Address Aging" on page 57. ***Note:*** While 802.1D specifies a range of values of 10–1,000,000s, this register does not enforce this range.	600d

IPG Shrink Control Register (Page 02h: Address 0Ch–0Fh)

Table 95: IPG Shrink Control Register (Page 02h: Address 0Ch–0Fh)

Bit	Name	R/W	Description	Default
31:18	Reserved	R/W	Write as default. Ignore on read.	0
17:0	IPG_SHK_CTRL	R/W	IPG shrink control Specifies IPG for each port at egress. • Bit [17:16] = Port 8 • Bit [15:12] = Reserved • Bit [11:00] = Ports 5–0 Bit values are as follows: • 00 = No IPG shrinking (default) • 01 = IPG shrinks by 1-byte • 10 = IPG shrinks by 4-bytes • 11 = IPG shrinks by 5-bytes	0

Mirror Capture Control Register (Page 02h: Address 10h–11h)

Table 96: Mirror Capture Control Register (Page 02h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15	Mirror Enable	R/W	Global mirror enable 0 = Disable mirror capture feature. 1 = Enable mirror capture feature.	0

Table 96: Mirror Capture Control Register (Page 02h: Address 10h–11h) (Cont.)

Bit	Name	R/W	Description	Default
14	BLK_NOT_MIR	R/W	When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked, except for mirror traffic. Nonmirror traffic is disabled. 0 = No traffic blocking on mirror capture port 1 = Traffic to mirror capture port blocked unless mirror traffic	0
13:4	Reserved	R/W	Write as default. Ignore on read.	0
3:0	Mirror Capture Port ID	R/W	Binary value identifies single unique port designated as the port where all ingress or egress traffic is mirrored	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Ingress Mirror Control Register (Page 02h: Address 12h–13h)

Table 97: Ingress Mirror Control Register (Page 02h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:14	IN_MIRROR_FILTER	R/W	Ingress mirror filter Filters frames to be forwarded to the mirror capture port specified in "Mirror Capture Control Register (Page 02h: Address 10h–11h)" on page 166. 00 = Mirror all ingress frames. 01 = Mirror all ingress frames with DA = IN_MIRROR_MAC. 10 = Mirror all ingress frames with SA = IN_MIRROR_MAC. 11 = Reserved. IN_MIRROR_MAC is specified in the "Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)" on page 168.	0
13	IN_DIV_EN	R/W	Ingress divider enable Ingress divider mirrors every n^{th} ingress frame that has passed through the IN_MIRROR_FILTER (*n* represents the IN_MIRROR_DIV defined in "Ingress Mirror Divider Register (Page 02h: Address 14h–15h)" on page 168). 0 = Disable ingress divider feature. 1 = Enable ingress divider feature.	0
12:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 97: Ingress Mirror Control Register (Page 02h: Address 12h–13h) (Cont.)

Bit	Name	R/W	Description	Default
8:0	IN_MIRROR_MASK	R/W	Ingress mirror port mask • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. Ports with the corresponding bit set to 1 have ingress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an ingress mirror port, severe congestion or frame loss, or both, may occur if excessive bandwidth from the ingress mirrored port is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or divider using bit 13 may be helpful.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Ingress Mirror Divider Register (Page 02h: Address 14h–15h)

Table 98: Ingress Mirror Divider Register (Page 02h: Address 14h–15h)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as default. Ignore on read.	0
9:0	IN_MIRROR_DIV	R/W	Ingress mirror divider Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 12h–13h)" on page 167 is set, frames that pass the IN_MIRROR_FILTER rule are further divided by *n*, where *n* = IN_MIRROR_DIV + 1.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)

Table 99: Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)

Bit	Name	R/W	Description	Default
47:0	IN_MIRROR_MAC	R/W	Ingress mirror MAC address MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in "Ingress Mirror Control Register (Page 02h: Address 12h–13h)" on page 167.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)

Table 100: Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)

Bit	Name	R/W	Description	Default
15:14	OUT_MIRROR_FILTER	R/W	Egress mirror filter Filters egress frames that are forwarded to the mirror capture port specified in "Mirror Capture Control Register (Page 02h: Address 10h–11h)" on page 166. 00 = Mirror all egress frames. 01 = Mirror all egress frames with DA = OUT_MIRROR_MAC. 10 = Mirror all egress frames with SA = OUT_MIRROR_MAC. 11 = Reserved. OUT_MIRROR_MAC is specified in "Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)" on page 170.	0
13	OUT_DIV_EN	R/W	Egress divider enable Egress divider mirrors every n^{th} egress frame that has passed through the OUT_MIRROR_FILTER (*n* represents the OUT_MIRROR_DIV defined in the "Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)" on page 170). 0 = Disable egress divider feature. 1 = Enable egress divider feature.	0
12:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	OUT_MIRROR_MASK	R/W	Egress mirror port mask • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. Ports with the corresponding bit set to 1 have egress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an egress mirror port, severe congestion or frame loss, or both, may occur if excessive bandwidth from the egress mirrored port is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or a divider using bit 13 may be helpful.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)

Table 101: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as default. Ignore on read.	0
9:0	OUT_MIRROR_DIV	R/W	Egress mirror divider Egressed frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the "Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)" on page 169 is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by *n*, where *n* = OUT_MIRROR_DIV + 1.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)

Table 102: Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)

Bit	Name	R/W	Description	Default
47:0	OUT_MIRROR_MAC	R/W	Egress mirror MAC address MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules defined in "Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)" on page 169.	0

For additional information about port mirroring, see "Port Mirroring" on page 43.

Device ID Register (Page 02h: Address 30h–33h)

Table 103: Device ID Register (Page 02h: Address 30h–33h)

Bit	Name	R/W	Description	Default
31:0	Device_ID	RO	Device ID	32'0005_3101

Revision Number Register (Page 02h: Address 40h)

Table 104: Revision Number Register (Page 02h: Address 40h)

Bit	Name	R/W	Description	Default
7:0	Revision_ID	RO	Revision number	0

High-Level Protocol Control Register (Page 02h: Address 50h–53h)

Table 105: High-Level Protocol Control Register (Page 02h: Address 50h–53h)

Bit	Name	R/W	Description	Default
31:19	Reserved	R/W	Write as default. Ignore on read.	–
18	MLD_QRY_FWD_MODE	R/W	MLD query message forwarding mode 1 = MLD query message frames are trapped to CPU port only 0 = MLD query message frames are forwarded by L2 result and also copied to CPU	0
17	MLD_QRY_EN	R/W	MLD query message snooping/redirect enable 1 = Enable MLD query message snooping/ redirect. 0 = Disable	0
16	MLD_RPTDONE_FWD_MODE	R/W	MLD report/done message forwarding mode 1 = MLD report/done message frames are trapped to CPU port only 0 = MLD report/done message frames are forwarded by L2 result and also copied to CPU	0
15	MLD_RPTDONE_EN	R/W	MLD report/done message snooping/redirect enable 1 = Enable MLD report/done message snooping/ redirect. 0 = Disable	0
14	IGMP_UKN_FWD_MODE	R/W	IGMP unknown message forwarding mode 1 = IGMP unknown message frames are trapped to CPU port only 0 = IGMP Unknown Message frames are forwarded by L2 result and also copied to CPU	0
13	IGMP_UKN_EN	R/W	IGMP unknown message snooping/redirect enable 1 = Enable IGMP unknown message snooping/ redirect. 0 = Disable	0
12	IGMP_QRY_FWD_MODE	R/W	IGMP query message forwarding mode 1 = IGMP query message frames are trapped to CPU port only 0 = IGMP query message frames are forwarded by L2 result and also copied to CPU	0
11	IGMP_QRY_EN	R/W	IGMP query message snooping/redirect enable 1 = Enable IGMP query message snooping/ redirect 0 = Disable	0

Table 105: High-Level Protocol Control Register (Page 02h: Address 50h–53h) (Cont.)

Bit	Name	R/W	Description	Default
10	IGMP_RPTLVE_FWD_MODE	R/W	IGMP report/leave message forwarding mode 1 = IGMP report/leave message frames are trapped to CPU port only 0 = IGMP report/leave message frames are forwarded by L2 result and also copied to CPU	0
9	IGMP_RPTLVE_EN	R/W	IGMP report/leave message snooping/redirect enable 1 = Enable IGMP report/leave message Snooping/Redirect 0 = Disable	0
8	IGMP_DIP_EN	R/W	IGMP L3 DIP checking enable In addition to the IP datagram with a protocol value of 2, IGMP are classified by matching its DIP with the Class D IP address (224.0.0.0–239.255.255.255).	0
7:6	Reserved	R/W	Write as default. Ignore on read.	0
5	ICMPv6_FWD_MODE	R/W	ICMPv6 (exclude MLD) forwarding mode 1 = ICMPv6 frames are trapped to CPU port only. 0 = ICMPv6 frames are forwarded by L2 result and also copied to CPU.	0
4	ICMPv6_EN	R/W	ICMPv6 (exclude MLD) snooping/redirect enable ICMPv6 with a next header value of 58 are classified by IPv6 datagram.	0
3	ICMPv4_EN	R/W	ICMPv4 snooping enable 1 = ICMPv4 frames are forwarded by L2 result and also copied to CPU. 0 = ICMPv4 frames are forwarded by L2 result.	0
2	DHCP_EN	R/W	DHCP snooping enable 1 = DHCP frames are forwarded by L2 result and also copied to CPU. 0 = DHCP frames are forwarded by L2 result.	0
1	RARP_EN	R/W	RARP snooping enable 1 = RARP frames are forwarded by L2 result and also copied to CPU. 0 = RAPR frames are forwarded by L2 result.	0
0	ARP_EN	R/W	ARP snooping enable 1 = ARP frames are forwarded by L2 result and also copied to CPU. 0 = ARP frames are forwarded by L2 result.	0

Page 04h: ARL Control Register

Table 106: ARL Control Registers (Page 04h)

Address	Bits	Register Name
00h	8	"Global ARL Configuration Register (Page 04h: Address 00h)" on page 174
01h–03h	–	Reserved
04h–09h	48	"BPDU Multicast Address Register (Page 04h: Address 04h–09h)" on page 174
0Ah–0Dh	–	Reserved
0Eh–0Fh	16	"Multiport Control Register (Page 04h: Address 0Eh–0Fh)" on page 175
10h–17h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
18h–1Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
1Ch–1Fh	–	Reserved
20h–27h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
28h–2Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
2Ch–2Fh	–	Reserved
30h–37h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
38h–3Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
3Ch–3Fh	–	Reserved
40h–47h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
48h–4Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
4Ch–4Fh	–	Reserved
50h–57h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
58h–5Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
5Ch–5Fh	–	Reserved
60h–67h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176
68h–6Bh	32	"Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)" on page 177
6Ch–FEh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved

Table 106: ARL Control Registers (Page 04h) (Cont.)

Address	Bits	Register Name
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Global ARL Configuration Register (Page 04h: Address 00h)

Table 107: Global ARL Configuration Register (Page 04h: Address 00h)

Bit	Name	R/W	Description	Default
7:3	Reserved	R/W	Write as default. Ignore on read.	0
2	AGE_Accelerate	R/W	When enabled, aging time is reduced by 1/128. 1 = Accelerate aging 128 times. 0 = Keep original age process.	0
1	Reserved	R/W	Write as default. Ignore on read.	1
0	Hash Disable	R/W	Disables the hash function of the ARL table so that entries are directly mapped to the table instead of being hashed to an index. 1 = Disable hash function. 0 = Enable hash function (default). For more information see "Address Table Organization" on page 50.	0

BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Table 108: BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/W	BPDU multicast address 1 Defaults to IEEE 802.1-defined reserved multicast address for bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address are forwarded to the designated management port.	01-80-c2-00-00-00

Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Table 109: Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	MPORT0_TS_EN	R/W	MPort 0 timestamp enable 1 = Packet is timestamped if forwarded to CPU. MPORT_VECTOR0 should be programmed to CPU only if this bit is set. 0 = Packet is not timestamped.	0
14:12	Reserved	R/W	Write as default. Ignore on read.	0
11:10	MPORT_CTRL5	R/W	Multiport 5 control 00 = Disable multiport 5 forward. 10 = Compare MPORT_ADD5 only; forward based on MPORT_Vector 5 if matched. 01 = Compare MPORT_ETYPE5 only; forward based on MPORT_Vector 5 if matched. 11 = Compare MPORT_ETYPE5 and MPORT_ADD5; forward based on MPORT_Vector 5 if matched.	00
9:8	MPORT_CTRL4	R/W	Multiport 4 control 00 = Disable multiport 4 forward. 10 = Compare MPORT_ADD4 only; forward based on MPORT_Vector 4 if matched. 01 = Compare MPORT_ETYPE4 only; forward based on MPORT_Vector 4 if matched. 11 = Compare MPORT_ETYPE4 and MPORT_ADD4; forward based on MPORT_Vector 4 if matched.	00
7:6	MPORT_CTRL3	R/W	Multiport 3 control 00 = Disable multiport 3 forward. 10 = Compare MPORT_ADD3 only; forward based on MPORT_Vector 3 if matched. 01 = Compare MPORT_ETYPE3 only; forward based on MPORT_Vector 3 if matched. 11 = Compare MPORT_ETYPE3 and MPORT_ADD3; forward based on MPORT_Vector 3 if matched.	00
5:4	MPORT_CTRL2	R/W	Multiport 2 control 00 = Disable multiport 2 forward. 10 = Compare MPORT_ADD2 only; forward based on MPORT_Vector 2 if matched. 01 = Compare MPORT_ETYPE2 only; forward based on MPORT_Vector 2 if matched. 11 = Compare MPORT_ETYPE2 and MPORT_ADD2; forward based on MPORT_Vector 2 if matched.	00

Table 109: Multiport Control Register (Page 04h: Address 0Eh–0Fh) (Cont.)

Bit	Name	R/W	Description	Default
3:2	MPORT_CTRL1	R/W	Multiport 1 control 00 = Disable multiport 1 forward. 10 = Compare MPORT_ADD1 only; forward based on MPORT_Vector 1 if matched. 01 = Compare MPORT_ETYPE1 only; forward based on MPORT_Vector 1 if matched. 11 = Compare MPORT_ETYPE1 and MPORT_ADD1; forward based on MPORT_Vector 1 if matched.	00
1:0	MPORT_CTRL0	R/W	Multiport 0 control 00 = Disable multiport 0 forward. 10 = Compare MPORT_ADD0 only; forward based on MPORT_Vector 0 if matched. 01 = Compare MPORT_ETYPE0 only; forward based on MPORT_Vector 0 if matched. 11 = Compare MPORT_ETYPE0 and MPORT_ADD0; forward based on MPORT_Vector 0 if matched.	00

Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)

Table 110: Multiport Address Register Address Summary

Address	Description
10h–17h	Multiport ETYPE address 0
20h–27h	Multiport ETYPE address 1
30h–37h	Multiport ETYPE address 2
40h–47h	Multiport ETYPE address 3
50h–57h	Multiport ETYPE address 4
60h–67h	Multiport ETYPE address 5

Table 111: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h)

BIt	Name	R/W	Description	Default
64:48	MPORT_ETYPE	R/W	Multiport Ethernet type Allows a frame with a matching MPORT_ETYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register. Must be enabled using the MPORT_CTRLx bit in the Multiport Control Register.	0000

Table 111: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR	R/W	Multiport address Allows a frame with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector N register. Must be enabled using the MPORT_CTRL bit in the Multiport Control register.	0000000 00000

Multiport Vector N (N=0–5) Register (Page 04h: Address 18h–6Bh)

Table 112: Multiport Vector Register Address Summary

Address	Description
18h–1Bh	Multiport vector 0
28h–2Bh	Multiport vector 1
38h–3Bh	Multiport vector 2
48h–4Bh	Multiport vector 3
58h–5Bh	Multiport vector 4
68h–6Bh	Multiport vector 5

Table 113: Multiport Vector Register (Page 04h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh, 58h–5Bh, 68h–6Bh)

Bit	Name	R/W	Description	Default
31:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	MPORT_VCTR_N	R/W	Multiport vector Bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address register will be forwarded to each port with a bit set in the Multiport Vector bit map. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively.	0

Page 05h: ARL/VTBL Access Registers

Table 114: ARL/VTBL Access Registers (Page 05h)

Address	Bits	Register Name
00h	8	"ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 179
01h–0Fh	–	Reserved
02h–07h	48	"MAC Address Index Register (Page 05h: Address 02h–07h)" on page 179
08h–09h	16	"VLAN ID Index Register (Page 05h: Address 08h–09h)" on page 180
0Ah–0Fh	–	Reserved
10h–17h	64	"ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180
18h–1Bh	16	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)" on page 181
1Ch–1Fh	–	Reserved
20h–27h	64	"ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180
28h–2Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)" on page 181
2Ch–2Fh	–	Reserved
30h–37h	64	"ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180
38h–3Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)" on page 181
3Ch–3Fh	–	Reserved
40h–47h	64	"ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180
48h–4Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)" on page 181
4Ch–4Fh	–	Reserved
50h	8	"ARL Table Search Control Register (Page 05h: Address 50h)" on page 183
51h–52h	16	"ARL Search Address Register (Page 05h: Address 51h–52H)" on page 183
60h–77h	64	"ARL Table Search MAC/VID Result N (N = 0–1) Register (Page 05h: Address 60h–77h)" on page 184
68h–7Bh	32	"ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–7Bh)" on page 184
7Ch–7Fh	–	Reserved
80h	8	"VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" on page 186
81h–82h	16	"VLAN Table Address Index Register (Page 05h: Address 81h–82h)" on page 186
83h–86h	32	"VLAN Table Entry Register (Page 05h: Address 83h–86h)" on page 186

Table 114: ARL/VTBL Access Registers (Page 05h) (Cont.)

Address	Bits	Register Name
87h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

ARL Table Read/Write Control Register (Page 05h: Address 00h)

Table 115: ARL Table Read/Write Control Register (Page 05h: Address 00h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done command Write as 1 to initiate a read/write command to the ARL table. The bit returns to 0 to indicate that a read/write operation is complete.	0
6:1	Reserved	R/W	Write as default. Ignore on read.	–
0	ARL_R/W	R/W	ARL table read/write Specifies whether the ARL command is a read or write operation. 1 = Read 0 = Write	0

For more information, see "Accessing the ARL Table Entries" on page 55.

MAC Address Index Register (Page 05h: Address 02h–07h)

Table 116: MAC Address Index Register (Page 05h: Address 02h–07h)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC Address Index ARL table read/write command uses this 48-bit address to index the ARL table. When IEEE 802.1Q is enabled, the ARL table is indexed by a combined hash of the MAC_ADDR_INDX and the VID_INDX, defined in the "VLAN ID Index Register (Page 05h: Address 08h–09h)" on page 180. For more information, see "Accessing the ARL Table Entries" on page 55.	0

VLAN ID Index Register (Page 05h: Address 08h–09h)

Table 117: VLAN ID Index Register (Page 05h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11:0	VID_INDX	R/W	VLAN ID index When IEEE 802.1Q is enabled, the VLAN ID Index is used with the MAC_ADDR_INDX, defined in the "MAC Address Index Register (Page 05h: Address 02h–07h)" on page 179, to form the hash index for which status is to be read or written. For more information, see "Accessing the ARL Table Entries" on page 55.	0

ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)

Table 118: ARL Table MAC/VID Entry N (N = 0–3) Register Address Summary

Address	Description
10h–17h	ARL table MAC/VID entry 0
20h–27h	ARL table MAC/VID entry 1
30h–37h	ARL table MAC/VID entry 2
40h–47h	ARL table MAC/VID entry 3

Table 119: ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h)

Bit	Name	R/W	Description	Default
63:60	Reserved	R/W	Write as default. Ignore on read.	0
59:48	VID_N	R/W	VID entry N VID field is either read from or written to the ARL table entry N. VID is a "don't-care" field when IEEE 802.1Q is disabled.	0
47:0	MACADDR_N	R/W	MAC address entry N 48-bit MAC address field to be either read from or written to the ARL table entry N.	0

Note: Together, the "ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180 and the "ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)" on page 181 compose a complete entry in the ARL table. For more information, see "Accessing the ARL Table Entries" on page 55.

ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–4Bh)

Table 120: ARL Table Data Entry N (N = 0–3) Register Address Summary

Address	Description
18h–1Bh	ARL table data entry 0
28h–2Bh	ARL table data entry 1
38h–3Bh	ARL table data entry 2
48h–4Bh	ARL table data entry 3

Table 121: ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	R/W	Write as default. Ignore on read.	0
16	VALID_N	R/W	Valid bit entry N Write 1 to this bit to indicate that a valid MAC address is stored in the MACADDR_N field defined in the "ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h–47h)" on page 180, and that the entry has not aged out. Reset when an entry is empty. This information is read from or written to the ARL table during a read/write command.	0
15	STATIC_N	RW	Static bit entry N Write 1 to this bit to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry. This information is read from or written to the ARL table during a read/write command.	0

Table 121: ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh) (Cont.)

Bit	Name	R/W	Description	Default
14	AGE_N	R/W	Age Bit Entry N Write 1 to this bit to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects that a valid entry has remained unused for the period set by the AGE_TIME (defined in the "Aging Time Control Register (Page 02h: Address 06h–09h)" on page 166) and the entry has not been marked as static, the entry has the valid bit cleared. The age bit is ignored if the entry has been marked as static. This information is read from or written to the ARL table during a read/write command.	0
13:11	PRIORITY_N	R/W	Priority bit for DA MAC-based QoS entry N These bits define the priority for DA MAC-based QoS packets. This information is read from or written to the ARL table during a read/write command.	0
10:9	ARL_MODE_N	R/W	ARL mode • 00 = Forward according to FWD_MAP only. • 01 = Drop if the entry is matched as a destination. • 10 = Drop if the entry is matched as a source. • 11 = Copy to CPU, in addition to forwarding according to FWD_MAP. ***Note:*** 01, 10, and 11 can only be used when the entry is static.	0
8:0	FWD_PRT_MAP_N	R/W	Multicast group forward portmap entry N For multicast entries, these bits define the forward port map. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively.	0
	PORTID_N	–	Unicast forward port ID entry N For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4] = Reserved Bits [3:0] = Port ID/port number which identifies where the station with unique MACADDR_N is connected.	0

ARL Table Search Control Register (Page 05h: Address 50h)

Table 122: ARL Table Search Control Register (Page 05h: Address 50h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Write as 1 to initiate a sequential search of the ARL table. Each entry found by the search is returned to the "ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–7Bh)" on page 184 and the "ARL Table Search MAC/VID Result N (N = 0–1) Register (Page 05h: Address 60h–77h)" on page 184. Reading the "ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–7Bh)" on page 184 allows the ARL table search to continue. The BCM53101M clears this bit when the ARL table search is complete.	0
6:1	Reserved	R/W	Write as default. Ignore on read.	0
0	ARL_SR_VALID	RC	ARL Search Result Valid Set by BCM53101M to indicate that an ARL entry is found by the ARL table search. The found entry is available in the "ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–7Bh)" on page 184. This bit automatically returns to 0 after the ARL Search Result register is read.	0

For more information, see "Accessing the ARL Table Entries" on page 55.

ARL Search Address Register (Page 05h: Address 51h–52H)

Table 123: ARL Search Address Register (Page 05h: Address 51h–52h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	ARL address valid Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry that is currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARL_ADDR	–	ARL address 14-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only.	0

ARL Table Search MAC/VID Result N (N = 0–1) Register (Page 05h: Address 60h–77h)

Table 124: ARL Table Search MAC/VID Result N (N = 0–1) Register Address Summary

Address	Description
60h–67h	ARL table search MAC/VID result 0
70h–77h	ARL table search MAC/VID result 1

Table 125: ARL Table Search MAC/VID Result N (N = 0–1) Register (Page 05h: Address 60h–67h, 70h–77h)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	Write as default. Ignore on read.	0
59:48	ARL_SR_VID_N	RO	ARL search VID result These bits store the VID of the ARL table entry found by the ARL table search function.	0
47:0	ARL_SR_MAC_N	RO	ARL search MAC address result These bits store the MAC address of the ARL table entry found by the ARL table search function.	N/A

For more information, see "Accessing the ARL Table Entries" on page 55.

ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–7Bh)

Table 126: ARL Table Search Data Result N (N = 0–1) Register Address Summary

Address	Description
68h–6Bh	ARL table search data result 0
78h–7Bh	ARL table search data result 1

Table 127: ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Ignore on read	0
16	ARL_SR_VALID_N	RO	ARL search valid bit result This bit stores the valid bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	0

Table 127: ARL Table Search Data Result N (N = 0–1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)

Bit	Name	R/W	Description	Default
15	ARL_SR_STATIC_N	RO	ARL search static bit result This bit stores the static bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	N/A
14	ARL_SR_AGE_N	RO	ARL search age bit result This bit stores the Age bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
13:11	ARL_SR_PRIORITY_N	RO	ARL search priority bits result These bits store the TC bits of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
10:9	ARL_CON_N	RO	ARL control bit for ARL control mode enhancement	0
8:0	FWD_PRT_MAP_N	RO	Multicast group forward portmap entry N For multicast entries, these bits define the forward port map. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively.	0
	PORTID_N	–	Unicast Forward PortID Entry N For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4] = Reserved Bits [3:0] = Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0

For more information, see "Accessing the ARL Table Entries" on page 55.

VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

Table 128: VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Command Write as 1 to initiate a read or write or clear-table command to the VLAN table. The bit returns to 0 to indicate that the read or write or clear-table operation is complete. ***Note:*** "VLAN Table Address Index Register (Page 05h: Address 81h–82h)"should be loaded with the VLAN ID for which the VTBL entry is to be read or written	0
6:2	Reserved	R/W	Write as default. Ignore on read.	0
1:0	VTBL_R/W/Clr	R/W	Read/Write/Clear-Table Specifies whether the current VLAN table read/write/clear-table command is a read or write or clear-table operation: • 11 = Reserved • 10 = Clear-table • 01 = Read • 00 = Write	0

See "Programming the VLAN Table" on page 39 for more information.

VLAN Table Address Index Register (Page 05h: Address 81h–82h)

Table 129: VLAN Table Address Index Register (Page 05h: Address 81h–82h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11:0	VTBL_ADDR_INDX	R/W	VLAN table address index Current VLAN table read/write uses this 12-bit address to index the VLAN table.	0

See "Programming the VLAN Table" on page 39 for more information.

VLAN Table Entry Register (Page 05h: Address 83h–86h)

Table 130: VLAN Table Entry Register (Page 05h: Address 83h–86h)

Bit	Name	R/W	Description	Default
31:24	Reserved	R/W	Write as default. Ignore on read.	0

Table 130: VLAN Table Entry Register (Page 05h: Address 83h–86h) (Cont.)

Bit	Name	R/W	Description	Default
23	Policing_ID	R/W	VLAN policing ID This bit specifies the Policing_ID (Bucket0 or Bucket1) when Policing_EN is set to '1'. 0 = Bucket0 1 = Bucket1	0
22	Policing_EN	R/W	VLAN policing enable Specifies this VLAN entry is the target for ingress policing. 1 = Enable 0 = Disable	0
21	FWD_MODE	R/W	Indicates whether the packet forwarding should be based on VLAN membership or based on ARL flow as follows: 1 = Based on VLAN membership (excluding Ingress port) 0 = Based on ARL flow. ***Note:*** The VLAN membership based forwarding mode is only used for certain ISP-tagged packets received from ISP port when the BCM53101M is operating in double-tagged mode.	0
20:18	MSPT_INDEX	R/W	Index for eight spanning trees	0
17:9	UNTAG_MAP	R/W	Untagged port map • Bit 17: IMP port • Bits [16:15]: Reserved • Bits [14:9] correspond to ports 5–0, respectively. Ports written to 1 are designated as untagged VLAN ports. VLAN-tagged frames destined for these ports are untagged before they are forwarded. When the IEEE 802.1Q feature is enabled, frames sent using the CPU (MII port configured as a management port) are tagged. ***Note:*** The packet forwarded to IMP port should always be VLAN tagged.	–
8:0	FWD_MAP	R/W	Forward port map VLAN-tagged frame is allowed to forward to the destination ports with the corresponding bits set to 1 in the FWD_MAP. • Bit 8: IMP port • Bits [7:6]: Reserved • Bits [5:0] correspond to ports 5–0, respectively.	–

See "Programming the VLAN Table" on page 39 for more information.

Page 10h–14h: Internal PHY MII Registers

Table 131: 10/100/1000 PHY Page Summary

Page	Description
10h	Port 0 Internal PHY MII Registers
11h	Port 1 Internal PHY MII Registers
12h	Port 2 Internal PHY MII Registers
13h	Port 3 Internal PHY MII Registers
14h	Port 4 Internal PHY MII Registers

Table 132: Register Map (Page 10h–14h)

SPI Offset Address	MII Address	Number of Bits	Register Table
10BASE-T/100BASE-TX Registers			
00h	00h	16	Table 133: "MII Control Register (Page 10h–14h: Address 00h–01h)," on page 189
02h	01h	16	Table 134: "MII Status Register (Page 10h–14h: Address 02h–03h)," on page 191
04h–06h	02h	32	Table 135: "PHY Identifier Register MSB (Page 10h–14h: Address 04–05h)," on page 193
08h	04h	16	Table 137: "Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)," on page 193
0Ah	05h	16	Table 138: "Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)," on page 195
0Ch	06h	16	Table 139: "Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh)," on page 196
0Eh	07h	16	Table 140: "Auto-Negotiation Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)," on page 197
10h	08h	16	Table 141: "Auto-Negotiation Link Partner Next Page Transmit Register (Page 10h–14h: Address 10h–11h)," on page 198
12h–1Fh	09h–0Fh	–	Reserved. (Do not read from or write to a reserved register.)
20h	10h	16	Table 142: "100BASE-X Auxiliary Control Register (Page 10h–14h: Address 20h–21h)," on page 198
22h	11h	16	Table 143: "100BASE-X Auxiliary Status Register (Page 10h–14h: Address 22h–23h)," on page 200
24h	12h	16	Table 144: "100BASE-X Receive Error Counter (Page 10h–14h: Address 24h–25h)," on page 201
26h	13h	16	Table 145: "100BASE-X False Carrier Sense Counter (Page 10h–14h: Address 26h–27h)," on page 201
28h	14h	16	Table 146: "100BASE-X Disconnect Counter (Page 10h–14h: Address 28h–29h)," on page 202

Table 132: Register Map (Page 10h–14h) (Cont.)

SPI Offset Address	MII Address	Number of Bits	Register Table
2Ah–2Ch	15h–16h		Reserved. (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)
30h	18h	–	Table 147: "Auxiliary Control/Status Register (Page 10h–14h: Address 30h–31h)," on page 202
32h	19h	16	Table 148: "Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)," on page 204
34h	–	–	Reserved
36h	1Bh	16	Table 149: "Auxiliary Mode 2 Register (Page 10h–14h: Address 36h–37h)," on page 205
3Ah	1Dh	16	Table 150: "Auxiliary Mode Register (Page 10h–14h: Address 3Ah–3Bh)," on page 206
3Ch	1Eh	16	Table 151: "Auxiliary Multiple PHY Register (Page 10h–14h: Address 3Ch–3Dh)," on page 206
3Eh	1Fh	16	Table 152: "Broadcom Test Register (Page 10h–14h: Address 3Eh–3Fh)," on page 208
Shadow Register Access: Writing 1 to bit 7 of the "Broadcom Test Register (Page 10h–14h: Address 3Eh–3Fh)" allows R/W access to the shadow registers.			
20h	10h	16	Table 153: "Miscellaneous Control Shadow Register (Page 10h–14h: Address 20h–21h)," on page 208
36h–37h	1Bh	16	Table 154: "Auxiliary Status 2 Shadow Register (Page 10h–14h: Address 36h–37h)," on page 209
38h	1Ch	16	Table 156: "Auxiliary Status 3 Shadow Register (Page 10h–14h: Address 38h–39h)," on page 209
3Ah	1Dh	16	Table 157: "Auxiliary Mode 3 Shadow Register (Page 10h–14h: Address 3Ah–3Bh)," on page 210
3Ch	1Eh	16	Table 159: "Auxiliary Status 4 Shadow Register (Page 10h–14h: Address 3Ch–3Dh)," on page 211

MII Control Register (Page 10h–14h: Address 00h–01h)

Table 133: MII Control Register (Page 10h–14h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15	Soft Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation is enabled. 0 = Auto-Negotiation is disabled.	1

Table 133: MII Control Register (Page 10h–14h: Address 00h–01h) (Cont.)

Bit	Name	R/W	Description	Default
11	Reserved	R/W	Write as default. Ignore on read.	0
10	Isolate	R/W	1 = Electrically isolate PHY from MII. 0 = Normal operation	0
9	Restart Auto-Negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-Negotiation restart is complete.	0
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0
7:0	Reserved	R/W	Write as default. Ignore on read.	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Soft Reset. To reset the PHY core by software control, a 1 must be written to bit 15 of the control register using an MII write operation. The bit clears itself after the reset process is complete and need not be cleared using a second MII write. Writes to other control register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing 0 to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it returns a 1 when read.

Loopback. The PHY core is placed into loopback mode by writing 1 to bit 14 of the control register. The loopback mode is cleared by writing 0 to bit 14 of the control register or by resetting the chip. When this bit is read, it returns a 0 when the chip is in software-controlled loopback mode; otherwise, it returns a 0.

Forced Speed Selection. If auto-negotiation is enabled, this bit has no effect on the speed selection. However, if auto-negotiation is disabled by software control, the operating speed of the PHY core can be forced by writing the appropriate value to bit 13 of the control register. Writing 1 to this bit forces 100BASE-X operation, while writing 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection from hardware or software control, use bit 2 of the Auxiliary Error and General Status register, 1Ch.

Auto-Negotiation Enable. Auto-Negotiation can be disabled either by hardware or software control. If bit 12 of the control register is written with a value of 0, auto-negotiation is disabled by software control. When auto-negotiation is disabled in this manner, writing 1 to the same bit of the control register or resetting the chip re-enables auto-negotiation. When read, this bit returns the value most recently written to this location or 1 if it has not been written since the last chip reset.

Isolate. Each individual PHY is isolated from its media-independent interface by writing 1 to bit 10 of the control register. All RXD0{*n*} outputs are tristated and all TXD0{*n*} inputs are ignored. Since the MII management interface is still active, the isolate mode is cleared by writing 0 to bit 10 of the control register or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode; otherwise, it returns a 0.

Restart Auto-Negotiation. Bit 9 of the control register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. In order for this bit to have an effect, auto-negotiation must be enabled. Writing 1 to this bit restarts the auto-negotiation, while writing 0 to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY register.

Duplex Mode. By default, the PHY core powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing 1 to bit 8 of the control register while auto-negotiation is disabled. Half-duplex mode can be resumed by writing 0 to bit 8 of the control register or by resetting the chip.

MII Status Register (Page 10h–14h: Address 02h–03H)

Table 134: MII Status Register (Page 10h–14h: Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capability	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO H	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	1
13	100BASE-TX HDX Capability	RO H	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO H	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
11	10BASE-T HDX Capability	RO H	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore on read	0000
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation is complete. 0 = Auto-Negotiation is in progress.	0
4	Reserved	RO	Ignore on read	0
3	Auto-Negotiation Capability	RO H	1 = Auto-Negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

100BASE-T4 Capability. The PHY core is not capable of 100BASE-T4 operation and returns a 0 when bit 15 of the status register is read.

100BASE-TX FDX Capability. The PHY core is capable of 100BASE-TX full-duplex operation and returns a 1 when bit 14 of the status register is read.

100BASE-TX HDX Capability. The PHY core is capable of 100BASE-TX half-duplex operation and returns a 1 when bit 13 of the status register is read.

10BASE-T FDX Capability. The PHY core is capable of 10BASE-T full-duplex operation and returns a 1 when bit 12 of the status register is read.

10BASE-T HDX Capability. The PHY core is capable of 10BASE-T half-duplex operation and returns a 1 when bit 11 of the status register is read.

Management Frames Preamble Suppression. This bit is the only writable bit in the status register. Setting this bit to a 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When preamble suppression is enabled, only 2 preamble bits are required between successive management commands, instead of the normal 32.

Auto-Negotiation Complete. Bit 5 of the status register returns a 1 if the auto-negotiation process has been completed and the contents of registers 4, 5, and 6 are valid.

Auto-Negotiation Capability. The PHY core is capable of performing IEEE auto-negotiation and returns a 1 when bit 4 of the status register is read, regardless of whether or not the auto-negotiation function has been disabled.

Link Status. The PHY core returns a 1 on bit 2 of the status register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the link-pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the link-pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The PHY core returns a 1 on bit 1 of the status register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The PHY core supports extended capability registers and returns a 1 when bit 0 of the status register is read. Several extended registers have been implemented in the PHY core and their bit functions are defined later in this section.

PHY Identifier Register (Page 10h–14h: Address 04h–07H)

Table 135: PHY Identifier Register MSB (Page 10h–14h: Address 04–05h)

Bit	Name	R/W	Description	Default
15:0	OUI	RO	Bits [3:18] of organizationally unique identifier	0362h

Table 136: PHY Identifier Register LSB (Page 10h–14h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:10	OUI	RO	Bits [19:24] of organizationally unique identifier	010111
9:4	MODEL	RO	Device model number	101101
3:0	REVISION	RO	Device revision number	*n*[a] (hex)

a. The revision number (*n*) changes with each silicon revision.

The [15:0] bits of MII register 04h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 06h (PHYID LOW) contain the most significant OUI bits [19:24], six manufacturer's model number bits, and four revision number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-1B-E9, expressed as hexadecimal values. The binary OUI [1:24] is 0000-0000-1101-1000-1001-0111. The model number for BCM53101M is 2Dh. Revision numbers start with 0h and increment by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + MODEL[5:0] + REVISION[3:0]

Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09H)

Table 137: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next page ability is enabled. 0 = Next page ability is disabled.	0
14	Reserved	R/W	Write as default. Ignore on read.	0
13	Remote Fault	R/W	1 = Advertise remote fault is detected. 0 = Advertise no remote fault is detected.	0
12:11	Reserved	R/W	Write as default. Ignore on read.	0
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation 0 = Incapable of pause operation	0

Table 137: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)

Bit	Name	R/W	Description	Default
9	Advertise 100BASE-T4	R/W	1 = Advertise 100BASE-T4 capability 0 = Do not advertise 100BASE-T4 capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex capability 0 = Do not advertise 100BASE-TX full-duplex capability	1
7	Advertise 100BASE-X HDX	R/W	1 = Advertise 100BASE-X half-duplex capability 0 = Do not advertise 100BASE-TX half-duplex capability	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex capability 0 = Do not advertise 10BASE-T full-duplex capability	1
5	Advertise 10BASE-T HDX	R/W	1 = Advertise 10BASE-T half-duplex capability 0 = Do not advertise 10BASE-T half-duplex capability	1
4:0	Protocol Selector Field	R/W	Bits [4:0] = 00001 indicates IEEE 802.3 CSMA/CD	00001

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Next Page. The PHY core supports the Next Page function.

Remote Fault. Writing 1 to bit 13 of the advertisement register causes a remote fault indicator to be sent to the link partner during auto-negotiation. Writing 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it or 0 if no write has been completed since the last chip reset.

Reserved Technologies. Ignore output when read.

Pause. Pause operation for full-duplex links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate pause capability to its link partner and has no effect on PHY operation.

Advertisement Bits. Bits [9:5] of the advertisement register allow the user to customize the ability information transmitted to the link partner. The default value for each bit reflects the abilities of the PHY core. By writing 1 to any of the bits, the corresponding ability is transmitted to the link partner. Writing 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits or the default values if no write has been completed since the last chip reset.

Advertise Selector Field. Bits [4:0] of the advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)

Table 138: Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	LP Next Page	RO	1 = Link partner has Next Page ability. 0 = Link partner does not have Next Page ability.	0
14	LP Acknowledge	RO	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	0
13	LP Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0
12:11	Reserved	RO	Ignore on read.	0
10	LP Advertise Pause Capable	RO	1 = Link partner is capable of pause operation. 0 = Link partner is incapable of pause operation.	0
9	LP Advertise 100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0
8	LP Advertise 100BASE-X FDX Capable	RO	1 = Link partner is 100BASE-X full-duplex capable. 0 = Link partner is not 100BASE-X full-duplex capable.	0
7	LP Advertise 100BASE-X HDX Capable	RO	1 = Link partner is 100BASE-X half-duplex capable. 0 = Link partner not 100BASE-X half-duplex capable.	0
6	LP Advertise 10BASE-T FDX Capable	RO	1 = Link partner is 10BASE-T full-duplex capable. 0 = Link partner is not 10BASE-T full-duplex capable.	0
5	LP Advertise 10BASE-T HDX Capable	RO	1 = Link partner is 10BASE-T half-duplex capable. 0 = Link partner is not 10BASE-T half-duplex capable.	0
4:0	LP Protocol Selector Field	RO	Link partner protocol selector field	00000

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Note: As indicated by bit 5 of the 10BASE-T/100BASE-TX MII Status register, the values contained in the 10BASE-T/100BASE-TX Auto-Negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

LP Next Page. The BCM53101M returns a 1 in bit 15 when the link partner wants to transmit Next Page information. The PHY core does not implement the Next Page function and ignores the Next Page bit, except to copy it to this register.

LP Acknowledge. The BCM53101M returns a 1 in bit 14 when the link partner has acknowledged reception of the link code word; otherwise, the BCM53101M returns a 0.

LP Remote Fault. Bit 13 of the Link Partner Ability register returns a value of 1 when the link partner signals that a remote fault has occurred. The PHY core simply copies the value to this register and does not act upon it.

Reserved Bits. Ignore when read.

LP Advertise Pause. Indicates that the link partner pause bit is set.

LP Advertise Bits. Bits [9:5] of the Link Partner Ability register reflect the abilities of the link partner. A 1 on any of these bits indicates that the link partner is capable of performing the corresponding mode of operation. Bits [9:5] are cleared any time auto-negotiation is restarted or the PHY is reset.

LP Protocol Selector Field. Bits [4:0] of the Link Partner Ability register reflect the value of the link partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh)

Table 139: Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore on read	0
4	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability. 0 = Link partner does not have Next Page capability.	0
2	Next Page Capable	RO H	1 = BCM53101M is Next Page capable. 0 = BCM53101M is not Next Page capable.	1
1	Page Received	RO LH	1 = New page has been received from link partner. 0 = New page has not been received.	0
0	Link Partner Auto-Negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not have auto-negotiation.	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Parallel Detection Fault. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, consult the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Ability. Bit 3 of the Auto-Negotiation Expansion Register returns a 1 when the link partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Next Page Capable. The PHY core Returns 1 when bit 2 of the Auto-Negotiation Expansion Register is read indicating that it has Next Page capabilities.

Page Received. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new link code word is received from the link partner, checked, and acknowledged. It remains high until the register is read or until the chip is reset.

Link Partner Auto-Negotiation Ability. Bit 0 of the Auto-Negotiation Expansion Register returns a 1 when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the link partner does not comply with IEEE auto-negotiation, the bit returns a 0.

Auto-Negotiation Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)

Table 140: Auto-Negotiation Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional Next Pages follow. 0 = Sending last Next Page.	0
14	Reserved	RO	Ignore on read.	0
13	Message Page	R/W	1 = Formatted page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Complies with message. 0 = Cannot comply with message.	0
11	Toggle	RO	Toggles between exchanges of different Next Pages. 1 = Previous value of the transmitted link code word equaled logic 0 0 = Previous value of the transmitted link code word equaled logic 1	0
10:0	Message/Unformatted Code Field	R/W	Next Page message code or unformatted data	1

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a message page from an unformatted page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the arbitration function to ensure synchronization with the link partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field that may contain an arbitrary value.

Auto-Negotiation Link Partner Next Page Transmit Register (Page 10h–14h: Address 10h–11H)

Table 141: Auto-Negotiation Link Partner Next Page Transmit Register (Page 10h–14h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional Next Pages follow. 0 = Sending last Next Page.	0
14	Reserved	RO	Ignore on read	0
13	Message Page	RO	1 = Formatted page 0 = Unformatted page	0
12	Acknowledge2	RO	1 = Complies with message. 0 = Cannot comply with message.	0
11	Toggle	RO	Toggles between exchanges of different Next Pages. 1 = Previous value of the transmitted link code word equaled logic 0 0 = Previous value of the transmitted link code word equaled logic 1	0
10:0	Message/Unformatted Code field	RO	Next page message code or unformatted data	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a message page from an unformatted page.

Acknowledge 2. Indicates that the link partner has the ability to comply with the message.

Toggle. Used by the arbitration function to ensure synchronization with the link partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field that may contain an arbitrary value.

100BASE-X Auxiliary Control Register (Page 10h–14h: Address 20h–21h)

Table 142: 100BASE-X Auxiliary Control Register (Page 10h–14h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/W	Write as default. Ignore on read.	0
13	Transmit Disable	R/W	1 = Transmitter outputs are disabled. 0 = Normal operation	0

Table 142: 100BASE-X Auxiliary Control Register (Page 10h–14h: Address 20h–21h) (Cont.)

Bit	Name	R/W	Description	Default
12:11	Reserved	R/W	Write as default. Ignore on read.	–
10	Bypass 4B/5B Encoder/Decoder (100BASE-T)	R/W	1 = Transmit and receive 5B codes over SMII pins. 0 = Normal SMII	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler are disabled. 0 = Scrambler and descrambler are enabled.	0
8	Bypass NRZI/MLT3 Encoder/ Decoder	R/W	1 = Bypass NRZI/MLT3 encoder and decoder. 0 = Normal operation	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols are not aligned. 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline Wander Correction disabled 0 = Baseline Wander Correction enabled	0
5	FEF Enable	R/W	1 = Far-End Fault enabled 0 = Far-End Fault disabled	–
4:3	Reserved	R/W	Write as default, ignore on read.	0
2	Extended FIFO Enable	R/W	1 = Extended FIFO mode 0 = Normal FIFO mode	0
1:0	Reserved	R/W	Write as default, ignore on read.	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Transmit Disable. The transmitter is disabled by writing 1 to bit 13 of this register. The transmitter output (TD±) is forced into a high-impedance state.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder are bypassed by writing 1 to bit 10 of this register. The transmitter sends 5B codes from the TXER and TXD signals directly to the scrambler. TXEN must be active and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RXER and RXD signals. CRS is asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The stream cipher function is disabled by writing 1 to bit 9 of this register. The stream cipher function is re-enabled by writing 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing 1 to bit 8 of this register, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) is re-enabled by writing 0 to this bit.

Bypass Receive Symbol Alignment. Receive symbol alignment is bypassed by writing 1 to bit 7 of this register. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD signals.

Baseline Wander Correction Disable. The baseline wander correction circuit is disabled by writing 1 to bit 6 of this register. The PHY corrects for baseline wander on the receive data signal when this bit is cleared.

Extended FIFO Enable. Controls the extended receive FIFO mechanism. This bit may have to be set if the Jumbo Packet Enable bit is set.

100BASE-X Auxiliary Status Register (Page 10h–14h: Address 22h–23h)

Table 143: 100BASE-X Auxiliary Status Register (Page 10h–14h: Address 22h–23h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore on read.	0
11	SMII Overrun/Underrun Detected	RO	1 = Error detected 0 = No error	0
10	Reserved	RO	Ignore on read.	X
9	Locked	RO	1 = Descrambler is locked. 0 = Descrambler is unlocked.	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote fault detected 0 = No remote fault detected	0
6	Reserved	RO	Ignore on read.	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No false carrier since last read	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No bad ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

SMII Overrun/Underrun Error. The PHY returns a 1 in bit 11 when the SMII receive FIFO encounters an overrun or underrun condition.

Locked. The PHY returns a 1 in bit 9 when the descrambler is locked to the incoming data stream. Otherwise, it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X link status is good. Otherwise, it returns a 0.

Remote Fault. The PHY returns a 1 while its link partner is signaling a far-end fault condition. Otherwise, it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise, it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an end-of-stream delimiter error has been detected since the last time this register was read. Otherwise, it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise, it returns a 0

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise, it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1 if the descrambler has lost lock since the last time this register was read. Otherwise, it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise, it returns a 0.

100BASE-X Receive Error Counter (Page 10h–14h: Address 24h–25h)

Table 144: 100BASE-X Receive Error Counter (Page 10h–14h: Address 24h–25h)

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	Number of noncollision packets with receive errors since last read	0000h

Receive Error Counter. This counter increments each time the PHY receives a noncollision packet containing at least one receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears itself when read.

100BASE-X False Carrier Sense Counter (Page 10h–14h: Address 26h–27h)

Table 145: 100BASE-X False Carrier Sense Counter (Page 10h–14h: Address 26h–27h)

Bit	Name	R/W	Description	Default
15:8	SMII Overrun/Underrun Counter [7:0]	R/W	Number of overruns/underruns since last read	00h
7:0	False Carrier Sense Counter[7:0]	R/W	Number of false carrier sense events since last read	00h

Overrun/Underrun Counter [7:0]. The overrun/underrun counter increments each time the PHY detects an overrun or underrun of the receive FIFOs. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting overrun/underrun errors until cleared.

False Carrier Sense Counter [7:0]. This counter increments each time the PHY detects a false carrier on the receive input. This counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting false carrier sense errors until cleared.

100BASE-X Disconnect Counter (Page 10h–14h: Address 28h–29h)

Table 146: 100BASE-X Disconnect Counter (Page 10h–14h: Address 28h–29h)

Bit	Name	R/W	Description	Default
15	SMII Fast RXD	RO	1 = In extended FIFO mode, detect fast receive data 0 = Normal	0
14	SMII Slow RXD	RO	0 = Normal 1 = In extended FIFO mode, detect slow receive data	0
13:10	Reserved	RO	Ignore on read	0
9	Reserved	RO	Ignore on read	1
8:0	Reserved	RO	Ignore on read	013:10

SMII Fast RXD. Extended FIFO operation only. Bit 15 of the Disconnect Counter register indicates the FIFO state machine has detected fast receive data relative to the reference input.

SMII Slow RXD. Extended FIFO operation only. Bit 14 of the Disconnect Counter register indicates the FIFO state machine has detected slow receive data relative to the reference input. Receive CRC Counter register (page 10h–14h: address 28h).

Auxiliary Control/Status Register (Page 10h–14h: Address 30h–31h)

Table 147: Auxiliary Control/Status Register (Page 10h–14h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15	Jabber Disable	R/W	1 = Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1 = Link integrity test disabled in PHY 0 = Link integrity test is enabled in PHY	0
13:8	Reserved	R/W	Write as default. Ignore on read.	000000
7:6	HSQ:LSQ	R/W	These two bits define the squelch mode of the 10BASE-T carrier sense mechanism: 00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Not allowed	00

Table 147: Auxiliary Control/Status Register (Page 10h–14h: Address 30h–31h) (Cont.)

Bit	Name	R/W	Description	Default
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indicator	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control register allows the user to disable the Jabber Detect function defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable. Writing 1 to bit 14 of the Auxiliary Control register allows the user to disable the Link Integrity state machines and places the PHY core into forced link pass status. Writing 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

HSQ:LSQ. Extends or decreases the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high-squelch and low-squelch levels are useful for situations where the IEEE- prescribed levels are inadequate. The squelch levels are used by the CRS/link block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the PHY core to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate [1:0]. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode.

Auto-Negotiation Indicator. A read-only bit that indicates whether auto-negotiation has been enabled or disabled in the PHY core. A 1 in bit 12 of the control register is required to enable auto-negotiation. When auto-negotiation is disabled, bit 3 of the Auxiliary Control register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 1. Bit 12 of the control register has been written as 0 and bit 13 of the control register has been written as 0. When bit 8 of the Auxiliary Control register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto-negotiation is enabled) or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control register is a read-only bit that shows the true current operation speed of the PHY core. A 1 bit indicates 100BASE-X operation, whereas a 0 indicates 10BASE-T operation. While the auto-negotiation exchange is being performed, the PHY core is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control register is a read-only bit that returns a 1 when the PHY is in full-duplex mode. In all other modes, it returns a 0.

Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)

Table 148: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)[a]

Bit	Name	R/W	Description	Default
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation is complete. 0 = Auto-Negotiation is in progress.	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link is good check state 0 = State not entered since last read	0
13	Auto-Negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state 0 = State not entered since last read	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state 0 = State not entered since last read	0
11	Auto-Negotiation Pause	RO	PHY and link partner pause operation bit set	0
10	Auto-Negotiation HCD Current Operating Speed and Duplex Mode	RO	11x = Undefined	0
9		RO	101 = 100BASE-TX full-duplex[b]	0
8		RO	100 = 100BASE-T4 011 = 100BASE-TX half-duplex[b] 010 = 10BASE-T full-duplex[b] 001 = 10BASE-T half-duplex[b] 000 = No highest common denominator or auto-negotiation is incomplete	0
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
6	Reserved	RO	Ignore on read.	0
5	Link Partner Page Received	RO	1 = New page has been received from the link partner. 0 = New page has not been received.	0
4	Link Partner Auto-Negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not perform auto-negotiation.	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0

Table 148: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)[a]

Bit	Name	R/W	Description	Default
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled	0
0	Full Duplex Indication	RO LL	1 = Full-duplex active 0 = Full-duplex inactive	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

a. The Auxiliary Status Summary register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with the primary register descriptions.
b. Indicates the negotiated HCD when Auto-Negotiation Enable = 1, or indicates the manually selected speed and duplex mode when Auto-Negotiation Enable = 0.

Auxiliary Mode 2 Register (Page 10h–14h: Address 36h–37h)

Table 149: Auxiliary Mode 2 Register (Page 10h–14h: Address 36h–37h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11	10BT Dribble Bit Correct	R/W	1 = Enable 0 = Disable	0
10	Jumbo Packet Mode	R/W	1 = Enable 0 = Disable	0
9	Jumbo Packet FIFO Enable	R/W	1 = Enable 0 = Disable	0
8	Reserved	R/W	Write as default. Ignore on read.	0
7	Block 10BT Echo Mode	R/W	1 = Enable 0 = Disable	1
6:2	Reserved	R/W	Write as default. Ignore on read.	0x02
1	Qual Parallel Detect Mode	R/W	1 = Enable 0 = Disable	1
0	Reserved	R/W	Write as default. Ignore on read.	0

10BT Dribble Bit Correct. When enabled, the PHY rounds down to the nearest nibble when dribble bits are present on the 10BASET input stream.

Jumbo Packet Mode. When enabled, the 100BASE-X unlock timer changes to allow long packets.

Jumbo Packet FIFO Enable. When enabled, the receive FIFO doubles from 7 nibbles to 14 nibbles. The Jumbo Packet FIFO Enable bit should be set to a 1 when jumbo packet mode is enabled.

Block 10BT Echo Mode. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal does not echo onto the RXDV signal. The TXEN echoes onto the CRS signal and the CRS deassertion directly follows the TXEN deassertion.

Qualified Parallel Detect Mode. This bit allows the auto-negotiation/parallel-detection process to be qualified with information in the advertisement register (08h) as follows:

- If this bit is not set, the local PHY device is enabled to auto-negotiate, the far-end device is a 10BASE-T or 100BASE-X non auto-negotiating legacy type, and the local device will auto-negotiate/parallel-detect the far-end device regardless of the contents of its Advertisement register.
- If this bit is set, the local device compares the detected link speed to the contents of its Advertisement register. If the particular link speed is enabled in the advertisement register, the local device asserts link. If the link speed is disabled in this register, the local device does not assert link and continues monitoring for a matching capability link speed.

Auxiliary Mode Register (Page 10h–14h: Address 3Ah–3Bh)

Table 150: Auxiliary Mode Register (Page 10h–14h: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
15:2	Reserved	R/W	Write as default. Ignore on read.	0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	R/W	Write as default. Ignore on read.	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3, or 4 TXC cycles all result in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

Auxiliary Multiple PHY Register (Page 10h–14h: Address 3Ch–3Dh)

Table 151: Auxiliary Multiple PHY Register (Page 10h–14h: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
15	HCD_TX_FDX	RO	1 = Auto-Negotiation result is full-duplex 100BASE-TX	0
14	HCD_T4	RO	1 = Auto-Negotiation result is 100BASE-T4	0
13	HCD_TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-Negotiation result is full-duplex 10BASE-T	0
11	HCD_10BASE-T	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	R/W	Write as default. Ignore on read.	0
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart auto-negotiation process 0 = No effect	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
6	Acknowledge Complete	RO	1 = Auto-Negotiation Acknowledge completed	0

Table 151: Auxiliary Multiple PHY Register (Page 10h–14h: Address 3Ch–3Dh) (Cont.)

Bit	Name	R/W	Description	Default
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge detected	0
4	Ability Detect	RO	1 = Auto-Negotiation Waiting for LP ability	0
3	Super-Isolate	R/W	1 = Super-Isolate mode 0 = Normal operation	0
2	Reserved	R/W	Write as default. Ignore on read.	0
1	10BASE-T Serial Mode	R/W	1 = Enable 10BASE-T Serial mode 0 = Disable 10BASE-T Serial mode	0
0	Reserved	R/W	Write as default. Ignore on read.	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

HCD Bits. Bits [15:11] of the Auxiliary Multiple PHY register are five read-only bits that report the Highest Common Denominator (HCD) result of the auto-negotiation process. Immediately upon entering the link-pass state after each reset or Restart Auto-Negotiation, only one of these five bits will be 1. The link-pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time auto-negotiation is restarted or the PHY is reset. For their intended application, these bits uniquely identify the HCD only after the first link-pass after reset or restart of auto-negotiation. On later link fault and subsequent renegotiations, if the ability of the link partner is different, more than one of the above bits may be active.

Restart Auto-Negotiation. A self-clearing bit that allows the auto-negotiation process to be restarted regardless of the current status of the state machine. For this bit to work, auto-negotiation must be enabled. Writing 1 to this bit restarts auto-negotiation. Since the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the control register.

Auto-Negotiation Complete. This read-only bit returns a 1 after the auto-negotiation process has been completed. It remains 1 until the auto-negotiation process is restarted, a link fault occurs, or the chip is reset. If auto-negotiation is disabled or the process is still in progress, the bit returns a 0.

Acknowledge Complete. This read-only bit returns a 1 after the acknowledgment exchange portion of the auto-negotiation process has been completed and the arbitrator state machine has exited the Acknowledge Complete state. It remains this value until the auto-negotiation process is restarted, a link fault occurs, auto-negotiation is disabled, or the PHY is reset.

Acknowledge Detected. This read-only bit is set to 1 when the arbitrator state machine exits the Acknowledge Detected state. It remains high until the auto-negotiation process is restarted or the PHY is reset.

Ability Detect. This read-only bit returns a 1 when the auto-negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the auto-negotiation process begins and exits after the first FLP burst or link pulses are detected from the link partner. This bit returns a 0 any time the auto-negotiation state machine is not in the Ability Detect state.

Super-Isolate. Writing 1 to this bit places the PHY core into super-isolate mode. Similar to isolate mode, all TXD0 inputs are ignored and all RXD outputs are tristated. Additionally, all link pulses are suppressed. This allows the PHY core to coexist with another PHY on the same adapter card with only one being activated at any time.

10BASE-T Serial Mode. Writing 1 to bit 1 of the Auxiliary Mode register enables the 10BASE-T serial mode. Serial operation is not available in 100BASE-X mode.

Broadcom Test Register (Page 10h–14h: Address 3Eh–3Fh)

Table 152: Broadcom Test Register (Page 10h–14h: Address 3Eh–3Fh)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Write as default. Ignore on read.	0
7	Shadow Register Enable	R/W	1 = Enable shadow registers 0 = Disable shadow registers	0
6:0	Reserved	R/W	Write as default. Ignore on read.	0001011

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Shadow Register Enable. Writing 1 to bit 7 of this register allows R/W access to the shadow registers located at addresses 1Eh–3Ch. To access the default MII registers (00h–3Ch), this bit must be set to 0.

Shadow Register Detailed Description

The following tables describe the shadow register bits and their functions. Shadow register access is enabled by writing 1 to bit 7 of the Broadcom Test register (3Eh). When nonshadow register access is required, write 0 to bit 7 of the same register.

Miscellaneous Control Shadow Register (Page 10h–14h: Address 20h–21h)

Table 153: Miscellaneous Control Shadow Register (Page 10h–14h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as default. Ignore on read.	0
14	Forced Auto-MDIX Enable	R/W	1 = Enable Auto-MDIX	0
13	Reserved	R/W	Write as default. Ignore on read.	0
12	Auto-Negotiation H/W Override Enable	R/W	0 = Auto-negotiation enabled 1 = Use MII register 0 values.	0
11:0	Local Master/Slave Seed Value	R/W	Returns the automatically generated master/slave random seed	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Forced Auto-MDIX Enable. When this bit is set to 0, HP auto-MDIX is in effect while auto-negotiation is enabled. If auto-negotiation is not enabled (forced 100BT or forced 10BT full- or half-duplex) and if auto-MDIX is still needed, set this bit to 1.

Auto-Negotiation Hardware Override. When this bit is set to 1, the PHY uses MII register 0h, bits 12, 13, and 8, respectively.

Auxiliary Status 2 Shadow Register (Page 10h–14h: Address 36h–37h)

Table 154: Auxiliary Status 2 Shadow Register (Page 10h–14h: Address 36h–37h)

Bit	Name	R/W	Description	Default
15	MLT3 Detected	RO	1 = MLT3 detected	0
14:6	Reserved	R/W	Write as default. Ignore on read.	0
5	APD Enable	R/W	0 = Normal mode 1 = Enable auto power-down mode	0
4	APD Sleep Timer	R/W	0 = 2.5-second sleep before wake up 1 = 5.0-second sleep before wake up	0
3:0	APD Wake-Up Timer [3:0]	R/W	Duration of wake up	0001

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

MLT3 Detected. The PHY returns a 1 in this bit whenever MLT3 signaling is detected.

APD Enable. When in normal mode, if this bit is set to 1, the PHY enters auto power-down mode. If this bit is set and the link is lost, the PHY enters low power-down mode. When energy is detected, the device enters full-power mode. Otherwise, it wakes up after either 2.5 seconds or 5.0 seconds, as determined by the APD Sleep Timer bit. When the PHY wakes up, it sends link pulses and also monitors energy. If the link partner's energy is detected, the PHY device continues to stay in wake-up mode for a duration determined by the APD wake-up timer before going to low-power mode.

APD Sleep Timer. This bit determines how long the PHY stays in low-power mode before waking up. If this bit is a 0, the PHY device waits approximately 2.5 seconds before waking up. Otherwise, it wakes up after approximately 5.0 seconds.

APD Wake-Up Timer [3:0]. This counter determines how long the PHY stays in wake-up mode before going to low-power mode. This value is specified in 40-millisecond increments from 0 to 600 milliseconds. A value of 0 forces the PHY to stay in low-power mode indefinitely. In this case, the PHY requires a hard reset to return to normal mode.

Auxiliary Status 3 Shadow Register (Page 10h–14h: Address 38h–39h)

Table 156: Auxiliary Status 3 Shadow Register (Page 10h–14h: Address 38h–39h)

Bit	Name	R/W	Description	Default
15:8	Noise [7:0]	RO	Current mean-squared error value, valid only if link is established	0
7:4	Reserved	RO	Ignore on read.	0

Table 156: Auxiliary Status 3 Shadow Register (Page 10h–14h: Address 38h–39h) (Cont.)

Bit	Name	R/W	Description	Default
3:0	FIFO Consumption [3:0]	RO	Currently used number of nibbles in the receive FIFO	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Noise [7:0]. The PHY provides the current mean-squared error value for noise when a valid link is established.

FIFO Consumption [3:0]. The PHY indicates the number of nibbles of FIFO currently used.

Auxiliary Mode 3 Shadow Register (Page 10h–14h: Address 3Ah–3Bh)

Table 157: Auxiliary Mode 3 Shadow Register (Page 10h–14h: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as default. Ignore on read.	0
3:0	FIFO Size Select [3:0]	R/W	Currently selected receive FIFO size	0100

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

FIFO Size Select [3:0]. The PHY indicates the current selection of receive FIFO size using bit 3 through 0 as shown in Table 158. The size can also be determined by the Extended FIFO Enable bit (register 10h, bit 2) and the Jumbo Packet Enable bit (register 1Bh, bit 9) for backward compatibility with 0.35 mm products.

Table 158: Current Receive FIFO Size

FIFO Size Select[3:0]	Receive FIFO size in use (Number of Bits)
0000	12
0001	16
0010	20
0011	24
0100	28
0101	32
0110	36
0111	40
1000	44
1001	48
1010	52
1011	56
1100	60
1101	64

Auxiliary Status 4 Shadow Register (Page 10h–14h: Address 3Ch–3Dh)

Table 159: Auxiliary Status 4 Shadow Register (Page 10h–14h: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
15:0	Packet Length Counter [15:0]	RO	Number of bytes in last received packet	0

R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation. Use the default value of a reserved bit when writing to a reserved bit.

Packet Length Counter [15:0]. The PHY shows the number of bytes in the last packet received. This is valid only when a valid link is established.

Page 20h–28h: Port MIB Registers

Note: When accessing the per-port MIB counters, the SNAPSHOT_MIRROR of Page 70h: MIB Snapshot Control Register must be set to the default value of 0; otherwise, the mirrored port MIB snapshot counters are accessed instead.

Table 160: Port MIB Registers Page Summary

Page	Description
20h	Port 0
21h	Port 1
22h	Port 2
23h	Port 3
24h	Port 4
25h	Port 5
26h	Reserved
27h	Reserved
28h	IMP port

Table 161: Page 20h–28h Port MIB Registers

ADDR	Bits	Name	Description
00h–07h	64	TxOctets	Total number of good bytes of data transmitted by a port (excluding preamble, but including FCS)
08h–0Bh	32	TxDropPkts	Counter incremented every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow) or an internal MAC sublayer transmit error not counted by the TxLateCollision counter

Table 161: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
0Ch–0Fh	32	TXQ0PKT	Total number of good packets transmitted on CoS0, specified in MIB queue select register when QoS is enabled
10h–13h	32	TxBroadcastPkts	Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
14h–17h	32	TxMulticastPkts	Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
18h–1Bh	32	TxUnicastPkts	Number of good packets transmitted by a port that are addressed to a unicast address
1Ch–1Fh	32	TxCollisions	Number of collisions experienced by a port during packet transmissions
20h–23h	32	TxSingleCollision	Number of packets successfully transmitted by a port that experienced exactly one collision
24h–27h	32	TxMultiple Collision	Number of packets successfully transmitted by a port that experienced more than one collision
28h–2Bh	32	TxDeferredTransmit	Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy
2Ch–2Fh	32	TxLateCollision	Number of times that a collision is detected later than 512 bit-times into the transmission of a packet
30h–33h	32	–	Reserved
34h–37h	32	TxFrameInDisc	Number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers [Page 0Ah].) This attribute only increments if a network device is not acting in compliance with a flow-control request or the BCM53101M internal flow control/buffering scheme has been misconfigured.
38h–3Bh	32	TxPausePkts	Number of PAUSE events on a given port
3Ch–3Fh	32	TXQ1PKT	Total number of good packets transmitted on CoS1, specified in MIB queue select register when QoS is enabled
40h–43h	32	TXQ2PKT	Total number of good packets transmitted on CoS2, specified in MIB queue select register when QoS is enabled
44h–47h	32	TXQ3PKT	Total number of good packets transmitted on CoS3, specified in MIB queue select register when QoS is enabled
48h–4Bh	32	TXQ4PKT	Total number of good packets transmitted on CoS4, specified in MIB queue select register when QoS is enabled
4Ch–4Fh	32	TXQ5PKT	Total number of good packets transmitted on CoS5, specified in MIB queue select register when QoS is enabled
50h–57h	64	RxOctets	Number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets
58h–5Bh	32	RxUndersizePkts	Number of good packets received by a port that are less than 64 bytes in length (excluding framing bits, but including the FCS)

Table 161: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
5Ch–5Fh	32	RxPausePkts	Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (88–08h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00–01), be a minimum of 64 bytes in length (excluding preamble, but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.
60h–63h	32	Pkts64Octets	Number of packets (including error packets) that are 64 bytes long
64h–67h	32	Pkts65to127Octets	Number of packets (including error packets) that are between 65 and 127 bytes long
68h–6Bh	32	Pkts128to255Octets	Number of packets (including error packets) that are between 128 and 255 bytes long
6Ch–6Fh	32	Pkts256to511Octets	Number of packets (including error packets) that are between 256 and 511 bytes long
70h–73h	32	Pkts512to1023Octets	Number of packets (including error packets) that are between 512 and 1023 bytes long
74h–77h	32	Pkts1024toMaxPktOctets	Number of packets (including error packets) that are between 1024 and MaxPacket bytes long
78h–7Bh	32	RxOversizePkts	Number of good packets received by a port that are greater than standard maximum frame size
7Ch–7Fh	32	RxJabbers	Number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error
80h–83h	32	RxAlignmentErrors	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard maximum frame size, inclusive, and have a bad FCS with a nonintegral number of bytes
84h–87h	32	RxFCSErrors	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard maximum frame size, inclusive, and have a bad FCS with an integral number of bytes
88h–8Fh	64	RxGoodOctets	Total number of bytes in all good packets received by a port (excluding framing bits but including FCS)

Table 161: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
90h–93h	32	RxDropPkts	Number of good packets received by a port that were dropped due to lack of resources (such as lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.
94h–97h	32	RxUnicastPkts	Number of good packets received by a port that are addressed to a unicast address
98h–9Bh	32	RxMulticastPkts	Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
9Ch–9Fh	32	RxBroadcastPkts	Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
A0h–A3h	32	RxSAChanges	Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.
A4h–A7h	32	RxFragments	Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error
A8h–ABh	32	JumboPkt	Number of frames received with frame size greater than the standard maximum size and less than or equal to the Jumbo Frame Size, regardless of CRC or alignment errors ***Note:*** InFrame count should count “the JumboPkt count with good CRC.”
ACh–AFh	32	RXSymbolError	Total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increments once per carrier event and does not increment on detection of collision during the carrier event.
B0h–B3h	32	InRangeErrors	Number of frames received with good CRC and the following conditions: • The value of Length/Type field is between 46 and 1500, inclusive, and does not match the number of (MAC Client Data + PAD) data octets received or • The value of Length/Type field is less than 46 and the number of data octets received is greater than 46 (which does not require padding).
B4h–B7h	32	OutOfRangeErrors	Number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536
C0h–C3h	32	RxDiscard	Number of good packets received by a port that were discarded by the forwarding process
F0h–F7h	64	–	“SPI Data I/O Register (Global, Address F0h–F7h)” on page 266, bytes 0–7
F8h–FDh	–	–	Reserved

Table 161: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
FEh	8	–	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	–	"Page Register (Global, Address FFh)" on page 267

Page 30h: QoS Registers

Table 162: Page 30h QoS Registers

Address	Bits	Description
00h	8	"QoS Global Control Register (Page 30h: Address 00h)" on page 216
01h–03h	–	Reserved
04h–05h	16	"QoS IEEE 802.1p Enable Register (Page 30h: Address 04h–05h)" on page 217
06h–07h	16	"QoS DiffServ Enable Register (Page 30h: Address 06h–07h)" on page 217
08h–0Fh	–	Reserved
10h–2Bh	32/port	"Port N (N = 0–5, 8) PCP_To_TC Map Register (Page 30h: Address 10h–2Bh)" on page 217
2Ch–2Fh	–	Reserved
30h–35h	48	"DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)" on page 218
36h–3Bh	48	"DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)" on page 219
3Ch–41h	48	"DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)" on page 220
42h–47h	48	"DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)" on page 220
48h–61h	–	Reserved
62h–63h	16	"TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221
64h–67h	32	"CPU_To_CoS Map Register (Page 30h: Address 64h–67h)" on page 222
68h–7Fh	–	Reserved
80h	8	"TX Queue Control Register (Page 30h: Address 80h)" on page 222
81h	8	"TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)" on page 223, Queue 0
82h	8	"TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)" on page 223, Queue 1
83h	8	"TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)" on page 223, Queue 2
84h	8	"TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)" on page 223, Queue 3

Table 162: Page 30h QoS Registers (Cont.)

Address	Bits	Description
85h–86h	16	"Class 4 Service Weight Register (Page 30h: Address 85h–86h)" on page 223
87h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

QoS Global Control Register (Page 30h: Address 00h)

Table 163: QoS Global Control Register (Page 30h: Address 00h)

Bit	Name	R/W	Description	Default
7	Aggregation Mode	R/W	When enable this bit, the IMP operates as the uplink port to the upstream network processor and the CoS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU and the CoS is decided based on the reasons for forwarding the packet to the CPU.	0
6	PORT_QOS_EN	R/W	Port-based QoS enable When port-based QoS is enabled, ingress frames are assigned a priority ID value based on the PORT_QOS_PRI bits in the "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)" on page 234. IEEE 802.1p and DiffServ priorities are disregarded. 0 = Disable port-based QoS. 1 = Enable port-based QoS. See "Quality of Service" on page 32 for more information.	0
5:4	Reserved	R/W	Write as default. Ignore on read.	0
3:2	QOS_LAYER_SEL	R/W	QoS priority selection Determine QoS priority scheme associated with frame: • 00 = Layer 2 QoS only. Select 802.1p if enabled and the RX frame is tagged; otherwise, select MAC-based • 01 = IP QoS only. Select DiffServ if enabled; otherwise, priority=0. • 10 = If (IP) then IP QoS else LAYER2 QoS. For IP frame, select DiffServ (0 if DiffServ is off); for L2 frames, select 802.1p if enabled and tagged; otherwise, MAC-based • 11 = Maximum priority of all QoS algorithms. Select maximum priority from port-based, DiffServ, or 802.1p if enabled. See Table 1 on page 35 for more information.	0
1:0	Reserved	R/W	Write as default. Ignore on read.	0

QoS IEEE 802.1p Enable Register (Page 30h: Address 04h–05h)

Table 164: QoS IEEE 802.1p Enable Register (Page 30h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	802_1P_EN	R/W	QoS IEEE 802.1p port mask • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Disable IEEE 802.1p priority for individual ports. 1 = Enable IEEE 802.1p priority for individual ports. See "IEEE 802.1Q VLAN" on page 38 for more information.	0

QoS DiffServ Enable Register (Page 30h: Address 06h–07h)

Table 165: QoS DiffServ Enable Register (Page 30h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as default. Ignore on read.	0
8:0	DIFFSERV_EN	R/W	DiffServ port mask • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Disable DiffServ priority for individual ports. 1 = Enable DiffServ priority for individual ports.	0

See "Quality of Service" on page 32 for more information.

Port N (N = 0–5, 8) PCP_To_TC Map Register (Page 30h: Address 10h–2Bh)

Table 166: Port N PCP_To_TC Map Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	IMP Port

These bits map the IEEE 802.1p priority level to one of the eight priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.

Table 167: Port PCP_To_TC Register (Page 30h: Address 10h–13h, 14h–17h, 18h–1Bh, 1Ch–1Fh, 20h–23h, 24h–27h, 28h–2Bh)

Bit	Name	R/W	Description	Default
31:24	Reserved	R/W	Write as default. Ignore on read.	0
23:21	1P_111_MAP	R/W	IEEE 802.1p priority tag field 111	111
20:18	1P_110_MAP	R/W	IEEE 802.1p priority tag field 110	110
17:15	1P_101_MAP	R/W	IEEE 802.1p priority tag field 101	101
14:12	1P_100_MAP	R/W	IEEE 802.1p priority tag field 100	100
11:9	1P_011_MAP	R/W	IEEE 802.1p priority tag field 011	011
8:6	1P_010_MAP	R/W	IEEE 802.1p priority tag field 010	010
5:3	1P_001_MAP	R/W	IEEE 802.1p priority tag field 001	001
2:0	1P_000_MAP	R/W	IEEE 802.1p priority tag field 000	000

See "Quality of Service" on page 32 for more information.

DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.

Table 168: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 001111_MAP	R/W	DiffServ DSCP priority tag field 001111	0
44:42	DIFFSERV_ 001110_MAP	R/W	DiffServ DSCP priority tag field 001110	0
41:39	DIFFSERV_ 001101_MAP	R/W	DiffServ DSCP priority tag field 001101	0
38:36	DIFFSERV_ 001100_MAP	R/W	DiffServ DSCP priority tag field 001100	0
35:33	DIFFSERV_ 001011_MAP	R/W	DiffServ DSCP priority tag field 001011	0
32:30	DIFFSERV_ 001010_MAP	R/W	DiffServ DSCP priority tag field 001010	0
29:27	DIFFSERV_ 001001_MAP	R/W	DiffServ DSCP priority tag field 001001	0
26:24	DIFFSERV_ 001000_MAP	R/W	DiffServ DSCP priority tag field 001000	0
23:21	DIFFSERV_ 000111_MAP	R/W	DiffServ DSCP priority tag field 000111	0
20:18	DIFFSERV_ 000110_MAP	R/W	DiffServ DSCP priority tag field 000110	0
17:15	DIFFSERV_ 000101_MAP	R/W	DiffServ DSCP priority tag field 000101	0
14:12	DIFFSERV_ 000100_MAP	R/W	DiffServ DSCP priority tag field 000100	0
11:9	DIFFSERV_ 000011_MAP	R/W	DiffServ DSCP priority tag field 000011	0
8:6	DIFFSERV_ 000010_MAP	R/W	DiffServ DSCP priority tag field 000010	0
5:3	DIFFSERV_ 000001_MAP	R/W	DiffServ DSCP priority tag field 000001	0

Table 168: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h) (Cont.)

Bit	Name	R/W	Description	Default
2:0	DIFFSERV_ 000000_MAP	R/W	DiffServ DSCP priority tag field 000000	0

See "Quality of Service" on page 32 for more information.

DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.

Table 169: DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 011111_MAP	R/W	DiffServ DSCP priority tag field 011111	0
44:42	DIFFSERV_ 011110_MAP	R/W	DiffServ DSCP priority tag field 011110	0
41:39	DIFFSERV_ 011101_MAP	R/W	DiffServ DSCP priority tag field 011101	0
38:36	DIFFSERV_ 011100_MAP	R/W	DiffServ DSCP priority tag field 011100	0
35:33	DIFFSERV_ 011011_MAP	R/W	DiffServ DSCP priority tag field 011011	0
32:30	DIFFSERV_ 011010_MAP	R/W	DiffServ DSCP priority tag field 011010	0
29:27	DIFFSERV_ 011001_MAP	R/W	DiffServ DSCP priority tag field 011001	0
26:24	DIFFSERV_ 011000_MAP	R/W	DiffServ DSCP priority tag field 011000	0
23:21	DIFFSERV_ 010111_MAP	R/W	DiffServ DSCP priority tag field 010111	0
20:18	DIFFSERV_ 010110_MAP	R/W	DiffServ DSCP priority tag field 010110	0
17:15	DIFFSERV_ 010101_MAP	R/W	DiffServ DSCP priority tag field 010101	0
14:12	DIFFSERV_ 010100_MAP	R/W	DiffServ DSCP priority tag field 010100	0
11:9	DIFFSERV_ 010011_MAP	R/W	DiffServ DSCP priority tag field 010011	0
8:6	DIFFSERV_ 010010_MAP	R/W	DiffServ DSCP priority tag field 010010	0
5:3	DIFFSERV_ 010001_MAP	R/W	DiffServ DSCP priority tag field 010001	0
2:0	DIFFSERV_ 010000_MAP	R/W	DiffServ DSCP priority tag field 010000	0

See "Quality of Service" on page 32 for more information.

DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.

Table 170: DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 101111_MAP	R/W	DiffServ DSCP priority tag field 101111	0
44:42	DIFFSERV_ 101110_MAP	R/W	DiffServ DSCP priority tag field 101110	0
41:39	DIFFSERV_ 101101_MAP	R/W	DiffServ DSCP priority tag field 101101	0
38:36	DIFFSERV_ 101100_MAP	R/W	DiffServ DSCP priority tag field 101100	0
35:33	DIFFSERV_ 101011_MAP	R/W	DiffServ DSCP priority tag field 101011	0
32:30	DIFFSERV_ 101010_MAP	R/W	DiffServ DSCP priority tag field 101010	0
29:27	DIFFSERV_ 101001_MAP	R/W	DiffServ DSCP priority tag field 101001	0
26:24	DIFFSERV_ 101000_MAP	R/W	DiffServ DSCP priority tag field 101000	0
23:21	DIFFSERV_ 100111_MAP	R/W	DiffServ DSCP priority tag field 100111	0
20:18	DIFFSERV_ 100110_MAP	R/W	DiffServ DSCP priority tag field 100110	0
17:15	DIFFSERV_ 100101_MAP	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DIFFSERV_ 100100_MAP	R/W	DiffServ DSCP priority tag field 100100	0
11:9	DIFFSERV_ 100011_MAP	R/W	DiffServ DSCP priority tag field 100011	0
8:6	DIFFSERV_ 100010_MAP	R/W	DiffServ DSCP priority tag field 100010	0
5:3	DIFFSERV_ 100001_MAP	R/W	DiffServ DSCP priority tag field 100001	0
2:0	DIFFSERV_ 100000_MAP	R/W	DiffServ DSCP priority tag field 100000	0

See "Quality of Service" on page 32 for more information.

DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.

Table 171: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 111111_MAP	R/W	DiffServ DSCP priority tag field 111111	0
44:42	DIFFSERV_ 111110_MAP	R/W	DiffServ DSCP priority tag field 111110	0
41:39	DIFFSERV_ 111101_MAP	R/W	DiffServ DSCP priority tag field 111101	0
38:36	DIFFSERV_ 111100_MAP	R/W	DiffServ DSCP priority tag field 111100	0
35:33	DIFFSERV_ 111011_MAP	R/W	DiffServ DSCP priority tag field 111011	0
32:30	DIFFSERV_ 111010_MAP	R/W	DiffServ DSCP priority tag field 111010	0
29:27	DIFFSERV_ 111001_MAP	R/W	DiffServ DSCP priority tag field 111001	0

Table 171: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h) (Cont.)

Bit	Name	R/W	Description	Default
26:24	DIFFSERV_ 111000_MAP	R/W	DiffServ DSCP priority tag field 111000	0
23:21	DIFFSERV_ 110111_MAP	R/W	DiffServ DSCP priority tag field 110111	0
20:18	DIFFSERV_ 110110_MAP	R/W	DiffServ DSCP priority tag field 110110	0
17:15	DIFFSERV_ 100101_MAP	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DIFFSERV_ 110100_MAP	R/W	DiffServ DSCP priority tag field 110100	0
11:9	DIFFSERV_ 110011_MAP	R/W	DiffServ DSCP priority tag field 110011	0
8:6	DIFFSERV_ 110010_MAP	R/W	DiffServ DSCP priority tag field 110010	0
5:3	DIFFSERV_ 110001_MAP	R/W	DiffServ DSCP priority tag field 110001	0
2:0	DIFFSERV_ 110000_MAP	R/W	DiffServ DSCP priority tag field 110000	0

See "Quality of Service" on page 32 for more information.

TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)

All the bits in Table 172 map the priority ID to one of the TX queues.

Table 172: TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)

Bit	Name	R/W	Description	Default
15:14	PRI_111_QID	R/W	Priority ID 111 mapped to TX Queue ID • 00 = Queue ID 0 • 01 = Queue ID 1 • 10 = Queue ID 2 • 11 = Queue ID 3	16'h0000
13:12	PRI_110_QID	R/W	Priority ID 110 mapped to TX Queue ID	
11:10	PRI_101_QID	R/W	Priority ID 101 mapped to TX Queue ID	
9:8	PRI_100_QID	R/W	Priority ID 100 mapped to TX Queue ID	
7:6	PRI_011_QID	R/W	Priority ID 011 mapped to TX Queue ID	
5:4	PRI_010_QID	R/W	Priority ID 010 mapped to TX Queue ID	
3:2	PRI_001_QID	R/W	Priority ID 001 mapped to TX Queue ID	
1:0	PRI_000_QID	R/W	Priority ID 000 mapped to TX Queue ID	

See "Quality of Service" on page 32 for more information.

CPU_To_CoS Map Register (Page 30h: Address 64h–67h)

Table 173: CPU_To_CoS Map Register (Page 30h: Address 64h–67h)

Bit	Name	R/W	Description	Default
31:18	Reserved	R/W	Write as default. Ignore on read.	0
17:15	Exception/Flooding Processing to CPU CoS Map	R/W	Packet forwarded to CPU for Exception Processing/Flooding reason The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
14:12	Protocol Snooping to CPU CoS Map	R/W	Packet forwarded to CPU for Protocol Snooping reason The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
11:9	Protocol Termination to CPU CoS Map	R/W	Packet forwarded to CPU for Protocol Termination reason The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
8:6	Switching/Flooding to CPU CoS Map	R/W	Packet forwarded to CPU for Switching/Flooding reason The CoS selection is based on the highest CoS values among all the reasons for the packet.	0
5:3	SA Learning to CPU CoS Map	R/W	Packet forwarded to CPU for SA Learning reason The CoS selection is based on the highest CoS among all the reasons for the packet.	0
2:0	Mirror to CPU CoS Map	R/W	Packet forwarded to CPU for mirroring reason The CoS selection is based on the highest CoS values among all the reasons for the packet.	0

TX Queue Control Register (Page 30h: Address 80h)

Table 174: TX Queue Control Register (Page 30h: Address 80h)

Bit	Name	R/W	Description	Default
7:2	Reserved	R/W	Write as default. Ignore on read.	0

Table 174: TX Queue Control Register (Page 30h: Address 80h) (Cont.)

Bit	Name	R/W	Description	Default
1:0	QoS_PRIORITY_CTRL	R/W	Best Effort Queues Priority Control This field controls the best effort queues' scheduling priority. 00 = All queues are weighted round robin 01 = CoS 3 is strict priority, CoS2–CoS0 are weighted round robin. 10 = CoS3 and CoS2 is strict priority, CoS1–CoS0 are weighted round robin. 11 = CoS3, CoS2, CoS1 and CoS0 are in strict priority. Strict priority: When it is in strict priority, the priority is CoS3 > CoS2 > CoS1 > CoS0. Weighted round robin: When it is in weighted round robin mode, the queues are scheduled in a round robin way according to the service weight of each queue.	00

See "Quality of Service" on page 32 for more information.

TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)

Table 175: TX Queue[0:3] Weight Register (Page 30h: Address 81h–84h)

Bit	Name	R/W	Description	Default
7:0	QSERV_WEIGHT	R/W	Queue Weight register The binary value of these bits sets the service weight of the given queue. The value of 1 allows the queue to send one packet for every round; the value of 4 allows the queue to send four packets for every round. It is suggested that the weight of each queue be Q3 > Q2 > Q1 > Q0 > 0. ***Note:*** The maximum allowable transmit queue weight is 31h. Programming a higher weight than 31h can yield unexpected results. This field must not be programmed as 0.	Queue 0 = 0001 Queue 1 = 0010 Queue 2 = 0100 Queue 3 = 1000

See "Quality of Service" on page 32 for more information.

Class 4 Service Weight Register (Page 30h: Address 85h–86h)

Table 176: Class 4 Service Weight Register (Page 30h: Address 85h–86h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0

Table 176: Class 4 Service Weight Register (Page 30h: Address 85h–86h) (Cont.)

Bit	Name	R/W	Description	Default
8	C4_Strict_Priority	R/W	C4 strict priority When this field is set to 1, the C4 _Service_Weight is "don't care" and Class 4 is in strict priority over the best effort queues (Q3–Q0).	1
7:0	C4 _Service_Weight	R/W	C4 service weight This field defines the service weight between Class 4 traffic and the Best Effort Q3–Q0. When this field is N, it means Class 4: Best-Effort = N:1 ***Note:*** When in weighted round robin mode, it is meaningless to set this field as 0.	1

Page 31h: Port-Based VLAN Registers

Table 177: Page 31h VLAN Registers

Address	Bits	Description
00h–11h	16/port	"Port-Based VLAN Control Register (Page 31h: Address 00h–11h)" on page 224
12h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Port-Based VLAN Control Register (Page 31h: Address 00h–11h)

Table 178: Port-Based VLAN Control Register Address Summary

Address	Description
00h–01h	Port 0
02h–03h	Port 1
04h–05h	Port 2
06h–07h	Port 3
08h–09h	Port 4
0Ah–0Bh	Port 5
0Ch–0Dh	Reserved
0Eh–0Fh	Reserved
10h–11h	IMP port

Table 179: Port VLAN Control Register (Page 31h: Address 00h–11h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	FORWARD_MASK	R/W	VLAN forwarding mask • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Disable VLAN forwarding to egress port. 1 = Enable VLAN forwarding to egress port.	1FFh

For more information, see "Port-Based VLAN" on page 37.

Page 32h: Trunking Registers

Table 180: Page 32h Trunking Registers

Address	Bits	Description
00h	8	"MAC Trunking Control Register (Page 32h: Address 00h)" on page 225
01h–0Fh	–	Reserved
10h–11h	16	"Trunking Group 0 Register (Page 32h: Address 10h–11h)" on page 226
12h–13h	16	"Trunking Group 1 Register (Page 32h: Address 12h–13h)" on page 226
14h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

MAC Trunking Control Register (Page 32h: Address 00h)

Table 181: MAC Trunk Control Register (Page 32h: Address 00h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	Write as default. Ignore on read.	0
3	MAC_BASE_TRNK_EN	R/W	Enable MAC base trunking The BCM53101M supports two trunking groups of up to four ports per group.	0
2	Reserved	R/W	Write as default. Ignore on read.	0

Table 181: MAC Trunk Control Register (Page 32h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
1:0	TRK_HASH_INDX	R/W	Trunk hash index selector 00 = Use hash [DA,SA] to generate index. 01 = Use hash [DA] to generate index. 10 = Use hash [SA] to generate index. 11 = Illegal state	0

See "Port Trunking/Aggregation" on page 40 for more information.

Trunking Group 0 Register (Page 32h: Address 10h–11h)

Table 182: Trunk Group 0 Register (Page 32h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	Trunk Group Enable	R/W	Trunk group enable 1 = Enable trunk group. 0 = Disable trunk group. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0

See "Port Trunking/Aggregation" on page 40 for more information.

Trunking Group 1 Register (Page 32h: Address 12h–13h)

Table 183: Trunk Group 1 Register (Page 32h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as default. Ignore on read.	0
8:0	Trunk Group Enable	R/W	Trunk group enable 1 = Enable trunk group. 0 = Disable trunk group. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively	0

Page 34h: IEEE 802.1Q VLAN Registers

Table 184: Page 34h IEEE 802.1Q VLAN Registers

Address	Bits	Description
00h	8	"Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 227
01h	8	"Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)" on page 229
02h	8	"Global VLAN Control 2 Register (Page 34h: Address 02h)" on page 229
03h–04h	16	"Global VLAN Control 3 Register (Page 34h: Address 03h–04h)" on page 230
05h	8	"Global VLAN Control 4 Register (Page 34h: Address 05h)" on page 231
06h	8	"Global VLAN Control 5 Register (Page 34h: Address 06h)" on page 232
07h–09h	8	Reserved
0Ah–0Bh	16	"VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)" on page 232
0Ch–0Fh	–	Reserved
10h–21h	16/port	"Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)" on page 234
22h–2Fh	–	Reserved
30h–31h	16	"Double Tagging TPID Register (Page 34h: Address 30h–31h)" on page 235
32h–33h	16	"ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)" on page 235
34h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Table 185: Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Bit	Name	R/W	Description	Default
7	Enable IEEE 802.1Q	R/W	Enable IEEE 802.1Q VLAN 0 = Disable IEEE 802.1Q VLAN. 1 = Enable IEEE 802.1Q VLAN. See "Programming the VLAN Table" on page 39 for more information. ***Note:*** This bit must be set if double tagging mode enable (En_DT_Mode = 01) in "Global VLAN Control 4 Register (Page 34h: Address 05h)" on page 231.	0

Table 185: Global IEEE 802.1Q Register (Pages 34h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
6:5	VLAN Learning Mode	R/W	VLAN learning mode • 00 = SVL (Shared VLAN learning mode) (MAC hash ARL table) • 11 = IVL (Individual VLAN learning mode) (MAC and VID hash ARL table) • 10 = Illegal setting • 01 = Illegal setting ***Note:*** Applied to 802.1Q enable, DT_Mode.	11
4	Reserved	R/W	Write as default. Ignore on read.	0
3	Change_1Q_VID	R/W	Change 1Q VID to PVID: Controls replacement of the 1Q VID with the PVID. 1 = • For a single tag frame with VID not = 0, change the VID to PVID. • For a double tag frame with outer VID not = 0, change outer VID to PVID. 0 = No change for 1Q/ISP tag if VID is not 0.	0
2	Reserved	R/W	Write as default. Ignore on read.	0
1	Change_1p_VID_Outer	R/W	Change outer 1p VID to PVID This bit controls replacement of the outer 1p VID with PVID: 1 = • For a single-tagged frame with VID = 0, change the VID to PVID. • For a double-tagged frame with outer VID = 0, change outer VID to PVID. 0 = No change for outer VID.	1
0	Change_1p_VID_Inner	R/W	Change inner 1p VID to PVID This bit controls replacement of the inner 1p VID with PVID: 1 = For a double-tagged frame with inner VID = 0, change inner VID to PVID. 0 = No change for inner VID.	1

See "IEEE 802.1Q VLAN" on page 38 for more information.

Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)

Table 186: Global VLAN Control 1 Register (Page 34h: Address 01h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Write as default. Ignore on read.	0
6	IPMC VLAN Untag Check Bypass	R/W	IPMC VLAN untagged map check 1 = IPMC frames are not checked against the VLAN untagged map. 0 = IPMC frames are checked against the VLAN untagged map. ***Note:*** Does not apply to the frame management port.	0
5	IPMC VLAN Forward Check Bypass	R/W	IPMC VLAN Forward Map Check 1 = IPMC frames are not checked against the VLAN forward map. 0 = IPMC frames are checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable, DT_Mode.	0
4	Reserved	R/W	Must not be 1	0
3	Reserved Multicast Untag Check Bypass	R/W	Reserved multicast (except GMRP and GVRP) VLAN untagged map check 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN untagged map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN untagged map. ***Note:*** Does not apply to the frame management port.	0
2	Reserved Multicast Forward Check Bypass	R/W	Reserved multicast (except GMRP and GVRP) VLAN forward map check 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN forward map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable, DT_Mode.	0
1	Reserved	R/W	Must not be 0	1
0	Reserved	R/W	Write as default. Ignore on read.	0

For more information, see "IEEE 802.1Q VLAN" on page 38.

Global VLAN Control 2 Register (Page 34h: Address 02h)

Table 187: Global VLAN Control 2 Register (Page 34h: Address 02h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Write as default. Ignore on read.	0

Table 187: Global VLAN Control 2 Register (Page 34h: Address 02h) (Cont.)

Bit	Name	R/W	Description	Default
6	GMRP/GVRP Untag Check Bypass	R/W	GMRP or GVRP VLAN untag map check 1 = GMRP or GVRP frames are checked against the VLAN untagged map. 0 = GMRP or GVRP frames are not checked against the VLAN untagged map. ***Note:*** Does not apply to the frame management port.	0
5	GMRP/GVRP Forward Check Bypass	R/W	GMRP or GVRP VLAN forward map check 1 = GMRP or GVRP frames are checked against the VLAN forward map. 0 = GMRP or GVRP frames are not checked against the VLAN forward map. ***Note:*** Does not apply to the frame management port. Applied to 802.1Q enable, DT_Mode.	0
4	Reserved	R/W	Write as default. Ignore on read.	1
3	Reserved	R/W	Write as default. Ignore on read.	0
2	IMP Frame Forward Bypass	R/W	IMP frame VLAN forward map check 1 = IMP frames are not checked against the VLAN forward map. 0 = IMP frames are checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable, DT_Mode.	0
1:0	Reserved	R/W	Write as default. Ignore on read.	00

For more information, see "IEEE 802.1Q VLAN" on page 38.

Global VLAN Control 3 Register (Page 34h: Address 03h–04h)

Table 188: Global VLAN Control 3 Register (Page 34h: Address 03h–04h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as default. Ignore on read.	N/A
8:0	Drop Non1Q Frames	R/W	Drop non-1Q frames When enabled, any frame without an IEEE 802.1Q tag is dropped by this port. This field does not apply to the IMP port (includes Port 5 if Dual-IMP ports enabled), En_IMP_PORT = 11 in "Global Management Configuration Register (Page 02h: Address 00h)" on page 164. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. ***Note:*** This field has no effect in double-tagging mode.	0

Global VLAN Control 4 Register (Page 34h: Address 05h)

Table 189: Global VLAN Control 4 Register (Page 34h: Address 05h)

Bit	Name	R/W	Description	Default
7:6	Ingress_VID_Check	R/W	Perform ingress VLAN source port membership check. Ingress VID violation is detected when the source port is not found in the VLAN Fwd_Map that is referred to by the ingress VID. • 00 = Forward ingress VID violation frame, but do not learn the SA into the ARL table. • 01 = Drop frame if ingress VID violation is detected. • 10 = Bypass checking for ingress VID violation, and learn the SA into the ARL table. • 11 = Forward ingress VID violation frame to IMP, but do not learn the SA into the ARL table. ***Note:*** Does not apply to the IMP port (includes Port 5 if Dual-IMP ports enabled), En_IMP_PORT = 11 in "Global Management Configuration Register (Page 02h: Address 00h)" on page 164).	11
5	Forward GVRP to Management	R/W	Forward all GVRP frames to the frame management port. • 1 = GVRP frames are forwarded to the management port. • 0 = GVRP frames are not forwarded to the management port.	0
4	Forward GMRP to Management	R/W	Forward all GMRP frames to the frame management port. • 1 = GMRP frames are forwarded to the management port. • 0 = GMRP frames are not forwarded to the management port.	0
3:2	En_DT_Mode	R/W	Enable double-tagging mode. • 00 = Disable double tagging mode • 01 = Enable DT_Mode (double tagging mode) • 1x = Reserved	2'b00
1	RSV_MCAST_FLOOD	R/W	Used when the BCM53101M is configured to operate in double-tagged mode (DT_Mode) and management mode 1 = Flood (including all data port and CPU) reserved multicast based on the VLAN rule. 0 = Trap reserved multicast to the CPU. ***Note:*** Reserved multicast includes 01-80-C2-00-00-(00,02–2F)	
0	Reserved	R/W	Write as default. Ignore on read.	0

For more information, see "IEEE 802.1Q VLAN" on page 38.

Global VLAN Control 5 Register (Page 34h: Address 06h)

Table 190: Global VLAN Control 5 Register (Page 34h: Address 06h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Write as default. Ignore on read.	0
6	Tag Status Preserve	R/W	IEEE 802.1Q tag/untag status preserved at egress. 1 = Regardless of untag map in VLAN table, non-1Q frames (including 802.1p frames) are not changed at TX (egress). ***Note:*** This field has no effect in double-tagged mode (DT_Mode).	0
5	Reserved	R/W	Reserved	0
4	Trunk Check Bypass	R/W	Trunk check bypass 1 = Egress directed frames issued from the IMP port bypass trunk checking. 0 = Egress directed frames issued from the IMP port are subject to trunk checking and redirection.	1
3	Drop Invalid VID	R/W	Drop frames with invalid VID. Frames with an invalid VID do not have a corresponding entry in the VLAN table. 1 = Ingress frames with invalid VID are dropped. 0 = Ingress frames with invalid VID are forwarded to the IMP port.	0
2	VID_FFF_Fwding	R/W	Enable VID FFF forward 1 = Forward frame 0 = Comply with standard, drop frame	0
1	Reserved	R/W	Reserved	0
0	Management CRC Check Bypass	R/W	Bypass CRC check at the frame management port. 1 = Ignore CRC check 0 = Check CRC	0

For more information, see "IEEE 802.1Q VLAN" on page 38.

VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Table 191: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0

Table 191: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
11	EN_MPORT5_untagmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
10	EN_MPORT5 _fwdmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
9	EN_MPORT4_untagmap	R/W	When set to 1, MPORT_ADD4 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
8	EN_MPORT4 _fwdmap	R/W	When set to 1, MPORT_ADD4 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
7	EN_MPORT3_untagmap	R/W	When set to 1, MPORT_ADD3 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
6	EN_MPORT3 _fwdmap	R/W	When set to 1, MPORT_ADD3 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
5	EN_MPORT2_untagmap	R/W	When set to 1, MPORT_ADD2 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
4	EN_MPORT2 _fwdmap	R/W	When set to 1, MPORT_ADD2 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
3	EN_MPORT1_untagmap	R/W	When set to 1, MPORT_ADD1 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0
2	EN_MPORT1 _fwdmap	R/W	When set to 1, MPORT_ADD1 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0
1	EN_MPORT0_untagmap	R/W	When set to 1, MPORT_ADD0 is checked by VLAN untag map. ***Note:*** Does not apply to the frame management port.	0

Table 191: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
0	EN_MPORT0 _fwdmap	R/W	When set to 1, MPORT_ADD0 is checked by VLAN forward map. ***Note:*** Does not apply to the frame management port.	0

Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)

Table 192: Default IEEE 802.1Q Tag Register Address Summary

Address	Description
10h–11h	Port 0
12h–13h	Port 1
14h–15h	Port 2
16h–17h	Port 3
18h–19h	Port 4
1Ah–1Bh	Port 5
1Ch–1Dh	Reserved
1Eh–1Fh	Reserved
20h–21h	IMP port

Table 193: Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)

Bit	Name	R/W	Description	Default
15:13	DEFAULT_PRI/ PORT_QoS_PRI	R/W	Default IEEE 802.1Q priority If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, these bits are the default priority value for the new tag. See "IEEE 802.1Q VLAN" on page 38 for more information. Port-based QoS priority map bits When port-based QoS is enabled in the Table : "QoS Global Control Register (Page 30h: Address 00h)," on page 216, these bits represent the TC for the ingress port. The TC determines the TX queue for each frame based on the "TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)" on page 221.	000
12	CFI	R/W	Conical form indicator	0
11:0	DEFAULT_VID	R/W	Default IEEE 802.1Q VLAN ID If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q or priority-tagged frame, these bits are the default VID for the new tag. See "IEEE 802.1Q VLAN" on page 38 for more information.	001

Double Tagging TPID Register (Page 34h: Address 30h–31h)

Table 194: Double Tagging TPID Register (Page 34h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:0	ISP_TPID	R/W	TPID used to identify double-tagged frame.	9100h

ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Table 195: ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:8	RESERVED	R/W	Write as default. Ignore on read.	0
7:0	ISP_Portmap	R/W	Bitmap that defines which port is designated as the ISP port. • Bit 8 = IMP port • Bits [7:6] = Reserved • Bits [5:0] correspond to ports 5–0, respectively. 0 = Indicates that it is not an ISP port. 1 = Indicates that it is an ISP port.	0

Page 36h: DoS Prevent Register

Table 196: DoS Prevent Register

Address	Bits	Description
00h–03h	32	“DoS Control Register (Page 36h: Address 00h–03h)” on page 236
04h	8	“Minimum TCP Header Size Register (Page 36h: Address 04h)” on page 237
05h–07h	–	Reserved
08h–0Bh	32	“Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)” on page 238
0Ch–0Fh	32	“Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)” on page 238
10h	8	“DoS Disable Learn Register (Page 36h: Address 10h)” on page 238
11h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h–F7h)” on page 266
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 267
FFh	8	“Page Register (Global, Address FFh)” on page 267

DoS Control Register (Page 36h: Address 00h–03h)

Table 197: DoS Control Register (Page 36h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:14	Reserved	RO	Write as default. Ignore on read.	0
13	ICMPv6_LongPing_DROP_EN	R/W	ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size 1 = Drop specified packet 0 = Do not drop	0
12	ICMPv4_LongPing_DROP_EN	R/W	ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its total length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header 1 = Drop specified packet 0 = Do not drop	0
11	ICMPv6_Fragment_DROP_EN	R/W	ICMPv6 protocol data unit carried in a fragmented IPv6 datagram 1 = Drop specified packet 0 = Do not drop	0
10	ICMPv4_Fragment_DROP_EN	R/W	ICMPv4 protocol data unit carried in a fragmented IPv4 datagram 1 = Drop specified packet 0 = Do not drop	0
9	TCP_FragError_DROP_EN	R/W	Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data 1 = Drop specified packet 0 = Do not drop	00
8	TCP_ShortHDR_DROP_EN	R/W	Length of TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size 1 = Drop specified packet 0 = Do not drop	00
7	TCP_SYNError_DROP_EN	R/W	SYN = 1, ACK = 0, and SRC_Port < 1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0

Table 197: DoS Control Register (Page 36h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
6	TCP_SYNFINScan_DROP_EN	R/W	SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0
5	TCP_XMASScan_DROP_EN	R/W	Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0
4	TCP_NULLScan_DROP_EN	R/W	Seq_Num = 0 and all TCP_FLAGs = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0
3	UDP_BLAT_DROP_EN	R/W	DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0
2	TCP_BLAT_DROP_EN	R/W	DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram 1 = Drop specified packet 0 = Do not drop	0
1	IP_LAN_DRIP_EN	R/W	IPDA = IPSA in an IPv4/v6 datagram 1 = Drop specified packet 0 = Do not drop	0
0	RESERVED	R/W	Write as default. Ignore on read. ***Note:*** It is illegal to set 0	1

Minimum TCP Header Size Register (Page 36h: Address 04h)

Table 198: Minimum TCP Header Size Register (Page 36h: Address 04h)

Bit	Name	R/W	Description	Default
7:0	MIN_TCP_HDR_SIZE	R/W	Minimum TCP header size allowed (0–256 bytes, inclusive)	14h

Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)

Table 199: Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv4_SIZE	R/W	Maximum ICMPv4 size allowed (0–9.6 KB, inclusive)	32'd512

Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)

Table 200: Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv6_SIZE	R/W	Maximum ICMPv6 size allowed (0–9.6 KB, inclusive)	32'd512

DoS Disable Learn Register (Page 36h: Address 10h)

Table 201: DoS Disable Learn Register (Page 36h: Address 10h)

Bit	Name	R/W	Description	Default
7:1	RESERVED	R/W	Write as default. Ignore on read.	–
0	DoS Disable Lrn	R/W	When this bit enabled, all frames dropped by DoS prevent are not learned.	0

Page 40h: Maximum Frame Control Registers

Table 202: Page 40h Jumbo Frame Control Registers

Address	Bits	Description
00h	–	Reserved
01h–04h	32	"Jumbo Frame Port Mask Register (Page 40h: Address 01h–04h)" on page 239
05h–06h	16	"Standard Maximum Frame Size Register (Page 40h: Address 05h–06h)" on page 240
07h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Jumbo Frame Port Mask Register (Page 40h: Address 01h–04h)

Table 203: Jumbo Frame Port Mask Register (Page 40h: Address 01h–04h)

Bit	Name	R/W	Description	Default
31:25	Reserved	RO	Write as default. Ignore on read.	0
24	Jumbo_EN	R/W	Jumbo Frame Enable Setting this bit enables the BCM53101M to receive and transmit 9KB (9216B) frames. If simultaneously enabling the jumbo packet mode and jumbo packet FIFO enable bits in the "Auxiliary Mode 2 Register (Page 10h–14h: Address 36h–37h)" on page 205, the maximum frame size that BCM53101M can receive and transmit is extended to 9720B.	0
23:9	Reserved	RO	Write as default. Ignore on read.	0
8:0	Jumbo Frame Port Mask	R/W	Jumbo Frame Port Mask Port mask that defines which correspondent port is enabled to receive/transmit jumbo frames. • Bit 8 = IMP port • Bits [7:] = Reserved • Bits [:0] correspond to ports 54–0, respectively – 1 = Jumbo frame capability is enabled – 0 = Jumbo frame capability is disabled	–

Note: A jumbo frame is any frame with a length that is over the standard maximum frame size and up to 9720B. Jumbo frames are allowed to be delivered among these ports. However, Broadcom recommends that no more than two ports be enabled simultaneously to ensure the system performance.

Standard Maximum Frame Size Register (Page 40h: Address 05h–06h)

Table 204: Standard Maximum Frame Size Register (Page 40h: Address 05h–06h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Write as default. Ignore on read.	0
13:0	Standard Maximum Frame Size	R/W	Standard maximum frame size Defines the standard maximum frame size for MAC and MIB counter. This register defines the maximum ingress packet size including all tags. The maximum value of this register is 2048. • When jumbo is disabled, the content of this register is used to define good frame length. • When jumbo is enabled, all frames are dropped if the frame length is larger than 9720 bytes. This register setting affects the following MIB counters: • RxSAChange • RxGoodOctets • RxUnicastPkts • RxMulticastPkts • RxBroadcastPkts • RxOverSizePkts	‘d2000

Page 41h: Broadcast Storm Suppression Registers

Table 205: Broadcast Storm Suppression Registers (Page 41h)

Address	Bits	Description
00h–03h	32	"Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)" on page 241
04h–0Fh	–	Reserved
10h–33h	32/port	"Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243
34h–7Fh	–	Reserved
80h–91h	16/port	"Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)" on page 246
92h–BFh	–	Reserved
C0h–C1h	8	"IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)" on page 247
C2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)

Table 206: Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:19	Reserved	R/W	Write as default. Ignore on read.	0
18	XLENEN	R/W	Packet length selection 0 = Ingress/egress rate excludes IPG. 1 = Ingress/egress rate includes IPG.	0
17	BUCK1_ BRM_SEL	R/W	Bit rate mode selection (bucket 1) 0 = Absolute bit rate mode — The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode — The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243 represents the incoming bit rate normalized with respect to the link speed mode. See "Rate Control" on page 41 for more details.	0
16	Reserved	R/W	Write as default. Ignore on read.	1

Table 206: Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
15:9	BUCK1_PACKET_TYPE	R/W	Suppressed packet type mask (bucket 1) Determines type of packets to be monitored by bucket 1. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: • Bit 9 = Unicast lookup hit • Bit 10 = Multicast lookup hit • Bit 11 = Reserved MAC Address Frame (01-80-C2-00-00-2F) • Bit 12 = Broadcast • Bit 13 = Multicast lookup failure • Bit 14 = Unicast lookup failure • Bit 15 = Reserved See "Rate Control" on page 41 for more details.	0
8	BUCK0_ BRM_SEL	R/W	Bit rate mode selection (bucket 0) 0 = Absolute bit rate mode — The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode — The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h–33h)" on page 243 represents the incoming bit rate normalized with respect to the link speed mode. See "Rate Control" on page 41 for more details.	0
7	Reserved	R/W	Write as default. Ignore on read.	1
6:0	BUCK0_PACKET_TYPE	R/W	Suppressed packet type mask (bucket 0) Determines type of packets to be monitored by bucket 0. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: • Bit 0 = Unicast lookup hit • Bit 1 = Multicast lookup hit • Bit 2 = Reserved MAC address frame (01-80-C2-00-00-2F) • Bit 3 = Broadcast • Bit 4 = Multicast lookup failure • Bit 5 = Unicast lookup failure • Bit 6 = Reserved See "Rate Control" on page 41 for more details.	0

Port Receive Rate Control Register (Page 41h: Address 10h–33h)

Table 207: Port Receive Rate Control Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	Reserved
2Ch–2Fh	Reserved
30h–33h	IMP port for BCM53101M

Table 208: Port Receive Rate Control Register (Page 41h: Address 10h–33h)

Bit	Name	R/W	Description	Default
31:30	Reserved	R/W	Write as default. Ignore on read.	0
29	En_VLAN-based_ Policing	R/W	Enable VLAN-based policing. • 1 = Enable • 0 = Disable When enabled, the ingress logic uses the final VID to look up the VLAN table, where two bits in the VLAN table decide whether that specific VLAN entry is targeted for VLAN policing, and the bucket ID of the policing. Each of the bucket 0/1 can police one or more VLAN + storm suppression traffic as specified in "Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)".	0
28	STRM_SUPR_EN	R/W	Enable storm suppression (supported by bucket 1). 0 = Disable 1 = Enable	0
27	RsvMC_SUPR_EN	R/W	Enable reserved multicast storm suppression. (Reserved multicast = 01-80-C2-00-00-00 to 01-80-C2-00-00-2F) 0 = Disable 1 = Enable	0
26	BC_SUPR_EN	R/W	Enable broadcast storm suppression. 0 = Disable 1 = Enable	0
25	MC_SUPR_EN	R/W	Enable multicast storm suppression. 0 = Disable 1 = Enable	0

Table 208: Port Receive Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

Bit	Name	R/W	Description	Default
24	DLF_SUPR_EN	R/W	Enable DLF (unicast) storm suppression. 0 = Disable 1 = Enable	0
23	Enable Bucket1	R/W	Enable rate control of the ingress port (bucket 1). 0 = Disable 1 = Enable	0
22	Enable Bucket0	R/W	Enable rate control of the ingress port (bucket 0). 0 = Disable 1 = Enable	0
21:19	BUCK1_SIZE	R/W	Bucket size Determine the maximum size of bucket 1. Bucket size affects burst traffic rate. This is specified on a per-port basis. • 000 = 16 KB (Valid 4 KB) • 001 = 20 KB (Valid 8 KB) • 010 = 28 KB (Valid 16 KB) • 011 = 44 KB (Valid 32 KB) • 100 = 76 KB (Valid 64 KB) • Others = 512 KB (Valid 500 KB) See “Rate Control” on page 41 for more details.	000
18:11	BUCK1_Rate_Cnt	R/W	Bucket rate count The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per-port basis. The programmed values of the rate count and the bit rate mode of the “Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)” on page 241 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the “Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)” on page 241. See “Rate Control” on page 41 for more details. Values written to these bits must be with the ranges specified by Table 3 on page 42. Values outside these ranges are not valid.	10h

Table 208: Port Receive Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

Bit	Name	R/W	Description	Default
10:8	BUCK0_SIZE	R/W	Bucket size Determine the maximum size of bucket 0. Bucket size affects burst traffic rate. This is specified on a per-port basis. • 000 = 16 KB (Valid 4 KB) • 001 = 20 KB (Valid 8 KB) • 010 = 28 KB (Valid 16 KB) • 011 = 44 KB (Valid 32 KB) • 100 = 76 KB (Valid 64 KB) • Others = 512 KB (Valid 500 KB) See "Rate Control" on page 41 for more details.	000
7:0	BUCK0_Rate_Cnt	R/W	Bucket rate count The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per-port basis. The programmed values of the rate count and the bit rate mode of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)" on page 241 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed packet type mask in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)" on page 241. See "Rate Control" on page 41 for more details.	10h

Port Suppressed Packet Drop Count Register (Page 41h: Address 50h–73h)

Table 209: Port Suppressed Packet Drop Count Register Address Summary

Address	Description
50h–53h	Port 0
54h–57h	Port 1
58h–5Bh	Port 2
5Ch–5Fh	Port 3
60h–63h	Port 4
64h–67h	Port 5
68h–6Bh	Reserved
6Ch–6Fh	Reserved
70h–73h	IMP port for BCM53101M

Table 210: Port Suppressed Packet Drop Count Register (Page 41h: Address 50h–73h)

Bit	Name	R/W	Description	Default
31:0	Packet Dropped Count	RO (SC)	Packet dropped count Record the dropped packet count for the suppression drop count or jumbo filtered count. This register clears itself after read.	0

Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)

Table 211: Port Egress Rate Control Configuration Register Address Summary

Address	Description
80h–81h	Port 0
82h–83h	Port 1
84h–85h	Port 2
86h–87h	Port 3
88h–89h	Port 4
8Ah–8Bh	Port 5
8Ch–8Dh	Reserved
8Eh–8Fh	Reserved
90h–91h	IMP port

Table 212: Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11	ERC_EN	R/W	Egress rate control enable (absolute bit rate)	0
10:8	BKT_SZE	R/W	Bucket size Determines maximum size of bucket 0. Specified on a per-port basis. • 000 = 6 KB (Valid 4 KB) • 001 = 20 KB (Valid 8 KB) • 010 = 28 KB (Valid 16 KB) • 011 = 44 KB (Valid 32 KB) • 100 = 76 KB (Valid 64 KB) • Others = 512 KB (Valid 500 KB) See “Rate Control” on page 41 for more details.	0
7:0	RFSH_CNT	R/W	Refresh count for bucket	0

IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)

Table 213: IMP Port (IMP/Port 5) Egress Rate Control Configuration Register Address Summary

Address	Description
C0h	IMP port
C1h	Port 5 (enable dual-IMP ports, En_IMP_PORT=11 in "Global Management Configuration Register (Page 02h: Address 00h)" on page 164.

Table 214: IMP Port Egress Rate Control Configuration Registers Bit Definitions

Bit	Name	R/W	Description	Default
7:6	RESERVED	R/W	Write as default. Ignore on read.	0
5:0	Rate_Index	R/W	Rate_Index is used to configure different egress rates for IMP in packets-per-second (pps). See Table 215: "Using Rate_Index to Configure Different Egress Rates for IMP in pps," on page 248. • When set to 0, the egress rate is limited to a maximum of 384 pps. • When set to 63, the egress rate control function is disabled and all packets are transmitted at wire-speed. ***Note:*** If Rate_Index is configured as a certain value, the egress rate is limited to the corresponding speed whether the switch is running at 10 Mbps, 100 Mbps, or 1 Gbps. ***Note:*** Rate_Index should be a reasonable value under the corresponding network speed configuration. It does not make sense to set a value of 63 with the network configuration at 10 Mbps. In that case, the egress rate is limited up to 10 Mbps.	6'd63

Table 215: Using Rate_Index to Configure Different Egress Rates for IMP in pps

Rate_Index	*pps*	*Rate_Index*	*pps*	*Rate_Index*	*pps*	*Rate_Index*	*pps*
0	384	16	5376	32	25354	48	357143
1	512	17	5887	33	27382	49	423729
2	639	18	6400	34	29446	50	500000
3	768	19	6911	35	31486	51	568182
4	1024	20	7936	36	35561	52	641026
5	1280	21	8960	37	39682	53	714286
6	1536	22	9984	38	42589	54	781250
7	1791	23	11008	39	56818	55	862069
8	2048	24	12030	40	71023	56	925926
9	2303	25	13054	41	85324	57	1000000
10	2559	26	14076	42	99602	58	1086957
11	2815	27	15105	43	113636	59	1136364
12	3328	28	17146	44	127551	60	1190476
13	3840	29	19201	45	142045	61	1250000
14	4352	30	21240	46	213675	62	1315789
15	4863	31	23299	47	284091	63	1388889

Page 42h: EAP Registers

Table 216: EAP Registers (Page 42h)

Address	Bits	Description
00h	8	"EAP Global Control Register (Page 42h: Address 00h)" on page 249
01h	8	"EAP Multiport Address Control Register (Page 42h: Address 01h)" on page 250
02h–09h	64	"EAP Destination IP Register 0 (Page 42h: Address 02h–09h)" on page 251
0Ah–12h	64	"EAP Destination IP Register 1 (Page 42h: Address 0Ah–12h)" on page 251
13h–1Fh	–	Reserved
20h–4Fh	64	"Port EAP Configuration Register (Page 42h: Address 20h–4Fh)" on page 251
50h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

EAP Global Control Register (Page 42h: Address 00h)

Table 217: EAP Global Control Registers (Page 42h: Address 00h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Write as default. Ignore on read.	0
6	EN_RARP	R/W	When EAP_BLK_MODE is set: 1 = Allow RARP to pass. 0 = Drop RARP	0
5	EN_BPDU	R/W	When EAP_BLK_MODE is set: 1 = BPDU Addresses are allowed to pass. 0 = Drop BPDU	0
4	EN_RMC	R/W	When EAP_BLK_MODE is set: 1 = Allows DA = 01-80-C2-00-00-02, 04–0F to pass. 0 = Drop DA = 01-80-C2-00-00-02, 04–0F.	0
3	EN_DHCP	R/W	When EAP_BLK_MODE is set: 1 = Allows DHCP to pass 0 = Drop DHCP	0
2	EN_ARP	R/W	When EAP_BLK_MODE is set: 1 = Allows ARP to pass 0 = Drop ARP	0

Table 217: EAP Global Control Registers (Page 42h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
1	EN_2DIP	R/W	When EAP_BLK_MODE bit is set: 1 = Two subnet IP addresses defined in "EAP Destination IP Register 0 (Page 42h: Address 02h–09h)" and "EAP Destination IP Register 1 (Page 42h: Address 0Ah–12h)" are allowed to pass. 0 = Drop	0
0	Reserved	R/W	Write as default. Ignore on read.	0

EAP Multiport Address Control Register (Page 42h: Address 01h)

Table 218: EAP Multiport Address Control Register (Page 42h: Address 01h)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Write as default. Ignore on read.	0
5	EN_MPORT5	R/W	1 = Allow multiport ETYPE address 5 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0
4	EN_MPORT4	R/W	1 = Allow multiport ETYPE address 4 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0
3	EN_MPORT3	R/W	1 = Allow Multiport ETYPE Address 3 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0
2	EN_MPORT2	R/W	1 = Allow Multiport ETYPE Address 2 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0
1	EN_MPORT1	R/W	1 = Allow Multiport ETYPE Address 1 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0
0	EN_MPORT0	R/W	1 = Allow Multiport ETYPE Address 0 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 to pass. 0 = Drop	0

EAP Destination IP Register 0 (Page 42h: Address 02h–09h)

Table 219: EAP Destination IP Registers 0 (Page 42h: Address 02h–09h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB 0	R/W	EAP destination IP subnet register 0	0
31:0	DIP_MSK 0	R/W	EAP destination IP mask register 0	0

EAP Destination IP Register 1 (Page 42h: Address 0Ah–12h)

Table 220: EAP Destination IP Registers 1 (Page 42h: Address 0Ah–12h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB 1	R/W	EAP destination IP subnet register 1	0
31:0	DIP_MSK 1	R/W	EAP destination IP mask register 1	0

Port EAP Configuration Register (Page 42h: Address 20h–4Fh)

Table 221: Port EAP Configuration Register Address Summary

Address	Description
20h–27h	Port 0
28h–2Fh	Port 1
30h–37h	Port 2
38h–3Fh	Port 3
40h–47h	Port 4
48h–4Fh	Port 5

Table 222: Port EAP Configuration Registers (Page 42h: Address 20h–4Fh)

BIt	Name	R/W	Description	Default
63:55	Reserved	R/W	Write as default. Ignore on read.	0
52:51	EAP_MODE	R/W	00 = Basic mode, do not check SA. 01 = Reserved 10 = Extend mode. Check SA and port number. Drop if SA is unknown. 11 = Simplified mode. Check SA and port number. Trap to management port if SA is unknown.	0
50:49	EAP_BLK_MODE	R/W	00 = Do not check EAP_BLK_MODE. 01 = Check EAP_BLK MODE on ingress port, only frame defined in EAP_GCFG will be forwarded. Otherwise, frame will be dropped. 10 = Reserved 11 = Check EAP_BLK MODE on both ingress and egress ports. Only frame defined in EAP_GCFG will be forwarded. The forwarding process will verify that each egress port is at block mode.	0
48	EAP_EN_DA	R/W	Enable EAP frame with DA	0
47:0	EAP_DA	R/W	EAP frame DA register	00-00-00-00-00-00

Page 43h: MSPT Registers

Table 223: MSPT Registers (Page 43h)

Address	Bits	Description
00h	8	MSPT control register
01h	–	Reserved
02h–05h	32	"MSPT Aging Control Register (Page 43h: Address 02h–05h)" on page 253
06h–0Fh	–	Reserved
10h–2Fh	32	"MSPT Table Register (Page 43h: Address 10h–2Fh)" on page 254
30h–4Fh	–	Reserved
50h–51h	16	"SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)" on page 254
52h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

MSPT Control Register (Page 43h: Address 00h–01h)

Table 224: MSPT Control Registers (Page 43h: Address 00h–01h)

Bit	Name	R/W	Description	Default
7:1	Reserved	R/W	Write as default. Ignore on read.	0
0	EN_802.1S	R/W	0 = Disable. Only 1 Spanning Tree support 1 = Enable 802.1S	0

MSPT Aging Control Register (Page 43h: Address 02h–05h)

Table 225: MSPT Aging Control Registers (Page 43h: Address 02h–05h)

Bit	Name	R/W	Description	Default
31:8	Reserved	R/W	Write as default. Ignore on read.	0
7:0	MSPT_AGE_MAP	R/W	Per spanning tree aging enable	0

MSPT Table Register (Page 43h: Address 10h–2Fh)

Table 226: MSPT Table Register Address Summary

Address	Description
10h–13h	MSPT 0
14h–17h	MSPT 1
18h–1Bh	MSPT 2
1Ch–1Fh	MSPT 3
20h–23h	MSPT 4
24h–27h	MSPT 5
28h–2Bh	MSPT 6
2Ch–2Fh	MSPT 7

Table 227: MSPT Table Registers (Page 43h: Address 10h–2Fh)

Bit	Name	R/W	Description	Default
31:18	Reserved	R/W	Write as default. Ignore on read.	0
17:15	SPT_STA5	R/W	Spanning tree state for port 5	0
14:12	SPT_STA4	R/W	Spanning tree state for port 4	0
11:9	SPT_STA3	R/W	Spanning tree state for Port 3	0
8:6	SPT_STA2	R/W	Spanning tree state for Port 2	0
5:3	SPT_STA1	R/W	Spanning tree state for Port 1	0
2:0	SPT_STA0	R/W	Spanning tree state for Port 0 • 000 = No spanning tree • 001 = Disabled • 010 = Blocking • 011 = Listening • 100 = Learning • 101 = Forwarding	0

SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

Table 228: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as default. Ignore on read.	0
5	EN_MPORT5_BYPASS_SPT	R/W	1 = MPORT_ADD_5 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_5 is checked by SPT status.	0

Table 228: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h) (Cont.)

Bit	Name	R/W	Description	Default
4	EN_MPORT4_BYPASS_SPT	R/W	1 = MPORT_ADD_4 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_4 will be checked by SPT status.	0
3	EN_MPORT3_BYPASS_SPT	R/W	1 = MPORT_ADD_3 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_3 is checked by SPT status.	0
2	EN_MPORT2_BYPASS_SPT	R/W	1 = MPORT_ADD_2 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_2 is checked by SPT status.	0
1	EN_MPORT1_BYPASS_SPT	R/W	1 = MPORT_ADD_1 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_1 is checked by SPT status.	0
0	EN_MPORT0_BYPASS_SPT	R/W	1 = MPORT_ADD_0 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h–67h)" on page 176 is not checked by SPT status. 0 = MPORT_ADD_0 is checked by SPT status.	0

Page 70h: MIB Snapshot Control Register

Table 229: MIB Snapshot Control Register

Address	Bits	Description
00h	8	"MIB Snapshot Control Register (Page 70h: Address 00h)" on page 256
01h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266 bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

MIB Snapshot Control Register (Page 70h: Address 00h)

Table 230: MIB Snapshot Control Register (Page 70h: Address 00h)

Bit	Name	R/W	Description	Default
7	SNAPSHOT_START/DONE	R/W SC	Snapshot start/done command When enabled, this self-clear bit indicates that the process is completed and the snapshot is ready at Page 71h: Port MIB Snapshot Register. • 1 = Initiate MIB snapshot function independent of the SNAPSHOT_MIRROR setting. • 0 = Snapshot function completed	0
6	SNAPSHOT_MIRROR	R/W	Snapshot mirror control 1 = Enable mirroring the port MIB counters from Page 71h: Port MIB Snapshot Register to Page 20h–28h: Port MIB Registers as specified in SNAPSHOT_PORT. 0 = Port MIB counters are accessible from Page 20h–28h: Port MIB Registers.	0
5:4	Reserved	R/W	Write as default. Ignore on read.	–
3:0	SNAPSHOT_PORT	R/W	Port number for MIB snapshot These bits specify the port number to snapshot: • 8 = IMP port • [7:6] = Reserved • [5:0] correspond to ports 5–0, respectively.	0

Page 71h: Port MIB Snapshot Register

Table 231: Port MIB Snapshot Control Register

Address	Bits	Description
71h	–	This page contains the snapshot of the "Page 20h–28h: Port MIB Registers" on page 211.

Page 85h: WAN Interface (Port 5) External PHY MII Registers

Table 232: WAN Interface (Port 5) External PHY MII Registers

Address	Bits	Description
85h	–	MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are "Page 10h–14h: Internal PHY MII Registers" on page 188.

Page 88h: IMP Port External PHY MII Registers Page Summary

Table 233: IMP Port External PHY MII Registers Page Summary

Address	Bits	Description
88h	–	MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are "Page 10h–14h: Internal PHY MII Registers" on page 188.

Page 90h: BroadSync™ HD Registers

Table 234: BroadSync HD Registers

Address	Bits	Description
00h–01h	16	BroadSync HD Enable Control Register (Page 90h, Address 00h–01h)
02h	8	BroadSync HD Timestamp Report Control Register (Page 90h, Address 02h)
03h	–	Reserved
04h–05h	16	BroadSync HD Maximum AV Packet Size Register (Page 90h, Address 04h–05h)
06h–0Fh	–	Reserved
10h–13Fh	32	BroadSync HD Time Base Register (Page 90h, Address 10h–13h)
14h–17h	32	BroadSync HD Timestamp Report Control Register (Page 90h, Address 14h–17h)
18h–1Bh	32	BroadSync HD Slot Number and Tick Counter Register (Page 90h, Address 18h–1Bh)
1Ch–1Fh	32	BroadSync HD Slot Adjustment Register (Page 90h, Address 1Ch–1Fh)
20h–2Fh	–	Reserved
30h–3Bh	16/port	BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
3Ch–5Fh	–	Reserved
60h–6Bh	16/port	BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
6Ch–8Fh	–	Reserved
90h–A7h	32/port	BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
A8h–AEh	–	Reserved
AFh	8	BroadSync HD Egress Timestamp Status Register (Page 90h, Address AFh)
B0h–B1h	16	BroadSync HD Port AV Link Status Register (Page 90h, Address B0h–B1h)
B2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

BroadSync HD Enable Control Register (Page 90h, Address 00h–01h)

Table 235: BroadSync HD Enable Control Register (Page 90h, Address 00h–01h)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as default. Ignore on read.	0
5:0	AV Enable	R/W	Per-port AV enable • 1 = Enable • 0 = Disable	0

BroadSync HD Timestamp Report Control Register (Page 90h, Address 02h)

Table 236: BroadSync HD Timestamp Report Control Register (Page 90h, Address 02h)

Bit	Name	R/W	Description	Default
7:1	Reserved	R/W	Write as default. Ignore on read.	0
0	TS_rpt_pkt_En	R/W	Timestamp reporting packet enable This field allows Timestamp Reporting Packet to IMP when the time synchronization packet transmitted on egress port • 1 = Enable • 0 = Disable	0

BroadSync HD Maximum AV Packet Size Register (Page 90h, Address 04h–05h)

Table 237: BroadSync HD Maximum AV Packet Size Register (Page 90h, Address 04h–05h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11:0	Max_ AV_Packet_Size	R/W	Maximum AV packet size This field defines the maximum packet size of AV packet (residential Ethernet). Ingress port uses it to qualify if a packet is allowed to pass through an AV link. Egress port uses it to perform the shaping gate.	12'd1518

BroadSync HD Time Base Register (Page 90h, Address 10h–13h)

Table 238: BroadSync HD Time Base Register (Page 90h, Address 10h–13h)

Bit	Name	R/W	Description	Default
31:0	TIME_BASE	R/W	Time base This is a 32-bit free running clock (running in 25 MHz) for BroadSync HD time base. Ingress and Egress ports use it for Time Synchronization Packet timestamp.	0

BroadSync HD Timestamp Report Control Register (Page 90h, Address 14h–17h)

Table 239: BroadSync HD Timestamp Report Control Register (Page 90h, Address 14h–17h)

Bit	Name	R/W	Description	Default
31:12	Reserved	R/W	Write as default. Ignore on read.	0
11:8	Time_Adjust_Period	R/W	Time adjust period This field defines the tick numbers that apply to the adjusted Time_Increment when Time_Increment does not equal 40. ***Example:*** Increment TIME_BASE to 41 for 10 ticks. In this case, set Time_Adjust_Period to 10 and Time_Increment to 41.	0
7:6	Reserved	R/W	Write as default. Ignore on read.	0
5:0	Time_Increment	R/W	Time increment This field defines the value to be added into the TIME_BASE in each 25 MHz tick during time adjust period. This field must be preconfigured prior to enabling for time adjustment.	0

BroadSync HD Slot Number and Tick Counter Register (Page 90h, Address 18h–1Bh)

Table 240: BroadSync HD Slot Number And Tick Counter Register (Page 90h, Address 18h–1Bh)

Bit	Name	R/W	Description	Default
31:28	Reserved	R/W	Write as default. Ignore on read.	0
27:16	TICK_COUNTER	R/W	Defines when SLOT_NUMBER counter increments. It runs from 1 to 3125 (or 3124, or 3126, depending on the SLOT_ADJUSTMENT setting of BroadSync HD Slot Adjustment Register (Page 90h, Address 1Ch–1Fh)) under 25 MHz.	0
15:5	Reserved	R/W	Write as default. Ignore on read.	0
4:0	SLOT_NUMBER	R/W	Specifies slot number for BroadSync HD	0

BroadSync HD Slot Adjustment Register (Page 90h, Address 1Ch–1Fh)

Table 241: BroadSync HD Slot Adjustment Register (Page 90h, Address 1Ch–1Fh)

Bit	Name	R/W	Description	Default
31:18	Reserved	R/W	Write as default. Ignore on read.	0
17:16	Macroslot Period	R/W	Macroslot period This field defines the slot time of a macroslot for Class 4 traffic: • 00 = 1 ms • 01 = 2 ms • 10 = 4 ms • 11 = Reserved Class 5 traffic slot time is always 125 µs period.	0
15:12	Reserved	R/W	Write as default. Ignore on read.	0
11:8	Slot Adjustment Period	R/W	Slot adjustment period This field defines the number of slots to apply to the altered slot adjustment.	0
7:2	Reserved	R/W	Write as default. Ignore on read.	0
1:0	Slot_Adjustment	R/W	Slot adjustment This field defines when Slot_Number counter increments by 1 (default is 40). Slot_Number increments by 1 when Tick_Counter rolls over. • 00 = 3125 • 01 = 3126 • 10 = 3124 • 11 = Reserved	

BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)

Table 242: BroadSync HD Class 5 Bandwidth Control Register Address Summary

Address	Description
30h–31h	Port 0 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
32h–33h	Port 1 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
34h–35h	Port 2 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
36h–37h	Port 3 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
38h–39h	Port 4 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)
3Ah–3Bh	Port 5 BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)

Table 243: BroadSync HD Class 5 Bandwidth Control Register (Page 90h, Address 30h–3Bh)

Bit	Name	R/W	Description	Default
15	C5_Window	R/W	Class 5 traffic credit carry-over control for port Controls the credit carry-over under different link speed: • For 100M link, 125 µs slot is too small such that BroadSync HD packet could easily "slip slot", so the credit carry-over should be allowed. • For 1G link, 125 µs slot is reasonably big such that the BW reservation could be done in a conservative way to prevent "slot slipping", so credit carry-over is not needed.	0
14	Reserved	R/W	Write as default. Ignore on read.	0
13:0	C5_Bandwidth	R/W	Class 5 bandwidth for port N Defines the byte count allowed for Class 5 traffic transmission within a slot time	0

BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)

Table 244: BroadSync HD Class 4 Bandwidth Control Register Address Summary

Address	Description
60h–61h	Port 0 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
62h–63h	Port 1 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
64h–65h	Port 2 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
66h–67h	Port 3 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
68h–69h	Port 4 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)
6Ah–6Bh	Port 5 BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)

Table 245: BroadSync HD Class 4 Bandwidth Control Register (Page 90h, Address 60h–6Bh)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/W	Write as default. Ignore on read.	0
13:0	C4_Bandwidth	R/W	Class 4 Bandwidth for port N This field defines the byte count allowed for Class 4 traffic transmission within a slot time.	0

BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)

Table 246: BroadSync HD Egress Timestamp Register Address Summary

Address	Description
90h–93h	Port 0 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
94h–97h	Port 1 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
98h–9Bh	Port 2 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
9Ch–9Fh	Port 3 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
A0h–A3h	Port 4 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)
A4h–A7h	Port 5 BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)

Table 247: BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h)

Bit	Name	R/W	Description	Default
31:0	Egress TS_Time_Stamp	R/W	Egress time synchronization packet timestamp This field reports the timestamp of the egress time synchronization packet. It uses 32 bit-time base for timestamping. The time between the departure of the first byte of the MAC DA and the timestamping point should be constant.	0

BroadSync HD Egress Timestamp Status Register (Page 90h, Address AFh)

Table 248: BroadSync HD Egress Timestamp Status Register (Page 90h, Address AFh)

Bit	Name	R/W	Description	Default
7:6	Reserved	R/W	Write as default. Ignore on read.	0
5:0	Valid_Status	R/W	Valid status Indicates the valid status for each timestamp register. ***Note:*** Once BroadSync HD Egress Timestamp Register (Page 90h, Address 90h–A7h) is read, the valid_status is cleared.	0

BroadSync HD Port AV Link Status Register (Page 90h, Address B0h–B1h)

Table 249: BroadSync HD Port AV Link Status Register (Page 90h, Address B0h–B1h)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as default. Ignore on read.	0
5:0	Port AV Link Status	R/W	When software write the port AV link status and select bit 14 in LED function, the AV link status is shown on the LED.	0
Note: Port 5 status can be outputted on serial LED, but not Parallel LED.				

Page 91h: Traffic Remarking Registers

Table 250: Traffic Remarking Registers

Address	Bits	Description
00h–03h	32	“Traffic Remarking Control Register (Page 91h: Address 00h–03h)” on page 265
04h–0Fh	–	Reserved
10h–57h	32	“Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h–57h)” on page 265
58h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h–F7h)” on page 266, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 267
FFh	8	“Page Register (Global, Address FFh)” on page 267

Traffic Remarking Control Register (Page 91h: Address 00h–03h)

Table 251: Traffic Remarking Control Register (Page 91h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:25	Reserved	R/W	Write as default. Ignore on read.	0
24:16	PCP_REMARKING_EN	R/W	PCP remarking enable • Bit 24 = IMP port • Bits [23:22] = Reserved • Bits [21:16] correspond to ports [5:0], respectively.	0
15:0	Reserved	R/W	Write as default. Ignore on read.	0

Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h–57h)

Table 252: Egress Non-BroadSync HD Packet TC to PCP Mapping Register Address Summary

Address	Description
10h–17h	Port 0
18h–1Fh	Port 1
20h–27h	Port 2
28h–2Fh	Port 3
30h–37h	Port 4
38h–3Fh	Port 5
40h–47h	Reserved
48h–4Fh	Reserved
50h–57h	IMP

Table 253: Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h–57h)

Bit	Name	R/W	Description	Default
63:31	Reserved	R/W	Write as default. Ignore on read.	0
30:28	PCP for TC = 7	R/W	The PCP field for TC = 7	3'b111
27	Reserved	R/W	Write as default. Ignore on read.	0
26:24	PCP for TC = 6	R/W	The PCP field for TC = 6	3'b110
23	Reserved	R/W	Write as default. Ignore on read.	0
22:20	PCP for TC = 5	R/W	The PCP field for TC = 5	3'b101
19	Reserved	R/W	Write as default. Ignore on read.	0
18:16	PCP for TC = 4	R/W	PCP field for TC = 4	3'b100

Table 253: Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h–57h) (Cont.)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as default. Ignore on read.	0
14:12	PCP for TC = 3	R/W	PCP field for TC = 3	3'b011
11	Reserved	R/W	Write as default. Ignore on read.	0
10:8	PCP for TC = 2	R/W	PCP field for TC = 2	3'b010
7	Reserved	R/W	Write as default. Ignore on read.	0
6:4	PCP for TC = 1	R/W	PCP field for TC = 1	3'b001
3	Reserved	R/W	Write as default. Ignore on read.	0
2:0	PCP for TC = 0	R/W	PCP field for TC = 0	3'b000

Global Registers

Table 254: Global Registers (Maps to All Pages)

Address	Bits	Description
F0h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 0
F1h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 1
F2h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 2
F3h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 3
F4h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 4
F5h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 5
F6h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 6
F7h	8	"SPI Data I/O Register (Global, Address F0h–F7h)" on page 266, 7
F8–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 267
FFh	8	"Page Register (Global, Address FFh)" on page 267

SPI Data I/O Register (Global, Address F0h–F7h)

Table 255: SPI Data I/O Register (Maps to All Registers, Address F0h–F7h)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes [7:0]	0

SPI Status Register (Global, Address FEh)

Table 256: SPI Status Register (Maps to All Registers, Address FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI read/write complete flag	0
6	Reserved	RO	Write as default. Ignore on read.	0
5	RACK	RO (SC)	SPI read data ready acknowledgement (self-clearing)	0
4:0	Reserved	RO	Write as default. Ignore on read.	0

Page Register (Global, Address FFh)

Table 257: Page Register (Maps to All Registers, Address FFh)

Bit	Name	R/W	Description	Default
7:0	PAGE_REG	R/W	Binary value, determines value of accessed register page	0

Section 9: Electrical Characteristics

Absolute Maximum Ratings

Table 258: Absolute Maximum Ratings

Symbol	Parameter and Pins	Minimum	Maximum	Units
–	Supply voltage: VDDBIAS, VDDXTAL	GND–0.3	2.75	V
–	Supply voltage: VDDC, VDDA, PLLAVDD, PLLDVDD	GND–0.3	1.32	V
–	Supply voltage: VDDO, VDDO1, VDDO2, VDDO3 at 2.5V	GND–0.3	2.75	V
–	Supply voltage: VDDO, VDDO1, VDDO2, VDDO3 at 3.3V	GND–0.3	3.63	V
I_I	Input current	–	–	mA
T_{STG}	Storage temperature	–40	+125	°C
V_{ESD}	Electrostatic discharge	–	–	V
–	Input voltage: digital input pins	–	–	V
T_J	Absolute maximum junction temperature	–	125	°C

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Recommended Operating Conditions

Table 259: Recommended Operating Conditions

Symbol	Parameter	Pins	Minimum	Maximum	Units
VDD	Supply voltage	VDDC, VDDA, PLLAVDD, PLLDVDD	1.14	1.26	V
		VDDO, VDDO1, VDDO2, VDDO3 at 3.3V	3.14	3.47	V
		VDDO, VDDO1, VDDO2, VDDO3 at 2.5V	2.38	2.63	V
		VDDBIAS, VDDXTAL	2.38	2.63	V
V_{IH}	High-level input voltage	All digital inputs	2.0	–	V
V_{IL}	Low-level input voltage	All digital inputs	–	0.8	V
T_A	Ambient operating temperature	_	0	70	°C

Electrical Characteristics

Table 260: I_{DD} for 10BASE-T (A0 Silicon)

Ports/Conditions	Parameter	Pins	Typical	Maximum	Units
5 ports	1.2V supply current	–	90.1	95.9	mA
	2.5V supply current	–	34	34.5	mA
	2.5V center tap current	–	196.8*	203.6*	mA
	2.5V (RGMII) current	VDDO2	4.7	4.9	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	9.4	10.9	mA
5 ports + MII + RGMII	1.2V supply current	–	96	102.2	mA
	2.5V supply current	–	34	34.5	mA
	2.5V center tap current	–	196.6*	203.4*	mA
	2.5V (RGMII) current	VDDO2	12.6	13.1	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	8.1	9.4	mA
4 ports + MII + RGMII	1.2V supply current	–	94.1	100.2	mA
	2.5V supply current	–	29.5	29.9	mA
	2.5V center tap current	–	159*	164.5*	mA
	2.5V (RGMII) current	VDDO2	12.6	13.1	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	7	8.1	mA
* The center tap current is approximately 3 mA higher per port for the B0 silicon.					

Table 261: I_{DD} for 100BASE-TX (A0 Silicon)

Condition	Parameter	Pins	Typical	Maximum	Units
5 ports	1.2V supply current	–	155.5	166.3	mA
	2.5V supply current	–	60.7	61.6	mA
	2.5V center tap current	–	129.1*	133.8*	mA
	2.5V (RGMII) current	VDDO2,	4.7	4.9	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	11.5	13.5	mA
5 ports + MII + RGMII	1.2V supply current	–	160.9	172.1	mA
	2.5V supply current	–	60.7	61.6	mA
	2.5V center tap current	–	129.1*	133.8*	mA
	2.5V (RGMII) current	VDDO2,	21.2	22	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	13.2	15.5	mA

Table 261: I_{DD} for 100BASE-TX (A0 Silicon) (Cont.)

Condition	Parameter	Pins	Typical	Maximum	Units
4 ports + MII + RGMII	1.2V supply current	–	146.2	156.4	mA
	2.5V supply current	–	50.8	51.6	mA
	2.5V center tap current	–	104.7*	108.5*	mA
	2.5V (RGMII) current	VDDO2,	19.8	20.5	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	11.1	13.0	mA

Table 262: I_{DD} for Power-Saving Mode (A0 Silicon)

Condition	Parameter	Pins	Typical	Maximum	Units
5 ports APD	1.2V supply current	–	81.1	–	mA
	2.5V supply current	–	11.4	–	mA
	2.5V center tap current	–	5.4*	–	mA
	2.5V (RGMII) current	VDDO2,	4.7	–	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	1.4	–	mA
5 ports sleep mode	1.2V supply current	–	36.9	–	mA
	2.5V supply current	–	11.2	–	mA
	2.5V center tap current	–	4.5*	–	mA
	2.5V (RGMII) current	VDDO2,	0.3	–	mA
	3.3V supply current	VDDO, VDDO1, VDDO3	1.4	–	mA
* The center tap current is approximately 3 mA higher per port for the B0 silicon.					

Table 263: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	Digital output pins at 3.3V VDDO, VDDO1, VDDO2, VDDO3	I_{OH} = –8 mA I_{OH} = –16 mA	2.4	–	–	V
		Digital output pins at 2.5V VDDO2		2.0	–	–	V
V_{OL}	Low-level output voltage	Digital output pins at 3.3V VDDO, VDDO1, VDDO2, VDDO3	I_{OL} = +8 mA I_{OL} = +16 mA	–	–	0.4	V
		Digital output pins at 2.5V VDDO2					
V_{IH}	High-level input voltage	Digital input pins at 3.3V: VDDO, VDDO1, VDDO2, VDDO3	–	2.0	–	–	V
		Digital input pins at 2.5V VDDO2	–	2.0	–	–	V

Table 263: Electrical Characteristics (Cont.)

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
V_{IL}	Low-level input voltage	Digital input pins at 3.3V: VDDO, VDDO1, VDDO2, VDDO3	–	–0.3	–	0.8	V
		Digital input pins at 2.5V VDDO2	–	–0.3	–	0.8	V
I_I	Input current	Digital inputs w/ pull-up resistors	V_I = 3.3V or 2.5V	–	–	–10	µA
		Digital inputs w/ pull-up resistors	V_I = GND	–	–	–250	µA
		Digital inputs w/ pull-down resistors	V_I = 3.3V or 2.5V	–	–	+250	µA
		Digital inputs w/ pull-down resistors	V_I = GND	–	–	+10	µA
		All other digital inputs	GND ≤ V_I ≤ 3.3V or 2.5V	–	–	±100	µA

Section 10: Timing Characteristics

Reset and Clock Timing

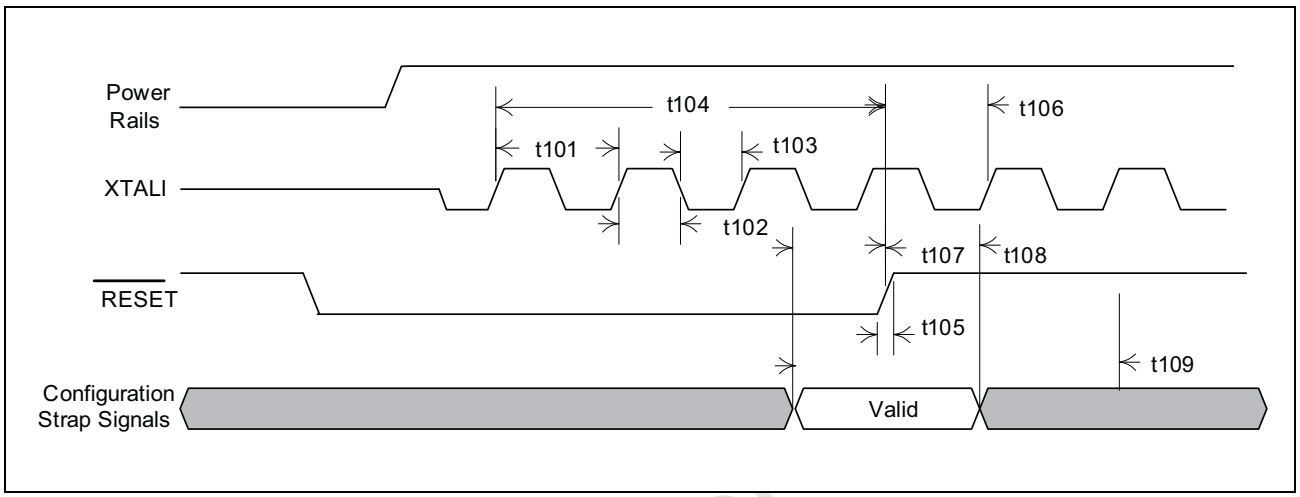


Figure 49: Reset and Clock Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 264: Reset and Clock Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
XTALI period	t101	39.998 ns	40 ns	40.002 ns
XTALI high time	t102	18 ns	–	22 ns
XTALI low time	t103	18 ns	–	22 ns
$\overline{\text{RESET}}$ low pulse duration	t104	80 ms	100 ms	–
$\overline{\text{RESET}}$ rise time	t105	–	–	25 ns
Configuration valid setup to $\overline{\text{RESET}}$ rising	t107	100 ns	–	–
Configuration valid hold from $\overline{\text{RESET}}$ rising	t108	–	–	100 ns
Hardware initialization is complete. All the strap pin values are clocked in, and the internal registers can be accessed.	t109	5 ms before the registers can be accessed		

MII/TMII Interface Timing

The following specifies timing information for the MII/TMII Interface pins.

MII/TMII Input Timing

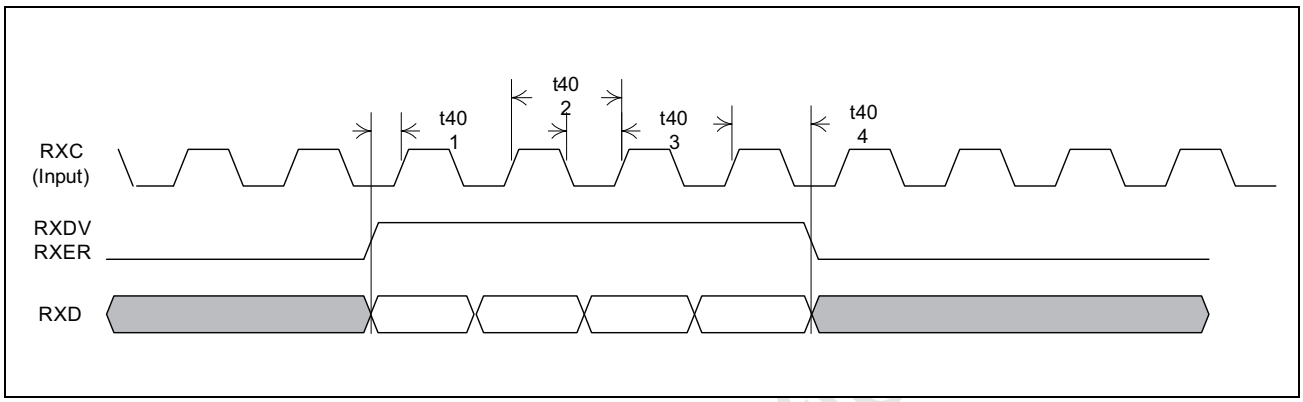


Figure 50: MII Input Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 265: MII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t401	RXDV, RXD to RXC rising setup time	10 ns	–	–
t402	RXC clock period (10BASE-T mode)	–	400 ns	–
	RXC clock period (100BASE-TX mode)	–	40 ns	–
t403	RXC high/low time (10BASE-T mode)	160 ns	–	240 ns
	RXC high/low time (100BASE-TX mode)	16 ns	–	24 ns
t404	RXDV, RXD to RXC rising hold time	10 ns	–	–
–	Duty cycle	–	–	–

Table 266: TMII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t401	RXDV, RXD to RXC rising setup time	5 ns	–	–
t402	RXC clock period	–	20 ns	–
t403	RXC high/low time	8 ns	–	12 ns

Table 266: TMII Input Timing

Parameter	Description	Min	Typ	Max
t404	RXDV, RXD to RXC rising hold time	5 ns	–	–
–	Duty cycle	–	–	–

MII/TMII Output Timing

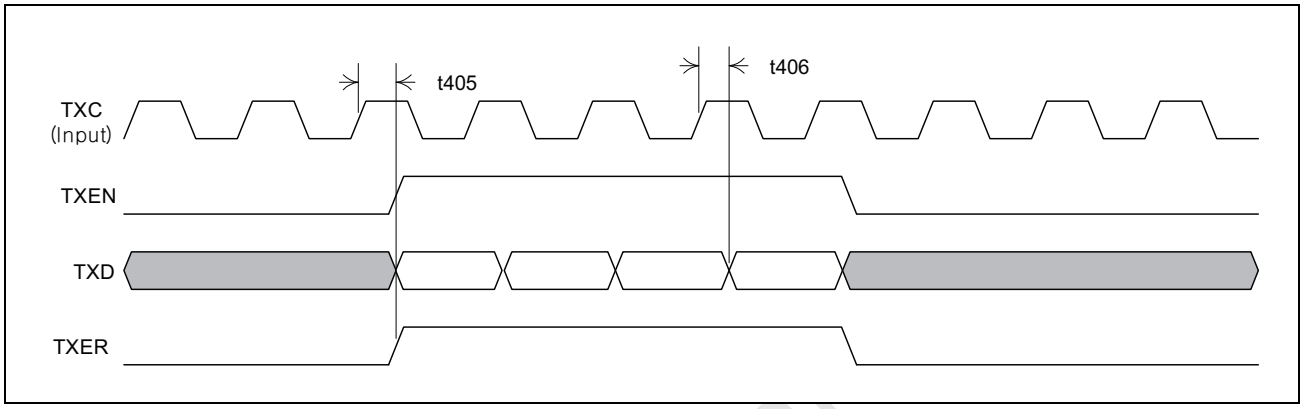


Figure 51: MII Output Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 267: MII Output Timing

Parameter	Description	Min	Typ	Max
t405	TXC high to TXEN, TXD valid	0 ns	–	25 ns
t406	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

Table 268: TMII Output Timing

Parameter	Description	Min	Typ	Max
t405	TXC high to TXEN, TXD valid	0 ns	–	12.5 ns
t405	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

RMII Interface Timing

RMII Input/Output Timing

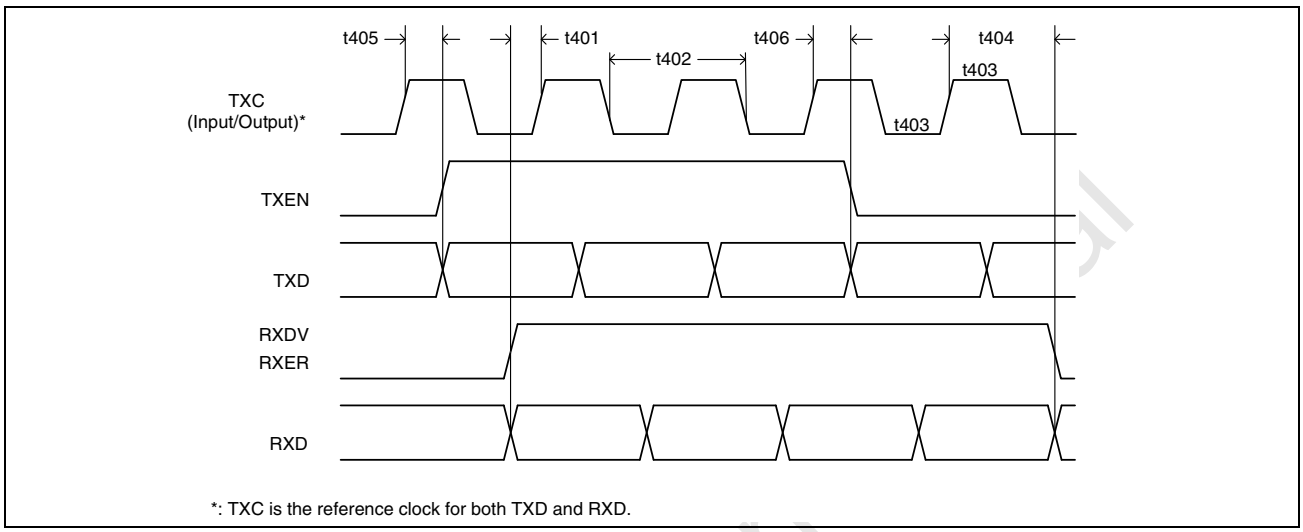


Figure 52: RMII Input/Output Timing

The following specifies timing information for the RMII interface pins.

Table 269: RMII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t401	RXDV, RXD to TXC rising setup time	4 ns	–	–
t402	TXC clock period (external clock mode)	–	20 ns	–
t403	TXC high/low time (external clock mode)	7 ns	–	13 ns
t404	RXDV, RXD to TXC rising hold time	2 ns	–	–
–	Duty cycle	–	–	–

Table 270: RMII Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t402	TXC clock period (internal clock mode)	–	20 ns	–
t403	TXC high/low time (internal clock mode)	7 ns	–	13 ns
t405	TXC high to TXEN, TXD valid	–	–	16 ns
t406	TXC high to TXEN, TXD invalid (hold)	2 ns	–	–

Reverse MII/TMII Interface Timing

The following specifies timing information regarding the Reverse MII/TMII interface pins.

Reverse MII/TMII Input Timing

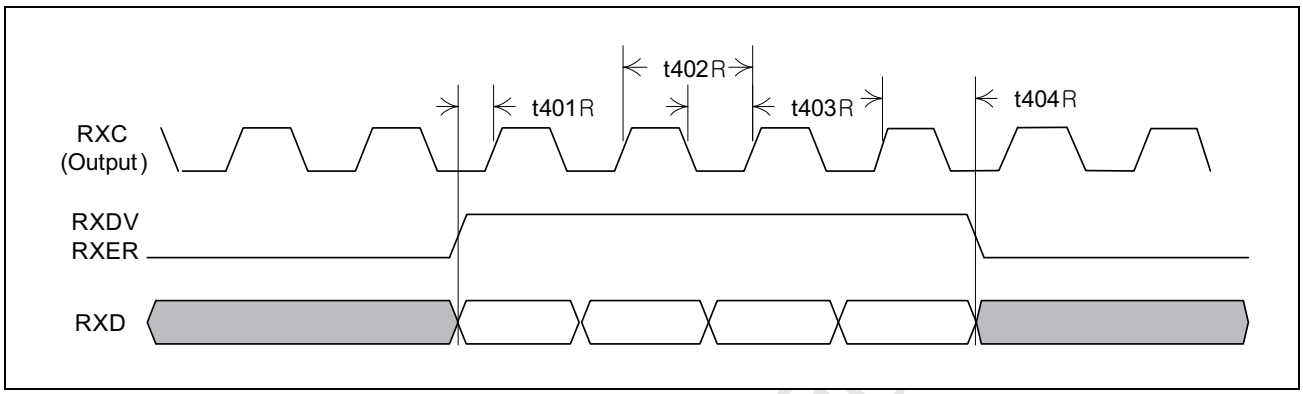


Figure 53: Reverse MII Input Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 271: Reverse MII Input Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
RXDV, RXD to RXC rising setup time	t401R	10	–	–	ns
RXC (output) clock period (10BASE-T mode)	t402R	–	400	–	ns
RXC clock period (100BASE-TX mode)		–	40	–	ns
RXC high/low time (10BASE-T mode)	t403R	160	–	240	ns
RXC high/low time (100BASE-TX mode)		16	–	24	ns
RXDV, RXD to RXC rising hold time	t404R	0	–	–	ns

Table 272: Reverse TMII Input Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
RXDV, RXD to RXC rising setup time	t401R	7.5 (Port 5) 10 (Port 8)	–	–	ns
RXC (output) clock period	t402R	–	20	–	ns
RXC high/low time (10BASE-T mode)	t403R	8	–	12	ns
RXDV, RXD to RXC rising hold time	t404R	0	–	–	ns

Reverse MII Output Timing

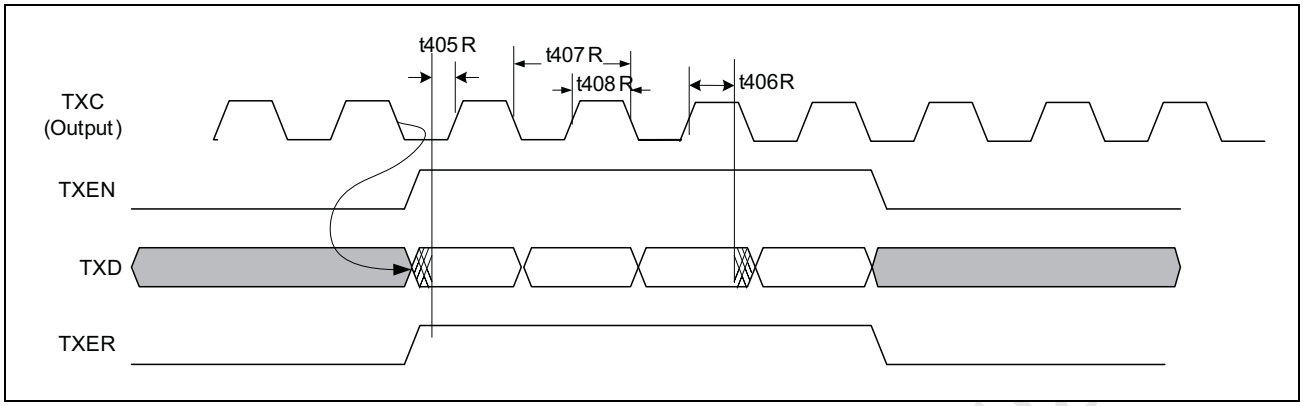


Figure 54: Reverse MII Output Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 273: Reverse MII Output Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Output (TXD, TX_EN) setup to TXC rising	t405R	15	–	25	ns
Output (TXD, TX_EN) hold from TXC rising	t406R	11	–	–	ns
TXC clock period	t407R	–	40	–	ns
TXC high/low time	t408R	15	–	22	ns

Table 274: Reverse TMII Output Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Output (TXD, TX_EN) setup to TXC rising	t405R	5	–	–	ns
Output (TXD, TX_EN) hold from TXC rising	t406R	5	–	–	ns
TXC clock period	t407R	–	20	–	ns
TXC high/low time	t408R	7.5	–	11	ns

RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

RGMII Output Timing (Normal Mode)

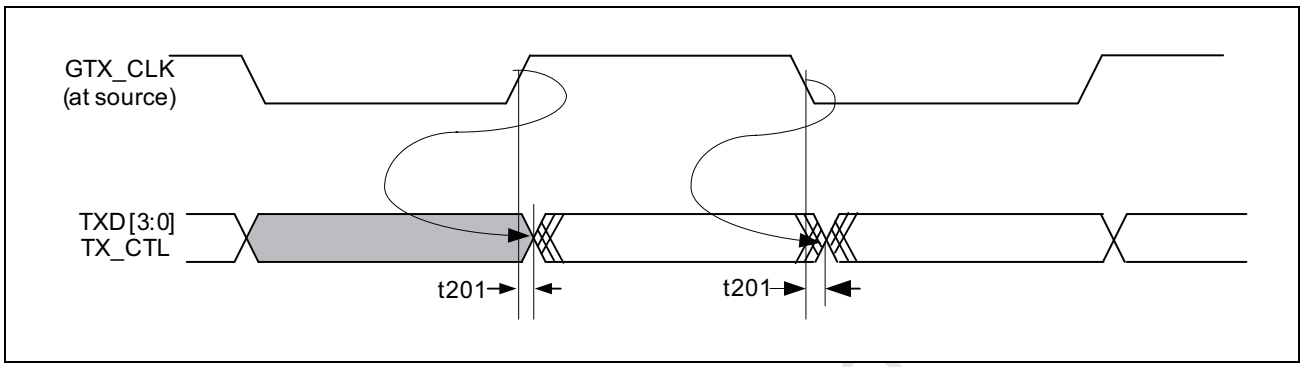


Figure 55: RGMII Output Timing (Normal Mode)

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 275: RGMII Output Timing (Normal Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TskewT: data to clock output skew	t201	–500 (1000M)	0	+500 (1000M)	ps
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

Note: The output timing in 10/100M operation is always as specified in the delayed mode.

RGMII Output Timing (Delayed Mode)

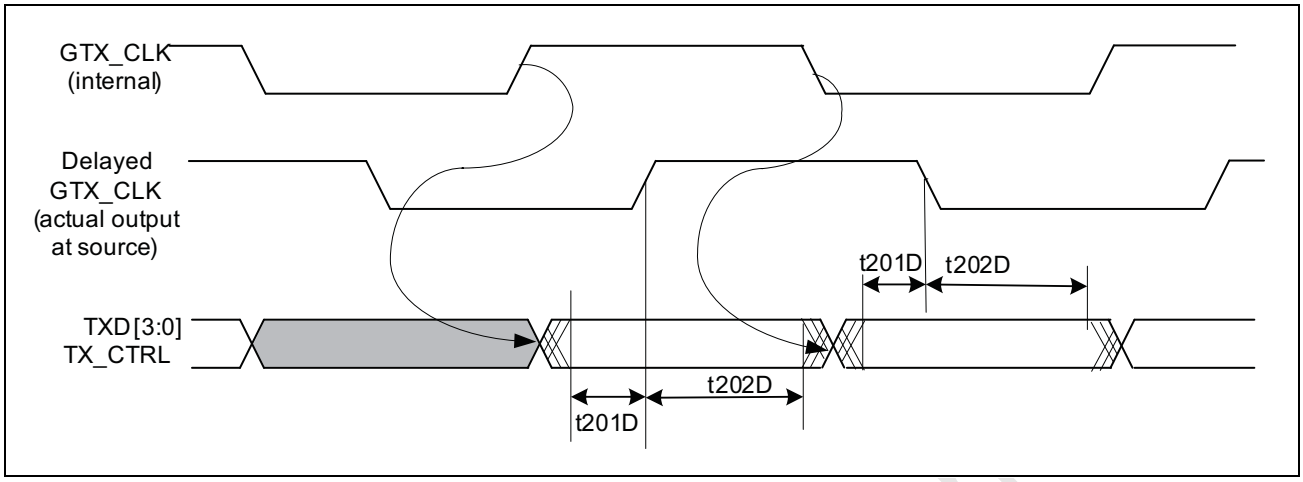


Figure 56: RGMII Output Timing (Delayed Mode)

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.+

Table 276: RGMII Output Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TsetupT Data valid to clock transition: Available setup time at the output source (delayed mode)	t201D	1.2 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (delayed mode)	t202D	1.2	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Normal Mode)

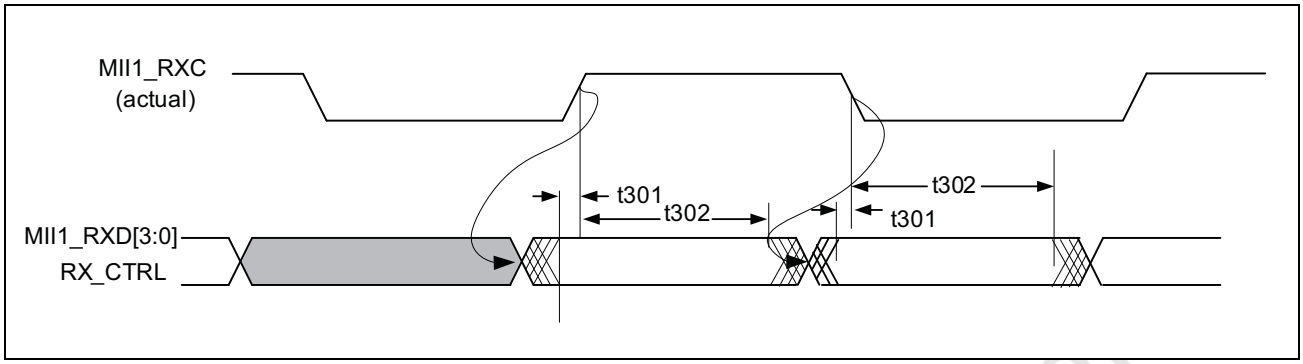


Figure 57: RGMII Input Timing (Normal Mode)

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 277: RGMII Input Timing (Normal Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
MII1_RXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_RXC clock period (100M mode)	–	36	40	44	ns
MII1_RXC clock period (10M mode)	–	360	400	440	ns
TsetupR Input setup time: valid data to clock	t301	1.0	2.0	–	ns
TholdR Input hold time: clock to valid data	t302	1.0	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Delayed Mode)

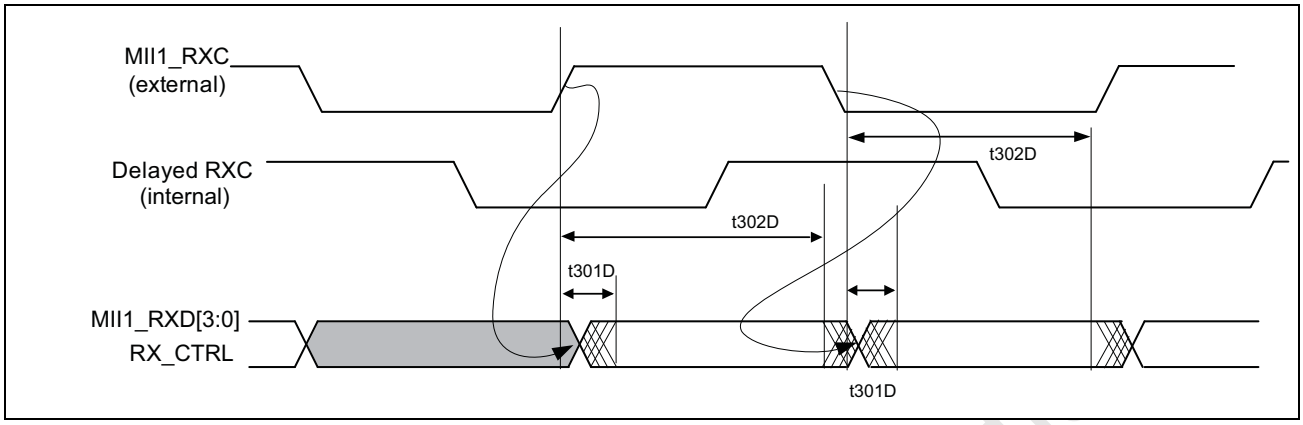


Figure 58: RGMII Input Timing (Delayed Mode)

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 278: RGMII Input Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
TsetupR Input setup time (delayed mode)	t301D	–1.0 (1000M)	–	–	ns
		–1.0 (10/100M)	–	–	ns
TholdR Input hold time (delayed mode)	t302D	3.0 (1000M)	–	–	ns
		9.0 (10/100M)	–	–	ns

MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.

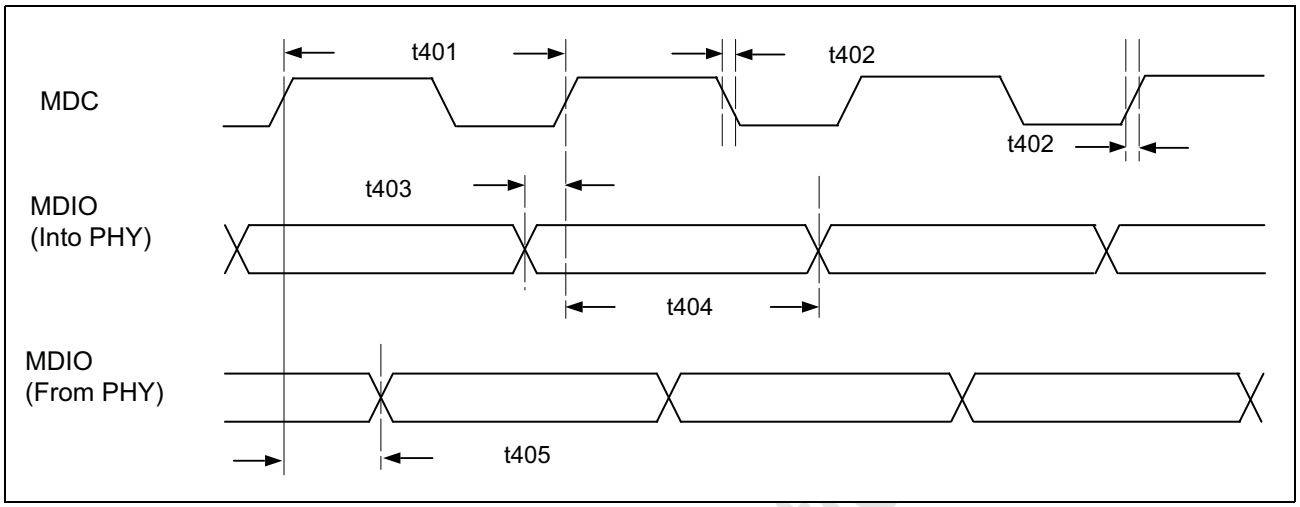


Figure 59: MDC/MDIO Timing (Slave Mode)

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 279: MDC/MDIO Timing (Slave Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
MDC cycle time	t401	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	7.5	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC rising	t405	0	–	45	ns

Table 280: MDC/MDIO Timing (Master Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
MDC cycle time	t401	400	–	–	ns
MDC high/low	–	160	–	240	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	80	–	–	ns

Table 280: MDC/MDIO Timing (Master Mode) (Cont.)

Description	Parameter	Minimum	Typical	Maximum	Units
MDIO input hold time from MDC rising	t404	0	–	–	ns
MDIO output delay from MDC rising	t405	15	–	90	ns

Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

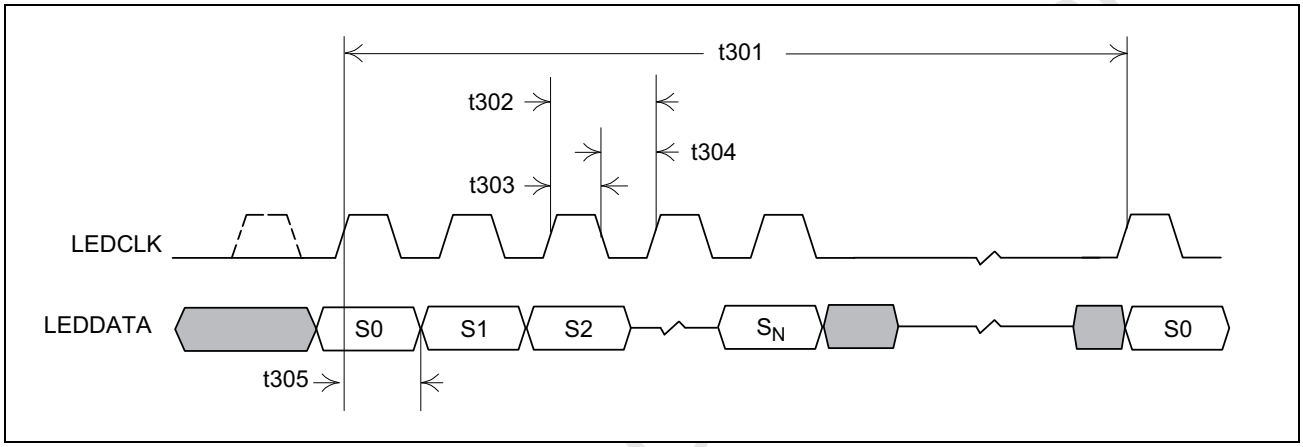


Figure 60: Serial LED Interface Timing

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 281: Serial LED Interface Timing

Description	Parameter	Minimum	Typical	Maximum	Units
LED update cycle period	t301	–	42	–	ms
LEDCLK period	t302	–	320	–	ns
LEDCLK high-pulse width	t303	150	–	170	ns
LEDCLK low-pulse width	t304	150	–	170	ns
LEDCLK to LEDDATA output time	t305	140	–	180	ns

SPI Timings

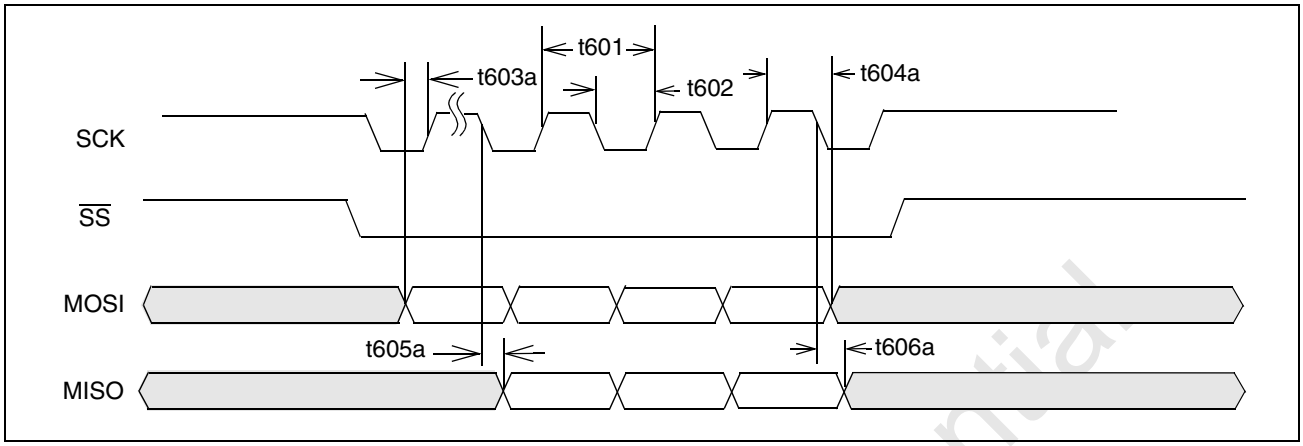


Figure 61: SPI Timings, SS Asserted During SCK High

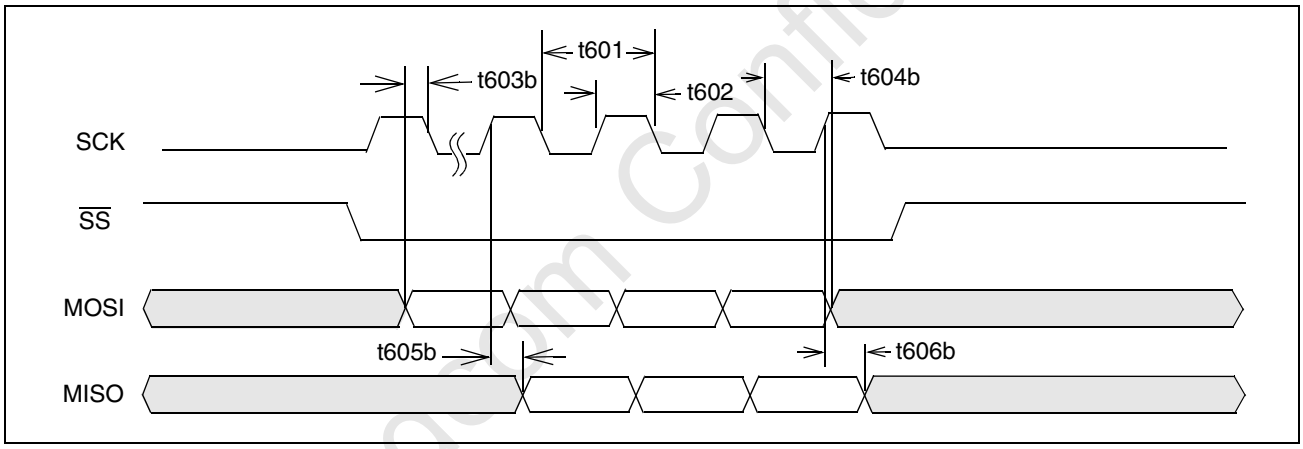


Figure 62: SPI Timings, SS Asserted During SCK Low

Note: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 282: SPI Timings

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
SCK clock period	t601	80 ns	500 ns	–
SCK high/low time	t602	40 ns	–	–
MOSI to SCK setup time	t603a, t603b	5 ns	–	–
MOSI to SCK hold time	t604a, t604b	5 ns	–	–

Table 282: SPI Timings (Cont.)

Description	Parameter	Minimum	Typical	Maximum
SCK to MISO valid	t605a, t605b	–	–	10 ns
SCK to MISO invalid	t606a, t606b	0 ns	–	–

Note: The BCM53101M behaves only as a slave device. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the BCM53101M samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM53101M samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM Timing

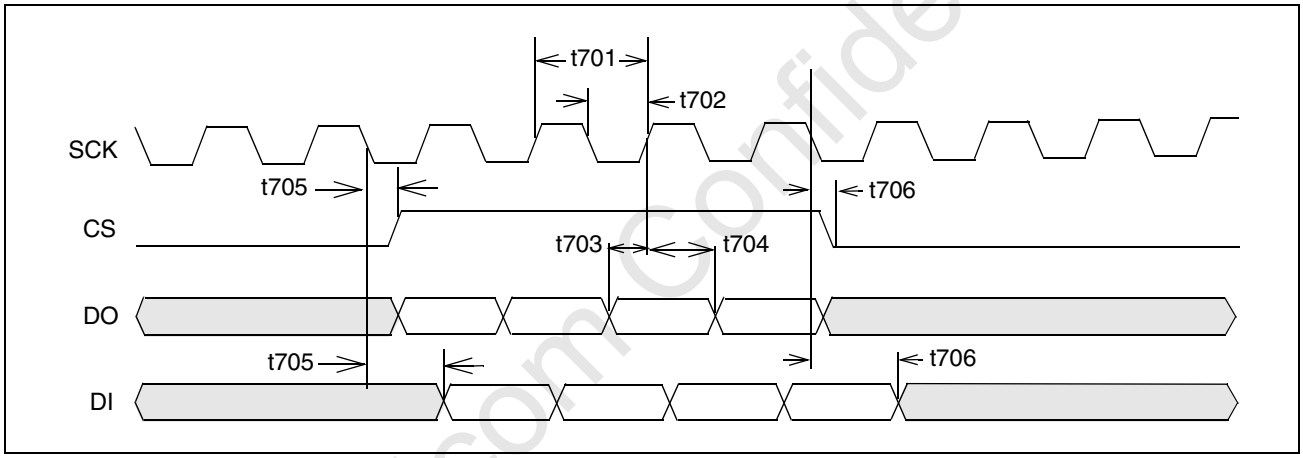


Figure 63: EEPROM Timing

Table 283: EEPROM Timing

Description	Parameter	Minimum	Typical	Maximum
SCK clock frequency	t701	–	200 kHz	–
SCK high/low time	t702	–	2.5 µs	–
DO to SCK rising setup time	t703	50 ns	–	–
DO to SCK rising hold time	t704	10 ns	–	–
SCK low to CS, DI valid time	t705	30 ns	–	100 ns
SCK low to CS, DI invalid time	t706	30 ns	–	–

Section 11: Thermal Characteristics

Table 284 shows the 132 DRQFN thermal characteristics at 70°C.

Table 284: 132 DRQFN Thermal Characteristics at 70°C No Heatsink

Air Flow (LFPM)	0	100	200	400	600
Theta-$_{JA}$ (°C/W)	20.75	17.42	16.27	15.16	14.62
Theta-$_{JB}$ (°C/W)	2.13	–	–	–	–
Theta-$_{JC}$ (°C/W)	20.54	–	–	–	–
Maximum Junction Temperature T_J	94.9	90.9	89.5	88.2	87.5

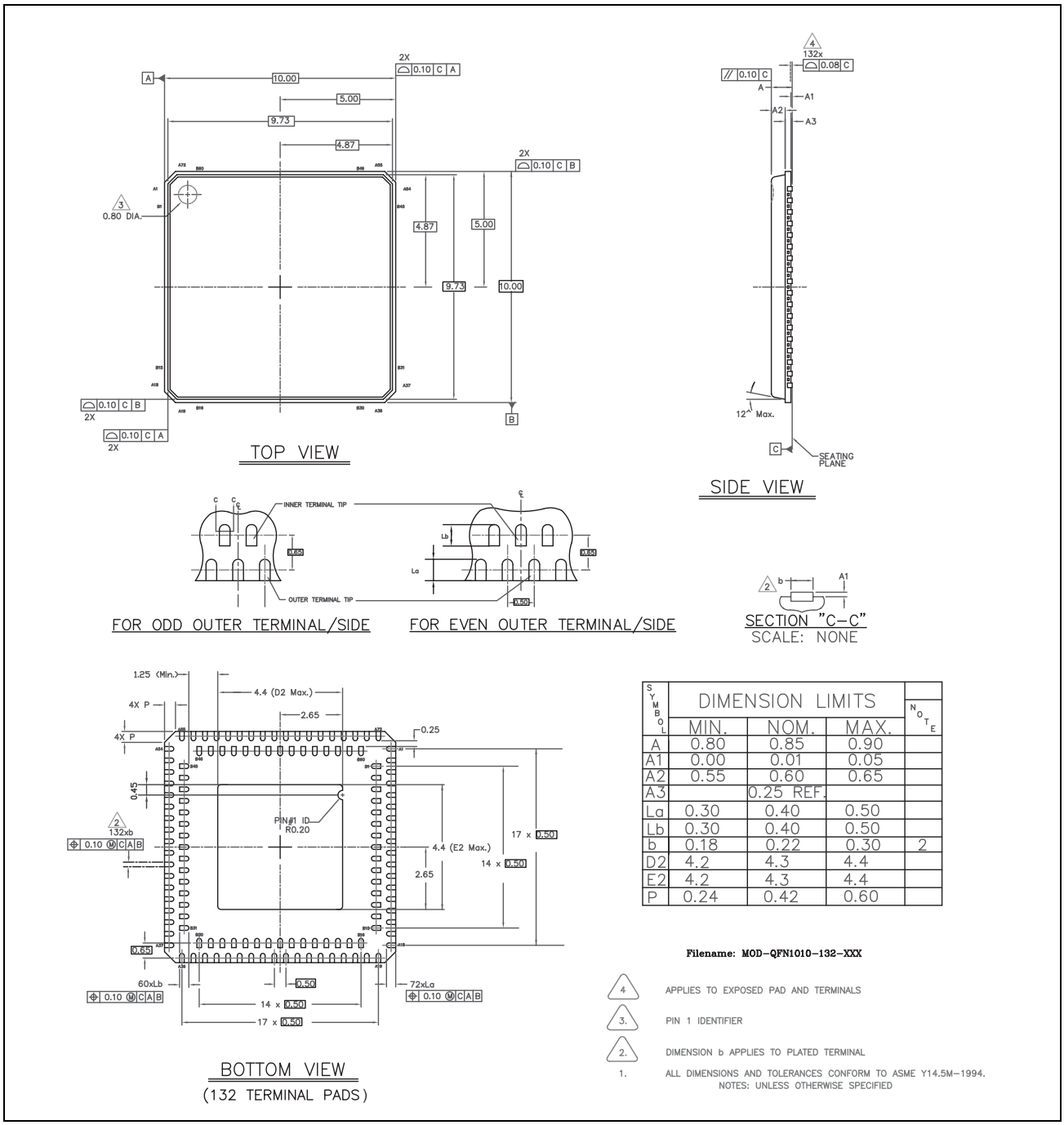
Table 285 shows the 132 DRQFN thermal characteristics at 85°C.

Table 285: 132 DRQFN Thermal Characteristics at 85°C No Heatsink

Air Flow (LFPM)	0	100	200	400	600
Theta-$_{JA}$ (°C/W)	20.75	17.42	16.27	15.16	14.62
Theta-$_{JB}$ (°C/W)	2.13	–	–	–	–
Theta-$_{JC}$ (°C/W)	20.54	–	–	–	–
Maximum Junction Temperature T_J	109.9	105.9	104.5	103.2	102.5

Section 12: Mechanical Drawing

Figure 64 shows the BCM53101M mechanical drawing. The device is housed in a dual-row MLF, 132 lead, 10 mm x 10 mm body (etched), 0.50 mm/0.65 mm lead-pitch interstitial type, with punch singulation.



SYMBOL	DIMENSION LIMITS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	
A2	0.55	0.60	0.65	
A3		0.25 REF.		
La	0.30	0.40	0.50	
Lb	0.30	0.40	0.50	
b	0.18	0.22	0.30	2
D2	4.2	4.3	4.4	
E2	4.2	4.3	4.4	
P	0.24	0.42	0.60	

Figure 64: BCM53101M Mechanical Drawing

Section 13: Ordering Information

Table 286: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM53101MKMLG	132-pin DRQFN (10 mm x 10 mm) lead-free	0° C to 70° C
BCM53101MIMLG	132-pin DRQFN (10 mm x 10 mm) lead-free	–40°C to 85°C

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