Multiport Gigabit Ethernet Switches

GENERAL DESCRIPTION

The Broadcom® BCM53118 is a highly integrated, cost-effective unmanaged-smart gigabit switch. The switch design is based on the field-proven, industry-leading ROBO architecture. This device combines all the functions of a high-speed switch system including packet buffers, PHY transceivers, media access controllers (MACs), address management, port-based rate control, and a non-blocking switch fabric into a single 65 nm CMOS device. Designed to be fully compliant with the IEEE 802.3™ and IEEE 802.3x specifications, including the MAC-control PAUSE frame, the BCM53118 provides compatibility with all industry-standard Ethernet, Fast Ethernet, and Gigabit Ethernet (GbE) devices.

The BCM53118 has a rich feature set suitable for not only standard GbE connectivity for desktop and laptop PCs, but also for next-generation gaming consoles, set-top boxes, networked DVD players, and home theater receivers. It is also specifically designed for next generation SOHO/SMB routers and gateways.

The BCM53118 contains eight full-duplex 10/100/1000BASE-TX Ethernet transceivers. In addition, the BCM53118 has one GMII/RGMII/MII/RvMII/TMII interface for the CPU or a router chip, providing flexible 10/100/1000-Mbps connectivity.

The BCM53118 provides 70+ on-chip MIB counters to collect receive and transmit statistics for each port.

The BCM53118 is available in commercial temperature (C-Temp) rated packages. The commercial-grade BCM53118 is provided in a 256-pin eLQFP (28 mm × 28 mm) package.

FEATURES

- Nine 10/100/1000 media access controllers
- Eight port 10/100/1000BASE-T/TX transceivers
- One GMII/RGMII/MII/RvMII/TMII interface for an in-band management port (IMP) for connection to a CPU/management entity without PHY
- IEEE 802.1p, MAC, Port, TOS, and DiffServ QoS for four queues, plus two time sensitive queues
- Port-based VLAN
- IEEE 802.1Q-based VLAN with 4K entries
- MAC-based trunking with automatic link failover
- Port-based rate control
- Port mirroring
- BroadSync™ HD
  - Timestamp tagging at MAC interface
  - Time-aware egress scheduler
- DOS attack prevention
  - Support IPv6
- IGMP snooping, MLD snooping support
- Green mode support
- Spanning tree support (multiple spanning trees–up to eight)
- Loop detection for unmanaged configurations with Broadcom's patented LoopDTech™ technology
- CableChecker™ with unmanaged mode support
- Double tagging/QinQ
- IEEE 802.3as support
- IEEE 802.3x programmable per-port flow control and backpressure, with IEEE 802.1x support for secure user authentication
- EEPROM, MDC/MDIO, and SPI Interfaces
- 4K entry MAC address table with automatic learning and aging
- 192 KB packet buffer
- 256 multicast group support
- Jumbo frame support up to 9720 bytes
- Serial and parallel LED interface
- 1.2V for core and 3.3V for I/O
- JTAG support
- 256 eLQFP

53118-DS07-R

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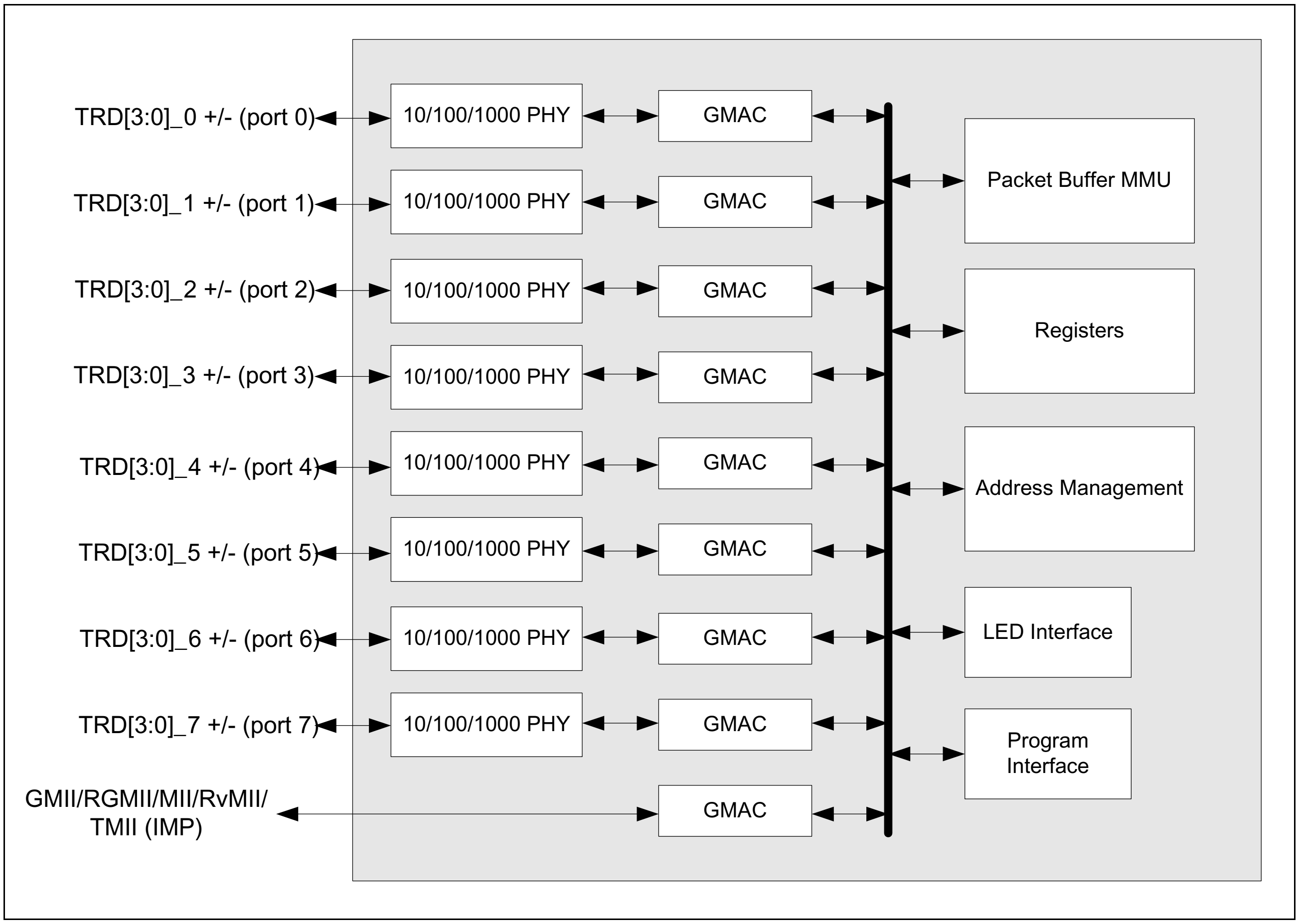
Figure 1: Functional Block Diagram



Revision History

Revision	*Date*	*Change Description*
53118-DS07-R	08/27/13	**Updated:** Bit default values in the following tables: • Table 120: “MII Control Register (Page 10h–17h: Address 00h–01h),” on page 187 • Table 124: “Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h–09h),” on page 190 • Table 129: “1000BASE-T Control Register (Page 10h–17h: Address 12h–13h),” on page 195
53118-DS06-R	10/03/11	**Updated:** • “MIB Counters Per Port” on page 80 • Table 164: “Page 20h–28h Port MIB Registers,” on page 220 • Table 266: “Absolute Maximum Ratings,” on page 277 • Table 268: “Electrical Characteristics,” on page 278 • Table 269: “Reset and Clock Timing,” on page 279
53118-DS05-R	8/6/09	**Updated:** • Table 82: “Aging Time Control Register (Page 02h: Address 06h–09h),” on page 162.
53118-DS04-R	12/4/09	**Updated:** • Figure 1, “Functional Block Diagram,” on page ii. • “Overview” on page 1. • “Frame Management Port Interface” on page 60. • Table 269, “Reset and Clock Timing,” on page 247. **Added:** • “TMII Interface Timing” on page 250.

Revision	***Date***	***Change Description***
53118-DS03-R	5/6/09	**Updated:** • Changed “Ethernet AV” to “BroadSync HD” throughout. • “Double-Tagging” on page 11 • “Green Mode” on page 22. • Table 5, “Cable Diagnostic Output,” on page 26. • “Integrated High-Performance Memory” on page 57. • Table 30, “Signal Type Definitions,” on page 93. • Table 62, “Port State Override Register (Page 00h: Address 58h–5Fh),” on page 122. • Table 83, “Mirror Capture Control Register (Page 02h: Address 10h–11h),” on page 131. • Table 213, “Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h),” on page 224. • Table 245, “BroadSync HD Max Packet Size Register (Page 90h: Address 04h),” on page 237. • Table 256, “BroadSync HD Egress Time Stamp Status Register (Page 90h: Address D0h),” on page 241. • Table 269, “Reset and Clock Timing,” on page 247. • Table 278, “GMII Output Timing,” on page 256. **Added:** • “Serial Flash Timing” on page 262. • Figure 65, “Serial FlashTiming,” on page 262. • Table 285, “Serial FlashTiming,” on page 262. • Table 286, “BCM53118KQLE Package with Heat Sink, 4-Layer Board, P = 3.8W,” on page 263. • Table 287, “BCM53118KQLE Package with Heat Sink, 2-Layer Board, P = 3.8W,” on page 263. **Removed:** • Table 286, “BCM53118KQLE Package–With Heat Sink,” on page 263.

Revision	*Date*	*Change Description*
53118-DS02-R	4/7/08	**Updated:** • “MSTP Multiple Spanning Tree” on page 22. • Table 30, “Signal Type Definitions,” on page 93. • Table 70, “Link Status Summary Register (Page 01h: Address 00h–01h),” on page 125. • Table 77, “Last Source Address (Page 01h: Address 10h–45h),” on page 128. • Table 189, “Global VLAN Control 1 Register (Page 34h: Address 01h),” on page 207. • Table 190, “Global VLAN Control 2 Register (Page 34h: Address 02h),” on page 208. • Table 226, “MSPT Aging Control Registers (Page 43h: Address 02h–05h),” on page 230. • Section 12 “Ordering Information” on page 265. **Added:** • “BCM53118KQLE Pin List by Signal Name” on page 103. • “BCM53118KQLE Pin List by Ball Name” on page 105. • Figure 66, “BCM53118 Mechanical Specifications,” on page 264.
53118-DS01-R	1/23/08	**Updated:** • Figure 2, “QoS Program Flow,” on page 4 • “CableChecker™” on page 26 • Figure 9, “Address Table Organization,” on page 28 • “Integrated 10/100/1000 PHY” on page 38 • “PHY Address” on page 43 • Table 18, “Egress Broadcom Tag Format (IMP to CPU),” on page 48 • “LED Interfaces” on page 86 • Table 27, “LED Output Pins Per Port,” on page 87 • Figure 45, “LED Interface Register Structure Diagram,” on page 88 • Figure 46, “LED Interface Block Diagram,” on page 89 • Table 266, “Absolute Maximum Ratings,” on page 245 • Table 267, “Recommended Operating Conditions,” on page 245 **Added:** • Table 28, “Dual Input Configuration/LED Outputs,” on page 90 • “Dual Input Configuration/LED Output Function” on page 90 • Table 30, “Signal Type Definitions,” on page 93 • Section 7 “Register Definitions” on page 107 • Section 8 “Electrical Characteristics” on page 245 • Section 9 “Timing Characteristics” on page 247 • Section 10 “Thermal Characteristics” on page 262 • Section 11 “Mechanical Information” on page 263 • Section 12 “Ordering Information” on page 264
53118-DS00-R	10/25/07	Initial release.

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM53118 gigabit switch device. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Technical Support

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In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

The BCM53118 is a single-chip, 9-port Gigabit Ethernet (GbE) switch device. It provides:

- A 9-port non-blocking 10/100/1000 Mbps switch controller
- Eight ports with 10/100/1000BASE-TX-compatible transceivers
- Nine integrated Gigabit MACs (GMACs)
- One GMII/RGMII/MII/RvMII/TMII port for PHY-less connection to the management agent
- An integrated Motorola® SPI-compatible interface
- High performance, integrated packet buffer memory
- An address resolution engine
- A set of management information base (MIB) statistics registers

The GMACs support full-duplex and half-duplex modes for 10 Mbps and 100 Mbps and full-duplex for 1000 Mbps. Flow control is supported in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is supported. The GMACs are IEEE 802.3-compliant and support maximum frame sizes of 9720 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 4K unicast addresses. Addresses are added to the table after receiving an error-free packet.

The MIB statistics registers collect receive and transmit statistics for each port and provide direct hardware support for the Ether-like MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface Port by an external microcontroller.

Audience

This document is for designers interested in integrating the BCM53118 switches into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM53118 switches.

Data Sheet Information

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active low (such as $\overline{\text{CE}}$).
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m (such as [7:0] indicates bits 7 through 0, inclusive).
- The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage (for example, 1 KB means 1,024 bytes, 100 Mbps [referring to fast Ethernet speed] means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).

Section 2: Features and Operation

Overview

The BCM53118 switches include the following features:

- "Quality of Service" on page 34
- "Port-Based VLAN" on page 38
- "IEEE 802.1Q VLAN" on page 39
- "Double-Tagging" on page 40
- "Jumbo Frame Support" on page 43
- "Port Trunking/Aggregation" on page 43
- "WAN Port" on page 44
- "Rate Control" on page 44
- "Protected Ports" on page 47
- "Port Mirroring" on page 47
- "IGMP Snooping" on page 49
- "MLD Snooping" on page 49
- "IEEE 802.1x Port-Based Security" on page 49
- "DoS Attack Prevention" on page 50
- "MSTP Multiple Spanning Tree" on page 51
- "Software Reset" on page 51
- "Loop Detection" on page 51
- "Green Mode" on page 52
- "BroadSync HD" on page 52
- "CableChecker™" on page 56
- "Egress PCP Remarking" on page 57
- "Address Management" on page 57

The following sections discuss each feature in more detail.

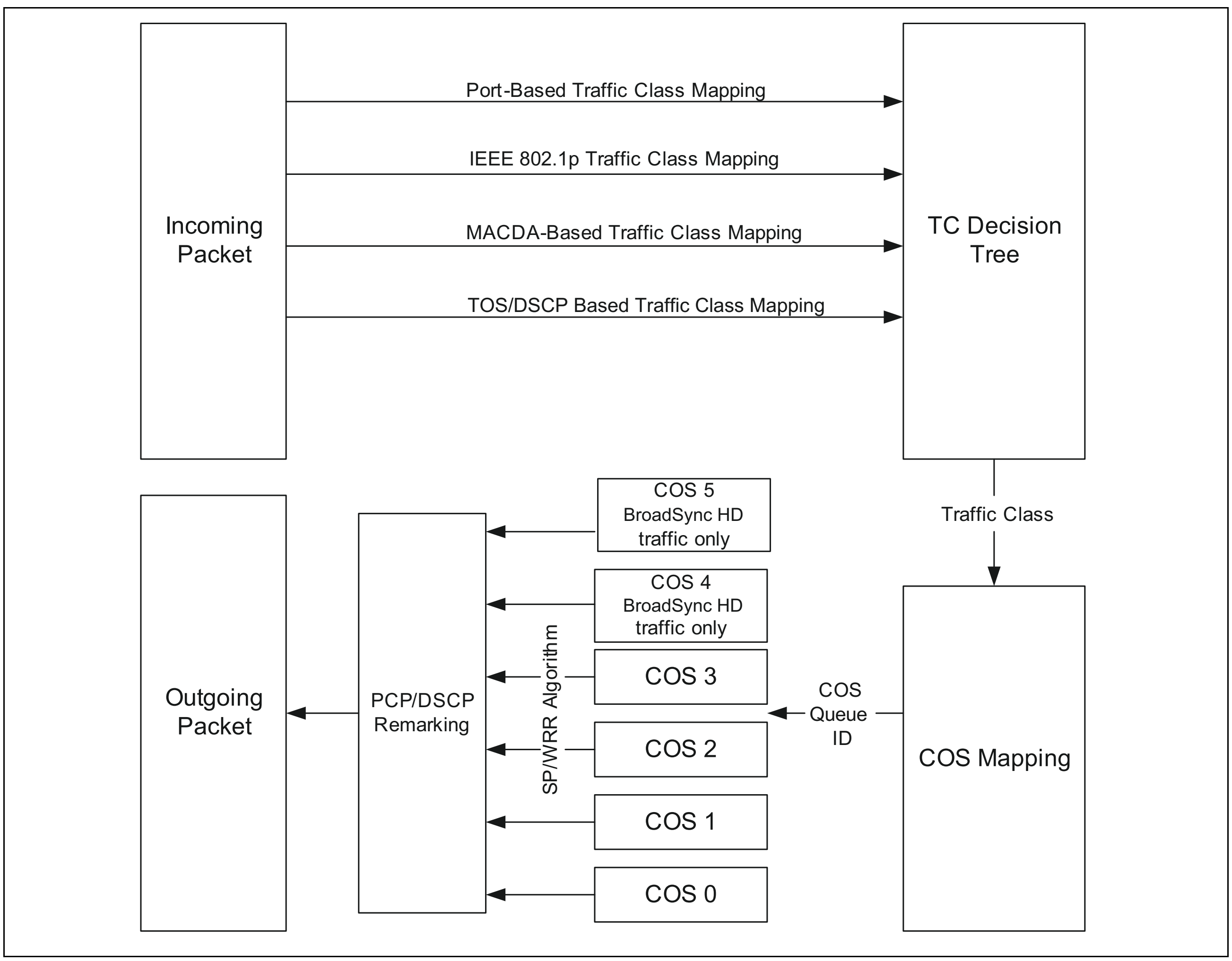
Quality of Service

The Quality of Service (QoS) feature provides up to six internal queues per port to support six different traffic classes (TC). The traffic classes can be programmed so that higher-priority TC in the switch experiences less delay than lower-priority TC under congested conditions. This can be important in minimizing latency for delay-sensitive traffic. The BCM53118 switches can assign the packet to one of the six egress transmit queues according to information in:

- "Port-Based QoS" on page 35 (ingress port ID)
- "IEEE 802.1p QoS" on page 35
- "MACDA-Based QoS" on page 36
- "TOS/DSCP QoS" on page 36

The "TC Decision Tree" on page 36 decides which priority system is used based on three programmable register bits detailed in Table 1: "TC Decision Tree Summary," on page 36. The corresponding traffic class is then assigned to one of the six queues on a port-by-port basis.

Figure 2: QoS Program Flow



Egress Transmit Queues

Each Ethernet egress port has six transmit queues (COS0−COS5). The COS4 and COS5 are dedicated to BroadSync HD traffic only and can not be shared with other traffic. Each COS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. Every Ethernet (ingress) port has its own set of counters to measure the buffer occupancy and the arrival rate related to the traffic received from the port.

The IMP (egress) port serves four queues (COS0–COS3) and the traffic generated by the Local Management Packet Generator which generate management report messages back to CPU, e.g., the Time Sync TX time stamp packets.

Each COS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. The IMP (ingress) port also has its own set of counters to measure the buffer occupancy and the arrival rated to the traffic received from the port, but should be used only if it is configured as a regular Ethernet port.

All incoming frames are assigned to an egress transmit queue depending on their assigned TC. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher TC queues being given greater access than the lower TC queues. Queue 0 is the lowest-TC queue.

The COS0−COS3 queues are dedicated to non-BroadSync HD traffic only and as programmed in the "TX Queue Control Register (Page 30h: Address 80h)" on page 233. The BCM53118 uses strict priority (SP) and weighted round robin (WRR) algorithm for COS0−COS3 queues scheduling. The scheduling is configurable via the "TX Queue Control Register (Page 30h: Address 80h)", as one of following combinations of SP and WRR; 4SP, 4WRR, 1SP and 3WRR, 2SP and 2WRR The WRR algorithm weights for each queue can be programmed via the "TX Queue Weight Register (Page 30h: Address 81h)" on page 233.

Port-Based QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with the TC configured for the corresponding port. The mapping mechanism is globally enabled/disabled via programming the "QoS Global Control Register (Page 30h: Address 00h)" on page 226, the mapping entry is also per-port configured via "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244. When disabled, the TC that results from this mapping is 000.

IEEE 802.1p QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC-configured for the corresponding IEEE 802.1p priority code point (PCP). The mapping mechanism is per port enabled/disabled via "QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)" on page 227, the mapping entries are per-port configured by "Port N (N = 0-7, 8) PCP_To_TC Register (Page 30h: Address 10h)" on page 228. When disabled or if the incoming packet is not tagged, the TC that results from this mapping is 000.

MACDA-Based QoS

MACDA-Based QoS is enabled when the IEEE 802.1p QoS is disabled via the 802_1P_EN bit in the "QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)" on page 227. When using MACDA-based QoS, the destination address and VLAN ID is used to index the ARL table as described in "Address Management" on page 57. The matching ARL entry contains a 3-bit TC field as shown in Table 7 on page 60. These bits set the MACDA-based TC for the frame. The MACDA-based TC is assigned to the TC bits depending upon the result shown in Table 1 on page 36. The TC for the frame is mapped to one of the egress transmit queues base on the ingress port via the TC_To_COS Mapping register. The TC bits for a learned ARL entry default to 0. To change the default, an ARL entry is written to the ARL table as described in the "Writing an ARL Entry" on page 64. For more information about the egress transmit queues, see "Egress Transmit Queues" on page 35.

TOS/DSCP QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC configured for the corresponding IP TOS/DSCP. The mapping mechanism is per port enabled/disabled via "QoS DiffServ Enable Register (Page 30h: Address 06h)" on page 227, the mapping entries are globally configured by "DiffServ Priority Map 0 Register (Page 30h: Address 40h)" on page 229 through "DiffServ Priority Map 3 Register (Page 30h: Address 52h)" on page 231. When disabled or the incoming packet is not of IPv4/v6 type, the TC resulted from this mapping is 000.

TC Decision Tree

Non-BroadSync HD Frame

The TC decision tree determines which priority system is assigned to TC-mapping bits for the given frame. As summarized above, the TC bits for the frame can be determined according to the ingress port-based TC, IEEE 802.1p TC, MACDA-based TC, DiffServ TC or MACSA-based TC information. The decision on which TC mapping to use is based on the Port_QoS_En bit and the QoS_Layer_Sel bits of the "QoS Global Control Register (Page 30h: Address 00h)" on page 226. Table 1 summarizes how these programmable bits affect the derived TC. The DiffServ and IEEE 802.1p QoS TC are only available if the respective QoS is enabled, and the received packet has the appropriate tagging.

Table 1: TC Decision Tree Summary

Port_QoS_En	*QoS_Layer_Sel*	*Value of TC Bits*
0	00	IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.
0	01	DiffServ TC mapping if available; otherwise, TC = 000.
0	10	DiffServ TC mapping for IP frame; otherwise, IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.
0	11	The highest available TC of the following: IEEE 802.1p TC mapping, DiffServ TC mapping, MACDA-based TC mapping or MACSA-based TC mapping.
1	00	MACSA-based TC mapping if available; otherwise, Port-based TC mapping.
1	01	MACSA-based TC mapping if available; otherwise, Port-based TC mapping.
1	10	MACSA-based TC mapping if available; otherwise, Port-based TC mapping.

Table 1: TC Decision Tree Summary (Cont.)

Port_QoS_En	QoS_Layer_Sel	Value of TC Bits
1	11	The highest available TC of the following: Port-based TC mapping, MACSA-based TC mapping, IEEE 802.1p TC mapping, DiffServ TC mapping or MACDA-based TC mapping.

BroadSync HD Frame

For the BroadSync HD packet from an Ethernet port, the TC is determined directly from the explicit IEEE 802.1Q/P tag carried in the BroadSync HD packets (BroadSync HD packets are expected to always be tagged), which is independent of Table 1 TC mapping.

The conditions deciding whether an incoming packet is BroadSync HD are:

1. The port from which the packet is received is configured as BroadSync HD-enabled.
2. The packet received is either VLAN tagged or priority tagged, with PCP = 4 or 5.
3. The MACDA is of multicast type and can be found through ARL table search.

Note: BroadSync HD cannot be received from the IMP port.

Queuing Class (COS) Determination

The BCM53118 supports the COS mapping through the mapping mechanisms listed below.

- TC to COS mapping: The queuing class to forward a packet to an Ethernet port is mapped from the TC determined for the packet. The mapping entries are globally configured via “TC_To_COS Mapping Register (Page 30h: Address 62h–63h)” on page 231.
- BroadSync HD to COS mapping: The queuing class to forward a BroadSync HD packet to a BroadSync HD-enabled Ethernet port is mapped from the PCP carried by the packet. PCP5 is mapped to COS5 and PCP4 is mapped to COS4.
- CPU to COS mapping: The queuing class to forward a packet to the external CPU through the IMP port is determined based on the reasons to forward (copy or trap) the packet to CPU. The mapping entries are globally configured via “CPU_To_COS Map Register (Page 30h: Address 64h–67h)” on page 232.

Note: When the BCM53118 is configured in the aggregation mode where the IMP operates as the uplink port to the upstream network processor, the COS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU, and the COS is decided based on the reasons for forwarding the packet to the CPU.

Table 2 shows the reasons for forwarding a packet to the CPU.

Table 2: Reasons to Forward a Packet to the CPU

ToCPU Reason	Description	ToCPU COS
Mirroring	The packet is forwarded (copied) through the IMP port because it needs to be mirrored to the CPU as the capturing device.	0
SA Learning	The packet is forwarded (copied) through the IMP port because its SA needs to be learned by the CPU.	0
Switching /Flooding	The packet is forwarded through the IMP port either because the CPU is one of the intended destination hosts of the packet or because the switch makes the flooding decision to reach all potential destinations.	0
Protocol Termination	The packet is forwarded (trapped) through the IMP port because it implies an IEEE 802.1 defined L2 protocol that needs to be terminated by the CPU.	0
Protocol Snooping	The packet is forwarded (copied) through the IMP port because it implies an L3 or application level protocol that needs to be monitored by the CPU for network security or operation efficiency.	0
Exception Processing	The packet is forwarded (trapped) through the IMP port for some special processing even though the CPU is not the intended destination.	0

The ToCPU COS values listed in Table 2 are the default setting and are configurable. In order to prevent out of order delivery of the same packet flow to the CPU, the COS for the mirroring and SA learning reasons must be programmed with a value that is lower than or equal to the value of the other reasons.

A packet could be forwarded to the CPU for more than one reason, therefore the COS selection is based on the highest COS values among all the reasons for the packet.

Port-Based VLAN

The port-based virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM53118 provide flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to non-private domain ports. The private domain ports are selected for each ingress port via "Port-Based VLAN Control Register (Page 31h: Address 00h)" on page 235. For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame will be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the non-private domain ports. The frame is only forwarded to those ports that meet the ARL table criteria, as well as the port-based VLAN criteria.

IEEE 802.1Q VLAN

The BCM53118 support IEEE 802.1Q VLAN and up to approximately 4000 VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM53118 autonomously handle all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups.

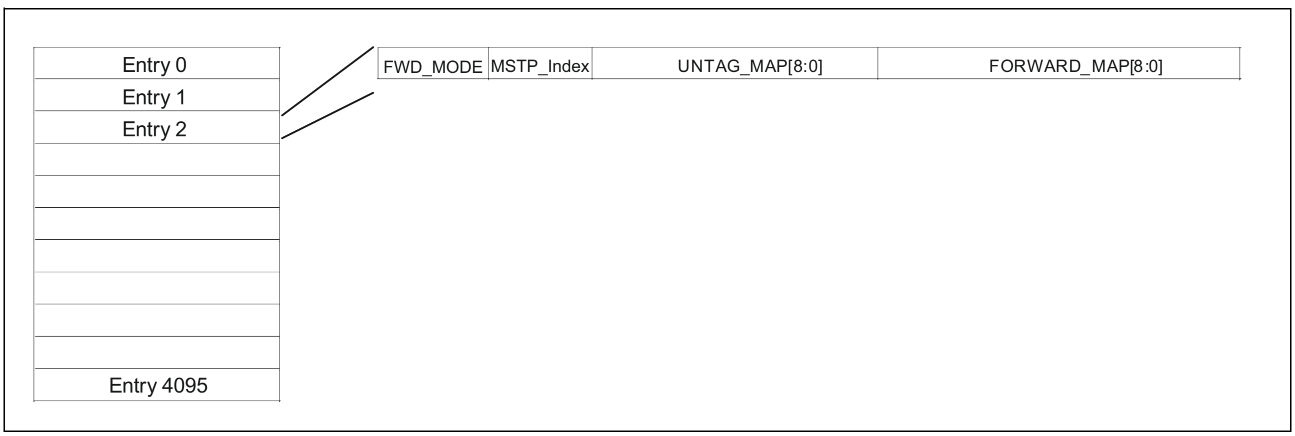
IEEE 802.1Q VLAN Table Organization

Each VLAN table entry, also referred to as a VLAN ID, an Untag map, and a Forward map.

- The Untag map controls whether the egress packet is tagged or untagged.
- The Forward map defines the membership within a VLAN domain.
- The FWD_MODE indicates whether the packet forwarding should be based on VLAN membership or based on ARL flow.

The Untag map and Forward map include bit-wise representation of all the ports.

Figure 3: VLAN Table Organization



Note: When the IEEE 802.1Q feature is enabled, frames sent via the CPU must be tagged. If the MII port is configured as a management port, then the tag is not stripped even if the untag bit is set.

Programming the VLAN Table

The IEEE 802.1Q VLAN feature can be enabled by writing to the Enable IEEE 802.1Q bit in the "Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 238. The default priority and VID can be assigned to each port in the "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244. These are necessary when tagging a previously untagged frame. The Hashing algorithm uses either [VID, MAC] or [MAC] for the ARL index key, depending on the VLAN Learning Mode bits in the "Global IEEE 802.1Q Register (Pages 34h: Address 00h)". If both the VID and MAC address are used, a single MAC address is able to be a member of multiple VLANs simultaneously.

The VLAN table can be written using the following steps:

1. Use the "VLAN Table Entry Register (Page 05h: Address 83h–86h)" on page 183 to define the ports that are part of the VLAN group and the ports that should be untagged.
2. Use the "VLAN Table Address Index Register (Page 05h: Address 81h)" on page 183 to define the VLAN ID of the VLAN group.

Note: VLAN ID 0xFFF is reserved. However VID = 0xFFF can be forwarded if the VID_FFF_Fwding bit is set in the "Global VLAN Control 5 Register (Page 34h: Address 06h)" on page 242.

3. Set bit [1:0] = 00 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" on page 182 to indicate a write operation.
4. Set bit 7 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" to 1, starting the write operation. This bit returns to 0 when the write is complete.

The VLAN table can be read using the following steps:

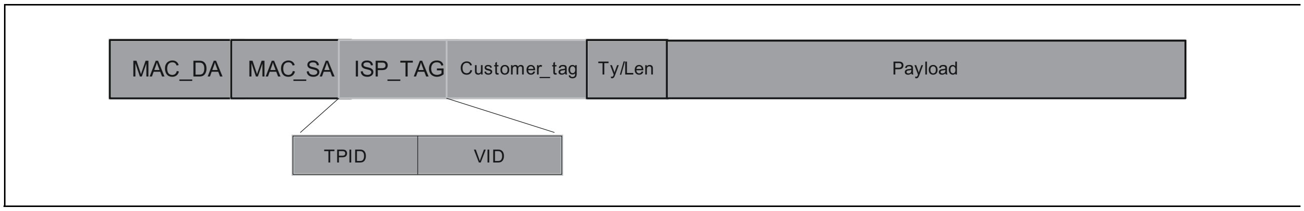
1. Use the "VLAN Table Address Index Register (Page 05h: Address 81h)" to define from which VLAN group to read the data.
2. Set bit [1:0] = 01 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" to indicate a read operation.
3. Set bit 7 of the "VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" to 1 to start the read operation. This bit returns to 0 when the read is complete.
4. Read the "VLAN Table Entry Register (Page 05h: Address 83h–86h)" to obtain the VLAN table entry information.

Double-Tagging

The BCM53118 provide the double tagging feature, which is useful for ISP applications. When the ISP aggregates incoming traffic from each individual customer, the extra tag (double tag) can provide an additional layer of tagging to the existing IEEE 802.1Q VLAN. The ISP tag (extra tag) is a way of separating individual customers from other customers. Using the IEEE 802.1Q VLAN tag, the individual customer's traffic can be separated.

When the double-tagging feature is enabled via the "Global VLAN Control 4 Register (Page 34h: Address 05h)" on page 241 and the Enable IEEE 802.1Q (bit7) of the "Global IEEE 802.1Q Register (Pages 34h: Address 00h)" on page 238, users can expect two VLAN tags in a frame: the tag close to MAC_SA is the ISP tag, and the one following is the customer tag as shown in Figure 4.

Figure 4: ISP Tag Diagram



The switch uses the ISP tag for ARL and VLAN table accesses and the customer tag as an IEEE 802.1Q tag. There is a per chip programmable register Double Tagging TPID register for ISP tag (default = 9100'h). All ISP tags will be qualified by this Tag Protocol ID (TPID) value.

When the double-tagging feature is enabled, all switch ports are separated into two groups, ISP ports and customer ports. The BCM53118 performs the normalization process for all ingress frames, whether from the ISP port or customer port. The normalization process is to insert an ISP tag, customer tag, or ISP + customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with a double tag. But if the ingress frames are with a double tag (ISP + customer tag), and the ISP tag TPID matches the TPID specified in the Double Tagging TPID register, it does not perform the normalization process. The ISP ports are defined in the ISP Port Selection Portmap register. When the port (s) corresponding bit(s) are set, that port (s) should be connected ISP, and otherwise connected to customers. Each switch device can have multiple ports assigned as ISP ports, and each ISP is uniquely identified using different VLAN forward maps or the port-based VLAN feature.

If the ingress frame is an untagged frame, the IEEE 802.1Q tag which can be configured by the Default IEEE 802.1Q Tag Register (Page 34h: Address 10h) will add to an incoming untagged frame. If the ingress frame is tagged with the 802.1p tag, the default VID which can be configured by the Default IEEE 802.1Q Tag Register (Page 34h: Address 10h) will be tagged the incoming 802.1p frame.

ISP Port

It is possible for ISP port to receive three different types of frames: untagged, ISP-tagged, and ISP+Customer-tagged frames.

When the double-tagging feature is enabled and the received frame is untagged (or the TPID does not match with ISP TPID specified in Double Tagging TPID register, the default ISP tag and customer tag are added, and VLAN ID of ISP tag receives it from the port default VID. The frames are forwarded according to the VLAN table. However, if the Port-Based VLAN Control register is enabled, the egress ports specified in the port-VLAN control register override the VLAN table settings. If the received frame is ISP tagged (TPID matches with the ISP tag VLAN ID specified in the double-tagging TPID register), the default customer tag (8100 + default PVID) is added, the ISP VID is used to access the ARL table, and the ISP tag can be stripped on the way out according to the untagged bit setting in the VLAN table. In addition, ISP port frame can forward to the destination port directly based on forward port map of VLAN table by setting FWD_MODE bit to 1 of VLAN Table Entry register.

The VLAN ID is generated from the ISP tag, and TC is generated from the ingress frame outer tag.

Customer Port

It is also possible for Customer port to receive two different types of frames: untagged and Customer-tagged frames.

When the double-tagging feature is enabled, all the ingress frames preform the normalization process to insert a ISP tag or ISP + Customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with a double tag. The VLAN ID of ISP tag receives it from the port default VID.

The VLAN ID is generated from the ISP tag, and the TC is generated from the ingress frame outer tag.

Note: It is illegal to strip out the ISP tag on the ISP egress port by using the untagged bit setting in the VLAN table.

Note: Only the VLAN tagged or untagged packets are expected for the ingress of the customer ports. The customer do not add the ISP tags.

There are two possible traffic scenarios; one from a customer port to an ISP port, and one from an ISP port to a customer port.

Uplink Traffic (from Customer Port to ISP)

Data traffic is traffic received from the customer port without tags or a customer tag, and the frame is destined for an ISP port. The customer ingress port performs a normalization process to allow ingress frames with double tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag.

However, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the customer port normalization process. The TC do not change.

Control traffic frames can be forwarded to the CPU first and then the CPU forwards to the ISP port if the switch management mode is enabled and if the RESV_MCAST_FLOOD bit=0 in the Global VLAN Control 4 register. In this case, the control frame adds an ISP tag by ingress port and forward to the CPU. The CPU can then forward it to the ISP port with or without the ISP tag by using the egress-direct feature.

Downlink Traffic (from ISP to Customer Port)

Data traffic frame received from ISP port may or may not have ISP tag attached. When the received frame does not have an ISP tag and customer tag, the ISP ingress port does a normalization process to insert double tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag. All ARL and VID table access should be based on the new tag. The traffic is then forwarded to the customer port through proper VLAN configuration. Usually, the software configures so the customer Egress port continuously removes the ISP tag. However, it is based on how the untagged map is configured.

Moreover, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the ISP port normalization process. The TC will not change.

The Control traffic is forwarded to the CPU when the switch management mode is enable and if the RESV_MCAST_FLOOD bit=0 in the Global VLAN Control 4 register. The BCM53118 can also support multiple ISP port configurations by enabled the FWD_MODE bit of VLAN Table Entry register. There are also two ways to separate traffic that belongs to two different ISP customers:

1. Each group (ISP, and customer) is assigned to the same VLAN group, so that traffic does not leak to other ISP.
2. Use the Port-based VLAN to separate traffic that belongs to a different ISP.

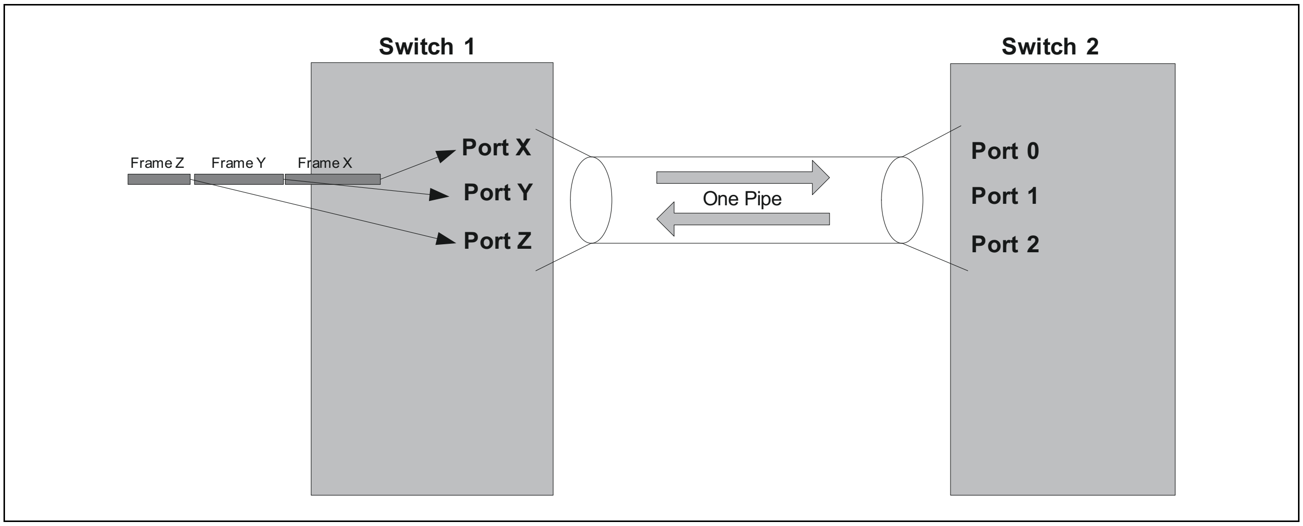
Jumbo Frame Support

The BCM53118 can receive and transmit frames of extended length on ports linked at gigabit speed. Referred to as jumbo frames, these packets are longer than standard maximum size which is defined via the "Standard Max Frame Size Register (Page 40h: Address 05h)" on page 250, but shorter than 9720 bytes. Jumbo packets can only be received or forwarded to 1000BASE-T linked ports that are jumbo-frame enabled. Up to 38 buffer memory pages are required for storing the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo enabled, it is recommended that no more than two be enabled simultaneously to ensure system performance. There is no performance penalty for enabling additional jumbo ports beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

Port Trunking/Aggregation

The BCM53118 support MAC-based trunking. The trunking feature allows up to four ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM53118 allow up to two trunk groups. Trunks are composed of predetermined ports and can be enabled via Trunking Group 0 register. Ports within a trunk group must be of the same linked speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other port within the trunk automatically assumes all traffic designated for the trunk. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed on either the DA, SA, or DA/SA, depending on the Trunk Hash Selector bit of "MAC Trunking Control Register (Page 32h: Address 00h)" on page 236.

Figure 5: Trunking



WAN Port

The BCM53118 offers a programmable WAN port feature: it has a "WAN Port Select Register (Page 00h: Address 26h–27h)" on page 149. Select a port as a WAN port, then all of that port's traffic is forwarded to the CPU port only. The non-WAN port traffic from all other local ports does not flood to the WAN port.

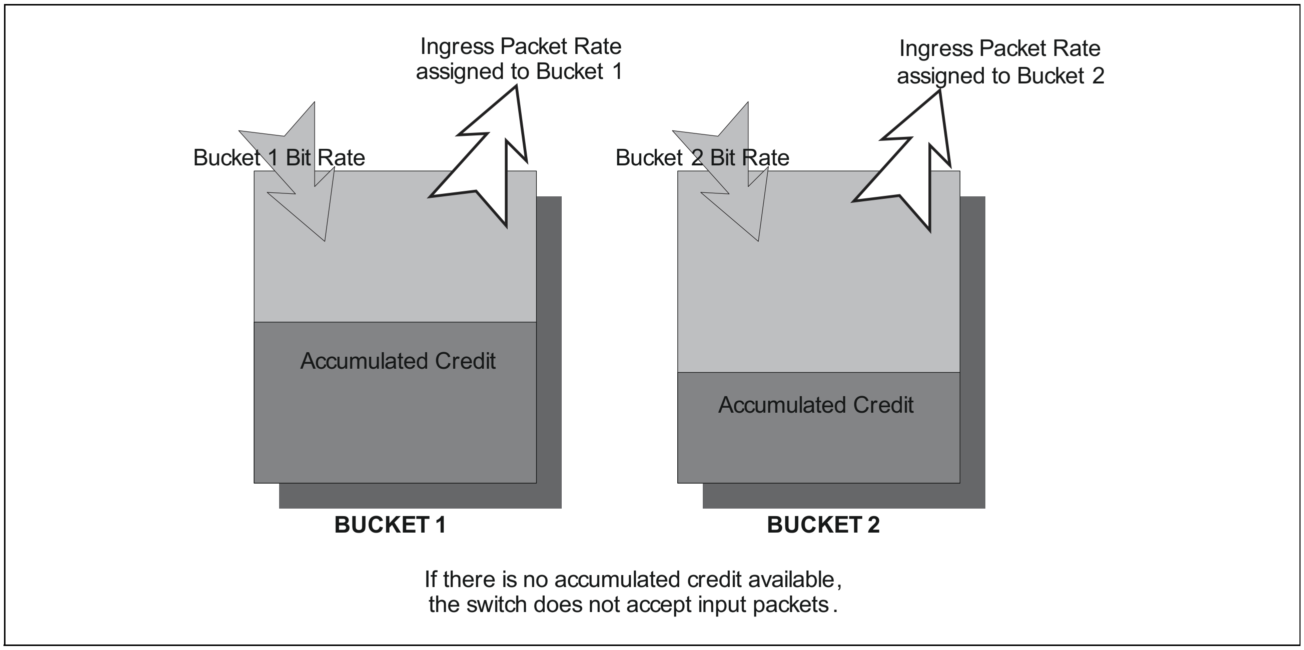
Rate Control

Ingress Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped. To enable the Broadcast Storm Suppression, pull the BC_SUPP_EN high during power-on/reset. Alternatively, the feature can be activated in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253.

The broadcast storm suppression mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 6 on page 45). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable-maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the bucket bit rate (the rate at which credit is added to the bucket). At this point, excess packets are either dropped or deterred via flow control, depending upon the Suppression Drop mode in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251.

Figure 6: Bucket Flow



Two-Bucket System

For added flexibility, the BCM53118 employ two buckets to track the rate of ingressed packets. Each of the two buckets (Bucket 0 and Bucket 1) can be programmed to monitor different packet types. For example, Bucket 0 could monitor broadcast packets, while Bucket 1 monitors multicast packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be individually programmed (see "Bucket Bit Rate" on page 46). For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed via the Suppressed Packet Type Mask of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251. This determines the maximum credit than can accumulate in each bucket. The Rate Count and Bucket Size can be individually programmed for each port, providing another level of flexibility. Suppression control can be enabled or disabled on a per-port basis "Ingress Rate Control Configuration Register (Page 41h: Address 00h)". This system allows the user to control dual packet-type rates on a per-port basis.

Egress Rate Control

The BCM53118 monitor the rate of egress traffic per port. Unlike the Ingress traffic rate control, the Egress Rate Control provides only the per port rate control regardless of traffic types. This feature only uses one bucket to track the rate of egressed packets. The Egress Rate Control feature can be enabled in the "Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)" on page 255, and the output rate per port can be controlled by setting the bucket size and Refresh Count in the same register. The Egress Rate Control feature only support absolute bit rate mode (Bit Rate Mode = 0) and the bucket bit rate calculation is shown in Table 3 on page 46.

Bucket Bit Rate

The relative ingress rates of each bucket can be programmed "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 on a per port basis. Each port has a programmable Rate Count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251 on a chip basis. If this bit is 1, the packet rate is automatically scaled according to the port link speed. Ports operating at 1000 Mbps would be allotted a 100 times higher ingress rate than ports linked at 10 Mbps. Together, the Rate Count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The Rate Count values are specified in Table 3. Values outside these ranges are not valid entries.

Table 3: Bucket Bit Rate

Rate Count (RC)	***Bit Rate Mode***	***Link Speed***	***Bucket Bit Rate Equation***	***Approximate Computed Bucket Bit Rate Values (as a function of RC)***
1–28	0	Any	= (RC x 8 x 1M) / 125	64 KB, 128 KB, 192 KB,..., 1.792 MB
29–127	0	Any	= (RC – 27) x 1M	2 MB, 3 MB, 4 MB,..., 100 MB
128–240	0	Any	= (RC – 115) x 1M x 8	104 MB, 112 MB, 120 MB,..., 1000 MB
1–125	1	10 Mbps	= (RC x 8 x 1M) / 100	0.08 MB, 0.16 MB, 0.24 MB,... 10 MB
1–125	1	100 Mbps	= (RC x 8 x 1M) / 10	0.8 MB, 1.6 MB, 2.4 MB,..., 100 MB
1–125	1	1000 Mbps	= RC x 8 x 1M	8 MB, 16 MB, 24 MB,... 1000 MB
Note: 1M represents 1 x 10^6.				

IMP Port Egress Rate Control

The IMP port egress is configurable of rate limiting at packet-per-second (PPS) granularity, in addition to bits-per-second (BPS) granularity. It can be configured via the"IMP Port Egress Rate Control Configuration Register (Page 41h: Address C0h)" on page 256.

Protected Ports

The Protected Ports feature allows certain ports to be designated as protected "Protected Port Selection Register (Page 00h: Address 24h–25h)" on page 148. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. Several applications that can benefit from protected ports:

- Aggregator: For example, all the available ports are designated as protected ports except a single aggregator port. No traffic incoming to the protected ports is sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent non-secured ports from monitoring important information on a server port, the server port and non-secured ports are designated as protected. The non-secured ports will not be able to receive traffic from the server port.

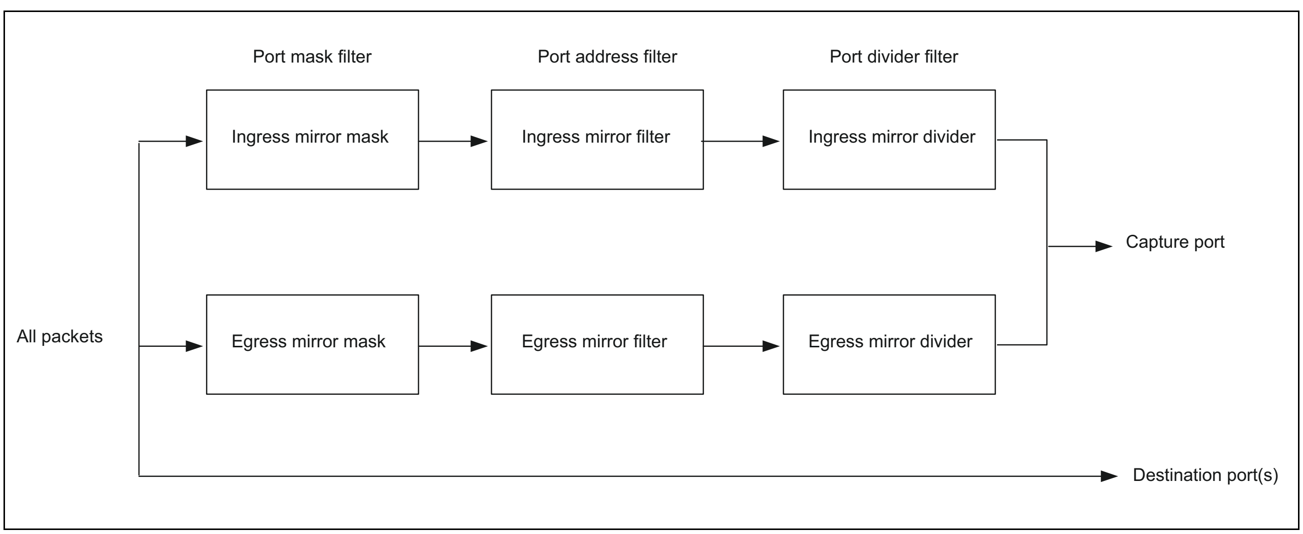
Port Mirroring

The BCM53118 support Port Mirroring, allowing ingress and/or egress traffic to be monitored by a single port designated as the mirror capture port. The BCM53118 can be configured to mirror the ingress traffic and/or egress traffic of any other port (s). Mirroring multiple ports is possible, but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

Enabling Port Mirroring

Port Mirroring is enabled by setting the Mirror Enable bit in the "Mirror Capture Control Register (Page 02h: Address 10h)" on page 163.

Figure 7: Mirror Filter Flow



Capture Port

The capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the Capture port according to the mirror filtering rules discussed below. The Capture port is specified by the Capture Port bits of the "Mirror Capture Control Register (Page 02h: Address 10h)".

Mirror Filtering Rules

Mirror filtering rules consist of a set of three filter operations (Port Mask, Packet Address, and Packet Divider) that are applied to traffic ingressed and/or egressed at a switch port.

Port Mask Filter

The IN_MIRROR_MASK bits in the "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 164 define the receive ports that are monitored. The OUT_MIRROR_MASK bits in the "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 166 define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one-mirror capture port should be taken into account to avoid congestion or packet loss.

Packet Address Filter

The "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 164 is used to set the type of filtering that is applied to frames received on the mirrored ports. The IN_MIRROR_FILTER bits select among the following:

- Mirror all received frames
- Mirror received frames with DA = x
- Mirror received frames with SA = x

where x is the 48-bit MAC address programmed into the "Ingress Mirror MAC Address Register (Page 02h: Address 16h)" on page 165. Likewise, the "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 166 is used to set the type of filtering that is applied to frames transmitted on the egressed mirrored ports. The filtering MAC address is specified in the "Egress Mirror MAC Address Register (Page 02h: Address 20h)" on page 167.

Packet Divider Filter

The IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 164 allows further statistical sampling. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the "Ingress Mirror Divider Register (Page 02h: Address 14h)" on page 165. Only one out of every n frames is forwarded to the mirror capture port, where n = IN_MIRROR_DIV +1. This allows the following additional capabilities:

- Mirror every n^{th} received frame
- Mirror every n^{th} received frame with DA = x
- Mirror every n^{th} received frame with SA = x

Similarly, the Egress Mirror Divide function is controlled by the “Egress Mirror Control Register (Page 02h: Address 1Ch)” on page 166 and the “Egress Mirror Divider Register (Page 02h: Address 1Eh)” on page 166.

Note: When multiple ingress ports have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN_MIRROR_DIV to deliver the nth receive frame to the mirror capture port. Egressed frames are governed by the OUT_MIRROR_MASK bit and the OUT_MIRROR_DIV bit.

IGMP Snooping

The BCM53118 supports IP layer IGMP Snooping which includes IGMP unknown, query, report, and leave messages via the “High-Level Protocol Control Register (Page 02h: Address 50h–53h)” on page 168, and the minimum value of IP header Internet Header Length field is 6.

A frame with a value of 2 in the IP header protocol field and IGMP frames are forwarded to the CPU port. The management CPU can then determine, from the IGMP control packets which port should participate in the multi-group session. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. If the IGMP_FWD_EN in the “High-Level Protocol Control Register (Page 02h: Address 50h–53h)” is enabled, IGMP frames will be trapped to the CPU port only.

MLD Snooping

The BCM53118 supports IP layer MLD Snooping including MLD query, report, and done messages via the “High-Level Protocol Control Register (Page 02h: Address 50h–53h)” on page 168.

IEEE 802.1x Port-Based Security

IEEE 802.1x is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM53118 detect EAPOL frames by checking the destination address of the frame. The Destination addresses should be either a multicast address as defined in IEEE 802.1x (01-80-C2-00-00-03) or a user-predefined MAC (unicast or multicast) address. Once EAPOL frames are detected, the frames are forwarded to the CPU so it can send the frames to the authenticator server. Eventually, the CPU determines whether the requestor is qualified or not based on its MAC_Source addresses, and frames are either accepted or dropped. The per-port EAP can be programmed in the register.

BCM53118 provides three modes for implementing the IEEE 802.1x feature. Each mode can be selected by setting the appropriate bits in the register.

The Basic Mode (when EAP Mode = 00'b) is the standard mode, the EAP_BLK_MODE bit would be set before authentication to block all of the incoming packets, upon authentication, the EAP_BLK_MODE bit would be cleared to allow all the incoming packets. In this mode, the Source Address of incoming packets is not checked.

The second mode is Extended Mode (when EAP Mode = 10'b), where an extra filtering mechanism is implemented after the port is authenticated. If the Source MAC address is unknown, the incoming packets would be dropped and the unknown SA would not be learned. However if the incoming packet is IEEE 802.1x packet, or special frames, the incoming packets will be forwarded. The definition of the Unknown SA in this case is when the switch cannot match the incoming Source MAC address to any of the addresses in ARL table, or the incoming Source MAC address matches the address in ARL table, but the port number is mismatched. The third mode is Simplified Mode (when EAP Mode = 11'b). In this mode, the unknown Source MAC address packets would be forwarded to CPU rather than dropped. Otherwise, it is same as the Extended Mode operation.

Note: The BCM53118 checks only the destination addresses to qualify EAPOL frames. Ethernet type fields, packet type fields, or non-IEEE 802.1Q frames are not checked.

DoS Attack Prevention

The BCM53118 supports the detection of the following DoS (Denial of Service) attack types based on a register setting, which can be programmed to drop or not to drop each type of DoS packet, respectively.

Table 4: DoS Attacks Detected by BCM53118

DoS Attack Type	*Description*
IP_LAND	IPDA = IPSA in an IPv4/IPv6 datagram
TCP_BLAT	DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
UDP_BLAT	DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
TCP_NULLScan	Seq_Num = 0 and all TCP_FLAGs = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
TCP_XMASScan	Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
TCP_SYNFINScan	SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
TCP_SYNError	SYN = 1, ACK = 0, and SRC_Port < 1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram
TCP_ShortHDR	The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size
TCP_FragError	The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data
ICMPv4_Fragment	The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram
ICMPv6_Fragment	The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram

Table 4: DoS Attacks Detected by BCM53118 (Cont.)

DoS Attack Type	*Description*
ICMPv4_LongPing	The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header
ICMPv6_LongPing	The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size

- MIN_TCP_Header_Size is programmable between 0 and 255 bytes, inclusive. The default value is set to 20 bytes (TCP header without options).
- MAX_ICMPv4_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.
- MIN_TCP_Header_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.
- The default control setting for all types of DoS attacks is not to drop the DoS attack packet.
- It is globally configurable whether to perform the SA learning operation with the received packets of the DoS attack type defined in the registers, regardless of the individual DoS attack types.
- Once a packet is detected as a DoS attack type that must be dropped, the packet is dropped regardless of ARL forwarding decisions, but its forwarding based on mirroring function is not affected.

MSTP Multiple Spanning Tree

The BCM53118 supports up to eight multiple spanning trees. When the EN_RX_BPDU bit = 1, the BCM53118 forwards BPDU packets to the management port only.

Software Reset

The BCM53118 provide Software Resets. Software Resets can be triggered by programming the "Software Reset Control Register (Page 00h: Address 79h)" on page 155.

Loop Detection

The BCM53118 provide the Loop Detection feature for unmanaged environments (that is, those without a management CPU). When the Loop Detection feature is enabled and activated, the switch generates Broadcom proprietary tag frames (Loop Discovery Frames) at a programmed interval, and when it detects a loop, it gives a loop detected warning with a blinking LED or with a sound produced by a speaker. This feature does not repair the loop, but only issues a warning.

The Discovery Frame is a broadcast frame, and the switch ensures the forwarding of the frame by providing special priority for the frame by giving it a higher priority over other broadcast frames, assigning highest queue automatically and overwriting the pause condition. The control/options over this feature are provided beginning with the "Loop Detection Control Register (Page 72h: Address 00h)" on page 265.

The Loop Discovery frame uses a default multicast address (01-80-C2-00-00-01) in the Loop Detect Source Address register as a source address. Using a multicast address as a source address is illegal in the IEEE standard; however, since this is only intended to be used in the ROBO environment only, it should be allowed. This address scheme is used to avoid a possible disruption in forwarding decision by using a regular random Source Address.

The Loop Discovery frame also uses the Module ID 0 register along with the Module ID 1 register to identify the origin of the Discovery frame. These registers are used to define a Source Chip ID and Source Port ID to distinguish the Discovery Frames from other ROBO chips.

The implementation example for the Loop Detect feature is described in the *BCM53118 Design Guide*.

Green Mode

The BCM53118 supports Green mode for power saving within 10 meter cable lengths and it can be enabled by the strap pin "En_Green". When the Green mode feature is enabled, the BCM53118 can detect cable length automatically and perform power saving for cable lengths less than 10 meters. It is for the link at Giga only. If Green mode is enabled (strap pin En_Green = 1), the external CPU could not access the BCM53118 through the Pseudo-PHY or SPI interface. En_Green strap pin to enable Green mode is for unmanaged systems.

BroadSync HD

BroadSync HD is the enhancement to IEEE 802.3 MAC and IEEE 802.1D bridges to support the kind of low-latency isochronous services and guaranteed quality of service (QoS) that is required for many consumer electronics applications.

The BCM53118 provides the BroadSync HD feature through the "BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)" on page 268. The BCM53118 always forwards BPDU, MRP packets to CPU for BroadSync HD applications, and handles the IEEE 802.1 Time Sync Protocol.

The BCM53118 can identify a packet as a BroadSync HD packet if the MAC DA matches a multicast group (configured based on MRP protocols). The PCP equals four or five and the ingress port is BroadSync HD-enabled. There are two dedicated queues for BroadSync HD Class 5 and Class 4 traffic per egress port. BCM53118 enhances shaping and scheduling for BroadSync HD operation.

Time Base and Slot Generation

For BroadSync HD applications, the BCM53118 maintains a time base (32-bit counter) running at a granularity of 1 ns, which can be adjusted by CPU for synchronization with the BroadSync HD time master unit (Switch or Host) through the IEEE 802.1 Time Synchronized (TS) protocol (to be standardized). The TS protocol is implemented by the CPU which requires the BCM53118 to perform the following operations.

- A received TS protocol packet is time stamped at the ingress port when the first byte (of MACDA) arrives, and is transferred along with the receiving time stamp to the CPU.
- A TS protocol packet initiated by the CPU (to be transmitted at an egress port) is time stamped at the egress port when the first byte (of MACDA) is transmitted, and the transmit time stamp recorded at the egress port is reported back to CPU.

It is required that the time synchronization point peers over an Ethernet link is chosen such that the link delay is perceived as constant, and the protocol exchange occurs at least every 10 ms over every link.

The CPU may be required to speed up or slow down the timebase maintained in BCM53118 based on the TS protocol execution. The BCM53118 provides the time base adjustment mechanism for graceful time changes based on CPU instructions.

In addition, the BCM53118 maintains counter mechanism to generate time Slot for BroadSync HD traffic scheduling.

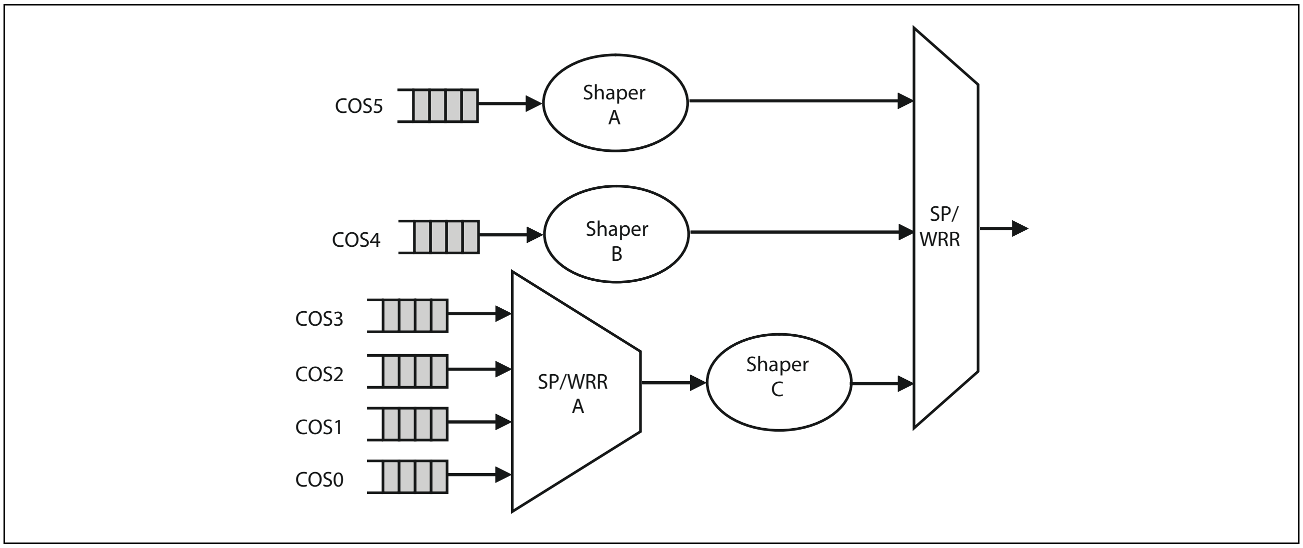
- A Slot is defined as 125 µs, it is used to pace the BroadSync HD Class 5 traffic which has tight jitter requirements;
- A MacroSlot is configurable as 1 ms, 2 ms, or 4 ms (binary number of Slots) via the "BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)" on page 271. It is used to pace the BroadSync HD Class 4 traffic which has relaxed jitter requirements.

The CPU may be required to make the Slot wider or narrower based on the TS protocol execution. The BCM53118 provides the Slot adjustment mechanism for graceful Slot width changes based on CPU instructions.

Transmission Shaping and Scheduling

Packets queued at each Ethernet (egress) port is subject to the scheduling behavior as shown in Figure 8 on page 54.

Figure 8: BroadSync HD Shaping and Scheduling



BroadSync HD Class 5 Media Traffic

The COS5 queue is dedicated for BroadSync HD Class 5 traffic only, and a COS5 packet is always the highest priority to be scheduled for transmission, if it is allowed by the Shaper A that operates as follows.

- The Shaper A is an emulation of fixed bandwidth pipe for Class 5 BroadSync HD traffic with tight jitter adaptively to handle interference from non-BroadSync HD or Class 4 BroadSync HD traffic. Note that the preamble and IPG transmission are not taken into account for the pipe operation.
- Tunable parameters for the Shaper A are listed as follows.
  - MaxAVPacketSize indicates the maximum packet size allowed on a BroadSync HD-enabled port. It is a global setting via "BroadSync HD Max Packet Size Register (Page 90h: Address 04h)" on page 269.
  - Class5_BW indicates the reserved bandwidth for Class 5 BroadSync HD traffic at granularity of Byte (per Slot, 125 µs). It is a per-port setting via "BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)" on page 271.
  - Class5_Window indicates the jitter control for Class 5 BroadSync HD transmission. It is a per-port setting via "BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)" on page 271.
- At the start of each Slot,
  - Reset the credit in the shaping bucket to Class5_BW, if the queue is empty.
  - Reset the credit in the shaping bucket to Class5_BW, if the queue is not empty and Class5_Window is set to 0.
  - Reset the credit in the shaping bucket to Class5_BW, if the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is greater than MaxAVPacketSize.
  - Add Class5_BW to the credit in the shaping bucket, if the queue is not empty, Class5_Window is set to 1, and the credit remained in the shaping bucket is less than or equal to MaxAVPacketSize.
- The credit in the shaping bucket decrements for every byte transmitted for the Class 5 BroadSync HD traffic through the port.

- If the credit reaches 0 before the end of the current Slot while transmitting a Class 5 BroadSync HD packet, the ongoing packet transmission is not interrupted, and the credit stays at 0 until being reset at the start of next Slot.
- The credit decrements resumes at the next Slot if the ongoing transmission continues.

- As long as the credits in the shaping bucket is greater than 0, a Class 5 BroadSync HD packet is allowed to be scheduled for transmission.

BroadSync HD Class 4 Media Traffic

The COS4 queue is dedicated for BroadSync HD Class 4 traffic only, and a COS4 packet always yield to COS5 traffic (if allowed to be scheduled), but takes precedence over the traffic from COS0~COS3 queues or follow the weight ratio between COS4 and COS0~COS3 for transmission scheduling, if it is allowed by the Shaper B that operates as follows.

- The Shaper B is an emulation of fixed bandwidth pipe for Class 4 BroadSync HD traffic with relaxed jitter adaptively to handle interference from non-BroadSync HD or Class 5 BroadSync HD traffic. It also statistically levels the Class 4 BroadSync HD transmission bursts towards the next hop switch to reduce the buffering requirements, by using Slot (instead of MacroSlot) as the pacing mechanism. The preamble and IPG transmission are not accounted for in the pipe operation.
- Tunable parameters for the Shaper B are listed as follows:
  - MacroSlot_Period indicates the periodic cycle time to shape the Class 4 traffic. It is a global setting via "BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)" on page 271 to indicate 1 ms, 2 ms, or 4 ms.
  - MaxAVPacketSize indicates the maximum packet size allowed on a BroadSync HD-enabled port. It is a global setting. (same as for BroadSync HD Class 5 setting)
  - Class4_BW indicates the evenly divided bandwidth share per Slot, which is derived from dividing the reserved bandwidth for Class 4 BroadSync HD traffic at granularity of Byte (per MacroSlot) by the number of Slots within a MacroSlot. It is a per-port setting via "BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)" on page 272.
- At the start of each Slot,
  - If the Slot is the first one for the current MacroSlot, reset the credit bucket to Class4_BW+MaxAVPacketSize; (MaxAVPacketSize is used as the deficit base)
  - Otherwise, add Class4_BW to the credit in the shaping bucket.
- The shaping credit bucket decrements for every byte transmitted for the Class 4 BroadSync HD traffic.

As long as the credits in the shaping bucket is greater than or equal to MaxAVPacketSize, a Class 4 BroadSync HD packet is allowed to be scheduled for transmission

CableChecker™

The BCM53118 provide the cable diagnostic capabilities for unmanaged environments. The actual cable diagnostic feature lies in the PHY functional block. The BCM53118 devices let the user monitor the cable diagnostic results through LED display by setting the appropriate bits in the LED refresh registers.

The BCM53118 uses the existing LED display (which is already assigned to various functions) to indicate the cable diagnostic results. Table 5 shows the cable diagnostic result output for each LED function where 1 and 0 represent the LED indication pin status; 1 indicates active and 0 indicates non-active.

Note:

- The best way for a user to visualize the cable diagnostic test result through LEDs is to bring out the LINK status bit to the LED display along with other functions to be displayed per port. In this way, the user can observe the cable diagnostic result from the flashing (or lit) LED of other functions while LINK LED is off. The switch will turn off the LINK status LED during the cable diagnostic mode.
- The cable diagnostic is expected to be most effective when the user cannot establish the link with the partner.

Table 5: Cable Diagnostic Output

LED Function in LED Function Register	*Cable Diagnostic Output*
Reserved	–
LNK	No output during the cable diagnostic mode
DPX	1: Passed 0: Failed
ACT	1: Passed 0: Failed
COL	1: Passed 0: Failed
LNK/ACT	No output during the cable diagnostic mode
DPX/COL	1: Passed 0: Failed
SPD10M	1: Failed 0: Passed
SPD100M	In LED function0 map 1: Cable diagnostic passed 0: Failed In LED function1 map 1: Cable diagnostic failed 0: Passed
SPD1G	1: Passed 0: Failed

Table 5: Cable Diagnostic Output (Cont.)

LED Function in LED Function Register	*Cable Diagnostic Output*
10M/ACT	1: Failed 0: Passed
100M/ACT	In LED function0 map 1: Cable diagnostic passed 0: Failed In LED function1 map 1: Cable diagnostic failed 0: Passed
10–100M/ACT	1: Failed 0: Passed
1G/ACT	1: Passed 0: Failed
Reserved	–

Egress PCP Remarking

The BCM53118 provides an egress PCP remarking feature of the outer tag at each egress port which includes the CFI and PCP field modification based on the internal generated TC. The Egress PCP remarking process applies to Ethernet ports only and can be enabled by "Traffic Remarking Control Register (Page 91h: Address 00h)" on page 274. Each Ethernet port can provide a 8-entry mapping table indexed by TC to map to the {New CFI, New PCP} field for the outgoing packet via "Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h)" on page 275.

Note: For the BroadSync HD-enabled egress port, the egress PCP for the non-BroadSync HD class of traffic must never be programmed with values of 100 and 101.

Address Management

The BCM53118 Address Resolution Logic contains the following features:

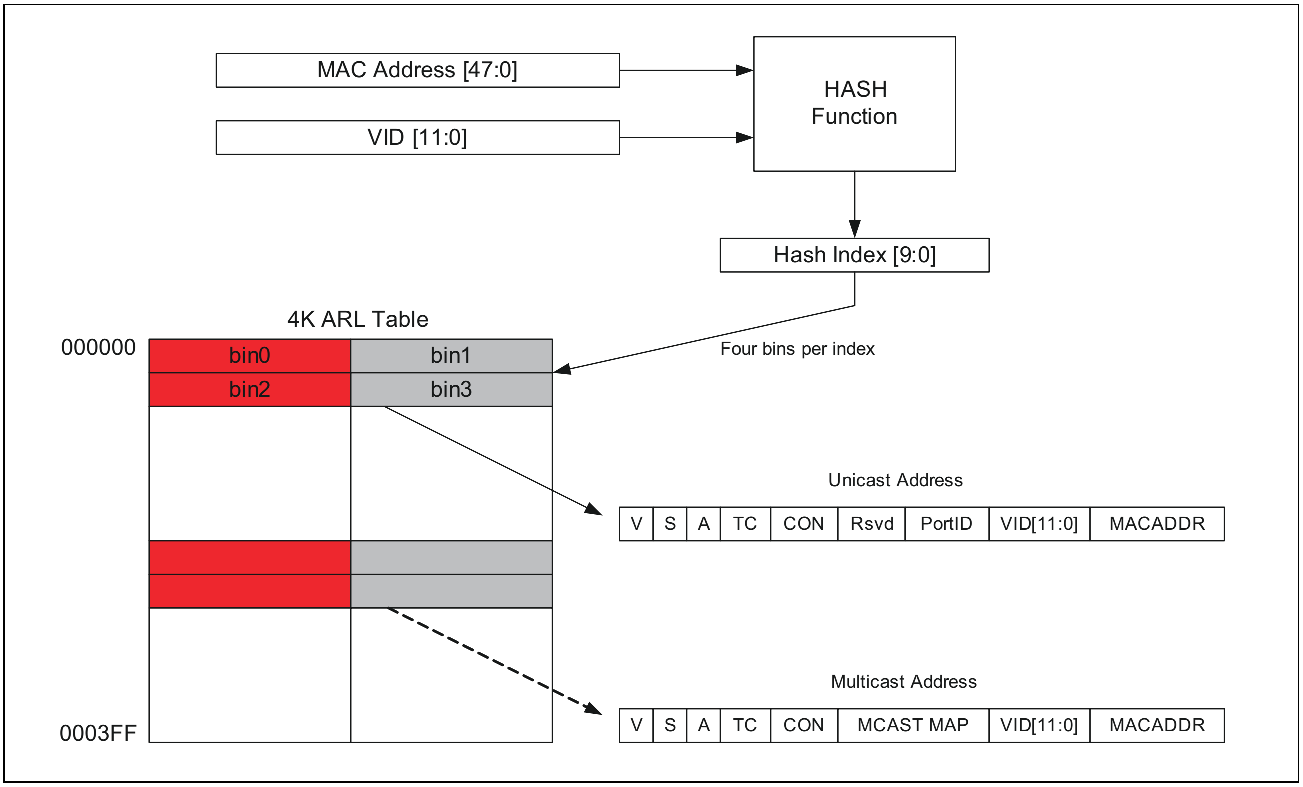
- Four bins per bucket address table configuration.
- Hashing of the MAC/VID address to generate the address table point.

The address management unit of the BCM53118 provides wire speed learning and recognition functions. The address table supports 4K unicast/multicast addresses using on-chip memory.

Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains four entries or bins. The address table has 1K buckets with four entries in each bucket. This allows up to four different MAC addresses with the same hashed index bits to be simultaneously mapped into the address table. In the ARL DA/SA lookup process, it hashes a 10-bit search index and read out bin0 and bin1 in the first cycle, and read out bin2 and bin3 in the second cycle. These four entries are used for ARL routing and learning.

Figure 9: Address Table Organization



The index to the address table is computed using a hash algorithm based on the MAC address and the VLAN ID (VID) if enabled.

Note: In the Enable IEEE 802.1Q and VLAN Learning Mode both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See "IEEE 802.1Q VLAN" on page 39 for more information.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits[9:0] of the hash are used as an index to the approximately 4K locations of the address table.

The CRC-CCITT polynomial is:

$$x^{16}+x^{12}+x^{5}+1$$

Address Learning

Information is gathered from received unicast packets and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.
- The packet does not have a reserved multicast destination address. The Multicast Learning bit of the "Reserved Multicast Control Register (Page 00h: Address 2Fh)" on page 149 can disable this condition.
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 7 on page 60 for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table, but must be written via one of the "Programming Interfaces" on page 92. See "Writing an ARL Entry" on page 64 and Table 9 on page 61 for more information.

Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The destination address (DA) and VID of the received packet are used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for "Unicast Addresses" on page 59 and "Multicast Addresses" on page 60.

Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. Listed below is the unicast address-resolution algorithm:

- If the multiport addressing feature is enabled and the DA matches one of the programmed multiport addresses, then it is forwarded accordingly. See "Using the Multiport Addresses" on page 65.
- The lower 10 bits of the hashed index key are used as a pointer into the address table memory, and the entry is retrieved.
- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.
  - If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the unicast DLF forward bit is set, the frame is forwarded according to the port map in the "Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)" on page 151.

- Otherwise, the packet is flooded to all appropriate ports.

See Table 6 on page 60 for definitions of the unicast index key and the assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See Table 7 for a description of a unicast ARL entry.

Table 6: Unicast Forward Field Definitions

EN_1QVLAN	Index Key	Forwarding Field
1	DA and VID	Port ID
0	DA	Port ID

Table 7: Address Table Entry for Unicast Address

Field	Description
VID	VLAN ID associated with the MAC address.
VALID	1 = Entry is valid. 0 = Entry is empty.
STATIC	1 = Entry is static—Should not be aged out and is written and updated by software. 0 = Entry is dynamically learned and aged.
AGE	1 = Entry has been accessed or learned since last aging process. 0 = Entry has not been accessed since last aging process.
TC	MACDA-based TC (only valid for static entries). See “Quality of Service” on page 34 for more information.
Reserved	–
Reserved	Only 00 is valid.
PORTID	Port identifier. The port associated with the MAC address.
MAC ADDRESS	48-bit MAC address.

Note: The fields described in Table 7 can be written via the“ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 177 and “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 178.

Multicast ARL table entries are described in Table 9 on page 61.

Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP_MULTICAST bit is set, multicast frames are assigned a forwarding field corresponding to a multicast port map from the matching ARL entry (see “Address Management” on page 57). If no matching ARL entry is found, the packet is flooded to all appropriate ports. Listed below is the multicast address resolution algorithm:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 10 on page 62.
- If the multiport addressing feature is enabled and the DA matches one of the programmed Multiport Addresses, then it is forwarded accordingly. See "Using the Multiport Addresses" on page 65.
- Otherwise, the lower 10 bits of the hashed index key are used as a pointer into the ARL table memory, and the entry is retrieved.
- If the valid indicator is set, and the address stored at the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the multicast DLF forward bit is set (see "Address Management" on page 57), the frame is forwarded according to the port map in the "Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)" on page 151.
- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

See Table 8 for definitions of the multicast index key and the assigned forwarding field. The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See Table 9 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 63 for more information.

Table 8: Multicast Forward Field Definitions

EN_1QVLAN	*IP_MULTICAST*	*Index Key*	*Forwarding Field*
1	0	DA and VID	Port ID
0	0	DA	Port ID
1	1	DA and VID	IPMC0
0	1	DA	IPMC0

Table 9: Address Table Entry for Multicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address.
VALID	1 = Entry is valid. 0 = Entry is empty.
STATIC	1 = Entry is static—This entry is not aged out and is written and updated by software. 0 = Not defined.
AGE	The AGE bit is ignored for static ARL table entries.
TC	MACDA-based TC (only valid for static entries). See "Quality of Service" on page 34 for more information.
Reserved	–
IPMC0 [8:0]	Multicast forwarding mask. 1 = Forwarding enable. 0 = Forwarding disable.
MAC ADDRESS	48-bit MAC address.

Note: The fields described in Table 9 can be written via the “ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 177 and “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 178.

Unicast ARL table entries are described in Table 7 on page 60.

Reserved Multicast Addresses

Table 10 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions. Bits[4:0] of the “Reserved Multicast Control Register (Page 00h: Address 2Fh)” on page 149 program groups of these addresses to be dropped or forwarded. Writing to these bits can change the default action of Unmanaged mode summarized in Table 10.

Table 10: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*IEEE 802.1 Specified Action*	*Unmanaged Mode Action*	*Managed Mode Action*
01-80-C2-00-00-00	Bridge group address	Drop frame	Flood frame	Forward frame to IMP only
01-80-C2-00-00-01	IEEE 802.3x MAC control frame	Drop frame	Receive MAC determines if it is a valid pause frame and then acts accordingly	Receive MAC determines if valid pause frame and acts accordingly.
01-80-C2-00-00-02	Reserved	Drop frame	Drop frame	Forward to frame management port only
01-80-C2-00-00-03	IEEE 802.1x port-based network access control	Drop frame	Drop frame	Forward frame to management port only
01-80-C2-00-00-04–01-80-C2-00-00-0F	Reserved	Drop frame	Drop frame	Forward frame to management port only
01-80-C2-00-00-10	All LANs bridge management group address	Forward frame	Flood frame	Forward frame to all ports including management port
01-80-C2-00-00-11–01-80-C2-00-00-1F	Reserved	Forward frame	Flood frame	Forward frame to all ports excluding management port
01-80-C2-00-00-20	GMRP address	Forward frame	Flood frame	Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 4 of page 34, offset 04h register)

Table 10: Behavior for Reserved Multicast Addresses (Cont.)

MAC Address	Function	IEEE 802.1 Specified Action	Unmanaged Mode Action	Managed Mode Action
01-80-C2-00-00-21	GVRP address	Forward frame	Flood frame	Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 5 of page 34, offset 04h register)
01-80-C2-00-00-22–01-80-C2-00-00-2F	Reserved	Forward frame	Flood frame[a]	Forward frame to all ports excluding management port

a. Frames flood to all ports. Certain exclusions apply, such as VLAN restrictions.

Static Address Entries

The BCM53118 supports static ARL table entries that are created and updated via one of the “Programming Interfaces” on page 92. These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location via an “Page 05h: ARL/VTBL Access Registers” on page 175 and setting the STATIC bit. The AGE bit is ignored. Static entries do not automatically learn MAC addresses or port associations and are not aged out by the automatic internal aging process. See “Writing an ARL Entry” on page 64 for details.

Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL read/write control, which allows an address-entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

Reading an ARL Entry

To read an ARL entry:

1. Set the MAC address in the “MAC Address Index Register (Page 05h: Address 02h)” on page 176.
2. Set the VLAN ID in the “VLAN ID Index Register (Page 05h: Address 08h)” on page 176. This is necessary only if the VID is used in the index key.
3. Set the ARL_R/W bit to 1 in the “ARL Table Read/Write Control Register (Page 05h: Address 00h)” on page 176.
4. Set the START/DONE bit to 1 in the “ARL Table Read/Write Control Register (Page 05h: Address 00h)”. This initiates the read operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. The matching ARL entry is read. The contents of entry are stored in the “ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)” on page 177 and the “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 178.

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. Entries that do not match may be a valid entry, but are not a valid match for the index key. All other read entries are considered valid ARL entries.

Writing an ARL Entry

To write an ARL entry:

1. Follow the steps in "Reading an ARL Entry" to read the ARL entry matching the MAC address and VID that are written to the table.
2. Keep the values that remain from the previous read operation.
   - "MAC Address Index Register (Page 05h: Address 02h)"
   - "VLAN ID Index Register (Page 05h: Address 08h)" on page 176
   - "ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)"
   - "ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)"
3. Modify the correct entry as necessary. Set the STATIC bit so that the entry is not aged out.
4. Set the ARL_R/W bit to 0 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 176.
5. Set the START/DONE bit to 1 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)". This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table.

Searching the ARL Table

The second method to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the Start/Done bit in the "ARL Table Search Control Register (Page 05h: Address 50h)" on page 179 begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the Search Valid bit indicates when a found valid entry is available in the "ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)" on page 180 and the "ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)" on page 181. When the host reads the contents of the ARL Table Search Data Result 1 register which located in Page 05h: Address 78h, the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write, or search process and then read/write other registers, returning periodically to see if the operation has completed.

Address Aging

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous one to two aging intervals. The aging interval is programmable via the Aging Enable and AGE TIME bit in the "Aging Time Control Register (Page 02h: Address 06h)" on page 163.

Entries that are written and updated via one of the "Programming Interfaces" on page 92, should have the STATIC bit set. Thus, they are not affected by the aging process.

For each entry in the ARL table, the aging process performs the following:

- If the VALID bit is not set, no further action is required.
- If the VALID bit is set and the STATIC is set, no further action is required.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is set, then clear the AGE bit. This keeps the entry in the table, but marks it so that it is removed if it is not accessed before the subsequent aging scan.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is reset, then reset the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

Fast Aging

The fast aging function can be enabled per port or VLAN ID:

The port fast aging can be enabled by setting the Start/Done of the "Fast-Aging Control Register (Page 00h: Address 88h)" on page 155, the Fast Age All Ports bit of the "Fast-Aging Port Control Register (Page 00h: Address 89h)" on page 156, and the appropriate port bits in the "Fast-Aging Port Control Register (Page 00h: Address 89h)".

The VLAN ID fast aging can be enabled by setting the Start/Done of the "Fast-Aging Control Register (Page 00h: Address 88h)", the Fast Age All VID bit of the "Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)" on page 156, and the appropriate VLAN ID bits of the "Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)".

Using the Multiport Addresses

The "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 can be used to forward a given MAC address and Ether Type to multiple ports. Packets with a corresponding DA are forwarded to the port map contained in the "Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174. These registers must be controlled via "Multiport Control Register (Page 04h: Address 0Eh–0Fh)" on page 172.

Note: The "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" is the only mechanism for TS Protocol qualification for the BroadSync HD application. It can be enabled by "Multiport Control Register (Page 04h: Address 0Eh–0Fh)".

Section 3: System Functional Blocks

Overview

The BCM53118 include the following blocks:

- "Media Access Controller" on page 66
- "Integrated 10/100/1000 PHY" on page 68
- "Frame Management" on page 77
- "MIB Engine" on page 80
- "Integrated High-Performance Memory" on page 87
- "Switch Controller" on page 87

Each of these is discussed in more detail in the following sections.

Media Access Controller

The BCM53118 contains six 10/100/1000 GMACs, and one MAC.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3-, IEEE 802.3u-, and IEEE 802.3x-compliant.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than the standard maximum frame size or 9,720 bytes for jumbo-enabled ports.

Note: Frames longer than standard max frame size which configured via "Standard Max Frame Size Register (Page 40h: Address 05h)" on page 250 are considered oversized frames. When jumbo-frame mode is enabled, only the frames longer than 9,720 bytes are bad frames and dropped.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled by writing to "Port Traffic Control Register (Page 00h: Address 00h)" on page 141.

Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In 10/100 Mbps half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted, and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame, and the 96-bit times of IPG have been observed. Transmit functions can be disabled by writing to “Port Traffic Control Register (Page 00h: Address 00h)” on page 141.

Flow Control

The BCM53118 implement an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port’s speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53118 initiate flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes.

10/100 Mbps Half-Duplex

In 10/100 half-duplex mode, the MAC back-pressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

10/100/1000 Mbps Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM53118 are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner flow control (IEEE 802.3x) capability. See Table 11 for detailed information.

Table 11: Flow Control Modes

Link Partner Flow Control (IEEE 802.3x)	*Control Input ENFDXFLOW*	*Control Input ENHDXFLOW*	*Auto-negotiated Link Speed*	*Flow Control Mode*
X	X	0	Half-duplex	Disabled
X	X	1	Half-duplex	Jam pattern
0	0	X	Full-duplex	Disabled
0	1	X	Full-duplex	Disabled
1	0	X	Full-duplex	Disabled
1	1	X	Full-duplex	IEEE 802.3x flow control

Integrated 10/100/1000 PHY

There are eight integrated PHY blocks in the BCM53118. For more information see "Copper Interface" on page 89. The following sections describe the operations of the internal PHY block.

Encoder

There are eight integrated PHY blocks in the BCM53118. The PHY is the Ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface, which performs the reverse process on data received at the MDI interface. The registers of the PHY are read via the "Programming Interfaces" on page 92. The following sections describe the operations of the internal PHY block. For more information, see "Copper Interface" on page 89.

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM53118 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in "Stream Cipher" on page 71. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM53118 simultaneously transmits and receives a continuous data stream on all 4 pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn-to-zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM53118 asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails, or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. Decoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM53118 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

Cross Talk Canceler

The BCM53118 transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125-MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25-MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25-MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM53118 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and therefore, produces very low noise transmit signals.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit non-repeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53118 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM53118 detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM53118 is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM53118 has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM53118) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable.
- Polarity errors caused by the swapping of wires within a pair.

The BCM53118 also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM53118 can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Automatic MDI Crossover

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53118 can perform an automatic media-dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM53118 normally transmits and receives on the TRD pins.

When connecting to another device that does not perform MDI crossover, the BCM53118 automatically switches its TRD in pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM53118 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function cannot be disabled when in 1000BASE-T mode. During 10BASE-TX and 100BASE-T operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation by writing to the "PHY Extended Control Register (Page 10h–17h: Address 20h)" on page 198, bit 14=1.

Note: This function only operates when the copper auto-negotiation is enabled.

10/100BASE-TX Forced Mode Auto-MDIX

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for at least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Tx idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4.

Note: This function only operates when the copper auto-negotiation is disabled.

Resetting the PHY

The BCM53118 provides a hardware reset pin, RESET, which resets all internal nodes to a known state. Hardware reset is accomplished by holding the RESET pin low for at least 1 ms. Once RESET is brought high, the PHY will complete its reset sequence within 5 ms. All outputs will be inactive until the PHY has completed its reset sequence. The PHY will keep the inputs inactive for 5 ms after the de-assertion of hardware reset. The hardware configuration pins and the PHY address pins will be read on the de-assertion of hardware reset.

The BCM53118 also has a software reset capability. To enable the software reset, a 1 must be written to the bit. This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit. Mode pins that are labelled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for the SOR mode pins.

PHY Address

The BCM53118 has eight unique PHY addresses for MII management of the internal PHYs. The PHY addresses for each port are as follows,

- PHY address for Port 0 is 0
- PHY address for Port 1 is 1
- PHY address for Port 2 is 2
- PHY address for Port 3 is 3
- PHY address for Port 4 is 4
- PHY address for Port 5 is 5
- PHY address for Port 6 is 6
- PHY address for Port 7 is 7

Super Isolate Mode

When in Super Isolate mode, the transmit and receive functions on the Copper Media Dependent Interface are disabled (No link will be established with the PHY's copper link partner). Any data received from the switch will be ignored by the BCM53118 and no data will be sent from the BCM53118.

Standby Power-Down Mode

The BCM53118 can be placed into standby power-down mode using software commands. In this mode, all PHY functions except for the serial management interface are disabled. To enter standby power-down mode, set MII Control register (Page 10h–17h: Address 00h), bit 11 = 1. There are three ways to exit standby power-down mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control register (Page 10h–17h: Address 00h).
- Assert the hardware $\overline{\text{RESET}}$ pin.

Read or write operations to any MII register, other than MII Control register, while the device is in the standby power-down mode returns unpredictable results. Upon exiting standby power-down mode, the BCM53118 remains in an internal reset state for 40 µs and then resumes normal operation.

Auto Power-Down Mode

The BCM53118 can be placed into auto power-down mode. Auto power-down mode reduces device power when the signal from the copper link partner is not present. The auto power-down mode works whether the device is in Auto-negotiation Enabled or Forced mode. This mode is enabled by setting bit 5 =1 of Auto Power-Down register. When auto power-down mode is enabled, the BCM53118 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the BCM53118 is in auto power-down mode, it wakes up after 2.7s or 5.4s, which determined by bit 4 of Auto Power-Down register, and sends link pulses while monitoring for energy from the link partner. The BCM53118 enters normal operation and establishes a link if energy is detected, otherwise the wake-up mode continues for a duration of 84 ms to 1260 ms. This is determined by the timer bits [3:0] of Auto Power-Down register. before going back to low-power mode.

External Loopback Mode

The External Loopback mode allows in-circuit testing of the BCM53118 as well as the transmit path through the magnetics and the RJ-45 connector. External loopback can be performed with and without a jumper block. External loopback with a jumper block tests the path through the magnetics and RJ-45 connector. External loopback without the jumper block only tests the BCM53118’s transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1------------3
2------------6
4------------7
5------------8

The following six tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 12: 1000BASE-T External Loopback With External Loopback Plug

Register Writes	Comments
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode
Write 0040h to MII Control register	Enable Force 1000BASE-T
Write 8400h to Auxiliary Control register	Enable External Loopback Mode with external loopback plug

Table 13: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	Comments
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode
Write 0040h to MII Control register	Enable Force 1000BASE-T
Write 8400h to Auxiliary Control register	Enable External Loopback Mode
Write 0014h to Auxiliary Control register	Enable External Loopback Mode without external loopback plug

Table 14: 100BASE-TX External Loopback With External Loopback Plug

Register Writes	Comments
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode

Table 15: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	Comment
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode
Write 0014h to Auxiliary Control register	Enable external loopback mode without external loopback plug

Table 16: 10BASE-T External Loopback With External Loopback Plug

Register Writes	***Comments***
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode

Table 17: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	***Comments***
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode
Write 0014h to Auxiliary Control register	Enable external loopback mode without external loopback plug

Note: To exit the External Loopback mode, a software or hardware reset is recommended.

Full-Duplex Mode

The BCM53118 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

Copper Mode

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of MII Control register.

When auto-negotiation is enabled, the full-duplex capability is advertised for:

- 10BASE-T when bit 6 of "Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h)" on page 190 is set.
- 100BASE-T when bit 8 "Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h)" is set.
- 1000BASE-T when bit 9 of "1000BASE-T Control Register (Page 10h–17h: Address 12h)" on page 195 is set.

Master/Slave Configuration

In 1000BASE-T mode, the BCM53118 and its link partner perform loop timing. One end of the link must be configured as the timing master, and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. Each end generates an 11-bit random seed if the two settings are equal, and the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM53118 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted. This is used to set the BCM53118 to manual master/slave configuration or to set the advertised repeater/DTE configuration.

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM53118 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM53118 is configured to advertise 1000BASE-T capability.

The BCM53118 also supports software controlled Next Page exchanges. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM53118 automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM53118 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM53118 is not configured to advertise 1000BASE-T capability and bit 15 of the "Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h)" on page 190 is set, the BCM53118 does not advertise Next Page ability.

Frame Management

The BCM53118 provides a Frame Management block that works in conjunction with one of the GMII ports operate in IMP mode as the full duplex packet streaming interface to the external CPU, with in-band messaging mechanism for management purpose.

In-Band Management Port

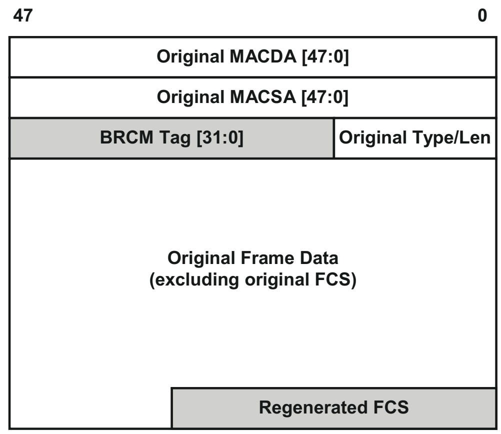
The GMII port can be configured as the management port, using the Frame Management Port bits in the "Global Management Configuration Register (Page 02h: Address 00h)" on page 162. When the GMII port is defined as the Frame Management Port, it is referred to as the in-band management port (IMP).

The IMP can be used as a full-duplex 10/100/1000 Mbps port, which can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system.

As IMP is defined as the frame management port, normal frame data is forwarded to the port based on the state of the RX_UCST_EN, RX_MCST_EN and RX_BCST_EN bits in the "IMP Port Control Register (Page 00h: Address 08h)" on page 142. If these bits are cleared, no frame data will be forwarded to the Frame Management Port, with the exception that frames meeting the mirror ingress/egress rules criteria, will always be forwarded to the designated frame management port.

Packets transferred over the IMP port are tagged with the Broadcom proprietary header to carry the necessary information which is of interest to the management entity running on the CPU, as shown below, except for the PAUSE frame. The IMP port must support normal Ethernet pause based flow control mechanism.

Figure 10: IMP Packet Encapsulation Format



The BRCM tag is designed for asymmetric operation across the IMP port. The information carried from the switching device to the CPU is different from the information carried from the CPU to the switching device.

Similarly, the host system must insert the BRCM tag fields into frames it wished to send into the management port, to be routed to specific egress ports. The OPCODE within the tag field determines how the frame is handled, and allows frames to be forwarded using the normal address lookup via a port ID designation within the Tag.

The BRCM tag are transmitted with the convention of highest significant octet first, followed by the next lowest significant octet, and so on, with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM tag field in Table 18, the most significant octet would be transmitted first (bits [24:31]), with bit 24 being the first bit transmitted.

Broadcom Tag Format For Egress Packet Transfer

When a packet is forwarded by the switching device to the external CPU for processing, the BRCM tag is formatted as shown below.

Table 18: Egress Broadcom Tag Format (IMP to CPU)

31–29	***28–24***	***23–16***	***15–8***	***7–5***	***4–0***
OPCODE=000	Reserved	Reserved	REASON_CODE[7:0]	TC[2:0]	SRC_PID[4:0]
63–61	***60–38***			***37***	***36–32***
OPCODE=001	Reserved			T/R	T/R_PID[4:0]
31–0					
TIME_STAMP[31:0]					

- OPCODE 000

  This indicates the packet transfer with explicit reasons to help the external CPU to direct the packet for the appropriate packet processing entities.

- REASON_CODE [7:0]

  This indicates the reasons why the packet is forwarded to the external CPU so that the CPU can identify the appropriate software routines for packet processing.
  - Bit [0] indicates mirroring
  - Bit [1] indicates SA learning
  - Bit [2] indicates switching
  - Bit [3] indicates protocol termination
  - Bit [4] indicates protocol snooping
  - Bit [5] indicates flooding/exception processing
  - Bit [6] and Bit[7] are reserved
- TC [2:0]

  This indicates the traffic class classified by the switching device when forwarding the packet to the CPU.
- SRC_PID [4:0]

  This indicates the ingress port of the switching device where the packet is received.
- OPCODE 001

  This indicates a packet transfer with explicit time stamp recorded at the port where it was transmitted or received (indicated by the T/R_PID) for IEEE 802.1as protocol implementation.
- T/R

  This indicates the type of time stamp. 0 indicates the time stamp recorded when the packet was received through the port (indicated by the T/R_PID); 1 indicates the time stamp recorded when the packet was transmitted through the port (indicated by the T/R_PID).
- T/R_PID [4:0]

  This indicates the port through which the packet was transmitted when T/R = 1, or the port through which the packet was received when T/R = 0.
- TIME_STAMP [31:0]

  This carries the time stamp value recorded at the ingress port for a received TS protocol packet.

Broadcom Tag Format For Ingress Packet Transfer

For packet transfer from the external CPU to the switching device, the BRCM tag is formatted as shown below.

Table 19: Ingress BRCM Tag (CPU to IMP)

<table>
<tr><th>31–29</th><th>28–26</th><th>25–24</th><th colspan="2">23–0</th></tr>
<tr><td>OPCODE=000</td><td>TC[2:0]</td><td>TE[1:0]</td><td colspan="2">Reserved</td></tr>
<tr><th>31–29</th><th>28–26</th><th>25–24</th><th>23</th><th>22–0</th></tr>
<tr><td>OPCODE=001</td><td>TC[2:0]</td><td>TE[1:0]</td><td>TS</td><td>DST_MAP[22:0]</td></tr>
</table>

- OPCODE 000

  It indicates that the external CPU is not dictating how the packet is forwarded, and the packet is forwarded by the switching device based on the original Ethernet packet information.

- OPCODE 001

  This indicates the packet is forwarded to multiple (or single) egress ports by the switching device based on the explicit direction of the external CPU.
- DST_MAP [22:0]

  This indicates the egress port bit map to which the external CPU intends to forward the packet.
- TC [2:0]

  This indicates the traffic class with which the external CPU intends to forward the packet.
- TS (time stamp request)

  This indicates whether the transmit time stamped at the egress port should be reported back to the external CPU.
- TE (tag enforcement)

  This indicates the 802.1Q/P tagging/untagging encapsulation enforcement for the packet transmission.

  00: No enforcement (follow VLAN untag mask rules)

  01: Untag enforcement

  10: Tag enforcement

  11: Reserved

MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53118 implement 70-plus MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. This latter group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The section below describes each individual counter.

The BCM53118 offers the MIB snapshot feature per port enabled via "Page 70h: MIB Snapshot Control Register" on page 264. A snapshot of a selected port MIB registers can be captured and available to the users while MIB counters are continuing to count.

If bit[7:6] = 10 of "Page 70h: MIB Snapshot Control Register", the captured snapshot MIB counters can be read from "Page 71h: Port Snapshot MIB Control Register" on page 264 after bit 7 of "Page 70h: MIB Snapshot Control Register" is cleared to 0. Registers in "Page 20h–28h: Port MIB Registers" on page 221 can be read for live counter.

If bit[7:6] = 11 of "Page 70h: MIB Snapshot Control Register", the captured snapshot MIB counters can be read from "Page 71h: Port Snapshot MIB Control Register" or "Page 20h–28h: Port MIB Registers" (depending on which port is captured) after bit 7 of "Page 70h: MIB Snapshot Control Register" is cleared to 0. The live counters cannot be read.

MIB Counters Per Port

Receive Only Counters (19)	Description of Counter

RxDropPkts (32 bit)	The number of good packets received by a port that were dropped due to a lack of resources (e.g., lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters.
RxOctets (64 bit)	The number of data bytes received by a port (excluding preamble, but including FCS), including bad packets.
RxBroadcastPkts (32 bit)	The number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed.
RxMulticastPkts (32 bit)	The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed.
RxSAChanges (32 bit)	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed.
RxUndersizePkts (32 bit)	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).
RxOversizePkts (32 bit)	The number of good packets received by a port that are greater than standard max frame size. The maximum packet size can be programmed.
RxFragments (32 bit)	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
RxJabbers (32 bit)	The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.
RxUnicastPkts (32 bit)	The number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed.
RxAlignmentErrors (32 bit)	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a non-integral number of bytes.
RxFCSErrors (32 bit)	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets (64 bit)	The total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed.
JumboPktCount (32 bit)	The number of good packets received by a port that are greater than the standard maximum size and less than or equal to the jumbo packet size, regardless of CRC or alignment errors.

RxPausePkts (32 bit)	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88–08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00–01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a non-compliant transmitting device on the network.
RxSymbolErrors (32 bit)	The total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event.
RxDiscard (32 bit)	The number of good packets received by a port that were discarded by the Forwarding Process.
InRangeErrors (32 bit)	The number of packets received with good CRC and one of the following: (1) The value of length/type field is between 46 and 1500 inclusive, and does not match the number of (MAC client data + PAD) data octets received, OR (2) The value of length/type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).
OutOfRangeErrors (32 bit)	The number of packets received with good CRC and the value of length/type field is greater than 1500 and less than 1536.
Transmit Counters Only (18)	**Description of Counter**
TxDropPkts (32 bit)	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.
TxOctets (64 bit)	The total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts (32 bit)	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts (32 bit)	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions (32 bit)	The number of collisions experienced by a port during packet transmissions.
TxUnicastPkts (32 bit)	The number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision (32 bit)	The number of packets successfully transmitted by a port that have experienced exactly one collision.
TxMultipleCollision (32 bit)	The number of packets successfully transmitted by a port that have experienced more than one collision.
TxDeferredTransmit (32 bit)	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. This only applies to the Half Duplex mode, while the Carrier Sensor Busy.

TxLateCollision (32 bit)	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxPausePkts (32 bit)	The number of PAUSE events at each port.
TxFrameInDisc (32 bit)	The number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM53118 internal flow-control/buffering scheme has been configured incorrectly.
TxQ0PKT(32 bit)	The total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.
TxQ1PKT(32 bit)	The total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.
TxQ2PKT(32 bit)	The total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.
TxQ3PKT(32 bit)	The total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.
TxQ4PKT(32 bit)	The total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.
TxQ5PKT(32 bit)	The total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.
Transmit or Receive Counters (6)	**Description of Counter**
Pkts64Octets (32 bit)	The number of packets (including error packets) that are 64 bytes long.
Pkts65to127Octets (32 bit)	The number of packets (including error packets) that are between 65 and 127 bytes long.
Pkts128to255Octets (32 bit)	The number of packets (including error packets) that are between 128 and 255 bytes long.
Pkts256to511Octets (32 bit)	The number of packets (including error packets) that are between 256 and 511 bytes long.
Pkts512to1023Octets (32 bit)	The number of packets (including error packets) that are between 512 and 1023 bytes long.
Pkts1024toMaxPktOctets (32 bit)	The number of packets that (include error packets) are between 1024 and the standard maximum packet size inclusive.

Total number of counters per port: 43

Table 20 on page 84 identifies the mapping of the BCM53118 MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs that are supported. Direct mappings are defined. However, there are several additional statistics counters, which are indirectly supported that make up the full complement of the counters required to fully support each MIB. These are shown in Table 21 on page 86.

Finally, Table 22 on page 86 identifies the additional counters supported by the BCM53118 and references the specific standard or reason for the inclusion of the counter.

Table 20: Directly Supported MIB Counters

BCM53118 MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
RxDropPkts	dot3StatsInternalMACReceiveErrors	dot1dTpPortInDiscards	ifInDiscards	–
RxOctets	–	–	ifInOctets	etherStatsOctets
RxBroadcastPkts	–	–	ifInBroadcastPkts	etherStatsBroadcastPkts
RxMulticastPkts	–	–	ifInMulticastPkts	etherStatsMulticastPkts
RxSAChanges	Note 2	Note 2	Note 2	Note 2
RxUndersizePkts	–	–	–	etherStatsUndersizePkts
RxOversizePkts	dot3StatsFrameTooLongs	–	–	etherStatsOverrsizePkts
RxFragments	–	–	–	eytherStatsFragments
RxJabbers	–	–	–	etherStatsJabbers
RxUnicastPkts	–	–	ifInUcastPkts	–
RxAlignmentErrors	dot3StatsAlignmentErrors	–	–	–
RxFCSErrors	dot3StatsFCSErrors	–	–	–
RxGoodOctets	–	–	–	–
RxExcessSizeDisc	Note 2	Note 2	Note 2	Note 2
RxPausePkts	Note 2	Note 2	Note 2	Note 2
RxSymbolErrors	Note 2	Note 2	Note 2	Note 2
Note 1	–	–	ifInErrors	–
Note 1	–	–	ifInUnknownProtos	–
Note 1	–	dot1dTpPortInFrames	–	–
TxDropPkts	dot3StatsInternal MACTransmitErrors	–	ifOutDiscards	–
TxOctets	–	–	ifOutOctets Note 3	–
Note 1	–	dot1dTpPortOutFrames	–	–
TxBroadcastPkts	–	–	ifOutBroadcastPkts	–
TxMulticastPkts	–	–	ifOutMulticastPkts	–
TxCollisions	–	–	–	etherStatsCollisions
TxUnicastPkts	–	–	ifOutUcastPkts	–
TxSingleCollision	dot3StatsSingle CollisionFrames	–	–	–
TxMultipleCollision	dot3StatsMultiple CollisionFrames	–	–	–

Table 20: Directly Supported MIB Counters (Cont.)

BCM53118 MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
TxDeferredTransmit	dot3StatsDeferred Transmissions	–	–	–
TxLateCollision	dot3StatsLate Collision	–	–	–
TxExcessiveCollision	dot3StatsExcessive Collision	–	–	–
TxFrameInDisc	Note 2	Note 2	Note 2	Note 2
TxPausePkts	Note 2	Note 2	Note 2	Note 2
Note 4	dot3StatsCarrier SenseErrors	–	–	–
Note 1	–	–	ifOutErrors	–
Pkts64Octets	–	–	–	etherStatsPkt64 Octets
Pkts65to127Octets	–	–	–	etherStatsPkt65to 127Octets
Pkts128to255Octets	–	–	–	etherStatsPkt128to 255Octets
Pkts256to511Octets	–	–	–	etherStatsPkt256to 511Octets
Pkts512to1023Octets	–	–	–	etherStatsPkt512to 1023Octets
Pkts1024toMaxPkt Octets	–	–	–	etherStatsPkt1024to MaxPktOctets
Note 1	–	–	–	etherStatsDrop Events
Note 1	–	–	–	etherStatsPkts
Note 1	–	–	–	etherStatsCRCAlign Errors
Note 4	dot3StatsSQETest Errors	–	–	–

Note 1: Derived by summing two or more of the supported counters. See Table 21 on page 86 for specific details.

Note 2: Extensions required by recent standards developments or BCM53118 operation specifics.

Note 3: The MIB II interfaces specification for if OutOctets includes preamble/SFD and errored bytes. Because IEEE 802.3-compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets counter maintained by the BCM53118 is consistent with good bytes transmitted, excluding preamble, but including FCS. The count can be adjusted to more closely match the if OutOctets definition by adding the preamble for TxGoodPkts and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.

Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM53118. These attributes were originally defined to support coax-based AUI transceivers. The BCM53118 integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 (not supported).

Table 21: Indirectly Supported MIB Counters

BCM53118 MIB	***Ethernet-Like MIB RFC 1643***	***Bridge MIB RFC 1493***	***MIB II Interface RFC 1213/1573***	***RMON MIB RFC 1757***
RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers	–	–	ifInErrors	–
	–	–	ifInUnknownProtos	–
RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts	–	dot1dTpPortIn Frames	–	–
DropEvents = RxDropPkts + TxDropPkts	–	–	–	etherStatsDrop Events
RxTotalPkts = RxGoodPkts + RxErrorPkts	–	–	–	etherStatsPkts
RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors	–	–	–	etherStatsCRCAlign Errors
–	dot3StatsSQETest Errors	–	–	–
RxFramesTooLong = RxOversizePkts + RxJabber	dot3StatsFrameToo Longs	–	–	–
TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts	–	dot1dTpPortOut Frames	–	–
TxErrorPkts = TxExcessiveCollision + TxLateCollision Note 1	–	–	ifOutErrors	–

Note 1: The number of packets transmitted from a port that experienced a late collision or excessive collisions. While some media types operate in half-duplex mode, frames that experience carrier sense errors are also summed in this counter. The BCM53118 integrated design means this error condition is eliminated.

Table 22: BCM53118 Supported MIB Extensions

BCM53118 MIB	***Appropriate Standards Reference***
RxSAChanges	IEEE 802.3u Clause 30—Repeater Port Managed Object Class a SourceAddressChanges.

Table 22: BCM53118 Supported MIB Extensions (Cont.)

BCM53118 MIB	Appropriate Standards Reference
RxExcessSizeDisc	The BCM53118 cannot store packets in excess of 1536 bytes (excluding preamble/ SFD, but inclusive of FCS). This counter indicates packets that were discarded by the BCM53118 due to excessive length.
RxPausePkts	IEEE 802.3x Clause 30—PAUSE Entity Managed Object Class aPAUSEMACCtrlFramesReceived.
RxSymbolErrors	IEEE 802.3u Clause 30—Repeater Port Managed Object Class aSymbolErrorDuringPacket.
TxFrameInDisc	Internal diagnostic use for optimization of flow control and buffer allocation algorithm.
TxPausePkts	The number of PAUSE events at a given port.

Integrated High-Performance Memory

The BCM53118 embed a 192 KB high-performance SRAM for storing packet data. This eliminates the need for external memory and allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance for stand-alone 8-port applications.

Switch Controller

The core of the BCM53118 devices is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully non-blocking solution.

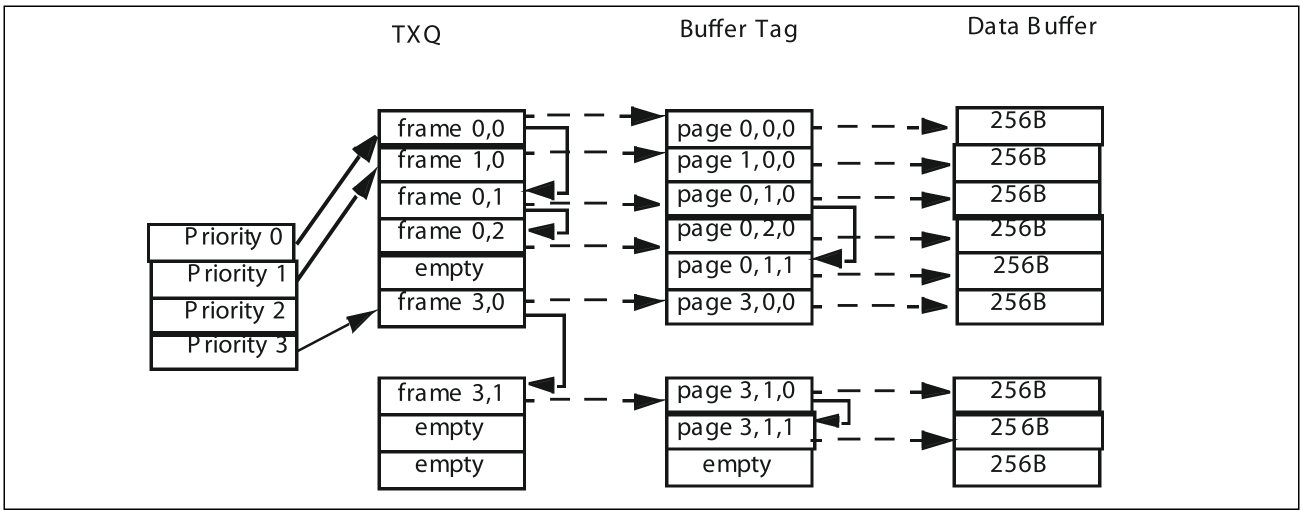
Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see Figure 11). The first level is the TXQ linked list, and the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame TC order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to six transmit queues for servicing Quality of Service (QoS). All six transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as a linked list, and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 9720-byte jumbo frame requires 38 buffer tags for handling the frame.

Figure 11: TXQ and Buffer Tag Structure



Section 4: System Interfaces

Overview

The BCM53118 include the following interfaces:

- "Copper Interface" on page 89
- "Frame Management Port Interface" on page 90
- "Configuration Pins" on page 91
- "Programming Interfaces" on page 92
- "MDC/MDIO Interface" on page 109
- "LED Interfaces" on page 116

Each interface is discussed in detail in these sections.

Copper Interface

The internal PHYs transmit and receive data via the analog copper interface. This section discusses the following topics:

- "Auto-Negotiation" on page 89
- "Lineside (Remote) Loopback Mode" on page 90
- "Reverse MII Port (RvMII)" on page 90
- "GMII Port" on page 91
- "RGMII Port" on page 91
- "SPI-Compatible Programming Interface" on page 92
- "EEPROM Interface" on page 106
- "MDC/MDIO Interface Register Programming" on page 109
- "Pseudo-PHY" on page 110

Auto-Negotiation

The BCM53118 negotiate a mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the BCM53118 automatically choose the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53118 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be disabled by software control, but is required for 1000BASE-T operation.

Lineside (Remote) Loopback Mode

The lineside loopback mode allows the testing of the copper interface from the link partner. This mode is enabled by setting bit 15 of the Miscellaneous Test register. The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the internal MAC interface.

Frame Management Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see “Frame Management” on page 77. The port is configurable to Reverse MII (RvMII), GMII, or RGMII via strap pins or software configuration.

MII/TMII Interface

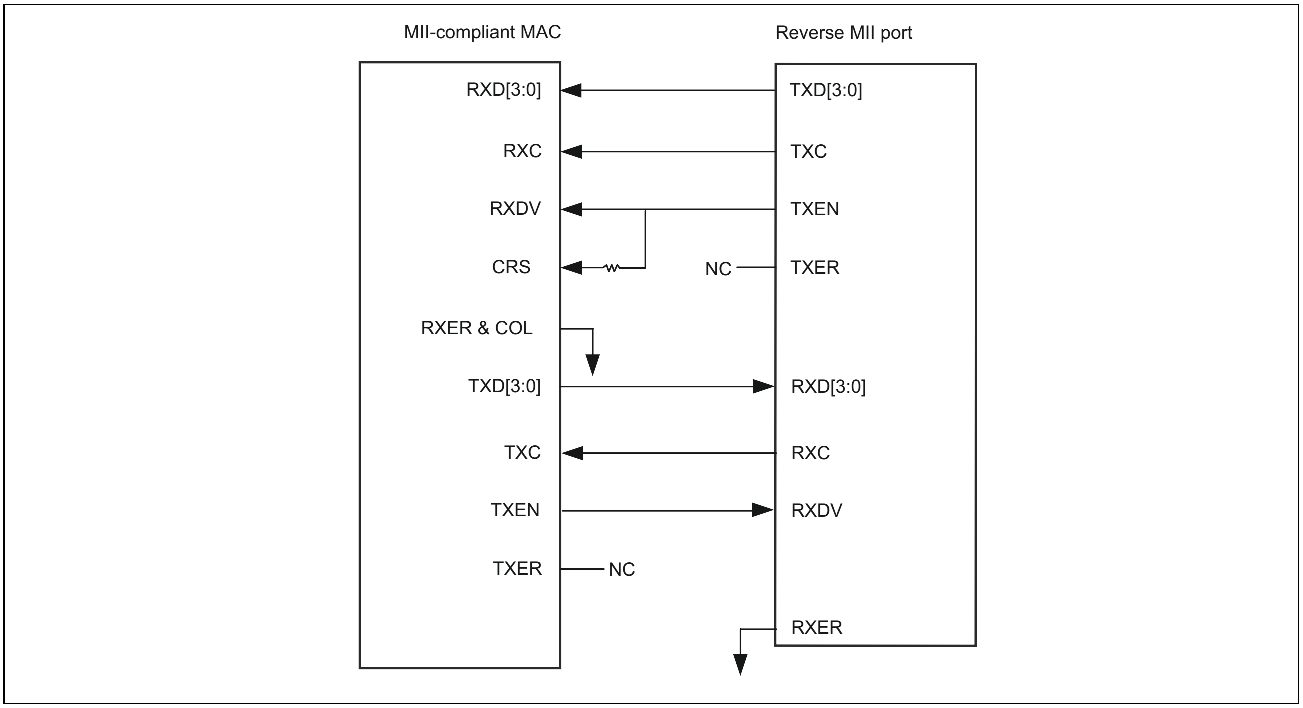
The BCM53118 provides a fully IEEE 802.3u compatible MII interface. This interface can run at the standard 100 Mbps speed with 25 MHz clocks from the link partner, or it can run at 200 Mbps with 50 MHz clocks from an external source.

Note: Reverse TMII (RvTMII) is not supported by the BCM53118 device.

Reverse MII Port (RvMII)

The media independent interface (MII) serves as a digital data interface between the BCM53118 and an external 10/100 Mbps management entity. Reverse MII notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 100 Mbps and 10 Mbps for both full-duplex and half-duplex operation. See Figure 12 for connection information.

Figure 12: RvMII Port Connection



GMII Port

The Gigabit Media Independent Interface (GMII) serves as a digital data interface between the BCM53118 and an external gigabit management entity. Transmit and receive data is clocked on the rising edge of the clocks. The GMII transmits data synchronously via the TXD[7:0] and RXD[7:0] data signals.

RGMII Port

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM53118 and an external gigabit management entity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits data synchronously via the TXD[3:0] and RXD[3:0] data signals.

Configuration Pins

Initial configuration of the BCM53118 takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes, and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration. See “Signal Descriptions” on page 123 for more information.

Programming Interfaces

The BCM53118 can be programmed via the SPI interface or the EEPROM interface. The interfaces share a common pin set that is configured via the CPU_EPROM_SEL strap pin. The "SPI-Compatible Programming Interface" on page 92 provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM53118 register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the "EEPROM Interface" on page 106 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM53118 devices is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

An explanation follows for using the serial interface with an SPI-compatible CPU ("SPI-Compatible Programming Interface" on page 92) or an EEPROM ("EEPROM Interface" on page 106). Either mode can be selected with the strap pin, CPU_EPROM_SEL. Either mode has access to the same register space.

SPI-Compatible Programming Interface

One way to access the BCM53118 internal registers is to use the serial peripheral interconnect (SPI) compatible interface. This four-pin interface is designed to support a fully functional, bi-directional Motorola® serial peripheral interface (SPI) for register read/write accesses. The maximum speed of operation is 2 MHz. The SPI interface shares pins with the EEPROM interface. To select the SPI interface, pull up or float the CPU_EPROM_SEL pin. (The internal pull-up resistor defaults SPI interface over EEPROM interface.)

The SPI is a four-pin interface consisting of:

- Device select ($\overline{SS}$: slave select, input to BCM53118)
- Device clock (SCK: which operates at speeds up to 2 MHz, input to BCM53118)
- Data write line (MOSI: Master Out/Slave In, input to BCM53118)
- Data read line (MISO: Master In/Slave Out, output from BCM53118)

Note: All the RoboSwitch™ SPI interfaces are designed to operate in slave mode. Therefore, the SCK and SS signals are driven by the external master host device when accessing the BCM53118 registers. For more detailed descriptions reader may refer to the *Motorola SPI spec MC68HC08AS20-Rev. 4.0*.

$\overline{SS}$: Slave Select

The $\overline{SS}$ signal is used to select a slave device and to indicate the beginning of transmission. The BCM53118 SPI interface operates in the clock phase one (CPHA = 1) transmission format. In this format, the SS signal is driven active low while the SCK signal is high, and remains low throughout the transmission including multiple-byte transfers. The minimum time requirement between $\overline{SS}$ operation is 200 ns.

SCK: Serial Clock

The serial clock SCK maximum operating frequency is 2 MHz for the BCM53118 family of devices. The SCK is used to clock data into and out of the Slave ROBO device. The SCK signal is expected to remain high when the interface is idle. This is because the BCM53118 SPI design is based on CPOL = 1 (Clock Polarity = 1). This is not programmable on BCM53118. The BCM53118 is designed so that data is driving by the falling edge and sampling by the rising edge of the SCK clock. This clock is not a free-running clock, it is generated only during a data transaction, and remains high when the clock is idle.

MOSI: Master Output Slave Input

The MOSI signal is used by the master device to transmit the data to the slave device. The data is put on the bus and is expected to be clocked in by a rising edge of the SCK clock signal. This line is used to issue a command and to set the register page and address value of read/write operations.

MISO: Master Input Slave Output

The MISO signal is used by the Slave device to output the data to the master device. The data is put on the bus and is expected to be clocked out by a rising edge of the SCK clock signal. This line is used to transmit the status and the content of the register of read operation.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM53118. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM53118 slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. Figure 13 shows the normal SPI command byte, and Figure 14 shows the Fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 13: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 14: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is a 1, bits 7:5 indicate a fast SPI command byte, and bits 7:5 indicate the byte offset into the register that the BCM53118 starts to read from (byte offsets are not supported for write operations).

In command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM53118 operates as a single-chip system, the CHIP ID is 000.

Note: The SS# signal must also be active for any BCM53118 device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Non-contiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The SS signal must remain low for the entire read or write transaction, as shown in Figure 15 and Figure 16, with the transaction terminated by the deassertion of the SS line by the master.

Figure 15: SPI Serial Interface Write Operation

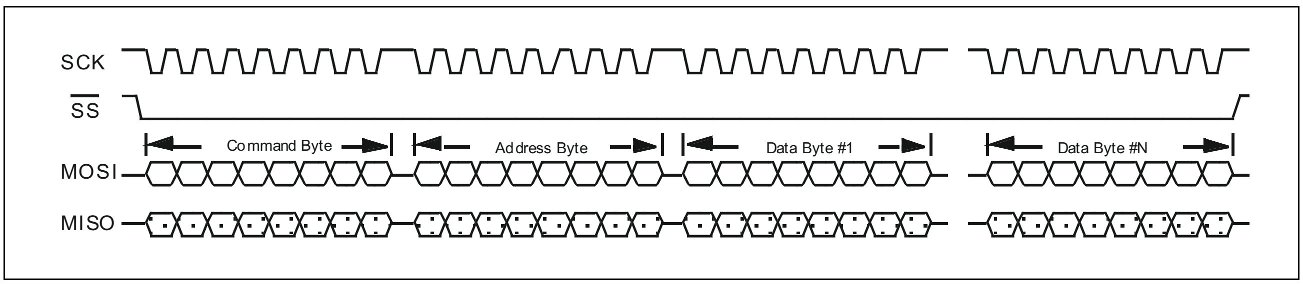
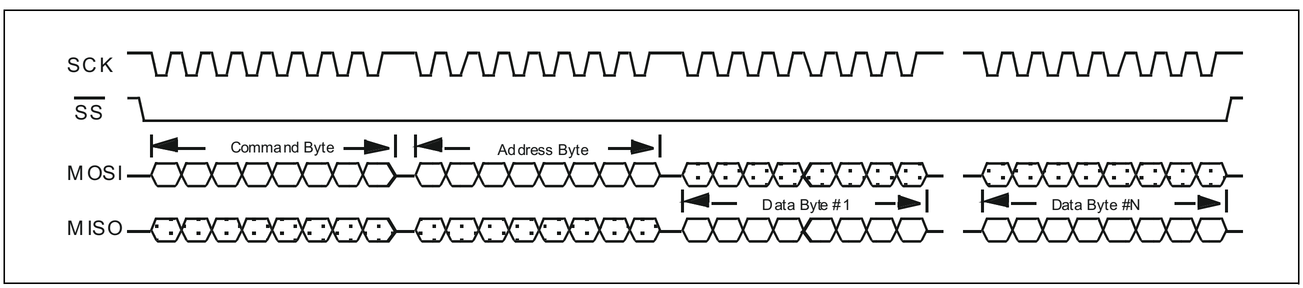


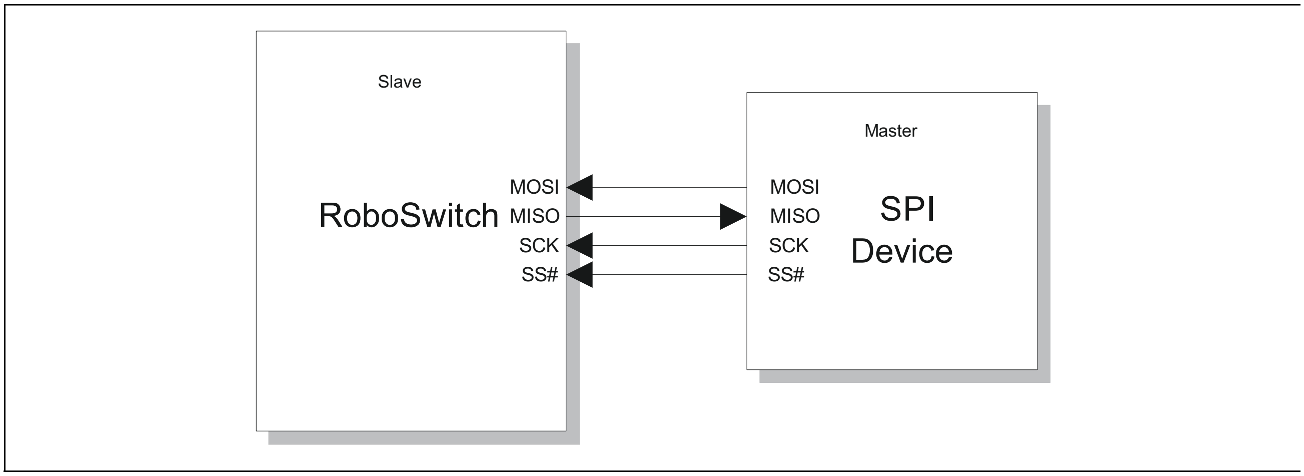
Figure 16: SPI Serial Interface Read Operation



The following diagram shows the typical connection block diagram for SPI interface with/without external PHY devices.

Without External PHY

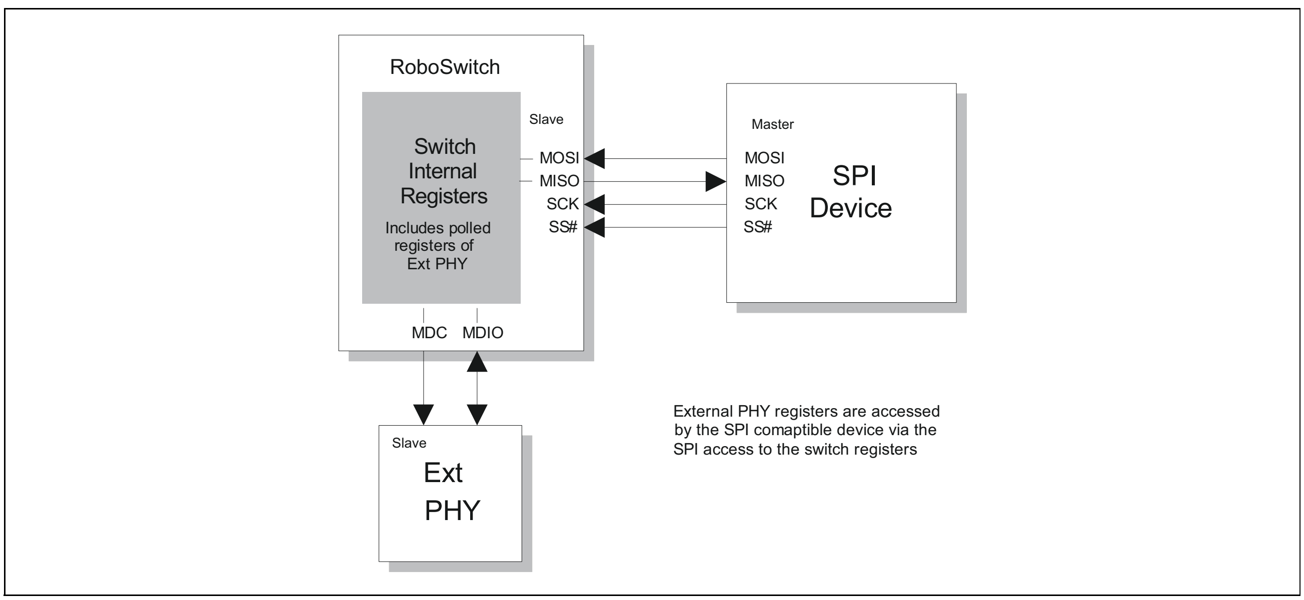
Figure 17: SPI Interface Without External PHY Device



External PHY Registers

The BCM53118 also uses the MDIO/MDC interface for polling registers of an external PHY. In this case, the MDIO/MDC interface polls the external PHY registers pulling the data internal to the BCM53118. Then, the external PHYs and retrieved from the register data using the SPI interface. The MDIO/MDC interface is not used as a method to access internal PHY registers. This must be done via the SPI interface.

Figure 18: Accessing External PHY Registers



Reading and Writing BCM53118 Registers Using SPI

BCM53118 internal register read and write operations are executed by issuing a command followed by multiple accesses of the SPI registers in the BCM53118. There are three SPI interface registers in the BCM53118 that are used by the master device to access the internal switch registers. The SPI interface registers are:

- SPI Page register (page: global, address: FFh): used to specify the value of the specific register pages.
- SPI Data I/O register (page: global, address: F0h): used to write and read the specific register's content.
- SPI Status Register (page: global, address: FEh): used to check for an operation completion.
  - Bit 7: SPIF, SPI read/write complete flag
  - Bit 6: Reserved
  - Bit 5: RACK, SPI read data ready acknowledgement
  - Bit 4:3: Reserved
  - Bit 2: MDIO_Start, Start/Done MDC/MDIO operation
  - Bit 1: Reserved
  - Bit 0: Reserved

The BCM53118 SPI interface supports the following operating modes.

- Normal read mode
- Fast read mode
- Normal write mode

Note: The RoboSwitch family does not support fast-write mode.

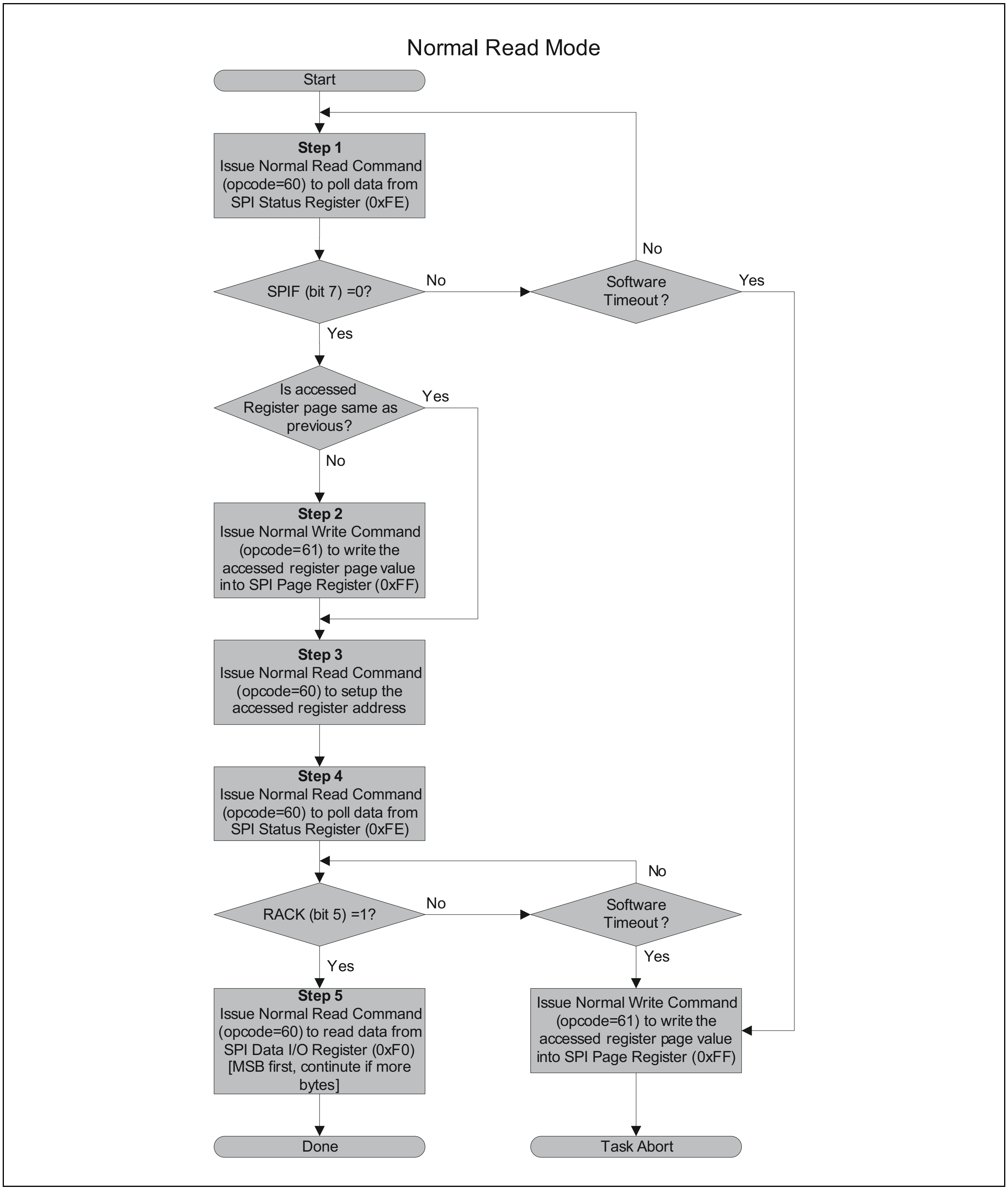
The details of each modes are described in the following paragraphs.

Normal Read Operation

Normal Read operation consists of five transactions (five $\overline{SS}$ operations):

1. Issue a Normal Read Command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a Normal Write command (opcode = 0x61) to write the register page value into the SPI Page register 0xFF.
3. Issue a Normal Read command (opcode = 0x60) to setup the required RoboSwitch register address.
4. Issue a Normal Read command (opcode = 0x60) to poll the RACK bit in the SPI status register(0xFE) to determine the completion of read (register content gets loaded in SPI Data I/O register).
5. Issue a Normal Read command (opcode = 0x60) to read the specific registers' content placed in the SPI Data I/O register (0xF0).

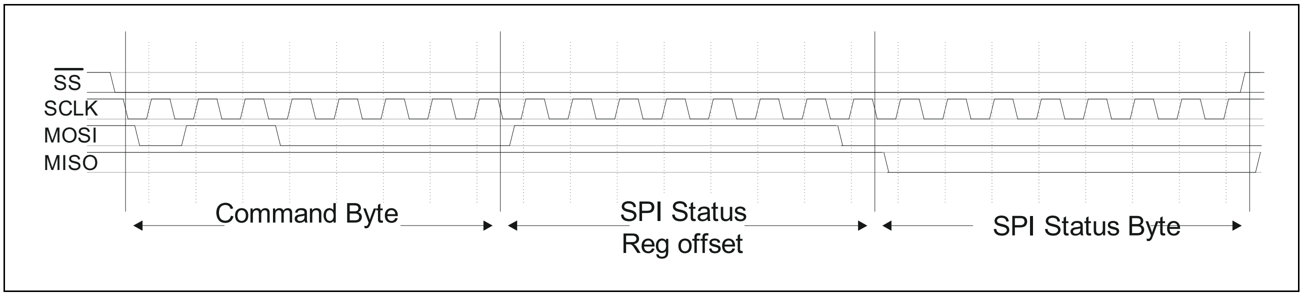
Figure 19: Normal Read Operation



Example: Read from 1000BASE-T Control register (Page 10h, Offset 12h).

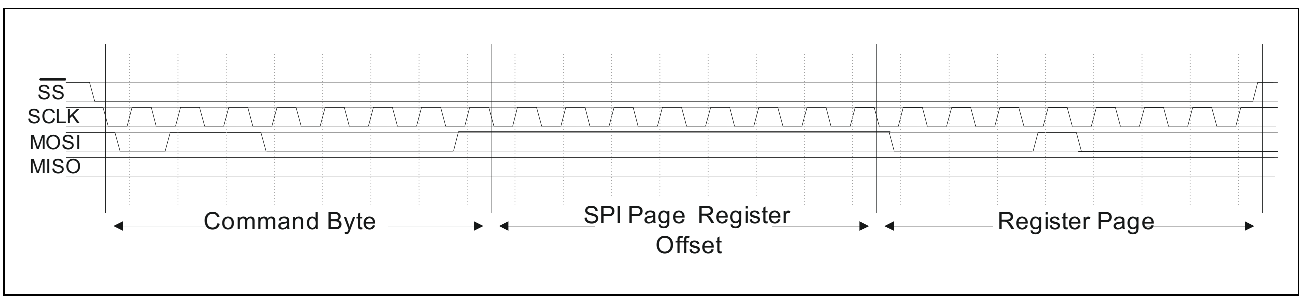
1. Issue a Normal Read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a Normal Read Command Byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
   - Clock in the SPI Status register address (0xFE)
   - Clock out the SPI Status register value: 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
   - Deassert $\overline{SS}$ while SCK is high idle state

Figure 20: Normal Read Mode to Check the SPIF Bit of SPI Status Register



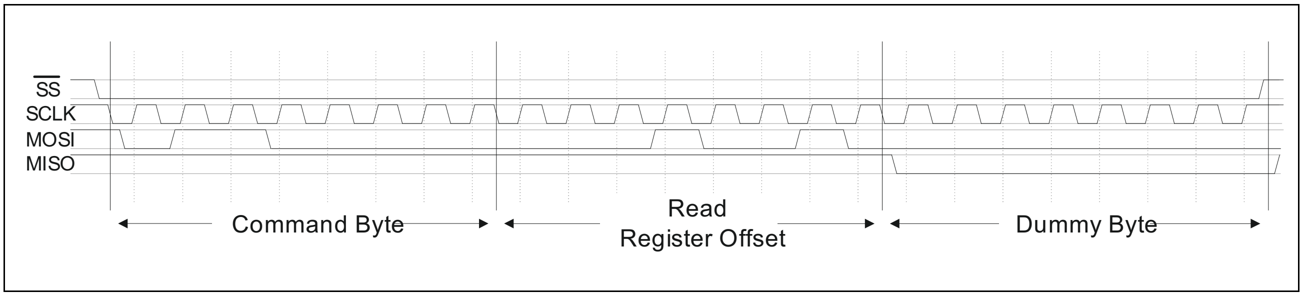
2. Issue a Normal Write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI Page Reigster(0xFF) —this step is required only if previous read/write was not to/from Page 10h.
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a Normal Write Command Byte: 0 1 1 0 0 0 0 1 (opcode = 0x61)
   - Clock in offset of Page register (0xFF)
   - Clock in the accessed register page value,: 0 0 0 1 0 0 0 0 (Page register: 0x10)
   - Deassert $\overline{SS}$ while SCK is high idle state

Figure 21: Normal Read Mode to Setup the Accessed Register Page Value



3. Issue a Normal Read command (opcode = 0x60) and write the accessed register address value 0x12, and clock out 8 bits to complete the read cycle, but discard result (this is where the state machine triggers a internal data transfer from Address 0x12 to the SPI Data I/O register)
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a Normal Read Command Byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
   - Clock in the address of accessed register address value (0x12)
   - Clock out eight clocks for the dummy read, and discard results on MISO
   - Deassert $\overline{SS}$ while SCK is high idle state

Figure 22: Normal Read Mode to Setup the Accessed Register Address Value (Dummy Read)

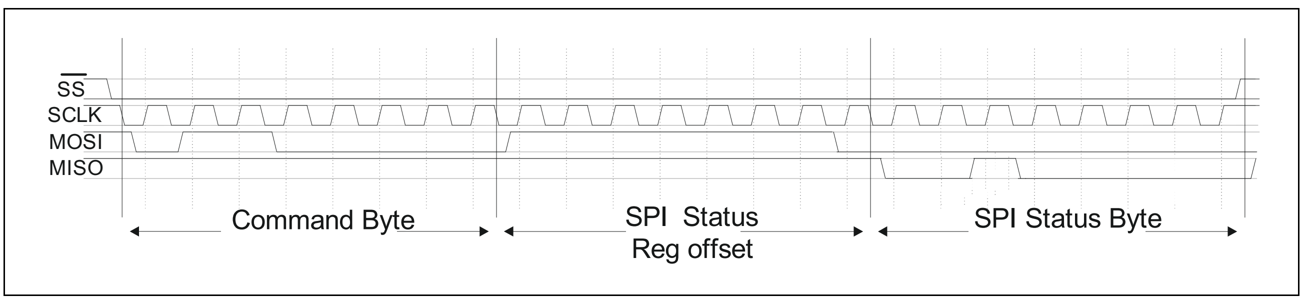


Note: This dummy read is always eight clock cycles, whether or not it is an 8-bit register.

4. Issue a Normal Read command (opcode = 0x60) to read the SPI Status to check the RACK bit for completion of the register content transfer to the SPI Data I/O register.(this step may be repeated until the proper bit set is read.)

- Assert SS while SCK is high idle state
- Clock in a Normal Read Command Byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in offset for SPI Status Register (0xFE): 1 1 1 1 1 1 1 0
- Clock out the content of SPI Status bits
- Repeat the polling until the content of SPI Status Register value: 0 0 1 0 0 0 0 0 (RACK bit 5 = 1)
- Deassert SS while SCK is high idle state

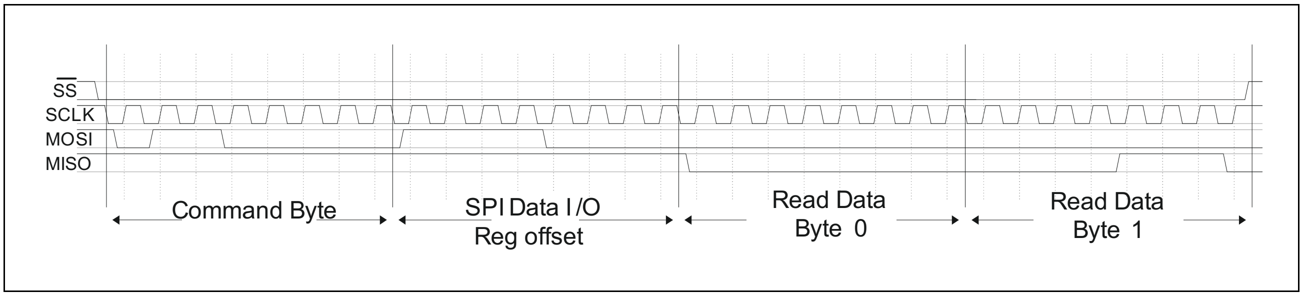
Figure 23: Normal Read Mode to Check the SPI Status for Completion of Read



5. Issue a Normal Read command (opcode = 0x60) to read the data from the SPI Data I/O register:

- Assert SS while SCK is high idle state
- Clock in Command Byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in offset of SPI Data I/O Register (0xF0)
- Clock out first data byte on MISO line: 0 0 0 0 0 0 0 0 (Byte 0: Bit 7 to Bit 0: MSB to LSB)
- Clock out next byte (in this case, last) on MISO line: 0 0 0 0 1 1 1 0 (Byte 1: Bit 15 to Bit 8)
- [Continue if more bytes]
- Deassert SS while SCK is high idle state

Figure 24: Normal Read Mode to Obtain the Register Content



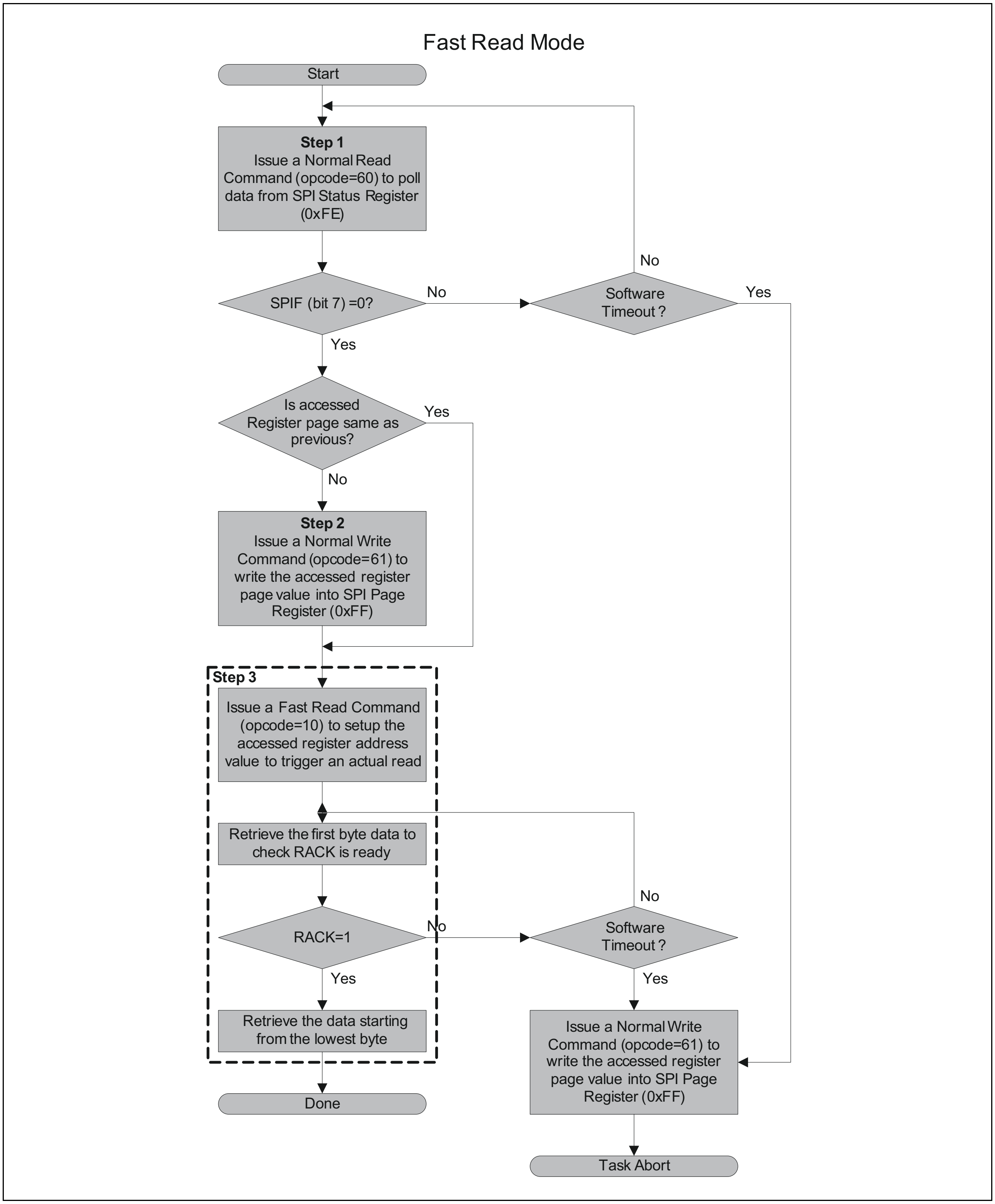
Fast Read Operation

Fast Read operation consists of 3 transactions (three $\overline{SS}$ operations)

1. Issue a Normal Read Command (opcode = 0x60) to poll the SPIF bit in the SPI Status Register (0xFE) to determine the operation can start.
2. Issue a Fast Read command (opcode = 0x10) to setup the accessed Register Page value into the Page register (0xFF).
3. Issue a Fast Read command (opcode = 0x10) to setup the accessed register address value, to trigger an actual read, and retrieve the accessed register content till the completion

Fast Read mode process is different from Normal Read mode, once the switch receives a fast read command followed by the register page and address information, the status and the data (register content) will be put on the MISO line without going through the SPI Status register or SPI Data I/O register. Once RACK bit of the bytes following the Fast Read command with Address information is recognized the register content will be put on MISO line immediately following the byte with RACK bit set. The Fast Read process is described in the following paragraphs with a flowchart followed by a step by step description.

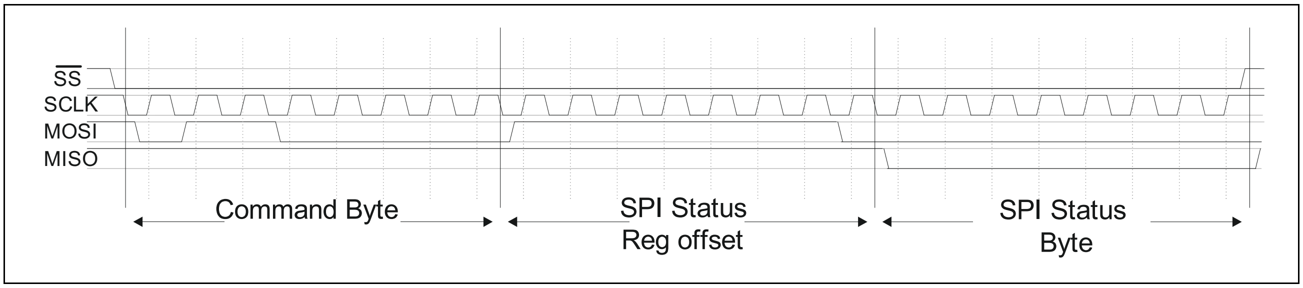
Figure 25: Fast Read Operation



Example: Read from 1000BASE-T Control register (Page 10h, Offset 12h).

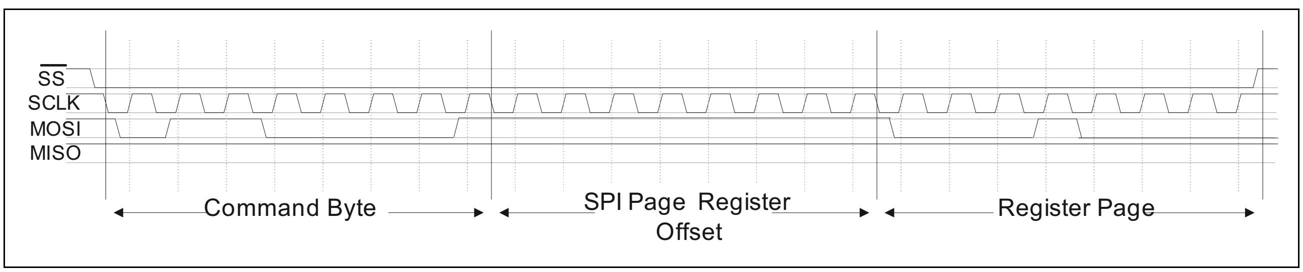
1. Issue a Normal Read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Normal Read Command Byte: 0 1 1 0 0 0 0 0(opcode = 0x60)
- Clock in the SPI Status register address (0xFE)
- Clock in the accessed register page value: 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
- Deassert $\overline{SS}$ while SCK is high idle state

Figure 26: Normal Read Mode to Check the SPIF Bit of SPI Status Register



2. Issue a Normal Write command (opcode = 0x61) and write the accessed register page value of 0x10 in to SPI Page Reigster(0xFF) —this step is required only if previous read/write was not to/from Page 10h.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Fast Read Command Byte: 0 11 0 0 0 0 0 1 (opcode = 0x61)
- Clock in offset of Page register (0xFF)
- Clock in the accessed register page value: 0 0 0 1 0 0 0 0 (Page register: 0x10)
- Deassert $\overline{SS}$ while SCK is high idle state

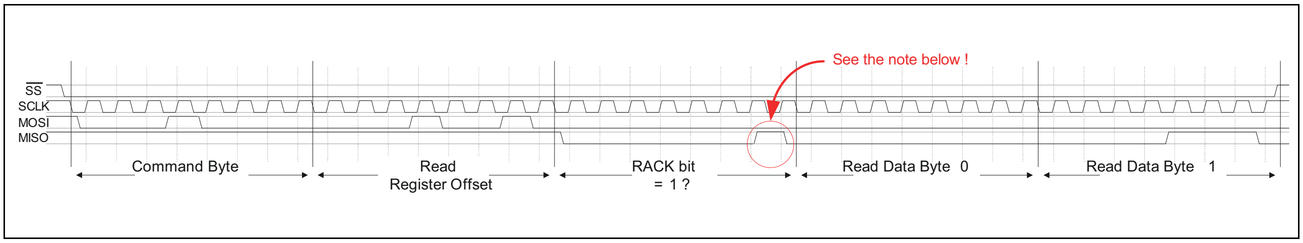
Figure 27: Fast Read Mode to Setup New Page Value



3. Issue a Fast Read command (opcode = 0x10), followed by the Address of the accessed register (0x12), check for a read completion by checking the RACK bit in the SPI Status register, and finally clock out the read data.
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Fast Read Command Byte: 0 0 0 1 0 0 0 0 (opcode = 0x10)
- Clock in the Address of accessed register (0x12)
- Clock out Bytes Until Bit 0 or Bit 1 = 1 : 0 0 0 0 0 0 0 1 (RACK bit 0=1)
- Clock out first data byte: 0 0 0 0 0 0 0 0 (Byte 0: Bit 7 to Bit 0)
- Clock out next data (in this case, last) byte: 0 0 0 0 1 1 1 0 (Byte 1: Bit 15 to Bit 8)

- [Continue if more bytes]
- Deassert $\overline{SS}$ while SCK is high idle state

Figure 28: Fast Read to Read the Register



Note: There is an errata on the RACK output timing in Fast Read mode. The RACK (bit 0) must be sampled prior to toggling the clock to shift out the bit 0.

Normal Write Operation

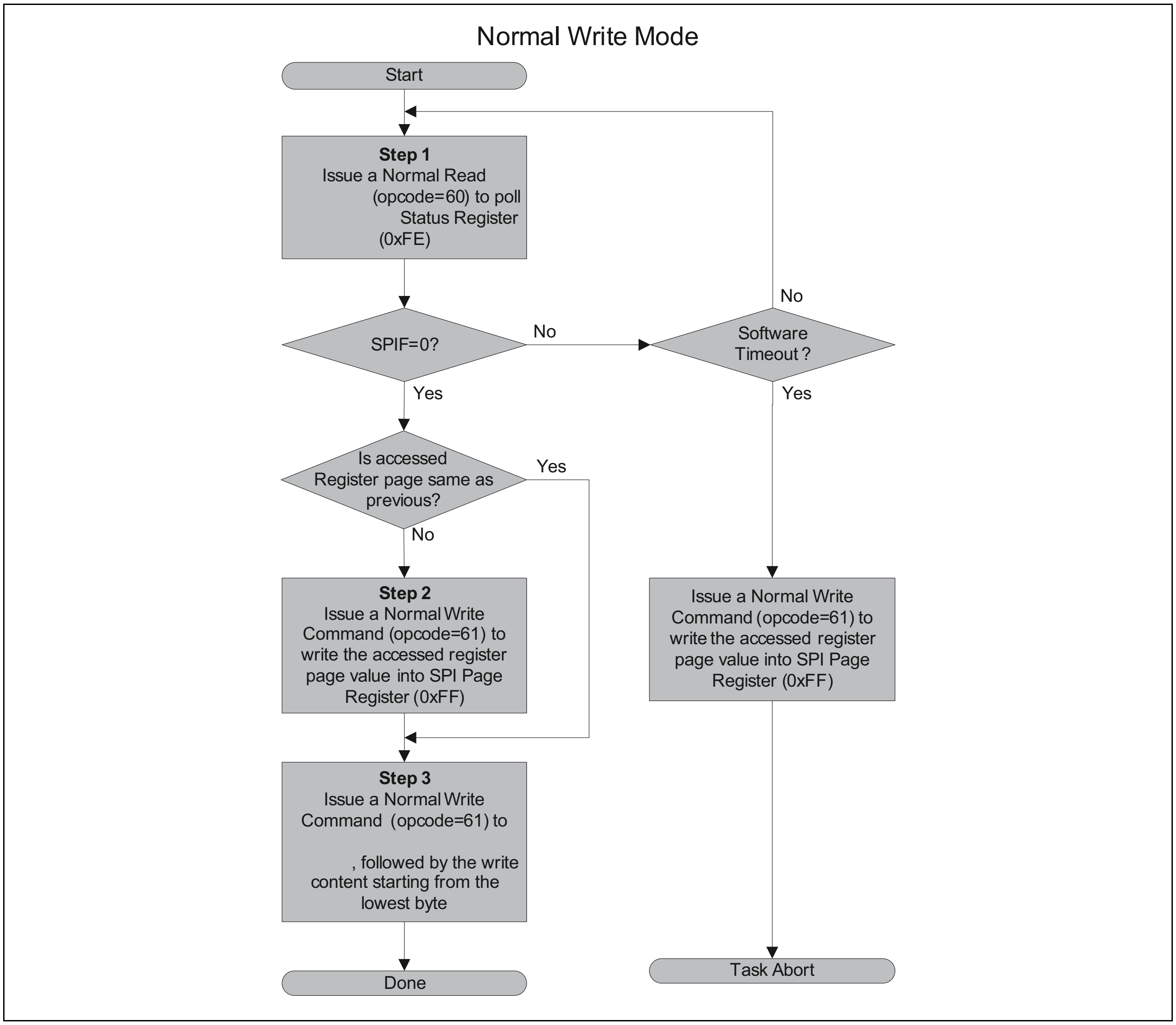
Normal Write operation consists of three transactions (three $\overline{SS}$ operations)

1. Issue a Normal Read Command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a Normal Write command (opcode = 0x61) to setup the accessed register page value into the page register (0xFF).
3. Issue a Normal Write command (opcode = 0x61) to setup the accessed register address value, followed by the write content starting from a lower byte.

The Normal Write Mode process is described in the following paragraphs with a flowchart followed by a step by step description.

Note: The RoboSwitch does not support Fast Write mode.

Figure 29: Normal Write Operation

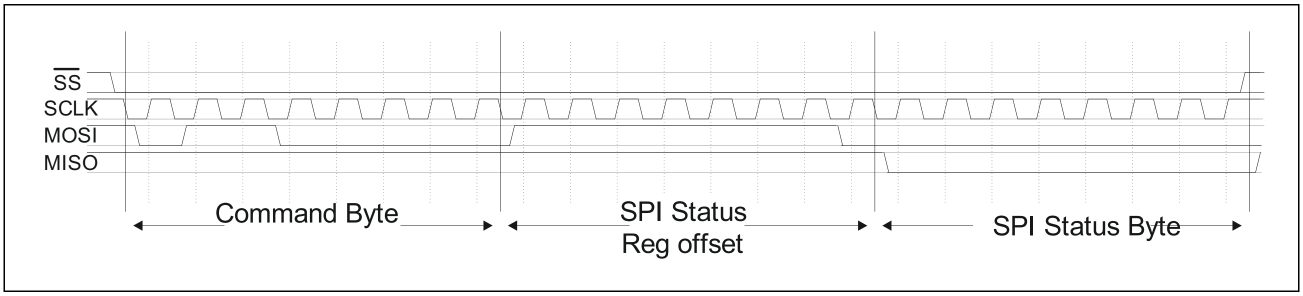


Example: 0x1600h is written to 1000BASE-T Control register (Page 0x10, Offset 0x12).

1. Issue a Normal Read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).

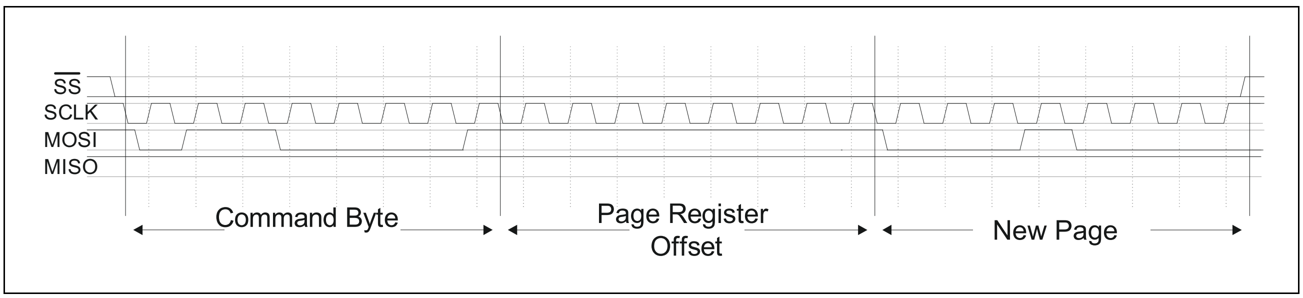
- Assert $\overline{SS}$ while SCK is high idle state
- Clock in a Normal Read Command Byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
- Clock in the SPI Status register address (0xFE)
- Clock in the accessed register page value,: 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
- Deassert $\overline{SS}$ while SCK is high idle state

Figure 30: Normal Read Mode to Check the SPIF Bit of SPI Status Register



2. Issue a Normal Write command (opcode = 0x61) and write the accessed register page value of 0x10 into SPI Page register (0xFF)—this step is required only if previous read/write was not from/to Page 0x10.
   - Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a Normal Write Command Byte: 0 1 1 0 0 0 0 1 (opcode = 0x61)
   - Clock in offset of Page register (0xFF)
   - Clock in 1 byte of the accessed register page value (Page register 0x10)
   - Deassert $\overline{SS}$ while SCK is high idle state

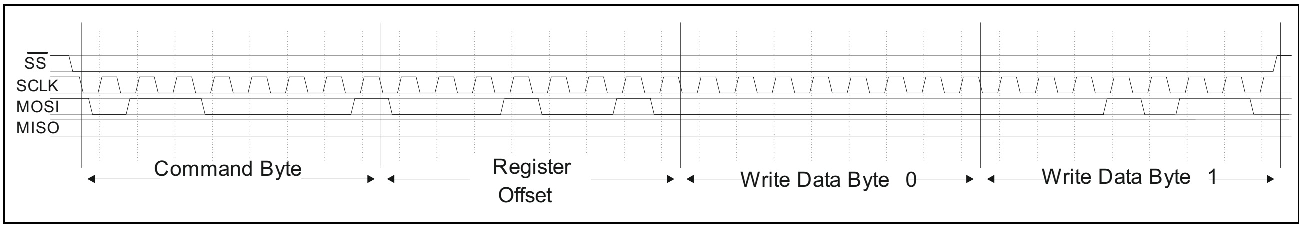
Figure 31: Normal Write to Setup the Register Page Value



3. Issue a Normal Write command (opcode = 0x61) and write the Address of the accessed register followed by the write content starting from a lower byte.

- Assert $\overline{SS}$ while SCK is high idle state
   - Clock in a Normal Write Command Byte: 0 1 1 0 0 0 0 1 (opcode = 0x61)
   - Clock in Offset of Address of accessed register (0x12)
   - Clock in lower data byte first: 0 0 0 0 0 0 0 0 (Byte 0: Bit 7 to Bit 0)
   - Clock in upper data byte next: 0 0 0 1 0 1 1 0 (Byte 1: Bit 15 to Bit 8)
   - [Continue if more bytes]
   - Deassert $\overline{SS}$ while SCK is high idle state

Figure 32: Normal Write to Write the Register Address Followed by Written Data



EEPROM Interface

The BCM53118 can be connected via the serial interface to a low-cost external serial EEPROM, enabling it to download register-programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

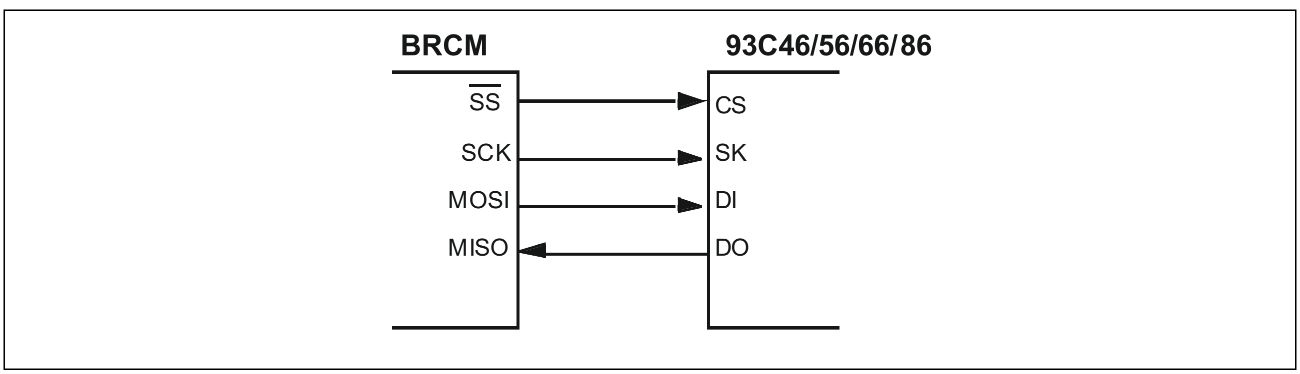
During the chip-initialization phase, the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and it matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

Due to the different access cycles of different capacity EEPROMs, the strap pins EEPROM_TYPE[1:0] are used to support the various EEPROM devices according to Table 23.

Table 23: EEPROM_TYPE[1:0] Settings

EEPROM_TYPE[1:0]	EEPROM
00	93C46
01	93C56
10	93C66
11	93C86

Figure 33: Serial EEPROM Connection



EEPROM Format

The EEPROM should be configured to x16 word format. The header contains key and length information as shown in Table 24. The actual data stored in the EEPROM is byte-swapped as shown in Table 25.

- Upper 5 bits are magic code 15h, which indicates that valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speedup. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words
  - 93C86 up to 1024 words

Table 24: EEPROM Header Format

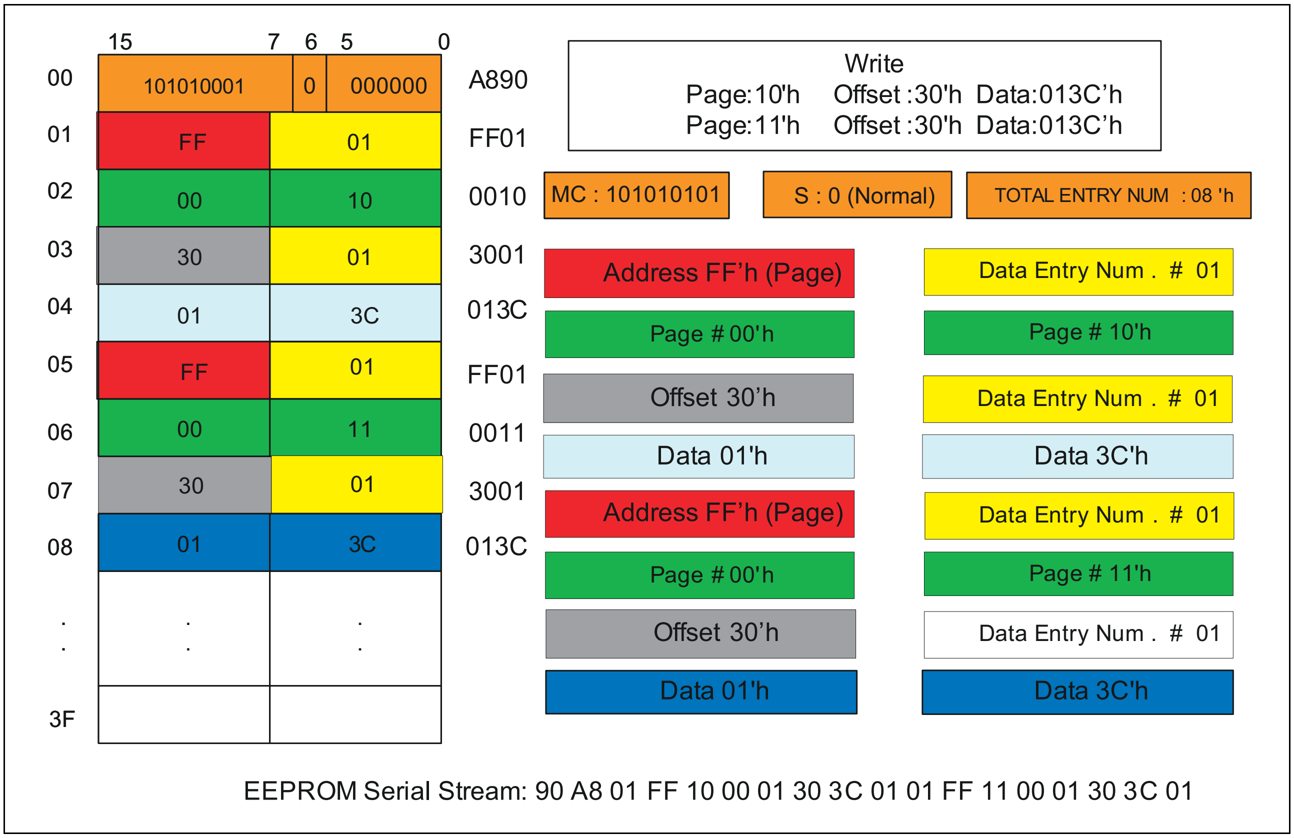
Bits [15:11}	***Bit 10***	***Bits [9:0]***
Magic code, 15h	Speed	Total entry number 93C46: 0 ~ 63 93C56: 0 ~ 127 93C66: 0 ~ 255 93C86: 0 ~ 1023

Table 25: EEPROM Contents

Bits [7:0]	***Bits [15:11]***	***Bit 10***	***Bits [9:8]***
Total entry number	Magic code, 15h	Speed	Total entry number

Figure 34 on page 108 shows an EEPROM programming example.

Figure 34: EEPROM Programming Example



MDC/MDIO Interface

BCM53118 offers an MDC/MDIO interface for accessing the switch registers as well as the PHY registers. An external management entity can access the switch registers through this interface when the SPI interface is not used. (i.e., when the SPI clock is in idle mode.) The switch registers are accessed through the Pseudo PHY interface, and the PHY registers are accessed directly by using PHY addresses.

External PHY can be connected to GMII interface of IMP port. Through the SPI interface, by accessing the Page 88h, the external PHY MII registers can be accessed. The actual PHY address can be assigned through the "MDIO IMP Port Address Register (Page 00h: Address 78h)" on page 154.

Note: The PHY registers are not accessible through the Pseudo PHY operation.

MDC/MDIO Interface Register Programming

The BCM53118 are designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM53118 sources a 2.5-MHz clock. Serial bidirectional data transmitted via the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM53118 and contains the following:

- **Preamble (PRE)**. To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- **Start of Frame** (**ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code** (**OP**). A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address** (**PHYAD**). A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address** (**REGAD**). A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround** (**TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM53118 chip during these two bit times. When a read operation is being performed, the MDIO pin of the BCM53118 must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.
- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM53118. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Pseudo-PHY

The MDC/MDIO can be used by an external management entity to read/write register values internal to the BCM53118. This mode offers an alternative programming interface to the chip. The BCM53118 operate in slave mode with a PHY address of 30d. The following figures show the register setup flow chart for accessing the registers via the MDC/MDIO interface.

Figure 35: Pseudo-PHY MII Register Definitions

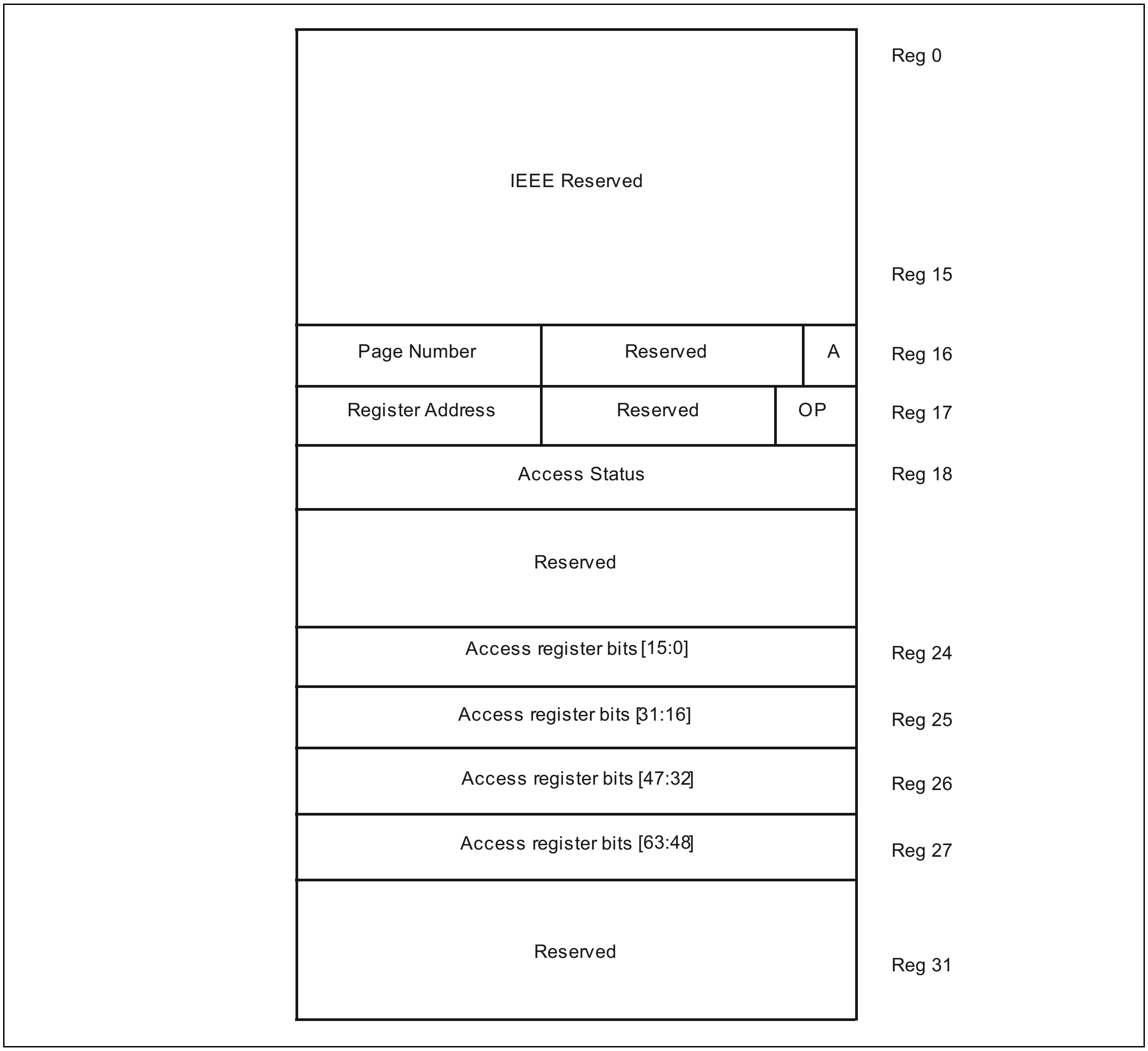
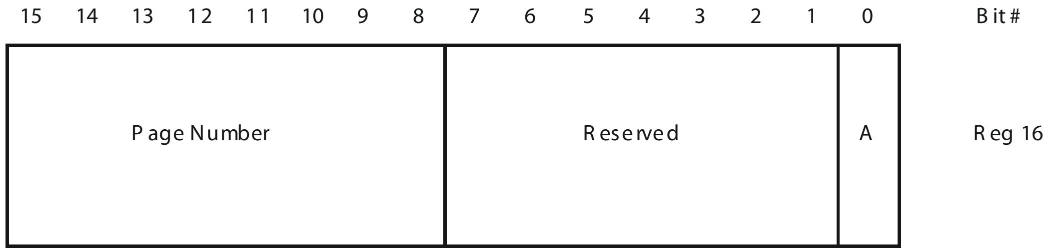


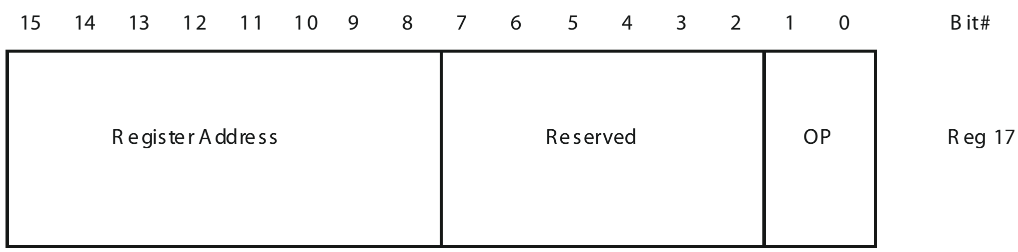
Figure 36: Pseudo-PHY MII Register 16: Register Set Access Control Bit Definition



bits [15:8] => Page number (RW)
bits [71] => Reserved
Bit 0 => Register set MDC/MDIO access enable (RW)

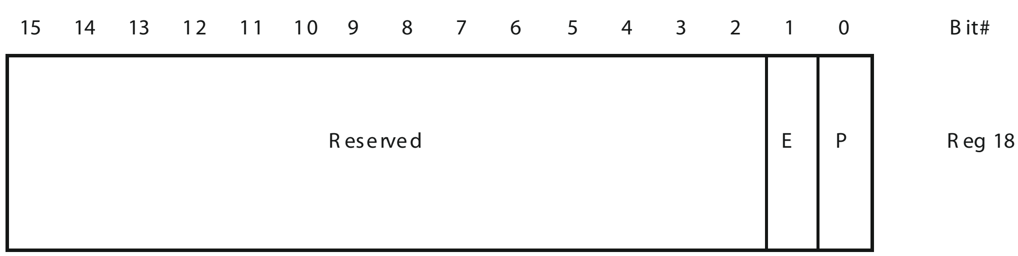
Note: The bit 0 (MDC/MDIO Access Enable) in register 16 should be released (set to 0) after a transaction is completed. This allows the SPI interface to access the switch register if required.

Figure 37: Pseudo-PHY MII Register 17: Register Set Read/Write Control Bit Definition



bits [15:8] => Register address (RW)
bits [7:2] => Reserved
bits [1:0] => OP code (RW/SC), 00 = No operation
01 = Write operation
10 = Read operation
11 = Reserved

Figure 38: Pseudo-PHY MII Register 18: Register Access Status Bit Definition



bits [15:1] => Reserved
Bit 1 => Operation Error (RO/LH), when op_code = 2'b11, this bit is set to show operation error.
Bit 0 => Prohibit Access (RO/LH), for Page Number = 8'h1X, which are PHY MII registers.

Figure 39: Pseudo-PHY MII Register 24: Access Register Bit Definition

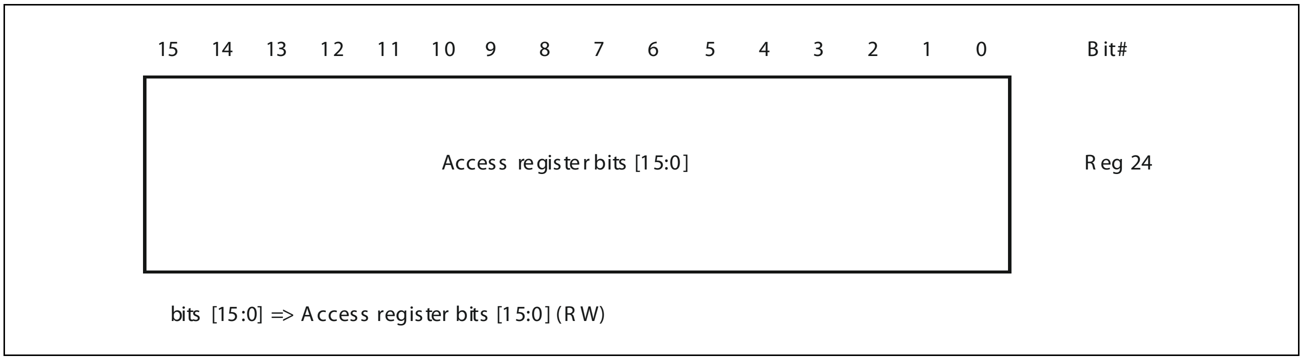


Figure 40: Pseudo-PHY MII Register 25: Access Register Bit Definition

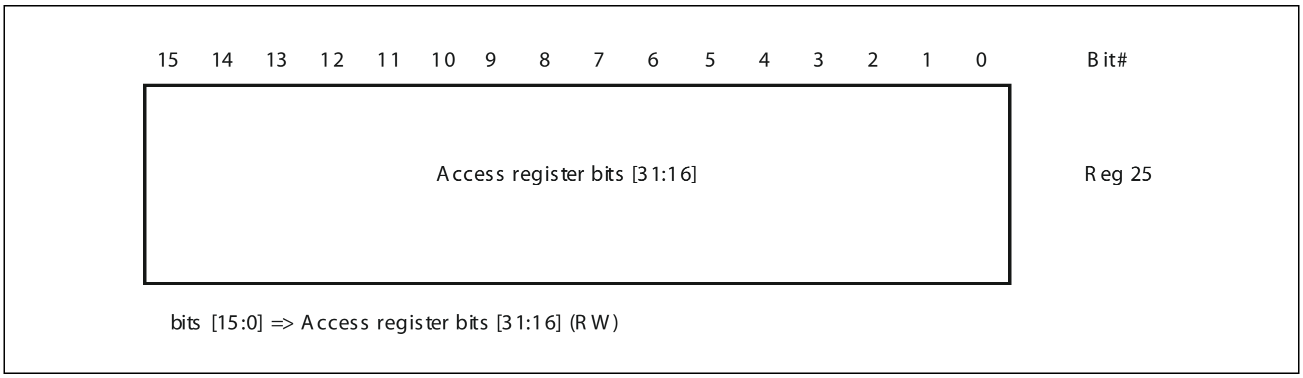


Figure 41: Pseudo-PHY MII Register 26: Access Register Bit Definition

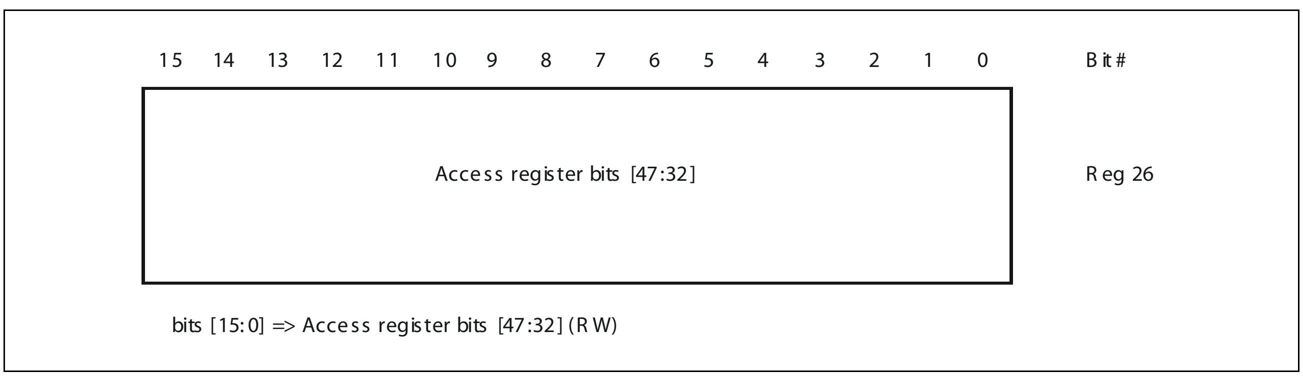


Figure 42: Pseudo-PHY MII Register 27: Access Register Bit Definition

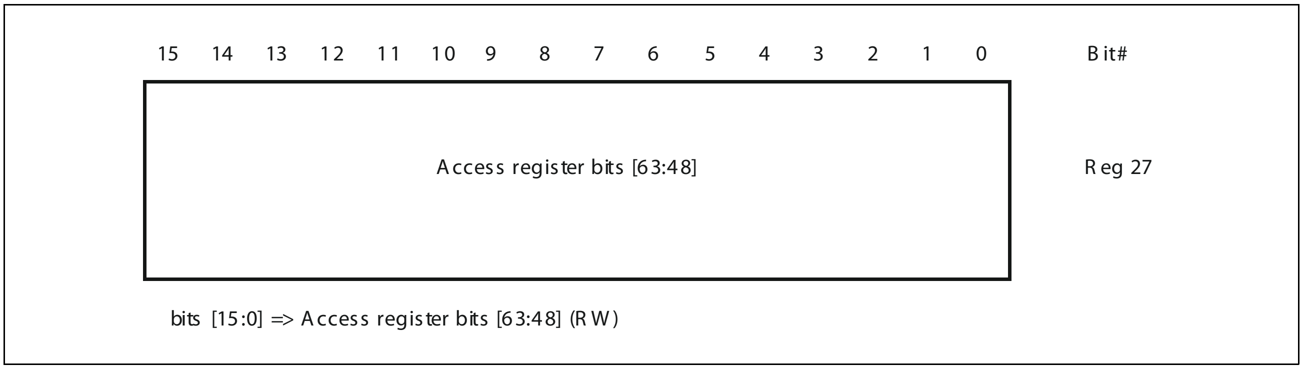


Figure 43: Read Access to the Register Set via the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

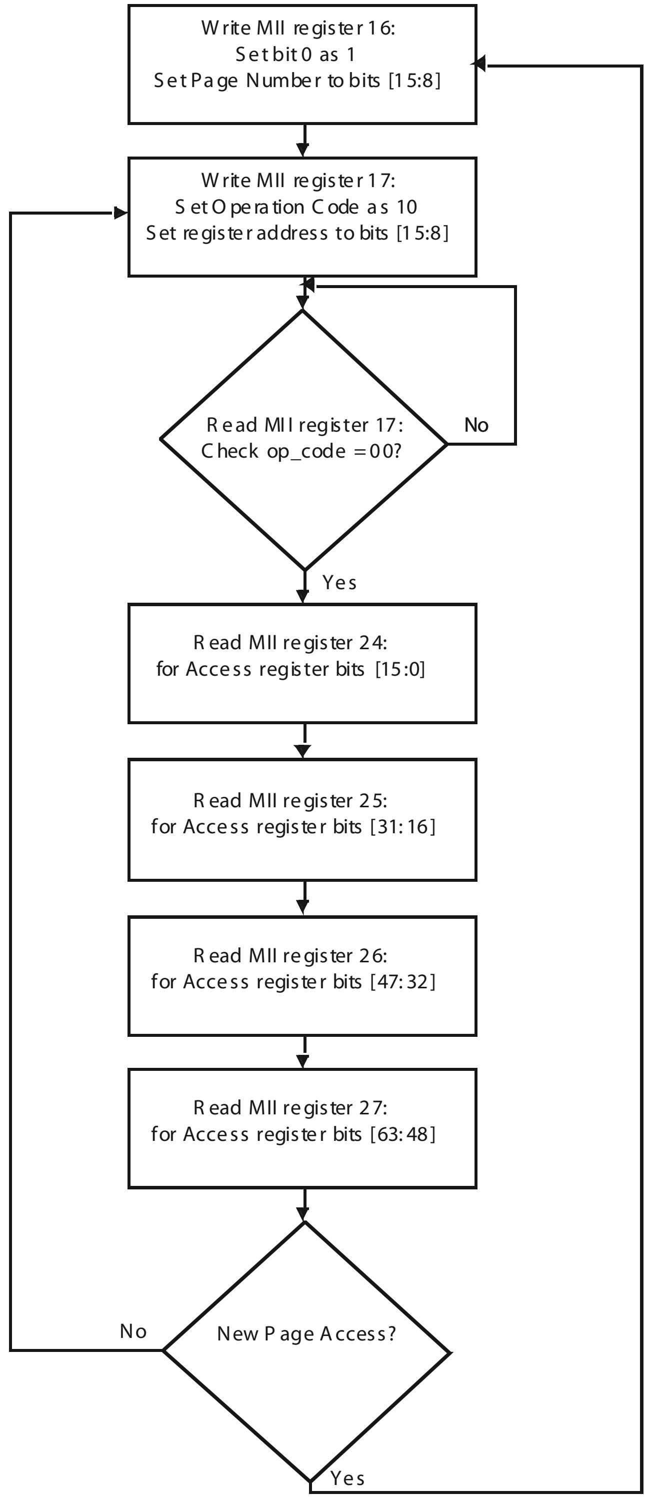


Figure 44: Write Access to the Register Set via the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

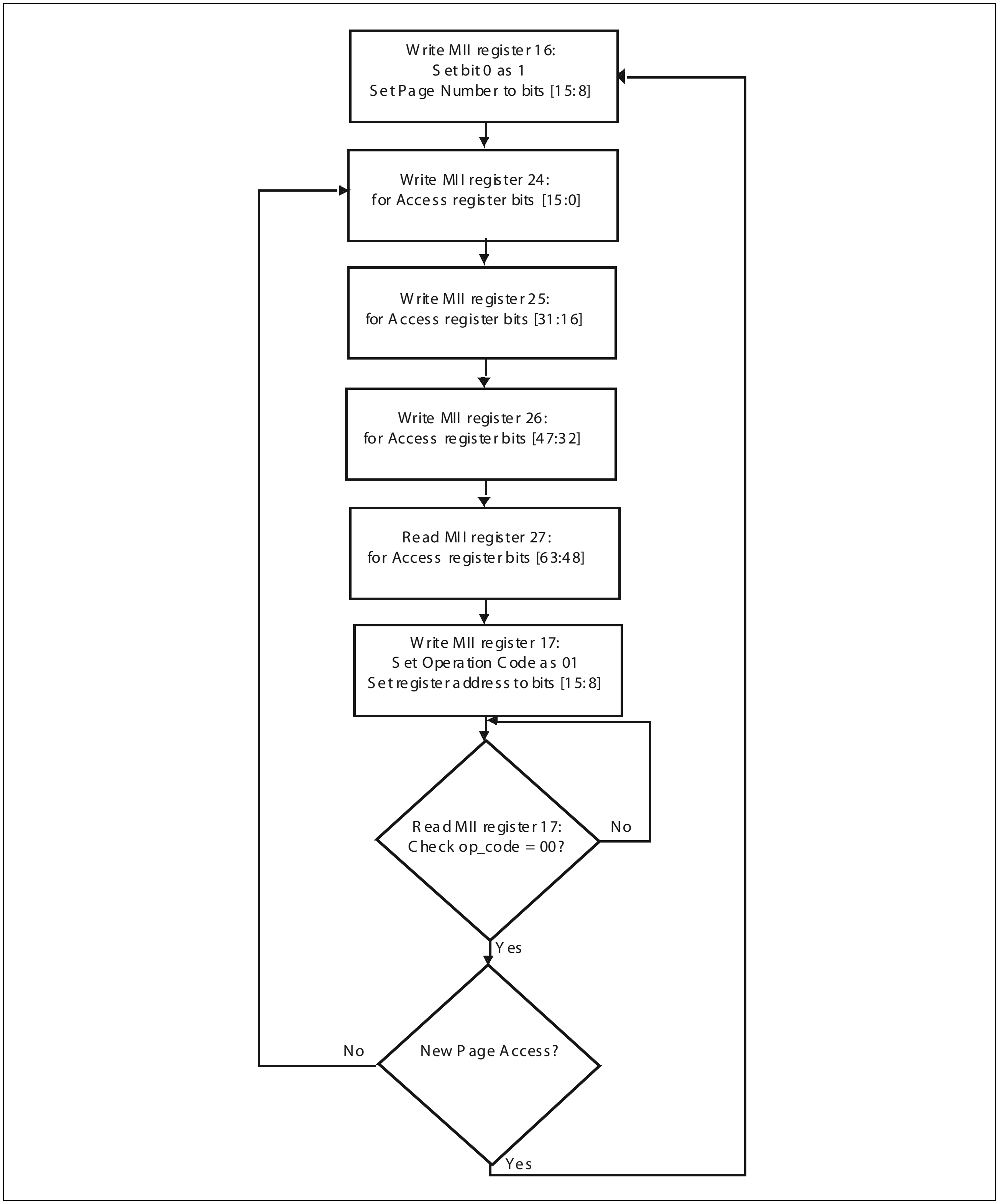


Table 26 summarizes the complete management frame format.

Table 26: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven by master Driven by slave
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to master

See “MDC/MDIO Interface” on page 109 for more information regarding the timing requirements.

LED Interfaces

The BCM53118 provides flexible visibility per-port status of various functions. The LED Interface offers an option to display different functions for each port given the number of LED bits available. The BCM53118 provides a total of 32 LED pins. In a 5-port switch application, these are dedicated as four LED pins per port as shown in Table 27. If one or more ports are not used in an application and are disabled via LED Enable Map register (Page 00h: Address 16h), and no more than four LED pins are to be used per port, the locations of the pins for the enabled ports are the same as if all eight ports were used, with four pins reserved per port, regardless of whether the port is enabled.

For example, if Port7~2 LED displays are disabled (value of register page 00h, address 16h = 0003), Port0 and Port1 LED display are still from LED pins LEDP28~31 (Port0), LEDP24~27 (Port1), just as if all eight ports were used. If Port1 and Port0 LED displays are disabled (value of register page 00h, address 16h = 00FC), Port5, Port6, and Port7 are still from LED pins LEDP8~11 (Port5), LEDP4~7 (Port6), and LEDP0~3 (Port7), also just as if all eight ports were used.

To set up the LED interface, configure strap pins LED_MODE[1:0] or select the desired display the functions in the LED Function 0 Control register/LED Function 1 Control register. The per-port LED display is fixed with four functions.

- To configure the strap pins, set the predefined functions to be displayed by setting the strap pins LED_MODE[1:0]. The predefined functions are described in Table 30: “Signal Type Definitions,” on page 123. Per-port LED display is fixed four functions and occupy four LED pins.
- To configure LED display function in the two LED Function Control registers, assign each port to one of the LED Function 0 Control register and LED Function 1 Control register by enabling the bits in the LED Function Map register. The LED interface shifts out the status of the selected functions for ports enabled in the LED Enable Map register.

Only four or less than four functions can be selected, and the per-port LED display occupies four LED pins (fixed four functions). For example, if LED display function via LED Function 1 Control register is configured and the value is set to 0324h (four LED functions) or 0320h (three LED functions), the per-port LED display has four fixed functions and occupies four LED pins per port, Port7 (LEDP0~3), Port6 (LEDP4~7), ...Port0 (LEDP28~31).

The status of enabled ports is sent out from a higher port number to the lowest port number. The output order that is in the shift out is from LEDP[0], LEDP[1], LEDP[2],.....LEDP[31]. The output port order for LED is from high port number to low port number, and the output bit order within the port LED is form MSB to LSB.

The LED MODE MAP 0 and 1 (Page 00h: Address 18h, and 1Ah) can be set to select:

- LED to blinking,
- LED on, or
- LED auto mode.

Bit 7, LED_EN, of the LED Refresh register is default enabled. When this bit 7 is enabled, the LED display of each port status is normal and truly reflects each port link up/link down status. If bit 7 is disabled, the LED status is latched in its current state.

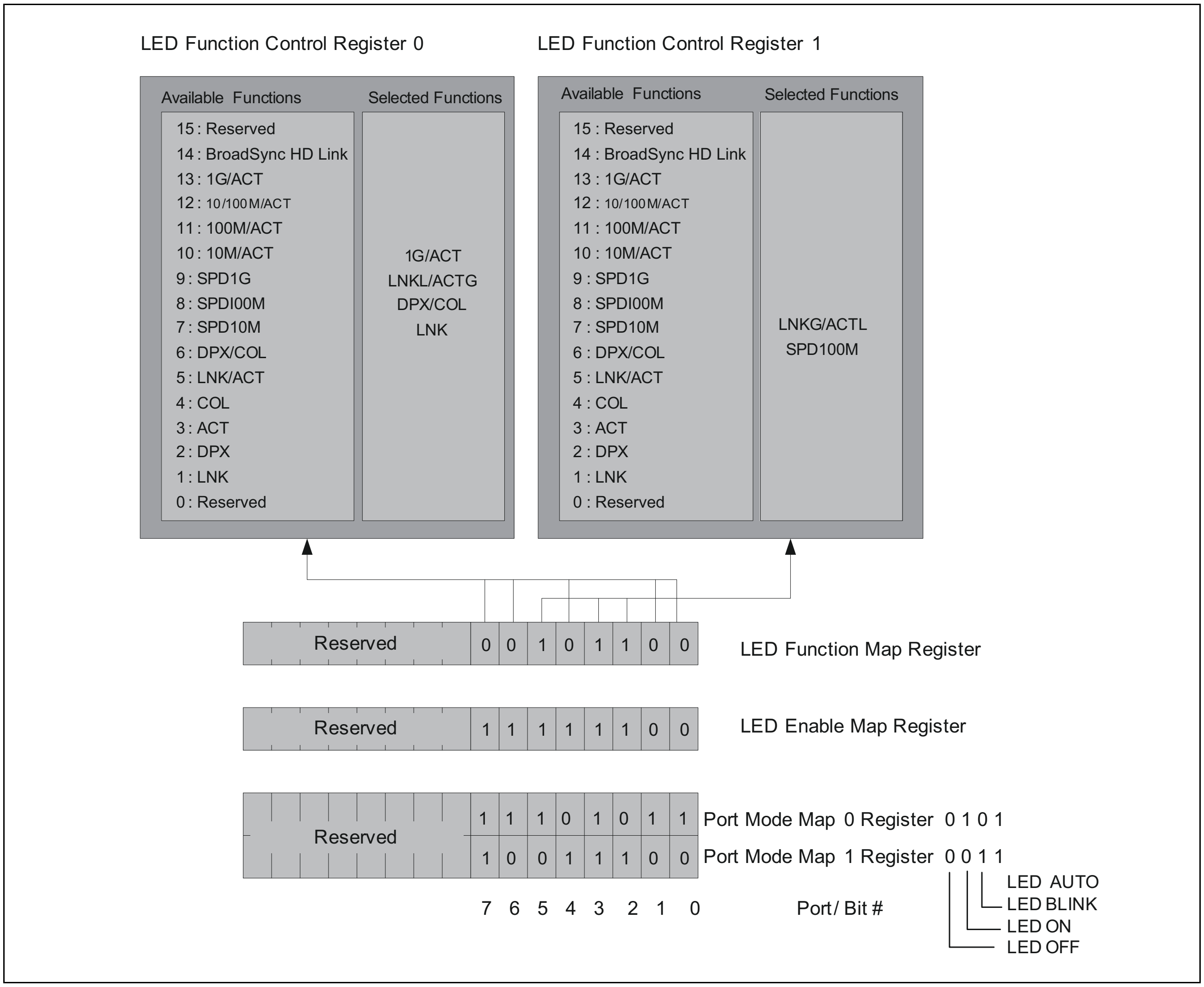
LED signals are active low, and for the dual function LEDs, LNK, DPX, and Speed state are active low. The ACT (activity) indicator is indicated by blinking.

Table 27: LED Output Pins Per Port

Port	***LED Output Pins***
Port 7	LEDP [0:3]
Port 6	LEDP [4:7]
Port 5	LEDP [8:11]
Port 4	LEDP [12:15]
Port 3	LEDP [16: 19]
Port 2	LEDP [20:23]
Port 1	LEDP [24:27]
Port 0	LEDP [28: 31]

Figure 45 shows the LED Interface register structure.

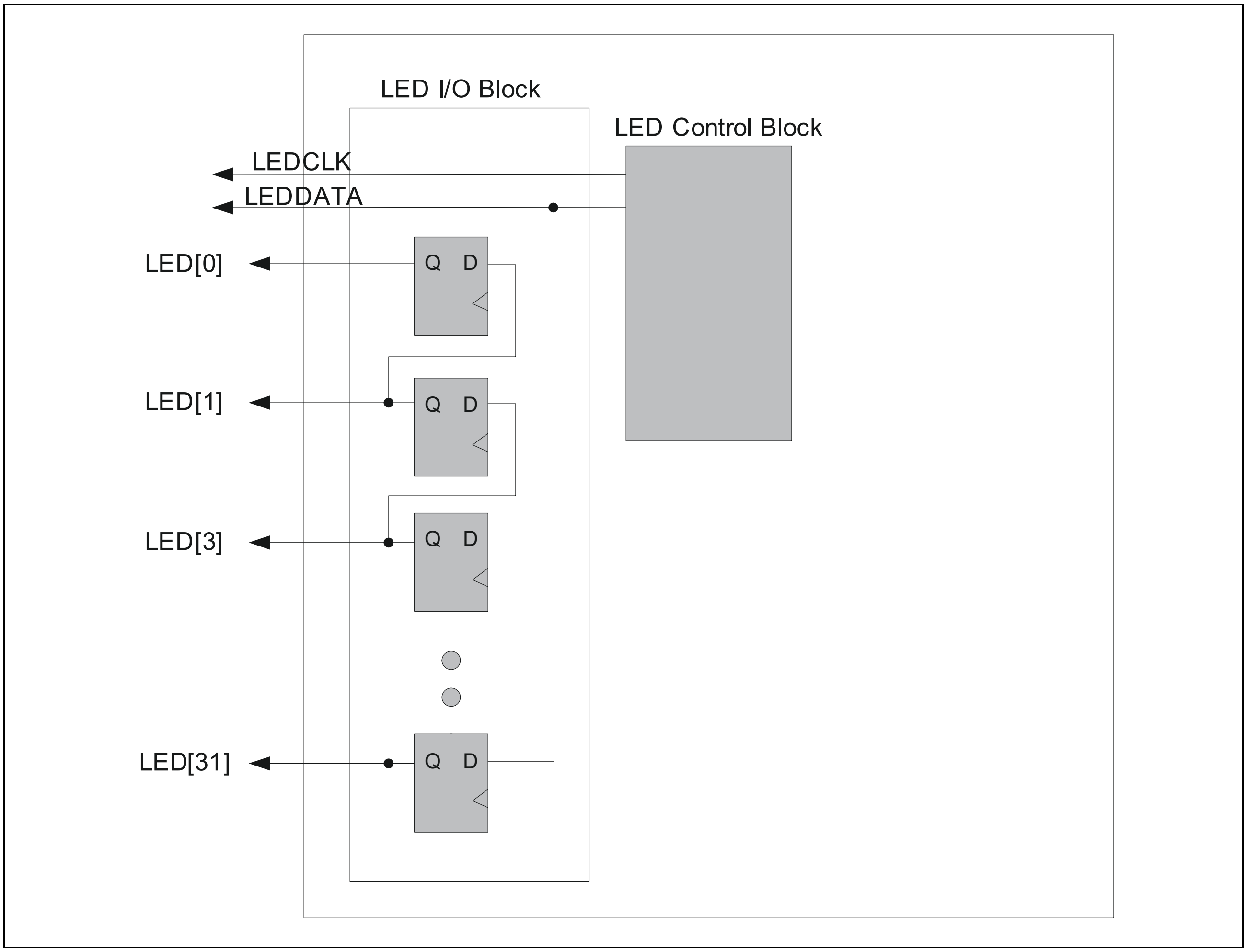
Figure 45: LED Interface Register Structure Diagram



The BCM53118 offers two LED Interfaces, Parallel LED Interface and Serial Interface. As shown in Figure 46, the source of LED status stream is the same for both interfaces; the status bit stream is based on the programmed register settings. The Parallel LED Interface provides all the shifting and storing of the status internally, so that it does not require any external shift registers, but it requires more I/O pins to be connected on the part.

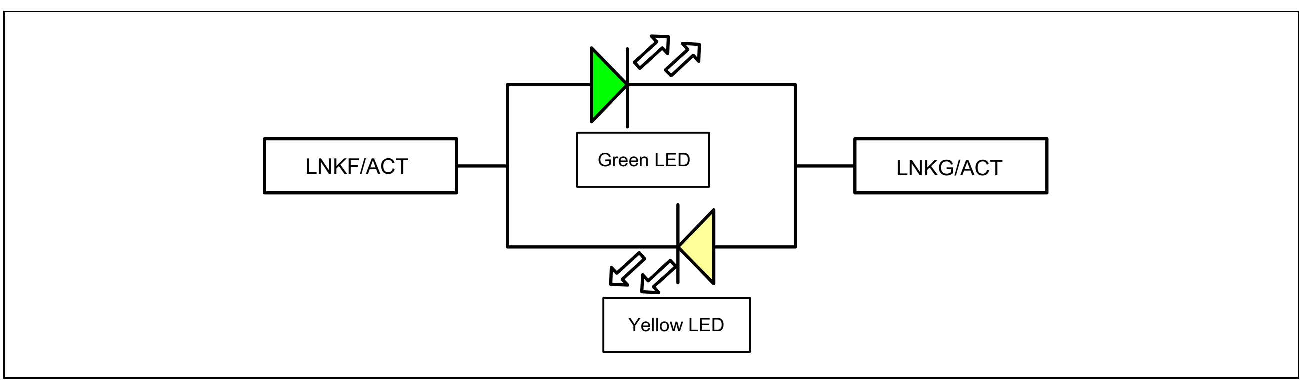
The Serial LED Interface is being output through two pins (LEDDATA, LEDCLK). It saves the number of I/O pins, but it requires the user to design in the external shift registers.

Figure 46: LED Interface Block Diagram



Dual LED is used for displaying more than one status using one LED cell. By packing two different colors LED into one holder, dual LED can display more than two states in one cell. Figure 47 shows a typical dual LED usage. Green LED is to display LNKG/ACT status, while Yellow LED is to display LNKF/ACT status.

Figure 47: Dual LED Usage Example



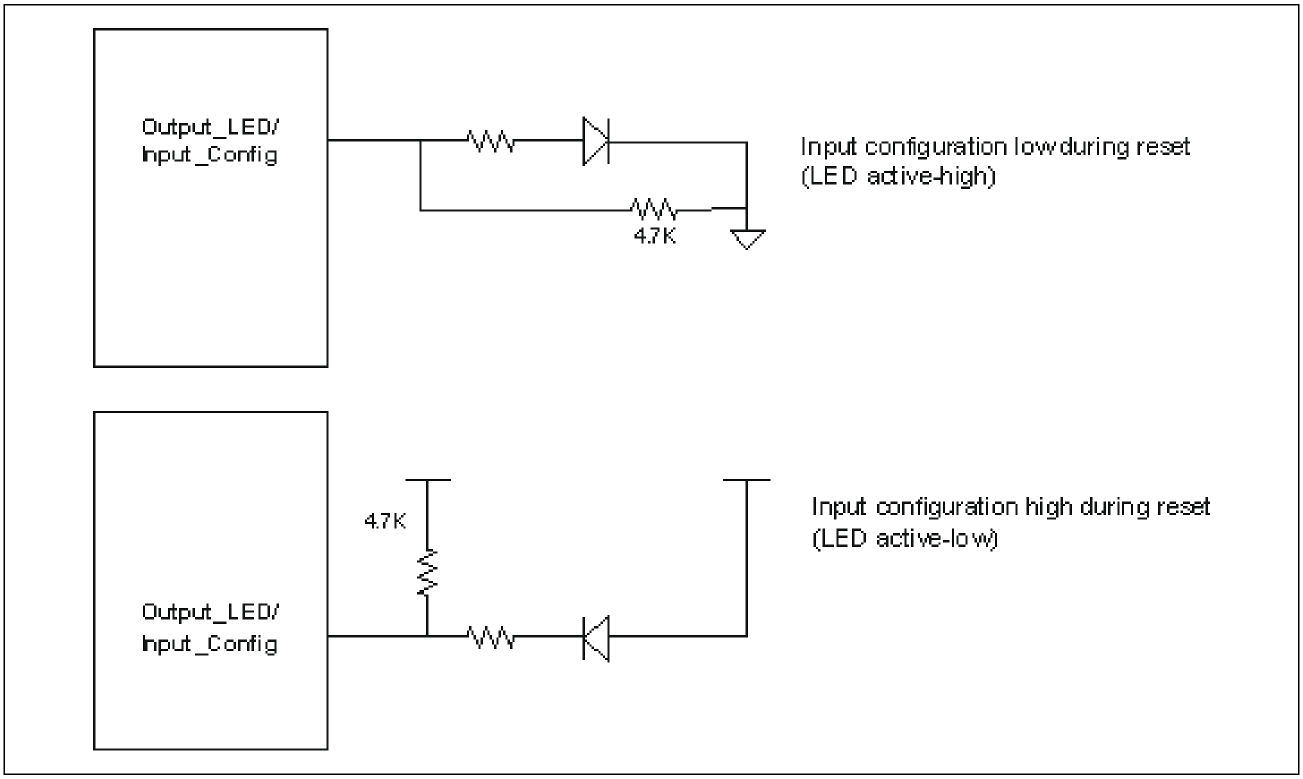
Dual Input Configuration/LED Output Function

There are 12 LEDs pins that have secondary functions. These pins serve as input pins during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active-low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 28 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output (see Figure 48 on page 121).

Table 28: Dual Input Configuration/LED Outputs

LED Output Pins (Normal Operation)	***Input Configuration Pin (Latched During Reset)***
LEDP3	En_Green
LEDP10	EEPROM_TYPE0
LEDP11	EEPROM_TYPE1
LEDP14	LOOP_DET_EN
LEDP15	LOOP_IMP_SEL
LEDP18	BC_SUPP_EN
LEDP22	DIS_IMP
LEDP23	IMP_DUMB_FWDG_EN
LEDP26	ENFDXFLOW
LEDP27	ENHDXFLOW
LEDP30	IMP_TXC_DELAY
LEDP31	IMP_RXC_DELAY

Figure 48: LED Circuit for Dual Input Configuration/LED Output Pins



Section 5: Hardware Signal Definition Table

I/O Signal Types

The following conventions are used to identify the I/O types shown in the following table. The I/O pin type is useful in referencing the DC-pin characteristics.

Table 29: I/O Signal Type Definitions

Abbreviation	*Description*
XYZ	Active low signal
A	Analog pin type
B	Bias pin type
CS	Continuously sampled
D	Digital pin type
DNC	Do not connect
GND	Ground
I	Input
I/O	Bidirectional
I_{PU}	Input with internal pull-up
O_{3S}	Tristated Signal
O_{DO}	Open-drain output
O	Output
O_{PU}	Output with internal pull-up
O_{PD}	Output with internal pull-down
PD	Internal pull-down
SOR	Sample on reset
PWR	Power pin supply
PU	Internal pull-up
XT	Crystal pin type

Signal Descriptions

Table 30: Signal Type Definitions

Signal Name	Type	Description
Serial Interface		
TRD0_0+/- TRD1_0+/- TRD2_0+/- TRD3_0+/- TRD0_1+/- TRD1_1+/- TRD2_1+/- TRD3_1+/- TRD0_2+/- TRD1_2+/- TRD2_2+/- TRD3_2+/- TRD0_3+/- TRD1_3+/- TRD2_3+/- TRD3_3+/- TRD0_4+/- TRD1_4+/- TRD2_4+/- TRD3_4+/- TRD0_5+/- TRD1_5+/- TRD2_5+/- TRD3_5+/- TRD0_6+/- TRD1_6+/- TRD2_6+/- TRD3_6+/- TRD0_7+/- TRD1_7+/- TRD2_7+/- TRD3_7+/-	I_A/O_A	**Transmit/Receive Pairs.** In TRD [pair number]_[port number]± 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. In auto-negotiation and 10BASE-T and 100BASE-TX modes, the BCM53118 normally transmits on TRD[0]_[port number]± and receives on TRD[1]_{port number}±. Auto-MDIX operation can reverse the pairs TRD[0]_{7:0}± and TRD[1]_{7:0}±
Clock/Reset		
RESET	I_{PU}	**Hardware Reset Input**. Active low Schmitt-triggered input. Resets the BCM53118.

Table 30: Signal Type Definitions (Cont.)

Signal Name	***Type***	***Description***
XTALI	I_{XT}	**25-MHz Crystal Oscillator Input/Output**. A continuous 25-MHz reference clock must be supplied to the BCM53118 by connecting a 25-MHz crystal between these two pins or by driving XTALI with an external 25-MHz oscillator clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage is 3.3V.
XTALO	O_{XT}	
IMP Interface		
IMP_TXCLK	I/O	**MII Transmit Clock.** This is an input pin in MII mode, or GMII mode but speed is 100Mbps/10Mbps. It synchronizes the TXD[3:0] and connects to the PHY Entity TXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. **RvMII Receive Clock.** This is an output pin in RvMII mode. It synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/ Management Entity RXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. This output pin has an internal 25Ω-series termination resistor. This clock is not use in the other conditions.
IMP_TXD[3:0]	O	**GMII Transmit Data Output (first nibble)**. Data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RGMII Transmit Data Output**. For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK. **RvMII Receive Data Output**. Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity. **MII Transmit Data Output**. Clocked on the rising edge of TXCLK supplied by MAC/Management entity. These output pins have internal 25Ω-series termination resistor.
IMP_TXD[7:4]	O	**GMII Transmit Data Output (second nibble)**. Data bits [7:4] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω-series termination resistor.
IMP_TXEN	O	**GMII/MII Transmit Enable**. Active high. TXEN indicates the data on the TXD pins are encoded and transmitted. **RGMII Transmit Control**. On the rising edge of TXCLK, TXEN indicates that a transmit frame is in progress, and the data present on the TXD[3:0] output pins is valid. On the falling edge of TXCLK, TXEN is a derivative of GMII mode TXEN and TXER signals. **RvMII Receive Data Valid**. Active high. Connected to RXDV pin of MAC/ Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid. This output pin has an internal 25Ω-series termination resistor.
IMP_TXER	O	**GMII/MII Transmit Error**. Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. This output pin has an internal 25Ω-series termination resistor.

Table 30: Signal Type Definitions (Cont.)

Signal Name	*Type*	*Description*
IMP_RXCLK	I	**GMII Receive Clock**. 125 MHz for 1000 Mbps operation. **RGMII Receive Clock**. 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK. **MII Receive Clock.** 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation.
	O	**RvMII Transmit Clock**. Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. This output pin has an internal 25Ω-series termination resistor.
IMP_RXD[3:0]	I	**GMII Receive Data Inputs (first nibble)**. Data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RGMII Receive Data Inputs**. For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RvMII Transmit Data Inputs**. Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity. **MII Receive Data Input.** Data bits RXD[3:0] are clocked on the rising edge of RXCLK.
IMP_RXD[7:4]	I	**GMII Receive Data Inputs (second nibble)**. Data bits RXD[7:4] are clocked out on the rising edge of RXCLK.
IMP_RXDV	I	**GMII/MII Receive Data Valid**. Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid. **RGMII Receive Data Valid**. Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK. **RvMII Transmit Enable**. Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity.
IMP_RXER	I	**GMII/MII Receive Error**. Indicates an error during the receive frame.
IMP_CRS	I	**Carrier Sense.** Active-high, indicates traffic on link
IMP_COL	I	**Collision Detect.** In half-duplex mode, active-high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.

Table 30: Signal Type Definitions (Cont.)

Signal Name	***Type***	***Description***
IMP_GTX_CLK	O	**GMII Transmit clock.** This clock is driven to synchronize the transmit data in 1000 Mbps speed in GMII mode. **RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode(125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0]. IMP_GTX_CLK is used in RGMII and 1000 Mbps speed in GMII mode. IMP_TXCLK is used for MII mode, and 10/100 Mbps speed in GMII mode. This output pin has an internal 25Ω-series termination resistor.
MDC/MDIO Interface		
MDIO	I/OPD	**Management Data I/O.** In master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers via the Pseudo-PHY. See the MDC/MDIO interface for more information.
MDC	I/OPD	**Management Data Clock.** In master mode, this 2.5-MHz clock sourced by BCM53118 to the external PHY device. In slave mode, it is sourced by an external entity.
Test Interface		
TCK	IPU	**JTAG Test Clock Input.** Clock Input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	IPU	**JTAG Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected. Shared with MOSI.
TDO	O	JTAG Test Data Output.
TMS	IPU	JTAG Mode Select Input.
TRST	IPU	JTAG Test Reset. Active low. Resets the JTAG controller. This signal must be pulled low during normal operation.
Configuration Pins		
CLK_FREQ1	IPD, SOR	**System Clock Selection.** Determines rate of system clock. 00 = 83 MHz 01 = 91 MHZ (normal operation) 10 = 100 MHz 11 = 111 MHz
CLK_FREQ0	IPU, SOR	
CPU_EEPROM_SEL	IPU, SOR	CPU or EEPROM Interface Selection. CPU_EEPROM_SEL = 0: Enable EEPROM interface. CPU_EEPROM_SEL = 1: Enable SPI Interface, The SPI interface has to be enabled (CPU_EEPROM_SEL = 1) for Pseudo-PHY accesses through the MDC/MDIO Interface. See ""Programming Interfaces" on page 92 for more information.
HW_FWDG_EN	IPD, SOR	**Forwarding Enable.** Active high. If this pin is pulled low at power-up, frame forwarding is disabled.

Table 30: Signal Type Definitions (Cont.)

Signal Name	Type	Description
LED MODE[1:0]	Bit 0: I_{PD}, Bit 1: I_{PU}, SOR	LED Mode. Users can select predefined functions to be displayed for each port by setting the bits accordingly. **When LED MODE[1:0] = 00** FE configuration SPD100M LNK/ACT PHYLED4 GbE configuration SPD1G SPD100M LNK/ACT PHYLED4 **When LED MODE[1:0] = 01** FE configuration 100M/ACT 10M/ACT DPX/COL PHYLED4 GbE configuration 1G/ACT 10/100M/ACT DPX/COL PHYLED4 **When LED MODE[1:0] = 10** FE configuration SPD100M LNK/ACT DPX GbE configuration SPD1G SPD100M LNK/ACT DPX **When LED MODE[1:0] = 11** FE configuration 100M/ACT 10M/ACT DPX GbE configuration 1G/ACT 100M/ACT 10M/ACT DPX

Table 30: Signal Type Definitions (Cont.)

Signal Name	Type	Description
IMP_SPD_SEL[1:0]	Bit 0: I_{PD}, Bit 1: I_{PU}	**IMP Port Speed Select.** 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps (default) 11 = Illegal
IMP_MODE[1:0]	Bit 0: I_{PU}, Bit 1: I_{PU} SOR	**IMP Port Mode.** Sets the mode of the IMP port based on the value of the pins at power-on reset. 00 = RGMII mode 01 = MII mode 10 = RvMII mode 11 = GMII mode
IMP_DUPLEX	I_{PU}	IMP Port Duplex Mode. 0 = IMP in half-duplex mode 1 = IMP in full-duplex mode
IMP_LINK	I_{PD}	IMP Port Link. 0 = IMP link-down 1 = IMP link-up
IMP_PAUSE_CAP_RX	I_{PU}	**Enable IMP Port Pause Capable in RX.** 0 = Disable Pause capable 1 = Enable Pause capable
IMP_PAUSE_CAP_TX	I_{PU}	Enable IMP Port Pause Capable in TX. 0 = Disable Pause capable 1 = Enable Pause capable
IMP_VOL_SEL[1:0]	I_{PD}	**IMP Interface Voltage Control.** RGMII needs to be set to 01 for 2.5V, GMII/MII/RvMII needs to be set to 00 for 3.3V. 00: 3.3V 01: 2.5V 10: Reserved 11: Reserved
EN_CLK25_OUT/ CLK25_OUT	O, I_{PD}, SOR	**Enable CLK25 Out and CLK_25 Output.** En_CLK25_Out is a strap pin function. 0 = Disable clock out 1 = Enable clock out
EN_CLK50_OUT/ CLK50_OUT	O, I_{PD}, SOR	**Enable CLK50 Out and CLK_50 Output.** En_CLK50_Out is a strap pin function. 0 = Disable clock out 1 = Enable clock out
ACT_LOOP_DET	I_{PD}	**Loop Detection Feature Activation.**
LOOP_DETECTED	O_{PD}	**Loop Found.** This signal is to indicate there is a loop detected in the local network connection.

Table 30: Signal Type Definitions (Cont.)

Signal Name	***Type***	***Description***
LED Interface		
LEDP0	O	**Port 7 Parallel LED Indicators.** Active low.
LEDP1	O	**Port 7 Parallel LED Indicators.** Active low.
LEDP2	O	**Port 7 Parallel LED Indicators.** Active high.
LEDP3/En_Green	O, I_{PD}, SOR	This is a dual function pin: **Port 7 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. Green Mode Enable. Sampled on reset. 1= Enable Green mode 0= Disable Green mode
LEDP4	O	**Port 6 parallel LED Indicators.** Active low.
LEDP5	O	**Port 6 parallel LED Indicators.** Active low.
LEDP6	O	**Port 6 parallel LED Indicators.** Active low.
LEDP7	O	**Port 6 parallel LED Indicators.** Active high.
LEDP8	O	**Port 5 parallel LED Indicators.** Active low.
LEDP9	O	**Port 5 parallel LED Indicators.** Active low.
LEDP10/ EEPROM_TYPE0	O, I_{PD}, SOR	This is a dual function pin. **Port 5 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Extended EEPROM Interface Selection.** Sampled on reset. EEPROM_TYPE[1:0] = 00: Supports 93C46 EEPROM EEPROM_TYPE[1:0] = 01: Supports 93C56 EEPROM EEPROM_TYPE[1:0] = 10: Supports 93C66 EEPROM EEPROM_TYPE[1:0] = 11: Supports 93C86 EEPROM
LEDP11/ EEPROM_TYPE1	O, I_{PD}, SOR	This is a dual function pin. **Port 5 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Extended EEPROM Interface Selection.** Sampled on reset. EEPROM_TYPE [1:0] = 00: Supports 93C46 EEPROM EEPROM_TYPE [1:0] = 01: Supports 93C56 EEPROM EEPROM_TYPE [1:0] = 10: Supports 93C66 EEPROM EEPROM_TYPE [1:0] = 11: Supports 93C86 EEPROM
LEDP12	O	**Port 4 parallel LED Indicators.** Active low.
LEDP13	O	**Port 4 parallel LED Indicators.** Active low.
LEDP14/ LOOP_DET_EN	O, I_{PD}, SOR	This is a dual function pin. **Port 4 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Enable Loop Detection Mode.** Sampled on reset.

Table 30: Signal Type Definitions (Cont.)

Signal Name	***Type***	***Description***
LEDP15/ LOOP_IMP_SEL	O, I_{PD}, SOR	This is a dual function pin. **Port 4 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Exclude IMP Port in Loop Detection Function.** Sampled on reset. 0 = Exclude IMP port from loop detection function 1 = Include IMP port in loop detection function
LEDP16	O	**Port 3 Parallel LED Indicators.** Active low.
LEDP17	O	**Port 3 Parallel LED Indicators.** Active low.
LEDP18/ BC_SUPP_EN	O, I_{PD}, SOR	This is a dual function pin. **Port 3 Parallel LED Indicators.** Polarity determined at reset. "Dual Input Configuration/LED Output Function" on page 120. **Broadcast Suppression Enable.** Sampled on reset. See "Rate Control" on page 44 for more information. 0=Disable rate-based broadcast suppression. 1=Enable rate-based broadcast suppression.
LEDP19	O	**Port 3 Parallel LED Indicators.** Active high.
LEDP20	O	**Port 2 Parallel LED Indicators.** Active low.
LEDP21	O	**Port 2 Parallel LED Indicators.** Active low.
LEDP22/ DIS_IMP	O, I_{PD}, SOR	This is a dual function pin. **Port 2 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Disables IMP Port.** Sampled on reset. 0 = Enable IMP port 1 = Disable IMP port, and external pull-up resister is required.
LEDP23/ IMP_DUMB_FWDG_EN	O, I_{PD}, SOR	This is a dual function pin. **Port 2 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **IMP Port in Blocking State for Unmanaged Mode.** Sampled on reset. When this pin is pulled up, the IMP port is not in management mode, the IMP port is in a regular port. 0 = Blocking for dumb mode 1 = Forwarding for dumb mode
LEDP24	O	**Port 1 Parallel LED Indicators.** Active low.
LEDP25	O	**Port 1 Parallel LED Indicators.** Active low.
LEDP26/ ENFDXFLOW	O, I_{PU}, SOR	This is a dual function pin. **Port 1 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Enable Automatic Full-Duplex Flow Control.** Sampled on reset. In combination with the results of auto-negotiation, sets the flow control mode. See "Flow Control" on page 67 for more information.

Table 30: Signal Type Definitions (Cont.)

Signal Name	*Type*	*Description*
LEDP27/ ENHDXFLOW	O, I_{PU}, SOR	This is a dual function pin. **Port 1 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **Enable Automatic Backpressure.** Sampled on reset. When this pin is pulled high, it enables half-duplex backpressure flow control when a port is configured to half-duplex. See "Flow Control" on page 67.
LEDP28	O	**Port 0 Parallel LED Indicators.** Active low.
LEDP29	O	**Port 0 Parallel LED Indicators.** Active low.
LEDP30/ IMP_TXC_DELAY	O, I_{PD}, SOR	This is a dual function pin. **Port 0 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **TXCLK Clock Timing Delay.** Sampled on reset. Active high. This pin enables the TXCLK to data timing delay in RGMII mode. See "RGMII Interface Timing" on page 287.
LEDP31/ IMP_RXC_DELAY	O, I_{PD}, SOR	This is a dual function pin. **Port 0 Parallel LED Indicators.** Polarity determined at reset. See "Dual Input Configuration/LED Output Function" on page 120. **RXCLK Clock Timing Delay.** Sampled on reset. Active high. This pin enables the RXCLK to data-sampling timing delay. See "RGMII Interface Timing" on page 287.
LEDCLK	O_{PD}	**LED Shift Clock.** This clock is periodically active to enable LEDDATA to shift into external registers.
LEDDATA	O_{PD}	**Serial LED Data Output.** Serial LED data for all ports is shifted out when LEDCLK is active. LEDMODE[1:0] pins set the serial data content. See "LED Interface" on page 129 for a functional description of this signal.
Programming Interfaces		
SCK	I_{PD}	**SPI Serial Clock.** The clock input to the BCM53118 SPI interface is supplied by the SPI master, which supports up to 2 MHz, and is enabled if CPU_EPROM_SEL is high during power-on reset.
	O_{PD}	**EEPROM Serial Clock.** The clock output to an external EEPROM device, and is enabled if CPU_EPROM_SEL is low during power-on reset. See the programming interfaces for more information.
SS/CS	I_{PU}	**SPI Slave Select.** Active low signal which enables an SPI interface read or write operation. Enable if CPU_EPROM_SEL is high during power-on reset.
	O_{PU}	**EEPROM Chip Select.** Active high control signal that enables a read operation from an external EEPROM device. Enable if CPU_EPROM_SEL is low during power-on reset. See the programming interfaces for more information.

Table 30: Signal Type Definitions (Cont.)

Signal Name	*Type*	*Description*
MOSI/DI	I_{PU}	**SPI Master-Out/Slave-in.** Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. Enabled if CPU_EPROM_SEL is high during power-on reset.
	O_{PU}	**EEPROM Data In.** Serial data input of an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset. See the programming interfaces for more information.
MISO/DO	O_{PU}	**SPI Master-In/Slave-Out.** Output signal which transmits serial data during an SPI interface read operations. Enabled if CPU_EPROM_SEL is high during power-on reset.
	I_{PU}	**EEPROM Data Out.** Serial data output of an external EEPROM device. Enable if CPU_EPROM_SEL is low during power-on reset. See the programming interfaces for more information.
Serial Flash Interfaces		
FSO	O_{PD}	**Serial Data Output.**
FCSB	O_{PD}	**Chip Select.**
FCLK	O	**Clock Output.**
FSI	I_{PD}	**Serial Data Input.**
Interrupt Pin		
INT	O_{3S}	**Link Status Change Interrupt.** If the interrupt is enabled, this pin asserted low when link status change occurs. This pin will be tri-state after reading Link Status Register (Page 01h: Address 02h).
Bias		
GPHY1_RDAC	B	A 1.24-k Ω resistor to GND is required.
GPHY2_RDAC	B	A 1.24-k Ω resistor to GND is required.
Power Interfaces		
AVDDH	PWR	3.3V Analog I/O Power.
AVDDL	PWR	1.2V Analog Core Power.
DVDD	PWR	1.2V Digital Core Power.
OVDD	PWR	**Power for GMII/RGMII/MII/RvMII of IMP.** Depends on IMP_VOL_SEL[1:0] configuration. 3.3V if IMP_VOL_SEL[1:0] = 00 2.5V if IMP_VOL_SEL[1:0] = 01
OVDD2	PWR	3.3V Digital I/O Power.
GPHY1_BAVDD	PWR	3.3V Analog Power.
GPHY2_BAVDD	PWR	3.3V Analog Power.
PLL_AVDD	PWR	1.2V Analog Power.
GPHY1_PLLDVDD	PWR	1.2V Analog Power.
GPHY2_PLLDVDD	PWR	1.2V Analog Power.
XTAL_AVDD	PWR	3.3V Analog Power.

Table 30: Signal Type Definitions (Cont.)

Signal Name	***Type***	***Description***
IMP_VOL_REF	PWR	**IMP Interface Reference Power.** Connect this pin to ground.
PLL_AVSS	GND	Shared Digital Ground.
XTAL_AVSS	GND	Shared Digital Ground.
EXPOSEPAD	GND	Ground.
No Connect		
NC	DNC	Do not connect.

Section 6: Pin Assignment

BCM53118KQLE Pin List by Signal Name

Table 31: BCM53118KQLE Pin List by Signal Name

Signal	Ball
ACT_LOOP_DETECT	59
AVDDH	74
AVDDH	80
AVDDH	86
AVDDH	92
AVDDH	103
AVDDH	109
AVDDH	115
AVDDH	121
AVDDH	203
AVDDH	209
AVDDH	215
AVDDH	221
AVDDH	232
AVDDH	238
AVDDH	244
AVDDH	250
AVDDL	71
AVDDL	77
AVDDL	83
AVDDL	89
AVDDL	95
AVDDL	100
AVDDL	106
AVDDL	112
AVDDL	118
AVDDL	124
AVDDL	200
AVDDL	206
AVDDL	212
AVDDL	218
AVDDL	224
AVDDL	229
AVDDL	235
AVDDL	241
AVDDL	247
AVDDL	253
CLK_FREQ0	14
CLK_FREQ1	15
CPU_EEPROM_SEL	18
DVDD	16
DVDD	27
DVDD	31
DVDD	40
DVDD	53
DVDD	135
DVDD	148
DVDD	162
DVDD	169
DVDD	183
EN_CLK25_OUT/ CLK25_OUT	26
EN_CLK50_OUT/ CLK50_OUT	21
GPHY1_BVDD	227
GPHY1_PLLVDD	226
GPHY1_RDAC	228
GPHY2_BVDD	97
GPHY2_PLLVDD	98
GPHY2_RDAC	96
HW_FWDG_EN	9
IMP_COL	159
IMP_CRS	143
IMP_DUPLEX	52
IMP_GTXCLK	132
IMP_LINK	54
IMP_MODE0	7
IMP_MODE1	8
IMP_PAUSECAP_RX	55
IMP_PAUSECAP_TX	56
IMP_RXCLK	144
IMP_RXD0	150
IMP_RXD1	151
IMP_RXD2	152
IMP_RXD3	154
IMP_RXD4	155
IMP_RXD5	156
IMP_RXD6	157
IMP_RXD7	158
IMP_RXDV	149
IMP_RXER	147
IMP_SPEED0	51
IMP_SPEED1	50
IMP_TXCLK	141
IMP_TXD0	137
IMP_TXD1	136
IMP_TXD2	134
IMP_TXD3	131
IMP_TXD4	130
IMP_TXD5	128
IMP_TXD6	127
IMP_TXD7	126
IMP_TXEN	139
IMP_TXER	140
IMP_VOL_REF	146
IMP_VOL_SEL0	49
IMP_VOL_SEL1	48
INTR_B	60
LEDCLK	167
LEDDATA	166
LEDMODE0	12
LEDMODE1	13
LEDP0	168
LEDP1	170
LEDP10/ EPROM_TYPE0	181
LEDP11/ EPROM_TYPE1	182
LEDP12	184
LEDP13	185
LEDP14/ LOOP_DETECT_EN	186
LEDP15/ LOOP_IMP_SEL	188
LEDP16	189
LEDP17	190
LEDP18/ BC_SUPP_EN	191
LEDP19	192
LEDP2	171
LEDP20	194
LEDP21	195
LEDP22/DIS_IMP	196
LEDP23/ IMP_DUMB_FWDG_ EN	197
LEDP24	198
LEDP25	199
LEDP26/ ENFDXFLOW	254
LEDP27/ ENHDXFLOW	255
LEDP28	256
LEDP29	1
LEDP3/EN_GREEN	172
LEDP30/ IMP_TXC_DELAY	2
LEDP31/ IMP_RXC_DELAY	4
LEDP4	174
LEDP5	175
LEDP6	176

Signal	Ball
LEDP7	177
LEDP8	178
LEDP9	179
LOOP_DETECTED	58
MDC	62
MDIO	61
MISO	161
MOSI	164
NC	42
NC	45
NC	20
FCSB	65
FSCLK	66
FSI	67
FSO	64
NC	38
NC	5
NC	6
NC	47
NC	37
NC	39
NC	28
NC	46
NC	225
NC	99
NC	70
NC	69
NC	41
NC	10
OVDD	125
OVDD	129
OVDD	133
OVDD	138
OVDD	142
OVDD	145
OVDD	153
OVDD2	3
OVDD2	11
OVDD2	19
OVDD2	43
OVDD2	44
OVDD2	57
OVDD2	63

Signal	Ball
OVDD2	68
OVDD2	165
OVDD2	173
OVDD2	180
OVDD2	187
OVDD2	193
PLL_AVDD	29
PLL_AVSS	30
RESET	17
SCK	163
SS	160
TCK	24
TDI	23
TDO	22
TMS	25
TRD[0]-{0}	202
TRD[0]-{1}	222
TRD[0]-{2}	231
TRD[0]-{3}	251
TRD[0]-{4}	73
TRD[0]-{5}	93
TRD[0]-{6}	102
TRD[0]-{7}	122
TRD[0]+{0}	201
TRD[0]+{1}	223
TRD[0]+{2}	230
TRD[0]+{3}	252
TRD[0]+{4}	72
TRD[0]+{5}	94
TRD[0]+{6}	101
TRD[0]+{7}	123
TRD[1]-{0}	204
TRD[1]-{1}	220
TRD[1]-{2}	233
TRD[1]-{3}	249
TRD[1]-{4}	75
TRD[1]-{5}	91
TRD[1]-{6}	104
TRD[1]-{7}	120
TRD[1]+{0}	205
TRD[1]+{1}	219
TRD[1]+{2}	234
TRD[1]+{3}	248

Signal	Ball
TRD[1]+{4}	76
TRD[1]+{5}	90
TRD[1]+{6}	105
TRD[1]+{7}	119
TRD[2]-{0}	208
TRD[2]-{1}	216
TRD[2]-{2}	237
TRD[2]-{3}	245
TRD[2]-{4}	79
TRD[2]-{5}	87
TRD[2]-{6}	108
TRD[2]-{7}	116
TRD[2]+{0}	207
TRD[2]+{1}	217
TRD[2]+{2}	236
TRD[2]+{3}	246
TRD[2]+{4}	78
TRD[2]+{5}	88
TRD[2]+{6}	107
TRD[2]+{7}	117
TRD[3]-{0}	210
TRD[3]-{1}	214
TRD[3]-{2}	239
TRD[3]-{3}	243
TRD[3]-{4}	81
TRD[3]-{5}	85
TRD[3]-{6}	110
TRD[3]-{7}	114
TRD[3]+{0}	211
TRD[3]+{1}	213
TRD[3]+{2}	240
TRD[3]+{3}	242
TRD[3]+{4}	82
TRD[3]+{5}	84
TRD[3]+{6}	111
TRD[3]+{7}	113
TRST	36
XTAL_AVDD	35
XTAL_AVSS	32
XTALI	34
XTALO	33
EXPOSEPAD	H

BCM53118KQLE Pin List by Ball Name

Table 32: BCM53118KQLE Pin List by Signal Name

Ball	Signal
1	LEDP29
2	LEDP30/ IMP_TXC_DELAY
3	OVDD2
4	LEDP31/ IMP_RXC_DELAY
5	NC
6	NC
7	IMP_MODE0
8	IMP_MODE1
9	HW_FWDG_EN
10	NC
11	OVDD2
12	LEDMODE0
13	LEDMODE1
14	CLK_FREQ0
15	CLK_FREQ1
16	DVDD
17	RESET
18	CPU_EEPROM_SEL
19	OVDD2
20	NC
21	EN_CLK50_OUT/ CLK50_OUT
22	TDO
23	TDI
24	TCK
25	TMS
26	EN_CLK25_OUT/ CLK25_OUT
27	DVDD
28	NC
29	PLL_AVDD
30	PLL_AVSS
31	DVDD
32	XTAL_AVSS
33	XTALO
34	XTALI
35	XTAL_AVDD
36	TRST
37	NC
38	NC
39	NC
40	DVDD
41	NC
42	NC
43	OVDD2
44	OVDD2
45	NC
46	NC
47	NC
48	IMP_VOL_SEL1
49	IMP_VOL_SEL0
50	IMP_SPEED1
51	IMP_SPEED0
52	IMP_DUPLEX
53	DVDD
54	IMP_LINK
55	IMP_PAUSECAP_RX
56	IMP_PAUSECAP_TX
57	OVDD2
58	LOOP_DETECTED
59	ACT_LOOP_DETECT
60	INTR_B
61	MDIO
62	MDC
63	OVDD2
64	FSO
65	FCSB
66	FSCLK
67	FSI
68	OVDD2
69	NC
70	NC
71	AVDDL
72	TRD[0]+{4}
73	TRD[0]-{4}
74	AVDDH
75	TRD[1]-{4}
76	TRD[1]+{4}
77	AVDDL
78	TRD[2]+{4}
79	TRD[2]-{4}
80	AVDDH
81	TRD[3]-{4}
82	TRD[3]+{4}
83	AVDDL
84	TRD[3]+{5}
85	TRD[3]-{5}
86	AVDDH
87	TRD[2]-{5}
88	TRD[2]+{5}
89	AVDDL
90	TRD[1]+{5}
91	TRD[1]-{5}
92	AVDDH
93	TRD[0]-{5}
94	TRD[0]+{5}
95	AVDDL
96	GPHY2_RDAC
97	GPHY2_BVDD
98	GPHY2_PLLVDD
99	NC
100	AVDDL
101	TRD[0]+{6}
102	TRD[0]-{6}
103	AVDDH
104	TRD[1]-{6}
105	TRD[1]+{6}
106	AVDDL
107	TRD[2]+{6}
108	TRD[2]-{6}
109	AVDDH
110	TRD[3]-{6}
111	TRD[3]+{6}
112	AVDDL
113	TRD[3]+{7}
114	TRD[3]-{7}
115	AVDDH
116	TRD[2]-{7}
117	TRD[2]+{7}
118	AVDDL
119	TRD[1]+{7}
120	TRD[1]-{7}
121	AVDDH
122	TRD[0]-{7}
123	TRD[0]+{7}
124	AVDDL
125	OVDD
126	IMP_TXD7
127	IMP_TXD6
128	IMP_TXD5
129	OVDD
130	IMP_TXD4
131	IMP_TXD3
132	IMP_GTXCLK
133	OVDD
134	IMP_TXD2
135	DVDD
136	IMP_TXD1
137	IMP_TXD0
138	OVDD
139	IMP_TXEN
140	IMP_TXER
141	IMP_TXCLK
142	OVDD
143	IMP_CRS
144	IMP_RXCLK
145	OVDD
146	IMP_VOL_REF
147	IMP_RXER
148	DVDD
149	IMP_RXDV
150	IMP_RXD0
151	IMP_RXD1
152	IMP_RXD2
153	OVDD

Ball	Signal
154	IMP_RXD3
155	IMP_RXD4
156	IMP_RXD5
157	IMP_RXD6
158	IMP_RXD7
159	IMP_COL
160	SS
161	MISO
162	DVDD
163	SCK
164	MOSI
165	OVDD2
166	LEDDATA
167	LEDCLK
168	LEDP0
169	DVDD
170	LEDP1
171	LEDP2
172	LEDP3/EN_GREEN
173	OVDD2
174	LEDP4
175	LEDP5
176	LEDP6
177	LEDP7
178	LEDP8
179	LEDP9
180	OVDD2
181	LEDP10/ EPROM_TYPE0
182	LEDP11/ EPROM_TYPE1
183	DVDD
184	LEDP12
185	LEDP13
186	LEDP14/ LOOP_DETECT_EN
187	OVDD2
188	LEDP15/ LOOP_IMP_SEL
189	LEDP16
190	LEDP17
191	LEDP18/ BC_SUPP_EN
192	LEDP19
193	OVDD2
194	LEDP20
195	LEDP21
196	LEDP22/DIS_IMP
197	LEDP23/ IMP_DUMB_FWDG_ EN
198	LEDP24
199	LEDP25
200	AVDDL
201	TRD[0]+{0}
202	TRD[0]-{0}
203	AVDDH
204	TRD[1]-{0}
205	TRD[1]+{0}
206	AVDDL
207	TRD[2]+{0}
208	TRD[2]-{0}
209	AVDDH
210	TRD[3]-{0}
211	TRD[3]+{0}
212	AVDDL
213	TRD[3]+{1}
214	TRD[3]-{1}
215	AVDDH
216	TRD[2]-{1}
217	TRD[2]+{1}
218	AVDDL
219	TRD[1]+{1}
220	TRD[1]-{1}
221	AVDDH
222	TRD[0]-{1}
223	TRD[0]+{1}
224	AVDDL
225	NC
226	GPHY1_PLLVDD
227	GPHY1_BVDD
228	GPHY1_RDAC
229	AVDDL
230	TRD[0]+{2}
231	TRD[0]-{2}
232	AVDDH
233	TRD[1]-{2}
234	TRD[1]+{2}
235	AVDDL
236	TRD[2]+{2}
237	TRD[2]-{2}
238	AVDDH
239	TRD[3]-{2}
240	TRD[3]+{2}
241	AVDDL
242	TRD[3]+{3}
243	TRD[3]-{3}
244	AVDDH
245	TRD[2]-{3}
246	TRD[2]+{3}
247	AVDDL
248	TRD[1]+{3}
249	TRD[1]-{3}
250	AVDDH
251	TRD[0]-{3}
252	TRD[0]+{3}
253	AVDDL
254	LEDP26/ ENFDXFLOW
255	LEDP27/ ENHDXFLOW
256	LEDP28
H	EXPOSEPAD

Section 7: Register Definitions

Register Definition

BCM53118 register sets can be accessed through the programming interfaces described on page 92. The register space is organized into pages, each containing a certain set of registers. Table 33 lists the pages defined in the BCM53118. To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their addresses. See “Programming Interfaces” on page 92 for more information.

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or to write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Clear on read

Reserved bits must be written as the default value and ignored when read.

Global Page Register

Table 33: Global Page Register Map

Page	*Description*
00h	“Page 00h: Control Registers” on page 140
01h	“Page 01h: Status Registers” on page 157
02h	“Page 02h: Management/Mirroring Registers” on page 161
03h	Reserved
04h	“Page 04h: ARL Control Register” on page 170
05h	“Page 05h: ARL/VTBL Access Registers” on page 175
06h, 07h	Reserved
08h	Reserved

Table 33: Global Page Register Map (Cont.)

Page	Description
09h	Reserved
0Ah	Reserved
0Bh–0Fh	Reserved
10h–17h	"Page 10h–17h: Internal GPHY MII Registers" on page 185
18h–1Fh	Reserved
20h–28h	"Page 20h–28h: Port MIB Registers" on page 221
29h–2Fh	Reserved
30h	"Page 30h: QoS Registers" on page 225
31h	"Page 31h: Port-Based VLAN Registers" on page 235
32h	"Page 32h: Trunking Registers" on page 236
33h	Reserved
34h	"Page 34h: IEEE 802.1Q VLAN Registers" on page 237
35h	Reserved
36h	"Page 36h: DOS Prevent Register" on page 246
37h–3Fh	Reserved
40h	"Page 40h: Jumbo Frame Control Register" on page 249
41h	"Page 41h: Broadcast Storm Suppression Register" on page 251
42h	"Page 42h: EAP Register" on page 257
43h	"Page 43h: MSPT Register" on page 261
44h–6Fh	Reserved
70h	"Page 70h: MIB Snapshot Control Register" on page 264
71h	"Page 71h: Port Snapshot MIB Control Register" on page 264
72h	"Page 72h: Loop Detection Register" on page 265
73h–7Fh	Reserved
80h–83h	Reserved
84h	Reserved
85h	Reserved
86h–87h	Reserved
88h	"Page 88h: IMP Port External PHY MII Registers Page Summary" on page 267
90h	"Page 90h: BroadSync HD Register" on page 267
91h	"Page 91h: Traffic Remarking Register" on page 274
92h–9Fh	Reserved
A0h	Reserved
A1h	Reserved
A2h–EFh	Reserved
Maps to all pages	"Global Registers" on page 276

Page 00h: Control Registers

Table 34: Control Registers (Page 00h)

Address	*Bits*	*Register Name*
00h–07h	8/port	"Port Traffic Control Register (Page 00h: Address 00h)" on page 141
08h	8	"IMP Port Control Register (Page 00h: Address 08h)" on page 142
09h–0Ah	8	Reserved
0Bh	8	"Switch Mode Register (Page 00h: Address 0Bh)" on page 143
0Ch–0Dh	16	Reserved
0Eh	8	"IMP Port State Override Register (Page 00h: Address 0Eh)" on page 143
0Fh	8	"LED Refresh Register (Page 00h: Address 0Fh)" on page 144
10h–11h	16	"LED Function 0 Control Register (Page 00h: Address 10h)" on page 145
12h–13h	16	"LED Function 1 Control Register (Page 00h: Address 12h)" on page 146
14h–15h	16	"LED Function Map Register (Page 00h: Address 14h–15h)" on page 146
16h–17h	16	"LED Enable Map Register (Page 00h: Address 16h–17h)" on page 147
18h–19h	16	"LED Mode Map 0 Register (Page 00h: Address 18h–19h)" on page 147
1Ah–1Bh	16	"LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)" on page 147
1Ch	–	Reserved
1Dh	8	"PHY LED Control Register (Page 00h: Address 1Dh)" on page 148
1Eh	–	Reserved
1Fh	8	Reserved
20h	–	Reserved
21h	8	"Port Forward Control Register (Page 00h: Address 21h)" on page 148
22h–23h	–	Reserved
24h–25h	16	"Protected Port Selection Register (Page 00h: Address 24h–25h)" on page 148
26h–27h	16	"WAN Port Select Register (Page 00h: Address 26h–27h)" on page 149
28h–2Bh	32	"Pause Capability Register (Page 00h: Address 28h–2Bh)" on page 149
2Ch–2Eh	–	Reserved
2Fh	8	"Reserved Multicast Control Register (Page 00h: Address 2Fh)" on page 149
30h	–	Reserved
31h	8	Reserved
32h–33h	16	"Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)" on page 151
34h–35h	16	"Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)" on page 151
36h–37h	16	"MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)" on page 152
38h–39h	16	"Pause Pass Through for RX Register (Page 00h: Address 38h–39h)" on page 152
3Ah–3Bh	16	"Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)" on page 152

Table 34: Control Registers (Page 00h) (Cont.)

Address	Bits	Register Name
3Ch–3Dh	16	"Disable Learning Register (Page 00h: Address 3Ch–3Dh)" on page 152
3Eh–3Fh	16	"Software Learning Register (Page 00h: Address 3Eh–3Fh)" on page 153
40h–49h	–	Reserved
4Ah–4Bh	–	Reserved
4Ch–57h	–	Reserved
58h–5Fh	8/port	"Port State Override Register (Page 00h: Address 58h)" on page 153
60h–65h	–	Reserved
66h–74h	–	Reserved
75h	–	Reserved
78h	–	"MDIO IMP Port Address Register (Page 00h: Address 78h)" on page 154
79h	–	"Software Reset Control Register (Page 00h: Address 79h)" on page 155
7Ah–7Fh	–	Reserved
80h	8	"Pause Frame Detection Control Register (Page 00h: Address 80h)" on page 155
81h–87h	–	Reserved
88h	8	"Fast-Aging Control Register (Page 00h: Address 88h)" on page 155
89h	8	"Fast-Aging Port Control Register (Page 00h: Address 89h)" on page 156
8Ah–8Bh	16	"Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)" on page 156
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0-7
F8h–FDh	–	Reserved
8Ch–EFh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Port Traffic Control Register (Page 00h: Address 00h)

Table 35: Port Traffic Control Register Address Summary

Address	Description
00h	Port 0
01h	Port 1
02h	Port 2
03h	Port 3
04h	Port 4
05h	Port 5
06h	Port 6
07h	Port 7

Table 36: Port Control Register (Page 00h: Address 00h–07h)

BIt	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	CPU writes the current computed states of its spanning tree algorithm for a given port. 000 = No spanning tree (default for unmanaged mode) 001 = Disabled state (default for managed mode) 010 = Blocking state 011 = Listening state 100 = Learning state 101 = Forwarding state 110–111= Reserved	~ HW_FWDG_EN
4:2	Reserved	–	–	000
1	TX_DISABLE	R/W	0 = Enable the transmit function of the port at the MAC level. 1 = Disable the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	0 = Enable the receive function of the port at the MAC level. 1 = Disable the receive function of the port at the MAC level.	0

IMP Port Control Register (Page 00h: Address 08h)

Table 37: IMP Port Control Register (Page 00h: Address 08h)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	–	–
4	RX_UCST_EN	R/W	Receive unicast enable Allow unicast frames to be forwarded to the IMP, when the IMP is configured as the frame management port, and the frame was matching address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the Frame Management Port.	0
3	RX_MCST_EN	R/W	Receive multicast enable Allow multicast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port.	0

Table 37: IMP Port Control Register (Page 00h: Address 08h) (Cont.)

Bit	Name	R/W	Description	Default
2	RX_BCST_EN	R/W	Receive broadcast enable Allow broadcast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port.	0
1:0	Reserved	R/W	–	0

Switch Mode Register (Page 00h: Address 0Bh)

Table 38: Switch Mode Register (Page 00h: Address 0Bh)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	–	000001
1	SW_FWDG_EN	R/W	Software forwarding enable SW_FWDG_EN = 1: Frame forwarding is enabled. SW_FWDG_EN = 0: Frame forwarding is disabled. Managed switch implementations should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters before frame forwarding is enabled.	HW_FWDG_EN
0	SW_FWDG_MODE	R/W	Software forwarding mode 0 = Unmanaged mode. 1 = Managed mode. The ARL treats reserved multicast addresses differently depending on this selection.	~HW_FWDG_EN

IMP Port State Override Register (Page 00h: Address 0Eh)

Table 39: IMP Port State Override Register (Page 00h: Address 0Eh)

Bit	Name	R/W	Description	Default
7	MII_SW_OR	R/W	MII software override 0 = Use MII hardware pin status. 1 = Use contents of this register.	0
6	Reserved	R/W	Reserved	0
5	Tx Flow Control Capability	RO	Link partner flow control capability 0 = Not PAUSE capable 1 = PAUSE capable	0

Table 39: IMP Port State Override Register (Page 00h: Address 0Eh)

Bit	Name	R/W	Description	Default
4	Rx Flow Control Capability	R/W	Link partner flow control capability 0 = Not PAUSE-capable 1 = PAUSE-capable	0
3:2	SPEED	R/W	Speed 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps	10
1	FDX	R/W	Full-duplex 0 = Half-duplex 1 = Full-duplex	1
0	LINK	R/W	Link status 0 = Link fail 1 = Link pass	0

LED Control Register (Page 00h: Address 0Fh–1Bh)

Table 40: LED Control Register Address Summary

Address	Description
0Fh	LED refresh control register
10h–11h	LED function 0 control register
12h–13h	LED function 1 control register
14h–15h	LED function map control register
16h–17h	LED enable map register
18h–19h	LED mode map 0 register
1Ah–1Bh	LED mode map 1 register

LED Refresh Register (Page 00h: Address 0Fh)

Table 41: LED Refresh Register (Page 00h: Address 0Fh)

Bit	Name	R/W	Description	Default
7	LED_EN	R/W	Enable LED	1
6	POST_EXEC	R/W	Write 1 to re-start POST.	0
5	POST_PSCAN_EN	R/W	When enabled, switch scans the port during the POST period.	0
4	POSt_Cable_diag_en	R/W	Enable cable diagnostics display during POST	0
3	Normal_Cable_diag_en	R/W	Enable cable diagnostics display in normal mode	0

Table 41: LED Refresh Register (Page 00h: Address 0Fh) (Cont.)

Bit	Name	R/W	Description	Default
2:0	LED_Refresh_rate	R/W	LED refresh count register (i.e., LED blinking rate) Refresh time = (N+1) * 10 ms • 000: Reserved • 001: 20 ms/25 Hz • 010: 30 ms/16 Hz • 011: 40 ms/12 Hz • 100: 50 ms/10 Hz • 101: 60 ms/8 Hz • 110: 70 ms/7 Hz • 111: 80 ms/6 Hz	3h

LED Function 0 Control Register (Page 00h: Address 10h)

Table 42: LED Function 0 Control Register (Page 00h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:0	LED_FUNCTION	R/W	The following is the list of functions assigned to each bit: 15: Reserved 14: BroadSync HD Link 13: 1G/ACT 12: 10/100M/ACT 11: 100M/ACT 10: 10M/ACT 9: SPD1G 8: SPD100M 7: SPD10M 6: DPX/COL 5: LNK/ACT 4: COL 3: ACT 2: DPX 1: LNK 0: Reserved	LED MODE[1:0] = 00: 16'h0120 LED MODE[1:0] = 01: 16'h0C40 LED MODE[1:0] = 10: 16'h0124 LED MODE[1:0] = 11: 16'h0C04

LED Function 1 Control Register (Page 00h: Address 12h)

Table 43: LED Function 1 Control Register (Page 00h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15:0	LED_FUNCTION	R/W	The following is the list of functions assigned to each bit: 15: Reserved 14: BroadSync HD Link 13: 1G/ACT 12: 10/100M/ACT 11: 100M/ACT 10: 10M/ACT 9: SPD1G 8: SPD100M 7: SPD10M 6: DPX/COL 5: LNK/ACT 4: COL 3: ACT 2: DPX 1: LNK 0: Reserved	LED MODE[1:0] = 00: 16'h0320 LED MODE[1:0] = 01: 16'h3040 LED MODE[1:0] = 10: 16'h0324 LED MODE[1:0] = 11: 16'h2C04

LED Function Map Register (Page 00h: Address 14h–15h)

Table 44: LED Function Map Register (Page 00h: Address 14h–15h)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	LED_FUNC_MAP	R/W	Per port select function bit. Each port LED follows the function table specified for each port. 1: Select Function 1. 0: Select Function 0. Bits [7:0] correspond to ports [7:0].	1FFh

LED Enable Map Register (Page 00h: Address 16h–17h)

Table 45: LED Enable Map Register (Page 00h: Address 16h–17h)

BIt	***Name***	***R/W***	***Description***	***Default***
15:9	Reserved	R/W	–	0
8:0	LED_EN_MAP	R/W	Per port enable bit 1: Enable 0: Disable Bits [7:0] correspond to ports [7:0].	9'h1F

LED Mode Map 0 Register (Page 00h: Address 18h–19h)

Table 46: LED Mode Map 0 Register (Page 00h: Address 18h–19h)

BIt	***Name***	***R/W***	***Description***	***Default***
15:9	Reserved	R/W	–	0
8:0	LED_MODE_MAP0	R/W	Combine with LED_MODE_MAP1 to decide per port LED output mode. Bits [7:0] correspond to ports [7:0].	1FFh

LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)

Table 47: LED Function Map 1 Control Register (Page 00h: Address 1Ah–1Bh)

BIt	***Name***	***R/W***	***Description***	***Default***
15:9	Reserved	R/W	–	0
8:0	LED_MODE_MAP1	R/W	Per port select function bit LED_FUNC_MAP[1:0] 00: LED off 01: LED on 10: LED blinking 11: LED auto	1FFh

See "LED Interfaces" on page 116 for more information.

PHY LED Control Register (Page 00h: Address 1Dh)

Table 48: PHY LED Control Register (Page 00h: Address 1Dh)

Bit	Name	R/W	Description	Default
7:4	PHY_LED_FUNC1	R/W	Bit 7: PHYLED4 of LED Function 1 Bit 6: PHYLED3 of LED Function 1 Bit 5: PHYLED2 of LED Function 1 Bit 4: PHYLED1 of LED Function 1	LED Mode[1:0] = 00: 8'h88 LED Mode[1:0] = 01: 8'h88
3:0	PHY_LED_FUNC0	R/W	Bit 3: PHYLED4 of LED Function 0 Bit 2: PHYLED3 of LED Function 0 Bit 1: PHYLED2 of LED Function 0 Bit 0: PHYLED1 of LED Function 0	LED Mode[1:0] = 10: 8''h00 LED Mode[1:0] = 11: 8'h00

Port Forward Control Register (Page 00h: Address 21h)

Table 49: Port Forward Control Register (Page 00h: Address 21h)

Bit	Name	R/W	Description	Default
7	MCST_DLF_FWD_EN	R/W	1 = Forward multicast lookup failed frames according to multicast lookup failed forward map register (Page 00h: Address 34h) 0 = Flood multicast packet if fail ARL table lookup	0
6	UCST_DLF_FWD_EN	R/W	1 = Forward unicast lookup failed frames according to Unicast Lookup failed forward map register (Page 00h: Address 32h) 0 = Flood unicast packet if fail ARL table lookup	0h
5:1	Reserved	R/W	–	0
0	Reserved	R/W	–	1

See “Egress PCP Remarking” on page 57 for more information.

Protected Port Selection Register (Page 00h: Address 24h–25h)

Table 50: Protected Port Selection Register (Page 00h: Address 24h–25h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	PORT_SELECT	R/W	Protected port selection Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 1 = Port protected. Cannot send/receive to other protected ports. 0 = Port is not protected.	0

See “Protected Ports” on page 47 for more information.

WAN Port Select Register (Page 00h: Address 26h–27h)

Table 51: WAN Port Select Register (Page 00h: Address 26h–27h)

BIt	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9	Reserved	R/W	–	–
8	Reserved	R/W	–	–
7:0	WAN_PORT_MAP	R/W	Set assigned WAN port to 1. Bits [7:0] correspond to ports [7:0], respectively.	0

Pause Capability Register (Page 00h: Address 28h–2Bh)

Table 52: Pause Capability Register (Page 00h: Address 28h–2Bh)

BIt	Name	R/W	Description	Default
31:24	Reserved	RO	–	0
23	EN_OVERIDE	R/W	Forces the content of this register setting to be used over the auto negotiation result.	0
22:18	Reserved	–	–	–
17:9	EN_RX_PAUSE_CAP	–	Enabling the receive pause capability. Bit 17: IMP port Bits [16:9] correspond to ports [7:0], respectively.	0h
8:0	EN_TX_PAUSE_CAP	–	Enables the transmit pause capability. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0h

Reserved Multicast Control Register (Page 00h: Address 2Fh)

Table 53: Reserved Multicast Control Register (Page 00h: Address 2Fh)

BIt	Name	R/W	Description	Default
7	Multicast Learning	R/W	Multicast learning enable 0 = Do not learn unicast source addresses of frames that have a reserved multicast destination address. 1 = Learn unicast source addresses even from frames that have a reserved multicast destination address. See “Address Management” on page 57 for more information.	0
6:5	Reserved	R/W	–	0

Table 53: Reserved Multicast Control Register (Page 00h: Address 2Fh) (Cont.)

BIt	Name	R/W	Description	Default
4	En_Mul_4	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-20 ~ 01-80-C2-00-00-2F 0 = Forward 1 = Drop	0
3	En_Mul_3	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-11 ~ 01-80-C2-00-00-1F 0 = Forward 1 = Drop	0
2	En_Mul_2	R/W	Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-10 0 = Forward 1 = Drop	0
1	En_mul_1	R/W	Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F 0 = Forward 1 = Drop	1
0	En_Mul_0	R/W	Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode. 01-80-C2-00-00-00 0 = Forward 1 = Drop	0

See "Multicast Addresses" on page 60 for more information.

Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)

Table 54: Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	UNI_DLF_MAP	R/W	Unicast lookup failed forward map Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. When the UCST_DLF_FWD_EN bit in "Port Forward Control Register (Page 00h: Address 21h)" on page 148 is enabled and a unicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a unicast lookup failure to this port. 1 = Forward a unicast lookup failure to this port.	0

See "Unicast Addresses" on page 59 for more information.

Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Table 55: Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	MCST_DLF_MAP	R/W	Multicast lookup failed forward map Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. When the MCST_DLF_FWD_EN bit in port forward control register (Page 00h:Address 21h) is enabled and a multicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped. 0 = Do not forward a multicast lookup failure to this port. 1 = Forward a multicast lookup failure to this port.	0

See "Multicast Addresses" on page 60 for more information.

MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)

Table 56: MLF IMPC Forward Map Register (Page 00h: Address 36h–37h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	MLF_IPMC_FWD_MAP	R/W	IPMC forward map Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

Table 57: Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

BIt	Name	R/W	Description	Default
15:8	Reserved	RO	–	0
7:0	IGNORE_PAUSE FRAME _RX	R/W	RX pause pass through map 1: Ignore IEEE 802.3x 0: Comply with IEEE 802.3x pause frame receiving. Bits [7:0] correspond to ports [7:0], respectively.	0

Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

Table 58: Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	IGNORE_PAUSE FRAME _TX	R/W	TX pause pass through map 1: Ignore IEEE 802.3x. 0: Comply with IEEE 802.3x pause frame receiving Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Disable Learning Register (Page 00h: Address 3Ch–3Dh)

Table 59: Disable Learning Register (Page 00h: Address 3Ch–3Dh)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	DIS_LEARNING	R/W	1 = Disable learning 0 = Enable learning Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Software Learning Register (Page 00h: Address 3Eh–3Fh)

Table 60: Software Learning Control Register (Page 00h: Address 3Eh–3Fh)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	–
8:0	SW_LEARN_CNTL	R/W	1: Software learning control enabled. The behaviors are as follows. • Forwarding behavior: Incoming packet with unknown SA will be copied to CPU port. • Learning behavior: Allow S/W to decide whether incoming packet learn or not. In S/W learning mode, the H/W learning mechanism will be disabled automatically. • Refreshed behavior: Allow refreshed mechanism to operate properly even through the H/W learning had been disabled. 0: Software learning control disabled. Forwarding/Learning/Refreshed behavior to keep hardware operation. Bit 8: IMP port Bits [7:0] correspond to ports [7:0]	0

Port State Override Register (Page 00h: Address 58h)

Table 61: Port State Override Register Address Summary

Address	Description
58h	Port 0
59h	Port 1
5Ah	Port 2
5Bh	Port 3
5Ch	Port 4
5Dh	Port 5
5Eh	Port 6
5Fh	Port 7

Table 62: Port State Override Register (Page 00h: Address 58h–5Fh)

BIt	Name	R/W	Description	Default
7	Reserved	R/W	–	–
6	Software Override	R/W	Writing 1 to this bit allows the values of the bits [7:0] to be written to the external PHY. Writing 0 to this bit prevents these values from overriding the present external PHY conditions.	0
5	TXFlow Control Enable	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for transmit traffic. 1 = Flow control enabled for transmit traffic.	0
4	RX Flow Control Enable	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Flow control disabled for receive traffic. 1 = Flow control enabled for receive traffic.	0
3:2	Speed	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Illegal state	10
1	Duplex Mode	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1. 0 = Half-duplex 1 = Full-duplex	1
0	Link State	R/W	The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written 1. 1 = Link-up 0 = Link-down	1

MDIO IMP Port Address Register (Page 00h: Address 78h)

Table 63: MDIO IMP PORT Address Register (Page 00h: Address 78h)

BIt	Name	R/W	Description	Default
7:5	Reserved	RO	–	0
4:0	IMP_MDIO_ADDRESS	R/W	IMP PORT MDIO address	18h

Software Reset Control Register (Page 00h: Address 79h)

Table 64: Software Reset Control Register (Page 00h: Address 79h)

BIt	Name	R/W	Description	Default
7	SW_RST	R/W	Software reset (Bit4 “EN_SW_RST” MUST be enabled as well). Software reset, write “1” to activate a RESET, “0” to clear the reset state. 1 = Activate reset. 0 = Clear reset.	–
6:5	Reserved	–	–	–
4	EN_SW_RST	R/W	Enable software reset.	0
3:0	Reserved	R/W	–	–

Pause Frame Detection Control Register (Page 00h: Address 80h)

Table 65: Pause Frame Detection Control Register (Page 00h: Address 80h)

BIt	Name	R/W	Description	Default
7:1	Reserved	RO	–	0
0	PAUSE_IGNORE_DA	R/W	0 = Check DA field on pause frame detection. 1 = Ignore DA field on pause frame detection.	0

Fast-Aging Control Register (Page 00h: Address 88h)

Table 66: Fast-Aging Control Register (Page 00h: Address 88h)

BIt	Name	R/W	Description	Default
7	Fast_Age_Start/Done	R/W	Set bit to 1 triggers the fast aging process. When the fast aging process is done, this bit is cleared to 0.	0
6	Reserved	–	–	–
5	EN_AGE_MCAST	R/W	Enable Aging Multicast Entry 1: Aging multicast Entries in ARL Table 0: Disable Aging Multicast Entries in ARL Table ***Note:*** The EN_AGE_MCAST and the EN_AGE_Port can not enable (set to 1) at the same time.	0
4	EN_AGE_SPT	R/W	When set, check spanning tree ID.	–
3	EN_AGE_VLAN	R/W	When set, check VLAN ID.	–
2	EN_AGE_Port	R/W	When set, check port ID.	–
1	EN_AGE_Dynamic	R/W	When set, age out dynamic entry.	–
0	EN_AGE_Static	R/W	When set, age out static entry.	–

Fast-Aging Port Control Register (Page 00h: Address 89h)

Table 67: Fast-Aging Port Control Register (Page 00h: Address 89h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	–	0
3:0	Fast Age Single Port	R/W	Fast age single port select Writing bits [3:0] selects the port to be fast-aged.	0

Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Table 68: Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	–	0
11:0	Fast Age Single VID	R/W	Fast age single VID select Writing bits [11:0] selects the VID to be fast-aged.	0

Page 01h: Status Registers

Table 69: Status Registers (Page 01h)

Address	Bits	Register Name
00h–01h	16	"Link Status Summary (Page 01h: Address 00h)" on page 157
02h–03h	16	"Link Status Change (Page 01h: Address 02h)" on page 158
04h–07h	32	"Port Speed Summary (Page 01h: Address 04h)" on page 158
08h–09h	16	"Duplex Status Summary (Page 01h: Address 08h)" on page 159
0Ah–0Dh	32	"Pause Status Summary (Page 01h: Address 0Ah)" on page 159
0Eh–0Fh	16	"Source Address Change Register (Page 01h: Address 0Eh)" on page 160
10h–45h	48/port	"Last Source Address Register (Page 01h: Address 10h)" on page 160
46h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Link Status Summary (Page 01h: Address 00h)

Table 70: Link Status Summary Register (Page 01h: Address 00h–01h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	LINK_STATUS	RO	Link status Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Link fail 1 = Link pass	0

Link Status Change (Page 01h: Address 02h)

Table 71: Link Status Change Register (Page 01h: Address 02h–03h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	LINK_STATUS_CHANGE	RO	Link status change. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link status constant. 1 = Link status change.	0

Port Speed Summary (Page 01h: Address 04h)

Table 72: Port Speed Summary Register (Page 01h: Address 04h–07h)

BIt	Name	R/W	Description	Default
31:18	Reserved	PO	Reserved	0
17:0	PORT_SPEED	RO	Port speed The speed of each port is reported based on the mapping below: • bits [17:16] = IMP port • bits [15:14] = Port 7 • bits [13:12] = Port 6 • bits [11:10] = Port 5 • bits [9:8] = Port 4 • bits [7:6] = Port 3 • bits [5:4] = Port 2 • bits [3:2] = Port 1 • bits [1:0] = Port 0 The value of the bits are: • 00 = 10 Mbps • 01 = 100 Mbps • 10 = 1000 Mbps • 11 = Illegal state	0

Duplex Status Summary (Page 01h: Address 08h)

Table 73: Duplex Status Summary Register (Page 01h: Address 08h–09h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	DUPLEX_STATE	RO	Duplex state Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Half-duplex 1 = Full-duplex	0

Pause Status Summary (Page 01h: Address 0Ah)

Table 74: PAUSE Status Summary Register (Page 01h: Address 0Ah–0Dh)

BIt	Name	R/W	Description	Default
31:18	Reserved	RO	Reserved	0
17:9	RECEIVE_PAUSE_STATE	RO	Pause state. Receive pause capability Bit 17: IMP port Bits [16:9] correspond to ports [7:0], respectively. 0 = Disabled 1 = Enabled	0
8:0	TRANSMIT_PAUSE_STATE	RO	Transmit pause capability Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Disabled 1 = Enabled	

Source Address Change Register (Page 01h: Address 0Eh)

Table 75: Source Address Change Register (Page 01h: Address 0Eh–0Fh)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	SRC_ADDR_CHANGE	RC	Source address change Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. The value of this bit is 1 if a change in the source address is detected on the given port. The bit remains set until cleared by a read operation. 0 = No change in source address since last read. 1 = Source address has changed since last read.	0

Last Source Address Register (Page 01h: Address 10h)

Table 76: Last Source Address Register Address Summary

Address	Description
10h–15h	Port 0
16h–1Bh	Port 1
1Ch–21h	Port 2
22h–27h	Port 3
28h–2Dh	Port 4
2Eh–33h	Port 5
34h–39h	Port 6
3Ah–3Fh	Port 7
40h–45h	IMP port

Table 77: Last Source Address (Page 01h: Address 10h–45h)

BIt	Name	R/W	Description	Default
47:0	LAST_SOURCE_ADD	RO	The 48-bit source address detected on the last packet ingressed.	0

Page 02h: Management/Mirroring Registers

Table 78: Aging/Mirroring Registers (Page 02h)

Address	Bits	Register Name
00h	8	“Global Management Configuration Register (Page 02h: Address 00h)” on page 162
01h–02h	–	Reserved
03h	8	“Broadcom Header Control Register (Page 02h: Address 03h)” on page 162
04h–05h	16	“RMON MIB Steering Register (Page 02h: Address 04h)” on page 163
06h–09h	32	“Aging Time Control Register (Page 02h: Address 06h)” on page 163
0Ah–0Fh	–	Reserved
10h–11h	16	“Mirror Capture Control Register (Page 02h: Address 10h)” on page 163
12h–13h	16	“Ingress Mirror Control Register (Page 02h: Address 12h)” on page 164
14h–15h	16	“Ingress Mirror Divider Register (Page 02h: Address 14h)” on page 165
16h–1Bh	48	“Ingress Mirror MAC Address Register (Page 02h: Address 16h)” on page 165
1Ch–1Dh	16	“Egress Mirror Control Register (Page 02h: Address 1Ch)” on page 166
1Eh–1Fh	16	“Egress Mirror Divider Register (Page 02h: Address 1Eh)” on page 166
20h–25h	48	“Egress Mirror MAC Address Register (Page 02h: Address 20h)” on page 167
26h–EFh	–	Reserved
30h–33h	8	Device ID number
34h–3Fh	–	Reserved
40h	8	Revision ID number
41h–4Fh	–	Reserved
50h–53h	32	“High-Level Protocol Control Register (Page 02h: Address 50h–53h)” on page 168
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 276
FFh	8	“Page Register (Global, Address FFh)” on page 277

Global Management Configuration Register (Page 02h: Address 00h)

Table 79: Global Management Configuration Register (Page 02h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	En_IMP_Port	R/W	IMP port enable 00=No frame management port. 01=Reserved. 10=Enable IMP port only. All traffic to CPU from LAN and WAN ports will be forwarded to IMP port. 11=Reserved. These bits are ignored when SW_FWD_MODE = Unmanaged in the "Switch Mode Register (Page 00h: Address 0Bh)" on page 143.	00
5	Reserved	R/W	–	0
4	Intrpt_En	R/W	Link status change interrupt enable 0 = Disable link status change interrupt 1 = Enable link status change interrupt	0
3:2	Reserved	R/W	–	0
1	En_Rx_BPDU	R/W	Receive BPDU enable Enables all ports to receive BPDUs and forwards to the IMP port. This bit must be set to globally allow BPDUs to be received.	0
0	Reset MIB	R/W	Reset MIB counters Resets all MIB counters for all ports to 0 (pages 20h–28h). This bit must be set and then cleared in successive write cycles to activate the reset operation.	0

Broadcom Header Control Register (Page 02h: Address 03h)

Table 80: Broadcom Tag Control Register (Page 02h: Address 03h)

Bit	Name	R/W	Description	Default
7:1	Reserved	RO	–	0
0	BRCM_HDR_EN	R/W	Broadcom Tag enable for IMP. Enable Broadcom header for IMP port. • 1: Additional header information is inserted into the original frame, between original SA field and Type/ Length fields. The tag includes the Broadcom Tag field. • 0: Without additional header information.	1

RMON MIB Steering Register (Page 02h: Address 04h)

Table 81: RMON MIB Steering Register (Page 02h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	R/W	–	0
8:0	Override RMON Receive	R/W	Override RMON receive Forces the RMON packet size bucket counters from the normal default of snooping on the receive side of the MAC to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Aging Time Control Register (Page 02h: Address 06h)

Table 82: Aging Time Control Register (Page 02h: Address 06h–09h)

BIt	Name	R/W	Description	Default
31:21	Reserved	RO	–	–
20	Age Change	R/W	Age change enable 1 = Set age time via bits [19:0] 0 = Age time default 300s	0
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned addresses. Maximum age time is 1,048,575s. Setting the AGE_TIME to 0 disables the aging process. For more information on ARL table aging, see “Address Aging” on page 64.	300d

Mirror Capture Control Register (Page 02h: Address 10h)

Table 83: Mirror Capture Control Register (Page 02h: Address 10h–11h)

BIt	Name	R/W	Description	Default
15	Mirror Enable	R/W	Global mirror enable 0 = Disable mirror capture feature 1 = Enable mirror capture feature	0
14	BLK_NOT_MIR	R/W	When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked, except for mirror traffic. Nonmirror traffic is disabled. 0 = No traffic blocking on mirror capture port 1 = Traffic to mirror capture port blocked unless mirror traffic	0
13:6	Reserved	RO	–	0

Table 83: Mirror Capture Control Register (Page 02h: Address 10h–11h) (Cont.)

Blt	Name	R/W	Description	Default
5:4	Reserved	R/W	Reserved	0
3:0	Capture Port	R/W	Mirror capture port ID Binary value identifies the single unique port that is designated as the port where all ingress and/or egress traffic is mirrored.	0

For additional information about port mirroring, see “Port Mirroring” on page 47.

Ingress Mirror Control Register (Page 02h: Address 12h)

Table 84: Ingress Mirror Control Register (Page 02h: Address 12h–13h)

Blt	Name	R/W	Description	Default
15:14	IN_MIRROR_FILTER	R/W	Ingress mirror filter Filters frames to be forwarded to the mirror capture port, specified in “Mirror Capture Control Register (Page 02h: Address 10h)” on page 163. 00 = Mirror all ingress frames. 01 = Mirror all ingress frames with DA = IN_MIRROR_MAC. 10 = Mirror all ingress frames with SA = IN_MIRROR_MAC. 11 = Reserved. IN_MIRROR_MAC is specified in “Ingress Mirror MAC Address Register (Page 02h: Address 16h)” on page 165.	0
13	IN_DIV_EN	R/W	Ingress divider enable The ingress divider mirrors every n^{th} ingress frame that has passed through the IN_MIRROR_FILTER (n represents the IN_MIRROR_DIV defined in “Ingress Mirror Divider Register (Page 02h: Address 14h)” on page 165). 0 = Disable ingress divider feature. 1 = Enable ingress divider feature.	0
12:9	Reserved	R/W	–	0
8:0	IN_MIRROR_MASK	R/W	Ingress mirror port mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. Ports with the corresponding bit set to 1 have ingress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an Ingress Mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the ingress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter via bits [15:14] or divider via bit 13 may be helpful.	0

For additional information about port mirroring, see “Port Mirroring” on page 47.

Ingress Mirror Divider Register (Page 02h: Address 14h)

Table 85: Ingress Mirror Divider Register (Page 02h: Address 14h–15h)

BIt	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9:0	IN_MIRROR_DIV	R/W	Ingress mirror divider Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 164 is set, frames that pass the IN_MIRROR_FILTER rule are further divided by n, where n = IN_MIRROR_DIV + 1.	0

For additional information about port mirroring, see "Port Mirroring" on page 47.

Ingress Mirror MAC Address Register (Page 02h: Address 16h)

Table 86: Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)

BIt	Name	R/W	Description	Default
47:0	IN_MIRROR_MAC	R/W	Ingress mirror MAC address MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 164.	0

For additional information about port mirroring, see "Port Mirroring" on page 47.

Egress Mirror Control Register (Page 02h: Address 1Ch)

Table 87: Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)

BIt	Name	R/W	Description	Default
15:14	OUT_MIRROR_FILTER	R/W	Egress mirror filter Filters egress frames that are forwarded to the mirror capture port, specified in "Mirror Capture Control Register (Page 02h: Address 10h)" on page 163. 00 = Mirror all egress frames. 01 = Mirror all egress frames with DA = OUT_MIRROR_MAC. 10 = Mirror all egress frames with SA = OUT_MIRROR_MAC. 11 = Reserved. OUT_MIRROR_MAC is specified in "Egress Mirror MAC Address Register (Page 02h: Address 20h)" on page 167.	0
13	OUT_DIV_EN	R/W	Egress divider enable The egress divider mirrors every n^{th} egress frame that has passed through the OUT_MIRROR_FILTER (n represents the OUT_MIRROR_DIV defined in "Egress Mirror Divider Register (Page 02h: Address 1Eh)" on page 166). 0 = Disable egress divider feature. 1 = Enable egress divider feature.	0
12:9	Reserved	R/W	–	0
8:0	OUT_MIRROR_MASK	R/W	Egress mirror port mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. Ports with the corresponding bit set to 1 have egress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an egress mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the egress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter via bits [15:14] or a divider via bit 13 may be helpful.	0

For additional information about port mirroring, see "Port Mirroring" on page 47.

Egress Mirror Divider Register (Page 02h: Address 1Eh)

Table 88: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)

BIt	Name	R/W	Description	Default
15:10	Reserved	RO	–	0

Table 88: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)

BIt	Name	R/W	Description	Default
9:0	OUT_MIRROR_DIV	R/W	Egress mirror divider Egressed frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 166 is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by n, where n = OUT_MIRROR_DIV + 1.	0

For additional information about port mirroring, see "Port Mirroring" on page 47.

Egress Mirror MAC Address Register (Page 02h: Address 20h)

Table 89: Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)

BIt	Name	R/W	Description	Default
47:0	OUT_MIRROR_MAC	R/W	Egress mirror MAC address MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules defined in "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 166.	0

For additional information about port mirroring, see "Port Mirroring" on page 47.

Device ID Register (Page 02h: Address 30h–33h)

Table 90: Device ID Register (Page 02h: Address 30h–33h)

BIt	Name	R/W	Description	Default
31:0	Device_ID	RO	Device ID	32'0005_3118

Revision Number Register (Page 02h: Address 40h)

Table 91: Egress Mirror MAC Address Register (Page 02h: Address 40h)

BIt	Name	R/W	Description	Default
7:0	Revision_ID	RO	Revision number	0

High-Level Protocol Control Register (Page 02h: Address 50h–53h)

Table 92: High-Level Protocol Control Register (Page 02h: Address 50h–53h)

BIt	Name	R/W	Description	Default
31:19	Reserved	R/W	Reserved	–
18	MLD_QRY_FWD_MODE	R/W	MLD Query Message Forwarding Mode 1: MLD Query message frames will be trapped to CPU port only. 0: MLD Query message frames will be forwarded by L2 result and also copied to CPU.	0
17	MLD_QRY_EN	R/W	MLD Query Message Snooping/Redirect Enable 1: Enable MLD query message snooping/ redirect 0: Disable	0
16	MLD_RPTDONE_FWD_MOD E	R/W	MLD Report/Done Message Forwarding Mode 1: MLD report/done message frames will be trapped to CPU port only 0: MLD report/done message frames will be forwarded by L2 result and also copied to CPU	0
15	MLD_RPTDONE_EN	R/W	MLD Report/Done Message Snooping/Redirect Enable 1: Enable MLD report/done message snooping/ redirect 0: Disable	0
14	IGMP_UKN_FWD_MODE	R/W	IGMP Unknown Message Forwarding Mode 1: IGMP unknown message frames will be trapped to CPU port only 0: IGMP unknown message frames will be forwarded by L2 result and also copied to CPU	0
13	IGMP_UKN_EN	R/W	IGMP Unknown Message Snooping/Redirect Enable 1: Enable IGMP unknown message snooping/ redirect 0: Disable	0
12	IGMP_QRY_FWD_MODE	R/W	IGMP Query Message Forwarding Mode 1: IGMP query message frames will be trapped to CPU port only 0: IGMP query message frames will be forwarded by L2 result and also copied to CPU	0
11	IGMP_QRY_EN	R/W	IGMP Query Message Snooping/Redirect Enable 1: Enable IGMP query message Snooping/ Redirect 0: Disable	0

Table 92: High-Level Protocol Control Register (Page 02h: Address 50h–53h) (Cont.)

BIt	Name	R/W	Description	Default
10	IGMP_RPTLVE_FWD_MODE	R/W	IGMP Report/Leave Message Forwarding Mode 1: IGMP report/leave message frames will be trapped to CPU port only 0: IGMP report/leave message frames will be forwarded by L2 result and also copied to CPU	0
9	IGMP_RPTLVE_EN	R/W	IGMP Report/Leave Message Snooping/Redirect Enable 1: Enable IGMP report/leave message Snooping/Redirect 0: Disable	0
8	IGMP_DIP_EN	R/W	IGMP L3 DIP checking Enable In addition to the IP datagram with a protocol value of 2, IGMP will be classified by matching its DIP with the Class D IP address(224.0.0.0~239.255.255.255).	0
7:6	Reserved	R/W	Reserved	0
5	ICMPv6_FWD_MODE	R/W	ICMPv6 (exclude MLD) Forwarding Mode 1: ICMPv6 frames will be trapped to CPU port only. 0: ICMPv6 frames will be forwarded by L2 result and also copied to CPU.	0
4	ICMPv6_EN	R/W	ICMPv6 (exclude MLD) Snooping/Redirect Enable ICMPv6, with a next header value of 58, will be classified by IPv6 datagram.	0
3	ICMPv4_EN	R/W	ICMPv4 Snooping Enable ICMPv6, with a next header value of 0 and extension header next header value of 58, will be classified by IPv6 datagram. 1: ICMPv4 frames will be forwarded by L2 result and also copied to CPU. 0: ICMPv4 frames will be forwarded by L2 result.	0
2	DHCP_EN	R/W	DHCP Snooping Enable 1: DHCP frames will be forwarded by L2 result and also copied to CPU. 0: DHCP frames will be forwarded by L2 result.	0
1	RARP_EN	R/W	RARP Snooping Enable 1: RARP frames will be forwarded by L2 result and also copied to CPU. 0: RAPR frames will be forwarded by L2 result.	0
0	ARP_EN	R/W	ARP Snooping Enable 1: ARP frames will be forwarded by L2 result and also copied to CPU. 0: ARP frames will be forwarded by L2 result.	0

Page 04h: ARL Control Register

Table 93: ARL Control Registers (Page 04h)

Address	Bits	Register Name
00h	8	"Global ARL Configuration Register (Page 04h: Address 00h)" on page 171
01h–03h	–	Reserved
04h–09h	48	"BPDU Multicast Address Register (Page 04h: Address 04h)" on page 171
0Ah–0Dh	–	Reserved
0Eh–0Fh	16	"Multiport Control Register (Page 04h: Address 0Eh–0Fh)" on page 172
10h–17h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
18h–1Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
1Ch–1Fh	–	Reserved
20h–27h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
28h–2Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
2Ch–2Fh	–	Reserved
30h–37h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
38h–3Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
3Ch–3Fh	–	Reserved
40h–47h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
48h–4Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
4Ch–4Fh	–	Reserved
50h–57h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
58h–5Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
5Ch–5Fh	–	Reserved
60h–67h	64	"Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173
68h–6Bh	32	"Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)" on page 174
6Ch–FEh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Global ARL Configuration Register (Page 04h: Address 00h)

Table 94: Global ARL Configuration Register (Page 04h: Address 00h)

BIt	***Name***	***R/W***	***Description***	***Default***
7:5	Reserved	RO	–	0
4	Reserved	–	–	–
3	Reserved	RO	–	0
2	AGE_Accelerate	R/W	When enabled, the aging time is reduced by 1/128. 1 = Accelerate the aging 128 times 0 = Keep the original age process	–
1	Reserved	RO	–	1
0	Hash Disable	R/W	Hash function disable Disables the hash function of the ARL table so that entries are directly mapped to the table instead of being hashed to an index. 1 = Disable hash function 0 = Enable hash function For more information see "Address Table Organization" on page 58.	0

BPDU Multicast Address Register (Page 04h: Address 04h)

Table 95: BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Bit	***Name***	***R/W***	***Description***	***Default***
47:0	BPDU_MC_ADDR	R/W	BPDU multicast address 1 Defaults to the IEEE 802.1 defined reserved multicast address for the bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address are forwarded to the designated management port.	01-80-c2-00-00-00

Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Table 96: Multiport Control Register (Page 04h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	MPORT0_TS-EN	R/W	Mport 0 Time Sync Enable 1: Packet will be time-stamped if forwarded to CPU. MPORT_VECTOR0 should be programmed to CPU only if this bit is set. 0: Packet will not be time-stamped	0
14:12	Reserved	RO	Reserved	0
11:10	MPORT_CTRL5	R/W	Multiport 5 Control 00: Disable Multiport 5 Forward. 10: Compare MPORT_ADD5 only; Forward based on MPORT_Vector 5 if matched. 01: Compare MPORT_ETYPE5 only; Forward based on MPORT_Vector 5 if matched. 11: Compare MPORT_ETYPE5 and MPORT_ADD5; Forward based on MPORT_Vector 5 if matched.	00
9:8	MPORT_CTRL4	R/W	Multiport 4 Control 00: Disable Multiport 4 Forward. 10: Compare MPORT_ADD4 only; Forward based on MPORT_Vector 4 if matched. 01: Compare MPORT_ETYPE4 only; Forward based on MPORT_Vector 4 if matched. 11: Compare MPORT_ETYPE4 and MPORT_ADD4; Forward based on MPORT_Vector 4 if matched.	00
7:6	MPORT_CTRL3	R/W	Multiport 3 Control 00: Disable Multiport 3 Forward. 10: Compare MPORT_ADD3 only; Forward based on MPORT_Vector 3 if matched. 01: Compare MPORT_ETYPE3 only; Forward based on MPORT_Vector 3 if matched. 11: Compare MPORT_ETYPE3 and MPORT_ADD3; Forward based on MPORT_Vector 3 if matched.	00
5:4	MPORT_CTRL2	R/W	Multiport 2 Control 00: Disable Multiport 2 Forward. 10: Compare MPORT_ADD2 only; Forward based on MPORT_Vector 2 if matched. 01: Compare MPORT_ETYPE2 only; Forward based on MPORT_Vector 2 if matched. 11: Compare MPORT_ETYPE2 and MPORT_ADD2; Forward based on MPORT_Vector 2 if matched.	00

Table 96: Multiport Control Register (Page 04h: Address 0Eh–0Fh) (Cont.)

Bit	Name	R/W	Description	Default
3:2	MPORT_CTRL1	R/W	Multiport 1 Control 00: Disable Multiport 1 Forward. 10: Compare MPORT_ADD1 only; Forward based on MPORT_Vector 1 if matched. 01: Compare MPORT_ETYPE1 only; Forward based on MPORT_Vector 1 if matched. 11: Compare MPORT_ETYPE1 and MPORT_ADD1; Forward based on MPORT_Vector 1 if matched.	00
1:0	MPORT_CTRL0	R/W	Multiport 0 Control 00: Disable Multiport 0 Forward. 10: Compare MPORT_ADD0 only; Forward based on MPORT_Vector 0 if matched. 01: Compare MPORT_ETYPE0 only; Forward based on MPORT_Vector 0 if matched. 11: Compare MPORT_ETYPE0 and MPORT_ADD0; Forward based on MPORT_Vector 0 if matched.	00

Multiport Address N (N=0–5) Register (Page 04h: Address 10h)

Table 97: Multiport Address Register Address Summary

Address	Description
10h–17h	Multiport ETYPE Address 0
20h–27h	Multiport ETYPE Address 1
30h–37h	Multiport ETYPE Address 2
40h–47h	Multiport ETYPE Address 3
50h–57h	Multiport ETYPE Address 4
60h–67h	Multiport ETYPE Address 5

Table 98: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h)

BIt	Name	R/W	Description	Default
64:48	MPORT_ETYPE	R/W	Multiport Ethernet Type Allows a frames with a matching MPORT_ETYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register. Must be enabled using the MPORT_CTRL bit in the Multiport Control Register.	0000

Table 98: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h) (Cont.)

BIt	Name	R/W	Description	Default
47:0	MPORT_ADDR	R/W	Multiport Address Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register. Must be enabled using the MPORT_CTRL bit in the Multiport Control Register.	0000000 00000

Multiport Vector N (N = 0–5) Register (Page 04h: Address 18h)

Table 99: Multiport Vector Register Address Summary

Address	Description
18h–1Bh	Multiport Vector 0
28h–2Bh	Multiport Vector 1
38h–3Bh	Multiport Vector 2
48h–4Bh	Multiport Vector 3
58h–5Bh	Multiport Vector 4
68h–6Bh	Multiport Vector 5

Table 100: Multiport Vector Register (Page 04h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh, 58h–5Bh, 68h–6Bh)

BIt	Name	R/W	Description	Default
31:9	Reserved	R/O	–	0
8:0	MPORT_VCTR_N	R/W	Multiport Vector A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address Register will be forwarded to each port with a bit set in the Multiport Vector bit map. Bits[7:0] correspond to ports[7:0] Bit 8: Management Port (MII Management)	0

Page 05h: ARL/VTBL Access Registers

Table 101: ARL/VTBL Access Registers (Page 05h)

Address	Bits	Register Name
00h	8	"ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 176
01h–0Fh	–	Reserved
02h–07h	48	"MAC Address Index Register (Page 05h: Address 02h)" on page 176
08h–09h	16	"VLAN ID Index Register (Page 05h: Address 08h)" on page 176
0Ah–0Fh	–	Reserved
10h–17h	64	"ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177
18h–1Bh	16	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)" on page 178
1Ch–1Fh	–	Reserved
20h-27h	64	"ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177
28h-2Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)" on page 178
2Ch-2Fh	–	Reserved
30h-37h	64	"ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177
38h-3Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)" on page 178
3Ch-3Fh	–	Reserved
40h-47h	64	"ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177
48h-4Bh	32	"ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)" on page 178
4Ch-4Fh	–	Reserved
50h	8	"ARL Table Search Control Register (Page 05h: Address 50h)" on page 179
51h–52h	16	ARL Search Address
60h–77h	64	"ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)" on page 180
68h–7Bh	32	"ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)" on page 181
7Ch–7Fh	–	Reserved
80h	8	"VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)" on page 182
81h–82h	16	"VLAN Table Address Index Register (Page 05h: Address 81h)" on page 183
83h–86h	32	"VLAN Table Entry Register (Page 05h: Address 83h–86h)" on page 183
67h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

ARL Table Read/Write Control Register (Page 05h: Address 00h)

Table 102: ARL Table Read/Write Control Register (Page 05h: Address 00h)

BIt	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done command Write as 1 to initiate a read/write command to the ARL table. The bit returns to 0 to indicate that a read/write operation is complete.	0
6:1	Reserved	RO	–	–
0	ARL_R/W	R/W	ARL table read/write bit Specifies whether the ARL command is a read or write operation. 1 = Read 0 = Write	0

For more information, see "Accessing the ARL Table Entries" on page 63.

MAC Address Index Register (Page 05h: Address 02h)

Table 103: MAC Address Index Register (Page 05h: Address 02h–07h)

BIt	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC address index The ARL table read/write command uses this 48-bit address to index the ARL table. When IEEE 802.1Q is enabled, the ARL table is indexed by a combined hash of the MAC_ADDR_INDX and the VID_TBL_INDX, defined in the "VLAN ID Index Register (Page 05h: Address 08h)" on page 176. For more information, see "Accessing the ARL Table Entries" on page 63.	0

VLAN ID Index Register (Page 05h: Address 08h)

Table 104: VLAN ID Index Register (Page 05h: Address 08h–09h)

BIt	Name	R/W	Description	Default
15:12	Reserved	R/W	–	0

Table 104: VLAN ID Index Register (Page 05h: Address 08h–09h) (Cont.)

BIt	Name	R/W	Description	Default
11:0	VID_INDX	R/W	VLAN ID index When IEEE 802.1Q is enabled, the VLAN ID Index is used with the MAC_ADDR_INDX, defined in the "MAC Address Index Register (Page 05h: Address 02h)" on page 176, to form the hash index for which status is to be read or written. For more information, see "Accessing the ARL Table Entries" on page 63.	0

ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)

Table 105: ARL Table MAC/VID Entry N (N=0-3) Register Address Summary

Address	Description
10h–17h	ARL Table MAC/VID Entry 0
20h–27h	ARL Table MAC/VID Entry 1
30h–37h	ARL Table MAC/VID Entry 2
40h–47h	ARL Table MAC/VID Entry 3

Table 106: ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h)

BIt	Name	R/W	Description	Default
63:60	Reserved	R/O	–	0
59:48	VID_N	R/W	VID entry N The VID field is either read from or written to the ARL table entry N. The VID is a "don't-care" field when IEEE 802.1Q is disabled.	0
47:0	MACADDR_N	R/W	MAC address entry N The 48-bit MAC Address field to be either read from or written to the ARL table entry N.	0

Note: Together, the "ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177 and the "ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)" on page 178 compose a complete entry in the ARL table. For more information, see "Accessing the ARL Table Entries" on page 63.

ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)

Table 107: ARL Table Data Entry N (N=0-3) Register Address Summary

Address	Description
18h–1Bh	ARL Table Data Entry 0
28h–2Bh	ARL Table Data Entry 1
38h–3Bh	ARL Table Data Entry 2
48h–4Bh	ARL Table Data Entry 3

Table 108: ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh)

BIt	Name	R/W	Description	Default
31:17	Reserved	RO	–	0
16	VALID_N	R/W	Valid bit entry N Write this bit to 1 to indicate that a valid MAC address is stored in the MACADDR_N field defined in the "ARL Table MAC/VID Entry N (N=0-3) Register (Page 05h: Address 10h)" on page 177, and that the entry has not aged out. Reset when an entry is empty. This information is read from or written to the ARL table during a read/write command.	0
15	STATIC_N	RW	Static bit entry N Write this bit to 1 to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry. This information is read from or written to the ARL table during a read/write command.	0
14	AGE_N	R/W	Age bit entry N Write this bit to 1 to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects that a valid entry has remained unused for the period set by the AGE_TIME (defined in the "Aging Time Control Register (Page 02h: Address 06h)" on page 163) and the entry has not been marked as static, the entry has the valid bit cleared. The age bit is ignored if the entry has been marked as Static. This information is read from or written to the ARL table during a read/write command.	0

Table 108: ARL Table Data Entry N (N=0-3) Register (Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh)

BIt	Name	R/W	Description	Default
13:11	TC_N	R/W	TC bit for MAC-based QoS entry N These bits define the TC field for MAC-based QoS packets. This information is read from or written to the ARL table during a read/write command.	0
10:9	Reserved	R/W	–	–
8:0	FWD_PRT_MAP_N	R/W	Multicast Group Forward portmap entry N For multicast entries, these bits define the forward port map. Bit 8: CPU port/MII port Bits [7:0] correspond to ports [7:0], respectively.	0
	PORTID_N		Unicast Forward PortID entry N For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4]: Reserved Bits [3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0

ARL Table Search Control Register (Page 05h: Address 50h)

Table 109: ARL Table Search Control Register (Page 05h: Address 50h)

BIt	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done Write as 1 to initiate a sequential search of the ARL table. Each entry found by the search is returned to the "ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)" on page 181 and the "ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)" on page 180. Reading the "ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)" on page 181 allows the ARL table search to continue. BCM53118 clears this bit when the ARL table search is complete.	0
6:1	Reserved	RO	–	0
0	ARL_SR_VALID	RC	ARL search result valid Set by BCM53118 to indicate that an ARL entry is found by the ARL table search. The found entry is available in the "ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)" on page 181. This bit automatically returns to 0 after the ARL Search Result register is read.	0

For more information, see "Accessing the ARL Table Entries" on page 63.

ARL Search Address Register (Page 05h: Address 51h)

Table 110: ARL Search Address Register (Page 05h: Address 51h–52h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	ARL address valid Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry that is currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARL_ADDR	–	ARL address 14-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only.	0

ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)

Table 111: ARL Table Search MAC/VID Result N (N=0-1) Register Address Summary

Address	Description
60h–67h	ARL Table Search MAC/VID Result 0
70h–77h	ARL Table Search MAC/VID Result 1

Table 112: ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h–67h, 70h–77h)

BIt	Name	R/W	Description	Default
63:60	Reserved	RO	–	0
59:48	ARL_SR_VID_N	RO	ARL search VID result These bits store the VID of the ARL table entry found by the ARL table search function.	0
47:0	ARL_SR_MAC_N	RO	ARL search MAC address result. These bits store the MAC address of the ARL table entry found by the ARL table search function.	N/A

For more information, see "Accessing the ARL Table Entries" on page 63.

ARL Table Search Data Result N (N = 0-1) Register (Page 05h: Address 68h)

Table 113: ARL Table Search Data Result N (N=0-1) Register Address Summary

Address	Description
68h–6Bh	ARL Table Search Data Result 0
78h–7Bh	ARL Table Search Data Result 1

Table 114: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)

BIt	Name	R/W	Description	Default
31:17	Reserved	RO	–	0
16	ARL_SR_VALID_N	RO	ARL search valid bit result. This bit stores the valid bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	0
15	ARL_SR_STATIC_N	RO	ARL search static bit result. This bit stores the static bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	N/A
14	ARL_SR_AGE_N	RO	ARL search age bit result. This bit stores the Age bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
13:11	ARL_SR_TC_N	RO	ARL search TC bits result. These bits store the TC bits of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.	–
10:9	Reserved	RO	–	0

Table 114: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh) (Cont.)

BIt	Name	R/W	Description	Default
8:0	FWD_PRT_MAP_N	R/W	Multicast Group Forward portmap entry N For multicast entries, these bits define the forward port map. Bit 8: CPU port/MII port Bits [7:0] correspond to ports [7:0]	0
	PORTID_N		Unicast Forward PortID entry N For unicast entries, these bits define the port number associated with the entry of the ARL table. Bits [8:4]: Reserved Bits [3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0

For more information, see “Accessing the ARL Table Entries” on page 63.

VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

Table 115: VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

BIt	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done command Write as 1 to initiate a read or write or clear-table command to the VLAN table. The bit returns to 0 to indicate that the read or write or clear-table operation is complete.	0
6:2	Reserved	R/W	–	–
1:0	VTBL_R/W/Clr	R/W	Read/Write/Clear-table Specifies whether the current VLAN table read/write/ clear-table command is a read or write or clear-table operation. 11 = Reserved 10 = Clear-table 01 = Read 00 = Write	0

See “Programming the VLAN Table” on page 40 for more information.

VLAN Table Address Index Register (Page 05h: Address 81h)

Table 116: VLAN Table Address Index Register (Page 05h: Address 81h–82h)

BIt	**Name**	**R/W**	**Description**	**Default**
15:12	Reserved	RO	–	0
11:0	VTBL_ADDR_INDX	R/W	VLAN table address index The current VLAN table read/write uses this 12-bit address to index the VLAN table.	–

See “Programming the VLAN Table” on page 40 for more information.

VLAN Table Entry Register (Page 05h: Address 83h–86h)

Table 117: VLAN Table Entry Register (Page 05h: Address 83h–86h)

BIt	**Name**	**R/W**	**Description**	**Default**
31:22	Reserved	RO	–	0
21	FWD_MODE	R/W	This indicates whether the packet forwarding should be based on VLAN membership or based on ARL flow. 1:Based on VLAN membership (excluding Ingress port) 0: Based on ARL flow. Note that the VLAN membership based forwarding mode is only used for certain ISP Tagged packets received from ISP port when BCM53118 is operating in Double Tag Mode.	0
20:18	MSPT_INDEX	R/W	Index for 8 Spanning Trees	0
17:9	UNTAG_MAP	R/W	Untagged Port Map Bit 17: CPU Port/ MII Port Bits [16:9] correspond to ports [7:0], respectively. Ports written to 1 are designated as untagged VLAN ports. VLAN-tagged frames destined for these ports are untagged before they are forwarded. When the IEEE 802.1Q feature is enabled, frames sent via the CPU (MII port configured as a management port) are tagged. Note that the packet forwarded to IMP port should always be VLAN tagged.	–

Table 117: VLAN Table Entry Register (Page 05h: Address 83h–86h)

BIt	***Name***	***R/W***	***Description***	***Default***
8:0	FWD_MAP	R/W	Forward Port Map The VLAN-tagged Frame is allowed to be forwarded to the destination ports corresponding bits set in the Map Ports written to 1 are designated as capable of receiving VLAN-tagged frames. Bit 8: CPU Port/ MII Port Bits [7:0] correspond to Ports [7:0], respectively.	–

See “Programming the VLAN Table” on page 40 for more information.

Page 10h–17h: Internal GPHY MII Registers

Table 118: 10/100/1000 PHY Page Summary

Page	Description
10h	Port 0 Internal PHY MII Registers
11h	Port 1 Internal PHY MII Registers
12h	Port 2 Internal PHY MII Registers
13h	Port 3 Internal PHY MII Registers
14h	Port 4 Internal PHY MII Registers
15h	Port 5 Internal PHY MII Registers
16h	Port 6 Internal PHY MII Registers
17h	Port 7 Internal PHY MII Registers

Table 119: Register Map (Page 10h–17h)

SPI Offset Address	MII Address	Number of Bits	Register Table
10BASE-T/100BASE-TX/1000BASE-T Registers			
00h	00h	16	Table 120: "MII Control Register (Page 10h–17h: Address 00h–01h)," on page 187
02h	01h	16	Table 121: "MII Status Register (Page 10h–17h: Address 02h–03h)," on page 188
04h–06h	02h	32	Table 122: "PHY Identifier Register MSB (Page 10h–17h: Address 04–07h)," on page 189
08h	04h	16	Table 124: "Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h–09h)," on page 190
0Ah	05h	16	Table 125: "Auto-Negotiation Link Partner Ability Register (Page 10h–17h: Address 0Ah–0Bh)," on page 191
0Ch	06h	16	Table 125: "Auto-Negotiation Link Partner Ability Register (Page 10h–17h: Address 0Ah–0Bh)," on page 191
0Eh	07h	16	Table 127: "Next Page Transmit Register (Page 10h–17h: Address 0Eh–0Fh)," on page 193
10h	08h	16	Table 128: "Link Partner Received Next Page Register (Page 10h–17h: Address 10h–11h)," on page 194
12h	09h	16	Table 129: "1000BASE-T Control Register (Page 10h–17h: Address 12h–13h)," on page 195
14h	0Ah	16	Table 130: "1000BASE-T Status Register (Page 10h–17h: Address 14h–15h)," on page 196
16h–1Dh	–	16	Reserved (Do not read from or write to a reserved register.)
1Eh	0Fh	16	Table 131: "IEEE Extended Status Register (Page 10h–17h: Address 1Eh–1Fh)," on page 197

Table 119: Register Map (Page 10h–17h) (Cont.)

SPI Offset Address	MII Address	Number of Bits	Register Table
20h	10h	16	Table 132: "PHY Extended Control Register (Page 10h–17h: Address 20h–21h)," on page 198
22h	11h	16	Table 133: "PHY Extended Status Register (Page 10h–17h: Address 22h–23h)," on page 199
24h	12h	16	Table 134: "Receive Error Counter Register (Page 10h–17h: Address 24h–25h)," on page 200
26h	13h	16	Table 135: "False Carrier Sense Counter Register (Page 10h–17h: Address 26h–27h)," on page 200
28h	14h	16	Table 137: "Receiver NOT_OK Counter Register (Page 10h–17h: Address 28h–29h)," on page 201
2Ah–2Ch	15h–16h		Reserved (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)
2Eh	17h	16	Table 139: "Expansion Register Access Register (Page 10h–17h: Address 2Eh–2Fh)," on page 202
30h	18h	16	Table 144: "Auxiliary Control Register (Page 10h–17h: Address 30h, Shadow Value 000)," on page 204 Table 145: "10BASE-T Register (Page 10h–17h: Address 30h, Shadow Value 001)," on page 205 Table 146: "Power/MII Control Register (Page 10h–17h: Address 30h, Shadow Value 010)," on page 206 Table 147: "Miscellaneous Test Register (Page 10h–17h: Address 30h, Shadow Value 100)," on page 207 Table 148: "Miscellaneous Control Register (Page 10h–17h: Address 30h, Shadow Value 111)," on page 207
32h	19h	16	Table 149: "Auxiliary Status Summary Register (Page 10h–17h: Address 32h–33h)," on page 208
34h	1Ah	16	Table 150: "Interrupt Status Register (Page 10h–17h: Address 34h–35h)," on page 210
36h	1Bh	16	Table 151: "Interrupt Mask Register (Page 10h–17h: Address 36h)," on page 211
38h	1Ch	16	Table 153: "Spare Control 2 Register (Page 10h–17h: Address 38h, Shadow Value 00100)," on page 213 Table 153: "Spare Control 2 Register (Page 10h–17h: Address 38h, Shadow Value 00100)," on page 213 Table 154: "Auto Power-Down Register (Page 10h–17h: Address 38h, Shadow Value 01010)," on page 214 Table 156: "Mode Control Register (Page 10h–17h: Address 38h, Shadow Value 11111)," on page 216
3Ah	1Dh	16	Table 157: "Master/Slave Seed Register (Page 10h–17h: Address 3Ah–3Bh) Bit 15 = 0," on page 217 Table 158: "HCD Status Register (Page 10h–17h: Address 3Ah–3Bh) Bit 15 = 1," on page 217
3Ch	1Eh	16	Table 159: "Test Register 1 (Page 10h–17h: Address 3C–3Dh)," on page 219

Table 119: Register Map (Page 10h–17h) (Cont.)

SPI Offset Address	MII Address	Number of Bits	Register Table
3Eh	1Fh	16	Reserved (Do not read from or write to a reserved register.)
Expansion Registers: Read/Write through Register 2Ah (Accessed by Writing to Register 2Eh, Bits [11:0] = 1111 + Expansion Register Number)			
00h	–	–	Table 160: "Expansion Register 00h: Receive/Transmit Packet Counter," on page 220
01h	–	–	Table 161: "Expansion Register 01h: Expansion Interrupt Status," on page 220
04h	–	–	–
05h	–	–	–
07h	–	–	–
45h	–	–	Table 162: "Expansion Register 45h: Transmit CRC," on page 221

MII Control Register (Page 10h–17h: Address 00h–01h)

Table 120: MII Control Register (Page 10h–17h: Address 00h–01h)

Bit	Name	R/W	Description	Default
15	Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Speed Selection (LSB)	R/W	Bits [6,13]: 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps	0
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation is enabled. 0 = Auto-negotiation is disabled.	1
11	Power Down	R/W	1 = Power-down 0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from GMII. 0 = Normal operation	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-negotiation restart is complete.	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	1
7	Collision Test Enable	R/W	1 = Enable the collision test mode. 0 = Disable the collision test mode.	0
6	Speed Selection (MSB)	R/W	Works in conjunction with bit 13	1

Table 120: MII Control Register (Page 10h–17h: Address 00h–01h) (Cont.)

Bit	Name	R/W	Description	Default
5	Reserved	R/W	Write as 0, ignore on read.	0
4	Reserved	R/W	Write as 0 ignore on read	0
3	Reserved	R/W	Write as 0 ignore on read	0
2	Reserved	R/W	Write as 0 ignore on read	0
1	Reserved	R/W	Write as 0 ignore on read	0
0	Reserved	R/W	Write as 0 ignore on read	0

MII Status Register (Page 10h–17h: Address 02h)

Table 121: MII Status Register (Page 10h–17h: Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-X Full-Duplex Capable	RO H	1 = 100BASE-X full-duplex capable 0 = Not 100BASE-X full-duplex capable	1
13	100BASE-X Half-Duplex Capable	RO H	1 = 100BASE-X half-duplex capable 0 = Not 100BASE-X half-duplex capable	1
12	10BASE-T Full-Duplex Capable	RO H	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
11	10BASE-T Half-Duplex Capable	RO H	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
10	100BASE-T2 Full-Duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable 0 = Not 100BASE-T2 full-duplex capable	0
9	100BASE-T2 Half-Duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable 0 = Not 100BASE-T2 half-duplex capable	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh 0 = No extended status information in reg 0Fh	1
7	Reserved	RO	Ignore on read.	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed. 0 = Preamble always required	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation is complete. 0 = Auto-negotiation is in progress.	0
4	Remote Fault	RO LH	1 = Remote fault detected. 0 = No remote fault detected.	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0

Table 121: MII Status Register (Page 10h–17h: Address 02h–03h) (Cont.)

Bit	Name	R/W	Description	Default
1	Jabber Detect	RO LH	1 = Jabber condition detected. 0 = No jabber condition detected.	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

PHY Identifier Register (Page 10h–17h: Address 04h)

Table 122: PHY Identifier Register MSB (Page 10h–17h: Address 04–07h)

Bit	Name	R/W	Description	Default
15:0	OUI	RO	Bits 3:18 of organizationally unique identifier	0143 (hex)

Table 123: PHY Identifier Register LSB (Page 10h–17h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:10	OUI	RO	Bits 19:24 of organizationally unique identifier	101111
9:4	MODEL	RO	Device model number	111110
3:0	REVISION	RO	Device revision number	*n*[a] (hex)

a. The revision number (*n*) changes with each silicon revision.

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices developed by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], six manufacturer’s model number bits, and four revision number bits. The two
least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-0A-F7, expressed as hexadecimal values. The binary OUI is 0000-0000-0000-1010- 1111-0111. The model number for BCM53118 is 3Eh. Revision numbers start with 0h and increment by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h)

Table 124: Auto-Negotiation Advertisement Register (Page 10h–17h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next page ability is supported. 0 = Next page ability is not supported.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Remote Fault	R/W	1 = Advertise remote fault is detected. 0 = Advertise no remote fault is detected.	0
12	Reserved Technology	R/W	Write as 0, ignore on read.	0
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause 0 = Advertise no asymmetric pause	1
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation 0 = Not capable of pause operation	1
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
8	100BASE-TX Full-Duplex Capable	R/W	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	1
7	100BASE-TX Half-Duplex Capable	R/W	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1
6	10BASE-T Full-Duplex Capable	R/W	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
5	10BASE-T Half-Duplex Capable	R/W	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
4	Protocol Selector Field	R/W	Bits [4:0] = 00001 indicates IEEE 802.3 CSMA/CD	0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		1

Auto-Negotiation Link Partner Ability Register (Page 10h–17h: Address 0Ah)

Table 125: Auto-Negotiation Link Partner Ability Register (Page 10h–17h: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	0
14	Acknowledge	RO	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	0
13	Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0
12	Reserved Technology	RO	Write as 0, ignore on read.	0
11	Link Partner Asymmetric Pause	RO	1 = Link partner wants asymmetric pause. 0 = Link partner does not want asymmetric pause.	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation. 0 = Link partner is not capable of pause operation.	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0
8	100BASE-TX Full-Duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable. 0 = Link partner is not 100BASE-TX full-duplex capable.	0
7	100BASE-TX Half-Duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable. 0 = Link partner not 100BASE-TX half-duplex capable.	0
6	10BASE-T Full-Duplex Capable	RO	1 = Link partner is 10BASE-T full-duplex capable. 0 = Link partner is not 10BASE-T full-duplex capable.	0
5	10BASE-T Half-Duplex Capable	RO	1 = Link partner is 10BASE-T half-duplex capable. 0 = Link partner is not 10BASE-T half-duplex capable.	0
4	Protocol Selector Field	RO	Link partner protocol selector field	0
3		RO		0
2		RO		0
1		RO		0
0		RO		0

Note: As indicated by bit 5 of the 10BASE-T/100BASE-TX/1000BASE-T MII Status register, the values contained in the 10BASE-T/100BASE-TX/1000BASE-T Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

Next Page

BCM53118 returns a 1 in bit 15 when the link partner wants to transmit Next Page information.

Acknowledge

BCM53118 returns a 1 in bit 14 when the link partner has acknowledged reception of the link code word; otherwise, BCM53118 returns a 0.

Auto-Negotiation Expansion Register (Page 10h–17h: Address 0Ch)

Table 126: Auto-Negotiation Expansion Register (Page 10h–17h: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15	Reserved	R0	Ignore on read.	0
14	Reserved	R0	Ignore on read.	0
13	Reserved	R0	Ignore on read.	0
12	Reserved	R0	Ignore on read.	0
11	Reserved	R0	Ignore on read.	0
10	Reserved	R0	Ignore on read.	0
9	Reserved	R0	Ignore on read.	0
8	Reserved	R0	Ignore on read.	0
7	Reserved	R0	Ignore on read.	0
6	Next Page Receive Location Able	R/W	1 = Bit 5 in register 06h determines next page receive location. 0 = Bit 5 in register 06h does not determine next page receive location.	1
5	Next Page Receive Location	R/W	1 = Next pages stored in register 08h. 0 = Next pages stored in register 05h.	1
4	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
3	Link Partner Next Page Ability	RO	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	0
2	Next Page Capable	RO H	1 = BCM53118 is next page capable. 0 = BCM53118 is not next page capable.	1
1	Page Received	RO LH	1 = New page has been received from link partner. 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not have auto-negotiation.	0

Next Page Transmit Register (Page 10h–17h: Address 0Eh)

Table 127: Next Page Transmit Register (Page 10h–17h: Address 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next pages follow. 0 = Sending last next page.	0
14	Reserved	RO	Ignore on read.	0
13	Message Page	R/W	1 = Formatted page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Complies with message. 0 = Cannot comply with message. ***Note:*** Not used with 1000BASE-T next pages.	0
11	Toggle	RO	Toggles between exchanges of different next pages.	0
10	Message/Unformatted Code Field	R/W	Next page message code or unformatted data	0
9		R/W		0
8		R/W		0
7		R/W		0
6		R/W		0
5		R/W		0
4		R/W		0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		1

Link Partner Received Next Page Register (Page 10h–17h: Address 10h)

Table 128: Link Partner Received Next Page Register (Page 10h–17h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next pages follow. 0 = Sending last next page.	0
14	Acknowledge	RO	1 = Acknowledge 0 = No acknowledge	0
13	Message Page	RO	1 = Formatted page 0 = Unformatted page	0
12	Acknowledge2	RO	1 = Complies with message. 0 = Cannot comply with message. ***Note:*** Not used with 1000BASE-T next pages.	0
11	Toggle	RO	Toggles between exchanges of different next pages.	0
10	Message Code field	RO	Next page message code or unformatted data	0
9		RO		0
8		RO		0
7		RO		0
6		RO		0
5		RO		0
4		RO		0
3		RO		0
2		RO		0
1		RO		0
0		RO		0

1000BASE-T Control Register (Page 10h–17h: Address 12h)

Table 129: 1000BASE-T Control Register (Page 10h–17h: Address 12h–13h)

Bit	Name	R/W	Description	Default
15 14 13	Test Mode	R/W R/W R/W	1 X X = Test mode 4—Transmitter distortion test. 0 1 1 = Test mode 3—Slave transmit jitter test. 0 1 0 = Test mode 2—Master transmit jitter test. 0 0 1 = Test mode 1—Transmit waveform test. 0 0 0 = Normal operation	0 0 0
12	Master/Slave Configuration Enable	R/W	1 = Enable master/slave manual configuration value. 0 = Automatic master/slave configuration	0
11	Master/Slave Configuration Value	R/W	1 = Configure PHY as master. 0 = Configure PHY as slave.	1
10	Repeater/DTE	R/W	1 = Repeater/switch device port 0 = DTE device	1
9	Advertise 1000BASE-T Full-Duplex Capability	R/W	1 = Advertise 1000BASE-T full-duplex capability. 0 = Advertise no 1000BASE-T full-duplex capability.	1
8	Advertise 1000BASE-T Half-Duplex Capability	R/W	1 = Advertise 1000BASE-T half-duplex capability. 0 = Advertise no 1000BASE-T half-duplex capability.	1
7	Reserved	RO	Ignore on read.	0
6	Reserved	RO	Ignore on read.	0
5	Reserved	RO	Ignore on read.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	0
2	Reserved	RO	Ignore on read.	0
1	Reserved	RO	Ignore on read.	0
0	Reserved	RO	Ignore on read.	0

Test Mode

The BCM53118 can be placed in 1 of 4 transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written. For test modes 1, 2, and 4, the PHY must have auto-negotiation disabled and forced to 1000BASE-T mode and Auto-MDIX disabled.

- Disable auto-negotiation and force to 1000BASE-T mode (write to register 00h = 0x0040)
- Disable Auto-MDIX (write to register 18h, shadow value 111, bit 9 = 0)
- Enter test modes (write to register 09h, bits [15:13] = the desired test mode)

Master/Slave Configuration Enable

When bit 12 is set = 1, the BCM53118 master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, the master/slave mode is configured using the automatic resolution function. This bit returns a 1 when manual master/slave configuration is enabled; otherwise, it returns a 0.

1000BASE-T Status Register (Page 10h–17h: Address 14h)

Table 130: 1000BASE-T Status Register (Page 10h–17h: Address 14h–15h)

Bit	Name	R/W	Description	Default
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master. 0 = Local transmitter is slave.	0
13	Local Receiver Status	RO	1 = Local receiver is OK. 0 = Local receiver is not OK.	0
12	Remote Receiver Status	RO	1 = Remote receiver is OK. 0 = Remote receiver is not OK.	0
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable. 0 = Link partner is not 1000BASE-T full-duplex capable.	0
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable. 0 = Link partner is not 1000BASE-T half-duplex capable.	0
9	Reserved	RO	Ignore on read.	0
8	Reserved	RO	Ignore on read.	0
7	Idle Error Count	RO CR	Number of idle errors since last read	0
6		RO CR		0
5		RO CR		0
4		RO CR		0
3		RO CR		0
2		RO CR		0
1		RO CR		0
0		RO CR		0

Note: As indicated by bit 5 of the MII Status register (0h), the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

IEEE Extended Status Register (Page 10h–17h: Address 1Eh)

Table 131: IEEE Extended Status Register (Page 10h–17h: Address 1Eh–1Fh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	1000BASE-X Full-Duplex Capable	RO L	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	0
14	1000BASE-X Half-Duplex Capable	RO L	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	0
13	1000BASE-T Full-Duplex Capable	RO H	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	1
12	1000BASE-T Half-Duplex Capable	RO H	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	1
11	Reserved	RO	Ignore on read.	0
10	Reserved	RO	Ignore on read.	0
9	Reserved	RO	Ignore on read.	0
8	Reserved	RO	Ignore on read.	0
7	Reserved	RO	Ignore on read.	0
6	Reserved	RO	Ignore on read.	0
5	Reserved	RO	Ignore on read.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	0
2	Reserved	RO	Ignore on read.	0
1	Reserved	RO	Ignore on read.	0
0	Reserved	RO	Ignore on read.	0

PHY Extended Control Register (Page 10h–17h: Address 20h)

Table 132: PHY Extended Control Register (Page 10h–17h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover is disabled. 0 = Automatic MDI crossover is enabled.	0
13	Transmit Disable	R/W	1 = Transmitter outputs are disabled. 0 = Normal operation	0
12:11	Reserved	–	–	–
10	Bypass 4B/5B Encoder/Decoder (100BASE-T)	R/W	1 = Transmit and receive 5B codes over MII pins. 0 = Normal MII	0
9	Bypass Scrambler/Descrambler (100BASE-T)	R/W	1 = Scrambler and descrambler are disabled. 0 = Scrambler and descrambler are enabled.	0
8	Bypass NRZI/MLT3 Encoder/ Decoder (100BASE-T)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder. 0 = Normal operation	0
7	Bypass Receive Symbol Alignment (100BASE-T)	R/W	1 = The 5B receive symbols are not aligned. 0 = Receive symbols aligned to 5B boundaries	0
6	Reset Scrambler (100BASE-T)	R/W SC	1 = Reset scrambler to initial state. 0 = Normal scrambler operation	0
5:3	Reserved	–	–	–
2	Reserved	R/W	Write as 0, ignore on read.	0
1	Reserved	R/W	Write as 0, ignore on read.	0
0	1000 Mbps PCS Transmit FIFO Elasticity	R/W	1 = High latency 0 = Low latency	0

PHY Extended Status Register (Page 10h–17h: Address 22h)

Table 133: PHY Extended Status Register (Page 10h–17h: Address 22h–23h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Base Page Selector Field Mismatch	RO LH	1 = Link partner base page selector field mismatched advertised selector field since last read. 0 = No mismatch detected since last read.	0
14	Ethernet@WireSpeed Downgrade	RO	1 = Auto-negotiation advertised speed downgraded 0 = No advertised speed downgrade	0
13	MDI Crossover State	RO	1 = Crossover MDI mode 0 = Normal MDI mode	0
12	Interrupt Status	RO	1 = Unmasked interrupt is currently active. 0 = Interrupt is cleared.	0
11	Remote Receiver Status	RO LL	1 = Remote receiver is OK. 0 = Remote receiver is not OK since last read	0
10	Local Receiver Status	RO LL	1 = Local receiver is OK. 0 = Local receiver is not OK since last read.	0
9	Locked	RO	1 = Descrambler is locked. 0 = Descrambler is unlocked.	0
8	Link Status	RO	1 = Link pass 0 = Link fail	0
7	CRC Error Detected	RO LH	1 = CRC error detected. 0 = No CRC error since last read.	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read. 0 = No carrier extension error since last read.	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read. 0 = No bad SSD error since last read.	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read. 0 = No bad ESD error since last read.	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read. 0 = No receive error since last read.	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read. 0 = No transmit error code received since last read.	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read. 0 = No lock error since last read.	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read. 0 = No MLT3 code error since last read.	0

Receive Error Counter Register (Page 10h–17h: Address 24h)

Table 134: Receive Error Counter Register (Page 10h–17h: Address 24h–25h)[a]

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	The number of noncollision packets with receive errors since last read	0000h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, 1000BASE-T Receive Error Counter when register 38h, shadow value11011, bit 9 = 0.

Copper Receive Error Counter

When bit 9 = 0 in register 38h, shadow value 11011, this counter increments each time BCM53118 receives a 10BASE-T, 100BASE-TX, 1000BASE-T noncollision packet containing at least one receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

False Carrier Sense Counter Register (Page 10h–17h: Address 26h)

Table 135: False Carrier Sense Counter Register (Page 10h–17h: Address 26h–27h)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore on read.	00h
7:0	False Carrier Sense Counter	R/W CR	The number of false carrier sense events since last read.	00h

a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T Carrier Sense Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 0.

Copper False Carrier Sense Counter

When bit 9 = 0 in register 1Ch, shadow value 11011 and bit 14 = 0 in register 3Ch, the False Carrier Sense Counter increments each time the BCM53118 detects a 10BASE-T, 100BASE-TX, 1000BASE-T false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

10BASE-T/100BASE-TX/1000BASE-T Packets Received with Transmit Error Codes Counter

Table 136: 10BASE-T/100BASE-TX/1000BASE-T Transmit Error Code Counter Register (Address 13h)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, ignore on read.	00h
7:0	Transmit Error Code Counter	R/W CR	The number of packets received with transmit error codes since last read.	00h

a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T packets received with transmit error codes counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 1.

Packets Received with Transmit Error Codes Counter

BCM53118 detects a 10BASE-T/100BASE-TX/1000BASE-T packet with a transmit error code violation when bit 9 = 0 in register 38h, shadow value 11011, and when bit 14 = 1 in register 1Eh, Packets Received with Transmit Error Codes Counter increments each time. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Receiver NOT_OK Counter Register (Page 10h–17h: Address 28h)

Table 137: Receiver NOT_OK Counter Register (Page 10h–17h: Address 28h–29h)[a]

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	The number of times local receiver was NOT_OK since last read.	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	The number of times BCM53118 detected that the remote receiver was NOT_OK since last read.	00h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receiver NOT_OK Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 0.

Copper Local Receiver NOT_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Copper Remote Receiver NOT_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 1000BASE-T, 100BASE-TX, or 10BASE-T remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Receive CRC Counter Register (Page 10h–17h: Address 28h)

Table 138: CRC Counter Register (Page 10h–17h: Address 28h–29h)[a]

Bit	Name	R/W	Description	Default
15:0	Receive CRC Counter	R/W CR	The number of times receive CRC errors were detected.	00h

a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receive CRC Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 1.

Copper CRC Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 1 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T detects a receive CRC error. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Expansion Register Access Register (Page 10h–17h: Address 2Eh)

Table 139: Expansion Register Access Register (Page 10h–17h: Address 2Eh–2Fh)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Reserved	R/W	Write as 0, ignore on read.	0
12	Reserved	R/W	Write as 0, ignore on read.	0
11	Expansion Register Select	R/W	1111 = Expansion register is selected.	0
10		R/W	0000 = Expansion register is not selected.	0
9		R/W		0
8		R/W	All others = Reserved (Do not use)	0
7	Expansion Register Accessed	R/W	Sets the expansion register number accessed when read/write to register 2Ah.	0
6		R/W		0
5		R/W		0
4		R/W		0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		0

Expansion Register Select

Setting bits [11:8] to 1111 enables the reading from and writing to the Expansion registers in conjunction with register 2Ah. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See “Expansion Registers” on page 220 for Expansion register detail.

Expansion Register Accessed

The Expansion registers can be accessed through register 2Ah when bits [11:8] of this register are set to 1111. The available expansion registers are listed in Table 140.

Table 140: Expansion Register Select Values

Expansion Register	Register Name
00h	"Expansion Register 01h: Expansion Interrupt Status"

Auxiliary Control Shadow Value Access Register (Page 10h–17h: Address 30h)

Available 30h registers are listed in the Table 141.

Table 141: Auxiliary Control Shadow Values Access Register (Page 10h–17h: Address 30h)

Shadow Value	Register Name
000	"Auxiliary Control Shadow Values Access Register (Page 10h–17h: Address 30h)" on page 203
001	"10BASE-T Register (Page 10h–17h: Address 30h, Shadow Value 001)" on page 205
010	"Power/MII Control Register (Page 10h–17h: Address 30h, Shadow Value 010)" on page 206
100	"Miscellaneous Test Register (Page 10h–17h: Address 30h, Shadow Value 100)" on page 207
111	"Miscellaneous Control Register (Page 10h–17h: Address 30h, Shadow Value 111)" on page 207

Read from register 30h, shadow value zzz.

Table 142: Reading Register 30h

Register Reads/Writes	Description
Write register 30h, bits [2:0] = 111	This selects the miscellaneous control register, shadow value 111. All reads must be done through the miscellaneous control register.
Bit 15 = 0	This allows only bits [14:12] and bits [2:0] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11: 3] = <don't care>	When bit 15 = 0, these bits will be ignored.
Bits [2:0] = 111	This sets the shadow register select to 111 (miscellaneous control register).
Read register 30h	Data read back is the value from shadow register zzz.

Write to register 30h, shadow value yyy.

Table 143: Writing Register 30h

Register Writes	*Description*
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the values to which the desired bits are written.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

Table 144: Auxiliary Control Register (Page 10h–17h: Address 30h, Shadow Value 000)

Bit	*Name*	*R/W*	*Description*	*Default*
15	External Loopback	R/W	1 = External Loopback is enabled 0 = Normal operation	0
14	Receive Extended Packet Length	R/W	1 = Allow reception of extended length packets. 0 = Allow reception of normal length Ethernet packets only.	0
13 12	Edge Rate Control (1000BASE-T)	R/W R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	0 0
11	Reserved	R/W	Write as 0, ignore on read.	0
10	Reserved	R/W	Write as 1, ignore on read.	1
9	Reserved	R/W	Write as 0, ignore on read.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5 4	Edge Rate Control (100BASE-TX)	R/W R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	0 0
3	Reserved	R/W	Write as 0, ignore on read	0
2 1 0	Shadow Register Select	R/W R/W R/W	000 = Auxiliary control register 001 = 10BASE-T register 010 = Power/MII control register 100 = Miscellaneous test register 111 = Miscellaneous control register	0 0 0

External Loopback

When bit 15 = 1, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

Receive Extended Packet Length

When bit 14 = 1, BCM53118 can receive packets up to 9720 bytes in length when in SGMII mode.

When the bit is cleared, the BCM53118 only receives packets up to standard maximum size in length.

Edge Rate Control (1000BASE-T)

Bits [13:12] control the edge rate of the 1000BASE-T transmit DAC output waveform.

Edge Rate Control (100BASE-TX)

Bits [5:4] control the edge rate of the 100BASE-TX transmit DAC output waveform.

Shadow Register Select

See the note on "Auxiliary Control Shadow Values Access Register (Page 10h–17h: Address 30h)" on page 203 describing reading from and writing to register 18h.

The register set shown above is that for normal operation obtained when the lower 3 bits are 000.

10BASE-T Register

Table 145: 10BASE-T Register (Page 10h–17h: Address 30h, Shadow Value 001)

Bit	Name	R/W	Description	Default
15	Manchester Code Error	RO LH	1 = Manchester code error (10BASE-T) 0 = No Manchester code error	0
14	EOF Error	RO LH	1 = EOF error is detected (10BASE-T). 0 = No EOF error is detected.	0
13	Polarity Error	RO	1 = Channel polarity is inverted. 0 = Channel polarity is correct.	0
12	Block RX_DV Extension (IPG)	R/W	1 = Block RX_DV for four additional RXC cycles for IPG. 0 = Normal operation	0
11	10BASE-T TXC Invert Mode	R/W	1 = Invert TXC output. 0 = Normal operation	0
10	Reserved	R/W	Write as 0, ignore on read	0
9	Jabber Disable	R/W	1 = Jabber function is disabled. 0 = Jabber function is enabled	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	10BASE-T Echo Mode	R/W	1 = Echo transmit data to receive data 0 = Normal operation	0

Table 145: 10BASE-T Register (Page 10h–17h: Address 30h, Shadow Value 001) (Cont.)

Bit	Name	R/W	Description	Default
5	SQE Enable Mode	R/W	1 = Enable SQE. 0 = Disable SQE.	0
4	10BASE-T No Dribble	R/W	1 = Correct 10BASE-T dribble nibble. 0 = Normal operation	0
3	Reserved	R/W	Write as 0, ignore on read.	0
2 1 0	Shadow Register Select	R/W R/W R/W	000 = Auxiliary control register 001 = 10BASE-T register 010 = Power/MII control register 100 = Miscellaneous test register 111 = Miscellaneous control register	0 0 1

Power/MII Control Register (Page 10h–17h: Address 30h)

Table 146: Power/MII Control Register (Page 10h–17h: Address 30h, Shadow Value 010)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Reserved	R/W	Write as 0, ignore on read.	0
12	Reserved	R/W	Write as 0, ignore on read.	0
11	Reserved	R/W	Write as 0, ignore on read.	0
10:7	Reserved	–	–	–
6	Reserved	R/W	Write as 0, ignore on read.	1
5	Super Isolate (Copper Only)	R/W	1 = Isolate mode with no link pulses transmitted. 0 = Normal operation	1
4	Reserved	R/W	Write as 0, ignore on read.	0
3	Reserved	R/W	Write as 0, ignore on read.	0
2 1 0	Shadow Register Select	R/W R/W R/W	000 = Auxiliary control register 001 = 10BASE-T register 010 = Power/MII control register 100 = Miscellaneous test register 111 = Miscellaneous control register	0 1 0

Super Isolate (Copper Only)

Setting bit 5 = 1, places the BCM53118 into the super isolate mode.

Shadow Register Select

See the note on "Auxiliary Control Shadow Values Access Register (Page 10h–17h: Address 30h)" on page 203 describing reading from and writing to register 30h.

Miscellaneous Test Register (Page 10h–17h: Address 30h)

Table 147: Miscellaneous Test Register (Page 10h–17h: Address 30h, Shadow Value 100)

Bit	Name	R/W	Description	Default
15	Lineside [Remote] Loopback Enable	R/W	1 = Enable lineside [remote] loopback. 0 = Disable loopback.	0
14	Reserved	R/W	Write as 0, ignore on read.	0
13	Reserved	R/W	Write as 0, ignore on read.	0
12	Reserved	R/W	Write as 0, ignore on read.	0
11	Reserved	R/W	Write as 0, ignore on read.	0
10	Reserved	R/W	Write as 0, ignore on read.	0
9	Reserved	R/W	Write as 0, ignore on read.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5	Reserved	R/W	Write as 0, ignore on read.	0
4	Swap RX MDIX	R/W	1 = RX and TX operate on same pair. 0 = Normal operation	0
3	10BASE-T Halfout	R/W	1 = Transmit 10BASE-T at half amplitude. 0 = Normal operation	0
2 1 0	Shadow Register Select	R/W R/W R/W	000 = Auxiliary control register 001 = 10BASE-T register 010 = Power/MII control register 100 = Miscellaneous test register 111 = Miscellaneous control register	1 0 0

Miscellaneous Control Register (Page 10h–17h: Address 30h)

Table 148: Miscellaneous Control Register (Page 10h–17h: Address 30h, Shadow Value 111)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W SC	1 = Write bits [14:3] 0 = Only write bits [14:12]	0

Table 148: Miscellaneous Control Register (Page 10h–17h: Address 30h, Shadow Value 111) (Cont.)

Bit	Name	R/W	Description	Default
14 13 12	Shadow Register Read Selector	R/W R/W R/W	These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read. 000 = Normal operation 001 = 10BASE-T register 010 = Power control register 100 = Miscellaneous test register 111 = Miscellaneous control register	0 0 0
11	Packet Counter Mode	R/W	1 = Receive packet counter. 0 = Transmit packet counter.	0
10	Reserved	R/W	Write as 0, ignore on read.	0
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled. 0 = Auto-MDIX is disabled when auto-negotiation is disabled.	0
8	Reserved	R/W	Write as 0, ignore on read.	0
7	Reserved	R/W	Write as 0, ignore on read.	0
6	Reserved	R/W	Write as 0, ignore on read.	0
5	Reserved	R/W	Write as 0, ignore on read.	0
4	Ethernet@WireSpeed Enable	R/W	1 = Enable Ethernet@WireSpeed 0 = Disable Ethernet@WireSpeed	1
3	MDIO All PHY Select	R/W	1 = The PHY ports accepts MDIO writes to PHY address = 00000. 0 = Normal operation	0
2 1 0	Shadow Register Select	R/W R/W R/W	000 = Auxiliary control register 001 = 10BASE-T register 010 = Power/MII control register 100 = Miscellaneous test register 111 = Miscellaneous control register	1 1 1

Auxiliary Status Summary Register (Page 10h–17h: Address 32h)

Table 149: Auxiliary Status Summary Register (Page 10h–17h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	1 = Auto-negotiation is complete. 0 = Auto-negotiation is in progress.	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link is good check state. 0 = State not entered since last read.	0

Table 149: Auxiliary Status Summary Register (Page 10h–17h: Address 32h–33h) (Cont.)

Bit	Name	R/W	Description	Default
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state. 0 = State not entered since last read	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state. 0 = State not entered since last read.	0
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation next page wait state. 0 = State not entered since last read.	0
10	Auto-negotiation HCD	RO	111 = 1000BASE-T full-duplex[a] 110 = 1000BASE-T half-duplex[a] 101 = 100BASE-TX full-duplex[a] 100 = 100BASE-T4 011 = 100BASE-TX half-duplex[a] 010 = 10BASE-T full-duplex[a] 001 = 10BASE-T half-duplex[a] 000 = No highest common denominator or auto-negotiation is incomplete.	0
9	Current Operating Speed and Duplex Mode	RO		0
8		RO		0
7	Parallel Detection Fault	RO LH	1 = Parallel link fault is detected. 0 = Parallel link fault is not detected.	0
6	Remote Fault	RO	1 = Link partner has detected a remote fault. 0 = Link partner has not detected a remote fault.	0
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from the link partner. 0 = New page has not been received.	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability. 0 = Link partner does not perform auto-negotiation.	0
3	Link Partner Next Page Ability	RO	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	0
2	Link Status	RO	1 = Link is up (link pass state). 0 = Link is down (link fail state).	0
1	Pause Resolution—Receive Direction	RO	1 = Enable pause receive. 0 = Disable pause receive.	0
0	Pause Resolution—Transmit Direction	RO	1 = Enable pause transmit. 0 = Disable pause transmit.	0

a. Indicates the negotiated HCD when Auto-negotiation Enable = 1, or indicates the manually selected speed and duplex mode when Auto-negotiation Enable = 0.

Interrupt Status Register (Page 10h–17h: Address 34h)

Table 150: Interrupt Status Register (Page 10h–17h: Address 34h–35h)

Bit	Name	R/W	Description	Default
15	Energy Detect Change	RO LH	1 = Energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1). 0 = Interrupt cleared.	0
14	Illegal Pair Swap	RO LH	1 = Illegal pair swap is detected. 0 = Interrupt cleared.	0
13	MDIX Status Change	RO LH	1 = MDIX status changed since last read. 0 = Interrupt cleared.	0
12	Exceeded High Counter Threshold	RO	1 = Value in one or more counters is above 32K. 0 = All counters below are 32K.	0
11	Exceeded Low Counter Threshold	RO	1 = Value in one or more counters is above 128K. 0 = All counters below are 128K.	0
10	Auto-negotiation Page Received	RO LH	1 = Page received since last read. 0 = Interrupt cleared.	0
9	No HCD Link	RO LH	1 = Negotiated HCD, did not establish link. 0 = Interrupt cleared.	0
8	No HCD	RO LH	1 = Auto-negotiation returned HCD = none. 0 = Interrupt cleared.	0
7	Negotiated Unsupported HCD	RO LH	1 = Auto-negotiation HCD is not supported by BCM53118. 0 = Interrupt cleared.	0
6	Scrambler Synchronization Error	RO LH	1 = Scrambler synchronization error occurred since last read. 0 = Interrupt cleared.	0
5	Remote Receiver Status Change	RO LH	1 = Remote receiver status changed since last read. 0 = Interrupt cleared.	0
4	Local Receiver Status Change	RO LH	1 = Local receiver status changed since last read. 0 = Interrupt cleared.	0
3	Duplex Mode Change	RO LH	1 = Duplex mode changed since last read. 0 = Interrupt cleared.	0
2	Link Speed Change	RO LH	1 = Link speed changed since last read. 0 = Interrupt cleared.	0
1	Link Status Change	RO LH	1 = Link status changed since last read. 0 = Interrupt cleared.	0
0	Receive CRC Error	RO LH	1 = Receive CRC error occurred since last read. 0 = Interrupt cleared.	0

The $\overline{\text{INTR}}$ LED output is asserted when any bit in 10BASE-T/100BASE-TX/1000BASE-T interrupt status register is set and the corresponding bit in the 10BASE-T/100BASE-TX/1000BASE-T interrupt mask register is cleared.

Interrupt Mask Register (Page 10h–17h: Address 36h)

Table 151: Interrupt Mask Register (Page 10h–17h: Address 36h)

Bit	Name	R/W	Description	Default
15	Signal Detect/Energy Detect Change (enabled by register 1Ch, shadow 05h, bit 5 = 1)	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
14	Illegal Pair Swap	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
13	MDIX Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
12	Exceeded High Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
11	MDIX Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
10	Exceeded High Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
9	HCD No Link	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
8	No HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
7	Negotiated Unsupported HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
6	Scrambler Synchronization Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
5	Remote Receiver Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
4	Local Receive Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Table 151: Interrupt Mask Register (Page 10h–17h: Address 36h) (Cont.)

Bit	Name	R/W	Description	Default
3	Duplex Mode Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
2	Link Speed Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
1	Link Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
0	CRC Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Interrupt Mask Vector

When bit n of the Interrupt Mask register is written to 1, the interrupt corresponding to the same bit in the Interrupt Status register is masked. The status bits still operate normally when the interrupt is masked, but do not generate an interrupt output. When this bit is written to 0, the interrupt is unmasked.

10BASE-T/100BASE-TX/1000BASE-T Register 38h Access

Reading from and writing to 10BASE-T/100BASE-TX/1000BASE-T register 38h is though register 38h bits [15:10]. The bits [14:10] set the shadow value of register 38h, and bit 15 enables the writing of the bits [9:0]. Setting bit 15 allows writing to bits [9:0] of register 38h. Before reading register 38h shadow zzzzz, writes to register 38h should be set with bit 15 = 0, and bits [14:10] to zzzzz. The subsequent register read from register 38h contains the shadow zzzzz register value. Table 152 lists all the register 38h shadow values.

Table 152: 10BASE-T/100BASE-TX/1000BASE-T Register 38h Shadow Values

Shadow Value	Register Name
00100	"Spare Control 2 Register (Page 10h–17h: Address 38h, Shadow Value 00100)" on page 213
00101	–
01000	–
01001	–
01010	"Auto Power-Down Register (Page 10h–17h: Address 38h, Shadow Value 01010)" on page 214
01101	–
01110	"LED Selector 2 Register (Page 10h–17h: Address 38h, Shadow Value 01110)" on page 215
11111	"Mode Control Register (Page 10h–17h: Address 38h, Shadow Value 11111)" on page 216

Spare Control 2 Register (Page 10h–17h: Address 38h)

Table 153: Spare Control 2 Register (Page 10h–17h: Address 38h, Shadow Value 00100)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14	Shadow Register Selector	R/W	00100 = Spare control 2 register	0
13		R/W		0
12		R/W		1
11		R/W		0
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	–	–	–
7	Reserved	R/W	Write as 0, ignore when read.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Reserved	R/W	Write as 0, ignore when read.	0
4 3 2	Ethernet@WireSpeed Retry Limit	RO	000 = Downgrade after 2 failed auto-negotiation attempts. 001 = Downgrade after 3 failed auto-negotiation attempts. 010 = Downgrade after 4 failed auto-negotiation attempts. 011 = Downgrade after 5 failed auto-negotiation attempts. 100 = Downgrade after 6 failed auto-negotiation attempts. 101 = Downgrade after 7 failed auto-negotiation attempts. 110 = Downgrade after 8 failed auto-negotiation attempts. 111 = Downgrade after 9 failed auto-negotiation attempts.	0 1 1
1	Energy Detect on $\overline{INTR}$ LED Pin	R/W	1 = Routes energy detect to interrupt signal. Use LED selectors (register 38h shadow 01101 and 01110) and program to $\overline{INTR}$ mode. 0 = $\overline{INTR}$ LED pin performs the Interrupt function.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Auto Power-Down Register (Page 10h–17h: Address 38h)

Table 154: Auto Power-Down Register (Page 10h–17h: Address 38h, Shadow Value 01010)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14	Shadow Register Selector	R/W	01010 = Auto power-down register	0
13		R/W		1
12		R/W		0
11		R/W		1
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	R/W	Write as 0, ignore when read.	0
7	Reserved	R/W	Write as 0, ignore when read.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Auto Power-Down Mode	R/W	1 = Auto power-down mode is enabled. 0 = Auto power-down mode is disabled.	0
4	Sleep Timer Select	R/W	1 = Sleep timer is 5.4 seconds. 0 = Sleep timer is 2.7 seconds.	0
3	Wake-up Timer Select	R/W	Counter for wake-up timer in units of 84 ms	0
2		R/W	0001 = 84 ms	0
1		R/W	0010 = 168 ms	0
0		R/W	... 1111 = 1.26 sec.	1

LED Selector 2 Register (Page 10h–17h: Address 38h)

Table 155: LED Selector 2 Register (Page 10h–17h: Address 38h, Shadow Value 01110)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14	Shadow Register Selector	R/W	01110 = LED status register	0
13		R/W		1
12		R/W		1
11		R/W		1
10		R/W		0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	R/W	Write as 0, ignore when read.	0
7	LED4 Selector	R/W	0000 = LINKSPD[1] 0001 = LINKSPD[2] 0010 = XMITLED 0011 = ACTIVITY 0100 = FDXLED 0101 = SLAVE 0110 = INTR 0111 = QUALITY 1000 = RCVLED 1001 = WIRESPD_DOWNGRADE 1010 = MULTICOLOR[2] 1011 = CABLE DIAGNOSTIC OPEN/SHORT 1100 = RESERVED 1101 = CRS (SGMII mode) 1110 = Off (high) 1111 = On (low)	0
6		R/W		1
5		R/W		1
4		R/W		0
3	LED3 Selector	R/W	0000 = LINKSPD[1] 0001 = LINKSPD[2] 0010 = XMITLED 0011 = ACTIVITY 0100 = FDXLED 0101 = SLAVE 0110 = INTR 0111 = QUALITY 1000 = RCVLED 1001 = WIRESPD_DOWNGRADE 1010 = MULTICOLOR[1] 1011 = CABLE DIAGNOSTIC OPEN/SHORT 1100 = RESERVED 1101 = CRS (SGMII mode) 1110 = Off (high) 1111 = On (low)	0
2		R/W		0
1		R/W		1
0		R/W		1

Mode Control Register (Page 10h–17h: Address 38h)

Table 156: Mode Control Register (Page 10h–17h: Address 38h, Shadow Value 11111)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14	Shadow Register Selector	R/W	11111 = LED status register	1
13		R/W		1
12		R/W		1
11		R/W		1
10		R/W		1
9	Reserved	RO	Ignore on read.	0
8	Reserved	–	–	–
7	Copper Link	RO	1 = Link is good on the copper interface. 0 = Copper link is down.	0
6	Reserved	–	–	–
5	Copper Energy Detect	RO	1 = Energy detected on the copper interface. 0 = Energy not detected on the copper interface.	0
4	Reserved	RO	Ignore on read.	0
3	Reserved	RO	Ignore on read.	1
2	Mode Select	R/W	00 = GMII 01 = Reserved 10 = Reserved 11 = Reserved	0
1				0
0	Reserved	–	–	–

Master/Slave Seed Register (Page 10h–17h: Address 3Ah)

Table 157: Master/Slave Seed Register (Page 10h–17h: Address 3Ah–3Bh) Bit 15 = 0

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select shadow register. 0 = Normal operation Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match. 0 = Seeds do not match.	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device. 0 = Link partner is a DTE device.	0
12	Link Partner Manual Master/ Slave Configuration Value	RO	1 = Link partner is configured as master. 0 = Link partner is configured as slave.	0
11	Link Partner Manual Master/ Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration is enabled. 0 = Link partner manual master/slave configuration is disabled.	0
10	Local Master/Slave Seed Value	R/W	Returns the automatically generated master/slave random seed.	0
9		R/W		0
8		R/W		0
7		R/W		0
6		R/W		0
5		R/W		0
4		R/W		0
3		R/W		0
2		R/W		0
1		R/W		0
0		R/W		0

HCD Status Register (Page 10h–17h: Address 3Ah)

Table 158: HCD Status Register (Page 10h–17h: Address 3Ah–3Bh) Bit 15 = 1

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select Shadow register. 0 = Normal operation	0
14	Ethernet@WireSpeed Disable Gigabit Advertising	RO	1 = Disable advertising gigabit. 0 = Advertise gigabit based on register 09h.	0

Table 158: HCD Status Register (Page 10h–17h: Address 3Ah–3Bh) Bit 15 = 1 (Cont.)

Bit	*Name*	*R/W*	*Description*	*Default*
13	Ethernet@WireSpeed Disable 100TX Advertising	RO	1 = Disable advertising 100TX. 0 = Advertise 100TX based on register 04h.	0
12	Ethernet@WireSpeed Downgrade	RO LH	1 = Ethernet@WireSpeed downgrade occurred since last read. 0 = Ethernet@WireSpeed downgrade cleared.	0
11	HCD 1000BASE-T Full-Duplex	RO LH	1 = Gigabit full-duplex occurred since last read. 0 = HCD cleared.	0
10	HCD 1000BASE-T Half-Duplex	RO LH	1 = Gigabit half-duplex occurred since last read. 0 = HCD cleared.	0
9	HCD 100BASE-TX Full-Duplex	RO LH	1 = 100BASE-TX full-duplex occurred since last read. 0 = HCD cleared.	0
8	HCD 100BASE-T Half-Duplex	RO LH	1 = 100BASE-TX half-duplex occurred since last read. 0 = HCD cleared.	0
7	HCD 10BASE-T Full-Duplex	RO LH	1 = 10BASE-T full-duplex occurred since last read 0 = HCD cleared.	0
6	HCD 10BASE-T Half-Duplex	RO LH	1 = 10BASE-T half-duplex occurred since last read. 0 = HCD cleared.	0
5	HCD 1000BASE-T Full-Duplex (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0
4	HCD 1000BASE-T Half-Duplex (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0
3	HCD 100BASE-TX Full-Duplex (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0
2	HCD 100BASE-T Half-Duplex (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0
1	HCD 10BASE-T Full-Duplex (Link Never Came Up)	RO LH	1 = 10BASE-T full-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0
0	HCD 10BASE-T Half-Duplex (Link Never Came Up)	RO LH	1 = 10BASE-T half-duplex HCD and *link never came up* occurred since the last read. 0 = HCD cleared.	0

Note: Bits [12:0] are also cleared when auto-negotiation is disabled via MII register 00h, bit 12 = 1, or restarted via MII register 00h, bit 9 = 1.

Test Register 1 (Page 10h–17h: Address 3Ch)

Table 159: Test Register 1 (Page 10h–17h: Address 3C–3Dh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	1 = Receiver NOT_OK counters (register 14h) becomes 16 bit CRC error counter (CRC errors are counted only after this bit is set). 0 = Normal operation	0
14	Transmit Error Code Visibility	R/W	1 = False carrier sense counters (register 13h) counts packets received with transmit error codes. 0 = Normal operation	0
13	Reserved	R/W	Write as 0, ignore when read.	0
12	Force Link 10/100/1000BASE-T	R/W	1 = Force link state machine into link pass state. 0 = Normal operation	0
11	Reserved	R/W	Write as 0, ignore when read.	0
10	Reserved	R/W	Write as 0, ignore when read.	0
9	Reserved	R/W	Write as 0, ignore when read.	0
8	Reserved	R/W	Write as 0, ignore when read.	0
7	Manual Swap MDI State	R/W	1 = Manually swap MDI state. 0 = Normal operation ***Note:*** To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a nonlink condition, then set bit 7 = 1 and finally set the PHY into force 100BASE-TX mode.	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Reserved	R/W	Write as 0, ignore when read.	0
4	Reserved	R/W	Write as 0, ignore when read.	0
3	Reserved	R/W	Write as 0, ignore when read.	0
2	Reserved	R/W	Write as 0, ignore when read.	0
1	Reserved	R/W	Write as 0, ignore when read.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Note: Preamble is still required on the first read or write. Preamble suppression cannot be disabled.

Expansion Registers

Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to "Expansion Register Access Register (Page 10h–17h: Address 2Eh–2Fh)" bits [11:0] = 'F00'h, and read/write access is through register 2Ah.

Table 160: Expansion Register 00h: Receive/Transmit Packet Counter

Bit	Name	R/W	Description	Default
15:0	Packet Counter (Copper Only)	R/W CR	Returns the transmitted and received packet count.	0000h

Packet Counter (Copper Only)

The mode of this counter is set by bit 11 of "Miscellaneous Control Register (Page 10h–17h: Address 30h, Shadow Value 111)". When bit 11 =1, then receive packets (both good and bad CRC error packets) are counted. When bit 11 = 0, then transmit packets (both good and bad CRC error packets) are counted. This counter is cleared on read and freezes at FFFFh.

Expansion Register 01h: Expansion Interrupt Status

Expansion register 00h is enabled by writing to "Expansion Register Access Register (Page 10h–17h: Address 2Eh–2Fh)" bits [11:0] = 'F01'h, and read/write access is through register 2Ah.

Table 161: Expansion Register 01h: Expansion Interrupt Status

Bit	Name	R/W	Description	Default
15:1	Reserved	RO	Write as 0, ignore on read	0
0	Transmit CRC Error	RO LH	1 = Transmit CRC error detected since last read. 0 = No transmit CRC error detected.	0

Transmit CRC Error

This bit indicates that a transmit CRC error has been detected since the last read.

Expansion Register 45h: Transmit CRC Enable

Expansion register 00h is enabled by writing to "Expansion Register Access Register (Page 10h–17h: Address 2Eh–2Fh)" bits [11:0] = 'F45'h, and read/write access is through register 2Ah.

Table 162: Expansion Register 45h: Transmit CRC

Bit	*Name*	*R/W*	*Description*	*Default*
15:13	Reserved	R/W	Write as 0, ignore on read.	000
12	Transmit CRC enable	R/W	1 = Enable transmit CRC checker. 0 = Disable transmit CRC checker. Register 18h, shadow value 100, bit 15 must be set to a 1.	0
11:0	Reserved	R/W	Write as 0, ignore on read.	0

Transmit CRC Checker

When register 30h, Shadow Value 100, bit 15 = 1 and Expansion Register 45h, bit 12 = 1, the transmit CRC checker is enabled. When a transmit CRC error occurs, Expansion Register 01h, bit 0 = 1.

Page 20h–28h: Port MIB Registers

Table 163: Port MIB Registers Page Summary

Page	*Description*
20h	Port 0
21h	Port 1
22h	Port 2
23h	Port 3
24h	Port 4
25h	Port 5
26h	Port 6
27h	Port 7
28h	IMP port

Table 164: Page 20h–28h Port MIB Registers

ADDR	*Bits*	*Name*	*Description*
00h–07h	64	TxOctets	The total number of good bytes of data transmitted by a port (excluding preamble, but including FCS).
08h–0Bh	32	TxDropPkts	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.

Table 164: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
0Ch–0Fh	32	TxQ0PKT	The total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.
10h–13h	32	TxBroadcastPkts	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
14h–17h	32	TxMulticastPkts	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
18h–1Bh	32	TxUnicastPkts	The number of good packets transmitted by a port that are addressed to a unicast address.
1Ch–1Fh	32	TxCollisions	The number of collisions experienced by a port during packet transmissions.
20h–23h	32	TxSingleCollision	The number of packets successfully transmitted by a port that experienced exactly one collision.
24h–27h	32	TxMultiple Collision	The number of packets successfully transmitted by a port that experienced more than one collision.
28h–2Bh	32	TxDeferredTransmit	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.
2Ch–2Fh	32	TxLateCollision	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
34h–37h	32	TxFrameInDisc	The number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers [Page 0Ah].) This attribute only increments if a network device is not acting in compliance with a flow-control request, or the BCM53118 internal flow control/buffering scheme has been misconfigured.
38h–3Bh	32	TxPausePkts	The number of PAUSE events on a given port.
3Ch–3Fh	32	TxQ1PKT	The total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.
40h–43h	32	TxQ2PKT	The total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.
44h–47h	32	TxQ3PKT	The total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.
48h–4Bh	32	TxQ4PKT	The total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.
4Ch–4Fh	32	TxQ5PKT	The total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.

Table 164: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
50h–57h	64	RxOctets	The number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.
58h–5Bh	32	RxUndersizePkts	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).
5Ch–5Fh	32	RxPausePkts	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (88–08h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00–01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.
60h–63h	32	Pkts64Octets	The number of packets (including error packets) that are 64 bytes long.
64h–67h	32	Pkts65to127Octets	The number of packets (including error packets) that are between 65 and 127 bytes long.
68h–6Bh	32	Pkts128to255Octets	The number of packets (including error packets) that are between 128 and 255 bytes long.
6Ch–6Fh	32	Pkts256to511Octets	The number of packets (including error packets) that are between 256 and 511 bytes long.
70h–73h	32	Pkts512to1023Octets	The number of packets (including error packets) that are between 512 and 1023 bytes long.
74h–77h	32	Pkts1024toMaxPktOctets	The number of packets (including error packets) that are between 1024 and MaxPacket bytes long.
78h–7Bh	32	RxOversizePkts	The number of good packets received by a port that are greater than standard max frame size.
7Ch–7Fh	32	RxJabbers	The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.
80h–83h	32	RxAlignmentErrors	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.
84h–87h	32	RxFCSErrors	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.
88h–8Fh	64	RxGoodOctets	The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).

Table 164: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
90h–93h	32	RxDropPkts	The number of good packets received by a port that were dropped due to lack of resources (e.g., lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.
94h–97h	32	RxUnicastPkts	The number of good packets received by a port that are addressed to a unicast address.
98h–9Bh	32	RxMulticastPkts	The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
9Ch–9Fh	32	RxBroadcastPkts	The number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
A0h–A3h	32	RxSAChanges	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.
A4h–A7h	32	RxFragments	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
A8h–ABh	32	JumboPkt	The number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors. ***Note:*** InFrame count should count "the JumboPkt count with good CRC."
ACh–AFh	32	RXSymbolError	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increments once per carrier event and does not increment on detection of collision during the carrier event.
B0h–B3h	32	InRangeErrors	The number of frames received with good CRC and the following conditions. The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received, OR The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).
B4h–B7h	32	OutOfRangeErrors	The number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536.
C0h–C3h	32	RxDiscard	The number of good packets received by a port that were discarded by the Forwarding Process.
F0h–F7h	64	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7	–

Table 164: Page 20h–28h Port MIB Registers (Cont.)

ADDR	Bits	Name	Description
F8h–FDh	–	Reserved	–
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276	–
FFh	8	"Page Register (Global, Address FFh)" on page 277	–

Page 30h: QoS Registers

Table 165: Page 30h QoS Registers

Address	Bits	Description
00h	8	"QoS Global Control Register (Page 30h: Address 00h)" on page 226
01h–02h	16	Reserved
03h	–	Reserved
04h–05h	16	"QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)" on page 227
06h–07h	16	"QoS DiffServ Enable Register (Page 30h: Address 06h)" on page 227
08h–0Fh	–	Reserved
10h–33h	32/port	"Port N (N = 0-7, 8) PCP_To_TC Register (Page 30h: Address 10h)" on page 228
34h–3Fh	–	Reserved
40h–45h	48	"DiffServ Priority Map 0 Register (Page 30h: Address 40h)" on page 229
46h–4Bh	48	"DiffServ Priority Map 1 Register (Page 30h: Address 46h)" on page 229
4Ch–51h	48	"DiffServ Priority Map 2 Register (Page 30h: Address 4Ch)" on page 230
52h–57h	48	"DiffServ Priority Map 3 Register (Page 30h: Address 52h)" on page 231
48h–61h	–	Reserved
62h–63h	16	"TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231
64h–67h	32	"CPU_To_COS Map Register (Page 30h: Address 64h–67h)" on page 232
68h–7Fh	–	Reserved
80h	8	"TX Queue Control Register (Page 30h: Address 80h)" on page 233
81h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 233, Queue 0
82h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 233, Queue 1
83h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 233, Queue 2

Table 165: Page 30h QoS Registers (Cont.)

Address	Bits	Description
84h	8	"TX Queue Weight Register (Page 30h: Address 81h)" on page 233, Queue 3
85h–86h	16	"COS4 Service Weight Register (Page 30h: Address 85h–86h)" on page 234
875h–9Fh	–	Reserved
A0h	–	Reserved
A1h	–	Reserved
A2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

QoS Global Control Register (Page 30h: Address 00h)

Table 166: QoS Global Control Register (Page 30h: Address 00h)

Bit	Name	R/W	Description	Default
7	Aggregation Mode	R/W	When enable this bit, the IMP operated as the uplink port to the upstream network processor and the COS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operated as the interface to the management CPU, and the COS is decided based on the reasons for forwarding the packet to the CPU.	0
6	PORT_QOS_EN	R/W	Port-based QoS enable When port-based QoS is enabled, ingress frames are assigned a priority ID value based on the PORT_QOS_PRI bits in the "Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244. IEEE 802.1p and DiffServ priorities are disregarded. 0 = Disable port-based QoS. 1 = Enable port-based QoS. See "Quality of Service" on page 34 for more information.	0
5:4	Reserved	R/W	–	0
3:2	QOS_LAYER_SEL	R/W	QoS priority selection These bits determine which QoS priority scheme is associated with the frame. See Table 1 on page 36 for more information.	0
1:0	Reserved	R/W	Reserved	0

QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)

Table 167: QoS.1P Enable Register (Page 30h: Address 04h–05h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	802_1P_EN	R/W	QoS IEEE 802.1p port mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Disable IEEE 802.1p priority for individual ports. 1 = Enable IEEE 802.1p priority for individual ports. See "IEEE 802.1Q VLAN" on page 39 for more information.	0

QoS DiffServ Enable Register (Page 30h: Address 06h)

Table 168: QoS DiffServ Enable Register (Page 30h: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	0
8:0	DIFFSERV_EN	R/W	DiffServ port mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Disable DiffServ priority for individual ports. 1 = Enable DiffServ priority for individual ports.	0

See "Quality of Service" on page 34 for more information.

Port N (N = 0-7, 8) PCP_To_TC Register (Page 30h: Address 10h)

Table 169: Port N (N=0-7,8) PCP_To_TC Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	Port 6
2Ch–2Fh	Port 7
30h–33h	IMP Port

These bits map the IEEE 802.1p priority level to one of the eight priority ID levels in the "TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231.

Table 170: Port N (N=0-7,8) PCP_To_TC Register (Page 30h: Address 10h–33h)

BIt	Name	R/W	Description	Default
31:24	Reserved	RO	–	0
23:21	1P_111_MAP	R/W	IEEE 802.1p priority tag field 111	111
20:18	1P_110_MAP	R/W	IEEE 802.1p priority tag field 110	110
17:15	1P_101_MAP	R/W	IEEE 802.1p priority tag field 101	101
14:12	1P_100_MAP	R/W	IEEE 802.1p priority tag field 100	100
11:9	1P_011_MAP	R/W	IEEE 802.1p priority tag field 011	011
8:6	1P_010_MAP	R/W	IEEE 802.1p priority tag field 010	010
5:3	1P_001_MAP	R/W	IEEE 802.1p priority tag field 001	001
2:0	1P_000_MAP	R/W	IEEE 802.1p priority tag field 000	000

See "Quality of Service" on page 34 for more information.

DiffServ Priority Map 0 Register (Page 30h: Address 40h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231.

Table 171: DiffServ Priority Map 0 Register (Page 30h: Address 40h–45h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 001111_MAP	R/W	DiffServ DSCP priority tag field 001111	0
44:42	DIFFSERV_ 001110_MAP	R/W	DiffServ DSCP priority tag field 001110	0
41:39	DIFFSERV_ 001101_MAP	R/W	DiffServ DSCP priority tag field 001101	0
38:36	DIFFSERV_ 001100_MAP	R/W	DiffServ DSCP priority tag field 001100	0
35:33	DIFFSERV_ 001011_MAP	R/W	DiffServ DSCP priority tag field 001011	0
32:30	DIFFSERV_ 001010_MAP	R/W	DiffServ DSCP priority tag field 001010	0
29:27	DIFFSERV_ 001001_MAP	R/W	DiffServ DSCP priority tag field 001001	0
26:24	DIFFSERV_ 001000_MAP	R/W	DiffServ DSCP priority tag field 001000	0
23:21	DIFFSERV_ 000111_MAP	R/W	DiffServ DSCP priority tag field 000111	0
20:18	DIFFSERV_ 000110_MAP	R/W	DiffServ DSCP priority tag field 000110	0
17:15	DIFFSERV_ 000101_MAP	R/W	DiffServ DSCP priority tag field 000101	0
14:12	DIFFSERV_ 000100_MAP	R/W	DiffServ DSCP priority tag field 000100	0
11:9	DIFFSERV_ 000011_MAP	R/W	DiffServ DSCP priority tag field 000011	0
8:6	DIFFSERV_ 000010_MAP	R/W	DiffServ DSCP priority tag field 000010	0
5:3	DIFFSERV_ 000001_MAP	R/W	DiffServ DSCP priority tag field 000001	0
2:0	DIFFSERV_ 000000_MAP	R/W	DiffServ DSCP priority tag field 000000	0

See "Quality of Service" on page 34 for more information.

DiffServ Priority Map 1 Register (Page 30h: Address 46h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231.

Table 172: DiffServ Priority Map 1 Register (Page 30h: Address 46h–4Bh)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 011111_MAP	R/W	DiffServ DSCP priority tag field 011111	0
44:42	DIFFSERV_ 011110_MAP	R/W	DiffServ DSCP priority tag field 011110	0
41:39	DIFFSERV_ 011101_MAP	R/W	DiffServ DSCP priority tag field 011101	0
38:36	DIFFSERV_ 011100_MAP	R/W	DiffServ DSCP priority tag field 011100	0
35:33	DIFFSERV_ 011011_MAP	R/W	DiffServ DSCP priority tag field 011011	0
32:30	DIFFSERV_ 011010_MAP	R/W	DiffServ DSCP priority tag field 011010	0
29:27	DIFFSERV_ 011001_MAP	R/W	DiffServ DSCP priority tag field 011001	0

Table 172: DiffServ Priority Map 1 Register (Page 30h: Address 46h–4Bh) (Cont.)

Bit	Name	R/W	Description	Default
26:24	DIFFSERV_ 011000_MAP	R/W	DiffServ DSCP priority tag field 011000	0
23:21	DIFFSERV_ 010111_MAP	R/W	DiffServ DSCP priority tag field 010111	0
20:18	DIFFSERV_ 010110_MAP	R/W	DiffServ DSCP priority tag field 010110	0
17:15	DIFFSERV_ 010101_MAP	R/W	DiffServ DSCP priority tag field 010101	0
14:12	DIFFSERV_ 010100_MAP	R/W	DiffServ DSCP priority tag field 010100	0
11:9	DIFFSERV_ 010011_MAP	R/W	DiffServ DSCP priority tag field 010011	0
8:6	DIFFSERV_ 010010_MAP	R/W	DiffServ DSCP priority tag field 010010	0
5:3	DIFFSERV_ 010001_MAP	R/W	DiffServ DSCP priority tag field 010001	0
2:0	DIFFSERV_ 010000_MAP	R/W	DiffServ DSCP priority tag field 010000	0

See “Quality of Service” on page 34 for more information.

DiffServ Priority Map 2 Register (Page 30h: Address 4Ch)

These bits map the DiffServ priority level to one of the eight priority ID levels in the “TC_To_COS Mapping Register (Page 30h: Address 62h–63h)” on page 231.

Table 173: DiffServ Priority Map 2 Register (Page 30h: Address 4Ch–51h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 101111_MAP	R/W	DiffServ DSCP priority tag field 101111	0
44:42	DIFFSERV_ 101110_MAP	R/W	DiffServ DSCP priority tag field 101110	0
41:39	DIFFSERV_ 101101_MAP	R/W	DiffServ DSCP priority tag field 101101	0
38:36	DIFFSERV_ 101100_MAP	R/W	DiffServ DSCP priority tag field 101100	0
35:33	DIFFSERV_ 101011_MAP	R/W	DiffServ DSCP priority tag field 101011	0
32:30	DIFFSERV_ 101010_MAP	R/W	DiffServ DSCP priority tag field 101010	0
29:27	DIFFSERV_ 101001_MAP	R/W	DiffServ DSCP priority tag field 101001	0
26:24	DIFFSERV_ 101000_MAP	R/W	DiffServ DSCP priority tag field 101000	0
23:21	DIFFSERV_ 100111_MAP	R/W	DiffServ DSCP priority tag field 100111	0
20:18	DIFFSERV_ 100110_MAP	R/W	DiffServ DSCP priority tag field 100110	0
17:15	DIFFSERV_ 100101_MAP	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DIFFSERV_ 100100_MAP	R/W	DiffServ DSCP priority tag field 100100	0
11:9	DIFFSERV_ 100011_MAP	R/W	DiffServ DSCP priority tag field 100011	0
8:6	DIFFSERV_ 100010_MAP	R/W	DiffServ DSCP priority tag field 100010	0
5:3	DIFFSERV_ 100001_MAP	R/W	DiffServ DSCP priority tag field 100001	0
2:0	DIFFSERV_ 100000_MAP	R/W	DiffServ DSCP priority tag field 100000	0

See “Quality of Service” on page 34 for more information.

DiffServ Priority Map 3 Register (Page 30h: Address 52h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231.

Table 174: DiffServ Priority Map 3 Register (Page 30h: Address 52h–57h)

Bit	Name	R/W	Description	Default
47:45	DIFFSERV_ 111111_MAP	R/W	DiffServ DSCP priority tag field 111111	0
44:42	DIFFSERV_ 111110_MAP	R/W	DiffServ DSCP priority tag field 111110	0
41:39	DIFFSERV_ 111101_MAP	R/W	DiffServ DSCP priority tag field 111101	0
38:36	DIFFSERV_ 111100_MAP	R/W	DiffServ DSCP priority tag field 111100	0
35:33	DIFFSERV_ 111011_MAP	R/W	DiffServ DSCP priority tag field 111011	0
32:30	DIFFSERV_ 111010_MAP	R/W	DiffServ DSCP priority tag field 111010	0
29:27	DIFFSERV_ 111001_MAP	R/W	DiffServ DSCP priority tag field 111001	0
26:24	DIFFSERV_ 111000_MAP	R/W	DiffServ DSCP priority tag field 111000	0
23:21	DIFFSERV_ 110111_MAP	R/W	DiffServ DSCP priority tag field 110111	0
20:18	DIFFSERV_ 110110_MAP	R/W	DiffServ DSCP priority tag field 110110	0
17:15	DIFFSERV_ 100101_MAP	R/W	DiffServ DSCP priority tag field 100101	0
14:12	DIFFSERV_ 110100_MAP	R/W	DiffServ DSCP priority tag field 110100	0
11:9	DIFFSERV_ 110011_MAP	R/W	DiffServ DSCP priority tag field 110011	0
8:6	DIFFSERV_ 110010_MAP	R/W	DiffServ DSCP priority tag field 110010	0
5:3	DIFFSERV_ 110001_MAP	R/W	DiffServ DSCP priority tag field 110001	0
2:0	DIFFSERV_ 110000_MAP	R/W	DiffServ DSCP priority tag field 110000	0

See "Quality of Service" on page 34 for more information.

TC_To_COS Mapping Register (Page 30h: Address 62h–63h)

All the bits in Table 175 map the priority ID to one of the TX queues.

Table 175: TC_To_COS Mapping Register (Page 30h: Address 62h–63h)

Bit	Name	R/W	Description	Default
15:14	PRI_111_QID	R/W	Priority ID 111 mapped to TX Queue ID	00
13:12	PRI_110_QID	R/W	Priority ID 110 mapped to TX Queue ID	00
11:10	PRI_101_QID	R/W	Priority ID 101 mapped to TX Queue ID	00
9:8	PRI_100_QID	R/W	Priority ID 100 mapped to TX Queue ID	00
7:6	PRI_011_QID	R/W	Priority ID 011 mapped to TX Queue ID	00
5:4	PRI_010_QID	R/W	Priority ID 010 mapped to TX Queue ID	00
3:2	PRI_001_QID	R/W	Priority ID 001 mapped to TX Queue ID	00
1:0	PRI_000_QID	R/W	Priority ID 000 mapped to TX Queue ID	00

See "Quality of Service" on page 34 for more information.

CPU_To_COS Map Register (Page 30h: Address 64h–67h)

Table 176: CPU_To_COS Map Register (Page 30h: Address 64h–67h)

BIt	Name	R/W	Description	Default
31:18	Reserved	RO	–	0
17:15	Exception/Flooding Processing to CPU COS Map	R/W	The packet forwarded to the CPU for Exception Processing/Flooding reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0
14:12	Protocol Snooping to CPU COS Map	R/W	The packet forwarded to the CPU for Protocol Snooping reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0
11:9	Protocol Termination to CPU COS Map	R/W	The packet forwarded to the CPU for Protocol Termination reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0
8:6	Switching to CPU COS Map	R/W	The packet forwarded to the CPU for Switching reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0
5:3	SA Learning to CPU COS Map	R/W	The packet forwarded to the CPU for SA Learning reason. The COS selection is based on the highest COS among all the reasons for the packet.	0
2:0	Mirror to CPU COS Map	R/W	The packet forwarded to the CPU for mirroring reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0

TX Queue Control Register (Page 30h: Address 80h)

Table 177: TX Queue Control Register (Page 30h: Address 80h)

Bit	Name	R/W	Description	Default
7:4	Reserved	R/W	–	0
3:2	Reserved	R/W	–	–
1:0	QOS_PRIORITY_CTRL	R/W	Best Effort Queues Priority Control This field controls the best effort queues' scheduling priority. It doesn't affect the behavior of COS4 and COS5. 00: all queues are weighted round robin 01: COS3 is strict priority, COS2-COS0 are weighted round robin. 10: COS3 and COS2 is strict priority, COS1-COS0 are weighted round robin. 11: COS3, COS2, COS1 and COS0 are in strict priority. Strict priority: When it is in strict priority, the priority is COS3 > COS2 > COS1 > COS0. The G_TXPORT will always serve the higher queue first if it is not empty. In this mode, the service weight are don't care. Weighted round robin: When it is in weighted round robin mode, the queues are scheduled in a round robin way according to the service weight of each queue.	00

See "Quality of Service" on page 34 for more information.

TX Queue Weight Register (Page 30h: Address 81h)

Table 178: TX Queue Weight Register Queue[0:3] (Page 30h: Address 81h–84h)

Bit	Name	R/W	Description	Default
7:0	QSERV_WEIGHT	R/W	Queue weight register The binary value of these bits sets the service weight of the given queue. The value of 1 allows the queue to send one packet for every round; the value of 4 allows the queue to send four packets for every round. It is suggested that the weight of each queue be Q3 > Q2 > Q1 > Q0 > 0. ***Note:*** The maximum allowable transmit queue weight is 31h. Programming a higher weight than 31h can yield unexpected results. This field must not be programmed as zero.	Queue: 0: 0001 1: 0010 2: 0100 3: 1000

See "Quality of Service" on page 34 for more information.

COS4 Service Weight Register (Page 30h: Address 85h–86h)

Table 179: COS4 Service Weight Register (Page 30h: Address 85h–86h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	0
8	COS4 Strict Priority	R/W	COS4 Strict Priority When this field is set to ‘1’, the C4 service weight is don’t care and Class 4 is in strict priority over the best effort queues (COS3–COS0).	1
7:0	COS4 Weight	R/W	COS4 Service Weight This field defines the service weight between Class 4 traffic and the Best Effort COS3-COS0. When this field is N, it means Class-4:Best-Effort = N:1 When in weighted round robin mode, it is meaningless to set this field as zero.	1

Page 31h: Port-Based VLAN Registers

Table 180: Page 31h VLAN Registers

Address	Bits	Description
00h–11h	16/port	"Port-Based VLAN Control Register (Page 31h: Address 00h)" on page 235
1Fh–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Port-Based VLAN Control Register (Page 31h: Address 00h)

Table 181: Port-Based VLAN Control Register Address Summary

Address	Description
00h–01h	Port 0
02h–03h	Port 1
04h–05h	Port 2
06h–07h	Port 3
08h–09h	Port 4
0Ah–0Bh	Port 5
0Ch–0Dh	Port 6
0Eh–0Fh	Port 7
10h–11h	IMP port

Table 182: Port VLAN Control Register (Page 31h: Address 00h–11h)

BIt	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
8:0	FORWARD_MASK	R/W	VLAN forwarding mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Disable VLAN forwarding to egress port. 1 = Enable VLAN forwarding to egress port.	1FFh

For more information, see "Port-Based VLAN" on page 38.

Page 32h: Trunking Registers

Table 183: Page 32h Trunking Registers

Address	Bits	Description
00h	8	"MAC Trunking Control Register (Page 32h: Address 00h)" on page 236
01h–0Fh	–	Reserved
10h–11h	16	Trunk group 0 register
12h–13h	16	Trunk group 1 register
14h–15h	–	Reserved
16h–17h	–	Reserved
18h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

MAC Trunking Control Register (Page 32h: Address 00h)

Table 184: MAC Trunk Control Register (Page 32h: Address 00h)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	–	–
3	MAC_BASE_TRNK_EN	–	Enable MAC base trunking	–
2	Reserved	–	–	–
1:0	TRK_HASH_INDX	R/W	Trunk hash index selector 00 = Use hash [DA,SA] to generate index. 01 = Use hash [DA] to generate index. 10 = Use hash [SA] to generate index. 11 = Illegal state	0

See "Port Trunking/Aggregation" on page 43 for more information.

Trunking Group 0 Register (Page 32h: Address 10h)

Table 185: Trunk Group 0 Register (Page 32h: Address 10h–11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:9	Reserved	R/W	–	0
8:0	Trunk Group Enable	R/W	Trunk group enable 1 = Enable trunk group. 0 = Disable trunk group. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

See “Port Trunking/Aggregation” on page 43 for more information.

Trunking Group 1 Register (Page 32h: Address 12h)

Table 186: Trunk Group 1 Register (Page 32h: Address 12h–13h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:9	Reserved	R/W	–	0
8:0	Trunk Group Enable	R/W	Trunk group enable 1 = Enable trunk group. 0 = Disable trunk group. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Page 34h: IEEE 802.1Q VLAN Registers

Table 187: Page 34h IEEE 802.1Q VLAN Registers

Address	*Bits*	*Description*
00h	8	“Global IEEE 802.1Q Register (Pages 34h: Address 00h)” on page 238
01h	8	“Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)” on page 239
02h	8	“Global VLAN Control 2 Register (Page 34h: Address 02h)” on page 240
03h–04h	16	“Global VLAN Control 3 Register (Page 34h: Address 03h)” on page 241
05h	8	“Global VLAN Control 4 Register (Page 34h: Address 05h)” on page 241
06h	8	“Global VLAN Control 5 Register (Page 34h: Address 06h)” on page 242
07h	8	Reserved
0Ah–0Bh	16	“VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)” on page 243

Table 187: Page 34h IEEE 802.1Q VLAN Registers (Cont.)

Address	Bits	Description
Reserved	32	Reserved
10h–21h	16/port	"Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)" on page 244
20h–2Fh	–	Reserved
30h–31h	16	"Double Tagging TPID Register (Page 34h: Address 30h–31h)" on page 245
32h–33h	16	"ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)" on page 245
34h–3Fh	–	Reserved
40h–43h	32	Reserved
44h–48h	32	Reserved
49h–EFh	–	–
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Table 188: Global IEEE 802.1Q Register (Pages 34h: Address 00h)

Bit	Name	R/W	Description	Default
7	Enable IEEE 802.1Q	R/W	Enable IEEE 802.1Q VLAN 0 = Disable IEEE 802.1Q VLAN. 1 = Enable IEEE 802.1Q VLAN. See "Programming the VLAN Table" on page 40 for more information. ***Note:*** This bit must be set if double tagging mode enable in "Global VLAN Control 4 Register (Page 34h: Address 05h)" on page 241.	0
6:5	VLAN Learning Mode	R/W	VLAN learning mode 00 = SVL (Shared VLAN learning mode) (MAC hash ARL table) 11 = IVL (Individual VLAN learning mode) (MAC and VID hash ARL table) 10 = Illegal setting 01 = Illegal setting ***Note:*** Applied to 802.1Q enable and DT_Mode.	11
4	Reserved	R/W	Reserved	0

Table 188: Global IEEE 802.1Q Register (Pages 34h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
3	Change_1Q_VID	R/W	Change 1Q VID to PVID 1 = • For a single tag frame with VID not = 0, change the VID to PVID. • For a double tag frame with outer VID not = 0, change outer VID to PVID. 0 = No change for 1Q/ISP tag if VID is not 0.	0
2	Reserved	R/W	Reserved	0
1	Reserved	R/W	Reserved	1
0	Reserved	R/W	Reserved	1

See "IEEE 802.1Q VLAN" on page 39 for more information.

Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)

Table 189: Global VLAN Control 1 Register (Page 34h: Address 01h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	Multicast Untag Check	R/W	Multicast VLAN untagged map check bypass 1 = Multicast frames are not checked against the VLAN untagged map. 0 = Multicast frames are checked against the VLAN untagged map. Does not apply to the frame management port.	0
5	Multicast Forward Check	R/W	Multicast VLAN forward map check bypass 1 = Multicast frames are not checked against the VLAN forward map. 0 = Multicast frames are checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable and DT_Mode.	0
4	Reserved	R/W	It is illegal to set 1.	0
3	Reserved Multicast Untag Check	R/W	Reserved multicast (except GMRP and GVRP) VLAN untagged map check bit 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN untagged map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN untagged map. Does not apply to the frame management port.	0

Table 189: Global VLAN Control 1 Register (Page 34h: Address 01h) (Cont.)

Bit	*Name*	*R/W*	*Description*	*Default*
2	Reserved Multicast Forward Check	R/W	Reserved multicast (except GMRP and GVRP) VLAN forward map check bit 1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN forward map. 0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable and DT_Mode.	0
1	Reserved	R/W	It is illegal to set 0.	1
0	Reserved	R/W	Reserved	0

For more information, see “IEEE 802.1Q VLAN” on page 39.

Global VLAN Control 2 Register (Page 34h: Address 02h)

Table 190: Global VLAN Control 2 Register (Page 34h: Address 02h)

Bit	*Name*	*R/W*	*Description*	*Default*
7	Reserved	R/W	Reserved	0
6	GMRP/GVRP Untag Check	R/W	GMRP or GVRP VLAN untag map check bit 1 = GMRP or GVRP frames are checked against the VLAN untagged map. 0 = GMRP or GVRP frames are not checked against the VLAN untagged map. ***Note:*** Does not apply to the frame management port.	0
5	GMRP/GVRP Forward Check	R/W	GMRP or GVRP VLAN forward map check bit 1 = GMRP or GVRP frames are checked against the VLAN forward map. 0 = GMRP or GVRP frames are not checked against the VLAN forward map. ***Note:*** Does not apply to the frame management port. Applied to 802.1Q enable and DT_Mode.	0
4	Reserved	R/W	Reserved	1
3	Reserved	R/W	Reserved	0
2	IMP Frame Forward Bypass	R/W	IMP Frame VLAN forward map check bit 1 = IMP frames are not checked against the VLAN forward map. 0 = IMP frames are checked against the VLAN forward map. ***Note:*** Applied to 802.1Q enable and DT_Mode.	0
1:0	Reserved	R/W	Reserved	00

For more information, see "IEEE 802.1Q VLAN" on page 39.

Global VLAN Control 3 Register (Page 34h: Address 03h)

Table 191: Global VLAN Control 3 Register (Page 34h: Address 03h–04h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	–	–
7:0	Drop Non1Q Frames	R/W	Drop non1Q frames When enabled, any frame without an IEEE 802.1Q tag is dropped by this port. This field does not apply to IMP port. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively.	0

Global VLAN Control 4 Register (Page 34h: Address 05h)

Table 192: Global VLAN Control 4 Register (Page 34h: Address 05h)

Bit	Name	R/W	Description	Default
7:6	Source Membership Check	R/W	Source membership check bit Frames with a VID matching a corresponding entry in the VLAN table can be checked for source membership. The source is a member only when the source address of the frame is included as a member in the corresponding VLAN entry. 00 = Forward frame, but do not learn the SA into the ARL table. 01 = Drop frame. 10 = Forward frame, and learn the SA into the ARL table. 11 = Forward frame to IMP, but not learn. ***Note:*** Does not apply to IMP port.	11
5	Forward GVRP to Management	R/W	Forward all GVRP frames to the frame management port bit. 1 = GVRP frames are forwarded to the management port. 0 = GVRP frames are not forwarded to the management port.	0
4	Forward GMRP to Management	R/W	Forward All GMRP Frames to the frame management port bit. 1 = GMRP frames are forwarded to the management port. 0 = GMRP frames are not forwarded to the management port.	0

Table 192: Global VLAN Control 4 Register (Page 34h: Address 05h) (Cont.)

Bit	Name	R/W	Description	Default
3:2	En_DT_Mode	R/W	00 = Disable double tagging mode 01 = Enable DT_Mode (double tagging mode) 10 = Reserved 11 = Reserved	2'b00
1	RSV_MCAST_FLOOD	R/W	When the BCM53118 is configured to operate in double tag feature management mode. 1 = Flood (including all data port and CPU), reserved mcast is based on the VLAN rule. 0 = Trap reserved mcast to CPU. Reserved mcast include: 01-80-C2-00-00- (00,02~2F)	
0	Reserved	R/W	–	0

For more information, see "IEEE 802.1Q VLAN" on page 39.

Global VLAN Control 5 Register (Page 34h: Address 06h)

Table 193: Global VLAN Control 5 Register (Page 34h: Address 06h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	Tag Status Preserve	R/W	IEEE 802.1Q tag/untag status preserved at egress. 1 = Regardless of untag map in VLAN table, non-1Q frames (including 802.1p frames) will not be changed at TX (egress). This field has no effect in double tagging mode (DT_Mode).	0
5	Reserved	R/W	Reserved	0
4	Trunk Check Bypass	R/W	Trunk check bypass 1 = Egress directed frames issued from the IMP port bypass trunk checking. 0 = Egress directed frames issued from the IMP port are subject to trunk checking and redirection.	1
3	Drop Invalid VID	R/W	Drop frames with invalid VID. Frames with an invalid VID do not have a corresponding entry in the VLAN table. 1 = Ingress frames with invalid VID are dropped. 0 = Ingress frames with invalid VID are forwarded to the IMP port.	0
2	VID_FFF_Fwding	R/W	Enable VID FFF forward 1 = Forward frame 0 = Comply with standard, drop frame	0
1	Reserved	R/W	Reserved	0

Table 193: Global VLAN Control 5 Register (Page 34h: Address 06h) (Cont.)

Bit	Name	R/W	Description	Default
0	Management CRC Check Bypass	R/W	Bypass CRC check at the frame management port. 1 = Ignore CRC check 0 = Check CRC	0

For more information, see "IEEE 802.1Q VLAN" on page 39.

VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Table 194: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	–	0
11	EN_MPORT5_untagmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN untag map. Does not apply to the frame management port.	0
10	EN_MPORT5 _fwdmap	R/W	When set to 1, MPORT_ADD5 is checked by VLAN forward map. Does not apply to the frame management port.	0
9	EN_MPORT4_untagmap	R/W	When set to 1, MPORT_ADD4 will be checked by VLAN untag map. Does not apply to the frame management port.	0
8	EN_MPORT4 _fwdmap	R/W	When set to 1, MPORT_ADD4 will be checked by VLAN forward map. Does not apply to the frame management port.	0
7	EN_MPORT3_untagmap	R/W	When set to 1, MPORT_ADD3 will be checked by VLAN untag map. Does not apply to the frame management port.	0
6	EN_MPORT3 _fwdmap	R/W	When set to 1, MPORT_ADD3 will be checked by VLAN forward map. Does not apply to the frame management port.	0
5	EN_MPORT2_untagmap	R/W	When set to 1, MPORT_ADD2 will be checked by VLAN untag map. Does not apply to the frame management port.	0
4	EN_MPORT2 _fwdmap	R/W	When set to 1, MPORT_ADD2 will be checked by VLAN forward map. Does not apply to the frame management port.	0
3	EN_MPORT1_untagmap	R/W	When set to 1, MPORT_ADD1 will be checked by VLAN untag map. Does not apply to the frame management port.	0

Table 194: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
2	EN_MPORT1 _fwdmap	R/W	When set to 1, MPORT_ADD1 will be checked by VLAN forward map. Does not apply to the frame management port.	0
1	EN_MPORT0_untagmap	R/W	When set to 1, MPORT_ADD0 will be checked by VLAN untag map. Does not apply to the frame management port.	0
0	EN_MPORT0 _fwdmap	R/W	When set to 1, MPORT_ADD0 will be checked by VLAN forward map. Does not apply to the frame management port.	0

Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)

Table 195: Default IEEE 802.1Q Tag Register Address Summary

Address	Description
10h–11h	Port 0
12h–13h	Port 1
14h–15h	Port 2
16h–17h	Port 3
18h–19h	Port 4
1Ah–1Bh	Port 5
1Ch–1Dh	Port 6
1Eh–1Fh	Port 7
20h–21h	IMP port

Table 196: Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)

Bit	Name	R/W	Description	Default
15:13	DEFAULT_PRI/ PORT_QOS_PRI	R/W	Default IEEE 802.1Q priority If an IEEE 802.1Q tag is added to an incoming untagged frame (IEEE 802.1Q VLAN or Double-Tagging enabled), these bits are the default priority value for the new tag. See "IEEE 802.1Q VLAN" on page 39 and "Double-Tagging" on page 40 for more information. Port-based QoS priority map bits When port-based QoS is enabled in the Table : "QoS Global Control Register (Page 30h: Address 00h)," on page 226, these bits represent the TC for the ingress port. The TC determines the TX queue for each frame based on the "TC_To_COS Mapping Register (Page 30h: Address 62h–63h)" on page 231.	000
12	CFI	R/W	Conical form indicator	0

Table 196: Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h) (Cont.)

Bit	Name	R/W	Description	Default
11:0	DEFAULT_VID	R/W	Default IEEE 802.1Q VLAN ID If an IEEE 802.1Q tag is tagged to an incoming non-IEEE 802.1Q frame (IEEE 802.1Q VLAN or Double-Tagging enabled), then these bits are the default VID for the new tag. See "IEEE 802.1Q VLAN" on page 39 and "Double-Tagging" on page 40 for more information.	001

Double Tagging TPID Register (Page 34h: Address 30h–31h)

Table 197: Double Tagging TPID Register (Page 34h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:0	ISP_TPID	R/W	The TPID used to identify double tagged frame.	9100

ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Table 198: ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:8	RESERVED	–	–	0
7:0	ISP_Portmap	R/W	Bitmap that defines which port is designated as the ISP port. Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Indicates that it is not an ISP port. 1 = Indicates that it is an ISP port.	–

Page 36h: DOS Prevent Register

Table 199: DOS Prevent Register

Address	Bits	Description
00h–03h	32	"DOS Control Register (Page 36h: Address 00h–03h)" on page 246
04h	8	"Minimum TCP Header Size Register (Page 36h: Address 04h)" on page 248
08h–0Bh	32	"Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)" on page 248
0Ch–0Fh	32	"Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)" on page 248
10h	8	"DOS Disable Learn Register (Page 36h: Address 10h)" on page 249
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

DOS Control Register (Page 36h: Address 00h–03h)

Table 200: DOS Control Register (Page 36h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:14	Reserved	RO	–	0
13	ICMPv6_LongPing_DROP_EN	R/W	The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size. 1= Drop 0= Do not drop	0
12	ICMPv4_LongPing_DROP_EN	R/W	The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header. 1= Drop 0= Do not drop	0
11	ICMPv6_Fragment_DROP_EN	R/W	The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram. 1= Drop 0= Do not drop	0

Table 200: DOS Control Register (Page 36h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
10	ICMPv4_Fragment_DROP_EN	R/W	The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram. 1= Drop 0= Do not drop	0
9	TCP_FragError_DROP_EN	R/W	The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data. 1 = Drop 0 = Do not drop	00
8	TCP_ShortHDR_DROP_EN	R/W	The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size. 1 = Drop 0 = Do not drop	00
7	TCP_SYNError_DROP_EN	R/W	SYN = 1, ACK = 0, and SRC_Port<1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1= Drop 0= Do not drop	0
6	TCP_SYNFINScan_DROP_EN	R/W	SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1= Drop 0= Do not drop	0
5	TCP_XMASScan_DROP_EN	R/W	Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop 0 = Do not drop	0
4	TCP_NULLScan_DROP_EN	R/W	Seq_Num = 0 and all TCP_FLAGs = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1= Drop 0= Do not drop	0

Table 200: DOS Control Register (Page 36h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
3	UDP_BLAT_DROP_EN	R/W	DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1= Drop 0= Do not drop	0
2	TCP_BLAT_DROP_EN	R/W	DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1= Drop 0= Do not drop	0
1	IP_LAN_DRIP_EN	R/W	IPDA = IPSA in an IPv4/v6 datagram. 1=Drop 0=Do not drop	0
0	RESERVED	R/W	Reserved	1

Minimum TCP Header Size Register (Page 36h: Address 04h)

Table 201: Minimum TCP Header Size Register (Page 36h: Address 04h)

Bit	Name	R/W	Description	Default
7:0	MIN_TCP_HDR_SZ	R/W	Minimum TCP header size allowed (0–256 bytes).	8'h14

Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)

Table 202: Maximum ICMPv4 Size Register (Page 36h: Address 08h-0Bh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv4_SIZE	R/W	Max ICMPv4 size allowed (0–9.6K bytes).	32'd512

Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)

Table 203: Maximum ICMPv6 Size Register (Page 36h: Address 0Ch-0Fh)

Bit	Name	R/W	Description	Default
31:0	MAX_ICMPv6_SIZE	R/W	Max ICMPv6 size allowed (0–9.6K bytes).	32'd512

DOS Disable Learn Register (Page 36h: Address 10h)

Table 204: DOS Disable Learn Register (Page 36h: Address 08h-0Bh)

Bit	*Name*	*R/W*	*Description*	*Default*
7:1	RESERVED	R/W	Reserved	–
0	DOS Disable Lrn	R/W	When this bit enabled, all frames dropped by DOS prevent will not be learned.	0

Page 40h: Jumbo Frame Control Register

Table 205: Page 40h Jumbo Frame Control Register

Address	*Bits*	*Description*
00h	–	Reserved
01h–04h	32	"Jumbo Frame Port Mask Register (Page 40h: Address 01h)" on page 249
05h–06h	16	"Standard Max Frame Size Register (Page 40h: Address 05h)" on page 250
07h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Jumbo Frame Port Mask Register (Page 40h: Address 01h)

Table 206: Jumbo Frame Port Mask Registers (Page 40h: Address 01h–04h)

BIt	*Name*	*R/W*	*Description*	*Default*
31:25	Reserved	RO	–	0
24:9	Reserved	R/W	–	0
8:0	JUMBO_PORT_MASK	R/W	Jumbo frame port mask Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. 0 = Disable jumbo frame capability on the port. 1 = Enable jumbo frame capability on the port. Jumbo frames can be ingressed and egressed only to the ports enabled via this port mask. Jumbo frame port mask has no effect on the traffic of normal sized frames. See "Jumbo Frame Support" on page 43 for more information.	0

Note: When the Jumbo Frame feature is enabled, the assigned Weight value for the WRR scheduling cannot be applied fairly over the queues. This is due to the internal Packet Buffer Memory size limitation.

Note: The Jumbo Frame feature is only supported in 1000 Mbps mode.

Standard Max Frame Size Register (Page 40h: Address 05h)

Table 207: Standard Max Frame Size Registers (Page 40h: Address 05h–06h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	–	0
13:0	Standard Max Frame Size	R/W	Standard Max Frame Size Defines the standard maximum frame size for MAC and MIB counter. This register only allowed to be configured as 14'd1518 or 14'd2000. When jumbo is disabled, the content of this register is used to define good frame length. • If it is configured as 1518, the tagged frames will be dropped if the frame length is larger than 1522 bytes; and the untagged frames will be dropped if the frame length is larger than 1518 bytes. • If it is configured as 2000, both tagged and untagged frames will be dropped if the frame length is larger than 2000 bytes. When jumbo is enabled, all frames will be dropped if the frame length is larger than 9720 bytes. The register setting affects the following MIB parameters: • RxSAChange • RxGoodOctets • RxUnicastPkts • RxMulticastPkts • RxBroadcastPkts • RxOverSizePkts	‘d2000

Page 41h: Broadcast Storm Suppression Register

Table 208: Broadcast Storm Suppression Register (Page 41h)

Address	Bits	Description
00h–03h	32	"Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251
04h–0Fh	–	Reserved
10h–33h	32/port	"Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253
34h–4Fh	–	Reserved
50h–73h	–	Reserved
74h–7Fh	–	Reserved
80h–91h	16/port	"Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)" on page 255
92h–BFh	–	Reserved
C0h	8	"IMP Port Egress Rate Control Configuration Register (Page 41h: Address C0h)" on page 256
C2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Ingress Rate Control Configuration Register (Page 41h: Address 00h)

Table 209: Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h)

BIt	Name	R/W	Description	Default
31:19	Reserved	RO	–	0
18	XLENEN	R/W	Packet Length Selection 0 = RX rate excludes IPG. 1 = RX rate includes IPG (and Preamble + SFD).	0
17	BUCK1_ BRM_SEL	R/W	Bit rate mode selection 0 = Absolute bit rate mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode—The rate count in the "Port Receive Rate Control Register (Page 41h: Address 10h)" on page 253 represents the incoming bit rate normalized with respect to the link speed mode. See "Rate Control" on page 44 for more details.	0
16	Reserved	R/W	Reserved	1

Table 209: Ingress Rate Control Configuration Register (Page 41h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
15:9	BUCK1_PACKET_TYPE	R/W	Suppressed packet type mask. This bit mask determines the type of packets to be monitored by bucket 1. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: Bit 9: Unicast lookup hit Bit 10: Multicast lookup hit Bit 11: Reserved MAC Address Frame Bit 12: Broadcast Bit 13: Multicast lookup failure Bit 14: Unicast lookup failure Bit 15: Reserved See “Rate Control” on page 44 for more details.	0
8	BUCK0_ BRM_SEL	R/W	Bit rate mode selection 0 = Absolute bit rate mode—The rate count in the “Port Receive Rate Control Register (Page 41h: Address 10h)” on page 253 represents the incoming bit rate as an absolute data rate. 1 = Bit rate normalized to link speed mode—The rate count in the “Port Receive Rate Control Register (Page 41h: Address 10h)” on page 253 represents the incoming bit rate normalized with respect to the link speed mode. See “Rate Control” on page 44 for more details.	BC_SUPP_EN
7	Reserved	R/W	Reserved	1
6	XLENEN_EG	R/W	Packet length selection for egress rate control. 0 = TX Rate Exclude IPG 1 = TX Rate Include IPG (and Preamble + SFD)	0
5:0	BUCK0_PACKET_TYPE	R/W	Suppressed packet type mask. This bit mask determines the type of packets to be monitored by bucket 0. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this bit field are defined as follows: Bit 0: Unicast lookup hit Bit 1: Multicast lookup hit Bit 2: Reserved MAC address frame Bit 3: Broadcast Bit 4: Multicast lookup failure Bit 5: Unicast lookup failure See “Rate Control” on page 44 for more details.	BC_SUPP_EN: 1: 001000 0: 000000

Port Receive Rate Control Register (Page 41h: Address 10h)

Table 210: Port Rate Control Register Address Summary

Address	Description
10h–13h	Port 0
14h–17h	Port 1
18h–1Bh	Port 2
1Ch–1Fh	Port 3
20h–23h	Port 4
24h–27h	Port 5
28h–2Bh	Port 6
2Ch–2Fh	Port 7
30h–33h	IMP port for BCM53118

Table 211: Port Rate Control Register (Page 41h: Address 10h–33h)

BIt	Name	R/W	Description	Default
31:29	Reserved	RO	–	0
28	STRM_SUPR_EN	R/W	Enable storm suppression (Supported by bucket1). 0 = Disable 1 = Enable	Reflects the strap pin BC_SUPP_EN
27	RsvMC_SUPR_EN	R/W	Enable reserved mulitcast storm suppression. 0 = Disable 1 = Enable	0
26	BC_SUPR_EN	R/W	Enable broadcast storm suppression. 0 = Disable 1 = Enable	0
25	MC_SUPR_EN	R/W	Enable multicast storm suppression. 0 = Disable 1 = Enable	0
24	DLF_SUPR_EN	R/W	Enable DLF storm suppression. 0 = Disable 1 = Enable	0
23	Enable Bucket1	R/W	Enable rate control of the ingress port, bucket 1. 0 = Disable 1 = Enable	0
22	Enable Bucket0	R/W	Enable rate control of the ingress port, bucket 0. 0 = Disable 1 = Enable	Reflects the strap pin BC_SUPP_EN

Table 211: Port Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

BIt	Name	R/W	Description	Default
21:19	BUCK1_SIZE	R/W	Bucket size This bit determines the maximum size of bucket 1. This is specified on a per port basis. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB 100 = 64 KB 101 = 500 KB 110 = 500 KB 111 = 500 KB See "Rate Control" on page 44 for more details.	000
18:11	BUCK1_Rate_Cnt	R/W	Rate count The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251. See "Rate Control" on page 44 for more details. Values written to these bits must be with the ranges specified by Table 3 on page 46. Values outside these ranges are not valid.	10h
10:8	BUCK0_SIZE	R/W	Bucket size This bit determines the maximum size of bucket 0. This is specified on a per port basis. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB 100 = 64 KB 101 = 500 KB 110 = 500 KB 111 = 500 KB See "Rate Control" on page 44 for more details.	000

Table 211: Port Rate Control Register (Page 41h: Address 10h–33h) (Cont.)

Bit	Name	R/W	Description	Default
7:0	BUCK0_Rate_Cnt	R/W	Rate count The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed packet type mask in the "Ingress Rate Control Configuration Register (Page 41h: Address 00h)" on page 251. See "Rate Control" on page 44 for more details.	10h

Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)

Table 212: Port Egress Rate Control Configuration Register Address Summary

Address	Description
80h–81h	Port 0
82h–83h	Port 1
84h–85h	Port 2
86h–87h	Port 3
88h–89h	Port 4
8Ah–8Bh	Port 5
8Ch–8Dh	Port 6
8Eh–8Fh	Port 7
90h–91h	IMP port

Table 213: Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	–	0
11	ERC_EN	R/W	Egress rate control enable ((Absolute Bit Rate)	0

Table 213: Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h) (Cont.)

BIt	Name	R/W	Description	Default
10:8	BKT_SZE	R/W	Bucket size This bit determines the maximum size of bucket 0. This is specified on a per port basis. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB 100 = 64 KB 101 = 500 KB 110 = 500 KB 111 = 500 KB See “Rate Control” on page 44 for more details.	0
7:0	RATE_CNT	R/W	Rate count for bucket	0

IMP Port Egress Rate Control Configuration Register (Page 41h: Address C0h)

Table 214: IMP Port Egress Rate Control Configuration Register Address Summary

Address	Description
C0h	IMP Port

Table 215: IMP Port Egress Rate Control Configuration Registers (Page 41h: Address C0h)

BIt	Name	R/W	Description	Default
7:6	RESERVED	RO	Reserved	0
5:0	Rate_Index	R/W	Rate_Index is used to configure different egress rates for IMP in packet per second (pps). See Table 216: “Using Rate_Index to Configure Different Egress Rates for IMP in pps,” on page 257. When set to 0, the egress rate is limited to a maximum of 384 pps. When set to 63, the egress rate control function is disabled and all packets are transmitted at wire-speed. ***Note:*** If the Rate_Index is configured as a certain value, the egress rate is limited to the corresponding speed whether the switch is running at 10 Mbps, 100 Mbps, or 1 Gbps. ***Note:*** The Rate_Index should be a reasonable value under the corresponding network speed configuration. It does not make sense to set a value of 63 with the network configuration at 10 Mbps. In that case, the egress rate is limited up to 10 Mbps.	6'd63

Table 216: Using Rate_Index to Configure Different Egress Rates for IMP in pps

Rate_Index	*pps*	*Rate_Index*	*pps*	*Rate_Index*	*pps*	*Rate_Index*	*pps*
0	384	16	5376	32	25354	48	357143
1	512	17	5887	33	27382	49	423729
2	639	18	6400	34	29446	50	500000
3	768	19	6911	35	31486	51	568182
4	1024	20	7936	36	35561	52	641026
5	1280	21	8960	37	39682	53	714286
6	1536	22	9984	38	42589	54	781250
7	1791	23	11008	39	56818	55	862069
8	2048	24	12030	40	71023	56	925926
9	2303	25	13054	41	85324	57	1000000
10	2559	26	14076	42	99602	58	1086957
11	2815	27	15105	43	113636	59	1136364
12	3328	28	17146	44	127551	60	1190476
13	3840	29	19201	45	142045	61	1250000
14	4352	30	21240	46	213675	62	1315789
15	4863	31	23299	47	284091	63	1388889

Page 42h: EAP Register

Table 217: Broadcast Storm Suppression Register (Page 42h)

Address	*Bits*	*Description*
00h	8	"EAP Global Control Register (Page 42h: Address 00h)" on page 258
01h	8	"EAP Multiport Address Control Register (Page 42h: Address 01h)" on page 258
02h–09h	64	"EAP Destination IP Register 0 (Page 42h: Address 02h)" on page 259
0Ah–12h	64	"EAP Destination IP Register 1 (Page 42h: Address 0Ah)" on page 259
20h–5Fh	64	"Port EAP Configuration Register (Page 42h: Address 20h)" on page 259
60h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

EAP Global Control Register (Page 42h: Address 00h)

Table 218: EAP Global Control Registers (Page 42h: Address 00h)

BIt	Name	R/W	Description	Default
7	Reserved	–	–	0
6	EN_RARP	–	When EAP_BLK_MODE is set: 1: Allow RARP to pass. 0: Drop RARP	0
5	EN_BPDU	–	When EAP_BLK_MODE is set: 1: BPDU Addresses are allowed to pass. 0: Drop	–
4	EN_RMC	–	When EAP_BLK_MODE is set: 1: Allows DA = 01-80-C2-00-00-02, 04~0F to pass. 0: Drop DA = 01-80-C2-00-00-02, 04~0F to pass.	–
3	EN_DHCP	–	When EAP_BLK_MODE is set: 1: Allows DHCP to pass 0: Drop DHCP	–
2	EN_ARP	–	When EAP_BLK_MODE is set: 1: Allows ARP to pass 0: Drop ARP	–
1	EN_2DIP	R/W	When EAP_BLK_MODE bit is set: 1: Two subnet IP addresses defined in EAP destination IP registers 0 and 1 are allowed to pass. 0: Drop	0
0	Reserved	–	–	0

EAP Multiport Address Control Register (Page 42h: Address 01h)

Table 219: EAP Multiport Address Control Register (Page 42h: Address 01h)

BIt	Name	R/W	Description	Default
7:6	Reserved	RO	–	–
5	EN_MPORT5	R/W	1: Allow Multiport ETYPE Address 5 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–
4	EN_MPORT4	R/W	1: Allow Multiport ETYPE Address 4 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–

Table 219: EAP Multiport Address Control Register (Page 42h: Address 01h) (Cont.)

BIt	Name	R/W	Description	Default
3	EN_MPORT3	R/W	1: Allow Multiport ETYPE Address 3 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–
2	EN_MPORT2	R/W	1: Allow Multiport ETYPE Address 2 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–
1	EN_MPORT1	R/W	1: Allow Multiport ETYPE Address 1 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–
0	EN_MPORT0	R/W	1: Allow Multiport ETYPE Address 0 define at "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 to pass. 0: Drop	–

EAP Destination IP Register 0 (Page 42h: Address 02h)

Table 220: EAP Destination IP Registers 0 (Page 42h: Address 02h–09h)

BIt	Name	R/W	Description	Default
63:32	DIP_SUB 0	R/W	EAP destination IP subnet register 0	0
31: 0	DIP_MSK 0	R/W	EAP destination IP mask register 0	0

EAP Destination IP Register 1 (Page 42h: Address 0Ah)

Table 221: EAP Destination IP Registers 1 (Page 42h: Address 0Ah–12h)

BIt	Name	R/W	Description	Default
63:32	DIP_SUB 1	R/W	EAP destination IP subnet register 1	0
31:0	DIP_MSK 1	R/W	EAP destination IP mask register 1	0

Port EAP Configuration Register (Page 42h: Address 20h)

Table 222: Port EAP Configuration Register Address Summary

Address	Description
20h–27h	Port 0
28h–2Fh	Port 1
30h–37h	Port 2

Table 222: Port EAP Configuration Register Address Summary (Cont.)

Address	Description
38h–3Fh	Port 3
40h–47h	Port 4
48h−4Fh	Port 5
50h–57h	Port 6
58h−5Fh	Port 7

Table 223: Port EAP Configuration Registers (Page 42h: Address 20h–47h)

BIt	Name	R/W	Description	Default
63:55	Reserved	RO	–	0
52:51	EAP_MODE	R/W	00 = Basic mode, do not check SA. 01 = Reserved 10 = Extend mode, check SA and port number, drop if SA is unknown. 11 = Simplified mode, check SA and port number trap to management port if SA is unknown.	0
50:49	EAP_BLK_MODE	R/W	00: Do not check EAP_BLK_MODE. 01: To check EAP_BLK MODE on ingress port, only the frame defined in EAP_GCFG will be forwarded. Otherwise, the frame will be dropped. 10: reserved 11: To check EAP_BLK MODE on both ingress and egress port, only the frame defined in EAP_GCFG will be forwarded. The forwarding process will verify that each egress port is at block mode.	0
48	EAP_EN_DA	R/W	Enable EAP frame with DA	0
47:0	EAP_DA	R/W	EAP frame DA register	00-00-00-00-00-00

Page 43h: MSPT Register

Table 224: Broadcast Storm Suppression Register (Page 43h)

Address	Bits	Description
00h	8	MSPT control register
01h	–	Reserved
02h–05h	32	“MSPT Aging Control Register (Page 43h: Address 02h)” on page 261
06h–0Fh	–	Reserved
10h–2Fh	32	“MSPT Table Register (Page 43h: Address 10h)” on page 262
30h–4Ah	–	Reserved
50h–51h	16	“SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)” on page 263
52h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 276
FFh	8	“Page Register (Global, Address FFh)” on page 277

MSPT Control Register (Page 43h: Address 00h)

Table 225: MSPT Control Registers (Page 43h: Address 00h–01h)

BIt	Name	R/W	Description	Default
7:1	Reserved	–	–	0
0	EN_802.1S	R/W	0: Disable 1: Enable	0

MSPT Aging Control Register (Page 43h: Address 02h)

Table 226: MSPT Aging Control Registers (Page 43h: Address 02h–05h)

BIt	Name	R/W	Description	Default
31:8	Reserved	R/W	–	0
7: 0	MSPT_AGE_MAP	R/W	Per spanning tree aging enable	0

MSPT Table Register (Page 43h: Address 10h)

Table 227: MSPT Table Register Address Summary

Address	Description
10h–13h	MSPT 0
14h–17h	MSPT 1
18h–1Bh	MSPT 2
1Ch–1Fh	MSPT 3
20h–23h	MSPT 4
24h–27h	MSPT 5
28h–2Bh	MSPT 6
2Ch–2Fh	MSPT 7

Table 228: MSPT Table Registers (Page 43h: Address 10h–2Fh)

BIt	Name	R/W	Description	Default
31:27	Reserved	RO	–	0
26:24	Reserved	R/W	–	0
23:21	Reserved	R/W	Spanning tree state for port 7	0
20:18	Reserved	R/W	Spanning tree state for port 6	0
17:15	SPT_STA5	R/W	Spanning tree state for port 5	0
14:12	SPT_STA4	R/W	Spanning tree state for port 4 000 = No spanning tree 001 = Disabled 010 = Blocking 011 = Listening 100 = Learning 101 = Forwarding	0
11:9	SPT_STA3	R/W	Spanning tree state for Port 3	0
8:6	SPT_STA2	R/W	Spanning tree state for Port 2	0
5:3	SPT_STA1	R/W	Spanning tree state for Port 1	0
2:0	SPT_STA0	R/W	Spanning tree state for Port 0	0

SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

Table 229: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

BIt	Name	R/W	Description	Default
15:6	Reserved	RO	–	–
5	EN_MPORT5_BYPASS_SPT	R/W	1: The MPORT_ADD_5 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_5 is checked by SPT status.	–
4	EN_MPORT4_BYPASS_SPT	R/W	1: The MPORT_ADD_4 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_4 will be checked by SPT status.	–
3	EN_MPORT3_BYPASS_SPT	R/W	1: The MPORT_ADD_3 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_3 is checked by SPT status.	–
2	EN_MPORT2_BYPASS_SPT	R/W	1: The MPORT_ADD_2 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_2 is checked by SPT status.	–
1	EN_MPORT1_BYPASS_SPT	R/W	1: The MPORT_ADD_1 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_1 is checked by SPT status.	–
0	EN_MPORT0_BYPASS_SPT	R/W	1: The MPORT_ADD_0 of "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 173 is not checked by SPT status. 0: The MPORT_ADD_0 is checked by SPT status.	0

Page 70h: MIB Snapshot Control Register

Table 230: MIB Snapshot Control Register

Address	Bits	Description
00h	8	"MIB Snapshot Control Register (Page 70h: Address 00h)" on page 264
01h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276 bytes 0-7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

MIB Snapshot Control Register (Page 70h: Address 00h)

Table 231: MIB Snapshot Control Register (Page 70h: Address 00h)

Bit	Name	R/W	Description	Default
7	SNAPSHOT_START/DONE	R/W SC	Write 1'b1 to initiate MIB snapshot access, clear to 1'b0 when MIB snapshot access is done	0
6	SNAPSHOT_MIRROR	R/W	1'b1: enable read address to port MIB, but data from MIB snapshot memory. 1'b0: enable to read from port MIB memory	0
5:4	Reserved	R/W	–	–
3:0	SNAPSHOT_PORT	R/W	Port Number for MIB snapshot function	0

Page 71h: Port Snapshot MIB Control Register

Table 232: Port Snapshot MIB Control Register

Address	Bits	Description
71h	–	The Port Snapshot MIB Registers are same as registers in "MII Control Register (Page 10h–17h: Address 00h–01h)" on page 187

Page 72h: Loop Detection Register

Table 233: Loop Detection Control Register (Page 72h)

Address	*Bits*	*Description*
00h–01h	16	“Loop Detection Control Register (Page 72h: Address 00h)” on page 265
02h	8	“Discovery Frame Timer Control Register (Page 72h: Address 02h)” on page 266
03h–04h	16	“LED Warning Port Map Register (Page 72h: Address 03h)” on page 266
05h–0Ah	48	Module ID 0
0Bh–10h	48	Module ID 1
11h– 16h	48	Loop detect frame SA
17h–EFh	–	Reserved
F0h–F7h	8	“SPI Data I/O Register (Global, Address F0h)” on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	“SPI Status Register (Global, Address FEh)” on page 276
FFh	8	“Page Register (Global, Address FFh)” on page 277

Loop Detection Control Register (Page 72h: Address 00h)

Table 234: Loop Detection Control Registers (Page 72h: Address 00h–01h)

BIt	*Name*	*R/W*	*Description*	*Default*
15:13	Reserved	R/W	–	0
12	EN_LOOP_DETECT	R/W	Enable loop detection feature. 0 = Disable 1 = Enable	
11	LOOP_IMP_SEL	R/W	Enable IMP loop detection feature. 0 = Disable 1 = Enable	Strap
10:3	LED_RST_TIMR_CTRL	R/W	Number of missed discovery time before LED warning portmap to be reset.	
2	OV_PAUSE_ON	R/W	1 = Transmit frame in highest queue even the port is in pause on state. 0 = Transmit frame follow the pause state rule.	
1:0	DISCOVERY_FRAME_QUEUE_SEL	R/W	Specifies which queue to be put for the received discovery frame.	

Discovery Frame Timer Control Register (Page 72h: Address 02h)

Table 235: Discovery Frame Timer Control Registers (Page 72h: Address 02h)

BIt	Name	R/W	Description	Default
7:4	Reserved	R/W	–	0
3:0	Discover_Frame_Timer	R/W	From 1 second (default) to 15 seconds. Scale = 1s. 0000 = 1s 0001 = 2s 0002 = 3s . . . 1110 = 15s	0

LED Warning Port Map Register (Page 72h: Address 03h)

Table 236: LED Warning Port Map Registers (Page 72h: Address 03h–04h)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/O	–	0
8:0	LED_WARNING_PORT MAP	R/O	Bit 8: IMP port Bits [7:0] correspond to ports [7:0], respectively. Each bit shows the status of Loop Detected on the corresponding port.	0

Module ID 0 Register (Page 72h: Address 05h)

Table 237: Module ID 0 Registers (Page 72h: Address 05h–0Ah)

BIt	Name	R/W	Description	Default
47:0	Module_ID_SA	RO	–	0

Module ID 1 Register (Page 72h: Address 0Bh)

Table 238: Module ID 1 Registers (Page 72h: Address 0Bh–10h)

BIt	Name	R/W	Description	Default
47	Module_ID_AVAILABLE	RO	Module ID is available when the first packet is received. 0 = Unavailable 1 = Available	0
46:40	Reserved	RO	–	0
39:32	MODULE_ID_PORT_NO	RO	This is an 8-bit port number for module ID.	0

Table 238: Module ID 1 Registers (Page 72h: Address 0Bh–10h) (Cont.)

BIt	Name	R/W	Description	Default
31:0	MODULE_ID_CRC	RO	This is an 32-bit CRC for module ID.	0

Loop Detect Source Address Register (Page 72h: Address 11h)

Table 239: Loop Detect Source Address Registers (Page 72h: Address 11h–16h)

BIt	Name	R/W	Description	Default
47:0	LD_SA	R/W	Loop detection frame SA	01-80-C2-00-00-01

Page 88h: IMP Port External PHY MII Registers Page Summary

Table 240: IMP Port External PHY MII Registers Page Summary

Address	Bits	Description
88h	–	MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are “Page 10h–17h: Internal GPHY MII Registers” on page 185

Page 90h: BroadSync HD Register

Table 241: BroadSync HD Register

Address	Bits	Description
00h–01h	16	“BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)” on page 268
02h	8	“BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)” on page 268
03h	8	“BroadSync HD PCP Value Control Register (Page 90h: Address 03h)” on page 269
04h–05h	8	“BroadSync HD Max Packet Size Register (Page 90h: Address 04h)” on page 269
06h–09h	–	Reserved
10h–13h	32	“BroadSync HD Time Base Register (Page 90h: Address 10h–13h)” on page 269
14h–17h	32	“BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17)” on page 270
18h–1Bh	32	“BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)” on page 270
1Ch–1Fh	32	“BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)” on page 271
20h–2Fh	–	Reserved
30h–3Fh	16	“BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)” on page 271

Table 241: BroadSync HD Register (Cont.)

Address	Bits	Description
40h–5Fh	–	Reserved
60h–6Fh	16	"BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)" on page 272
70h–8Fh	–	Reserved
90h–AFh	32	"BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)" on page 273
B0h−CFh	–	Reserved
D0h	8	"BroadSync HD Egress Time Stamp Status Register (Page 90h: Address D0h)" on page 273
D1h–DFh	–	Reserved
E0h–E1h	16	"BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)" on page 274
B2h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276 bytes 0-7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)

Table 242: BroadSync HD Enable Control Register (Page 90h: Address 00h–01h)

BIt	Name	R/W	Description	Default
15:8	Reserved	RO	Reserved	0
7:0	BroadSync HD Enable	R/W	BroadSync HD enable. Bits [7:0] correspond to ports [7:0]	0

BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)

Table 243: BroadSync HD Time Stamp Report Control Register (Page 90h: Address 02h)

BIt	Name	R/W	Description	Default
7:1	Reserved	RO	Reserved	0
0	TSRPT_PKT_EN	R/W	This field is to allow the Time Stamp Reporting Packet to IMP port when the time synchronization packet transmitted on egress port.	0

BroadSync HD PCP Value Control Register (Page 90h: Address 03h)

Table 244: BroadSync HD PCP Value Control Register (Page 90h: Address 03h)

BIt	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0
5:3	ClassB_PCP	R/W	BroadSync HD Class B PCP value. This field is used to qualify the PCP value of BroadSync HD packet. This BroadSync HD packet will be sent to Queue4.	3'd4
2:0	ClassA_PCP	R/W	BroadSync HD Class A PCP value. This field is used to qualify the PCP value of BroadSync HD packet. This BroadSync HD packet will be sent to Queue5.	3'd5

BroadSync HD Max Packet Size Register (Page 90h: Address 04h)

Table 245: BroadSync HD Max Packet Size Register (Page 90h: Address 04h)

BIt	Name	R/W	Description	Default
15:12	Reserved	RO	Reserved	0
11:0	MAX_BroadSync HD_PACKET_SIZE	R/W	This field is to define the max packet size of BroadSync HD. The ingress port uses it to qualify if the packet is allowed to pass through a BroadSync HD link. The egress prot uses it to perform shaping gate.	12’d1518

BroadSync HD Time Base Register (Page 90h: Address 10h–13h)

Table 246: BroadSync HD Time Base Register (Page 90h: Address 10h–13h)

BIt	Name	R/W	Description	Default
31:0	TIME BASE	RO	Time Base This is a 32-bit free running clock (running at 25 MHz) for BroadSync HD time base. Ingress port and Egress port use it for Time Synchronization Packet Time Stamp.	0

BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17)

Table 247: BroadSync HD Time Base Adjustment Register (Page 90h: Address 14h–17h)

BIt	Name	R/W	Description	Default
31:12	Reserved	RO	Reserved	0
11:8	TIME ADJUST PERIOD	R/W	Time Adjust Period This field defines the tick numbers to apply the adjusted Time Increment (when Time Increment does not equal to 40). For example, to increment the Time Base for 10 ticks with 41 ns per tick, Time Adjust Period is 10, and Time Increment is 41.	41. 4’h0
7:6	Reserved	RO	Reserved	0
5:0	TIME INCREMENT	R/W	Time Increment This field defines the value to add into Time Base in each 25 MHz tick. Default is 40.	6’d40

BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)

Table 248: BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)

BIt	Name	R/W	Description	Default
31:28	Reserved	RO	Reserved	0
27:16	TICK COUNTER	R/W	Tick Counter This is the tick counter which defines when will Slot Number increment. It runs from 1 to 3125 (or 3124, or 3126, depends on “BroadSync HD Slot Number and Tick Counter Register (Page 90h: Address 18h–1Bh)” on page 270 setting) under 25 MHz.	12’h0
15:5	Reserved	RO	Reserved	0
4:0	SLOT NUMBER	R/W	This field specifies the Slot Number for BroadSync HD.	8’h0

BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)

Table 249: BroadSync HD Slot Adjustment Register (Page 90h: Address 1Ch–1Fh)

BIt	Name	R/W	Description	Default
31:18	Reserved	RO	Reserved	0
17:16	MACRO SLOT PERIOD	R/W	Macro Slot Period This field defines the slot time of a macro slot for Class 4 traffic. 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = Reserved Class 5 traffic slot time is always 125s period.	2’h0
15:12	Reserved	RO	Reserved	0
11:8	SLOT ADJUST PERIOD	R/W	Slot Adjust Period This field defines the number of slots to apply the alterable slot adjustment.	8’h0
7:2	Reserved	RO	Reserved	0
1:0	SLOT ADJUSTMENT	R/W	Slot Adjustment This field defines when the slot number counter increment by 1. Default is 40. 00 = Slot Number increased by 1 when tick counter rolls over 3125. 01 = 3126 10 = 3124 11 = Reserved	2’h0

BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h)

Table 250: BroadSync HD Class 5 Bandwidth Control Register Address Summary

Address	Description
30h–31h	Port 0
32h–33h	Port 1
34h–35h	Port 2
36h–37h	Port 3
38h–39h	Port 4
3Ah-3Bh	Port 5
3Ch–3Dh	Port 6
3Eh-3Fh	Port 7

Table 251: BroadSync HD Class 5 Bandwidth Control Register (Page 90h: Address 30h–31h, 32h–33h, 34h–35h, 36h–37h, 38h–39h)

BIt	Name	R/W	Description	Default
15	C5_WINDOW	R/W	The purpose is to control the credit carry-over under different link speed. For a 100M link, the 125-µs slot is too small such that BroadSync HD packet could easily "slip slot", so the credit carry-over should be allowed. For a 1G link, 125-µs slot is reasonably big such that the BW reservation could be done in a conservative way to prevent "slot slipping", so credit carry-over is not needed.	1'b0
14	Reserved	RO	Reserved	0
13:0	C5_BANDWIDTH	R/W	This field defines the byte count allowed for Class 5 traffic transmission within a slot time.	14'h0

BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h)

Table 252: BroadSync HD Class 4 Bandwidth Control Register Address Summary

Address	Description
60h–61h	Port 0
62h–63h	Port 1
64h–65h	Port 2
66h–67h	Port 3
68h–69h	Port 4
6Ah-6Bh	Port 5
6Ch–6Dh	Port 6
6Eh-6Fh	Port 7

Table 253: BroadSync HD Class 4 Bandwidth Control Register (Page 90h: Address 60h–61h, 62h–63h, 64h–65h, 66h–67h, 68h–69h)

BIt	Name	R/W	Description	Default
15:14	Reserved	RO	Reserved	0
13:0	C4_BANDWIDTH	R/W	This field defines the byte count allowed for Class 4 traffic transmission within a slot time.	14'h0

BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)

Table 254: BroadSync HD Egress Time Stamp Register Address Summary

Address	Description
90h–93h	Port 0
94h–97h	Port 1
98h–9Bh	Port 2
9Ch–9Fh	Port 3
A0h–A3h	Port 4
A4h-A7h	Port 5
A8h–ABh	Port 6
ACh-AFh	Port 7

Table 255: BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h–93h, 94h–97h, 98h–9Bh, 9Ch–9Fh, A0h–A3h, A4h–A7h)

BIt	Name	R/W	Description	Default
31:0	EGRESS_TS	R	Egress Time Synchronous Packet Time Stamp This field reports the time stamp of egress time synchronous packet. It uses 32-bit time base as time stamping. The time between the departure of first byte of MAC DA and the time stamping point should be constant.	32’h0

BroadSync HD Egress Time Stamp Status Register (Page 90h: Address D0h)

Table 256: BroadSync HD Egress Time Stamp Status Register (Page 90h: Address D0h)

BIt	Name	R/W	Description	Default
7:0	VALID STATUS	RO	Valid Status 8-bit field indicating the valid status for each “BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)” on page 273. When “BroadSync HD Egress Time Stamp Register (Page 90h: Address 90h)” is read out by SPI, the valid status will be cleared, respectively.	8’h0

BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)

Table 257: BroadSync HD Link Status Register (Page 90h: Address E0h–E1h)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Reserved	0
8:0	Port BroadSync HD Link Status	R/W	BroadSync HD Link Status When software writes the port BroadSync HD link status and select bit 14 in LED Function Control Register. The BroadSync HD link status is shown on the LED. Bits [8:0] correspond to ports [8:0].	9'h0

Page 91h: Traffic Remarking Register

Table 258: Traffic Remarking Register

Address	Bits	Description
00h–03h	32	"Traffic Remarking Control Register (Page 91h: Address 00h)" on page 274
04h–0Fh	–	Reserved
10h-57h	32	"Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h)" on page 275
58h–EFh	–	Reserved
F0h–F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, bytes 0–7
F8h–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

Traffic Remarking Control Register (Page 91h: Address 00h)

Table 259: Traffic Remarking Control Register (Page 91h: Address 00h)

BIt	Name	R/W	Description	Default
31:25	Reserved	RO	Reserved	0
24:16	PCP_REMARKING_EN	R/W	PCP Remarking Enable Bit 24: IMP port Bits[23:16] correspond to ports [7:0], respectively	0
15:9	Reserved	R/W	Reserved	–
8:0	CFI_REMARKING_EN	R/W	CFI Remarking Enable Bit 8: IMP port Bits[7:0] correspond to ports [7:0], respectively	0

Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h)

Table 260: Egress Non-BroadSync HD Packet TC to PCP Mapping Register Address Summary

Address	Description
10h-17h	Port 0
18h-1Fh	Port 1
20h-27h	Port 2
28h-2Fh	Port 3
30h-37h	Port 4
38h-3Fh	Port 5
40h-47h	Port 6
48h-4Fh	Port 7
50h-57h	IMP

Table 261: Egress Non-BroadSync HD Packet TC to PCP Mapping Register (Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h-57h)

Bit	Name	R/W	Description	Default
63:32	Reserved	R/W	Reserved	4'b1111
31:28	{CFI,PCP} for TC = 7	R/W	The {CFI,PCP} field for TC = 7	4'b0111
27:24	{CFI,PCP} for TC = 6	R/W	The {CFI,PCP} field for TC = 6	4'b0110
23:20	{CFI,PCP} for TC = 5	R/W	The {CFI,PCP} field for TC = 5	4'b0101
19:16	{CFI,PCP} for TC = 4	R/W	The {CFI,PCP} field for TC = 4	4'b0100
15:12	{CFI,PCP} for TC = 3	R/W	The {CFI,PCP} field for TC = 3	4'b0011
11:8	{CFI,PCP} for TC = 2	R/W	The {CFI,PCP} field for TC = 2	4'b0010
7:4	{CFI,PCP} for TC = 1	R/W	The {CFI,PCP} field for TC = 1	4'b0001
3:0	{CFI,PCP} for TC = 0	R/W	The {CFI,PCP} field for TC = 0	4'b0000

Global Registers

Table 262: Global Registers (Maps to All Pages)

Address	Bits	Description
F0h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 0
F1h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 1
F2h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 2
F3h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 3
F4h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 4
F5h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 5
F6h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 6
F7h	8	"SPI Data I/O Register (Global, Address F0h)" on page 276, 7
F8–FDh	–	Reserved
FEh	8	"SPI Status Register (Global, Address FEh)" on page 276
FFh	8	"Page Register (Global, Address FFh)" on page 277

SPI Data I/O Register (Global, Address F0h)

Table 263: SPI Data I/O Register (Maps to All Registers, Address F0h–F7h)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes [7:0]	0

SPI Status Register (Global, Address FEh)

Table 264: SPI Status Register (Maps to All Registers, Address FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI read/write complete flag	0
6	Reserved	RO	–	0
5	RACK	RO (SC)	SPI read data ready acknowledgement (self-clearing)	0
4:2	Reserved	RO	–	0
1	Reserved	RO	–	0
0	Reserved	RO	–	0

Page Register (Global, Address FFh)

Table 265: Page Register (Maps to All Registers, Address FFh)

Bit	*Name*	*R/W*	*Description*	*Default*
7:0	PAGE_REG	R/W	The binary value determines the value of the accessed register page.	0

Section 8: Electrical Characteristics

Absolute Maximum Ratings

Table 266: Absolute Maximum Ratings

Symbol	*Parameter and Pins*	*Minimum*	*Maximum*	*Units*
–	Supply voltage: PLL_AVDD, DVDD, AVDDL	GND−0.3	1.32	V
–	Supply voltage: OVDD2, AVDDH, OVDD, XTAL_AVDD	GND–0.3	3.63	V
I_I	Input current	–	–	mA
T_{STG}	Storage temperature	–40	+125	°C
V_{ESD}	Electrostatic discharge	–	2000	V
–	Input voltage: digital input pins	–	–	V

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Recommended Operating Conditions

Table 267: Recommended Operating Conditions

Symbol	*Parameter*	*Pins*	*Minimum*	*Maximum*	*Units*
VDD	Supply voltage	AVDDL, DVDD, PLL_AVDD	1.14	1.26	V
		OVDD2, AVDD, XTAL_AVDD	3.14	3.47	V
		OVDD (RGMII mode)	2.38	2.63	V
		OVDD (GMII/RvMII mode)	3.14	3.47	V
V_{IH}	High-level input voltage	All digital inputs	2.0	–	V
V_{IL}	Low-level input voltage	All digital inputs	–	0.8	V
T_A	Ambient operating temperature	–	0	70	°C

Electrical Characteristics

Table 268: Electrical Characteristics

Symbol	*Parameter*	*Pins*	*Conditions*	*Minimum*	*Typical*	*Maximum*	*Units*
I_{DD}	Maximum supply current (for GMII/RvMII/MII operation)	1.2V power rail	–	–	1153	–	mA
		3.3V power rail	–	–	610	–	mA
		OVDD (3.3V for GMII/RvMII/MII)	–	–	27	–	mA
I_{DD}	Maximum supply current (for RGMII operation)	1.2V power rail	–	–	1153	–	mA
		3.3V power rail	–	–	610	–	mA
		OVDD (2.5V for RGMII)	–	–	28	–	mA
V_{OH}*	High-level output voltage	Digital output pins	I_{OH} = –8 mA I_{OH} = –16 mA	2.4	–	–	V
V_{OL}	Low-level output voltage	Digital output pins	I_{OL} = +8 mA I_{OL} = +16 mA	–	–	0.4	V
V_{IH}	High-level input voltage	Digital input pins	–	2.0	–	–	V
		XTALI	–	2.0	–	–	V
V_{IL}	Low-level input voltage	Digital input pins	–	–0.3	–	0.8	V
		XTALI	–	–0.3	–	0.8	V
I_I	Input current	Digital inputs w/ pull-up resistors	V_I = OVDD2	–	–	+100	µA
		Digital inputs w/ pull-up resistors	V_I = GND	–	–	–10	µA
		Digital inputs w/ pull-down resistors	V_I = OVDD2	–	–	+100	µA
		Digital inputs w/ pull-down resistors	V_I = GND	–	–	+10	µA
		All other digital inputs	GND ≤ V_I ≤ OVDD2	–	–	±100	µA

Note: For RGMII digital output pins, VOH minimum is 2.0V.

Section 9: Timing Characteristics

Reset and Clock Timing

Figure 49: Reset and Clock Timing

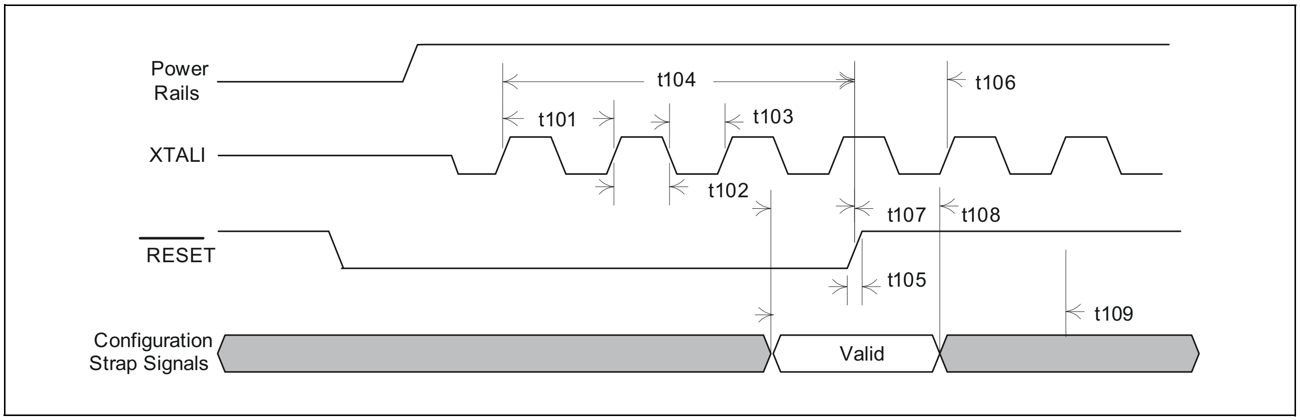


Table 269: Reset and Clock Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
XTALI period	t101	39.998 ns	40 ns	40.002 ns
XTALI high time	t102	18 ns	–	22 ns
XTALI low time	t103	18 ns	–	22 ns
RESET low pulse duration	t104	20 ms	80 ms	–
RESET rise time	t105	–	–	25 ns
Configuration valid setup to RESET rising	t107	100 ns	–	–
Configuration valid hold from RESET rising	t108	–	–	0 ns
Hardware initialization is complete. All the strap pin values are clocked in, and the internal registers can be accessed.	t109	5 ms before the registers can be accessed		

MII Interface Timing

The following specifies timing information regarding the MII Interface pins.

MII Input Timing

Figure 50: MII Input

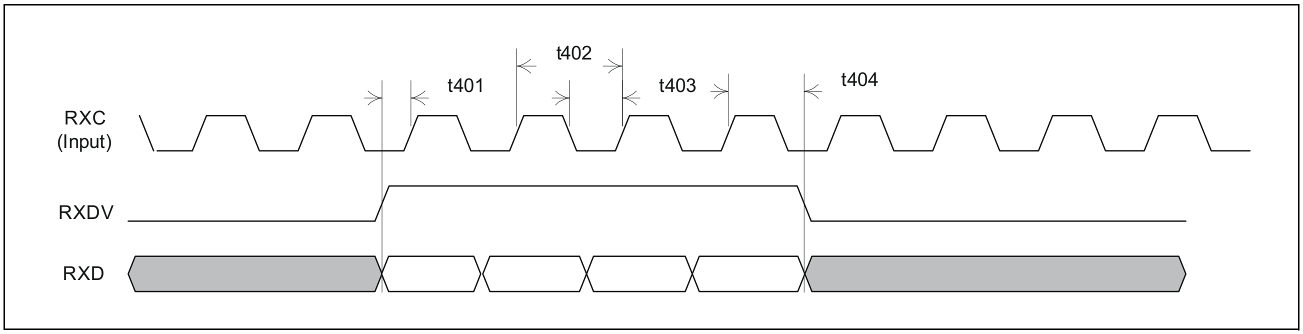


Table 270: MII Input Timing

Parameter	***Description***	***Min***	***Typ***	***Max***
t401	RXDV, RXD, to RXC rising setup time	10 ns	–	–
t402	RXC clock period (10BASE-T mode)	–	400 ns	–
	RXC clock period (100BASE-TX mode)	–	40 ns	–
t403	RXC high/low time (10BASE-T mode)	160 ns	–	240 ns
	RXC high/low time (100BASE-TX mode)	16 ns	–	24 ns
t404	RXDV, RXD, to RXC rising hold time	10 ns	–	–
–	Duty cycle	–	–	–

MII Output Timing

Figure 51: MII Output Timing

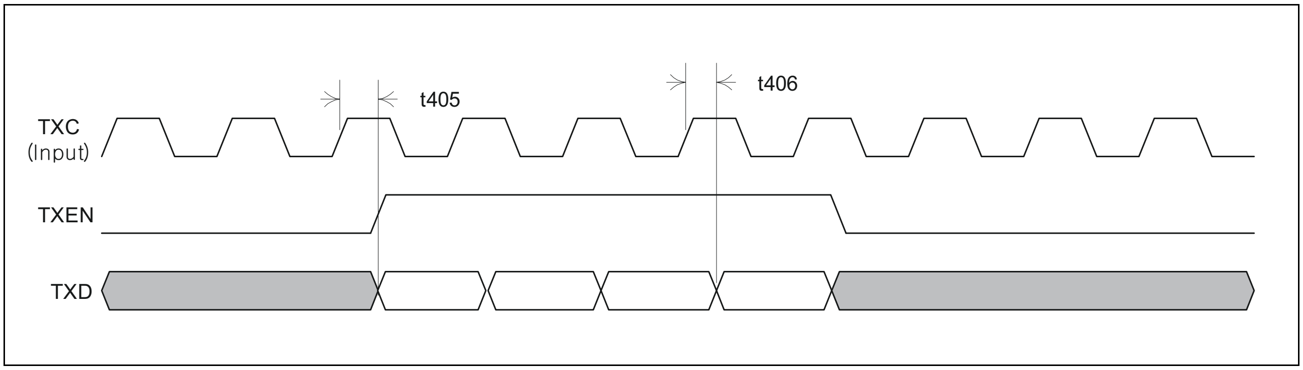


Table 271: MII Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t405	TXC high to TXEN, TXD valid	0 ns	–	25 ns
t406	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

TMII Interface Timing

The following specifies timing information regarding the TMII Interface pins.

TMII Input Timing

Figure 52: TMII Input

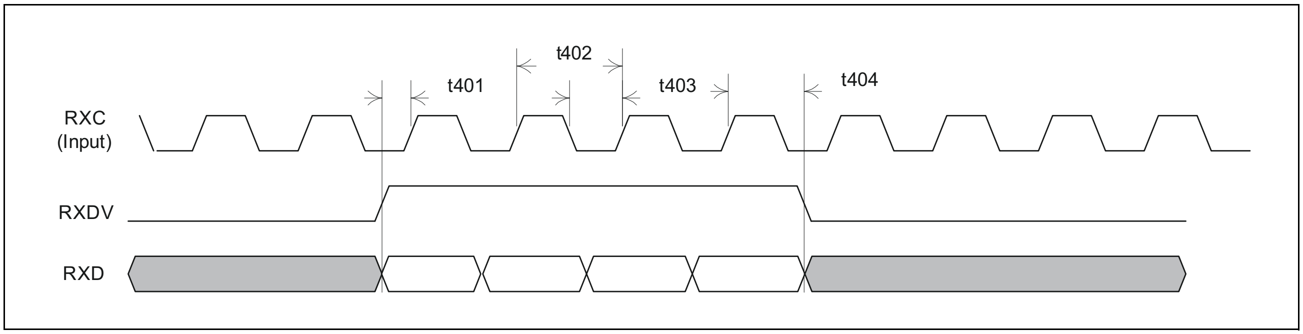


Table 272: TMII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t401	RXDV, RXD, to RXC rising setup time	5 ns	–	–
t402	RXC clock period (100BASE-TX mode)	–	20 ns	–
t403	RXC high/low time (100BASE-TX mode)	8 ns	–	12 ns
t404	RXDV, RXD, to RXC rising hold time	5 ns	–	–
–	Duty cycle	–	–	–

TMII Output Timing

Figure 53: TMII Output Timing

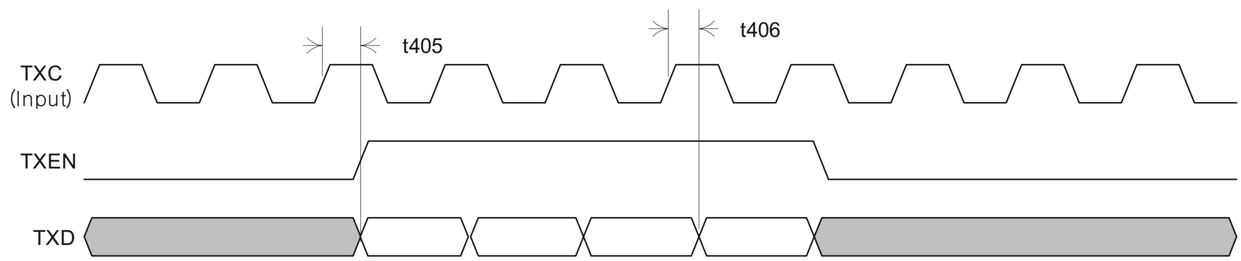


Table 273: TMII Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t405	TXC high to TXEN, TXD valid	0 ns	–	12.5 ns
t406	TXC high to TXEN, TXD invalid (hold)	0 ns	–	–

Reverse MII Interface Timing

The following specifies timing information regarding the Reverse MII Interface pins.

Reverse MII Input Timing

Figure 54: Reverse MII Input Timing

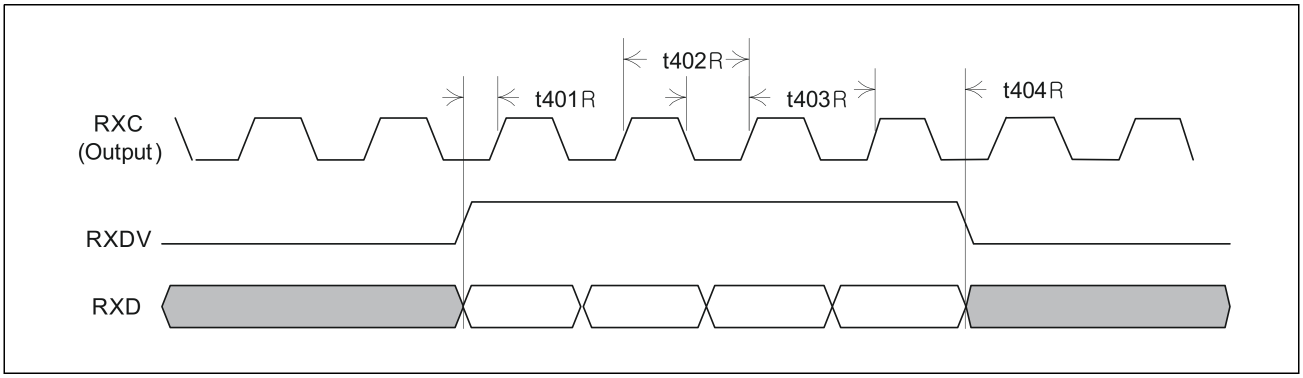


Table 274: Reverse MII Input Timing

Description	*Parameter*	*Min*	*Typ*	*Max*	*Units*
RXDV, RXD to RXC rising setup time	t401R	10	–	–	ns
RXC (output) clock period (10BASE-T mode)	t402R	–	400	–	ns
RXC clock period (100BASE-TX mode)		–	40	–	ns
RXC high/low time (10BASE-T mode)	t403R	160	–	240	ns
RXC high/low time (100BASE-TX mode)		16	–	24	ns
RXDV, RXD to RXC rising hold time	t404R	0	–	–	ns

Reverse MII Output Timing

Figure 55: Reverse MII Output Timing

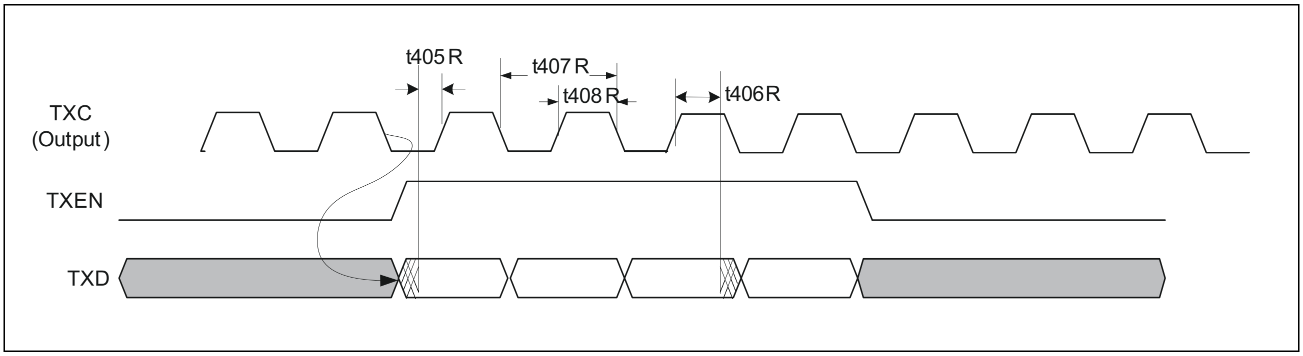


Table 275: Reverse MII Output Timing

Description	Parameter	Min	Typ	Max	Units
Output (TXD, TX_EN) setup to TXC rising	t405R	15	–	25	ns
Output (TXD, TX_EN) hold from TXC rising	t406R	11	–	–	ns
TXC clock period	t407R	–	40	–	ns
TXC high/low time	t408R	15	–	22	ns

RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

RGMII Output Timing (Normal Mode)

Figure 56: RGMII Output Timing (Normal Mode)

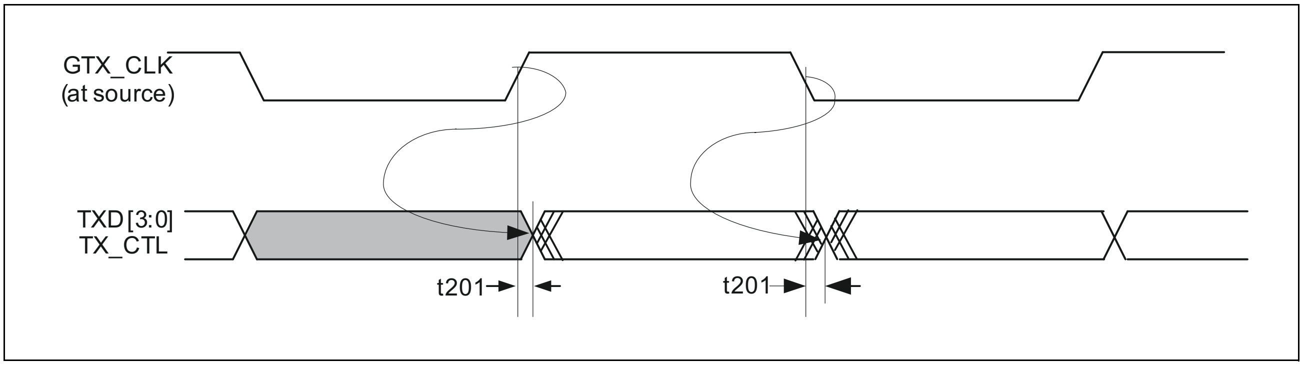


Table 276: RGMII Output Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
GTX_CLK clock period (1000M mode)	–	7.2	8	8.8	ns
GTX_CLK clock period (100M mode)	–	36	40	44	ns
GTX_CLK clock period (10M mode)	–	360	400	440	ns
TskewT: data to clock output skew	t201	–500 (1000M)	0	+500 (1000M)	ps
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

Note: The output timing in 10/100M operation is always as specified in the delayed mode.

RGMII Output Timing (Delayed Mode)

RGMII output timing defaults to the delayed mode when the TXC_DELAY pin is pulled high at power-on reset.

Figure 57: RGMII Output Timing (Delayed Mode)

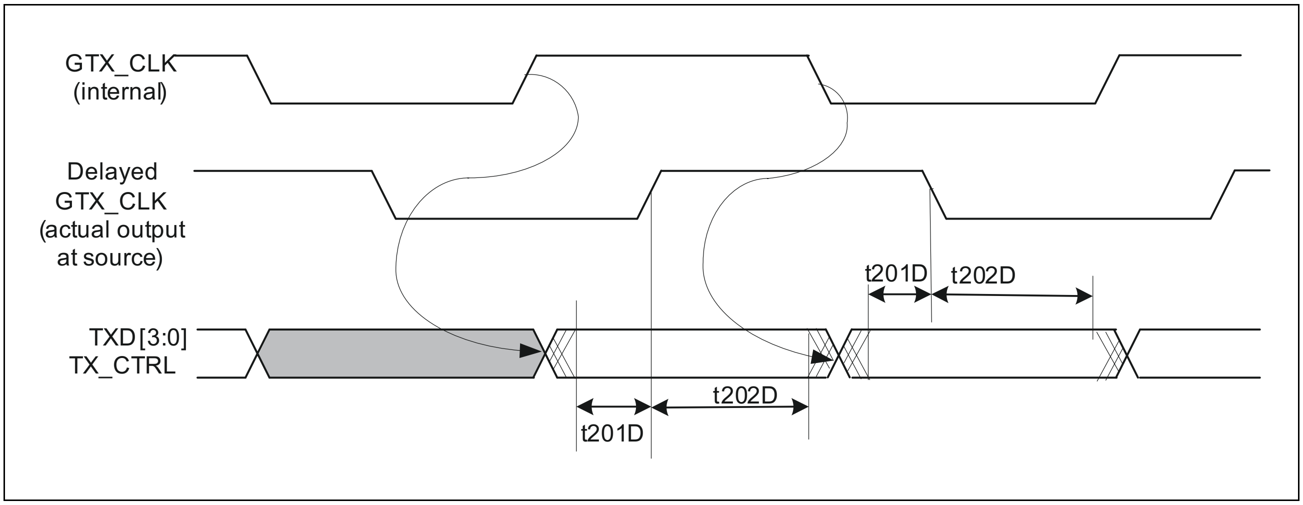


Table 277: RGMII Output Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTX_CLK clock period (1000M mode)	–	7.2	8	8.8	ns
GTX_CLK clock period (100M mode)	–	36	40	44	ns
GTX_CLK clock period (10M mode)	–	360	400	440	ns
TsetupT Data valid to clock transition: Available setup time at the output source (delayed mode)	t201D	1.2 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (delayed mode)	t202D	1.2	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Normal Mode)

Figure 58: RGMII Input Timing (Normal Mode)

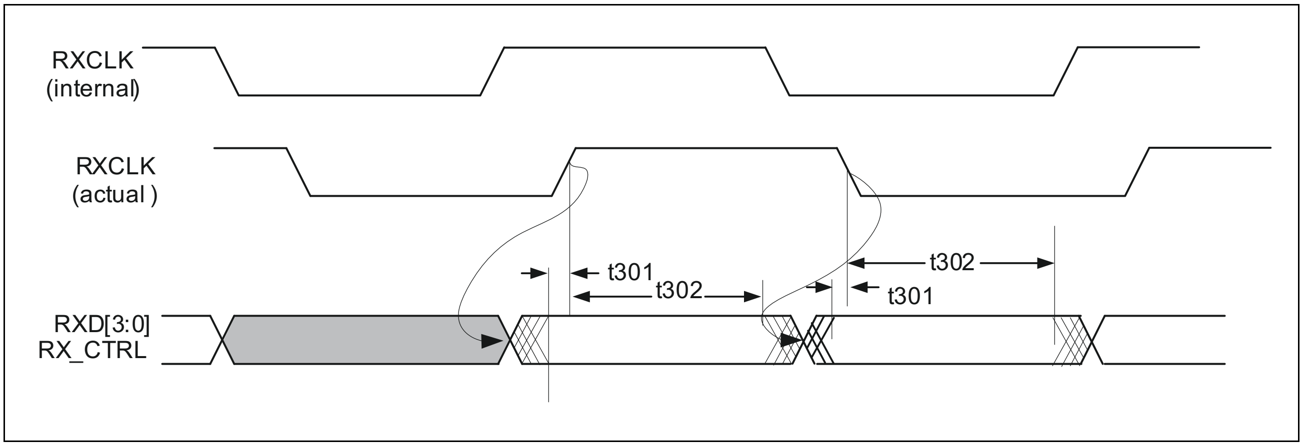


Table 278: RGMII Input Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
RXCLK clock period (1000M mode)	–	7.2	8	8.8	ns
RXCLK clock period (100M mode)	–	36	40	44	ns
RXCLK clock period (10M mode)	–	360	400	440	ns
TsetupR Input setup time: valid data to clock	t301	1.0	2.0	–	ns
TholdR Input hold time: clock to valid data	t302	1.0	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

RGMII Input Timing (Delayed Mode)

RGMII Input Timing defaults to the delayed mode when the RXC_DELAY pin is pulled high at power-on reset.

Figure 59: RGMII Input Timing (Delayed Mode)

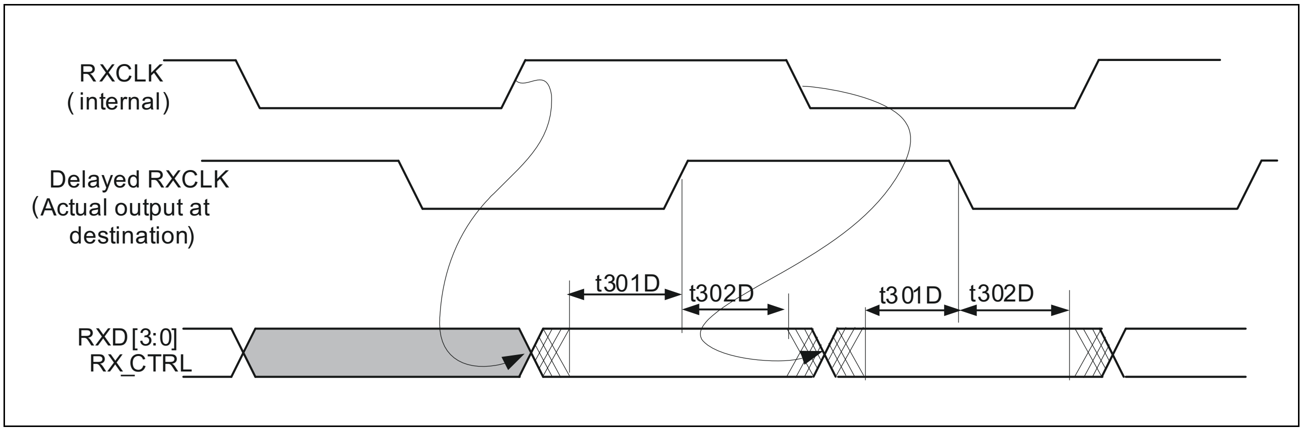


Table 279: RGMII Input Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
TsetupR Input setup time (delayed mode)	t301D	–1.0 (1000M)	–	–	ns
		–1.0 (10/100M)	–	–	ns
TholdR Input hold time (delayed mode)	t302D	3.0 (1000M)	–	–	ns
		9.0 (10/100M)	–	–	ns

GMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in GMII mode.

GMII Interface Output Timing

Figure 60: GMII Output Timings

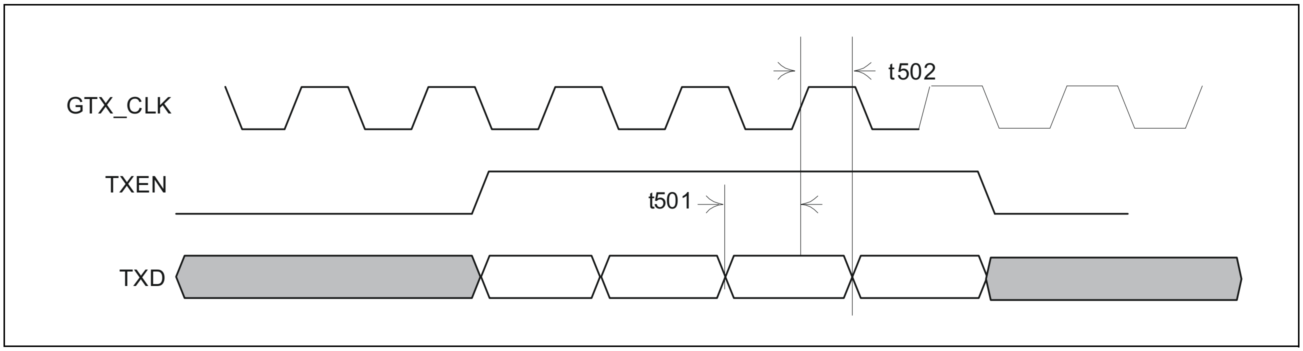


Table 280: GMII Output Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTX_CLK clock period (1000M mode)	–	7.5	8	8.5	ns
Output (TXD, TX_EN) setup to GTX_CLK rising	t501	2.5	–	–	ns
Output (TXD, TX_EN) hold from GTX_CLK rising	t502	0.5	–	5.5	ns

GMII Interface Input Timing

Figure 61: GMII Input Timings

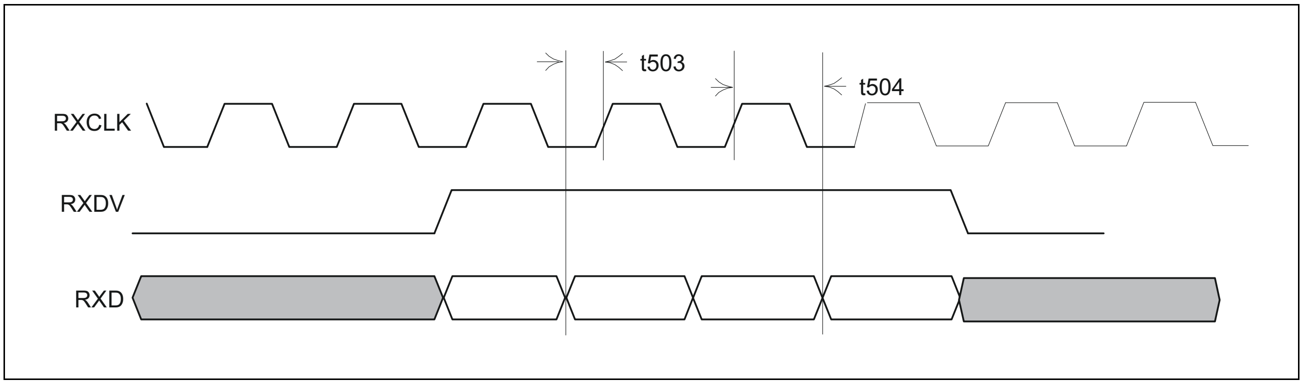


Table 281: GMII Input Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXCLK clock period (1000M mode)	–	–	8	–	ns
(RXD, RX_DV) Setup to RX_CLK rising	t503	2.0	–	–	ns
(RXD, RX_DV) Hold from RX_CLK rising	t504	0.0	–	–	ns

MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.

Figure 62: MDC/MDIO Timing (Slave Mode)

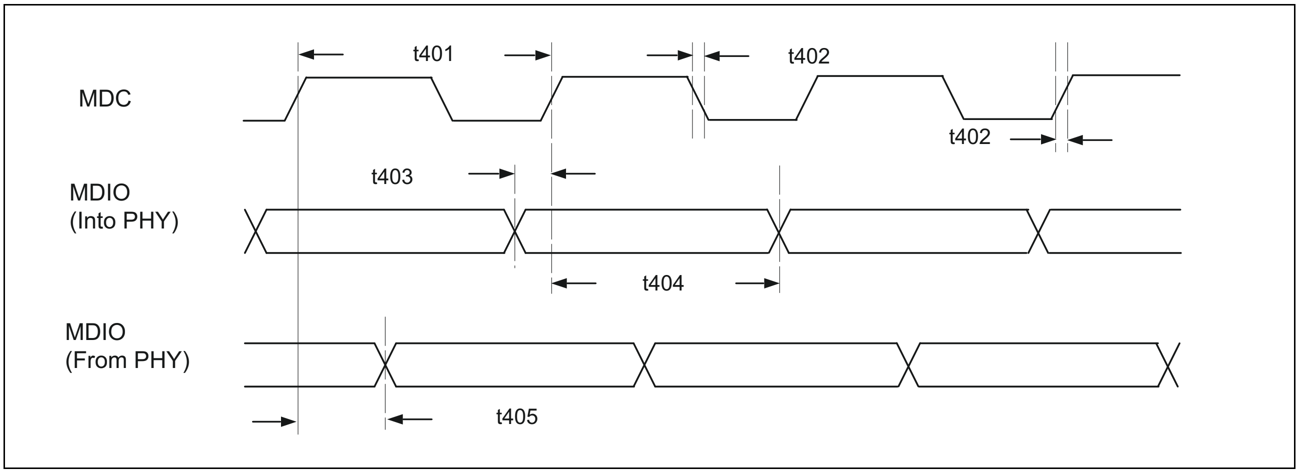


Table 282: MDC/MDIO Timing (Slave Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	t401	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	7.5	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC rising	t405	0	–	45	ns

Table 283: MDC/MDIO Timing (Master Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	t401	400	–	–	ns
MDC high/low	–	160	–	240	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	20	–	–	ns
MDIO input hold time from MDC rising	t404	0	–	–	ns
MDIO output delay from MDC rising	t405	15	–	90	ns

Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

Figure 63: Serial LED Interface Timing

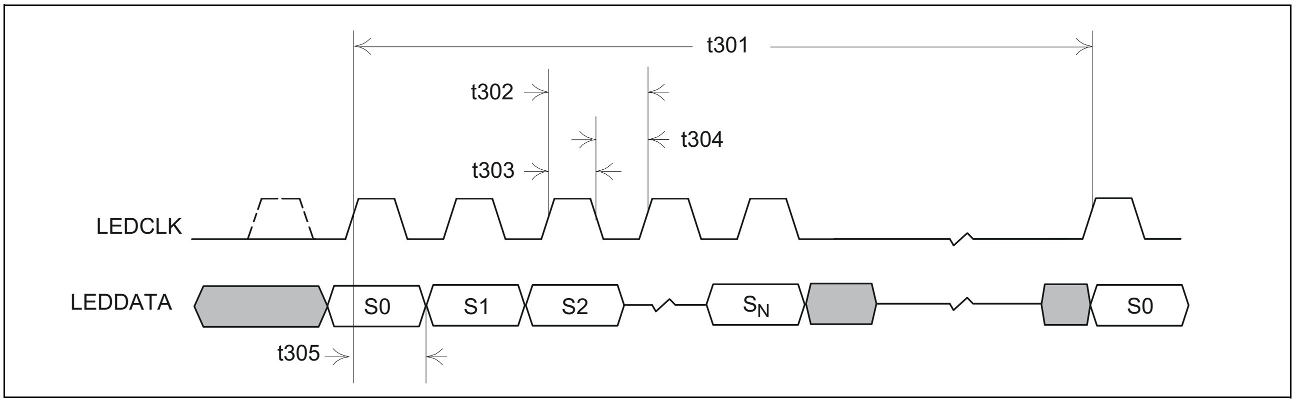


Table 284: Serial LED Interface Timing

Description	Parameter	Minimum	Typical	Maximum	Unit
LED update cycle period	t301	–	42	–	ms
LEDCLK period	t302	–	320	–	ns
LEDCLK high-pulse width	t303	150	–	170	ns
LEDCLK low-pulse width	t304	150	–	170	ns
LEDCLK to LEDDATA output time	t305	140	–	180	ns

SPI Timings

Figure 64: SPI Timings, $\overline{SS}$ Asserted During SCK High

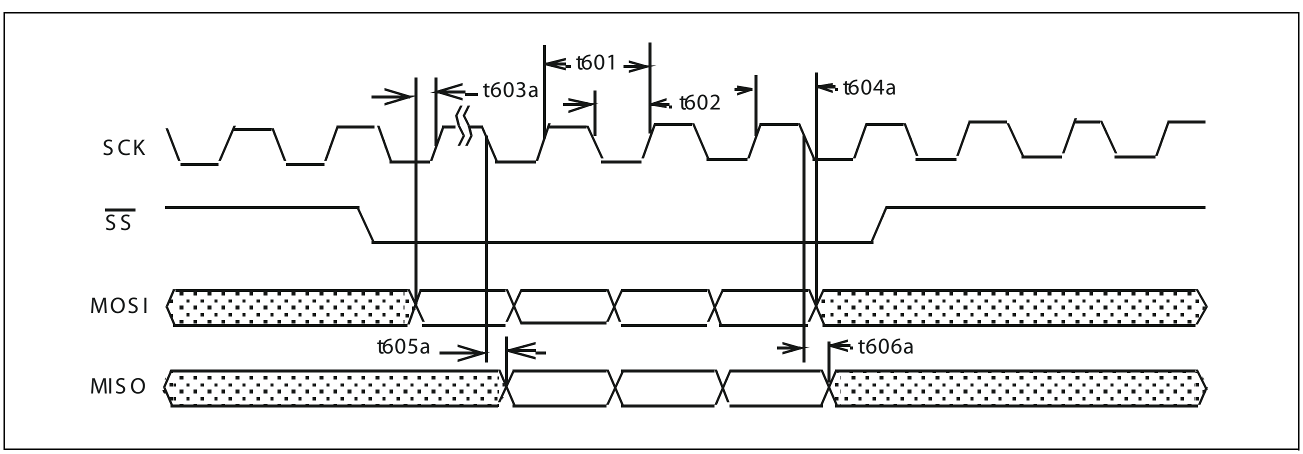


Figure 65: SPI Timings, $\overline{SS}$ Asserted During SCK Low

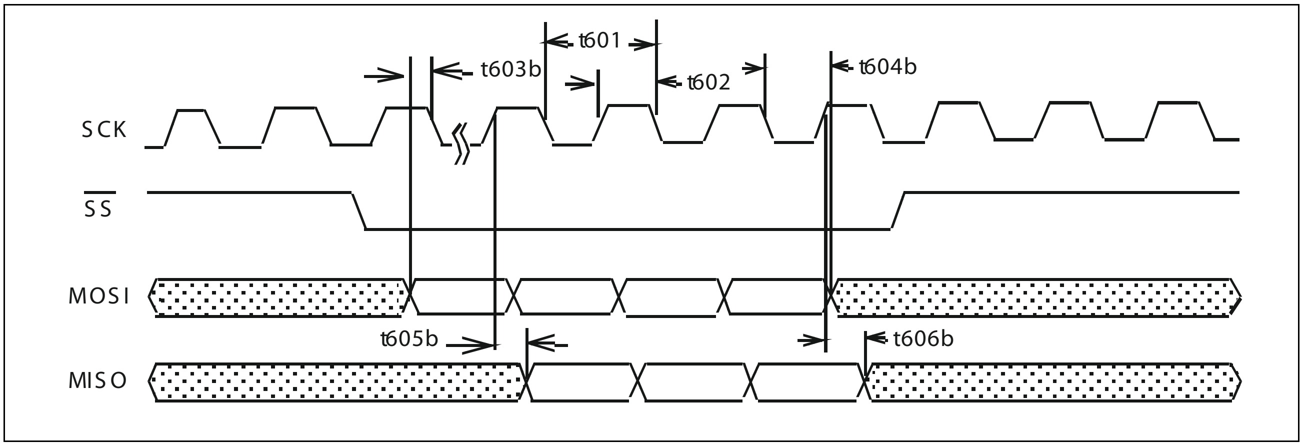


Table 285: SPI Timings

Description	Parameter	Minimum	Typical	Maximum
SCK clock period	t601	–	500 ns	–
SCK high/low time	t602	200 ns	–	300 ns
MOSI to SCK setup time	t603a, t603b	5 ns	–	–
MOSI to SCK hold time	t604a, t604b	12 ns	–	–
SCK to MISO valid	t605a, t605b	–	–	25 ns
SCK to MISO invalid	t606a, t606b	0 ns	–	–

Note: BCM53118 behaves only as slave devices. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the BCM53118 samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM53118 samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM Timing

Figure 66: EEPROM Timing

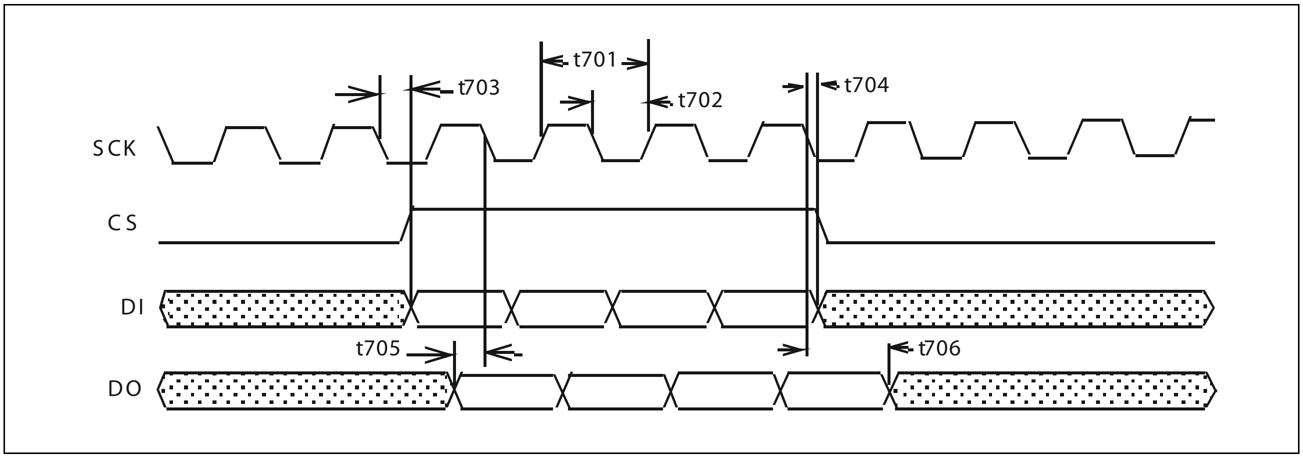


Table 286: EEPROM Timing

Description	***Parameter***	***Minimum***	***Typical***	***Maximum***
SCK clock frequency	t701	–	100 kHz	–
SCK high/low time	t702	–	5 µs	–
SCK low to CS, DI valid	t703	–	–	500 ns
SCK low to CS, DI invalid	t704	500 ns	–	–
DO to SCK falling setup time	t705	200 ns	–	–
DO to SCK falling hold time	t706	200 ns	–	–

Serial Flash Timing

Figure 67: Serial FlashTiming

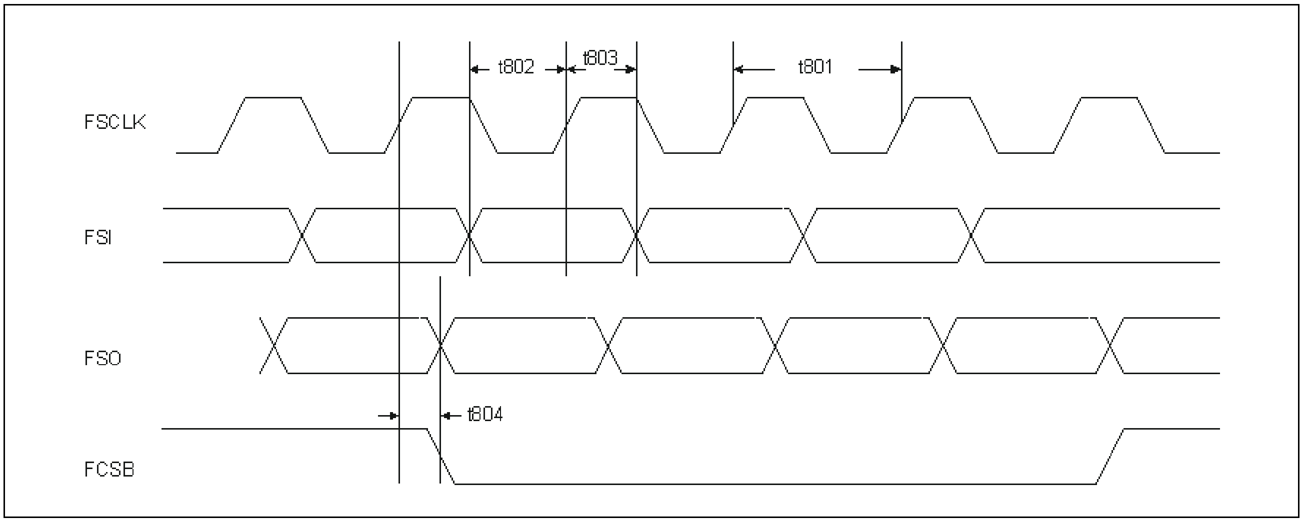


Table 287: Serial FlashTiming

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
FSCLK clock frequency	t801	–	11.4 MHz	–
FSI to FSCLK rising setup time	t802	11.6 ns	–	–
FSI to FSCLK rising hold time	t803	0 ns	–	–
FSCLK to FSO, FCSB delay	t804	5 ns	–	15.6 ns
Note: FSCLK clock is system clock divides eight, 11.4 MHz is at normal operation.				

Section 10: Thermal Characteristics

Note: The maximum allowed junction temperature is 125 ºC. Table 288 and Table 289 show the estimated junction temperature with heat sink.

Table 288: BCM53118KQLE Package with Heat Sink, 4-Layer Board, P = 3.8W

Device power dissipation, P (W)		3.8				
Ambient air temperature Ta (ºC)		70				
θ_{JA} is still air (ºC/W)		12.37				
θ_{JB} (ºC/W)		0.69				
θ_{JC} (ºC/W)		8.51				
External heat sink		Heat sink: 35 mm x 35 mm x 20 mm, k = 180 (W/m*k), aluminum blade-fin. Thermal interface: 28 mm x 28 mm x 0.37 mm, k = 1.3 (W/m*k)				
Package Thermal Performance Data						
Air Velocity		***TJ_max***	***TC_max***	ϑ_{JA}	Ψ_{JT}	Ψ_{JB}
m/s	***ft/min***	***(ºC)***	***(ºC)***	***(ºC/W)***	***(ºC/W)***	***(ºC/W)***
0	0	117.02	102.73	12.37	3.76	5.92
0.508	100	105.62	90.69	9.37	3.93	5.64
1.016	200	102.57	87.495	8.57	3.97	5.57
2.032	300	100.9	85.81	8.13	3.97	5.57
3.048	400	100.14	85.061	7.93	3.97	5.58

Table 289: BCM53118KQLE Package with Heat Sink, 2-Layer Board, P = 3.8W

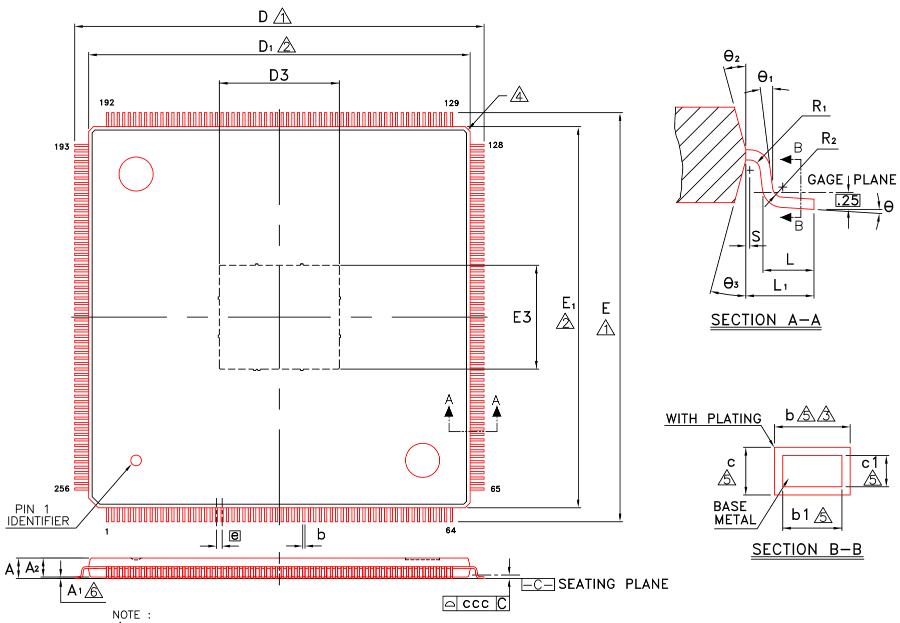
Device power dissipation, P (W)	3.8
Ambient air temperature Ta (ºC)	70
θ_{JA} is still air (ºC/W)	16.23
θ_{JB} (ºC/W)	0.69
θ_{JC} (ºC/W)	8.51
External heat sink	Heat sink: 35 mm x 35 mm x 20 mm, k = 180 (W/m*k), aluminum blade-fin. Thermal interface: 28 mm x 28 mm x 0.37 mm, k = 1.3 (W/m*k)

Package Thermal Performance Data

Air Velocity		***TJ_max***	***TC_max***	ϑ_{JA}	Ψ_{JT}	Ψ_{JB}
m/s	***ft/min***	***(ºC)***	***(ºC)***	***(ºC/W)***	***(ºC/W)***	***(ºC/W)***
0	0	131.67	111.25	16.23	5.37	9.33
0.508	100	117.14	96.51	12.41	5.43	8.77
1.016	200	113.56	92.87	11.46	5.44	8.73
2.032	300	111.53	90.81	10.93	5.45	8.61
3.048	400	110.79	90.02	10.73	5.47	8.58

Section 11: Mechanical Information

Figure 68: BCM53118 Mechanical Specifications



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D_1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E_1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	7° REF			7° REF		
θ_2	12° REF			12° REF		
θ_3	12° REF			12° REF		
ccc	0.08			0.003		

Exposed Pad Size			
L/F		Dimension in mm	Dimension in inch
①	D3/E3	8.79/7.62 REF	0.346/0.300 REF

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Section 12: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM53118KQLE(G)	256 eLQFP	0°C to 70°C

Note: (G) represents the lead-free package option.

Connecting everything®

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