

ACPL-0873T

Automotive 3-Channel Digital Filter for Sigma-Delta Modulators

Description

The Broadcom® ACPL-0873T is a 3-channel digital filter designed specifically for Second Order Sigma Delta Modulators in voltage and current sensing. Each input channel can receive an independent Sigma-Delta ($\Sigma\text{-}\Delta$) modulator bit stream. The bit streams are processed by three individual digital decimation filters. Features of the digital filter include four decimation ratios for Sinc² mode and three decimation ratios for Sinc³ mode, offset calibration, and fast over-range detection. Synchronization of inputs from three channels is done internally by the filter alignment.

The ACPL-0873T outputs an over-range signal for three channels, signaling over-voltage/current conditions. Programmable through SPI compatible interface, ACPL-0873T can directly connect to a microcontroller to output 16 bits digital filter data and write/read filter registers.

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Direct interface between Isolated Sigma-Delta Modulator (ACPL-C797T/C799T) and MCU/DSP
- Three individual digital filters
- Synchronizing sampling time
- Fast over-range detection
- Offset calibration
- Channel 1 MCLK clock detection at power up
- Programmable input configuration
- SPI-compatible interface
- Compact surface-mount QFN-20 5 mm × 5 mm

Specifications

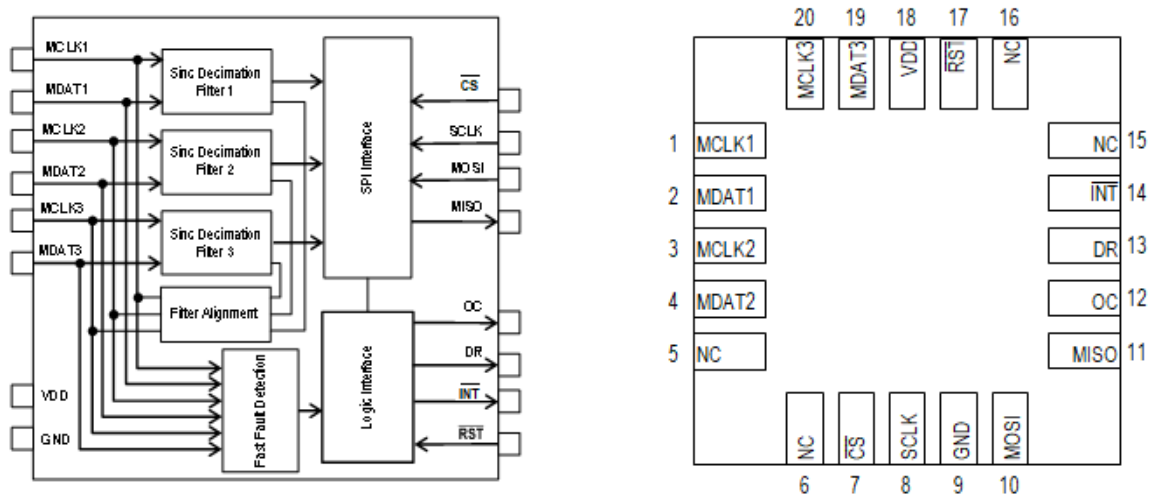
- Operating temperature –40°C to 125°C
- SPI clock frequency up to 17 MHz
- Modulator clock frequency up to 25 MHz

Applications

- Automotive electric motor phase and rail current sensing
- Automotive DC/DC converter current sensing
- Automotive AC-DC charger current sensing
- Automotive battery current sensing
- General voltage or current sensing

Schematic Diagram and Package Pin Out

Figure 1: Schematic Diagram and Package Pin Out



NOTE: 0.1-μF and 1-μF bypass capacitors between VDD and GND are recommended.

Table 1: Pin Function Description

Pin No.	Pin Name	Description	Type
1	MCLK1	Channel 1 Clock.	Input
2	MDAT1	Channel 1 Data. Input Data on MDAT1 is clocked in on the rising edge of MCLK1.	Input
3	MCLK2	Channel 2 Clock.	Input
4	MDAT2	Channel 2 Data. Input Data on MDAT2 is clocked in on the rising edge of MCLK2.	Input
5	NC	Not connected.	
6	NC	Not connected.	
7	\overline{CS}	Chip Select, Active Low of Chip Select for SPI interface and digital filter conversion start on the falling edge of CS.	Input
8	SCLK	SPI Clock input.	Input
9	GND	Ground.	Power Input
10	MOSI	SPI data Master Out Slave In.	Input
11	MISO	SPI data Master In Slave Out.	Output
12	OC	Over-range Condition.	Output
13	DR	Data Ready. 1. DR pin High indicates Digital Filter data conversion ready. 2. DR pin is automatically cleared to Low when \overline{CS} goes high.	Output
14	\overline{INT}	Interrupt, Active Low.	Output
15	NC	Not connected.	
16	NC	Not connected.	
17	\overline{RST}	Reset. Active Low, period 100 μs at least.	Input
18	VDD	Power Supply.	Power Input
19	MDAT3	Channel 3 Data. Input Data on MDAT3 is clocked in on the rising edge of MCLK3.	Input
20	MCLK3	Channel 3 Clock.	Input

Figure 2: ACPL-0873T Package Outline Drawing

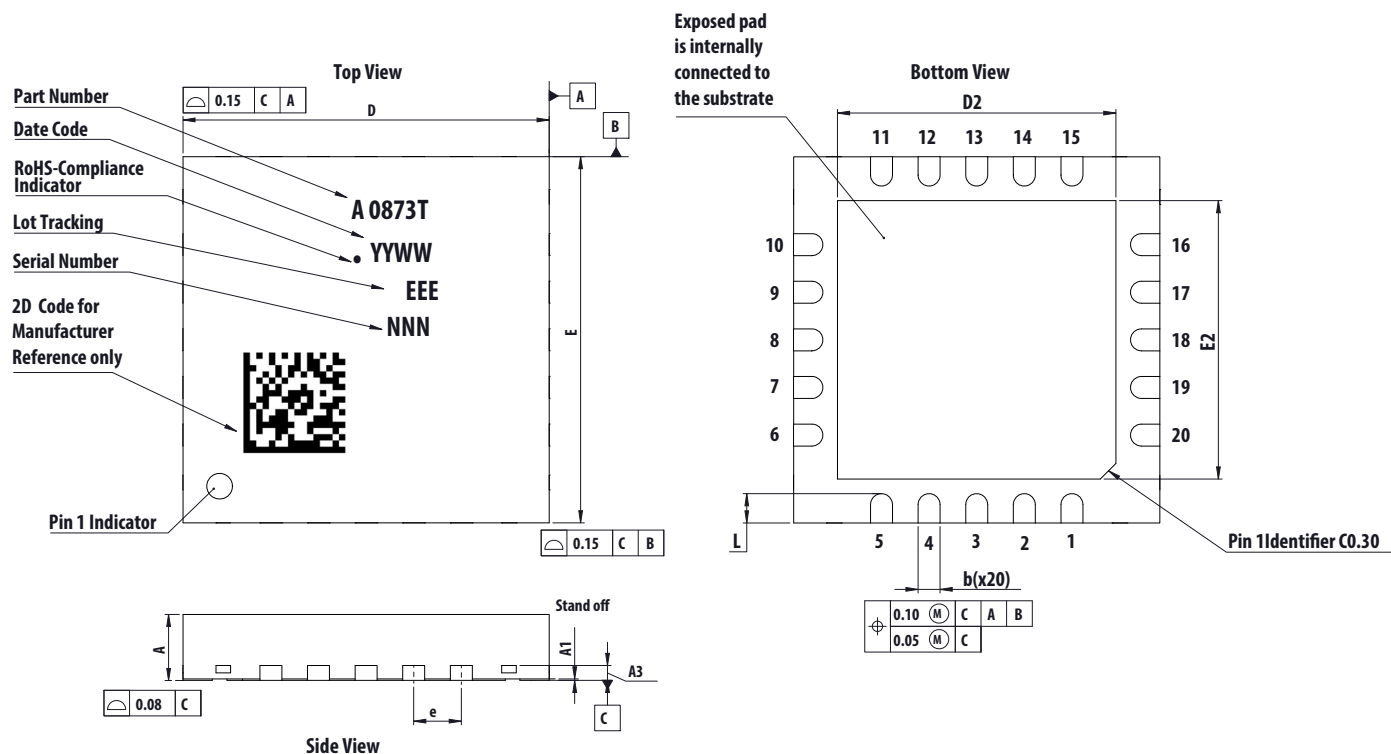
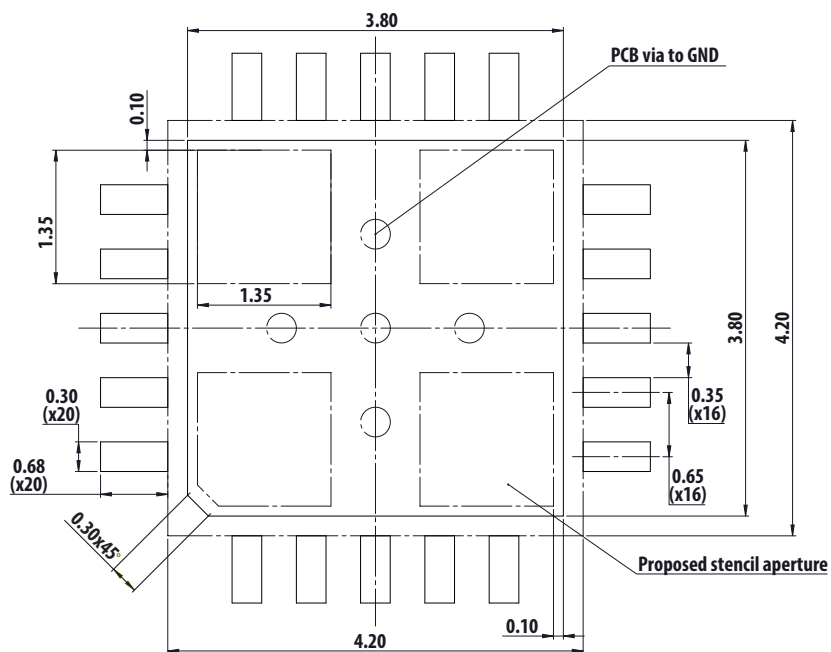


Figure 3: Recommended Land Pattern



NOTE: Connect all NC pins to GND.

Table 2: Dimensions

	Dimensions					
	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.850	0.900	0.950	0.033	0.035	0.037
A1	0.000	0.020	0.040	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.250	0.300	0.350	0.010	0.012	0.014
D	4.850	5.000	5.150	0.191	0.197	0.203
E	4.850	5.000	5.150	0.191	0.197	0.203
D2	3.700	3.800	3.900	0.146	0.150	0.154
E2	3.700	3.800	3.900	0.146	0.150	0.154
e	0.650 REF			0.026 REF		
L	0.350	0.400	0.450	0.014	0.016	0.018

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	Quantity
ACPL-0873T	-500E	QFN-20	X	X	2000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example:

ACPL-0873T-500E to order product of QFN-20 Surface Mount package in Tape and Reel packaging with RoHS compliant. Contact your Broadcom sales representative or authorized distributor for information.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Junction Temperature	T_J	-55	150	°C	
Ambient Operating Temperature	T_A	-40	125	°C	
Supply Voltage	V_{DD}	-0.5	6	Volts	
Input Voltage	All Inputs	-0.5	$V_{DD} + 0.5$	Volts	a
Output Voltage	All Outputs	-0.5	$V_{DD} + 0.5$	Volts	a

a. Do not exceed 6V.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Figure	Notes
Ambient Operating Temperature	T_A	-40	125	°C		
Supply Voltage	V_{DD}	3	5.5	Volts		
Input / Output Voltage		0	V_{DD}	Volts		

DC Electrical Specifications

All minimum/maximum specifications are at recommended operating conditions. Unless otherwise noted, all typical values at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Power Supply Current	I_{DD1}	—	3.6	8	mA	3 channels $f_{MCLK} = 20\text{ MHz}$, SPI $f_{SCLK} = 17\text{ MHz}$	7	
	I_{DD2}	—	3	6.5		3 channels $f_{MCLK} = 20\text{ MHz}$, no SPI clock		
Quiescent Power Supply Current	I_{DDQ}	—	—	1	μA	All 3 channels MCLK and MDAT short to GND, no SPI clock		
Input Voltage High Level	V_{IH}	$0.7 \times V_{DD}$	—	—	Volts			
Input Voltage Low Level	V_{IL}	—	—	$0.3 \times V_{DD}$	Volts			
DC Input Current	I_{IN}	—	—	10	μA			
Output Voltage High	V_{OH}	$0.8 \times V_{DD}$	—	—	V	$I_{OH} = 4\text{ mA}$		
Output Voltage Low	V_{OL}	—	—	0.4	V	$I_{OL} = 4\text{ mA}$		

Switching Specifications

All minimum/maximum specifications are at recommended operating conditions. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{DD}) and timed at 50% voltage level. Unless otherwise noted, all typical values at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Modulator Clock Frequency	f_{MCLK}	—	—	25	MHz			
Modulator Clock Duty Cycle	DC_{MCLK}	40	—	70	%			
MDAT Setup Time before MCLK Rising Edge	t_{MDAT_S}	10	—	—	ns		4	
MDAT Hold Time after MCLK Rising Edge	t_{MDAT_H}	3	—	—	ns		4	
SPI Clock Frequency	f_{SCLK}	—	—	17	MHz	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$		
		—	—	13		$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$		
SPI Clock Duty Cycle	DC_{SCLK}	40	—	60	%			
SPI MOSI Setup Time	t_{MOSI_S}	3	—	—	ns		5	
SPI MOSI Hold Time	t_{MOSI_H}	3	—	—	ns		5	
SPI Clock Falling Edge to MISO Valid	t_{MISO_V}	—	—	20	ns	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$	6	
		—	—	28		$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$		
Delay Time from \overline{CS} Low to First Rising Edge of SCLK	t_{D1}	150	—	—	ns		12, 13	
Delay Time from Last Rising Edge of SCLK to \overline{CS} High	t_{D2}	150	—	—	ns		12, 13, 14	
Delay Time from DR high to Start of First SCLK	t_{DR}	150	—	—	ns		14	
Chip Select High Time	t_{CS_H}	200	—	—	ns		15	

Figure 4: MDAT and MCLK Timing Chart

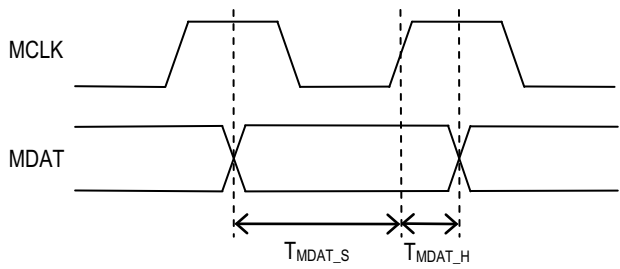


Figure 5: SPI Input Write Timing Chart

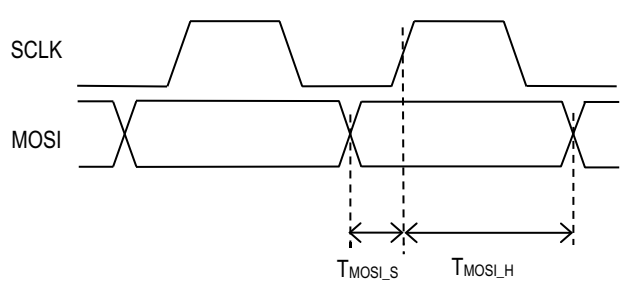


Figure 6: SPI Output Read Timing Chart

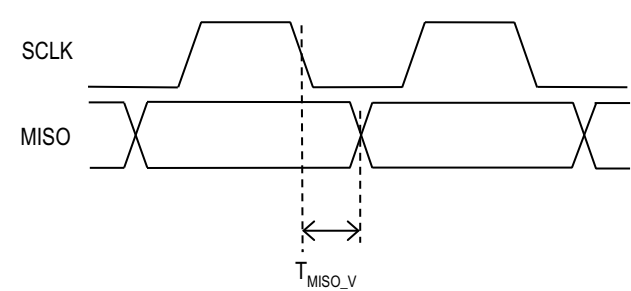
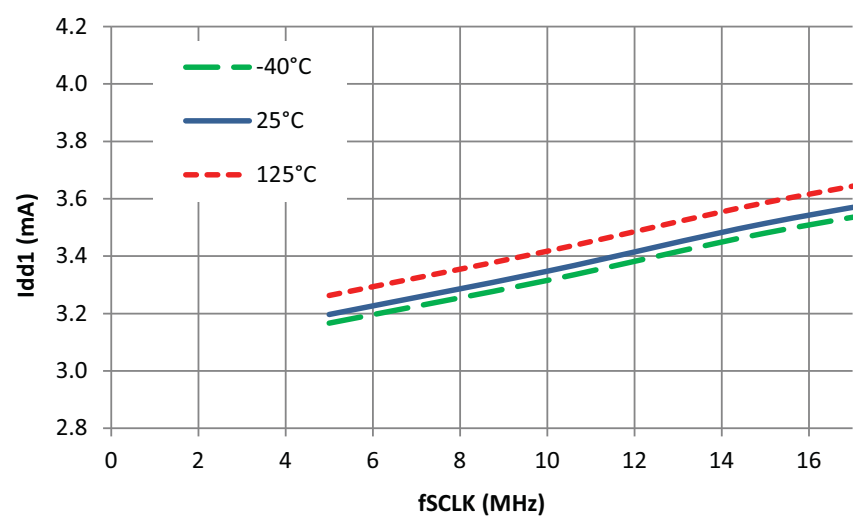


Figure 7: Power Supply Current vs. SPI Clock Frequency



Register Set

Register Address	Description	Default Value	Type
0x00	Filter setting	0x00	Read/Write
0x01	Channel selection & over-range setting	0x00	Read/Write
0x02	Interrupt status	0x00	Read Only
0x03	Interrupt enable	0x80	Read/Write
0x04	Offset Register for Channel 1 (MSB byte)	0x80	Read Only
0x05	Offset Register for Channel 1 (LSB byte)	0x00	Read Only
0x06	Offset Register for Channel 2 (MSB byte)	0x80	Read Only
0x07	Offset Register for Channel 2 (LSB byte)	0x00	Read Only
0x08	Offset Register for Channel 3 (MSB byte)	0x80	Read Only
0x09	Offset Register for Channel 3 (LSB byte)	0x00	Read Only

Register 0 (Address 0): Filter Setting

7	6	5	4	3	2	1	0
NA	Cal	Off_en	SYNC	Filter	NA	DC1	DC0

Default: 0x00 (Read/Write)

Filter	DC1	DC0	Decimation Ratio	Filter Type
0	0	0	1024	SINC ²
0	0	1	512	SINC ²
0	1	0	256	SINC ²
0	1	1	128	SINC ²
1	0	0	256	SINC ³
1	0	1	128	SINC ³
1	1	0	64	SINC ³

Filter	Filter Type
0	Sinc ² Filter
1	Sinc ³ Filter

SYNC	Synchronize
0	No synchronization, multi-clock filters
1	Synchronization of multi-clock filters

Off_en	Offset Enable
0	Filter data without offset
1	Filter data with offset

Cal	Calibration Offset and Store in Offset Registers
0	No offset action
1	Capture offset data and store in Offset Registers

Register 1 (Address 1): Channel Selection and Over-Range Setting

7	6	5	4	3	2	1	0
OV3	OV2	OV1	OV0	NA	NA	SEL1	SEL0

Default: 0x00 (Read/Write)

SEL1	SEL0	Channel Filter Operation Selection
0	0	Channel 1 Only
0	1	Channel 1 Only
1	0	Channel 1 and Channel 2 only
1	1	Channel 1, Channel 2, and Channel 3

OV3	OV2	OV1	OV0	Persistence of Continuous "1" or "0" Bit in MDAT Bit Stream
0	0	0	0	0 (No over-range detection)
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

NOTE: OV setting applied to channel 1, channel 2, and channel 3

Register 2 (Address 2): Interrupt Status

7	6	5	4	3	2	1	0
NA	NA	NA	NA	OV_CH3	OV_CH2	OV_CH1	DR

Default: 0x00 (Read only)

DR	Data Ready
0	Data not ready (ADC conversion in progress or not started)
1	ADC data ready to output

OV_CH1	Over-Range Trigger Status for Channel 1
0	No trigger for Channel 1 over-range
1	Triggered for Channel 1 over-range

OV_CH2	Over-Range Trigger Status for Channel 2
0	No trigger for Channel 2 over-range
1	Triggered for Channel 2 over-range

OV_CH3	Over-Range Trigger Status for Channel 3
0	No trigger for Channel 3 over-range
1	Triggered for Channel 3 over-range

NOTE:

- Interrupt status flag cleared after read from Interrupt register.
- Data Ready status for channel 1, channel 2, and channel 3. DR status output to DR pin.
- If more than one channel is turned on, Data Ready is from the slowest channel.

Register 3 (Address 3): Interrupt Enable

7	6	5	4	3	2	1	0
MCLK1_E	NA	NA	NA	OV_CH3_E	OV_CH2_E	OV_CH1_E	DR_E

Default: 0x80 (Read/Write)

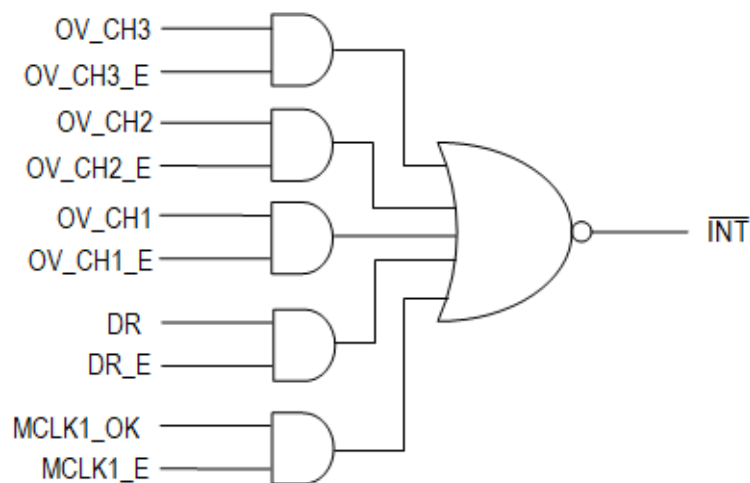
DR_E	Data Ready
0	Data Ready signal not output to Interrupt Pin $\overline{\text{INT}}$
1	Data Ready signal output to Interrupt Pin $\overline{\text{INT}}$

OV_CH1_E	Over-Range Trigger Status for Channel 1
0	Trigger for Channel 1 over-range status not output to $\overline{\text{INT}}$
1	Trigger for Channel 1 over-range status output to $\overline{\text{INT}}$

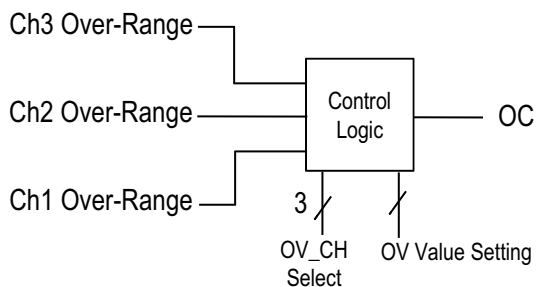
OV_CH2_E	Over-Range Trigger Status for Channel 2
0	Trigger for Channel 2 over-range status not output to $\overline{\text{INT}}$
1	Trigger for Channel 2 over-range status output to $\overline{\text{INT}}$

OV_CH3_E	Over-Range Trigger Status for Channel 3
0	Trigger for Channel 3 over-range status not output to $\overline{\text{INT}}$
1	Trigger for Channel 3 over-range status output to $\overline{\text{INT}}$

MCLK1_E	MCLK1 Activity Enable
0	MCLK1 Activity not output to Interrupt pin $\overline{\text{INT}}$
1	MCLK1 Activity output to Interrupt pin $\overline{\text{INT}}$ (default)

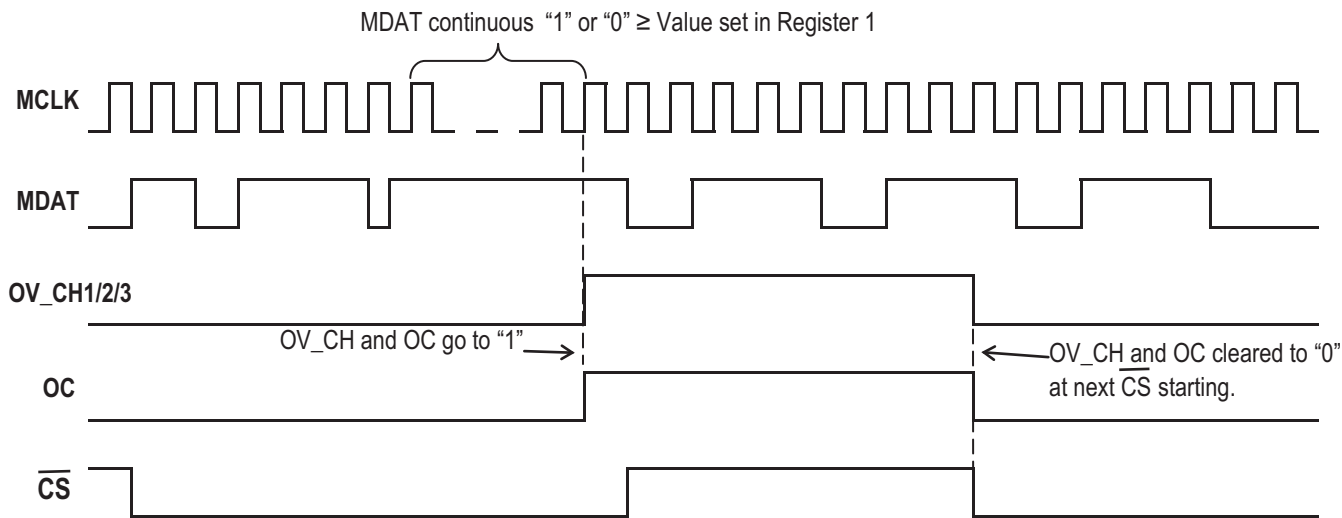
Figure 8: Interrupt Pin Implementation**Interrupt Pin Notes:**

- Interrupt output is active low.
- 0 = Check for interrupt status.
- 1 = No interrupt.

Figure 9: OC Pin Implementation

NOTE: OC pin is cleared by SPI \overline{CS} High to Low Transition.

Figure 10: Over-Range Detection Chart



Register 4 (Address 4): Offset Register for Channel 1 (MSB Byte)

7	6	5	4	3	2	1	0
off_15	off_14	off_13	off_12	off_11	off_10	off_9	off_8

Default: 0x80 (Read Only)

Register 5 (Address 5): Offset Register for Channel 1 (LSB Byte)

7	6	5	4	3	2	1	0
off_7	off_6	off_5	off_4	off_3	off_2	off_1	off_0

Default: 0x00 (Read Only)

Register 6 (Address 6): Offset Register for Channel 2 (MSB Byte)

7	6	5	4	3	2	1	0
off_15	off_14	off_13	off_12	off_11	off_10	off_9	off_8

Default: 0x80 (Read Only)

Register 7 (Address 7): Offset Register for Channel 2 (LSB Byte)

7	6	5	4	3	2	1	0
off_7	off_6	off_5	off_4	off_3	off_2	off_1	off_0

Default: 0x00 (Read Only)

Register 8 (Address 8): Offset Register for Channel 3 (MSB Byte)

7	6	5	4	3	2	1	0
off_15	off_14	off_13	off_12	off_11	off_10	off_9	off_8

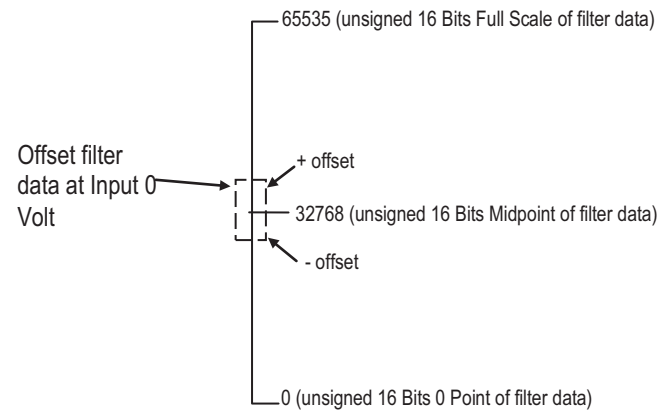
Default: 0x80 (Read Only)

Register 9 (Address 9): Offset Register for Channel 3 (LSB Byte)

7	6	5	4	3	2	1	0
off_7	off_6	off_5	off_4	off_3	off_2	off_1	off_0

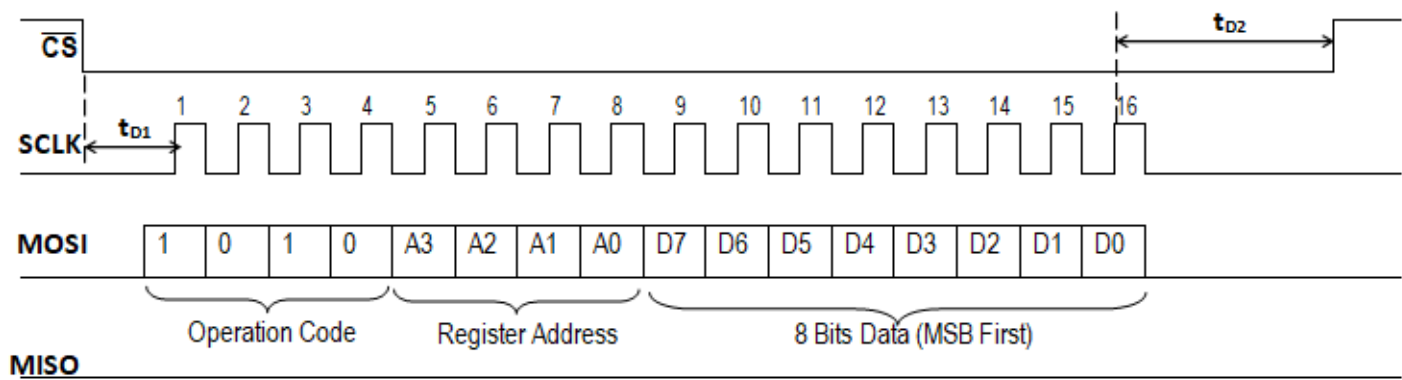
Default: 0x00 (Read Only)

Figure 11: Offset Filter Data



SPI – Write to Registers Timing Chart

Figure 12: SPI Writing to Registers Timing Chart



Operation code	1010
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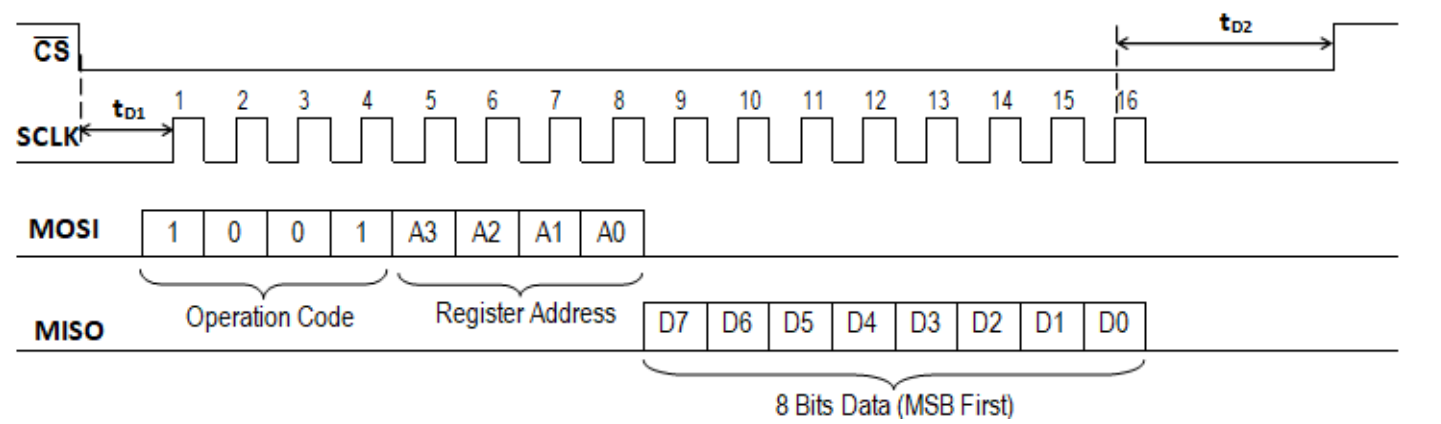
A3	A2	A1	A0	Register Address
0	0	0	0	0x00
0	0	0	1	0x01
0	0	1	1	0x03

8 bits data (MSB first)	D7	D6	D5	D4	D3	D2	D1	D0
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After \overline{CS} goes low, write/read must be in the multiple 16 bits (16 cycles of SCLK).

SPI – Read from Register Timing Chart

Figure 13: SPI Read from Registers Timing Chart



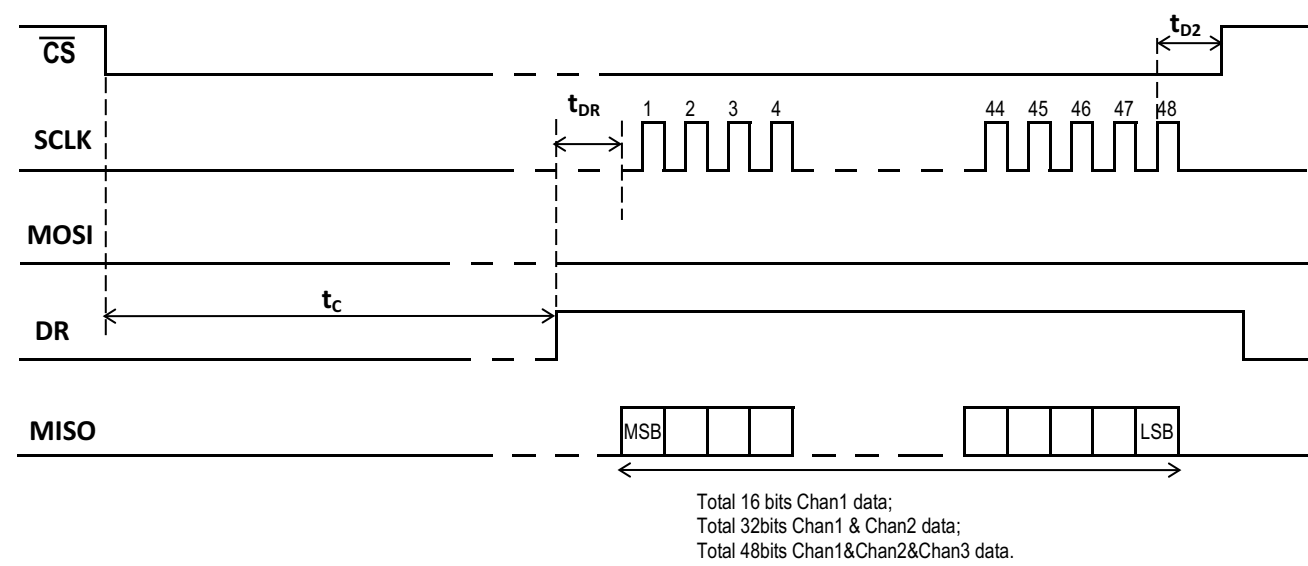
Operation code	1001
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A3	A2	A1	A0	Register Address
0	0	0	0	0x00
0	0	0	1	0x01
0	0	1	0	0x02
0	0	1	1	0x03
0	1	0	0	0x04
0	1	0	1	0x05
0	1	1	0	0x06
0	1	1	1	0x07
1	0	0	0	0x08
1	0	0	1	0x09

8 bits data (MSB first)	D7	D6	D5	D4	D3	D2	D1	D0
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SPI – Read from Filter's Data Timing Chart

Figure 14: SPI Read from Filter's Data Timing Chart



Chan 1 data	16 Bits Chan1 filter data		
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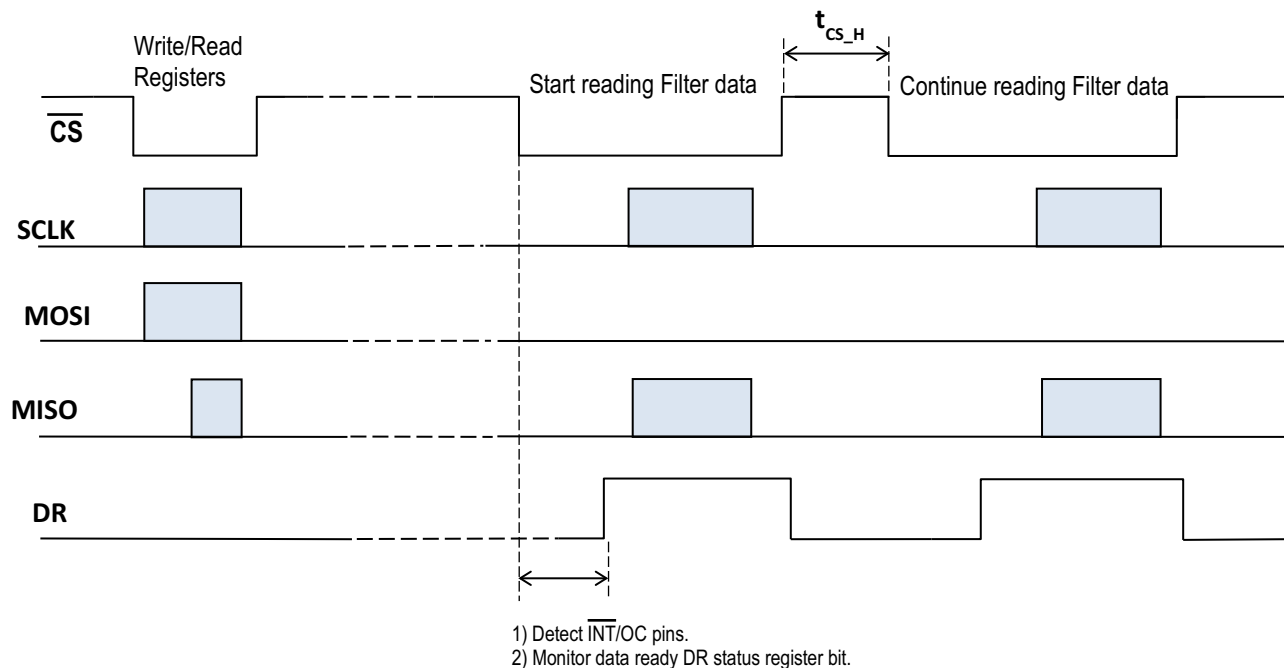
Chan1 data and Chan2 data	16 bits Chan1 filter data	16 bits Chan2 filter data	
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Chan1 data and Chan2 data and Chan3 data	16 bits Chan1 filter data	16 bits Chan2 filter data	16 bits Chan3 filter data
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- Filter conversion start after falling edge of \overline{CS} signal.
- After data ready, filters data can be read out in the multiple of 16 bits.
- \overline{CS} signal has two functions: filter conversion start and chip select for SPI interface.
- When \overline{CS} is low, write from and read to registers are allowed.

SPI – Combined Operation: Write/Read Register and Read from Filter's Data Timing Chart

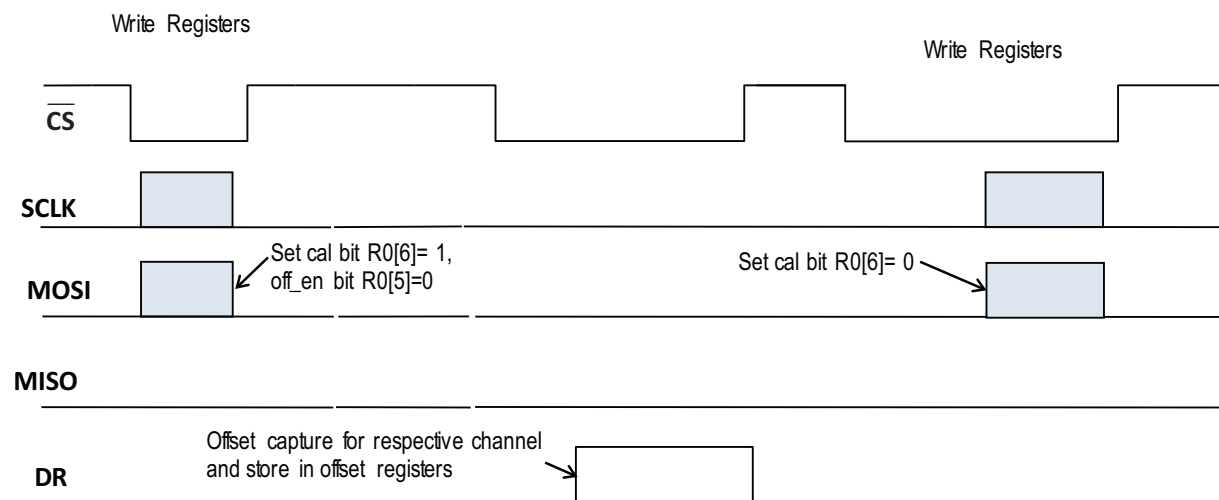
Figure 15: SPI Combined Operation: Write/Read Register and Read from Filter's Data Timing Chart



Total 16 bits Chan1 data;
 Total 32bits Chan1 & Chan2 data;
 Total 48bits Chan1&Chan2&Chan3 data.

SPI – Offset Calibration Operation

Figure 16: SPI Offset Calibration Operation



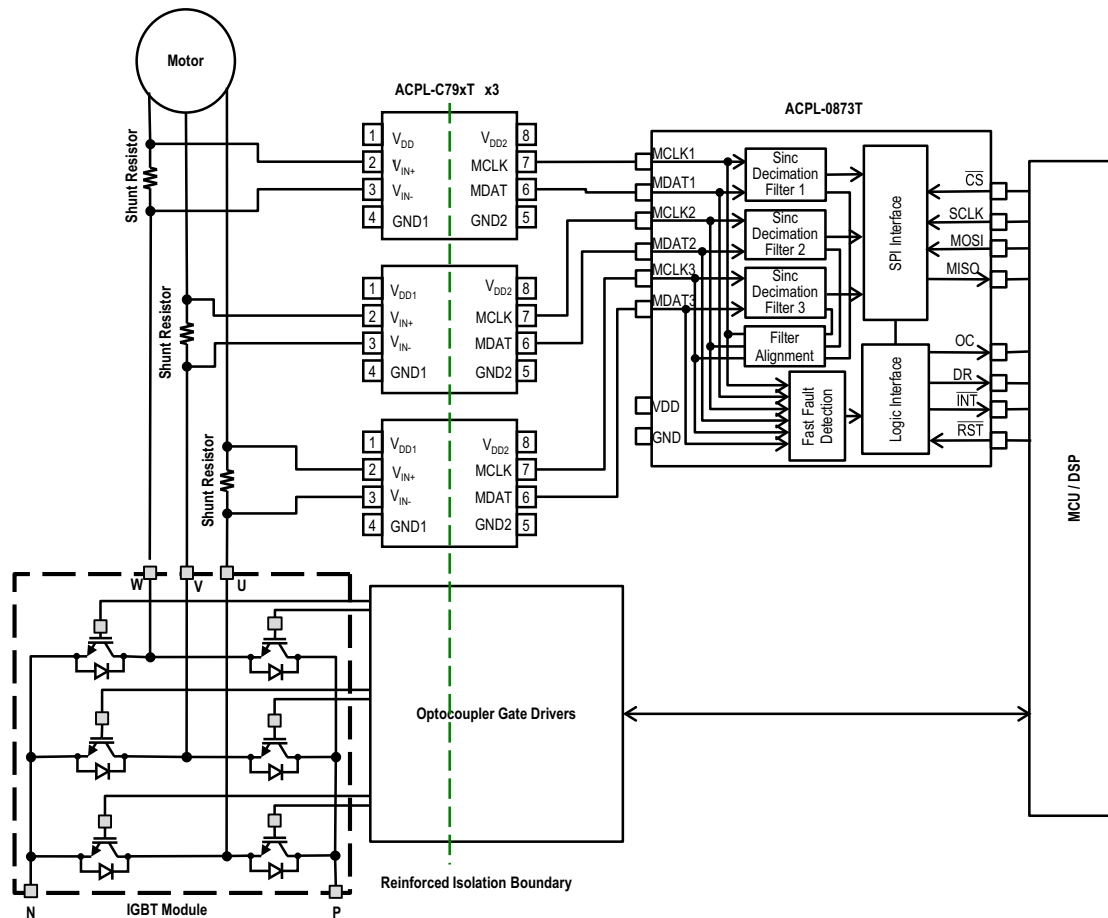
- Physically short Sigma-Delta Modulator (that is, ACPL-C799T) input pins Vin+ and Vin– to GND1.
- Set cal bit R0[6] = 1, Set off_en bit R0[5] = 0, Set filter setting to Sinc³ Decimation Ratio 256.
- $\overline{\text{CS}}$ goes low until DR goes high to capture the offset and store in offset registers.
- Set cal bit R0[6] = 0.
- To turn on the final filter data with offset, set off_en bit R0[5] = 1.
- To have the final filter data without any offset, set off_en bit R0[5] = 0.

Typical Application Circuit in Motor Drive Phase Current Sensing

The ACPL-0873T filter module implements second-order or third-order Sinc digital filtering technologies for three individual channels. Sinc² mode has four decimation ratios: x128, x256, x512, or x1024 and Sinc³ has three decimation ratios: x64, x128, or x256. The combination of Sinc^K and decimation ratio provides great flexibility with a total of seven filtering modes.

The ACPL-0873T communicates with MCUs and DSPs via an SPI interface. The SPI interface runs fully asynchronously to the inputs.

Figure 17: Typical Phase Current Sensing Circuit using ACPL-C79xT and ACPL-0873T



In a close-loop current feedback motor control application as shown in Figure 17, motor phase current is converted to voltage through a very low Ohm shunt. An isolated sigma-delta modulator, such as ACPL-C797T or ACPL-C799T, converts the analog voltage signal into a single-bit data stream. The digital filter ASIC ACPL-0873T converts the 1-bit data stream into 16-bit serial digital output interface that is compatible to SPI protocol, allowing direct connection to a microcontroller. The digital filter can select conversion channel at one channel, two channels, or three channels.

Channel 1 MCLK1 is detected when the device is powered up. When the MCLK1 is detected normal, the device operation is enabled; otherwise, all functional operation is disabled and interruption output $\overline{\text{INT}}$ is active.

All channel Sigma-Delta Modulators should be same nominal clock frequency, and highest channel to lowest channel MCLK clock frequency difference does not exceed 20%.

ACPL-0873T works as SPI slave device, and the master device should select clock phase mode CPHA=0 and clock polarity mode CPOL = 0. MOSI data is sampled in on the rising edge of SPI clock, MISO data is clocked out at the falling edge of SPI clock.

Thermal Resistance

ACPL-0873T IC (Die) junction temperature is calculated as:

$$T_j = R \times P + T_a$$

Where

R: Junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$).

P: Power dissipation of IC (W).

T_j: Junction temperature of IC.

T_a: Ambient temperature.

The IC was mounted on a low conductivity test board. The board measures 76.2 mm × 76.2 mm as per JEDEC standards. In total, two low-conductivity boards were prepared for the measurement. These test boards are made of FR-4 material and thickness of the copper traces as per JEDEC standards for low conductivity board. Tested “good” devices were used on all the boards. The thermal resistance measurement data is R = 74 $^{\circ}\text{C}/\text{W}$.

Appendices

Table 3: Digital Filter Typical Conversion Time

Filter (Sinc ^K)	Decimation Ratio (D)	Filter Conversion Time t _C at 10-MHz MCLK (1/t _C)
SINC ²	1024	205 μs (4.88 kHz)
SINC ²	512	102 μs (9.76 kHz)
SINC ²	256	51 μs (19.52 kHz)
SINC ²	128	25 μs (39.04 kHz)
SINC ³	256	77 μs (13.02 kHz)
SINC ³	128	38 μs (26.04 kHz)
SINC ³	64	19 μs (52.08 kHz)

NOTE: t_C is calculated as: $t_C = 1 / f_{\text{MCLK}} \times D \times K$.

Table 4: SPI Typical Timing

SPI Clock (MHz)	Time for 8 Bits Write (μs)	Time for 8 Bits Write and 8 Bits Read (μs)	Time for 48 Bits Read (μs)
5	1.60	3.20	9.6
10	0.80	1.60	4.8
15	0.53	1.06	3.18
17	0.47	0.94	2.82

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