BROADCOM®

BCM56450

102.5 Gbps Integrated Multilayer Ethernet Switch and Traffic Manager

GENERAL DESCRIPTION

The Broadcom® BCM56450 is purpose-built for next-generation Carrier Ethernet EAdvance Data Sheetdge and Mobile Backhaul platforms. It combines a feature-rich packet processing engine, integrated hierarchical traffic manager, deep external packet buffer, address management, and a non-blocking switch fabric into a single 40 nm CMOS device. The BCM56450 supports an integrated packet buffer with an external packet buffer expansion option, utilizing economical DDR3 SDRAM technology. The BCM56450 is capable of handling L2 switching, L3 routing, metro VPN tunneling, and access control lists (ACLs). The BCM56450 virtualized architecture enables seamless support for VPLS, VPWS, MPLS-TP, PBB, and PBB-TE tunneling. In addition, the BCM56450 supports internal processing of Ethernet OAM and BFD to enable a complete host CPU offload for these functions.

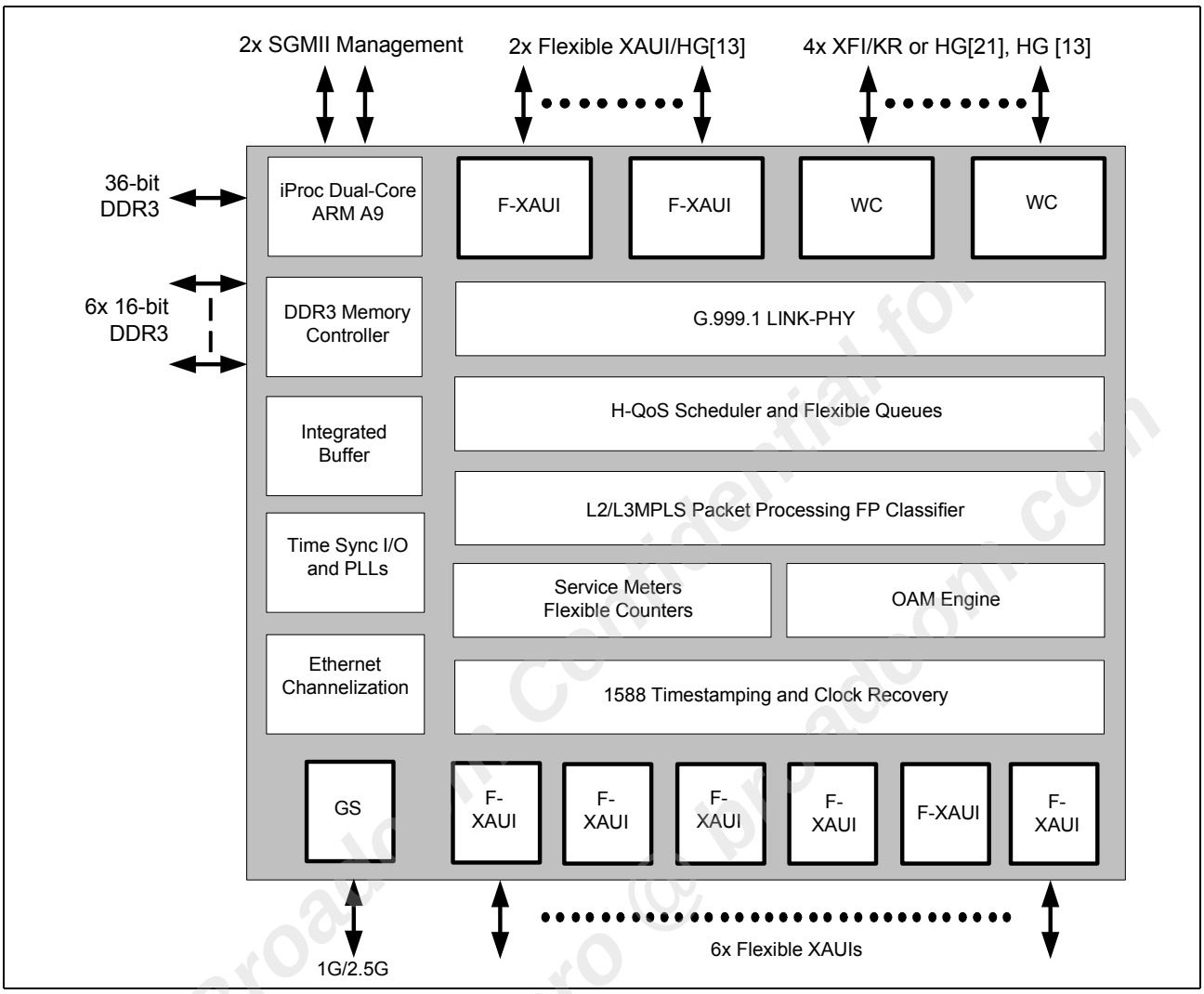
The BCM56450 has three ContentAware™ processors distributed throughout various stages of the pipeline to allow actions to be taken based on various matching criteria.The device complies with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab, and IEEE 802.3x specifications. It incorporates 10 flex XAUI cores, each core provides up to 4x 1GbE, 4x 2.5GbE, or 1x 10GbE. Within the 10 flex XAUI cores, there are up to four stacking ports that can be configured as HiGig2 stacking ports. Multiple BCM56450 devices can be connected together using the stacking links to create high port density systems. The BCM56450 supports flexible Quality of Service (QoS), including IEEE 802.1p and DiffServ/TOS. Up to 64K MAC addresses, 4K VLANs, STP, and IEEE 802.1x MAC security are supported. The device integrates a dual-core ARM Cortex A9 processor running at 1 GHz to allow a complete solution to be developed without an external host processor. The device also provides a two-lane PCI Express interface that can be configured to operate as a Root Complex or End-Point.

The BCM56450 also offers unparalleled integration for supporting Ethernet time synchronization. Synchronous Ethernet Clock recovery is supported on any of the ports to support physical layer clock synchronization. In addition to physical layer clock synchronization, the BCM56450 also provides hooks for both 1588v2 and IEEE 802.1as packet-based clock synchronization and offers an integrated DPLL for recovered clock cleanup, as well as G.823- and G.824-compliant clock synthesizer to reduce overall cost and ease production.

FEATURES

- Integrated 2.0 MB packet buffer
- Support for up to 720 MB of external packet buffer using six DDR3 SDRAMs
- Integrated hierarchical traffic manager supporting:
  - Four-level hierarchical scheduler
  - Min/Max rate guarantees at each scheduling level
- MEF-compliant hierarchical metering with 8 Kbps granularity
- Supports double-tagging for IEEE 802.1ad provider bridging, Broadband Forum TR-101, and TR-156
- Supports VLAN translation in both ingress and egress
- Supports Multi-protocol Label Switching (MPLS) for L2 VPLS/VPWS and L3 MPLS services
- Supports IEEE 802.1ah provider backbone bridging and IEEE 802.1Qay provider backbone bridging with traffic engineering
- Ethernet OAM support in hardware (IEEE 802.1ag and ITU Y.1731)
- Supports hardware-based IP multicast routing, forwarding, replication, and tunneling
- Advanced ContentAware processor for VLAN, ingress, and egress
- Advanced security features in hardware
- Supports port trunking and mirroring across stack
- Supports advanced packet flow control: Head of Line (HOL) blocking prevention, back pressure
- Supports packet classification using IEEE 802.1p QoS or DiffServ/TOS priority
- Low power 40 nm CMOS process
- 48 QoS queues for CPU
- RFC3176 sFlow traffic monitoring
- Virtual Route and Forwarding (VRF) support
- Equal cost multipath (ECMP) and weighted cost multipath (WCMP)
- Integrated host processor with dual ARM cores
- Ethernet channelization support through the use of an additional tag
- G.999.1 fragmentation and Ethernet Adaptation support

Figure 1: Functional Block Diagram



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