

ACPL-570xL, ACPL-573xL, ACPL-177xL, ACPL-675xL, 5962-08227¹



Hermetically Sealed 3.3V, Low I_F , Wide V_{CC} ,
High Gain Optocouplers

Data Sheet

Description

These devices are single, dual, and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial product or with full MIL-PRF-38534 Class Level H or K testing or from DLA Standard Microcircuit Drawing (SMD) 5962-08227. All devices are manufactured and tested on a MIL-PRF-38534 certified line and Class H and K devices are included in the DLA Qualified Products Database Supplemental Information Sheets QML-38534 as Hybrid Microcircuits.

Each channel contains a GaAsP light emitting diode that is optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output, providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers.

The supply voltage can be operated as low as 3.0V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA, making them ideal for use in low input current applications such as MOS, CMOS, low-power logic interfaces, or line receivers.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

1. See [Selection Guide — Package Styles and Lead Configuration Options](#) for available extensions.

Features

- Low power consumption
- 3.3V supply voltages
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Three hermetically sealed package configurations
- Performance guaranteed over full military temperature range: -55°C to $+125^{\circ}\text{C}$
- Low input current requirement: 0.5 mA
- High current transfer ratio: 1500% typical at $I_F = 0.5$ mA
- Low output saturation voltage: 0.11V typical
- 1500 Vdc withstand test voltage
- HCPL-4701/31, -070A/31 function compatibility

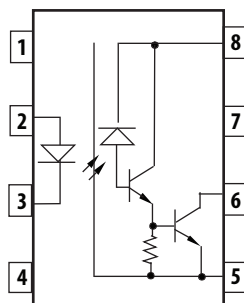
Applications

- Military and aerospace
- High reliability systems
- Telephone ring detection
- Microprocessor system interface
- Transportation, medical, and life critical systems
- Isolated input line receiver
- EIA RS-232-C line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Current loop receiver
- System test equipment isolation
- Process control input/output isolation

Package styles for these parts are 8- and 16-pin DIP through hole (case outlines P and E respectively), and 16-pin surface mount DIP flat pack (case outline F). Devices can be purchased with a variety of lead bend and plating options. See the [Selection Guide — Package Styles and Lead Configuration Options](#) table for details. Standard Military Drawing (SMD) parts are available for some package and lead styles.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are similar for all parts except as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities justify the use of a common data base for die related reliability.

Functional Diagram



Truth Table

(Positive Logic)

| Input | Output |
|---------|--------|
| On (H) | L |
| Off (L) | H |

NOTE The connection of a 0.1- μ F bypass capacitor between V_{CC} and GND is recommended.

Selection Guide — Package Styles and Lead Configuration Options

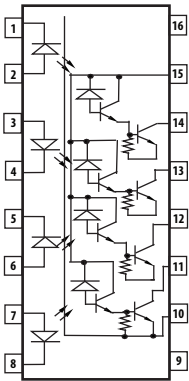
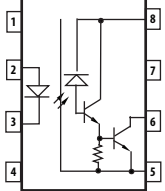
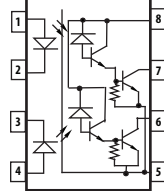
| Package | 16-Pin DIP | 8-Pin DIP | 8-Pin DIP | 16-Pin Flat Pack |
|-----------------------------------|----------------|--------------|----------------|------------------|
| Lead Style | Through Hole | Through Hole | Through Hole | Unformed leads |
| Channels | 4 | 1 | 2 | 4 |
| Common Channel Wiring | V_{CC} , GND | None | V_{CC} , GND | V_{CC} , GND |
| Withstand Test Voltage | 1500 Vdc | 1500 Vdc | 1500 Vdc | 1500 Vdc |
| Part Number and Options | | | | |
| Commercial | ACPL-1770L | ACPL-5700L | ACPL-5730L | ACPL-6750L |
| MIL-PRF-38534, Class H | ACPL-1772L | ACPL-5701L | ACPL-5731L | ACPL-6751L |
| MIL-PRF-38534, Class K | ACPL-177KL | ACPL-570KL | ACPL-573KL | ACPL-675KL |
| Standard Lead Finish ^a | Gold Plate | Gold Plate | Gold Plate | Gold Plate |
| Solder Dipped ^b | Option -200 | Option -200 | Option -200 | |
| Butt Cut/Gold Plate ^a | Option -100 | Option -100 | Option -100 | |
| Gull Wing/Soldered ^b | Option -300 | Option -300 | Option -300 | |
| Class H SMD Part Number | | | | |
| Prescript for all below | 5962- | 5962- | 5962- | 5962- |
| Gold Plate ^a | 0822703HEC | 0822701HPC | 0822702HPC | 0822704HZC |
| Solder Dipped ^b | 0822703HEA | 0822701HPA | 0822702HPA | |
| Butt Cut/Gold Plate ^a | 0822703HUC | 0822701HYC | 0822702HYC | |
| Butt Cut/Soldered ^b | 0822703HUA | 0822701HYA | 0822702HYA | |
| Gull Wing/Soldered ^b | 0822703HTA | 0822701HXA | 0822702HXA | |

| Package | 16-Pin DIP | 8-Pin DIP | 8-Pin DIP | 16-Pin Flat Pack |
|----------------------------------|------------|------------|------------|------------------|
| Class K SMD Part Number | | | | |
| Prescript for all below | 5962- | 5962- | 5962- | 5962- |
| Gold Plate ^a | 0822703KEC | 0822701KPC | 0822702KPC | 0822704KZC |
| Solder Dipped* | 0822703KEA | 0822701KPA | 0822702KPA | |
| Butt Cut/Gold Plate ^a | 0822703KUC | 0822701KYC | 0822702KYC | |
| Butt Cut/Soldered ^b | 0822703KUA | 0822701KYA | 0822702KYA | |
| Gull Wing/Soldered ^b | 0822703KTA | 0822701KXA | 0822702KXA | |

a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.

b. Solder lead finish: Sn63/Pb37.

Functional Diagrams

| 16-Pin DIP | 8-Pin DIP | 8-Pin DIP |
|--|--|--|
| Through Hole and Flat Pack | Through Hole | Through Hole |
| 4 Channels | 1 Channel | 2 Channels |
|  |  |  |

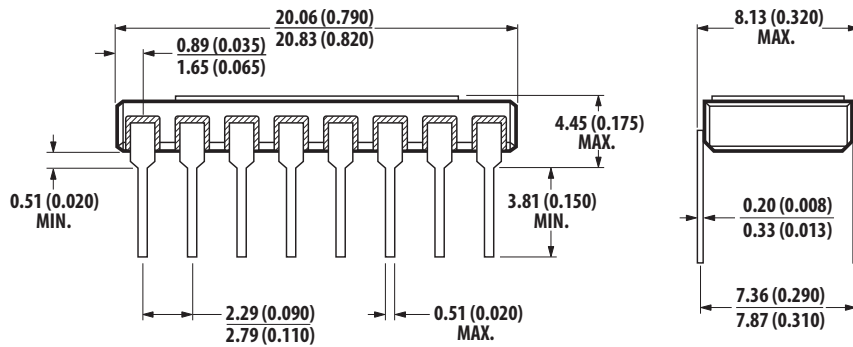
Device Marking

| | | | |
|------------------------|---|----------|--|
| Avago LOGO | → | A QYYWWZ | ← COMPLIANCE INDICATOR, ^[1] |
| Avago P/N | → | XXXXXX | DATE CODE, SUFFIX (IF NEEDED) |
| DLA SMD ^[1] | → | XXXXXX | |
| DLA SMD ^[1] | → | XXX XXX | ← COUNTRY OF MFR. |
| PIN ONE/ESD IDENT | → | X 50434 | ← Avago CAGE CODE ^[1] |

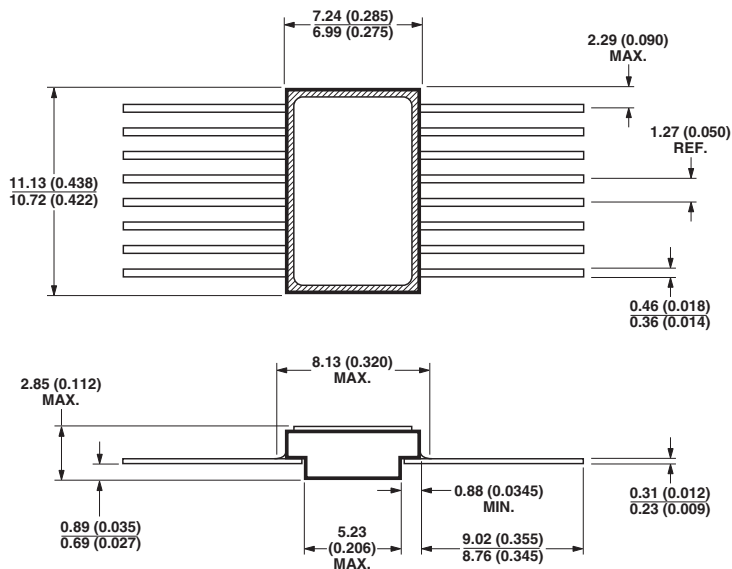
[1] QML PARTS ONLY

Outline Drawings

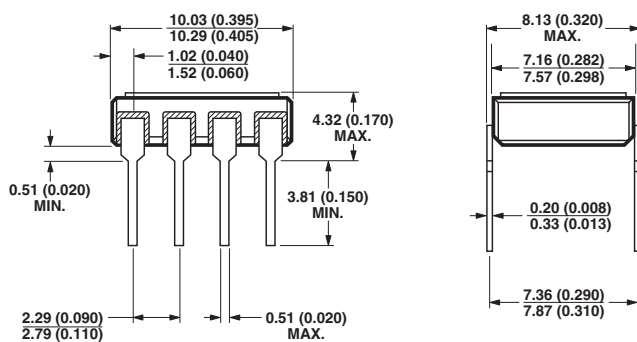
16-Pin DIP Through Hole, 4 Channels



16-Pin Flat Pack, 4 Channels

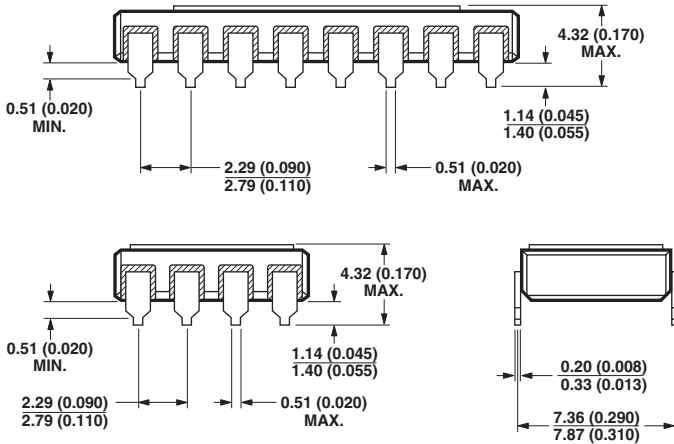
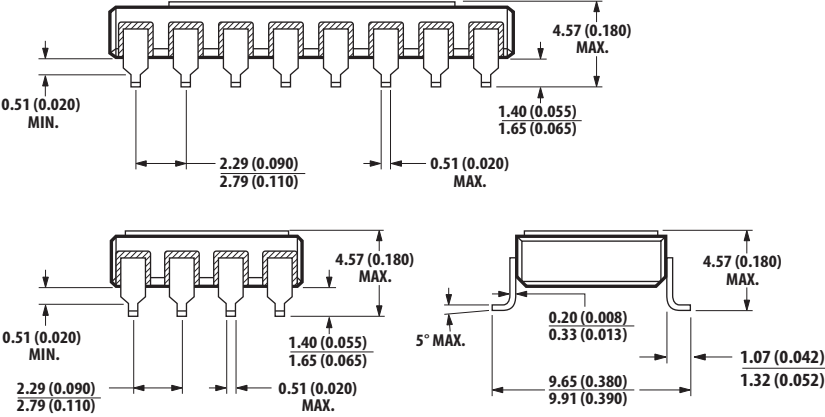


8-Pin DIP Through Hole, 1 and 2 Channel



Note: Dimensions in Millimeters (Inches).

Hermetic Optocoupler Options

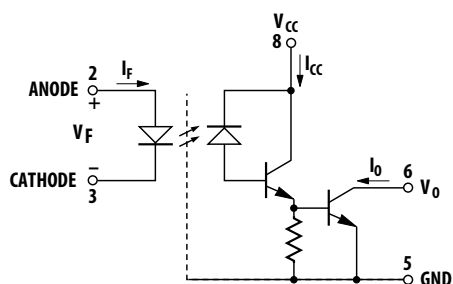
| Option | Description |
|--------|---|
| 100 | <p>Surface-mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H and Class K product in 8-pin and 16-pin DIP.</p>  <p>Top view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.14 (0.045) / 1.40 (0.055) mm; Package width 7.36 (0.290) / 7.87 (0.310) mm; Pin height from base 4.32 (0.170) mm MAX.</p> <p>Side view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.14 (0.045) / 1.40 (0.055) mm; Package width 7.36 (0.290) / 7.87 (0.310) mm; Pin height from base 4.32 (0.170) mm MAX.</p> <p>End view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.14 (0.045) / 1.40 (0.055) mm; Package width 7.36 (0.290) / 7.87 (0.310) mm; Pin height from base 4.32 (0.170) mm MAX.</p> |
| 200 | <p>Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H and Class K product in 8-pin and 16-pin DIP. DLA Drawing (SMD) part numbers contain provisions for lead finish.</p> |
| 300 | <p>Surface-mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H and Class K product in 8-pin and 16-pin DIP. This option has solder-dipped leads.</p>  <p>Top view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.40 (0.055) / 1.65 (0.065) mm; Package width 9.65 (0.380) / 9.91 (0.390) mm; Pin height from base 4.57 (0.180) mm MAX.</p> <p>Side view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.40 (0.055) / 1.65 (0.065) mm; Package width 9.65 (0.380) / 9.91 (0.390) mm; Pin height from base 4.57 (0.180) mm MAX.</p> <p>End view dimensions: Pin pitch 2.29 (0.090) / 2.79 (0.110) mm; Pin width 0.51 (0.020) mm; Pin height 1.40 (0.055) / 1.65 (0.065) mm; Package width 9.65 (0.380) / 9.91 (0.390) mm; Pin height from base 4.57 (0.180) mm MAX.</p> <p>Lead angle 5° MAX.</p> |

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|----------|------|----------------|------|-------|
| Storage Temperature | T_S | -65 | +150 | °C | |
| Operating Temperature | T_A | -55 | +125 | °C | |
| Case Temperature | T_C | — | +170 | °C | |
| Junction Temperature | T_J | — | +175 | °C | |
| Lead Solder Temperature | | — | 260 for 10 sec | °C | |
| Output Current (Each Channel) | I_O | — | 40 | mA | |
| Output Voltage (Each Channel) | V_O | -0.5 | 20 | V | a |
| Supply Voltage | V_{CC} | -0.5 | 20 | V | a |
| Output Power Dissipation (Each Channel) | | — | 50 | mW | b |
| Peak Input Current (Each Channel, <1 ms Duration) | | — | 20 | mA | |
| Average Input Current (Each Channel) | I_F | — | 10 | mA | c |
| Reverse Input Voltage (Each Channel) | V_R | — | 5 | V | |
| Package Power Dissipation (Each Channel) | P_D | — | 200 | mW | |

- GND pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0V, will provide lowest total I_{OH} over temperature.
- Output power is collector output power plus total supply power for the single-channel device. For the dual-channel device, output power is collector output power plus one half the total supply power. For the quad-channel device, output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
- Derate I_F at 0.33 mA/°C above 110°C.

8-Pin Ceramic DIP Single-Channel Schematic



ESD Classification

(MIL-STD-883, Method 3015)

| | |
|----------------------------------|-----------------|
| ACPL-5700L/01L/0KL, 5962-0822701 | ▲▲, Class 2 |
| ACPL-5730L/31L/3KL, 5962-0822702 | ▲▲▲ A, Class 3A |
| ACPL-1770L/2L/KL, 5962-0822703 | ▲▲▲ B, Class 3B |
| ACPL-6750L/1L/KL, 5962-0822704 | ▲▲▲ A, Class 3A |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit |
|--|--------------|------|------|---------------|
| Input Current, Low Level (Each Channel) | $I_{F(OFF)}$ | — | 2.0 | μA |
| Input Current, High Level (Each Channel) | $I_{F(ON)}$ | 0.5 | 5 | mA |
| Supply Voltage | V_{CC} | 3.0 | 7.0 | V |
| Output Voltage | V_O | 3.0 | 7.0 | V |

Electrical Characteristics

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.

| Parameter | | Symbol | Test Conditions | Group A ^a Subgroup | Limits | | | Unit | Fig. | Note |
|---|----------------|-----------|--|----------------------------------|--------|-------------------|------|---------------|------|---------|
| | | | | | Min. | Typ. ^b | Max. | | | |
| Current Transfer Ratio | | CTR | $I_F = 0.5 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 3.0 \text{ V}$ | 1, 2, 3 | 300 | 1500 | — | % | 3 | c, d |
| | | | $I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 3.0 \text{ V}$ | | 300 | 1300 | — | | | |
| | | | $I_F = 5 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 3.0 \text{ V}$ | | 200 | 800 | — | | | |
| Logic Low Output Voltage | | V_{OL} | $I_F = 0.5 \text{ mA}, I_{OL} = 1.5 \text{ mA}, V_{CC} = 3.0 \text{ V}$ | 1, 2, 3 | — | 0.05 | 0.4 | V | 2 | c |
| | | | $I_F = 1.6 \text{ mA}, I_{OL} = 4.8 \text{ mA}, V_{CC} = 3.0 \text{ V}$ | | — | 0.06 | 0.4 | | | c |
| | | | $I_F = 5 \text{ mA}, I_{OL} = 10 \text{ mA}, V_{CC} = 3.0 \text{ V}$ | | — | 0.09 | 0.4 | | | c |
| Logic High Output Current | | I_{OH} | $I_F = 2 \mu\text{A}, V_O = 7 \text{ V}, V_{CC} = 7 \text{ V}$ | 1, 2, 3 | — | 1.0 | 100 | μA | | c |
| | | I_{OHX} | | | — | 1.0 | 100 | μA | | c, e |
| Logic Low Supply Current | Single Channel | I_{CCL} | $I_F = 1.6 \text{ mA}, V_{CC} = 7 \text{ V}$ | 1, 2, 3 | — | 0.8 | 2 | mA | 4 | |
| | Dual Channel | | $I_{F1} = I_{F2} = 1.6 \text{ mA}, V_{CC} = 7 \text{ V}$ | | — | 0.8 | 4 | | | |
| | Quad Channel | | $I_{F1} = I_{F2} = I_{F3} = I_{F4} = 1.6 \text{ mA}, V_{CC} = 7 \text{ V}$ | | — | 1.3 | 4 | | | |
| Logic High Supply Current | Single Channel | I_{CCH} | $I_F = 0 \text{ mA}, V_{CC} = 7 \text{ V}$ | 1, 2, 3 | — | 0.01 | 20 | μA | | |
| | Dual Channel | | $I_{F1} = I_{F2} = 0 \text{ mA}, V_{CC} = 7 \text{ V}$ | | — | | 40 | | | |
| | Quad Channel | | $I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 \text{ mA}, V_{CC} = 7 \text{ V}$ | | — | | 40 | | | |
| Input Forward Voltage | | V_F | $I_F = 1.6 \text{ mA}$ | 1, 2, 3 | 1.0 | 1.4 | 1.8 | V | 1 | c |
| Input Reverse Breakdown Voltage | | B_{VR} | $I_R = 10 \mu\text{A}$ | 1, 2, 3 | 5 | — | — | V | | c |
| Input-Output Insulation Leakage Current | | I_{I-O} | $\leq 65\%$ Relative Humidity, $T_A = 25^\circ\text{C}$, $t = 5 \text{ s}, V_{I-O} = 1500 \text{ VDC}$ | 1 | — | — | 1.0 | μA | | f, g |
| Capacitance Between Input-Output | | C_{I-O} | $f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$ | 4 | — | — | 4 | pF | | c, h, i |

| Parameter | Symbol | Test Conditions | Group A ^a Subgroup | Limits | | | Unit | Fig. | Note |
|---|------------------|--|----------------------------------|--------|-------------------|------|------|------------|------------|
| | | | | Min. | Typ. ^b | Max. | | | |
| Propagation Delay Time to Logic Low at Output | t _{PHL} | I _F = 0.5 mA, R _L = 2.2 kΩ, V _{CC} = 3.3V | 9, 10, 11 | — | 40 | 100 | μs | 5, 6, 7, 8 | c |
| | t _{PHL} | I _F = 1.6 mA, R _L = 680Ω, V _{CC} = 3.3V | 9, 10, 11 | — | 9 | 30 | | | |
| | t _{PHL} | I _F = 5 mA, R _L = 330Ω, V _{CC} = 3.3V | 9 | — | 2 | 5 | | | |
| | | | 10, 11 | — | 2 | 10 | | | |
| Propagation Delay Time to Logic High at Output | t _{PLH} | I _F = 0.5 mA, R _L = 2.2 kΩ, V _{CC} = 3.3V | 9, 10, 11 | — | 10 | 60 | μs | 5, 6, 7, 8 | c |
| | t _{PLH} | I _F = 1.6 mA, R _L = 680Ω, V _{CC} = 3.3V | 9, 10, 11 | — | 8 | 50 | | | |
| | t _{PLH} | I _F = 5 mA, R _L = 330Ω, V _{CC} = 3.3V | 9 | — | 6 | 20 | | | |
| | | | 10, 11 | — | — | 30 | | | |
| Common Mode Transient Immunity at Low Output Level | CM _L | V _{CC} = 3.3V, I _F = 1.6 mA, R _L = 680Ω, V _{CM} = 50 V _{P-P} | 9, 10, 11 | 500 | 1000 | — | V/μs | 9 | c, j, k, i |
| Common Mode Transient Immunity at High Output Level | CM _H | V _{CC} = 3.3 V, I _F = 0 mA, R _L = 680Ω, V _{CM} = 50 V _{P-P} | 9, 10, 11 | 500 | 1000 | — | V/μs | 9 | c, j, k, i |

- a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- b. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
- c. Each channel.
- d. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
- e. I_{OHX} is the leakage current resulting from channel-to-channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
- f. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- g. This is a momentary withstand test, not an operating condition.
- h. Measured between each input pair shorted together and all output connections for that channel shorted together.
- i. Parameters tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.
- j. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).
- k. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge), a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is:

For single channel:

$$R_{CC} = \frac{1(V)}{0.15 I_F (mA)} \text{ k}\Omega$$

For dual channel:

$$R_{CC} = \frac{1(V)}{0.3 I_F (mA)} \text{ k}\Omega$$

For quad channel:

$$R_{CC} = \frac{1(V)}{0.6 I_F (mA)} \text{ k}\Omega$$

Typical Characteristics

$T_A = 25^\circ\text{C}$

| Parameter | Symbol | Typ. | Unit | Test Conditions | Note |
|---|---------------------------|-----------|----------------------|---|------|
| Input Capacitance | C_{IN} | 60 | pF | $V_F = 0V, f = 1\text{ MHz}$ | a |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ | -1.8 | mV/ $^\circ\text{C}$ | $I_F = 1.6\text{ mA}$ | a |
| Resistance (Input-Output) | R_{I-O} | 10^{12} | Ω | $V_{I-O} = 500V$ | a, b |
| Capacitance (Input-Output) | C_{I-O} | 2.0 | pF | $f = 1\text{ MHz}$ | a, b |
| Dual and Quad Channel Product Only | | | | | |
| Input-Input Leakage Current | I_{I-I} | 0.5 | nA | Relative Humidity = $\leq 65\%$, $V_{I-I} = 500V, t = 5\text{ s}$ | c |
| Resistance (Input-Input) | R_{I-I} | 10^{12} | Ω | $V_{I-I} = 500V$ | c |
| Capacitance (Input-Input) | C_{I-I} | 1.0 | pF | $f = 1\text{ MHz}$ | c |

- a. Each channel.
- b. Measured between each input pair shorted together and all output connections for that channel shorted together.
- c. Measured between adjacent input pairs shorted together for each multichannel device.

Figure 1 Input Diode Forward Current vs. Forward Voltage

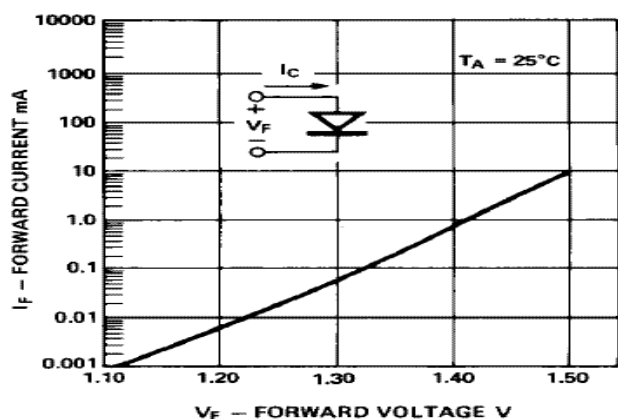


Figure 2 Normalized DC Transfer Characteristics

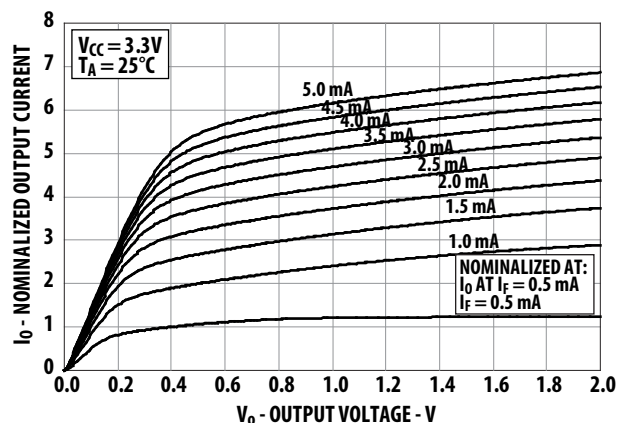


Figure 3 Normalized Current Transfer Ratio vs. Input Diode Forward Current

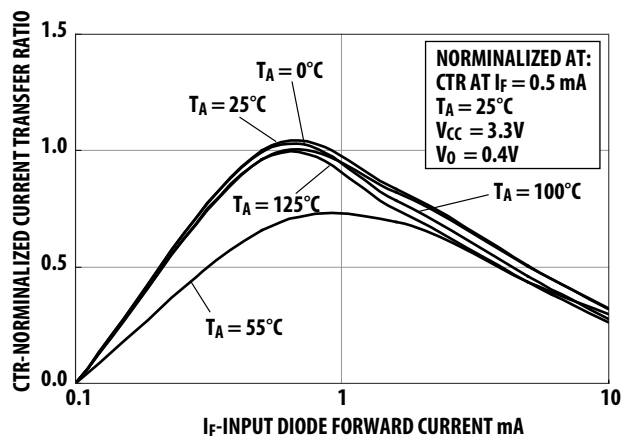


Figure 4 Normalized Supply Current vs. Input Diode Forward Current

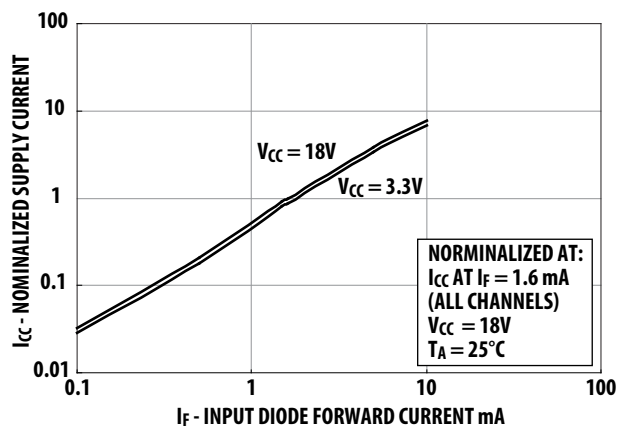


Figure 5 Propagation Delay to Logic Low vs. Input Pulse Period

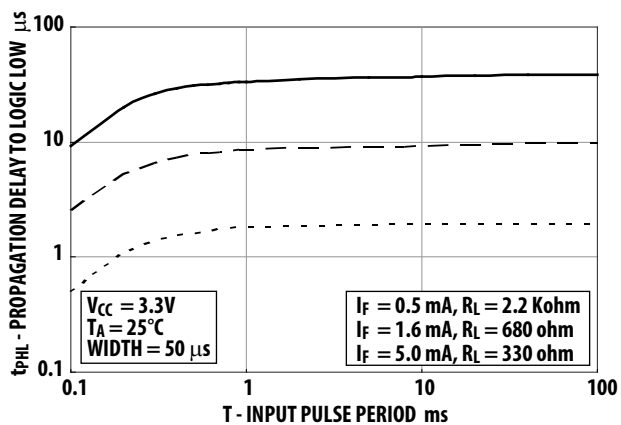


Figure 6 Propagation Delay vs. Temperature

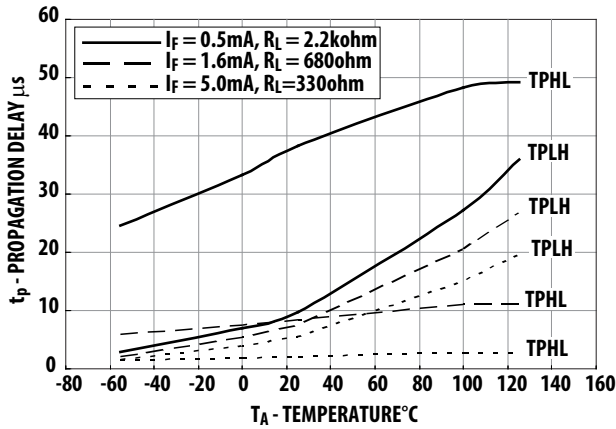


Figure 7 Propagation Delay vs. Input Diode Forward Current

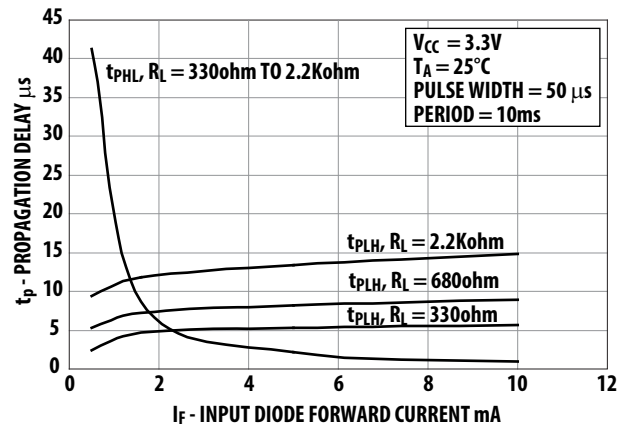
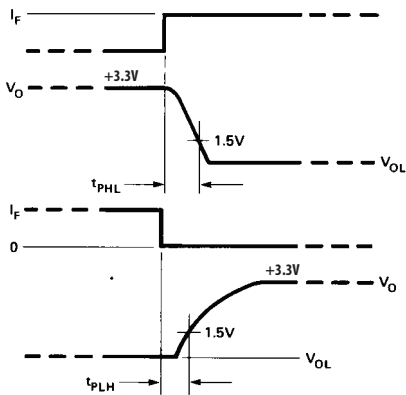
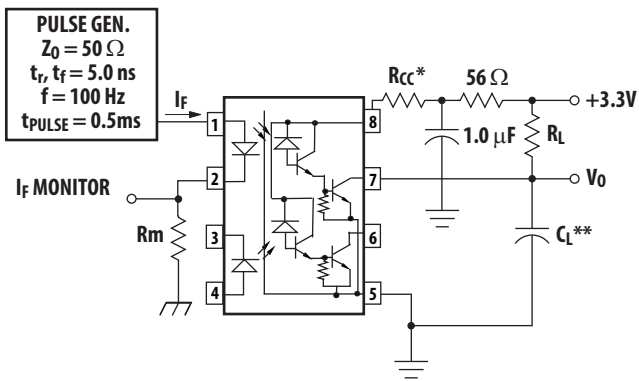


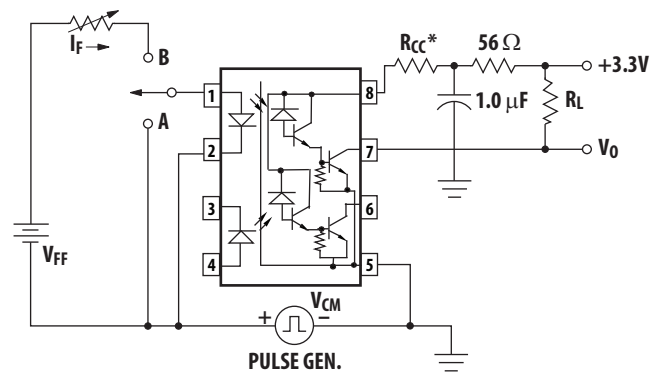
Figure 8 Switching Test Circuit



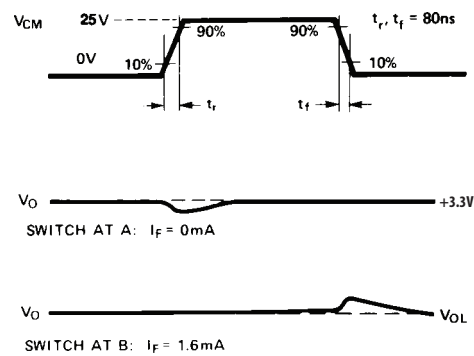
* See [Electrical Characteristics](#), footnote k.

** C_L includes probe and stray wiring capacitance.

Figure 9 Test Circuit for Transient Immunity and Typical Waveforms



* SEE NOTE 11



* See [Electrical Characteristics](#), footnote k.

Figure 10 Recommended Drive Circuitry Using TTL Open-Collector Logic

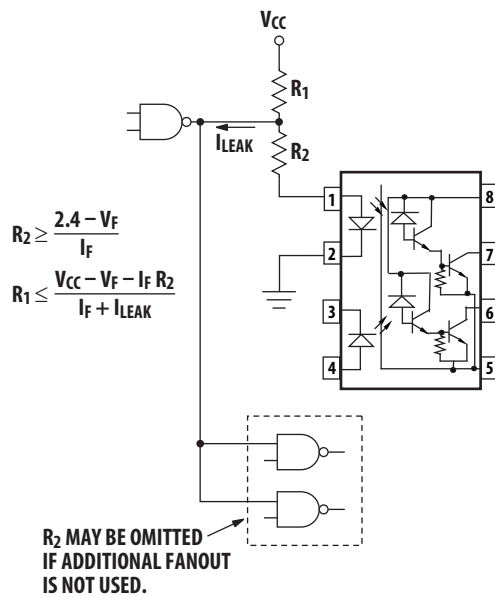
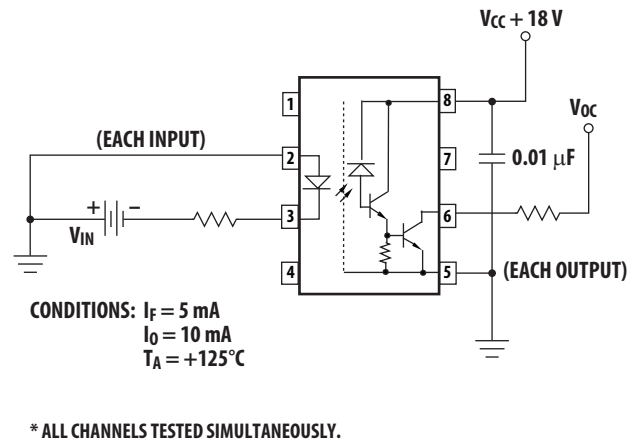


Figure 11 Operating Circuit for Burn-In and Steady State Life Tests



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