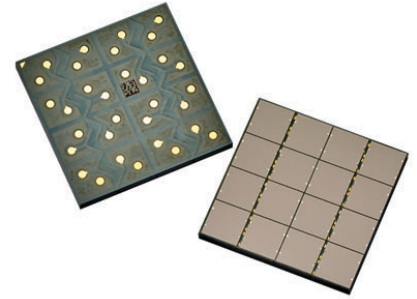


AFBR-S4N44P164M

4×4 NUV-MT Silicon Photomultiplier Array

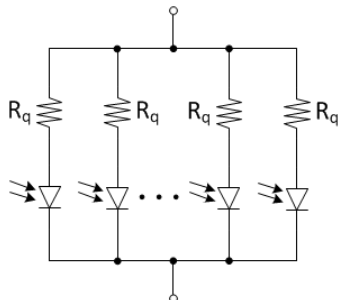


Description

The Broadcom® AFBR-S4N44P164M is a 4×4 silicon photomultiplier (SiPM) array used for ultra-sensitive precision measurements of single photons. This SiPM is based on NUV-MT technology, which combines improved photo-detection efficiency (PDE) with a decreased dark count rate and reduced crosstalk compared to NUV-HD technology. The pitch of SiPMs is 4 mm in both directions. Larger areas can be covered with a pitch of 16 mm by tiling multiple AFBR-S4N44P164M arrays almost without any edge losses. The encapsulation for good mechanical stability and robustness is realized by an epoxy clear mold compound, which is highly transparent down to UV wavelengths, resulting in a broad response in the visible light spectrum with high sensitivity toward the blue and near-UV region of the light spectrum. The array is best suited for the detection of low-level pulsed light sources, especially for the detection of Cherenkov or scintillation light from the most common organic (plastic) and inorganic scintillator materials (for example, LSO, LYSO, BGO, NaI, CsI, BaF, LaBr₃). This product is lead-free and compliant with RoHS.

Block Diagram

Figure 1: AFBR-S4N44P164M Block Diagram of a Single SiPM Element



Features

- 4×4 SiPM array
- Array size: 16.00 mm × 16.00 mm
- High PDE (63% at 420 nm)
- Excellent SPTR and CRT
- Excellent uniformity of breakdown voltage
- Excellent uniformity of gain
- 4-side tileable, with high fill factors
- Cell pitch: 40 μm
- Highly transparent epoxy protection layer
- Operating temperature range from –20°C to +50°C
- RoHS, CFM, and REACH compliant

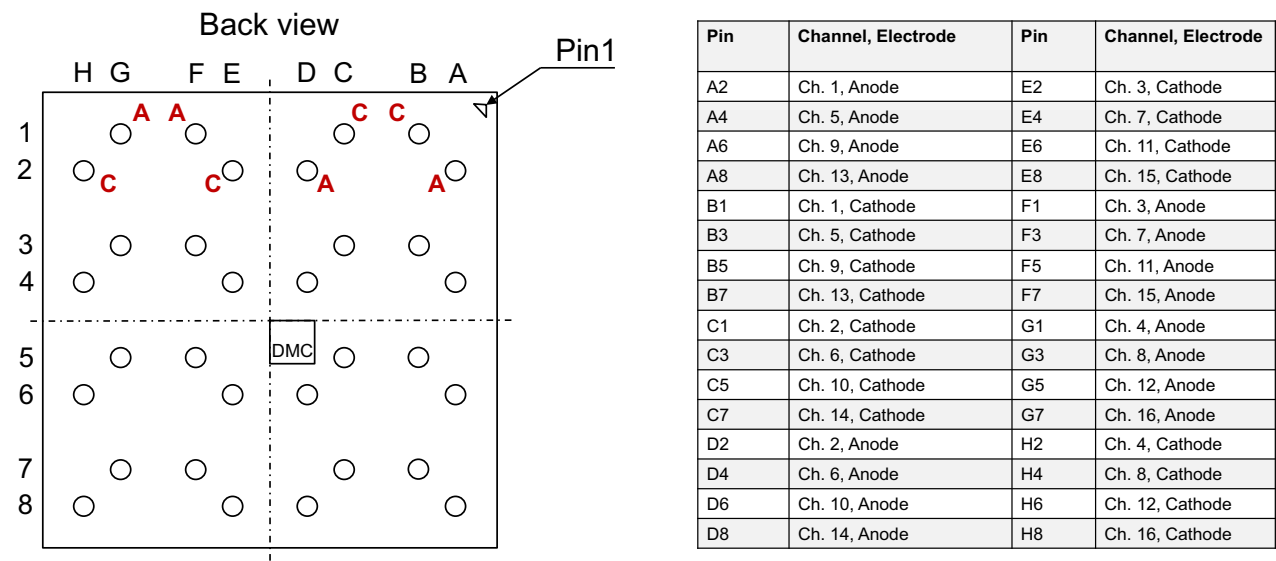
Applications

- X-ray and gamma-ray detection
- Nuclear medicine
- Positron emission tomography
- Safety and security
- Physics experiments
- Cherenkov detection

Pad Layout

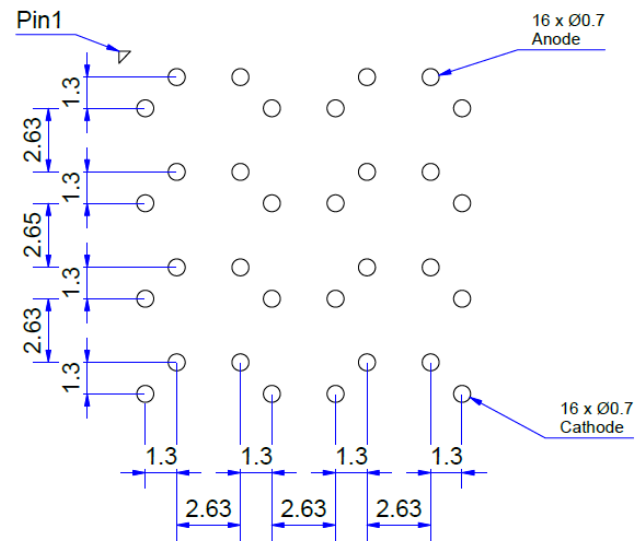
The AFBR-S4N44P164M has 32 signal pins. The anode and the cathode of each SiPM chip can be connected separately. The cathodes do not have a common connection on the module. [Figure 2](#) shows the pad layout, and [Figure 3](#) shows the recommended landing pattern.

Figure 2: Pad Layout



- NOTE:
- 1. Dimensions are in mm.
 - 2. “A” stands for anode, and “C” stands for cathode.

Figure 3: Recommended Landing Pattern



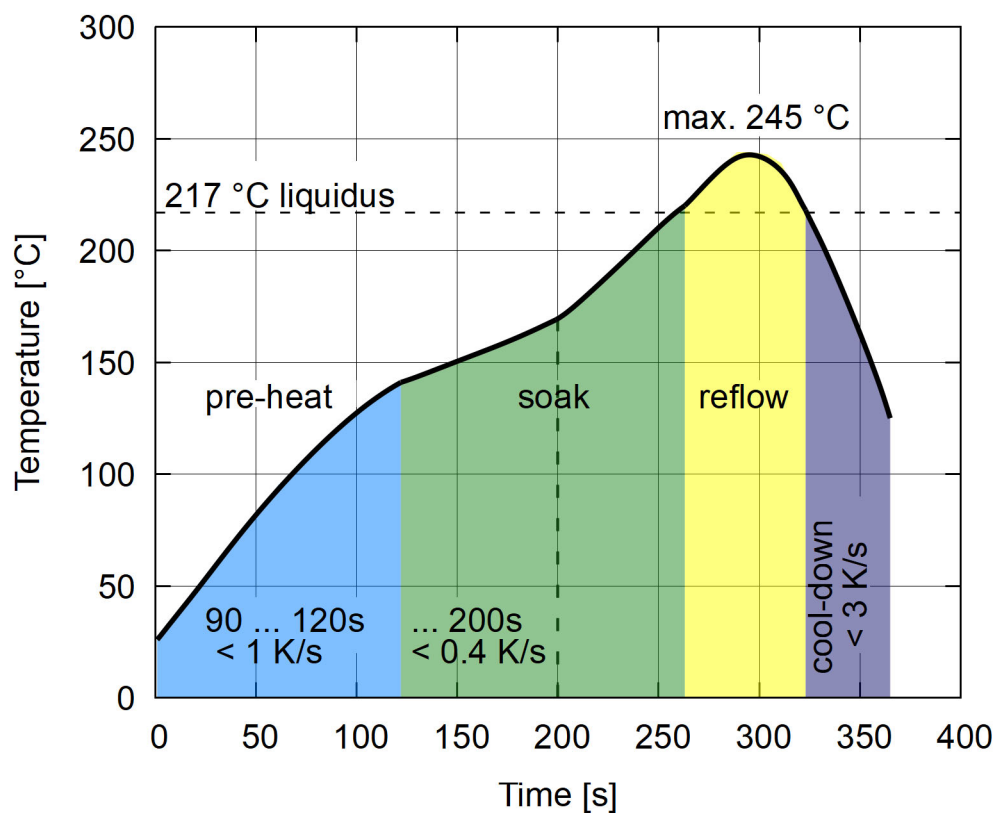
NOTE: Dimensions are in millimeters.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical pins, human-body model (contact ESD)	JESD22-A114	See Absolute Maximum Ratings .
Electrostatic discharge (ESD) to the electrical pins, charged-device model	JESD22-C101F	See Absolute Maximum Ratings .
Restriction of hazardous substances directive	RoHS Directive 2011/65/EU Annex II	Certified compliant.

Reflow Soldering Diagram

Figure 4: Recommended Reflow Soldering Profile



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause damage to the devices. Limits apply to each parameter in isolation. Absolute maximum ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{SG}	-20	+60	°C
Operating Temperature ^a	T_A	-20	+50	°C
Soldering Temperature ^{b, c}	T_{SOLD}	—	245	°C
Lead Soldering Time ^{b, c}	t_{SOLD}	—	60	seconds
Electrostatic Discharge Voltage Capability (HBM)	ESD_{HBM}	—	2	kV
Electrostatic Discharge Voltage Capability (CDM)	ESD_{CDM}	—	500	V
Operating Overvoltage	V_{OV}	—	16	V

a. Biased at constant voltage = 12V above breakdown.

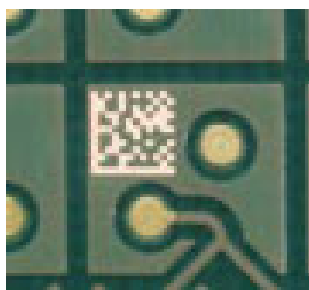
b. The tile is reflow solderable according to the solder diagram shown in [Figure 4](#).

c. In accordance with Broadcom's PCN-272931, there will be a transition in the moisture level definition (MLD) for the NUV-MT SiPM series from MSL 6 to MSL 5. Refer to the label of your devices for details on the MLD. For parts in accordance with MSL 6, baking at 125°C for 16 hours is mandatory before soldering. The floor life is 4 hours at 30°C and 60% relative humidity. For parts with an MLD according to MSL 5, the floor life is 48 hours at 30°C and 60% relative humidity. No baking is required before soldering unless the floor life is exceeded. For more details on soldering and handling, refer to Broadcom's application note [AFBR-S4NxxPyy4M-AN602](#).

Device Identification

Each device can be identified and tracked by a unique data matrix code (DMC) on the back of the PCB. The code is structured as follows: YYWWNNNNNN (Y – year, W – week, N – running number). [Figure 5](#) shows an example DMC.

Figure 5: Example Data Matrix Code for Tile Identification



Single Device Specification

Features are measured at 25°C unless otherwise specified.

Geometric Features

Parameter	Symbol	Value	Unit
Single device area	DA	3.84×3.74	mm ²
Active area	AA	$3.72 \times 3.62 \times 16$	mm ²
Element active area	EAA	3.72×3.62	mm ²
Micro cell pitch	L _{CELL}	40	μm
Number of micro cells per element	N _{CELLS}	8334	—

Optical and Electrical Features

Features are measured at 12V OV and 25°C unless otherwise specified.

Parameter	Symbol	Min.	Typ. ^a	Max.	Unit	Reference Plots
Spectral range	λ	250	—	900	nm	Figure 6
Peak sensitivity wavelength	λ_{PK}	—	420	—	nm	Figure 6
Breakdown voltage	V _{BD}	32	32.5	33	V	Figure 8
Temperature coefficient of breakdown voltage	$\Delta V_{BD}/\Delta T$	—	30	—	mV/°C	—
Photo-detection efficiency ^b	PDE	—	63	—	%	Figure 6 , Figure 7
Dark current per element	I _D	—	3.3	—	μA	Figure 8
Dark count rate per element ^c	DCR	—	1.7	—	Mcps	Figure 9
Dark count rate per unit area	DCR _{mm2}	—	125	—	kcps/mm ²	—
Gain	G	—	7.3	—	$\times 10^6$	Figure 10
Optical crosstalk	P _{XTALK}	—	23	—	%	Figure 11
Afterpulsing probability	P _{AD}	—	< 1	—	%	—
Recharge time constant	T _{FALL}	—	55	—	ns	Figure 12
Nominal terminal capacitance ^d	C _T	—	580	—	pF	—
Temperature coefficient of gain ^e	$\Delta G/\Delta T$	—	1.46	—	$\times 10^4/^\circ\text{C}$	—

a. Measured at 12V OV.

b. Measured at peak sensitivity wavelength. The measurement does not include correlated noise, such as afterpulsing or optical crosstalk.

c. Measured at 0.5-p.e. amplitude. The measurement does not include delayed correlated events.

d. Measured using the input sine wave with f = 200 kHz and V_{in} = 500 mV.

e. Calculated from the gain dependence on V and the breakdown voltage temperature coefficient: $dG/dT = dG/dV \times dV_{BD}/dT$.

Reference Plots

Features are measured at 25°C unless otherwise specified. The plotted data represents typical values per single element.

Figure 6: PDE vs. Wavelength

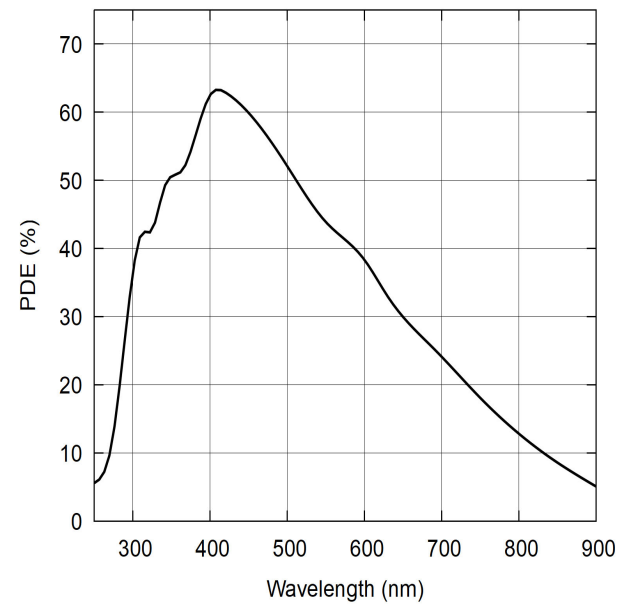


Figure 7: PDE at Peak λ vs. OV (Overmolded Package)

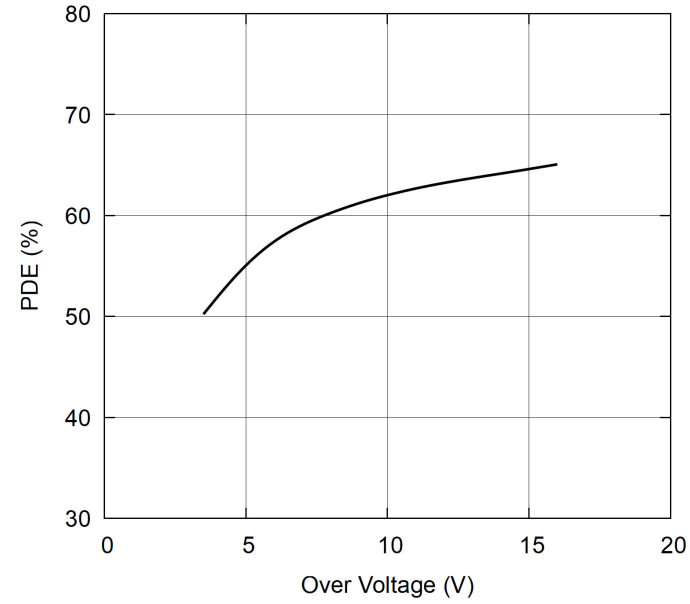


Figure 8: Reverse IV Curve

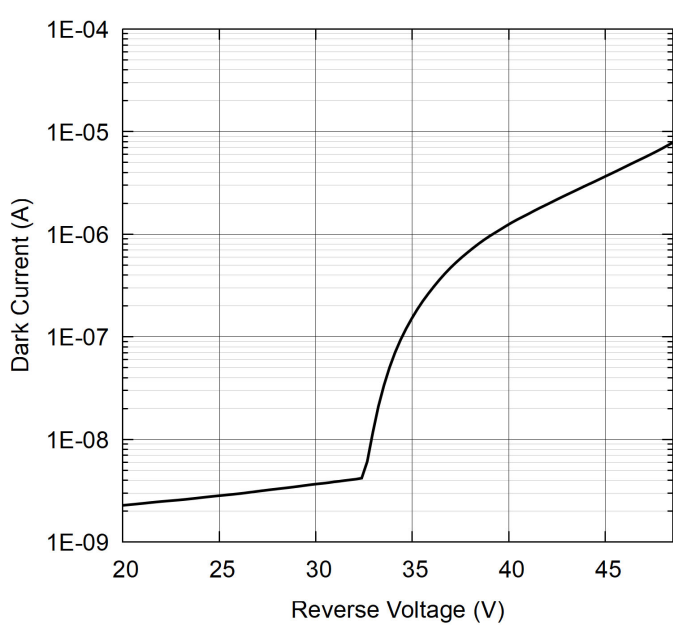


Figure 9: Dark Count Rate vs. OV

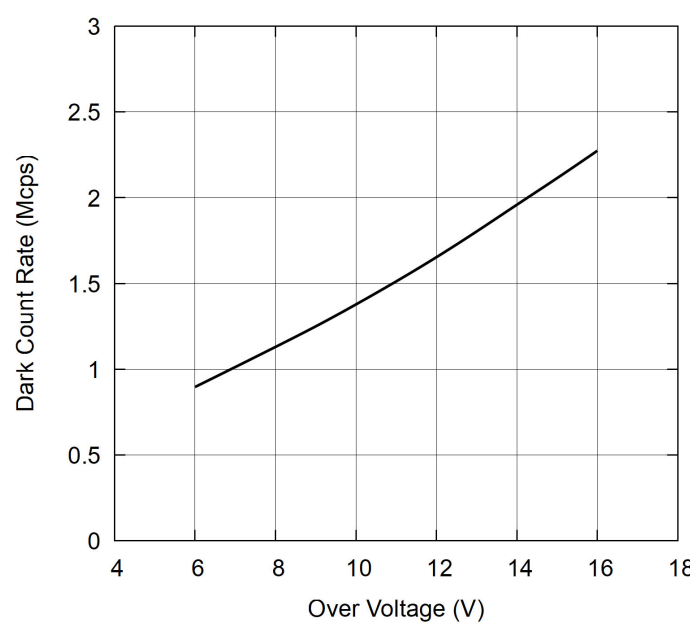


Figure 10: Gain vs. OV

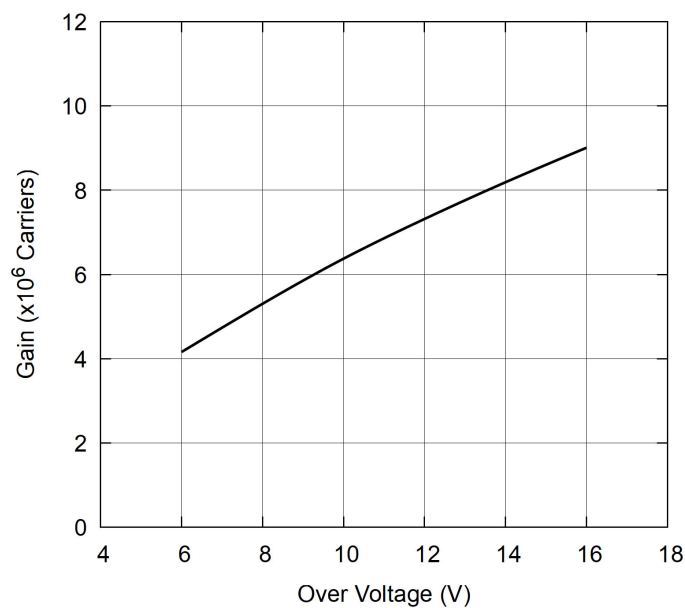


Figure 11: Correlated Noise vs. OV

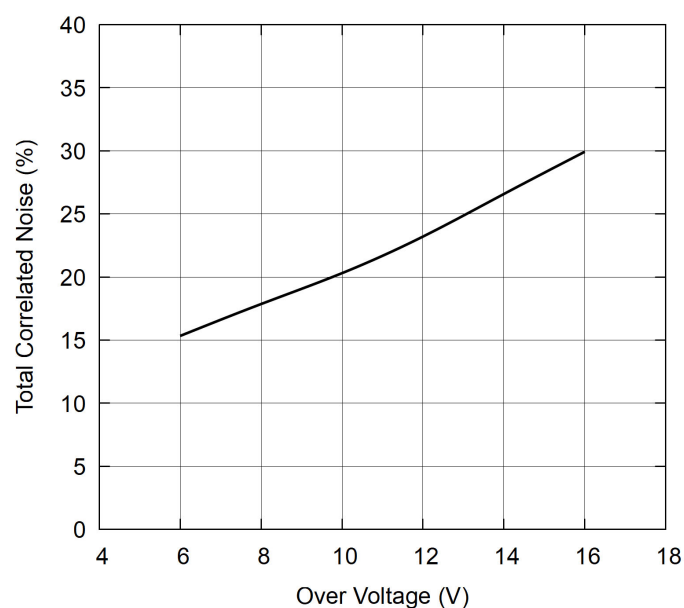
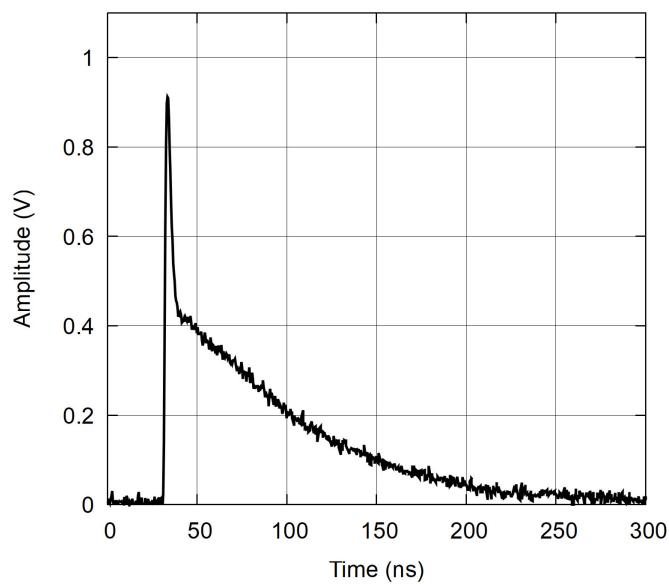


Figure 12: Example Signal Measured at 12V OV



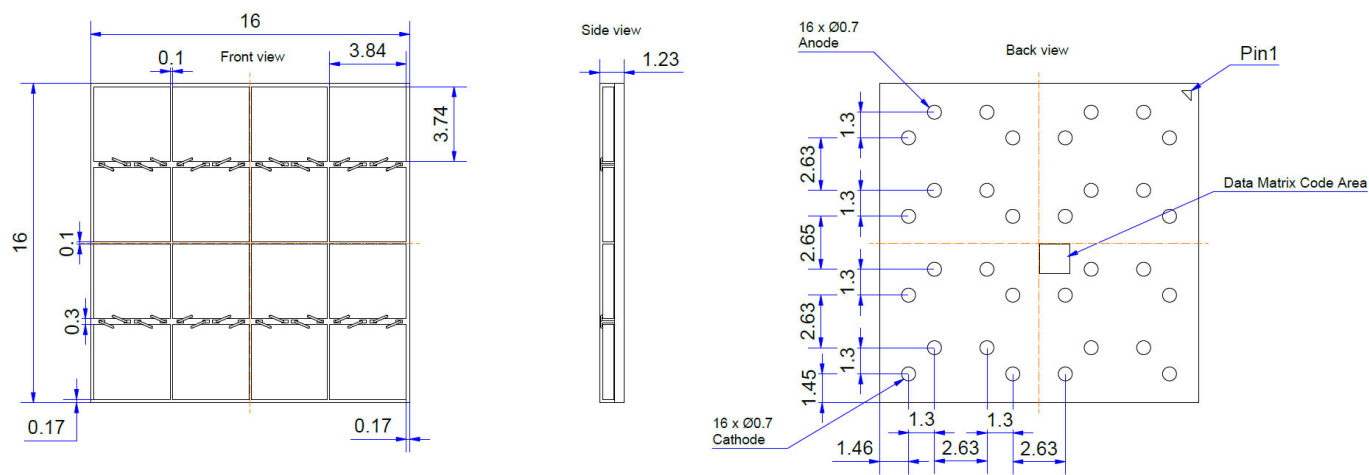
Array Specification

The array consists of 16 wire-bonded SiPM dies arranged in a 4x4 matrix with a package fill factor of 84% (active area versus total package area).

Parameter	Symbol	12V OV			Unit
		Min.	Typ.	Max.	
Dark current sum at 12V OV	ΣI_D	—	53	—	μA

Mechanical Data – Package Outline

Figure 13: Package Outline Drawing (Dimensions in mm, Numbers Rounded to Two Decimal Places)



- NOTE:
- 1. Dimensions are in millimeters.
 - 2. Nominal values rounded to two decimal places – Suppression of following zeros.

The AFBR-S4N44P164M is shipped in JEDEC trays with a standard quantity of 40 pieces per tray. The tray is filled starting at the chamfer (bottom left). A second tray is used as a cover.

[illegible]

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