Data Sheet

ACFJ-3262T

Automotive Dual-Channel 10-Amp Peak Gate Drive Optocoupler for MOSFET/IGBT with Rail-to-Rail Output Voltage in SO-24 Package

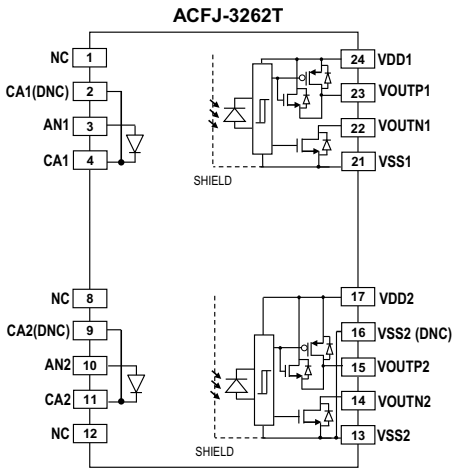
Description

The Broadcom® ACFJ-3262T driver is a 10A peak, rail-to-rail output Automotive R^{2}Coupler™ gate drive optocoupler. The ACFJ-3262T comes in a compact, surface-mountable SO-24 package with two independent isolated channels for space-savings. It provides an isolation voltage of 5k V_{rms} between input and output channels and differential voltage of 900V_{DC} between two output channels.

The ACFJ-3262T is primarily designed with high peak driving current capability to ensure optimum performance for direct driving MOSFET or IGBT in various applications. The ACFJ-3262T features fast propagation delay and tight channel-to-channel skew, which make it ideal for driving SiC MOSFET and IGBTs at high frequency DC-DC and AC-DC converters.

Broadcom R^{2}Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Figure 1: Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: –40°C to +125°C
- High output driving current: 10A (typical)
- Rail-to-rail output voltage
- Propagation delay: 95 ns max.
- Channel-to-channel skew: 9 ns max.
- Wide operating supply (V_{DD}) range: 10V to 25V
- Undervoltage lock-out (UVLO) protection with hysteresis
- Low supply current allows bootstrap half-bridge topology: I_{DD} = 4 mA max.
- Common mode transient immunity (CMTI) > 100 kV/µs at V_{CM} = 1000V
- High noise immunity
  - Direct LED input with low input impedance and low noise sensitivity
- Dual-channel in SO-24 package with 8.3-mm creepage and clearance
- 2.8-mm creepage between two output drivers
- Regulatory approvals:
  - UL1577 5k V_{rms} for 1 min
  - CAN/CSA-C22.2 No. 62368-1
  - DIN/EN 607474-5-5 V_{IORM} = 1230 V_{PEAK}

Applications

- Powertrain DC-DC converter
- EV/PHEV onboard charger
- Automotive isolated MOSFET/IGBT gate drive for inverter and HVAC

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACFJ-3262T	-000E	SO-24	X		X	45 per tube
	-500E		X	X	X	850 per reel

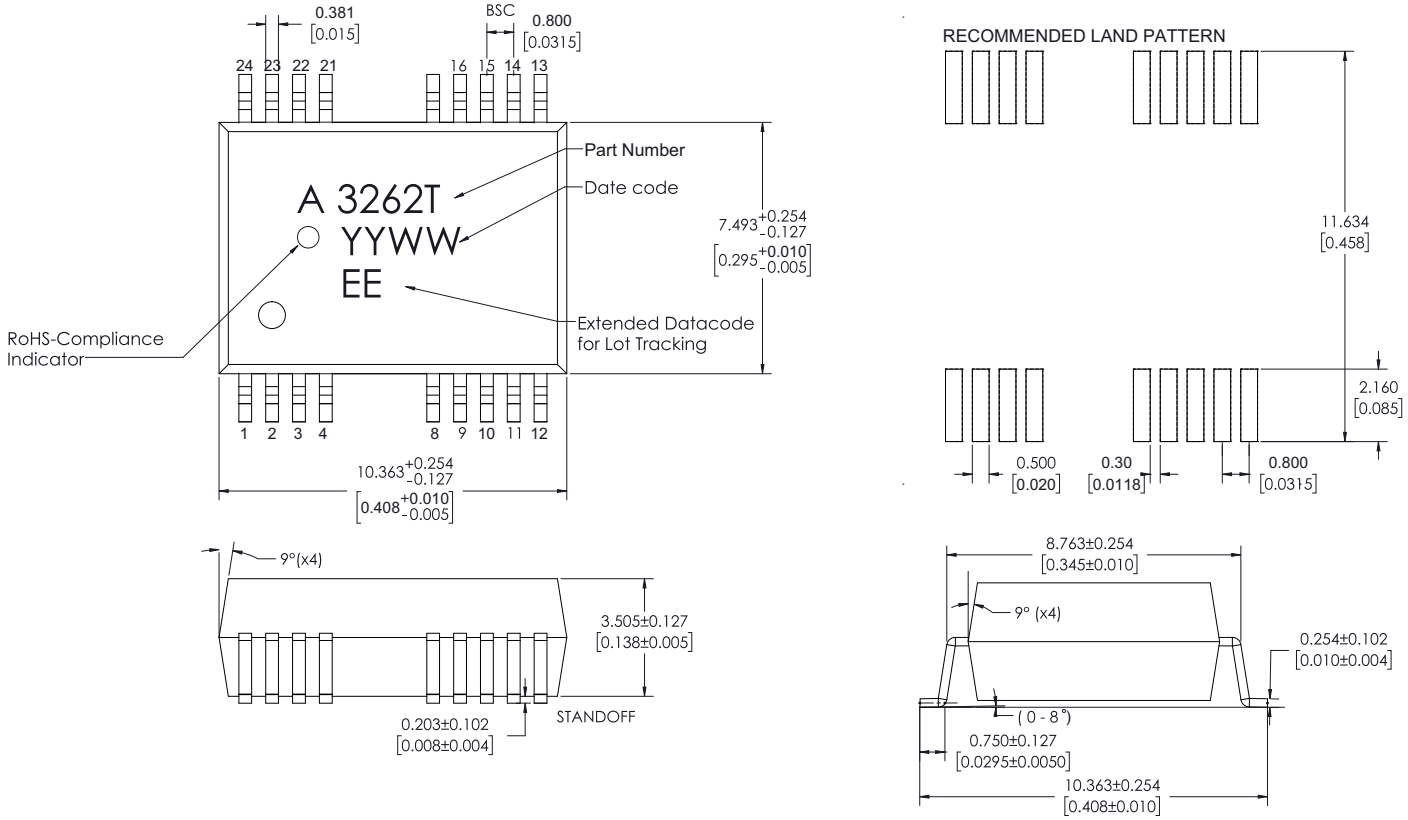
To order, choose a part number from the part number column and combine it with the desired option from the option column to form an order entry.

Example: ACFJ-3262T-500E to order the product of SO-24 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Options data sheets are available. Contact your Broadcom sales representative or an authorized distributor for information.

Package Outline Drawing

Figure 2: ACFJ-3262T



NOTE:

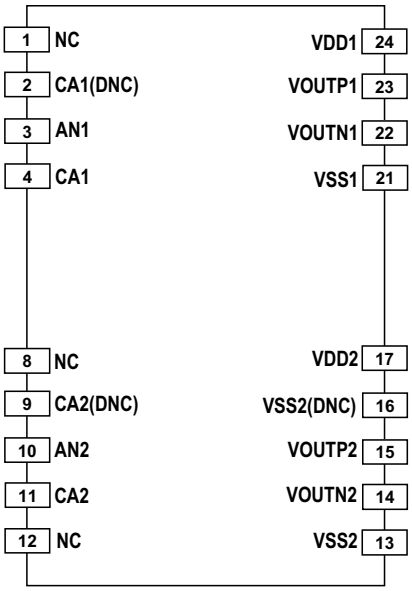
1. Dimensions are in millimeters (inches).
2. Lead coplanarity = 0.10 mm (0.004 inches), Mold Flash on each side = 0.203 mm (0.008 inches) max. Customers should contact their PCB manufacturers for solder-mask tolerance between and around signal pads.

Product Overview Description

The ACFJ-3262T (shown in Figure 1) is a dual-channel, high peak driving current, rail-to-rail output isolated MOSFET/IGBT gate driver in compact SO-24 package. It can operate over wide VDD range of 10V to 25V with undervoltage lock-out protection. The ACFJ-3262T has two separate source and sink outputs to facilitate tuning of turn-on and turn-off gate resistors. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increasing noise immunity.

Package Pinout

Figure 3: ACFJ-3262T Pinout



Pin Descriptions

Pin	Name	Function	Pin	Name	Function
1	NC	No connection	24	VDD1	Driver 1 supply voltage
2	CA1(DNC)	Cathode 1 (Do not connect externally.)	23	VOUTP1	Driver 1 output to turn on gate of MOSFET/IGBT
3	AN1	Anode 1	22	VOUTN1	Driver 1 output to turn off gate of MOSFET/IGBT
4	CA1	Cathode 1	21	VSS1	Driver 1 Ground (Connect a decoupling capacitor to VSS1 and VDD1 locally and closely to the device.)
8	NC	No connection	17	VDD2	Driver 2 supply voltage
9	CA2 (DNC)	Cathode 2 (Do not connect externally.)	16	VSS2 (DNC)	Driver 2 Ground (Additional pin for VSS2 lead frame support. Internally connected to pin 13. Do not connect externally to avoid ground loop.)
10	AN2	Anode 2	15	VOUTP2	Driver 2 output to turn on gate of MOSFET/IGBT
11	CA2	Cathode 2	14	VOUTN2	Driver 2 output to turn off gate of MOSFET/IGBT
12	NC	No connection	13	VSS2	Driver 2 Ground (Connect a decoupling capacitor to VSS2 and VDD2 locally and closely to the device.)

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used.

Regulatory Information

The ACFJ-3262T is approved by the following organizations:

- **UL** – Recognized under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}
- **CAN/CSA** – CAN/CSA-C22.2 No. 62368-1
- **IEC/DIN/EN** – IEC 60747-5-5, DIN/EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤ 150 V_{rms} For Rated Mains Voltage ≤ 300 V_{rms} For Rated Mains Voltage ≤ 600 V_{rms} For Rated Mains Voltage ≤ 1000 V_{rms}		 I – IV I – IV I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values – maximum values allowed in the event of a failure[b] Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 400 1200	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

b. Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface mount classification is Class A in accordance with CECCOO802.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.3	mm	Through insulation, distance conductor to conductor, usually the straight-line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 600	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		I	—	Material Group (DIN VDE 0110).

Absolute Maximum Ratings

Unless otherwise specifies, all voltages at output IC reference to V_{SS}.

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
IC Junction Temperature	T_J	—	150	°C	
Average LED Input Current	$I_{F(AVG1)}$, $I_{F(AVG2)}$	—	20	mA	
Peak Transient LED Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN1)}$, $I_{F(TRAN2)}$	—	1	A	
Reverse Input Voltage ($V_{CA} – V_{AN}$)	V_{R1}, V_{R2}	—	6	V	
Total Output Supply Voltage	($V_{DD1} – V_{SS1}$), ($V_{DD2} – V_{SS2}$)	–0.5	35	V	
High Side Output Voltage	V_{OH1}, V_{OH2}	–0.5	V_{DD}	V	
Low Side Output Voltage	V_{OL1}, V_{OL2}	–0.5	V_{DD}	V	
Output Sourcing Current	I_{OH1}, I_{OH2}	–7	—	A	a
Output Sinking Current	I_{OL1}, I_{OL2}	—	7	A	a
Output IC Power Dissipation	P_O	—	1000	mW	b
LED Power Dissipation	P_{LED}	—	100	mW	c
ESD Immunity	V_{ESD}	—	2.5	kV	d
		—	750	V	e
		—	500	V	f

a. Maximum pulse width = 100 ns and duty cycle at 0.4%.
b. Output IC power dissipation is derated linearly above 105°C from 1000 mW to 600 mW at 125°C.
c. Input LED power dissipation is derated linearly above 105°C from 100 mW to 80 mW at 125°C.
d. Human body model (HBM) per AEC Q100-002, all pins.
e. Charge device model (CDM) per AEC Q100-011, all corner pins.
f. Charge device model (CDM) per AEC Q100-011, all pins.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_A	–40	125	°C	
Total Output IC Supply Voltage	$(V_{DD} – V_{SS})$	10	25	V	
Input LED Turn On Current (ON)	$I_{F(ON)}$	10	16	mA	
Input LED Turn Off Voltage $(V_{AN} – V_{CA})$	$V_{F(OFF)}$	–5.5	0.8	V	
Output IC Supply Decoupling Capacitor $(V_{DD} – V_{SS})$	C_{VDD}	10	—	µF	a
Minimum Input Pulse Width	$t_{ON(LED)}$	100	—	ns	b

a. It is recommended to check external decoupling capacitor derating guidelines.

b. Minimum input pulse width for a guarantee output pulse under no load condition.

Electric Specifications (DC)

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions. All typical values are at T_A = 25°C, $V_{DD} – V_{SS}$ = 15V, V_{SS} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
$I_{OH1(PEAK)}$, $I_{OH2(PEAK)}$ Peak Sourcing Current	$I_{OH(PEAK)}$	—	–10	–6	A	$V_{DD} – V_{OUTP}$ = 15V	15	a
$I_{OL1(PEAK)}$, $I_{OL2(PEAK)}$ Peak Sinking Current	$I_{OL(PEAK)}$	6	9	—	A	$V_{OUTN} – V_{SS}$ = 15V	14	a
$R_{DS1,OH}$, $R_{DS2,OH}$ Output Resistance at High State	$R_{DS,OH}$	0.4	0.8	1.3	Ω	I_{OH} = –3A		b
$R_{DS1,OL}$, $R_{DS2,OL}$ Output Resistance at Low State	$R_{DS,OL}$	0.2	0.6	1.2	Ω	I_{OL} = 3A		b
V_{OH1}, V_{OH2} Output Voltage at High State	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.06	—	V	I_F = 10 mA, I_{OH} = –10 mA		c
V_{OL1}, V_{OL2} Output Voltage at Low State	V_{OL}	—	0.06	0.3	V	V_F = 0V, I_{OL} = 100 mA		
V_{UVLO1+}, V_{UVLO2+} UVLO Low to High Threshold	V_{UVLO+}	8.2	8.6	9.1	V	I_F = 10 mA, V_{OH} > 5V		
$V_{UVLO1–}$, $V_{UVLO2–}$ UVLO High to Low Threshold	$V_{UVLO–}$	7.2	7.6	8.0	V	I_F = 10 mA, V_{OL} < 5V		
V_{UVLO1_HYS}, V_{UVLO2_HYS} UVLO Hysteresis	V_{UVLO_HYS}	0.8	1	1.3	V			
I_{DDH1}, I_{DDH2} High Level Supply Current	I_{DDH}	—	2.8	4	mA	I_F = 10 mA, No Load	13,17	
I_{DDL1}, I_{DDL2} Low Level Supply Current	I_{DDL}	—	2.7	4	mA	V_F = 0V, No Load	12,17	
I_{TH1+}, I_{TH2+} LED Current Low to High Threshold	I_{TH+}	0.5	2.6	7	mA			
$I_{TH1–}$, $I_{TH2–}$ LED Current High to Low Threshold	$I_{TH–}$	—	2.1	6	mA			
I_{TH1_HYS}, I_{TH2_HYS} LED Turn on Current Hysteresis	I_{TH_HYS}	—	0.5	—	mA			

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
V_{F1}, V_{F2} LED Forward Voltage Drop	V_F	1.25	1.55	1.85	V	I_F = 10 mA	18,16	
$\Delta V_{F1}/\Delta T_{A1}$, $\Delta V_{F2}/\Delta T_{A2}$ Temperature Coefficient of V_{F1} ,V_{F2}	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C	I_F = 10 mA		
V_{FHL1}, V_{FHL2} LED High to Low Threshold Voltage	V_{FHL}	0.8	—	—	V			
V_{BR1}, V_{BR2} LED Reverse Breakdown Voltage ($V_{CA} – V_{AN}$)	V_{BR}	6	—	—	V	I_F = –100 µA		
C_{IN1}, C_{IN2} LED Input Capacitance	C_{IN}	—	30	—	pF			

a. Short circuit pulsed current at $V_{DD} – V_{SS}$ = 30V and pulse duration less than 1 µs.

b. Output is sourced at –3A or 3A with maximum pulse width of 10 µs.

c. V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{DD} as I_{OH} approaches zero amps.

Switching Specifications (AC)

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions. All typical values at T_A = 25°C, $V_{DD} – V_{SS}$ = 15V, V_{SS} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
t_{PLH1}, t_{PLH2} Input Pulse to High Level Output Propagation Delay Time	t_{PLH}	45	68	95	ns	C_L= 2.2 nF, f = 20 kHz, Duty cycle = 50% R_G = 2Ω R_{IN} = 240Ω V_{IN} = 5V $V_{DD} – V_{SS}$ = 15V	4, 5, 8	
t_{PHL1}, t_{PHL2} Input Pulse to Low Level Output Propagation Delay Time	t_{PHL}	45	67	95	ns		4, 5, 9	
PWD_1, PWD_2 Pulse Width Distortion	PWD	–20	1	20	ns		10	a
DTD_1, DTD_2 Dead Time Distortion Caused by Any Two Parts	DTD	–30	1	30	ns			b
T_{CSK1}, T_{CSK2} Channel-to-Channel Skew	T_{CSK}	–9	1	9	ns			c
t_{R1}, t_{R2} Output Rise Time (20% to 80%)	t_R	—	7	15	ns		5	
t_{F1}, t_{F2} Output Fall Time (80% to 20%)	t_F	—	7	15	ns		5	
$\|CM_{H1}\|$, $\|CM_{H2}\|$ Output High Level Common Mode Transient Immunity	$\|CM_H\|$	100	—	—	kV/µs	T_A = 25°C, V_{DD} = 15V, V_{CM} = 1 kV, with current limiting resistors at both AN and CA nodes	6	d
$\|CM_{L1}\|$, $\|CM_{L2}\|$ Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	100	—	—	kV/µs		7	e

a. Pulse width distortion (PWD) is defined as $t_{PHL} – t_{PLH}$ for the same part and channel.

b. Dead time distortion (DTD) is defined as $t_{PLH} – t_{PHL}$ between any two parts and channels under the same test condition. A negative DTD reduces original system dead time, while a positive DTD increases original system dead time.

c. Channel-to-channel skew (T_{CSK}) is defined as propagation delay difference for the same part between Channel 1 and Channel 2, on the same rising or falling edge (t_{PLH}/ t_{PHL}) under the same test condition.

d. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state (that is, V_O > 10V).

e. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (that is, V_O < 1.0V).

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH < 50%, t = 1 min. T_A = 25°C	a, b
Resistance (Input-Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V_{DC}	c
Capacitance (Input-Output)	C_{I-O}	—	0.8	—	pF	f = 1 MHz	c

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

b. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second.

c. The device is considered a two-terminal device: pins 1 to 12 are shorted together, and pins 13 to 24 are shorted together.

Parameter Measurements

Figure 4 depicts the test setup to measure the gate driver's propagation delay. These settings correlate to the loading effects found in most automotive applications.

Figure 4: Propagation Delay Measurement Test Setup

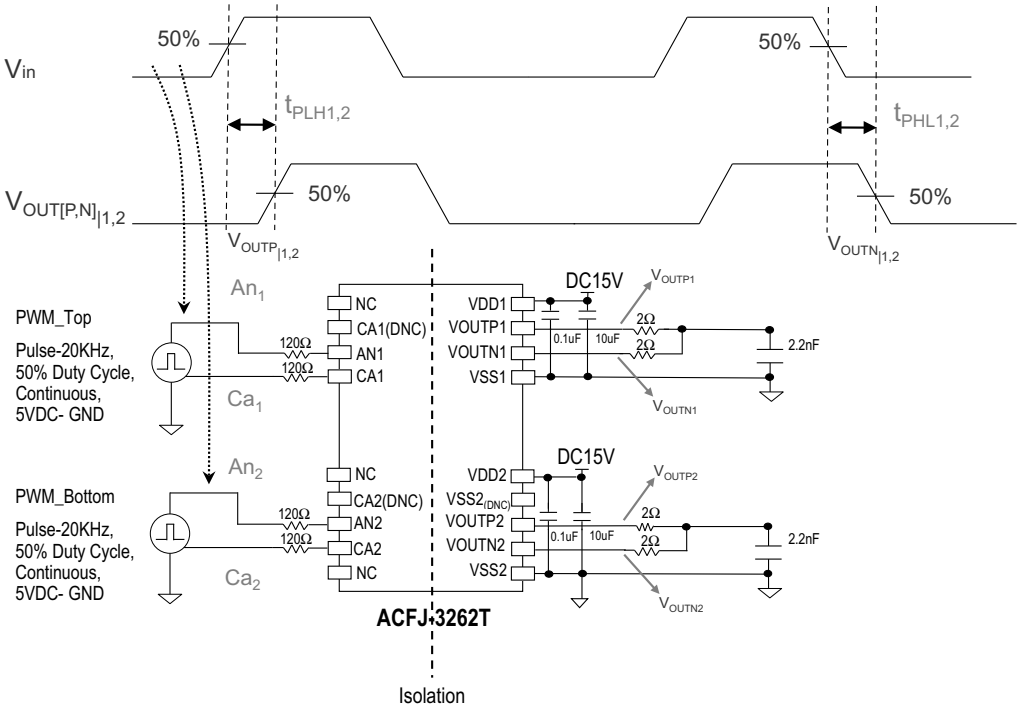
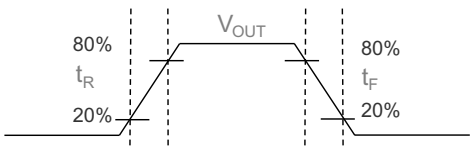


Figure 5 shows the 20% to 80% rise and fall time measurement.

Figure 5: Rise and Fall Time Measurement



The common mode rejection test circuitries are shown in the following figures. Both CMR High (Figure 6) and Low (Figure 7) V_O are probed in the presence of V_{CM} at 1000V.

Figure 6: CMR V_O High Test Circuit

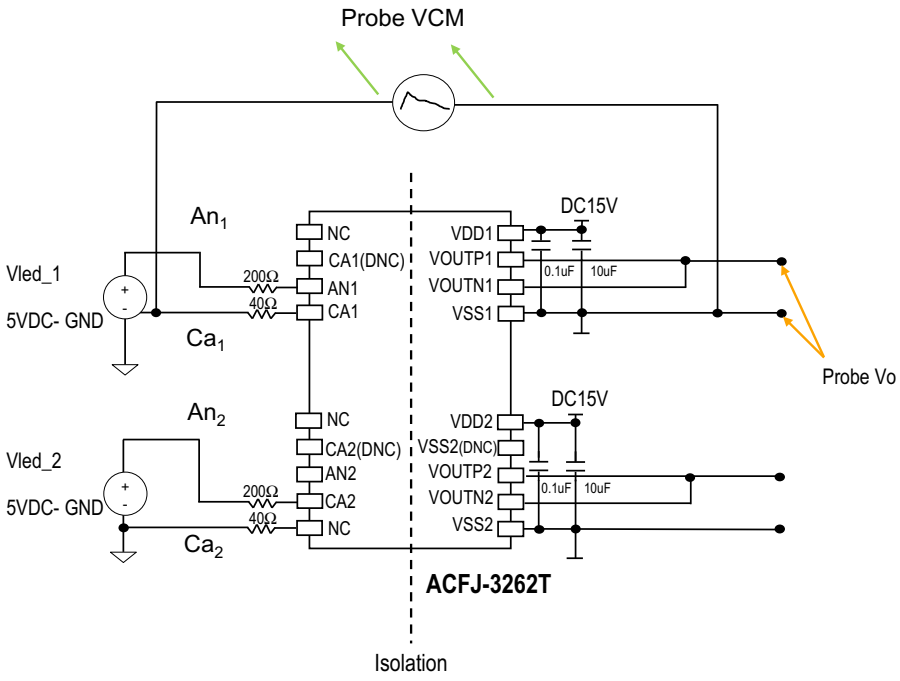
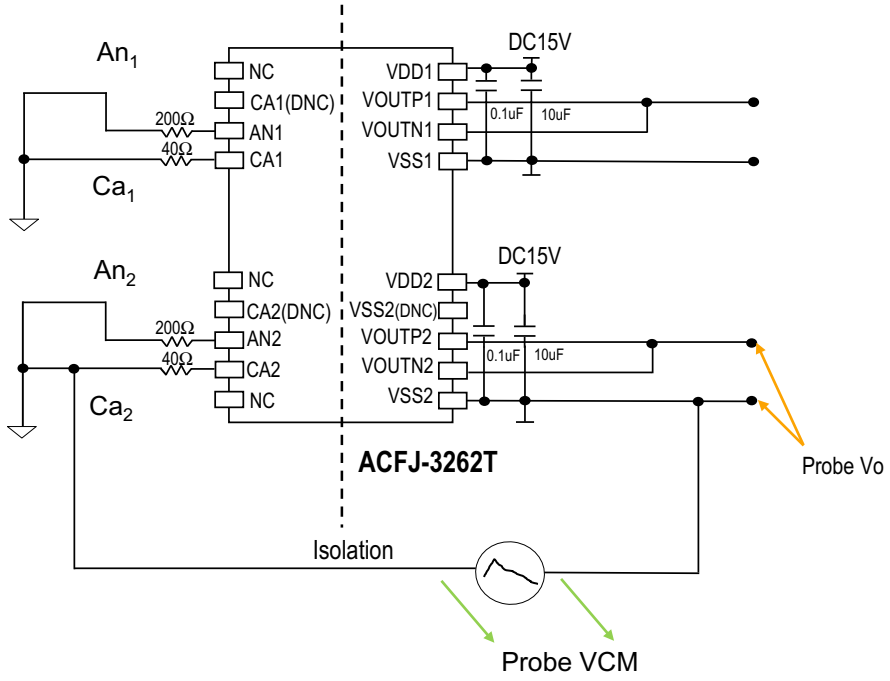


Figure 7: CMR V_O Low Test Circuit



Typical Performance Plots

T_A = 25°C, V_{DD} – V_{SS} = 15V, V_S = V_{SS} = 0V. With capacitance load of 2.2 nF, unless otherwise noted.

Figure 8: t_{PLH} vs Temperature (V_{OUTP})

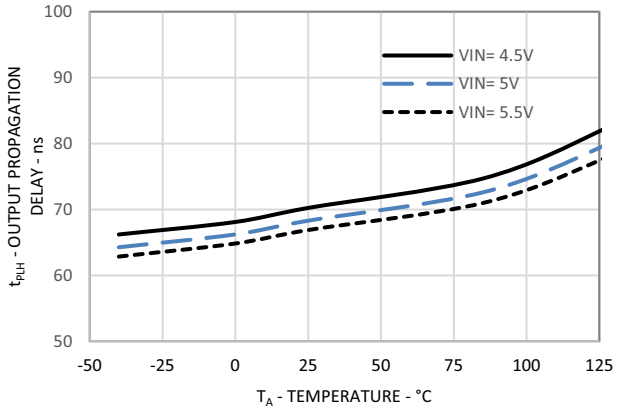


Figure 9: t_{PHL} vs Temperature (V_{OUTN})

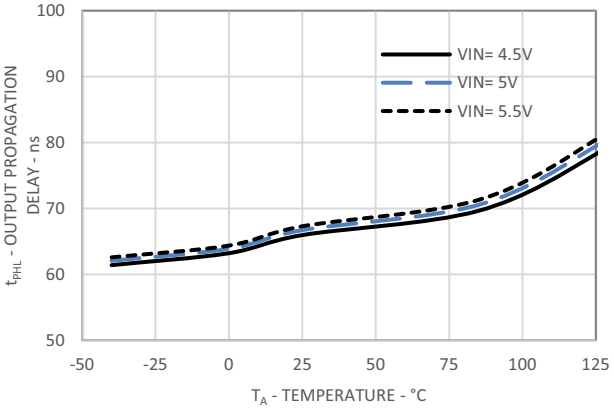


Figure 10: Pulse Width Distortion vs Temperature

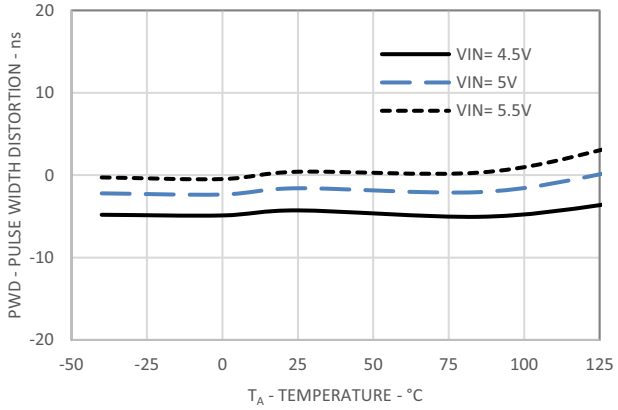


Figure 11: Channel-to-Channel Skew vs Temperature

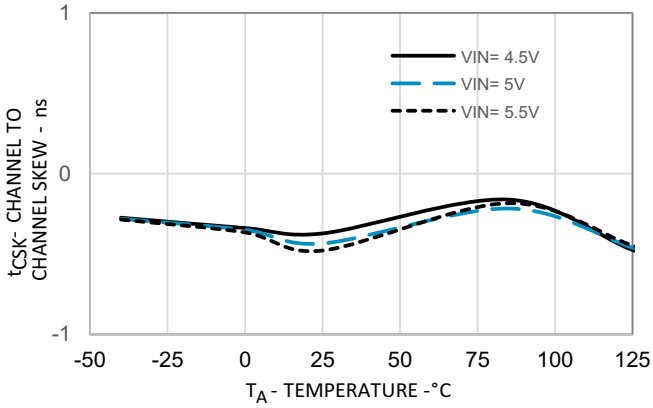


Figure 12: I_{DDL} vs Temperature

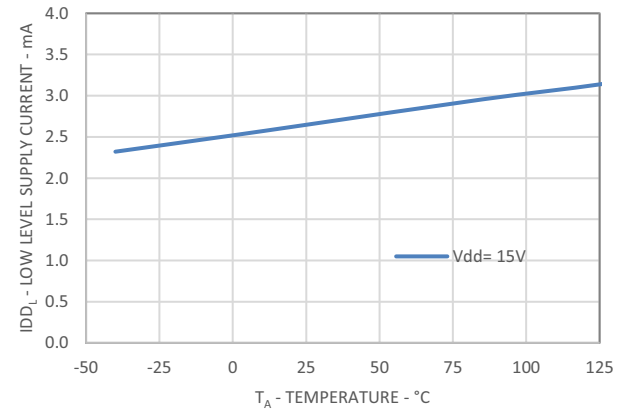


Figure 13: I_{DDH} vs Temperature

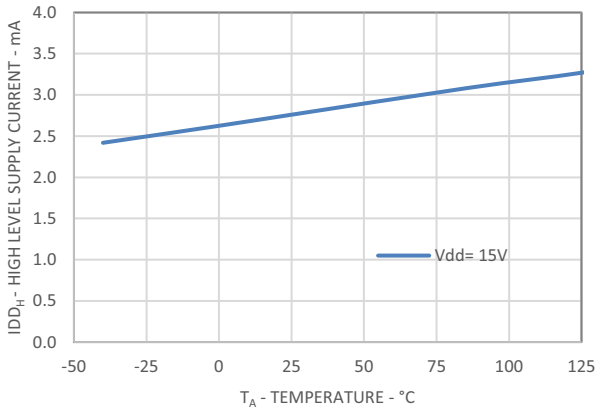


Figure 14: I_{OL} vs V_{OUTN}

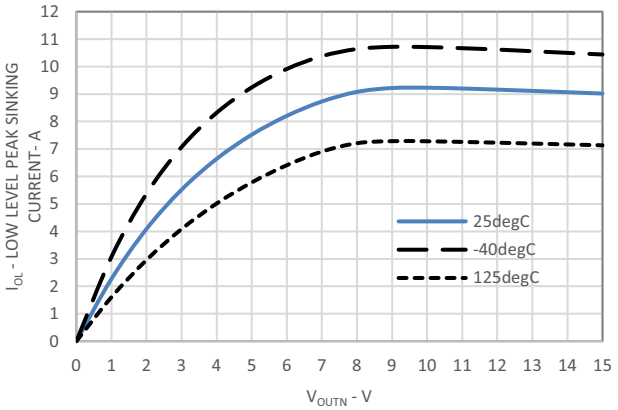


Figure 15: I_{OH} vs (V_{DD} – V_{OUTP})

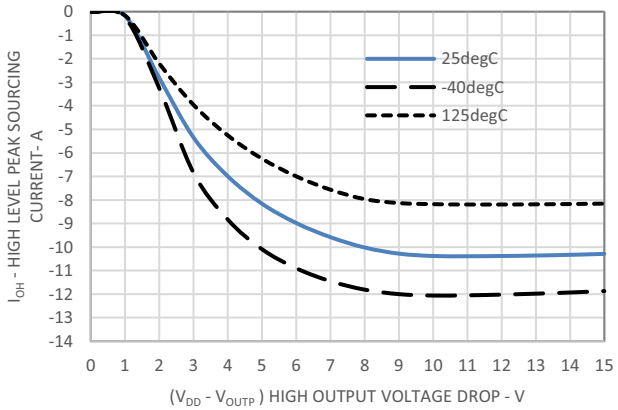


Figure 16: I_F vs V_F

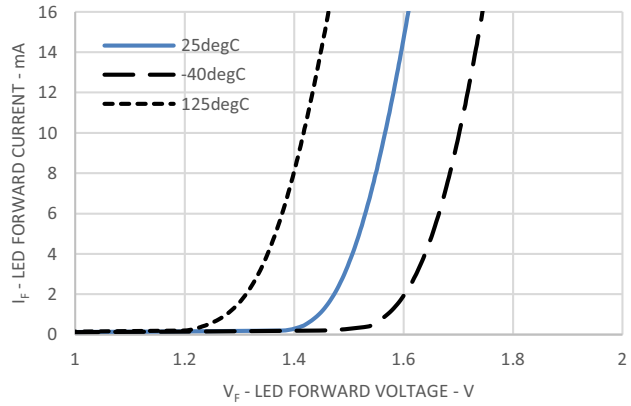


Figure 17: Supply Current vs. Supply Voltage

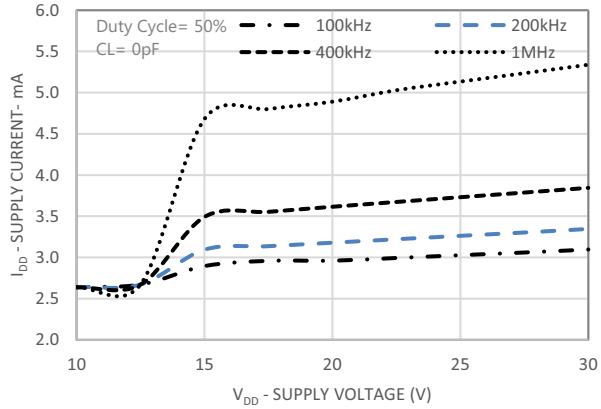
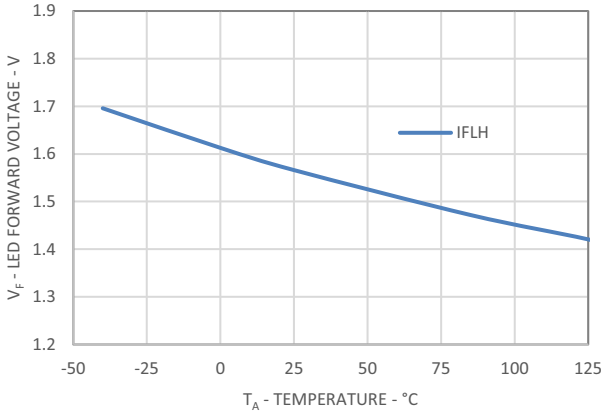


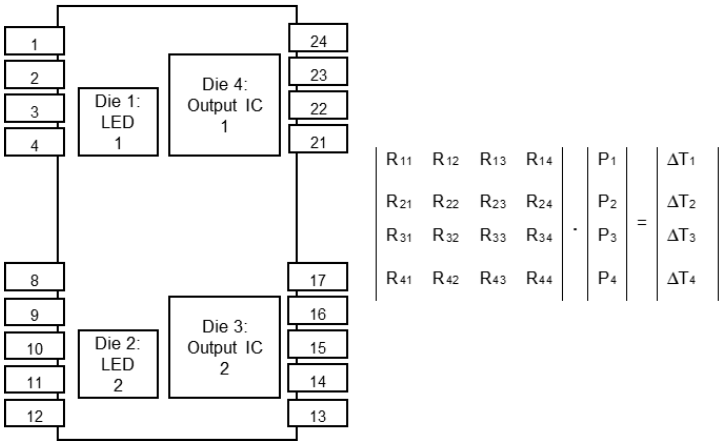
Figure 18: V_F vs Temperature



Thermal Resistance Model for ACFJ-3262T

Figure 19 shows the diagram for thermal resistance measurement. This is a multichip package with four heat sources. The effect of heating on one die due to the adjacent dice is considered by applying the theory of linear superposition. One die is heated while the temperatures of all the other dice are recorded after thermal equilibrium is reached. Hereafter, the second die is heated and all the dice temperatures are recorded, and so on, until the fourth die is heated. With the known ambient temperature, die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4-by-4 matrix for our case of four heat sources.

Figure 19: Thermal Resistance Measurements



Definitions

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (˚C/W)
R_{12}: Thermal Resistance of Die1 due to heating of Die2 (˚C/W)
R_{13}: Thermal Resistance of Die1 due to heating of Die3 (˚C/W)
R_{14}: Thermal Resistance of Die1 due to heating of Die4 (˚C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (˚C/W)
R_{22}: Thermal Resistance of Die2 due to heating of Die2 (˚C/W)
R_{23}: Thermal Resistance of Die2 due to heating of Die3 (˚C/W)
R_{24}: Thermal Resistance of Die2 due to heating of Die4 (˚C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (˚C/W)
R_{32}: Thermal Resistance of Die3 due to heating of Die2 (˚C/W)
R_{33}: Thermal Resistance of Die3 due to heating of Die3 (˚C/W)
R_{34}: Thermal Resistance of Die3 due to heating of Die4 (˚C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (˚C/W)
R_{42}: Thermal Resistance of Die4 due to heating of Die2 (˚C/W)
R_{43}: Thermal Resistance of Die4 due to heating of Die3 (˚C/W)
R_{44}: Thermal Resistance of Die4 due to heating of Die4 (˚C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P_3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (˚C)
T_2: Junction temperature of Die2 due to heat from all dice (˚C)
T_3: Junction temperature of Die3 due to heat from all dice (˚C)
T_4: Junction temperature of Die4 due to heat from all dice (˚C)

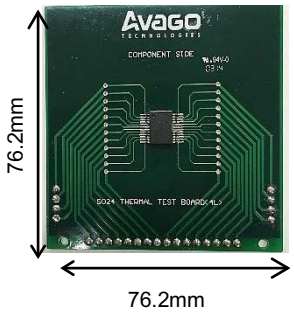
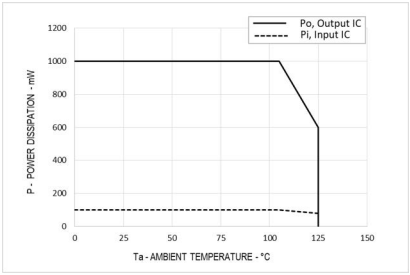
T_A: Ambient temperature (˚C)
ΔT_1: Temperature difference between Die1 junction and T_A
ΔT_2: Temperature deference between Die2 junction and T_A
ΔT_3: Temperature difference between Die3 junction and T_A
ΔT_4: Temperature deference between Die4 junction and T_A

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_A$ -- (1)
$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_A$ -- (2)
$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_A$ -- (3)
$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_A$ -- (4)

Measurement Data

Measurement is done on a high effective thermal conductivity board according to JEDEC Standard 51-7.

Table 1: Test Board Thermal Conductivity Measurement Data

Test Board	Test Board Conditions	Thermal Resistance	Power Dissipation Derating Chart
	4-layer board that embodies two signal layers, a power plane, and a ground plane. Outer layers: 2 oz. Copper thickness Inner layers: 1 oz. Copper thickness	R_{11} = 193.9°C/W R_{12} = 16.6°C/W R_{13} = 12°C/W R_{14} = 20.5°C/W R_{21} = 16.7°C/W R_{22} = 204.9°C/W R_{23} = 19.7°C/W R_{24} = 12°C/W R_{31} = 16.7°C/W R_{32} = 31°C/W R_{33} = 42°C/W R_{34} = 13.3°C/W R_{41} = 31.6°C/W R_{42} = 17.5°C/W R_{43} = 13.9°C/W R_{44} = 45.2°C/W	**Figure 20: Power Derating Chart Based on High Effective Thermal Conductivity**  **NOTE:** ■ Input LED power dissipation is derated linearly above 105°C from 100 mW to 80 mW at 125°C. ■ Output IC power dissipation is derated linearly above 105°C from 1000 mW to 600 mW at 125°C

Notes on Thermal Calculation

Application and environmental design for ACFJ-3262T needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The following equations are for the purposes of calculating the maximum power dissipation and corresponding effect on junction temperatures. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment; it can only be used as a reference for thermal performance comparison under specified PCB layout as shown in Table 1.

Calculation of Input LED Power Dissipation, P_1 and P_2

Input LED Power Dissipation (P_1) = $I_{F(LED)}$ (Recommended Max.) × $V_{F(LED,\ 125°C)}$ × Duty Cycle

Example:

P_1 = 16 mA × 1.85V × 50% duty cycle = 15 mW

P_2 = P_1 = 15 mW

Calculation of Output IC Power Dissipation, P_3 and P_4

Output IC Power Dissipation (P_3) = $P_{O(Static)} + P_{HS} + P_{LS}$

Where:

- $P_{O(Static)}$: Static power dissipated by the output IC = $I_{DD} \times V_{DD}$
- P_{HS}: High side switching power dissipation at V_{OH} pin = $(V_{DD} \times Q_G \times f_{PWM}) \times R_{DS,OH(MAX)}/(R_{DS,OH(MAX)} + R_{GH}) / 2$
- P_{LS}: Low side switching power dissipation at V_{OL} pin = $(V_{DD} \times Q_G \times f_{PWM}) \times R_{DS,OL(MAX)}/(R_{DS,OL(MAX)} + R_{GL}) / 2$
- Q_G: SiC gate charge at 16V supply voltage (110nC)
- f_{PWM}: Input LED switching frequency (400 kHz)
- $R_{DS,OH(MAX)}$: Maximum high side output impedance (1.3Ω)
- R_{GH}: External gate charging resistance (2.2Ω)
- $R_{DS,OL(MAX)}$: Maximum low side output impedance (1.2Ω)
- R_{GL}: External gate discharging resistance (2.2Ω)

Example:

P_{HS} = (16V × 110nC × 400 kHz) × 1.3Ω/ (1.3Ω + 2.2Ω) / 2 = 130.74 mW

P_{LS} = (16V × 110nC × 400 kHz) × 1.2Ω/ (1.2Ω + 2.2Ω) / 2 = 124.24 mW

$P_{O(Static)}$ = 4 mA (Data Sheet Max.) × 16V = 64 mW

P_3 = 64 mW + 130.74 mW + 124.24 mW = 320 mW

$P_3 = P_4$ = 0.32 mW

Calculation of Junction Temperature for High Effective Thermal Conductivity Board

Example:

Input LED1 Junction Temperature, T_1

= $(R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_A$

= (193.9°C/W × 15 mW) + (16.6°C/W × 15 mW) + (12°C/W × 320 mW) + (20.5°C/W × 320 mW) + 125°C

= 138°C < T_J(absolute max) of 150°C

Input LED2 Junction Temperature, T_2

= $(R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_A$

= (16.7°C/W × 15 mW) + (204.9°C/W × 15 mW) + (19.7°C/W × 320 mW) + (12°C/W × 320 mW) + 125°C

= 138°C < T_J(absolute max) of 150°C

Output IC2 Junction Temperature, T_3

= $(R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_A$

= (16.7°C/W × 15 mW) + (31°C/W × 15 mW) + (42°C/W × 320 mW) + (13.3°C/W × 320 mW) + 125°C

= 143°C < T_J(absolute max) of 150°C

Output IC1 Junction Temperature, T_4

= $(R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_A$

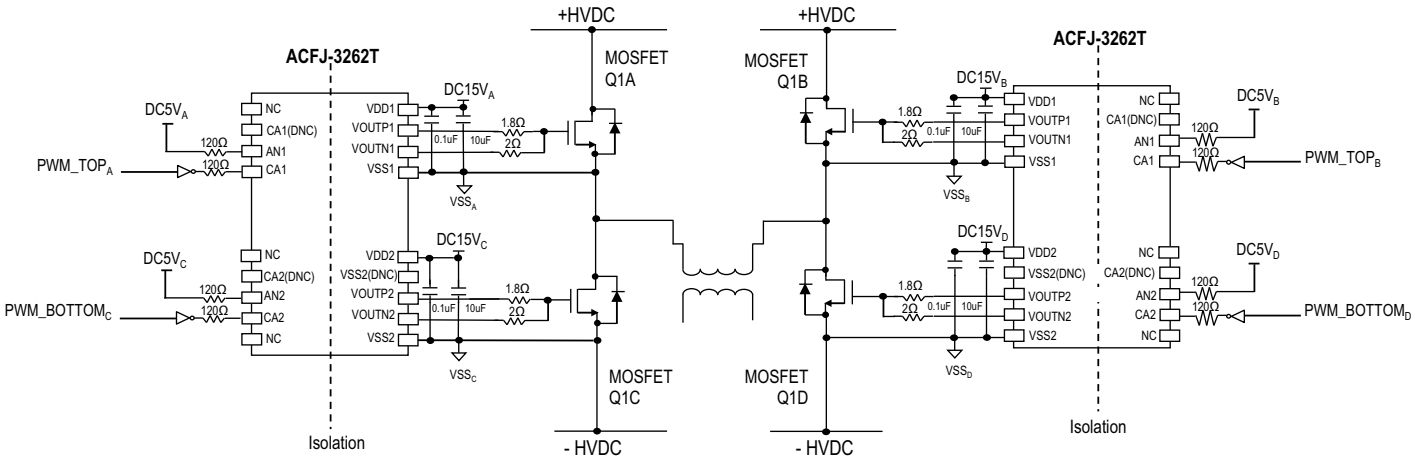
= (31.6°C/W × 15 mW) + (17.5°C/W × 15 mW) + (13.9°C/W × 320 mW) + (45.2°C/W × 320 mW) + 125°C

= 145°C < T_J(absolute max) of 150°C

NOTE: Junction temperature of T_1, T_2, T_3, and T_4 must not exceed 150°C at any given ambient temperature T_A.

Typical Application Circuit

Figure 21: ACFJ-3262T Typical Application Circuit



NOTE: Component value is subjected to change based on application conditions.

Sizing the External Gate Resistor

The ACFJ-3262T has two separate source and sink outputs, which offers flexibility in tuning the turn-on and turn-off gate resistors for optimum MOSFET/IGBT switching performance. Typically, when working on a new design, the gate resistor value can be selected based on the recommended values given in MOSFET/IGBT data sheet under certain test conditions. However, it is also important to consider the gate driver capability during the design so that peak gate current is within the recommended ratings of the driver. If the ACFJ-3262T is used to drive MOSFET/IGBT directly, the designer has to consider the power dissipation for both the gate driver and the external gate resistors.

Example:

Given V_{DD} = 15V, V_{SS} = Ground (0V):

- Recommended $I_{OH(PEAK)}$ = Maximum V_{OUTP} peak output souring current = –6A
- Recommended $I_{OL(PEAK)}$ = Minimum V_{OUTN} peak output souring current = 6A
- Minimum gate turn-on resistor, Rgon(min) ≥ $(V_{DD} – V_{SS})/I_{OH(PEAK)} – R_{DS,OH(ON)}$ = 15V/6A – 0.8Ω = 1.7Ω
  - Select Rgon = 1.8Ω to start with.
- Minimum gate turn-off resistor, Rgoff(min) ≥ $(V_{DD} – V_{SS})/I_{OL(PEAK)} – R_{DS,OL(ON)}$ = 15V/6A – 0.6Ω = 1.9Ω
  - Select Rgoff = 2Ω to start with.

Power dissipation of gate resistors can be calculated as follows:

Power dissipation in turn-on gate resistor, $P_{(Rgon)}$= Average Igate(on)^2 × Rgon

Power dissipation in turn-off gate resistor, $P_{(Rgoff)}$= Average Igate(off)^2 × Rgoff

When the initial Rgon and Rgoff values are selected, test the circuit with MOSFET/IGBT under actual application conditions to check for switching losses, MOSFET/IGBT voltage spike, and so on, to fine tune the gate resistor values.

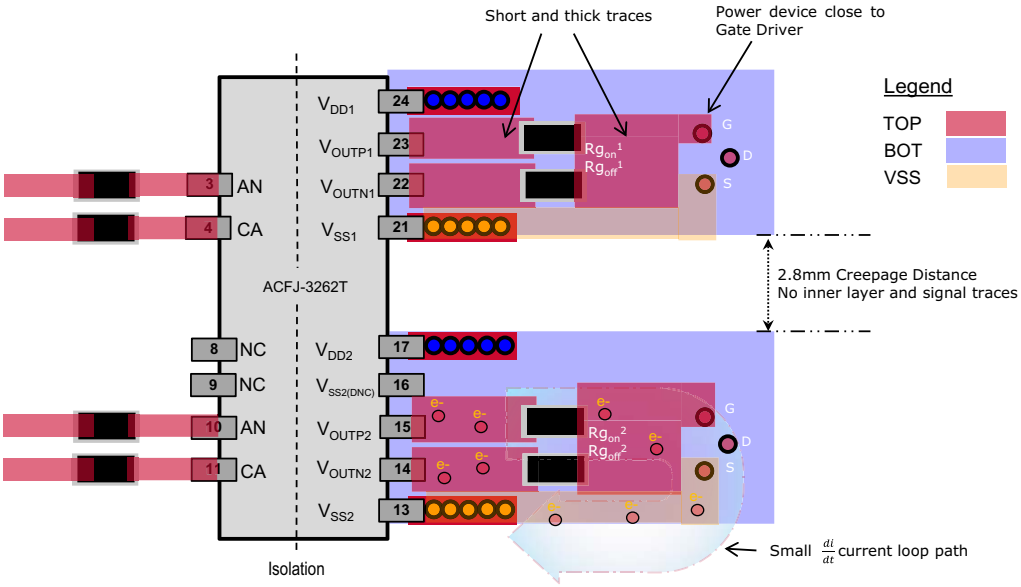
Layout Guidelines

The gate driver's output sinks about 10A, which the return current path of minimum inductance must be implemented during printed circuit board layout design to alleviate the effect of ground bounce, as the excitation of parasitic elements in the PCB/ gate driver become dominant.

The smallest loop between the outbound and return currents forms the least inductance. The gate driver should be placed close to the power devices (that is, MOSFET/IGBT) with short and thick traces to minimize the parasitic inductance along the high current switching path.

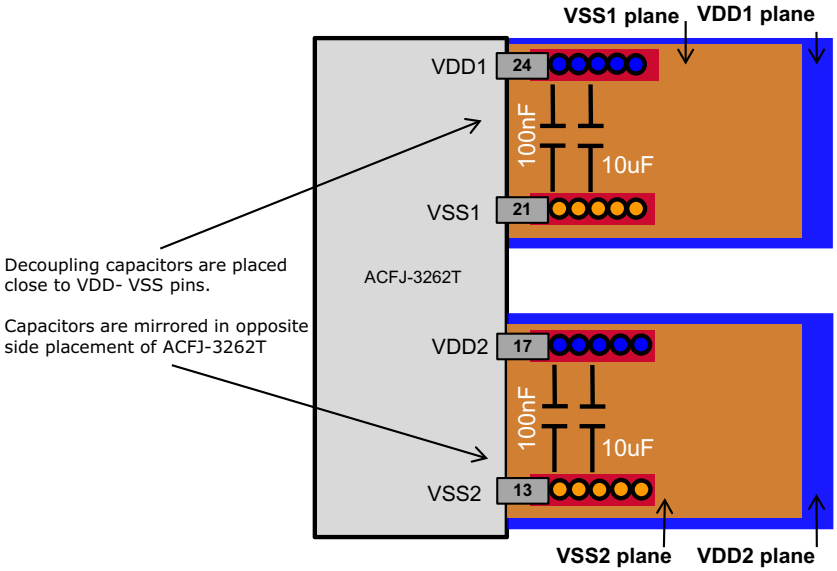
Adequate spacing should always be maintained between the high voltages isolated circuitry and any input referenced circuitry. Minimum spacing between two adjacent high-side isolated channels (that is, top and bottom channels) must be maintained as well. Insufficient spacing will reduce the effective isolation and may increase parasitic coupling that will degrade part performance. Figure 22 shows the recommended PCB layout guidelines.

Figure 22: PCB Layout Guidelines



The placement and routing of supply bypass capacitors require special attention. During switching transients, the majority of gate charge is supplied by bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms. It is recommended to connect the bypass capacitors to the power plane and ground plane with multiple via holes. The planes can provide better heat dissipation and, at the same time, serve as a natural decoupling capacitor to the IC. Figure 23 shows the bypass capacitors placement and PCB planes stack-up.

Figure 23: PCB Planes Stack-Up and Bypass Capacitors Placement



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