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BCM8727 PRODUCT Brief

DUAL-CHANNEL 10-GbE SFI-to-XAUI™ TRANSCEIVER with EDC

FEATURES

- Dual-channel SFI-to-XAUI™ transceiver
- Integrated microcontroller and AGC with a wide dynamic range
- Supports SFP+ SR, LR, and LRM optical interfaces and up to 15m of direct attached copper
- Programmable amplitude control on 10G serial transmitter interface
- Standard two-wire Broadcom Serial Interface (BSC) support for external E2, XFP, SFP, SFP+
- MDIO interface compliant to IEEE802.3ae Clause 45 with extended indirect address register access
- Support for XFP/XFI interfaces
- Physical Medium Dependent (PMD) interface: serial 10.3125 Gbps CML
- PCS 64B/66B scrambler/descrambler
- XGXS 8B/10B error detection ENDEC
- XAUI link synchronization/deskew
- 4-lane XAUI interface (3.125 Gbps)
- Built-In Self-Test (BIST) on 10G serial and XAUI interfaces
- Power dissipation: 2.4W
- Core supply—1.0V, I/O—3.3V
- Small 19 mm x 19 mm BGA package, 1-mm ball pitch

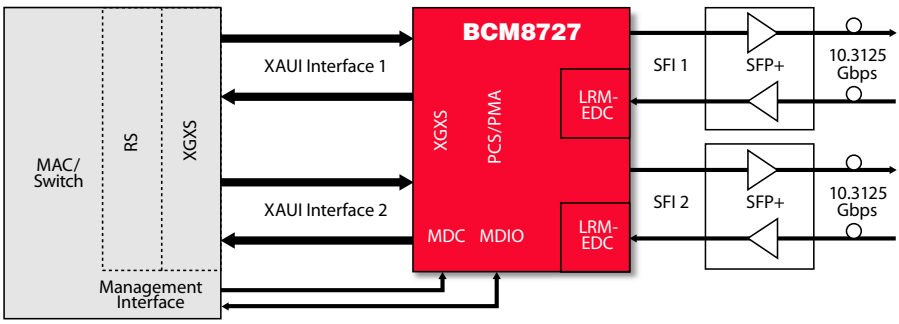
SUMMARY OF BENEFITS

- Single-reference clock input enables use of low-cost 156.25 MHz oscillator.
- Supports low-cost SFP+ copper twin-ax up to 15m
- LRM mode supports 300m of Multimode Fiber (MMF), exceeding the IEEE 802.3aq standard.
- PMD transmit preemphasis for flexible placement of Physical Layer (PHY)
- Support for module present detection and configuring of BCM8727 accordingly
- Multirate 10 GbE and 1 GbE support for legacy interfaces

APPLICATIONS

- High-density Ethernet Switching and Routing Platforms
- Next-generation Blade Servers
- SFP+ optical SR, LR, and LRM modules
- SFP+ copper twin-ax

BCM8727 Functional Block Diagram



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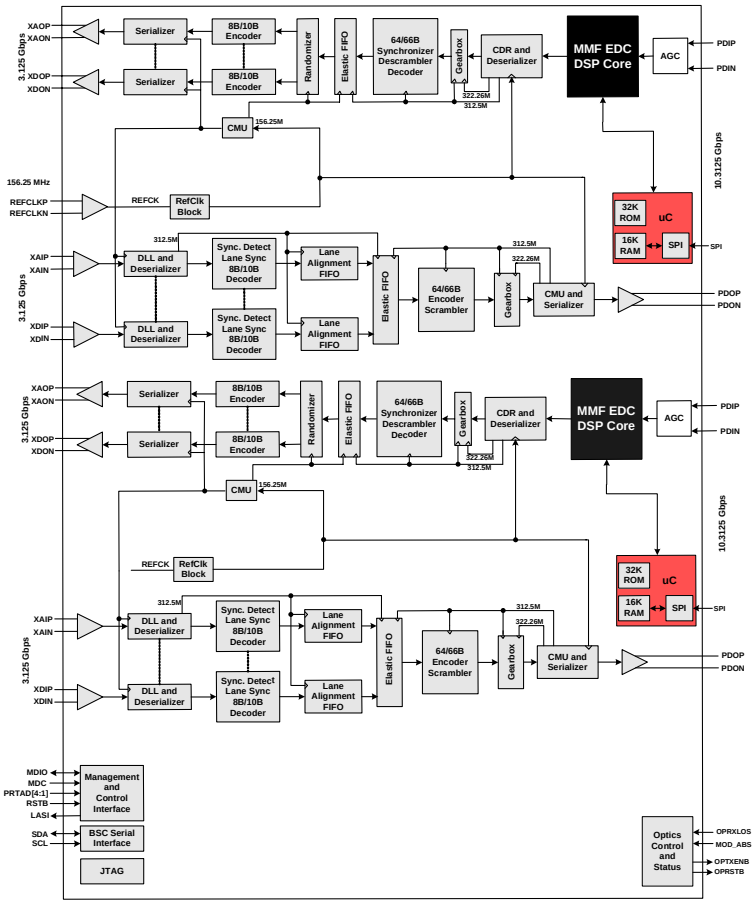
OVERVIEW



BCM8727 Block Diagram

The BCM8727 is a dual-channel 10-GbE SFI-to-XAUI transceiver that incorporates an Electronic Dispersion Compensation (EDC) equalizer supporting SFP+ line-card applications.

The BCM8727 is a multirate PHY targeted for SMF, MMF, or copper twin-ax applications interfacing to both limiting-based and linear-based SFP+ and SFP modules. The BCM8727 is fully compliant to the 10-GbE IEEE 802.3aq standard and also supports 1000BASE-X for 1-GbE operation.

The BCM8727 is developed using an all-DSP high-speed front-end providing the highest performance and most flexibility for line-card designers. An on-chip microcontroller implements the control algorithm for the DSP core.

On-chip clock synthesis is performed by the high-frequency, low-jitter, Phase-Locked Loops (PLLs) for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to the respective incoming data streams. An external 156.25 MHz reference clock input is required for each port.

The BCM8727 Ethernet LRM PHY device is a fully integrated SerDes (10.3125 Gbps) interface device performing the extension functions for a 10-Gigabit serial Ethernet Reconciliation Sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

The BCM8727 is available in a 19 mm x 19 mm, 1 mm pitch, 324-pin BGA, RoHS-compliant package. The BCM8727 supports a footprint-compatible layout with the BCM8726 dual LRM PHY.

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