U430, U431 N-Channel JFET

Features

- InterFET N0072L Geometry
- Low Noise: 2 nV/√Hz Typical
- Low Ciss: 4pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

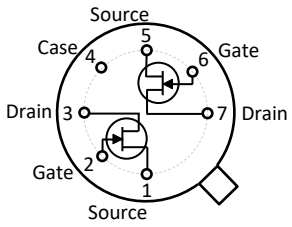
Applications

- Balanced Mixers
- Differential Amplifiers

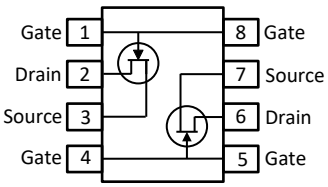
Description

The -25V InterFET U430 and U431 are targeted for balanced mixers and differential amplifier applications. Gate leakages are typically less than 10pA at room temperatures. Custom specifications, matching, and packaging options are available.

TO-78 Bottom View



SOIC8 Top View



Product Summary

Parameters		U430 Min	U431 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-25	-25	V
I_{DSS}	Drain to Source Saturation Current	12	24	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	-2	V
G_{FS}	Forward Transconductance	10	10	mS

Ordering Information

Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
U430; U431	Through-Hole	TO-78	Bulk
SMPU430; SMPU431	Surface Mount	SOIC8	Bulk
SMPU430TR; SMPU431TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
U430COT; U431COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
U430CFT; U431CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-25	V
I_{FG}	Continuous Forward Gate Current	20	mA
P_D	Continuous Device Power Dissipation	500	mW
P	Power Derating	4	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

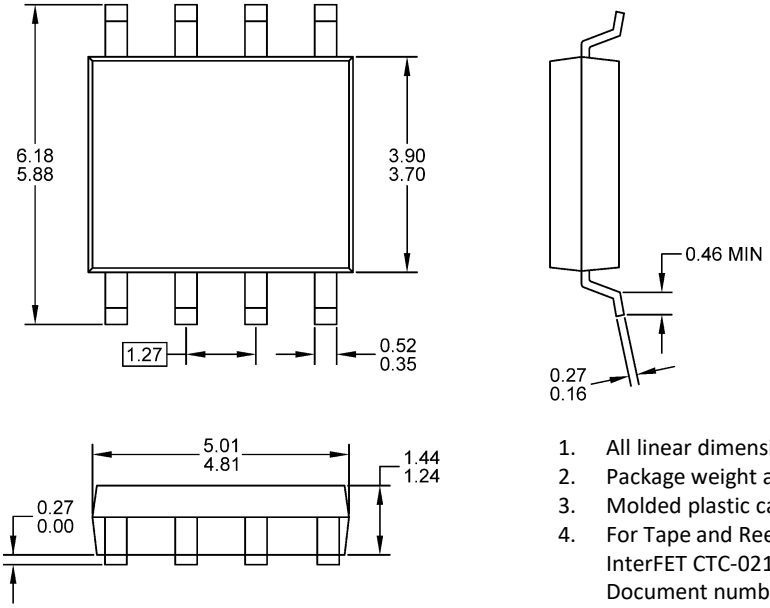
Parameters		Conditions	U430			U431			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-25			-25			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -15V, V_{DS} = 0V, T_A = 25°C V_{GS} = -15V, V_{DS} = 0V, T_A = 150°C			-150 -150			-150 -150	pA nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA	-1		-4	-2		-6	V
$V_{GS(F)}$	Gate to Source Forward Voltage	V_{DS} = 0V, I_G = 10mA			1			1	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 10V (Pulsed)	12		30	24		60	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	U430			U431			Unit
			Min	Typ	Max	Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 10mA, f = 1kHz V_{DS} = 10V, I_D = 10mA, f = 100MHz	10	17 12		10	17 12		mS
G_{OS}	Output Conductance	V_{DS} = 10V, I_D = 10mA, f = 1kHz V_{DS} = 10V, I_D = 10mA, f = 100MHz		 0.15	250		 0.15	250	µS
C_{dg}	Drain Gate Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz			5			5	pF
C_{gs}	Source Gate Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz			2.5			2.5	pF
e_n	Noise Voltage	V_{DS} = 10V, I_D = 10mA, f = 100kHz			10			10	nV/√Hz
G_{ig}	Power Match Source Admittance	V_{DS} = 10V, I_D = 10mA, f = 100MHz		12			12		-
G_c	Conversion Gain	V_{DS} = 20V, V_{GS} = ½ $V_{GS(OFF)}$, R_L = 2kΩ, f = 100MHz		3			3		dB
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio	V_{DS} = 10V, V_G = 0V	0.9		1	0.9		1	-
$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	Gate to Source Cutoff Voltage Ratio	V_{DS} = 10V, I_D = 1nA	0.9		1	0.9		1	-
g_{fs1}/g_{fs2}	Transconductance Ratio	V_{DS} = 10V, I_D = 10mA	0.9		1	0.9		1	-

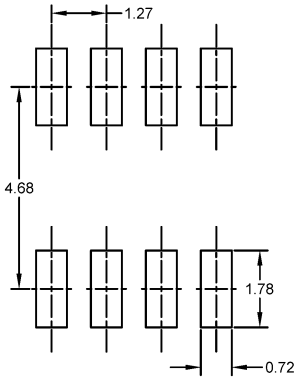
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

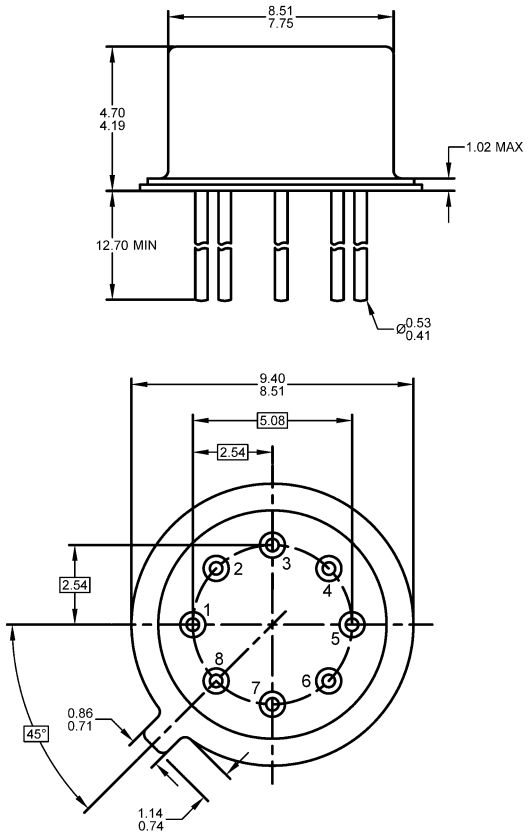
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

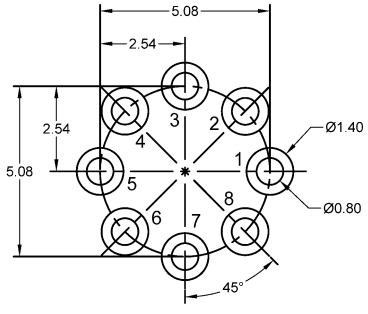
TO-78 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 7.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Mouser Electronics

Authorized Distributor

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InterFET:

U430 U431 SMPU430 SMPU430TR