





IF3602 Dual Matched N-Channel JFET

Features

- InterFET <u>N3600L Geometry</u>
- Ultra Low Noise: 0.5 nV/VHz Typical
- High Gain: 750mS Typical
- Low Rds(on): 2.0 Ohms Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- Low-Noise, High Gain Amplifiers
- Differential Amplifiers

Description

The -20V InterFET IF3602 JFET is targeted for ultra low noise high gain differential amplifier designs. The IF3602 has a cutoff voltage of less than 2.0V ideal for low voltage applications. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

	Parameters	IF3602 Min	Unit
BV _{GSS}	Gate to Source Breakdown Voltage	-20	V
I _{DSS}	Drain to Source Saturation Current	30	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.35	V
G _{FS}	Forward Transconductance	750 Typical	mS

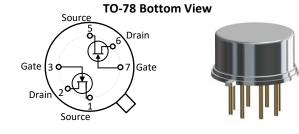
Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF3602T78	Through-Hole	TO-78	Bulk
IF3602COT *	Chip Orientated Tray (COT Waffle Pack)	СОТ	30/Waffle Pack
IF3602CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	30/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
VRGS	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	10	mA
PD	Continuous Device Power Dissipation	300	mW
Р	Power Derating	4	mW/°C
Τı	Operating Junction Temperature	-55 to 125	°C
T _{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

	Parameters	Conditions	Min	Тур	Max	Unit
V(BR)GSS	Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = -1µA	-20			v
I _{GSS}	Gate to Source Reverse Current	V_{GS} = -10V, V_{DS} = 0V			-0.1	nA
V _{GS(OFF)}	Gate to Source Cutoff Voltage	V _{DS} = 10V, I _D = 0.5nA	-0.35		-2.0	V
I _{DSS}	Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	30	300		mA

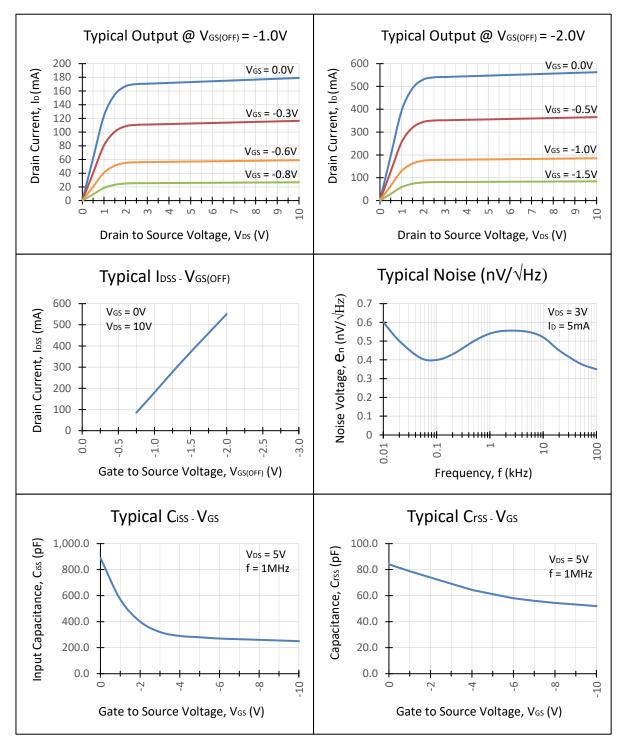
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

	Parameters	Conditions	Min	Тур	Max	Unit
Gfs	Forward Transconductance	$V_{DS} = 10V$, $V_{GS} = 0V$, $f = 1kHz$		750		mS
C _{iss}	Input Capacitance	$V_{DS} = 0V$, $V_{GS} = -4V$, $f = 1MHz$		300		pF
Crss	Reverse Transfer Capacitance	$V_{DS} = 0V$, $V_{GS} = -4V$, $f = 1MHz$		200		pF
en	Equivalent Circuit Input Noise Voltage	V _{DS} = 3V, I _D = 5mA, f = 100Hz		0.5		nV/√Hz
$\left V_{GS1} - V_{GS2}\right $	Differential Gate Source Voltage	V _{DS} = 10V, I _D = 500pA			100	mV





Typical IF3602 Characteristics

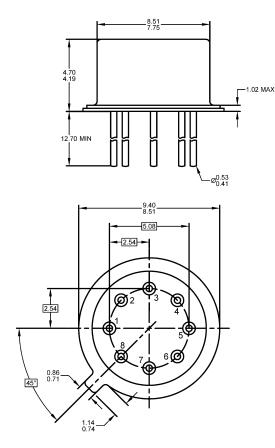




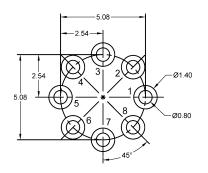


TO-78 Mechanical and Layout Data

Package Outline Data



Suggested Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- 2. Eight leaded device. Not all leads are shown in drawing views.
- 3. Some package configurations will not populate pin 8 and/or pin 7.
- 4. Package weight approximately 0.44 grams
- 5. Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

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InterFET: IF3602