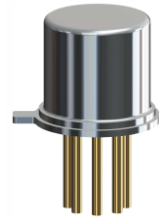
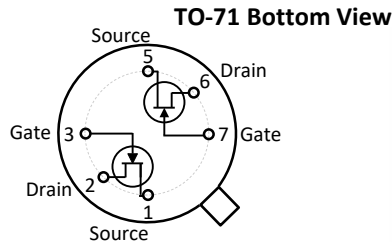


IF1322, IF1322A Dual Matched N-Channel JFET

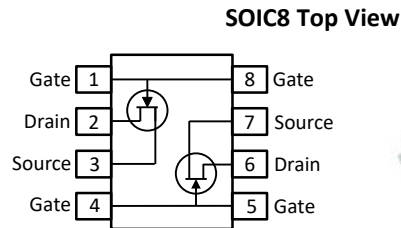
Features

- InterFET [N0132L Geometry](#)
- Low Noise: 1.0 nV/√Hz Typical
- High Gain: 20mS Typical
- Low Cutoff Voltage: 1.5V Maximum
- RoHS Compliant
- SMT, TH, and Bare Die Package options.



Applications

- Low Noise High Gain Amplifier
- Differential Amplifiers
- Instrumentation Amplifiers
- Acoustic and Vibration Sensors



Description

The -20V InterFET IF1322 matched pair JFET is targeted for low noise high gain differential amplifier designs. The IF1322 has a cutoff voltage of less than 1.5V ideal for low-level power supplies. The TO-71 package is hermetically sealed and suitable for military uses. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters	IF1322 Min	IF1322A Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-20	-20	V
I_{DSS} Drain to Source Saturation Current	8	8	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.8	-0.8	V
G_{FS} Forward Transconductance	10	10	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF1322T71; IF1322AT71	Through-Hole	TO-71	Bulk
IF1322S08; IF1322AS08	Surface Mount	SOIC8	Bulk
IF1322S08TR; IF1322AS08TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IF1322COT; IF1322ACOT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IF1322CFT; IF1322ACFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation	400	mW
P Power Derating	2.3	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

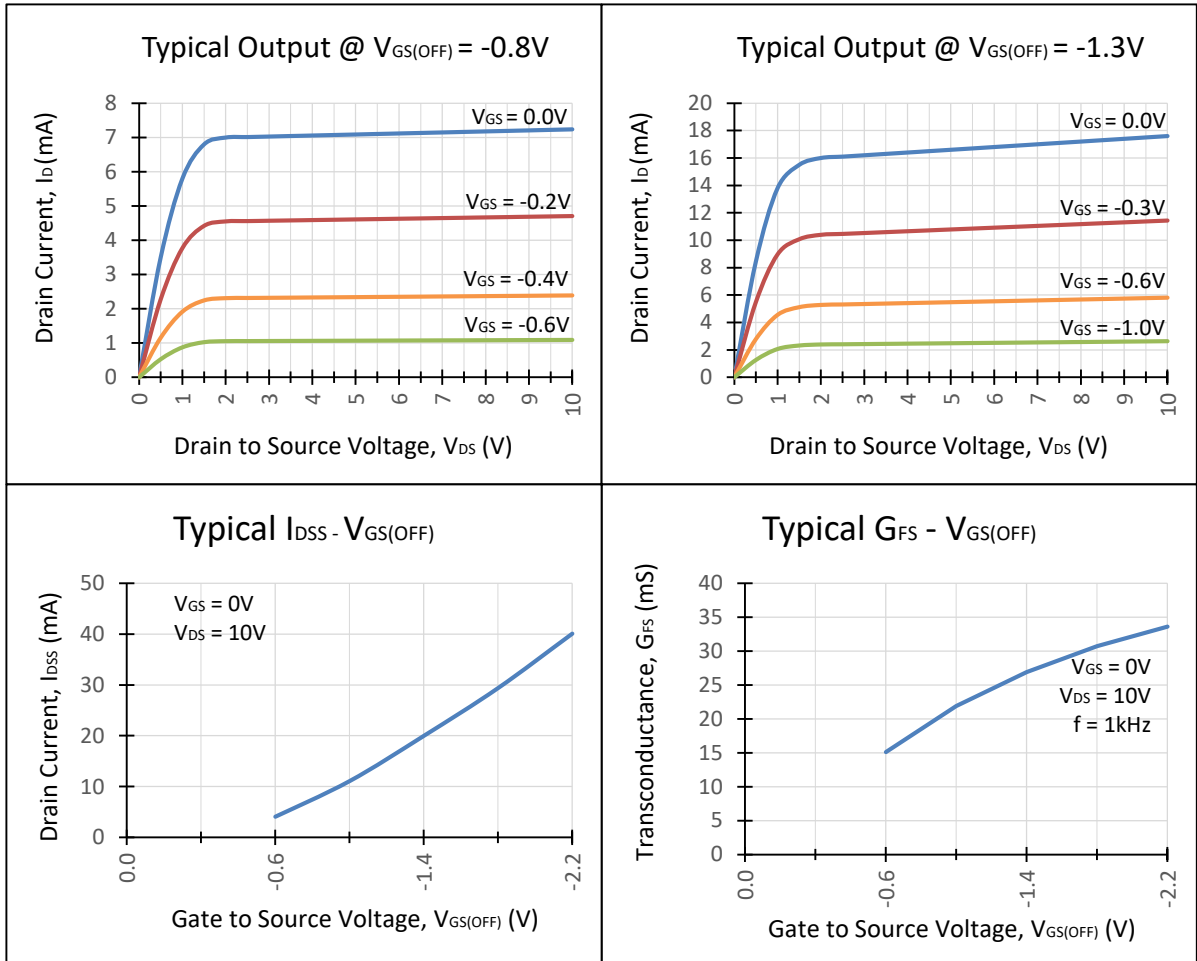
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IF1322		IF1322A		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	GSS1: $I_G = -25\mu\text{A}$, $V_{DS} = 0\text{V}$ GSS2: $I_G = -3\mu\text{A}$, $V_{DS} = 0\text{V}$ GSS3: $I_G = -1\mu\text{A}$, $V_{DS} = 0\text{V}$	-20		-20		V
I_{GSS} Gate to Source Reverse Current	$V_{DS} = 0\text{V}$, $V_{GS} = -10\text{V}$		-0.1		-0.1	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10\text{V}$, $I_D = 1\mu\text{A}$	-0.8	-1.5	-0.8	-1.5	V
$V_{GS(F)}$ Gate to Source Forward Voltage	$V_{DS} = 0\text{V}$, $I_G = -1\text{mA}$ $V_{DS} = 0\text{V}$, $I_G = -1\mu\text{A}$	0.3	1.0	0.3	1.0	V
I_{DSS} Drain to Source Saturation Current	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$ (Pulsed)	8	25	8	25	mA

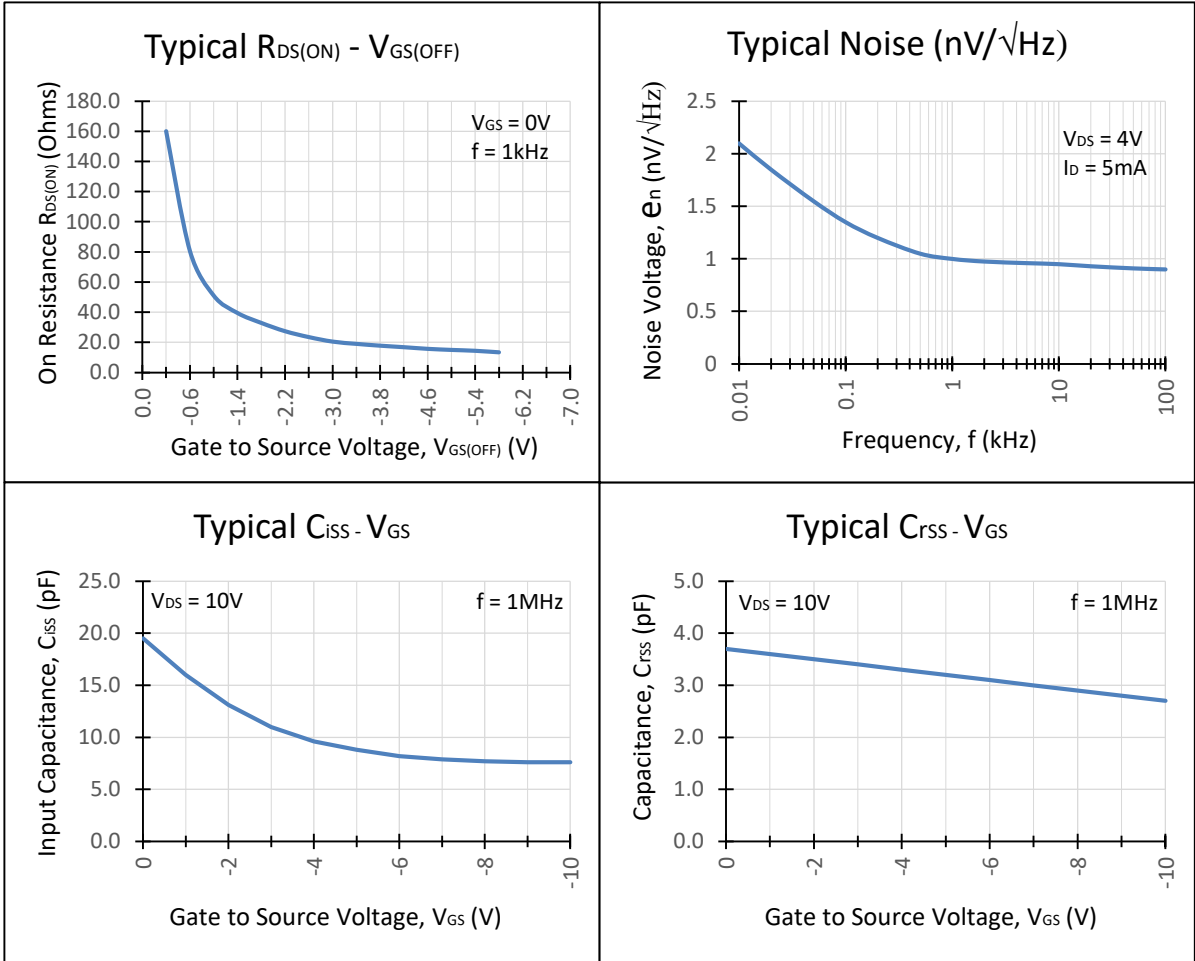
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IF1322		IF1322A		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 5\text{V}$, $V_{GS} = 0\text{V}$	10		10		mS
$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage	$V_{DS} = 5\text{V}$, $I_D = 3\text{mA}$		30		40	mV
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 5\text{V}$, $I_D = 3\text{mA}$, $f = 1\text{kHz}$ $V_{DS} = 5\text{V}$, $I_D = 3\text{mA}$, $f = 100\text{Hz}$		2 4		2 4	nV/ $\sqrt{\text{Hz}}$
i_n Equivalent Circuit Input Noise Current	$V_{DS} = 5\text{V}$, $I_D = 3\text{mA}$, $f = 1\text{kHz}$		0.05		0.05	pA/ $\sqrt{\text{Hz}}$

Typical IF1322, IF1322A Characteristics

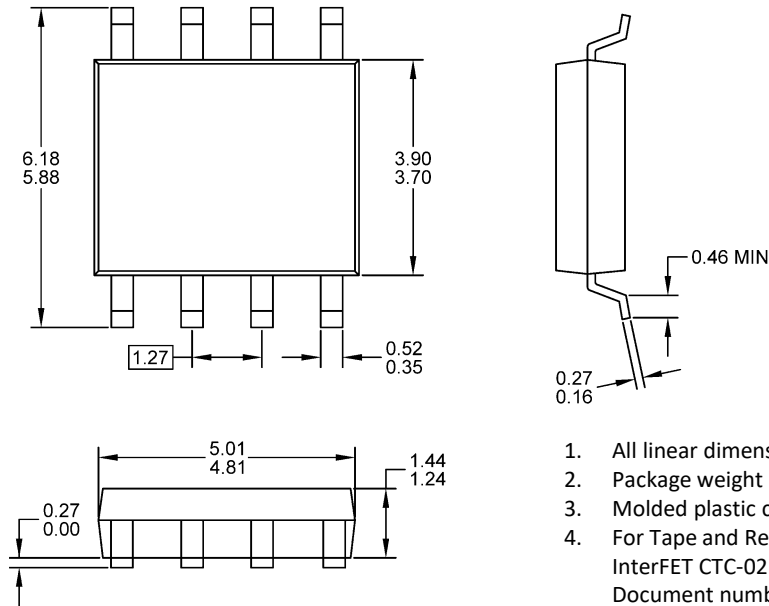


Typical IF1322, IF1322A Characteristics (Continued)



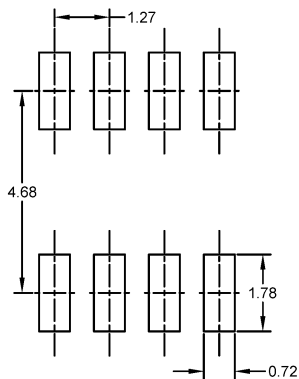
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

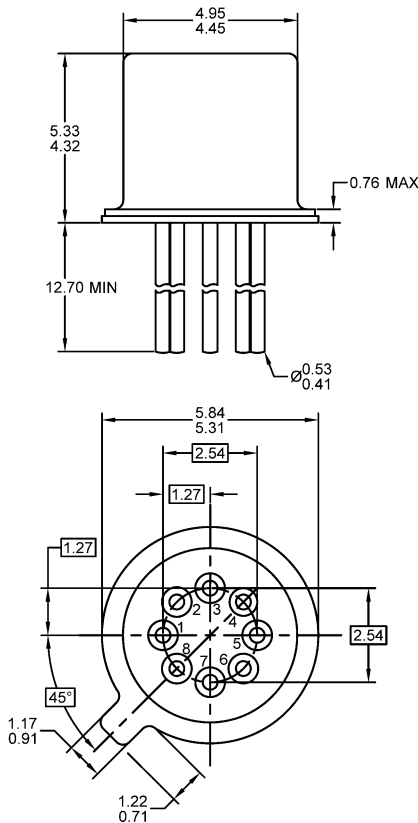
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

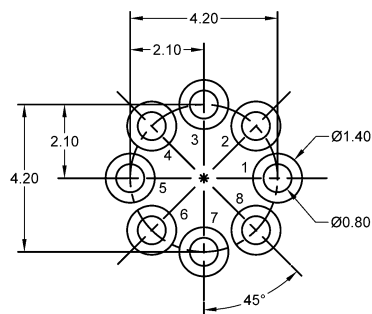
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

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[IF1322A](#) [IF1322B](#) [IF1322A-TR](#) [IF1322B-TR](#) [IF1323A](#)