DDR5 SDRAM RDIMM Core

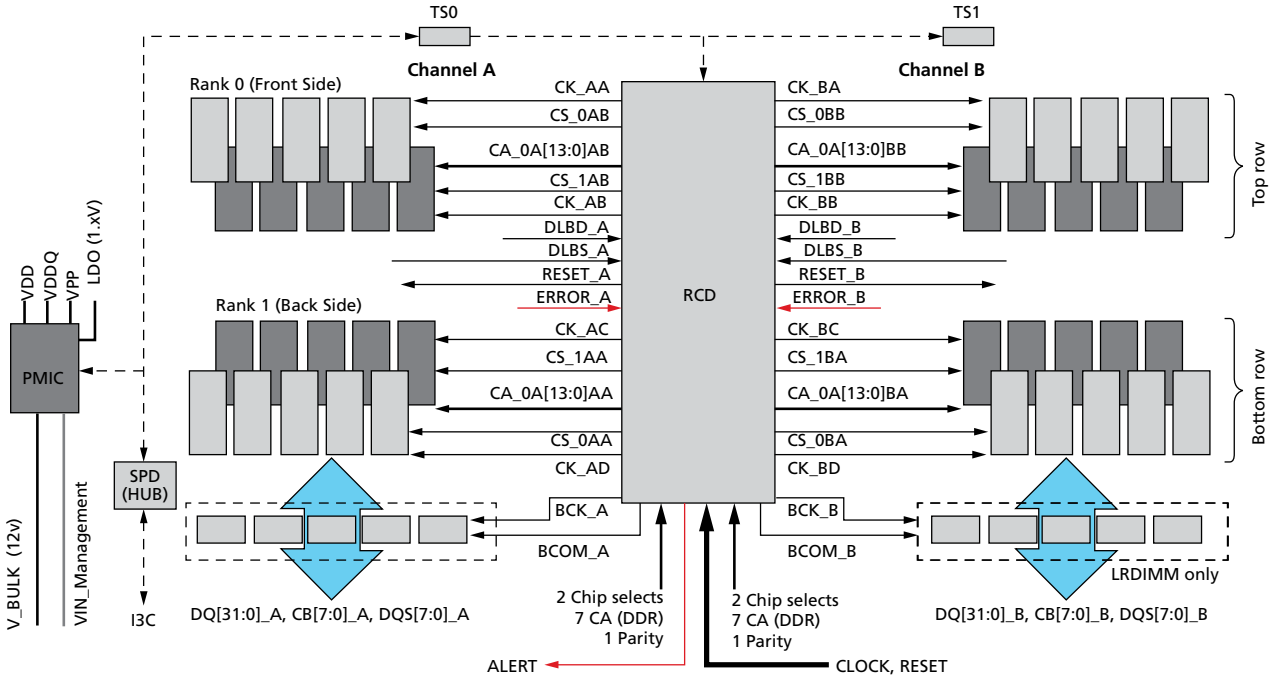
Product Description

This specification defines the electrical and mechanical requirements for 287-pin and 288-pin, 1.1V (V_{DD}) double data rate, synchronous DRAM, registered dual in-line memory modules (DDR5 SDRAM RDIMMs). These DDR5 RDIMMs are intended for use as main memory when installed in servers. Some specifications are part number-specific; refer to the module data sheet addendum of the specific Micron part number (MPN) for the complete specification.

Features

- DDR5 functionality and operations supported as defined in the component data sheet
- 287/288-pin RDIMM
- Supports ECC error detection and correction
- On-DIMM SPD EEPROM with Hub function and integrated temperature sensor (TS)
- Two on-DIMM discrete TS5 temperature sensors
- On-DIMM power management integrated circuit (PMIC)
- Sideband access with I3C-basic/I2C support
- Two independent I/O sub channels for increased bandwidth
- DDR command/address bus to RCD
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control and command/address bus

Figure 1: DDR5 LRDIMM/RDIMM Functional Block Diagram



Note: 1. The above illustrates a dual-rank x80 LRDIMM/RDIMM with DRAM, PMIC, RCD, SPD, temp sensors and data buffers.

Table 1: DDR5 Product Family Attributes[1]

Parameter	Options	Notes
DIMM organization	x80 ECC (EC8), x72 ECC (EC4)	Two independent 40-bit or 36-bit I/O sub-channels
DIMM dimensions (nominal)	133.35mm x 31.25mm	Refer to Module Dimensions
Pin count[2]	287, 288	
DDR5 SDRAM densities supported	8Gb, 16Gb, 24Gb	78/82-ball FBGA package for x4/x8 devices
Capacity	(16Gb) 16GB-256GB (24Gb) 24GB-1536GB	(DRAM) SDP, 2H, 4H, 8H, 16H
DDR5 SDRAM width	x4, x8	
Data transfer rate	PC5-4800 to PC5-6400	Refer to Key Timing Parameters
Serial presence detect hub with temperature sensor	1024 byte	
Voltage (external supply, nominal)	V_{IN_Bulk}: 12V	Bulk input DC supply voltage from system
	V_{IN_MGMT}: 3.3V	Management input supply voltage from system
Voltage (PMIC output)	V_{DD}: 1.1V	Supply voltage from PMIC
	V_{DDQ}: 1.1V	I/O Supply voltage from PMIC
	V_{PP}: 1.8V	Pump voltage from PMIC
	1.8V LDO output	From PMIC to HUB, TS
	1.0V LDO output	From PMIC to HUB, TS, RCD
DDR5 Interface	1.1V signaling	
DRAM operating temperature	T = 0 to 95 °C	Refer to Thermal Characteristics

Notes: 1. Attributes shown in this table are for reference only and do not necessarily reflect the same options supported by Micron. Please refer to the MPN-specific module addendum for supported features for the MPN.
2. Modules with nominal transfer rates ≥6400 MT/s will have 287 pins, while modules with nominal transfer rates <6400 MT/s will have 288 pins. Refer to Pin Assignments for details.

Table 2: Key Timing Parameters[1]

Speed Bins/ Micron Speed Grade	Data Rate (MT/s) CL =														t_{AA} MIN (ns)	t_{RCD} MIN (ns)	t_{RP} MIN (ns)	t_{RC} MIN (ns)
	56	54	52	50	48	46	42	40	36	32	30	28	26	22				
DDR5-6400B/ PC5-6400	6400	6000	6400	5600	6000	5600/ 5200	5200/ 4800	4800/ 4400	4400/ 4000	4000/ 3600	3600	3200	3200	2100	16.000	16.000	16.000	48.000
DDR5-5600B/ PC5-5600	–	–	–	5600	–	5600/ 5200	5200/ 4800	4800/ 4400	4400/ 4000	4000/ 3600	3600	3600	3200	2100	16.000	16.000	16.000	48.000
DDR5-5200B/ PC5-5200	–	–	–	–	–	5200	5200/ 4800	4800/ 4400	4400/ 4000	4000/ 3600	3600	3600	3200	2100	16.000	16.000	16.000	48.000
DDR5-4800B/ PC5-4800	–	–	–	–	–	–	4800	4800/ 4400	4400/ 4000	4000/ 3600	3600	3600	3200	2100	16.000	16.000	16.000	48.000

Note: 1. ^{t}AA,^{t}RCD, ^{t}RP and ^{t}RC values represent the tightest capability across all supported data rates and CL combinations above 3600 MT/s. For 3200–3600 MT/s, minimum values for ^{t}AA,^{t}RCD, and ^{t}RP = 16.250(ns) and ^{t}RC = 48.250(ns). Refer to component data sheet Speed Bin Tables for details.

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General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM modules utilizing 4- and 8-bit-wide DDR5 SDRAM devices have eight internal bank groups consisting of four memory banks each, providing a total of 32 banks. 16-bit-wide DDR5 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of sixteen banks. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of an 16*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16*n*-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR5 modules use two sets of differential signals (DQS_t and DQS_c) to capture data, and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR5 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be accounted for by using the write-leveling feature of DDR5.

Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR5 RDIMM modules. Certain pins may not apply for a specific part number. Refer to the functional block diagram in the module data sheet addendum for a specific MPN.

Table 3: Pin Assignments

288-Pin DDR5 RDIMM Front								288-Pin DDR5 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	V_{SS}	73	V_{SS}	109	DQ5_B	145	VIN_BULK	181	DQ22_A	217	CK_t	253	V_{SS}
2	RFU	38	DQ21_A	74	PAR_A	110	V_{SS}	146	VIN_BULK	182	V_{SS}	218	CK_c	254	DQ7_B
3	VIN_MGMT	39	V_{SS}	75	V_{SS}	111	DQ8_B	147	PCAMP	183	DQ23_A	219	V_{SS}	255	V_{SS}
4	HSCL	40	DQ24_A	76	CA0_B	112	V_{SS}	148	HSA	184	V_{SS}	220	RFU, NPP[1]	256	DQ10_B
5	HSDA	41	V_{SS}	77	V_{SS}	113	DQ9_B	149	RFU	185	DQ26_A	221	CA1_B	257	V_{SS}
6	V_{SS}	42	DQ25_A	78	CA2_B	114	V_{SS}	150	RFU	186	V_{SS}	222	V_{SS}	258	DQ11_B
7	DQ0_A	43	V_{SS}	79	V_{SS}	115	DQS1_B_t	151	V_{SS}	187	DQ27_A	223	CA3_B	259	V_{SS}
8	V_{SS}	44	DQS3_A_t	80	CA4_B	116	DQS1_B_c	152	DQ2_A	188	V_{SS}	224	V_{SS}	260	DQS6_B_c, TDQS6_B_c
9	DQ1_A	45	DQS3_A_c	81	V_{SS}	117	V_{SS}	153	V_{SS}	189	DQS8_A_c, TDQS8_A_c	225	CA5_B	261	DQS6_B_t, TDQS6_B_t
10	V_{SS}	46	V_{SS}	82	CA6_B	118	DQ12_B	154	DQ3_A	190	DQS8_A_t, TDQS8_A_t	226	V_{SS}	262	V_{SS}
11	DQS0_A_t	47	DQ28_A	83	V_{SS}	119	V_{SS}	155	V_{SS}	191	V_{SS}	227	PAR_B	263	DQ14_B
12	DQS0_A_c	48	V_{SS}	84	CS0_B_n	120	DQ13_B	156	DQS5_A_c, TDQS5_A_c	192	DQ30_A	228	V_{SS}	264	V_{SS}
13	V_{SS}	49	DQ29_A	85	V_{SS}	121	V_{SS}	157	DQS5_A_t, TDQS5_A_t	193	V_{SS}	229	CS1_B_n	265	DQ15_B
14	DQ4_A	50	V_{SS}	86	LBDQ	122	DQ16_B	158	V_{SS}	194	DQ31_A	230	V_{SS}	266	V_{SS}
15	V_{SS}	51	CB0_A	87	LBDQS	123	V_{SS}	159	DQ6_A	195	V_{SS}	231	RFU	267	DQ18_B
16	DQ5_A	52	V_{SS}	88	V_{SS}	124	DQ17_B	160	V_{SS}	196	CB2_A	232	RFU	268	V_{SS}
17	V_{SS}	53	CB1_A	89	CB4_B	125	V_{SS}	161	DQ7_A	197	V_{SS}	233	V_{SS}	269	DQ19_B
18	DQ8_A	54	V_{SS}	90	V_{SS}	126	DQS2_B_t	162	V_{SS}	198	CB3_A	234	CB6_B	270	V_{SS}
19	V_{SS}	55	DQS4_A_t	91	CB5_B	127	DQS2_B_c	163	DQ10_A	199	V_{SS}	235	V_{SS}	271	DQS7_B_c, TDQS7_B_c
20	DQ9_A	56	DQS4_A_c	92	V_{SS}	128	V_{SS}	164	V_{SS}	200	DQS9_A_c, TDQS9_A_c	236	CB7_B	272	DQS7_B_t, TDQS7_B_t
21	V_{SS}	57	V_{SS}	93	DQS9_B_t, TDQS9_B_t,	129	DQ20_B	165	DQ11_A	201	DQS9_A_t, TDQS9_A_t	237	V_{SS}	273	V_{SS}
22	DQS1_A_t	58	CB4_A	94	DQS9_B_c, TDQS9_B_c	130	V_{SS}	166	V_{SS}	202	V_{SS}	238	DQS4_B_c	274	DQ22_B
23	DQS1_A_c	59	V_{SS}	95	V_{SS}	131	DQ21_B	167	DQS6_A_c, TDQS6_A_c	203	CB6_A	239	DQS4_B_t	275	V_{SS}
24	V_{SS}	60	CB5_A	96	CB0_B	132	V_{SS}	168	DQS6_A_t, TDQS6_A_t	204	V_{SS}	240	V_{SS}	276	DQ23_B
25	DQ12_A	61	V_{SS}	97	V_{SS}	133	DQ24_B	169	V_{SS}	205	CB7_A	241	CB2_B	277	V_{SS}
26	V_{SS}	62	ALERT_n	98	CB1_B	134	V_{SS}	170	DQ14_A	206	V_{SS}	242	V_{SS}	278	DQ26_B
27	DQ13_A	63	V_{SS}	99	V_{SS}	135	DQ25_B	171	V_{SS}	207	RESET_n	243	CB3_B	279	V_{SS}

Table 3: Pin Assignments (Continued)

288-Pin DDR5 RDIMM Front								288-Pin DDR5 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
28	V_{SS}	64	CS0_A_n	100	DQ0_B	136	V_{SS}	172	DQ15_A	208	V_{SS}	244	V_{SS}	280	DQ27_B
29	DQ16_A	65	V_{SS}	101	V_{SS}	137	DQS3_B_t	173	V_{SS}	209	CS1_A_n	245	DQ2_B	281	V_{SS}
30	V_{SS}	66	CA0_A	102	DQ1_B	138	DQS3_B_c	174	DQ18_A	210	V_{SS}	246	V_{SS}	282	DQS8_B_c, TDQS8_B_c
31	DQ17_A	67	V_{SS}	103	V_{SS}	139	V_{SS}	175	V_{SS}	211	CA1_A	247	DQ3_B	283	DQS8_B_t, TDQS8_B_t,
32	V_{SS}	68	CA2_A	104	DQS0_B_t	140	DQ28_B	176	DQ19_A	212	V_{SS}	248	V_{SS}	284	V_{SS}
33	DQS2_A_t	69	V_{SS}	105	DQS0_B_c	141	V_{SS}	177	V_{SS}	213	CA3_A	249	DQS5_B_c, TDQS5_B_c	285	DQ30_B
34	DQS2_A_c	70	CA4_A	106	V_{SS}	142	DQ29_B	178	DQS7_A_c, TDQS7_A_c	214	V_{SS}	250	DQS5_B_t, TDQS5_B_t	286	V_{SS}
35	V_{SS}	71	V_{SS}	107	DQ4_B	143	V_{SS}	179	DQS7_A_t, TDQS7_A_t	215	CA5_A	251	V_{SS}	287	DQ31_B
36	DQ20_A	72	CA6_A	108	V_{SS}	144	RFU	180	V_{SS}	216	V_{SS}	252	DQ6_B	288	V_{SS}

Notes: 1. On modules with nominal transfer rates <6400 MT/s, this pin is RFU. On modules with nominal transfer rates ≥6400 MT/s, this pin is NPP (no pin present).

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR5 RDIMM/LRDIMM devices. All pins listed may not be supported on a specific module depending on DIMM type (RDIMM vs. LRDIMM), configuration, and density.

Table 4: Pin Descriptions

Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	V_{DD}	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	DDR Input	V_{DD}	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands.
CS[1:0]_A CS[1:0]_B	Input	V_{DD}	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}.
PAR_A PAR_B	Input	V_{DD}	**Command and Address Parity Input**: The RCD supports even parity check devices prior to forwarding commands to the DRAM. Once enabled on the RCD, the RCD calculates parity. Input parity should be maintained at the rising edge of the clock and at the same time with command and address with CSx_x_n LOW.
ALERT_n	Output	V_{DD}	**Alert:** If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	CMOS Input	V_{DD}	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
PCAMP	Input/ Output	V_{DD}	**Control and Monitor Port:** Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	Input	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Clock:** Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Data:** I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	**Host Sideband Bus Device ID:** Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.

Table 4: Pin Descriptions (Continued)

Symbol	Type	I/O Level	Description
DQ[31:0]_A DQ[31:0]_B	Input/ Output	V_{DD}	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0–DQ3 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	V_{DD}	**ECC Check Bits Input/Output:** Bidirectional data bus. On x72 ECC DIMMs. only 4 check bits per sub channel are present.
DQS[9:0]_A_t DQS[9:0]_B_t DQS[9:0]_A_c DQS[9:0]_B_c	Input/ Output	V_{DD}	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
TDQS[9:5]_A_t TDQS[9:5]_B_t TDQS[9:5]_A_c TDQS[9:5]_B_c	Input/ Output	V_{DD}	**Termination Data Strobe:** Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs. On DDR5, TDQS_t is a shared function with DM_n. Refer to the DRAM component data sheet for shared pin functionality.
LBDQ	Output	V_{DDQ}	**Loopback data output:** The output of this device on the loopback output select defined in MR53:OP[4:0]. When loopback is enabled, it is in driver mode using the default R_{ON} described in the loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
LBDQS	Output	V_{DDQ}	**Loopback data strobe output:** This is a single-ended strobe with the rising edge aligned with loopback data edge, falling edge aligned with data center. When loopback is enabled, it is in driver mode using the default R_{ON} described in the loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
VIN_BULK	Supply		**External Power Supply:** 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply		**External Power Supply:** 3.3V, 3.0V (min), 3.6V (max)
V_{SS}	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			**No connect:** No internal electrical connection is present.
NF			**No function:** May have internal connection present, but has no function.

Address Mapping to DRAM

Address Mirroring

DDR5 SDRAM has an MIR input pin. This pin is strapped (connected) to V_{SS} or V_{DDQ} on the PCB. This pin is used to inform the SDRAM device that it is being configured for mirrored mode vs. standard mode. With the MIR pin strapped to V_{DDQ}, the SDRAM internally swaps even-numbered CA with the next higher odd number CA. Normally, the MIR pin must be strapped to V_{SS} if no CA mirror is required. On registered DDR5 modules, the RCD will expand the incoming host-interface 7-bit DDR (Double data rate) CA bus (edge connector CA[6:0]) to 14 bits on the DRAM interface. The following table illustrates how the edge connector pin maps to the DRAM physical CA pins and internal CA function through the DDR input to the RCD (UI0 vs. UI1).

Table 5: Address Mirroring

Edge Connector Pin		Unmirrored DRAM (MIR = V_{SS})		Mirrored DRAM (MIR = V_{DDQ})	
		Physical Pin Connected	Internal Function	Physical Pin Connected	Internal Function
UI0	CA0	CA0	CA0	CA1	CA0
	CA1	CA1	CA1	CA0	CA1
	CA2	CA2	CA2	CA3	CA2
	CA3	CA3	CA3	CA2	CA3
	CA4	CA4	CA4	CA5	CA4
	CA5	CA5	CA5	CA4	CA5
	CA6	CA6	CA6	CA7	CA6
UI1	CA0	CA7	CA7	CA6	CA7
	CA1	CA8	CA8	CA9	CA8
	CA2	CA9	CA9	CA8	CA9
	CA3	CA10	CA10	CA11	CA10
	CA4	CA11	CA11	CA10	CA11
	CA5	CA12	CA12	CA13	CA12
	CA6	CA13	CA13	CA12	CA13

SPD EEPROM Hub and Integrated Thermal Sensor Operation

SPD EEPROM Hub Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function (SPD5 Hub) with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte, JEDEC JC-42.4-compliant EEPROM that is arranged as 16 blocks of 64 bytes per block, and each block may optionally be write-protected via software command. The SPD content is aligned with these blocks, as shown in the table below.

Block	Range		Description
0	0~63	0x000~0x03F	Base configuration and DRAM parameters
1	64~127	0x040~0x07F	Base configuration and DRAM parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0D0~0x0FF	Standard module parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard module parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard module parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard module parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FF	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End user programmable
11	704~767	0x2C0~0x2FF	End user programmable
12	768~831	0x300~0x33F	End user programmable
13	832~895	0x340~0x37F	End user programmable
14	896~959	0x380~0x3BF	End user programmable
15	960~1023	0x3C0~0x3FF	End user programmable

The first 640 bytes are programmed by Micron to comply with JEDEC standard JESD400-5, "DDR5 Serial Presence Detect (SPD) Contents." The remaining 384 bytes of storage are available for use by the end user.

The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM).

Micron implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected.

Integrated Thermal Sensor Operations

The integrated thermal sensor (TS) continuously monitors the temperature of the module PCB and updates the temperature data register. Temperature data may be read from the bus host at any time, which provides the host real-time feedback of the module's temperature. Multiple programmable and read-only temperature registers can be used to create a custom temperature-sensing solution based on system requirements. Refer to the DDR5 SPD5 Hub spec for detailed information on configuring and reading the integrated thermal sensor.

Registering Clock Driver Operation

Registered DDR5 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR5 RCD specification. Refer to the JESD82-511 (DDR5RCD01) and JESD82-512 (DDR5RCD02) specifications for more detail.

To reduce the electrical load on the host memory controller's command, address, and control bus, Micron's RDIMMs and LRDIMMs utilize a DDR5 registering clock driver (RCD). The RCD presents a single load to the controller while redriving signals to the DDR5 SDRAM devices, which helps enable higher densities and increase signal integrity. The RCD also provides a low-jitter, low-skew PLL that redistributes a differential clock pair to multiple differential pairs of clock outputs.

Control Words

The RCD device used on DDR5 RDIMMs and LRDIMMs contains configuration registers known as control words, which the host uses to configure the RCD based on criteria determined by the module design. Control words can be programmed by the host controller through either the DRAM command/address bus via mode register write (MRW) or the I3C-basic/I2C sideband bus interface. The RCD sideband bus interface resides on the same sideband bus interface as the module temperature sensor, SPD hub, and PMIC.

Parity Operations

The RCD includes a parity-checking function. By default, when device is put in I3C-basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. The RCD receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified command/address inputs; it indicates on its open-drain ALERT_n pin whether a parity error has occurred. If parity checking is enabled, the RCD forwards commands to the SDRAM when no parity error has occurred. If the parity error function is disabled, the RCD forwards sampled commands to the SDRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled. Parity is checked separately on the two sub-channels for both 1UI and 2UI command. A parity error on one sub-channel does not affect the operation of the other sub-channel.

Rank Addressing

Two chip select inputs per sub-channel (CS0_n and CS1_n) on Micron's modules are used to select a specific rank of DRAM. Each sub-channel has two chip select inputs (CS0x_n and CS1x_n).

Power Management Integrated Circuit Operation

The power management integrated circuit (PMIC) is new for DDR5. This operation converts a 12V supply into regulated values for components on the module. For LRDIMMs and RDIMMs, there are two devices defined within JEDEC: the PMIC5000 (high output power) and PMIC5010 (low output power). The PMIC5010 can support up to 15.3W of average power and the PMIC5000 can support up to 25.5W of average power. Both PMIC variants utilize the same pinout and 5mm x 5mm FCQFN package. The PMIC also allows the host to monitor voltage and current via the sideband channel. Refer to the PMIC5000, PMIC5010 JEDEC specification for full details.

The PMIC has two supply inputs, a 3.3V VIN_Mgmt supply and the 12V nominal supply from the card edge through VIN_Bulk. The VIN_Mgmt is used for internal operation of the PMIC and to generate LDO voltages.

The PMIC allows the DIMM manufacturer to set the target voltage levels for the DRAM and configure the ramp up and ramp down aspects of each power rail. For power up, each voltage rail can be configured in offsets of 2ms increments, and for power down, in increments of 1ms. Note, there will be independent power planes for all LRDIMM and RDIMM layouts. The DRAM supply inputs will be connected to the PMIC switch regulator outputs. The specific switch regulator output connection implementation may be raw-card dependent. The RCD and data buffers will be connected to V_{DDQ} plane. The PMIC has a CAMP (Control and Monitor Port) multi-purpose pin which is an open drain and will have an external pull-up.

As an output only, when the VIN_Mgmt input reaches a valid level, the PMIC will drive CAMP LOW until after the VR ENABLE command and all DRAM voltages are stable, indicating a successful initialization. At this time, the PMIC releases the CAMP signal and allows it to float HIGH (external pull-up resistor on the host side will pull it HIGH). At anytime thereafter if VIN_Bulk drops below a set threshold, or any of the regulated supplies fall out of specification, the PMIC will drive the CAMP signal LOW to flag the host. When the Fail_n function is enabled and regardless of Write Protect Feature, the PMIC also uses the CAMP signal as a command to disable the PMIC output regulators.

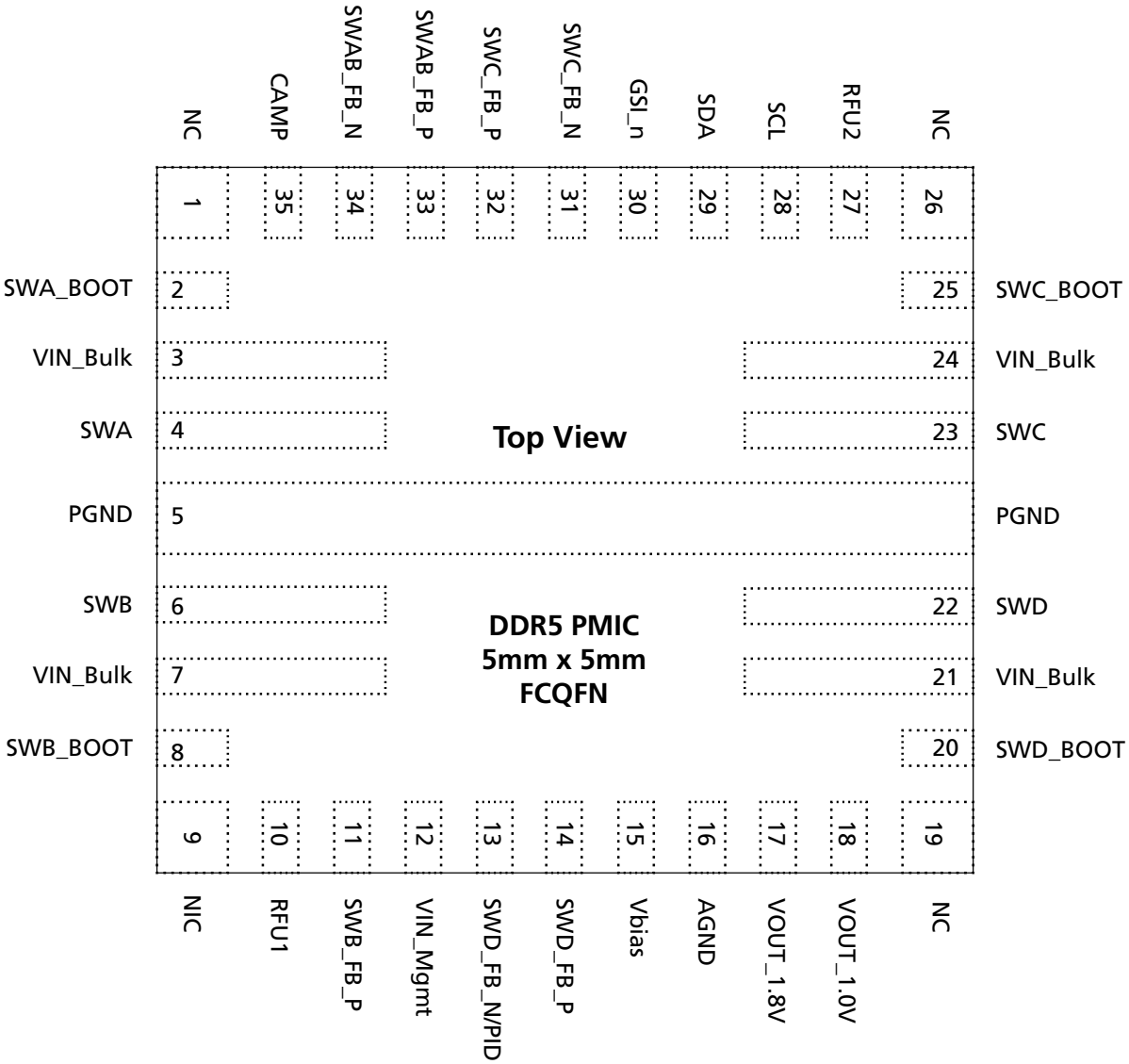
By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed. There are three address configurations for the PMIC Address ID (PID), device pin #13. See the table below for options.

Table 6: PMIC Addressing

PID Configuration (Pin #13)	PMIC Address ID (PID)			
	Bit 7	Bit 6	Bit 5	Bit 4
Pin to V_{SS}	1	0	0	1
Pin to 1.8V	1	1	0	0
Pin Floating	1	0	0	0

The PMIC has multiple sets of registers, primarily the DIMM vendor region and the host region. The vendor region is used to set up the voltage ramps, supply rail values, and threshold settings. Host can also set various registers to flag critical operation conditions and to help debug. The PMIC can only be programed while the CAMP signal is satisfied with the Write Protect Function enabled; after the VR ENABLE command has been issued, the device locks out the ability to change the contents of most registers.

Figure 2: PMIC Package



TS5 Serial Bus Temperature Sensor Operation

TS5 Temperature Sensor Operation

The TS5 (Fifth generation temperature sensor) devices incorporate thermal sensing capability which is controlled and read over two-wire bus. TS5 device operate from a nominal 1.8V nominal power supply (V_{DDSPD}) and a 1.0V nominal power supply (V_{DDIO}). The TS5 device is intended to operate up to 12.5 MHz on a 1.0V I3C-basic bus or up to 1 MHz on a 1.0V to 3.3 V (Grade dependent) I2C bus. The TS5 devices are intended to interface to I2C or I3C-basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus. All TS5 devices respond to specific pre-defined device select codes on the two-wire bus. Refer to the latest version of JEDEC JESD302-1 TS511x specification for more details.

Micron DDR5 based RDIMMs and LRDIMMs have two temperature sensors (identified as TS0, TS1 on the DIMM). Each temperature sensor is placed strategically near each end of the DIMM embedded between the memory components in order to account for proximity to sub-channel A and B.

Thermal Characteristics

Table 7: DDR5 SDRAM Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	DRAM Commercial operating case temperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	DRAM operating temperature range	0 to 95	°C	5, 7, 8
T_{STG}	DRAM Non-operating storage temperature	–55 to 100	°C	6

Notes: 1. Maximum operating case temperature; T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. The refresh rate must double when 85°C < T_C ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
7. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions for the commercial offering.
8. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.

DDR5 Module Capacitor Operating Temperature

Micron DDR5 SDRAM Modules use X5R capacitors which are limited to a maximum operating case temperature rating of 85C. All other components on the DIMM meet or exceed the DDR5 SDRAM maximum commercial operating case temperature rating of 95C. The JEDEC DIMM design specifications require all non-DRAM components are maintained within their respective operating temperature ratings when the case temperature of the DRAMs are at their minimum and maximum specified values.

DRAM Operating Conditions

AC operating conditions are provided in the DDR5 component data sheets. Please refer to both the DDR5 Product Core Data Sheet and the Die Revision-Specific Data Sheet Addendum. Component specifications are available at micron.com.

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

DRAM operating voltages are generated by an on-DIMM PMIC component. Power to the PMIC is provided through the VIN_BULK (12V for RDIMMs and LRDIMMs, 5V for UDIMMs and SODIMMs) and 3.3V VIN_MGMT (LRDIMMs and RDIMMs only) edge connector pins. Designers must account for any system voltage drops at anticipated power levels to ensure the required V_{IN} supply voltage is maintained.

SPD EEPROM Hub and Integrated Thermal Sensor Operating Conditions

The thermal sensor continuously monitors the module's temperature and can be read back at any time over the sideband bus shared with the serial presence-detect (SPD) EEPROM. Refer to JESD300-5 SPD5118 device specification for complete details.

SPD Data

For the latest SPD data, refer to Micron's SPD page: micron.com/SPD.

Table 8: SPD EEPROM Hub and Integrated Thermal Sensor Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	1.7	1.8	1.98	V
Supply voltage	V_{DDIO}	0.95	1.0	1.05	V
Input low voltage	V_{IL}	–0.35	–	0.3	V
Input high voltage	V_{IH}	0.7	–	3.6	V
Output low voltage	V_{OL}	–	–	0.3	V
Output high voltage	V_{OH}	0.75	–	–	V
Input leakage current	I_{LI}	–	–	±5	µA
Output leakage current	I_{LO}	–	–	±5	µA

Table 9: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	I2C Mode - Open Drain		I3C Basic Push-Pull		Units
		Min	Max	Min	Max	
Clock frequency	^{f}SCL	0.01	1	0	12.5	MHz
Clock pulse width HIGH time	$^{t}HIGH$	260	–	35	–	ns
Clock pulse width LOW time	^{t}LOW	500	–	35	–	ns
Detect clock LOW timeout	$^{t}TIMEOUT$	10	50	10	50	ns
SDA rise time	^{t}R	–	120	–	5	ns
SDA fall time	^{t}F	–	120	–	5	ns
Data-in setup time	$^{t}SU:DAT$	50	–	8	–	ns
Data-in hold time	$^{t}HD:DI$	0	–	3	–	ns
Data out hold time	$^{t}HD:DAT$	0.5	350	N/A	N/A	ns
Start condition setup time	$^{t}SU:STA$	260	–	12	–	ns
Start condition hold time	$^{t}HD:STA$	260	–	30	–	ns
Stop condition setup time	$^{t}SU:STO$	260	–	12	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	500	–	ns
Write time	^{t}W	–	5	–	5	ms

Table 9: Temperature Sensor and EEPROM Serial Interface Timing (Continued)

Parameter/Condition	Symbol	I2C Mode - Open Drain		I3C Basic Push-Pull		Units
		Min	Max	Min	Max	
Warm power cycle time off	$^{t}POFF$	1	–	1	–	ms
Time from power-on to first command	$^{t}INIT$	10	–	10	–	ms

Table 10: Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Units
Storage temperature	V_{DDSPD}	-65	150	°C
Supply voltage	V_{DDIO}	-0.5	2.1	V
Supply voltage	V_{DDSPD}	–0.5	2.1	V
HSA pin	HSA	–0.5	2.1	V
HSCL, HSDA, LSCL, LSDA pins	HSCL, HSDA, LSCL, LSDA	–0.5	3.6	V

Registering Clock Driver Operating Conditions

Table 11: Registering Clock Driver Electrical Characteristics

Symbol	Parameter	Min	Nom	Max	Units
V_{DD}	DC supply voltage	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 sideband interface I/O supply voltage	0.95	1.0	1.05	V
V_{IL}	Input low voltage (SCL, SDA)	–0.35	-	0.3	V
V_{IH}	Input high voltage (SCL, SDA)	0.7	-	1.3	V
V_{OL}	Output low voltage (SDA)	-	-	0.3	V
V_{OH}	Output high voltage (SDA)	V_{DDIO} - 0.3	-	-	V
T_J	Junction temperature	0	-	125	°C
T_{case}	Case temperature	-	-	103	°C

Table 12: Registering Clock Driver Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	–0.3	1.4	V
V_{IN}	Receiver input voltage	–0.3	V_{DD} + 0.5	V
V_{OUT}	Driver output voltage	–0.3	V_{DD} + 0.5	V
I_{IK}	Input clamp current	-	-50	mA
I_{OK}	Output clamp current	-	±50	mA
I_{OUT}	Continuous output current	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or V_{SS} pin	-	±100	mA
T_{stg}	Storage temperature	–55	100	°C

Power Management Integrated Circuit Operating Conditions

Due to the PMIC capability, 12V is the nominal supply to the PMIC from the host through the edge connector pins. The output voltage levels from the PMIC are expected to operate within ±2.5% in order to satisfy the DRAM voltage requirement range of –3% to +6%.

Table 13: PMIC 50x0 Input Supply Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk input supply voltage – DC voltage	VIN_Bulk	4.25	12	15	V	1, 2
Bulk input supply maximum – AC voltage	VIN_Bulk_AC	-	-	18	V	
Bulk input supply maximum voltage – start up overshoot	VIN_Bulk_OS_Startup	-	-	33	V*µs	3
Bulk input supply voltage – ramp up rate	VIN_Bulk_Ramp_Up	0.1	-	3	V/ms	4
Bulk input supply voltage – ramp down rate	VIN_Bulk_Ramp_Down	-	-	1	V/ms	5
Management input supply voltage	VIN_Mgmt	3	3.3	3.6	V	6
Management input supply – ramp up and ramp down rate	VIN_Mgmt_Ramp	0.15	-	3	V/ms	
Minimum management input supply current	IVIN_Mgmt	110	-	-	mA	7
Bulk input supply current	IVIN_Bulk	-	-	2.5	A	8

Notes: 1. During first power on, the input voltage supply must reach minimum value based on default from register 0x1A [7:5] + 1.0V for PMIC to detect valid input supply. Refer to the JEDEC PMIC50x0 specification for register implementation detail.
2. The PMIC efficiency is optimized for nominal input supply of 12V or lower. The PMIC efficiency above 13.8V is degraded and thermal impact must be considered. The PMIC operation above 14.2V should not be greater than 20% duty cycle at any time and should be limited to a maximum contiguous period of 10 minutes.
3. The area under the curve above VIN_Bulk = 15V. VIN_Bulk_AC spec must also be satisfied.
4. The ramp up rate between 300mV and 8.0V.
5. The ramp down rate between 8.0V and 300mV.
6. During first power-on, the input voltage supply must reach minimum value of 2.8V for PMIC to detect valid input supply.
7. This is a platform specification. It is the minimum input current delivered by the platform through the DIMM gold finger to deliver the maximum load on LDO outputs (1.8V LDO output + 1.0V LDO output = 25mA + 20mA) plus the current required by the PMIC for its own usage.
8. This is a platform specification. It is the maximum input current delivered by the platform through the DIMM gold fingers.

Table 14: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Bulk input supply voltage – DC voltage	VIN_Bulk	-0.3	16.2	V	
Management input supply voltage	VIN_Mgmt	-0.3	6.0	V	
SWA_FB_P, SWB_FB_P, SWC_FB_P, SWD_FB_P (to AGND) pins	SWA_FB_P, SWB_FB_P, SWC_FB_P, SWD_FB_P	-0.3	2.2	V	
SWAB_FB_N, SWC_FB_N, SWD_FB_N/PID pins	SWAB_FB_N, SWC_FB_N, SWD_FB_N/PID	-0.3	2.2	V	
Control and Monitor Port	CAMP	-0.3	5.0	V	1
SCL, SDA pins (I2C mode only)	SCL, SDA	-0.3	5.0	V	
SCL, SDA pins (I3C mode only)	SCL, SDA	-0.3	2.2	V	

Table 14: Absolute Maximum Ratings (Continued)

Parameter	Symbol	Min	Max	Unit	Notes
AGND, PGND pins	AGND, PGND	-0.3	0.3	V	

Notes: 1. CAMP pins shall withstand the stress when connected to maximum of 15V DC source through 250 Ohm series resistor for 10 seconds.

Table 15: PMIC 50x0 Switch Regulator Voltage Output Settings

Switch Node	Supply	Register	Min	Typ	Max	Unit
SWA	V_{DD}	R21[7:1]	1.095	1.1	1.135	V
SWB	V_{DD}	R23[7:1]	1.095	1.1	1.135	V
SWC	V_{DDQ}	R25[7:1]	1.095	1.1	1.135	V
SWD	V_{PP}	R27[7:1]	1.790	1.8	1.860	V

Notes: 1. Min/Max PMIC output voltage settings are determined based on PMIC output tolerance of ±2.5% as defined in JESD301-1 in order to ensure the DRAM input voltage specification is met.
2. SWA and SWB must be always programmed to the same value. Due to PMIC output tolerance of ±2.5%, the V_{DD} (SWA/SWB) and V_{DDQ}(SWC) difference may not be greater than 10mV in order to guarantee DRAM specification compliance.

TS5 Serial Bus Temperature Sensor Operating Conditions

Operating conditions and electrical characteristics of the TS5 device are defined below.

Table 16: TS5 Temperature Sensor Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DDSPD}	Input supply voltage	1.7	1.8	1.98	V	1
V_{DDIO}	Input supply voltage for I/O	0.95	1.0	1.25	V	2
T_{CASE}	Case operating temperature	–40	-	125	°C	

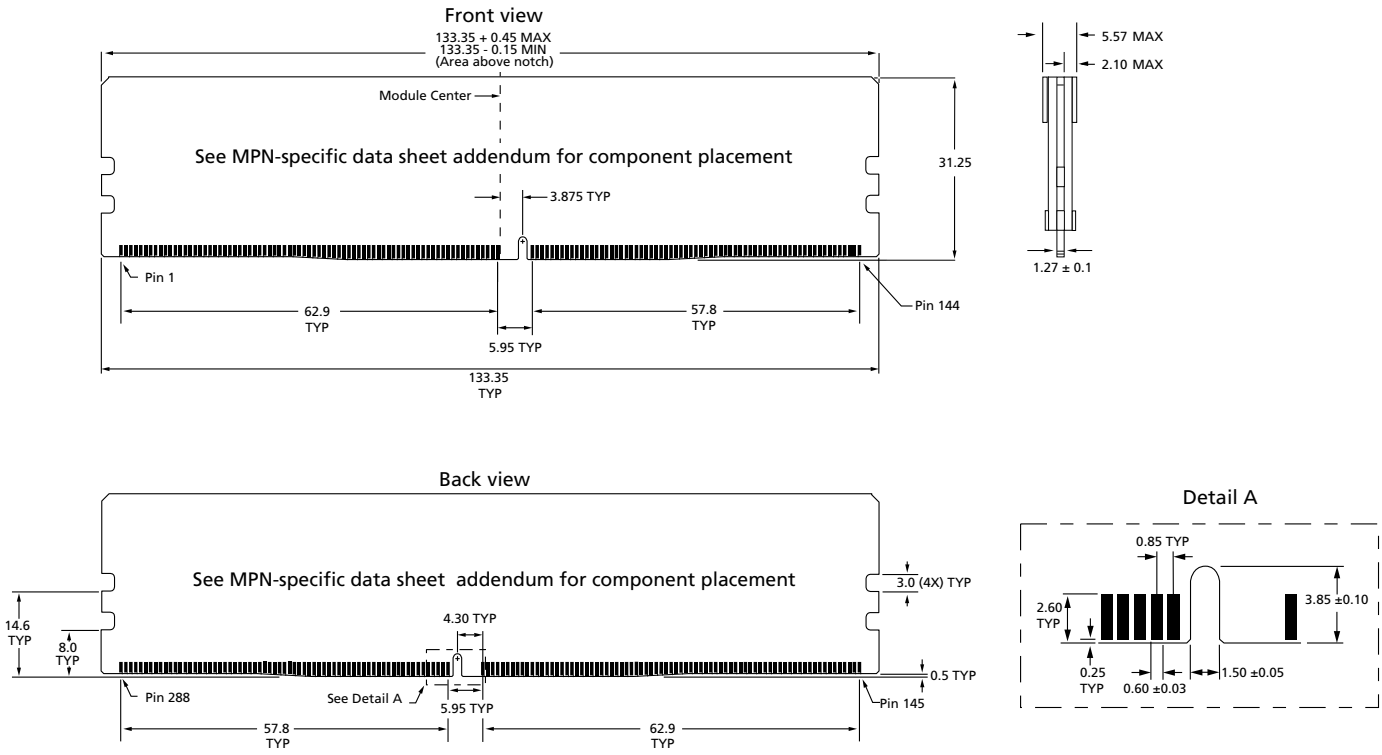
Notes: 1. For DDR5 DIMM application, the DDR5 PMIC V_{OUT} 1.8V setting should be selected such that absolute MIN and MAX values for TS spec are not violated
2. For DDR5 DIMM application, the DDR5 PMIC V_{OUT} 1.0V setting should be selected such that absolute MIN and MAX values for TS spec are not violated.

TS5 Temperature Sensor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	–65	150	°C
V_{DDIO}	Input supply voltage for IO	–0.5	2.1	V
V_{DDSPD}	Input supply voltage	–0.5	2.1	V
SA	SA pin	–0.5	2.1	V
SCL, SDA	SCL, SDA pins (Grade A)	–0.5	3.6	V
SCL, SDA	SCL, SDA pins (Grade B)	–0.5	2.1	V

Module Dimensions

Figure 3: 288-Pin DDR5 RDIMM



Notes: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15 unless otherwise specified.
3. The dimensional diagram is for reference only.

Revision History

Rev G – 05/23

- PC5-6400 added to product family attributes
- Updated Key Timing Parameters table
- Updated Pin Assignment table: for speeds ≥6400 MT/s, pin count is 287 and pin 220 is NPP; for speeds <6400 MT/s, pin count is 288 and pin 220 is RFU
- Removed PMIC VIN_BULK_RAMP_DOWN minimum spec
- Added note to PMIC 50x0 Switch Regulator Voltage Output Settings table

Rev. F – 10/22

- Remove confidential marking
- Update TBD reference from note 2 of Table 13 "PMIC 50x0 Input Supply Characteristics" to align with JESD301-1 Rev 1.8.3.
- Remove "Module and Component Speed Bins" table reference. Micron DDR5 Module and Component MPNs use the same part marking.
- Add table to PMIC 50x0 Operating Conditions topic for Absolute Maximum Ratings.
- Registering Clock Driver Operation updated to include reference to JESD82-512 (DDR5RCD02).
- Removed reference to JC 42.2 in SPD Hub Description.
- Added reference to latest JEDEC JESD302-01 in Temp Sensor Description.
- Added Table to HUB Operating Conditions topic for Absolute Maximum Ratings.
- Converted Speed Grade to Speed Bin, and corresponding data labels to reflect actual speed bin e.g. 48B to 4800B.
- Changed Speed Grades to Speed Bins in Module and Component Speed Grades (Bins) table under DRAM Operating Conditions.
- Input low voltage minimum changed from -0.3 to -0.35 in RCD Operating Conditions.
- Add table to "Power Management Integrated Circuit Operating Conditions" section to specify allowed PMIC output voltage setting range.
- Updated VDDIOmax supply voltage spec from 1.25V to 1.05V and tSU:DAT SPD timing to align with latest JESD300-5 (SPD Hub) spec rev 1.35
- Removed DM pin descriptions since this does not exist in the JEDEC RDIMM common design spec. Updated TDQS description to clarify that DM_n is shared with TDQS_t on the DRAM.

Rev. E – 08/2021

- Added Key Timing Parameters table

Rev. D – 08/2021

- Production Release

Rev. C – 02/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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