# LPDDR5/LPDDR5X SDRAM

## MT62F1536M32D4, MT62F3G32D8, MT62F768M32D2, MT62F768M64D4, MT62F1536M64D8

## Features

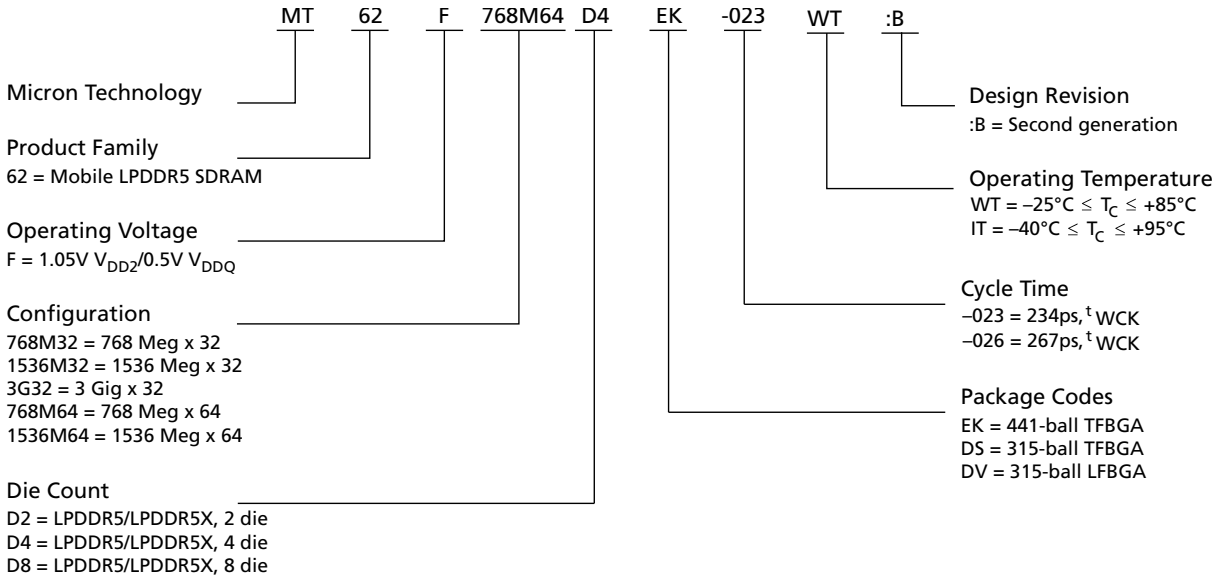
- **Architecture**
  - 17.1 GB/s maximum bandwidth per channel
  - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - $V_{DD1}$ = 1.70–1.95V; 1.80V TYP
  - $V_{DD2H}$ = 1.01–1.12V; 1.05V TYP
  - $V_{DD2L}$ = $V_{DD2H}$ or 0.87–0.97V; 0.90V TYP
  - $V_{DDQ}$ = 0.50V or 0.45V[1] TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, $V_{SS}$ terminated
  - $V_{OH}$-compensated output drive
  - Programmable $V_{SS}$ on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

| Options | Marking |
|---|---|
| **Operating Voltage** | F |
| – $V_{DD1}$/$V_{DD2H}$/$V_{DD2L}$/$V_{DDQ}$/$V_{DDQ}$ (ODT off only):1.80V/1.05V/$V_{DD2H}$ or 0.90V/0.50V or 0.45V[1]/0.30V | |
| **Array configuration** | |
| – 768 Meg x 32 (768M16 x 2Ch x 1R) | 768M32 |
| – 1536 Meg x 32 (768M16 x 2Ch x 2R) | 1536M32 |
| – 3 Gig x 32 (1536M16 x 2Ch x 2R) | 3G32 |
| – 768Meg x 64 (768M16 x 4Ch x 1R) | 768M64 |
| – 1536Meg x 64 (768M16 x 4Ch x 2R) | 1536M64 |
| **Device configuration** | |
| – 2 die in package (768M16 x 2 die) | D2 |
| – 4 die in package (768M16 x 4 die) | D4 |
| – 8 die in package (768M16 x 8 die) | D8 |
| – 8 die in package (1536M8 x 8 die) | D8 |
| **FBGA RoHS-compliant, "green" package** | |
| – 315-ball TFBGA 12.4mm x 15.0mm (TYP) Seated height 1.1mm (MAX) | DS |
| – 315-ball LFBGA 12.4mm x 15.0mm (TYP) Seated height 1.3mm (MAX) | DV |
| – 441-ball TFBGA 14.0mm x 14.0mm (TYP) Seated height 1.1mm (MAX) | EK |
| **Speed grade, cycle time ($^{t}$WCK)** | |
| – 8533 Mb/s | -023 |
| – 7500 Mb/s | -026 |
| **Operating temperature** | |
| – –25°C ≤ $T_C$ ≤ +85°C | WT |
| – –40°C ≤ $T_C$ ≤ +95°C | IT |
| **Revision** | :B |

**Note:** 1. $V_{DDQ}$ = 0.45V (TYP) only supported in 441-ball package up to 6400 Mb/s.

# Part Number Ordering Information

**Figure 1: Part Number Chart**




## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

## LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

# Contents

# List of Figures

# List of Tables

# Important Notes and Warnings

Micron Technology, Inc. ("Micron") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Micron.

**Automotive Applications.** Products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Micron products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

**Critical Applications.** Products are not authorized for use in applications in which failure of the Micron component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Micron component will not result in such harms. Should customer or distributor purchase, use, or sell any Micron component for any critical application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

**Customer Responsibility.** Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Micron products. ALL SEMICONDUCTOR PRODUCTS HAVE INHERENT FAILURE RATES AND LIMITED USEFUL LIVES. IT IS THE CUSTOMER'S SOLE RESPONSIBILITY TO DETERMINE WHETHER THE MICRON PRODUCT IS SUITABLE AND FIT FOR THE CUSTOMER'S SYSTEM, APPLICATION, OR PRODUCT. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or environmental damages will result from failure of any semiconductor component.

**Limited Warranty.** In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.

# General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

$V_{REF}$ indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

# Device Configuration

### Table 1: Die Organization in the Package (x32)

| Die Organization | 768M32 (24 Gb/package) | 1536M32 (48 Gb/package) | 3G32 (96 Gb/package) |
|---|---|---|---|
| Channel A | x16 mode × 1 die | – | – |
| Channel B | x16 mode × 1 die | – | – |
| Channel A, rank 0 | – | x16 mode × 1 die | – |
| Channel B, rank 0 | – | x16 mode × 1 die | – |
| Channel A, rank 1 | – | x16 mode × 1 die | – |
| Channel B, rank 1 | – | x16 mode × 1 die | – |
| Channel A, rank 0 DQ[7:0] | – | – | x8 mode × 1 die |
| Channel A, rank 1 DQ[7:0] | – | – | x8 mode × 1 die |
| Channel B, rank 0 DQ[7:0] | – | – | x8 mode × 1 die |
| Channel B, rank 1 DQ[7:0] | – | – | x8 mode × 1 die |
| Channel A, rank 0 DQ[15:8] | – | – | x8 mode × 1 die |
| Channel A, rank 1 DQ[15:8] | – | – | x8 mode × 1 die |
| Channel B, rank 0 DQ[15:8] | – | – | x8 mode × 1 die |
| Channel B, rank 1 DQ[15:8] | – | – | x8 mode × 1 die |

Notes: 1. Refer to the Package Block Diagram section in this data sheet.

### Table 2: Die Organization in the Package (x64)

| Die Organization | 768M64 (48 Gb/package) | 1536M64 (96 Gb/package) |
|---|---|---|
| Channel A, rank 0 | x16 mode × 1 die | x16 mode × 1 die |
| Channel B, rank 0 | x16 mode × 1 die | x16 mode × 1 die |
| Channel C, rank 0 | x16 mode × 1 die | x16 mode × 1 die |
| Channel D, rank 0 | x16 mode × 1 die | x16 mode × 1 die |
| Channel A, rank 1 | – | x16 mode × 1 die |
| Channel B, rank 1 | – | x16 mode × 1 die |
| Channel C, rank 1 | – | x16 mode × 1 die |
| Channel D, rank 1 | – | x16 mode × 1 die |

Notes: 1. Refer to the Package Block Diagram section in this data sheet.

### Table 3: Die Addressing

| Description | 768M32 (24 Gb/pkg), 1536M32 (48 Gb/pkg), 768M64 (48 Gb/pkg), 1536M64 (96 Gb/pkg) | | | 3G32 (96 Gb/package) | | |
|---|---|---|---|---|---|---|
| Density per die | 12Gb | | | 12Gb | | |
| Bits | 12,884,901,888 | | | 12,884,901,888 | | |
| Bank mode | BG mode | 16B mode | 8B mode | BG mode | 16B mode | 8B mode |
| Configuration | 48Mb × 16 DQ × 4 banks × 4BG | 48Mb × 16 DQ × 16 banks | 96Mb × 16 DQ × 8 banks | 96Mb × 8 DQ × 4 banks × 4BG | 96Mb × 8 DQ × 16 banks | 192Mb × 8 DQ × 8 banks |

**Table 3: Die Addressing (Continued)**

| Description | 768M32 (24 Gb/pkg), 1536M32 (48 Gb/pkg), 768M64 (48 Gb/pkg), 1536M64 (96 Gb/pkg) | | | 3G32 (96 Gb/package) | | |
|---|---|---|---|---|---|---|
| Number of banks | 4 | 16 | 8 | 4 | 16 | 8 |
| Number of bank groups | 4 | 1 | 1 | 4 | 1 | 1 |
| Array prefetch bits | 256 | 256 | 512 | 128 | 128 | 256 |
| Rows per bank | 49,152 | | | 98,304 | | |
| Columns | 64 | | | 64 | | |
| Page size (bytes) | 2048 | 2048 | 4096 | 1024 | 1024 | 2048 |
| Native burst length | 16 | 16 | 32 | 16 | 16 | 32 |
| Number of I/Os | 16 | | | 8 | | |
| Bank address | BA[1:0] | BA[3:0] | BA[2:0] | BA[1:0] | BA[3:0] | BA[2:0] |
| Bank group address | BG[1:0] | – | – | BG[1:0] | – | – |
| Row address | R[15:0] (R14 = 0 when R15 = 1) | | | R[16:0] (R15 = 0 when R16 = 1) | | |
| Column address | C[5:0] | | | C[5:0] | | |
| Burst address | B[3:0] | B[3:0] | B[4:0] | B[3:0] | B[3:0] | B[4:0] |
| Burst starting address boundary | 128-bit | | | 128-bit | | |

Notes: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.
2. Refer to the Speed Grades and Effective Burst Length in General LPDDR5/LPDDR5X Specifications 3.

# Refresh Requirement Parameters

**Table 4: Refresh Requirement Parameters**

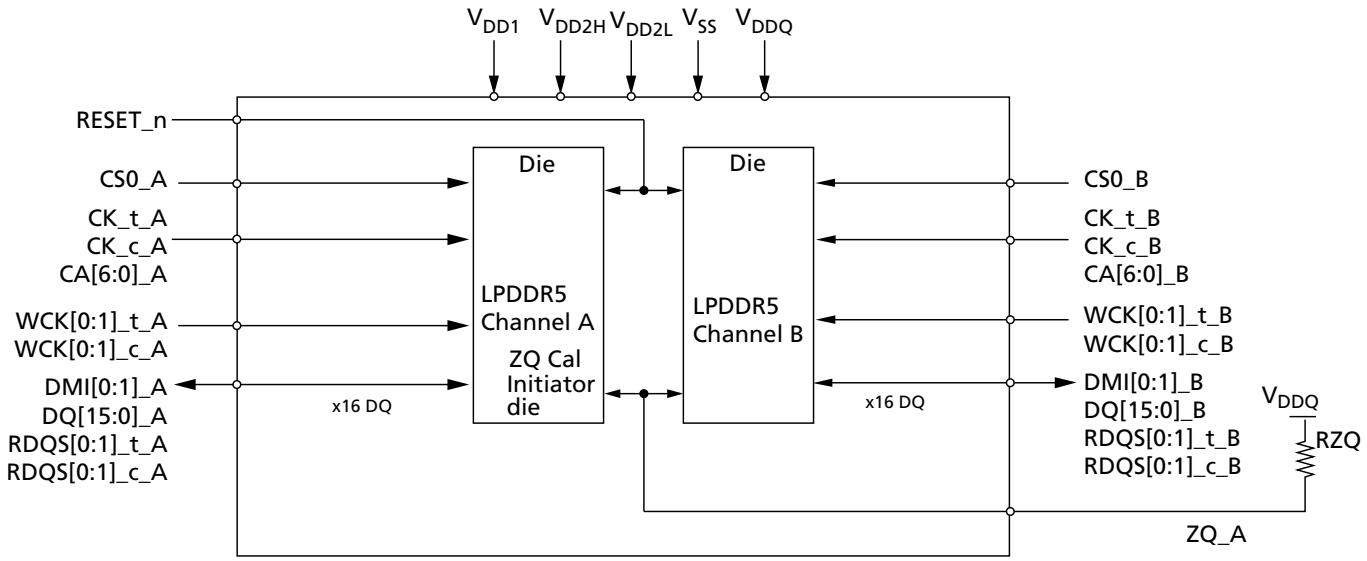
| Parameter | Symbol | 12Gb Die | | Unit |
|---|---|---|---|---|
| | | BG and 16B Mode | 8B Mode | |
| REFRESH cycle time (all banks) | $^{t}$RFCab | 280 | 280 | ns |
| REFRESH cycle time (per bank) | $^{t}$RFCpb | 140 | 140 | ns |
| Per bank refresh to per bank refresh time (different bank) | $^{t}$PBR2PBR | 90 | 90 | ns |
| Per bank refresh to ACTIVATE command time (different bank) | $^{t}$PBR2ACT | 7.5 | 10 | ns |

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

# Package Block Diagrams

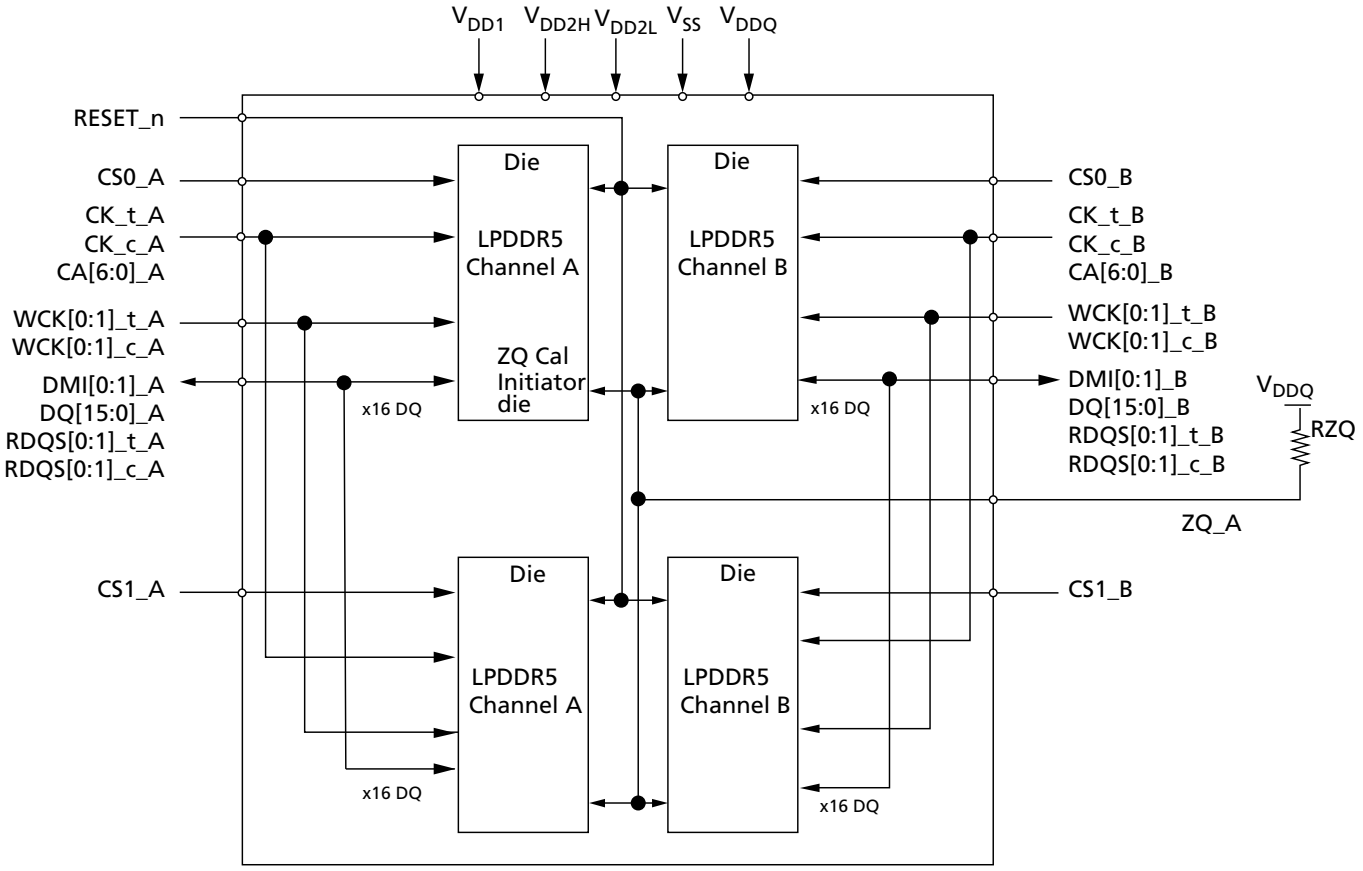
## Dual Die, Dual Channel, Single Rank

**Figure 2: Dual Die, Dual Channel, Single Rank Package Block Diagram**



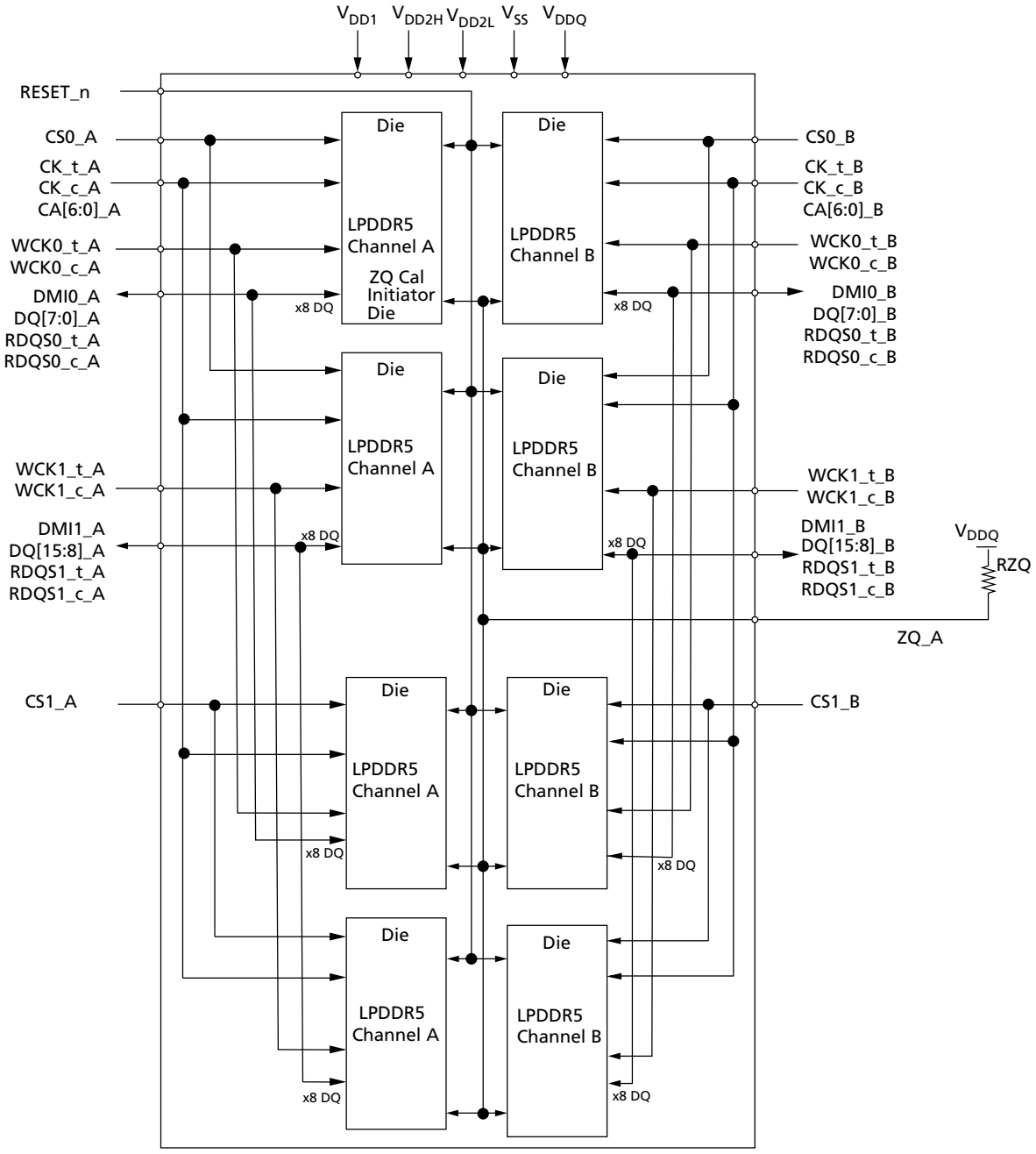
## Quad Die, Dual Channel, Dual Rank

**Figure 3: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram**



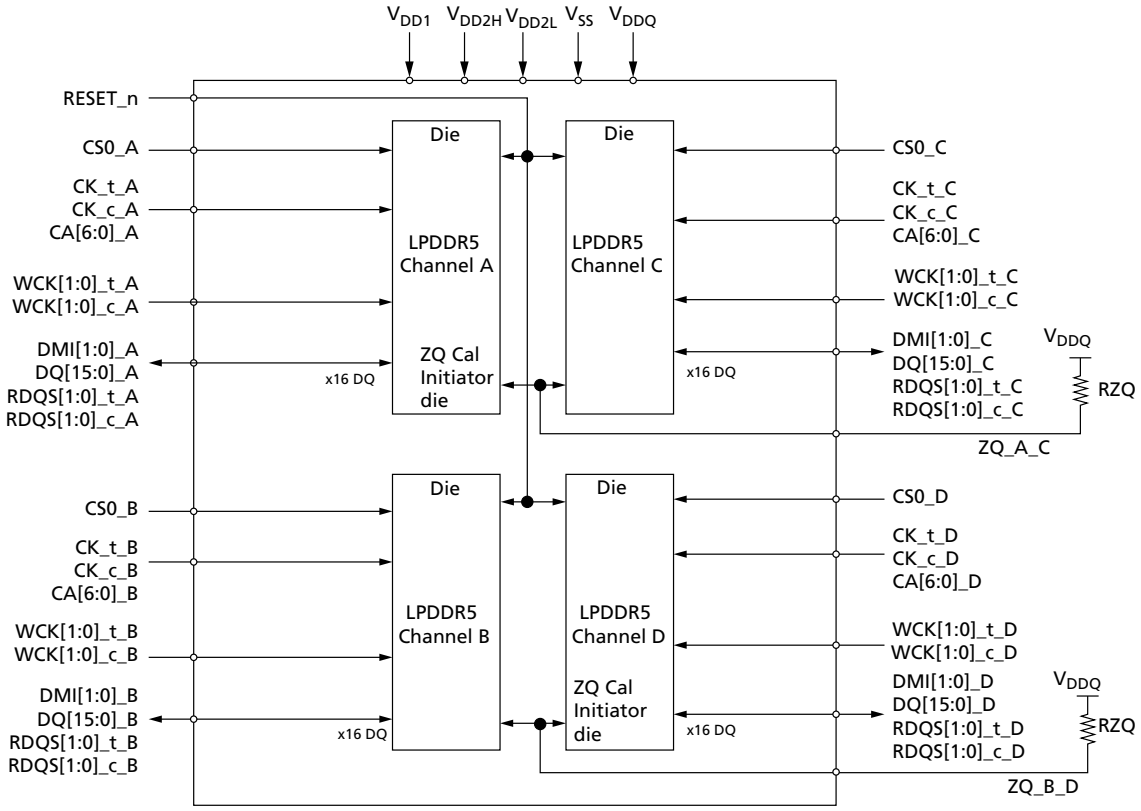
## Eight Die, Dual Channel, Dual Rank

### Figure 4: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram



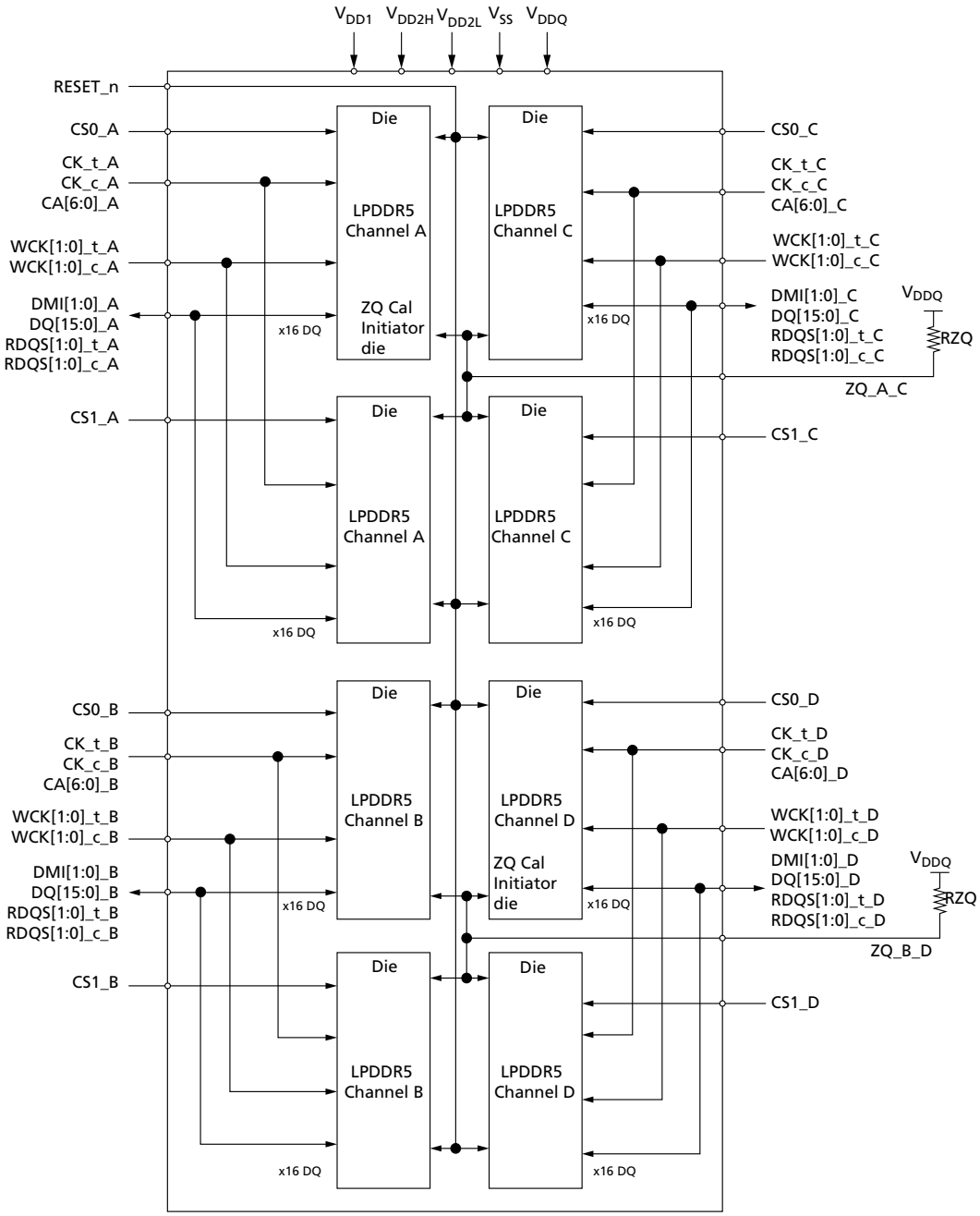
## Quad Die, Quad Channel, Single Rank

### Figure 5: Quad Die, Quad Channel, Single Rank Package Block Diagram



## Eight Die, Quad Channel, Dual Rank

### Figure 6: Eight Die, Quad Channel, Dual Rank Package Block Diagram



# Ball Assignments and Descriptions

**Table 5: 315-Ball/Pad Descriptions**

| Symbol | Type | Description |
|---|---|---|
| CK_t_[A:B]<br>CK_c_[A:B] | Input | **Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c). |
| CS0_[A:B], CS1_[A:B] | Input | **Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package. |
| CA[6:0]_[A:B] | Input | **Command/address inputs:** Provide the command and address inputs according to the command truth table. |
| WCK[1:0]_t_[A:B]<br>WCK[1:0]_c_[A:B] | Input | **Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output. |
| DQ[15:0]_[A:B] | I/O | **Data input/output:** Bidirectional data bus. |
| RDQS[1:0]_t_[A:B]<br>RDQS[1:0]_c_[A:B] | I/O<br>Output | **Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals. |
| DMI[1:0]_[A:B] | I/O | **Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal. |
| ZQ_A | Reference | **ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to $V_{DDQ}$ through a 240Ω ±1% resistor. |
| $V_{DDQ}$, $V_{DD1}$, $V_{DD2H}$, $V_{DD2L}$ | Supply | **Power supplies:** Isolated on the die for improved noise immunity. |
| $V_{SS}$ | Supply | **Ground reference:** Power supply ground reference. |
| RESET_n | Input | **Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal. |
| NC | – | **No connect:** Not internally connected. |

## Figure 7: 315-Ball Dual-Channel Discrete FBGA

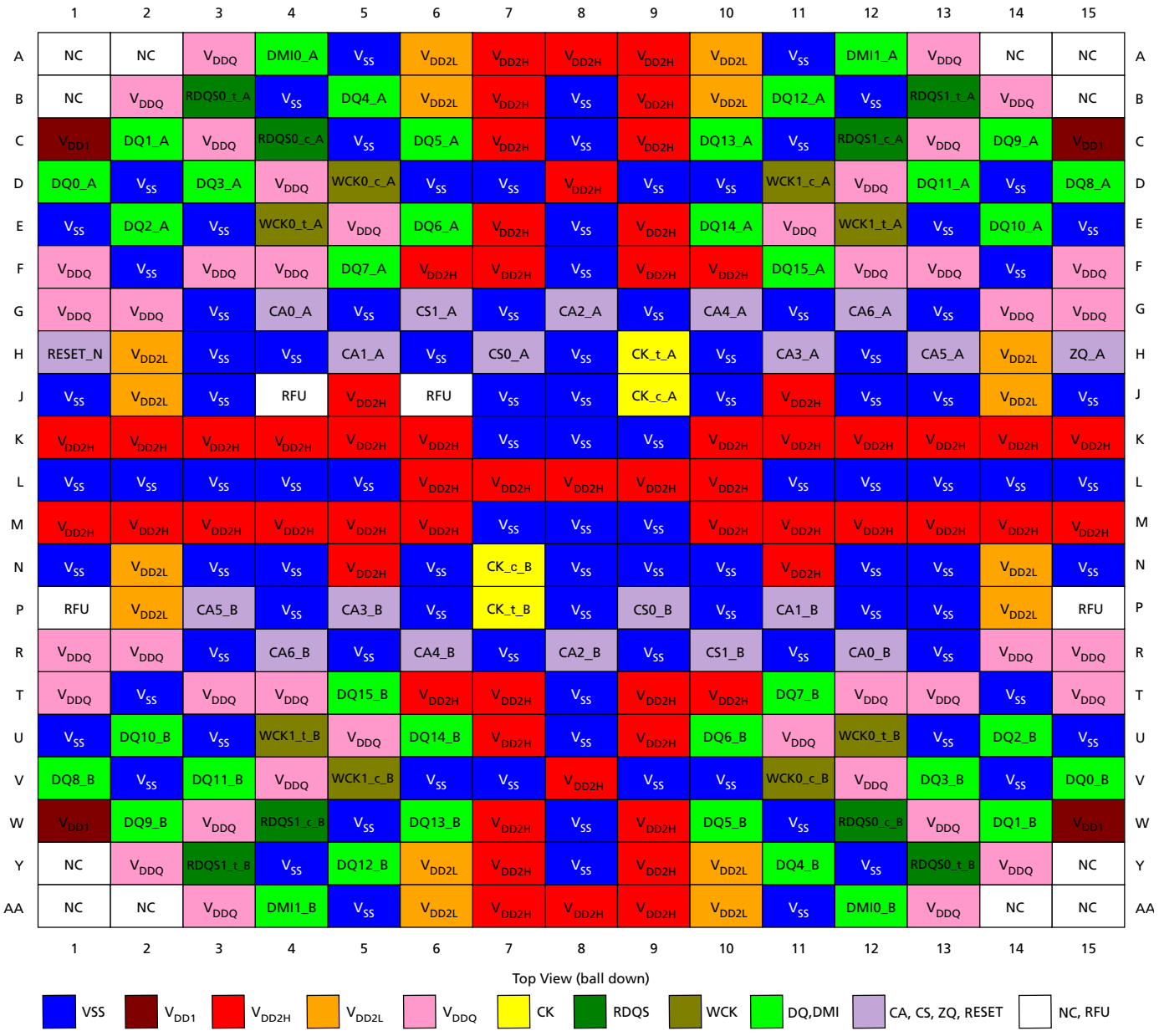
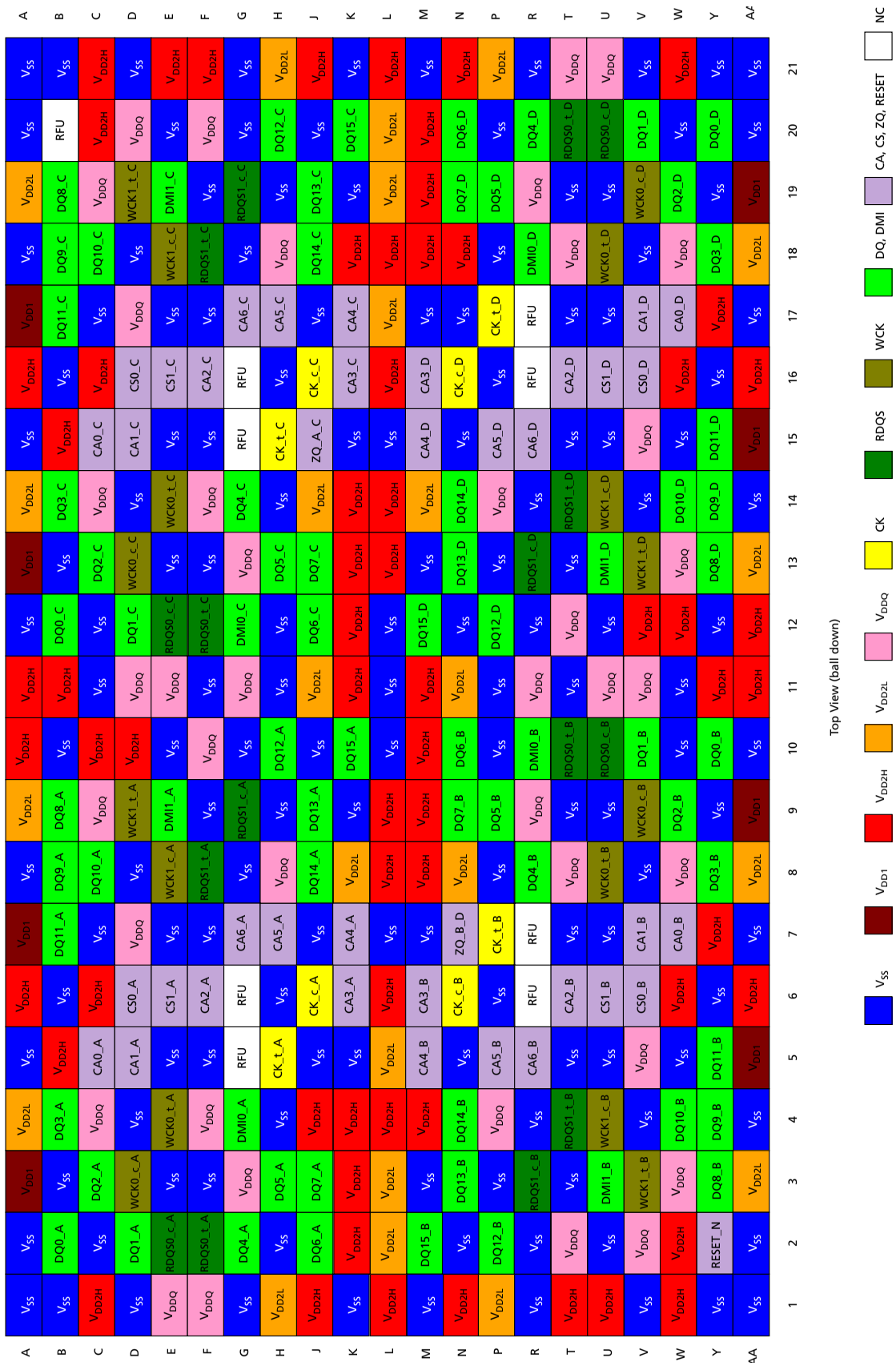


**Table 6:**

| Symbol | Type | Description |
|---|---|---|
| CK_t_[A:D]<br>CK_c_[A:D] | Input | **Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c). |
| CS0_[A:D], CS1_[A:D] | Input | **Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package. |
| CA[6:0]_[A:D] | Input | **Command/address inputs:** Provide the command and address inputs according to the command truth table. |
| WCK[1:0]_t_[A:D]<br>WCK[1:0]_c_[A:D] | Input | **Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output. |
| DQ[15:0]_[A:D] | I/O | **Data input/output:** Bidirectional data bus. |
| RDQS[1:0]_t_[A:D]<br>RDQS[1:0]_c_[A:D] | I/O<br>Output | **Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals. |
| DMI[1:0]_[A:D] | I/O | **Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal. |
| ZQ_A_C, ZQ_B_D | Reference | **ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to $V_{DDQ}$ through a 240Ω ±1% resistor. |
| $V_{DDQ}$, $V_{DD1}$, $V_{DD2H}$, $V_{DD2L}$ | Supply | **Power supplies:** Isolated on the die for improved noise immunity. |
| $V_{SS}$ | Supply | **Ground reference:** Power supply ground reference. |
| RESET_n | Input | **Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal. |
| NC | – | **No connect:** Not internally connected. |
| RFU | – | **Reserved Future Use:** Not internally connected. |

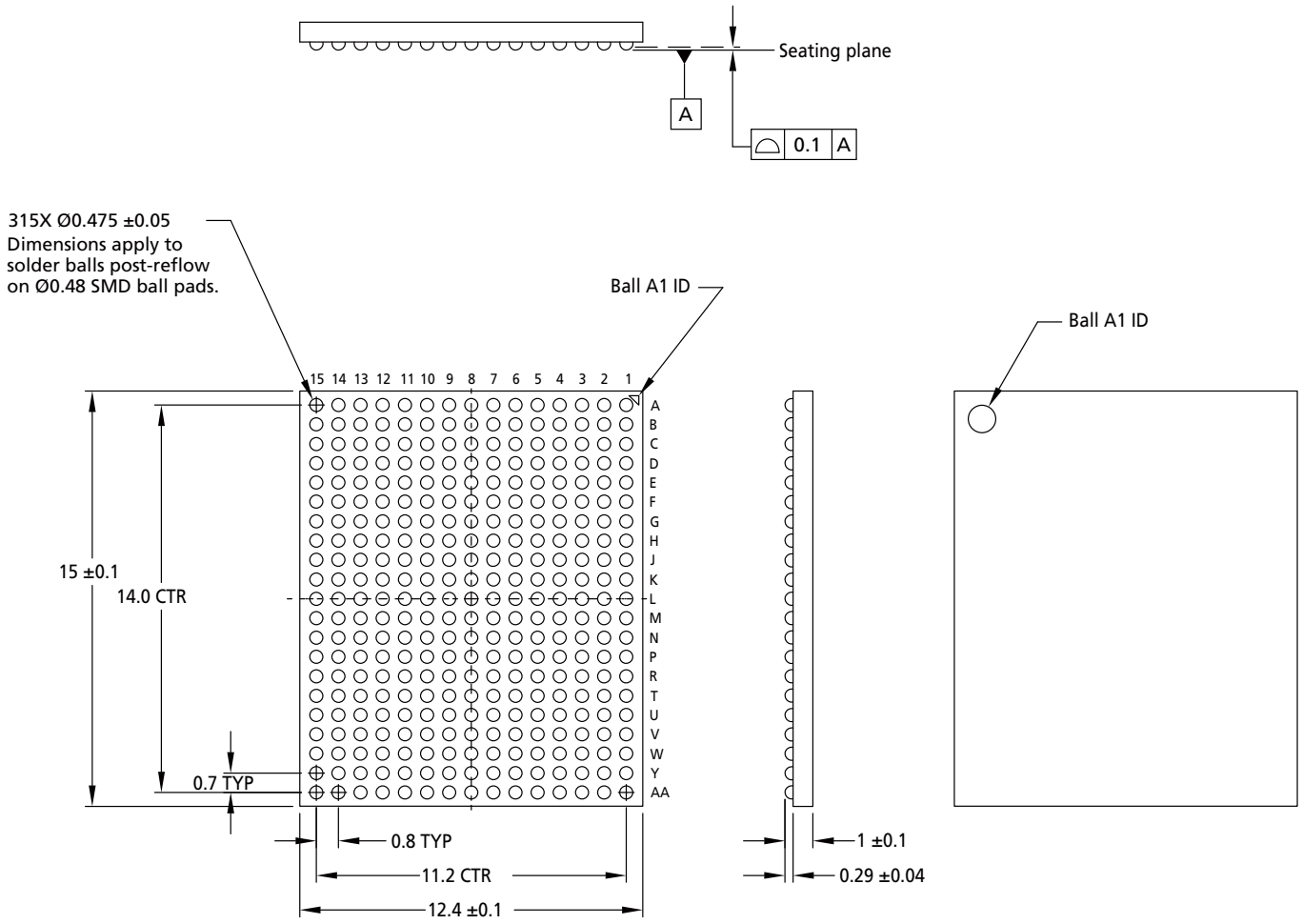
**Figure 8: 441-Ball Quad-Channel FBGA**



# Package Dimensions

## 315-Ball Package (Package Code: DS)

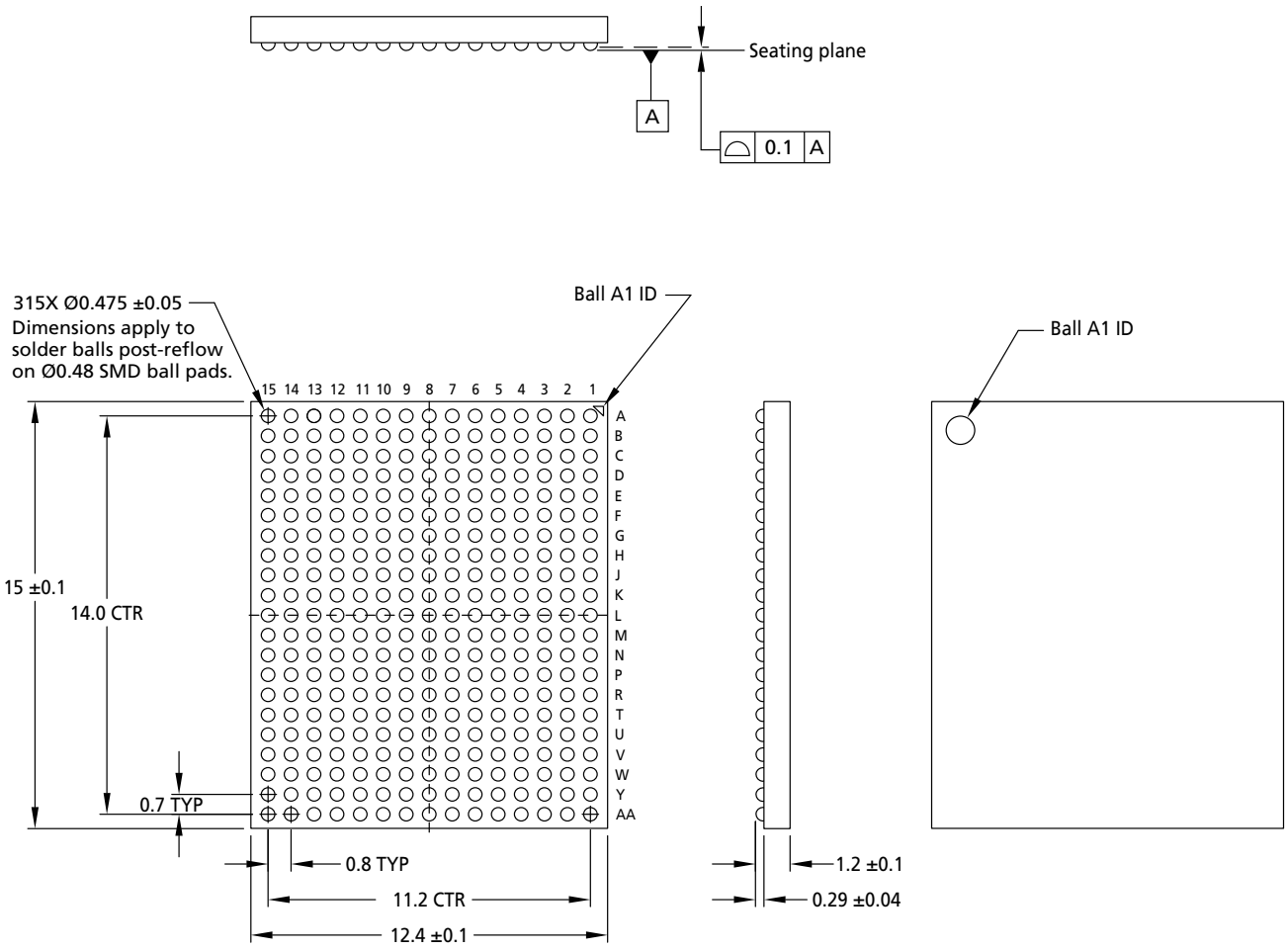
**Figure 9: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)**




Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

## 315-Ball Package (Package Code: DV)

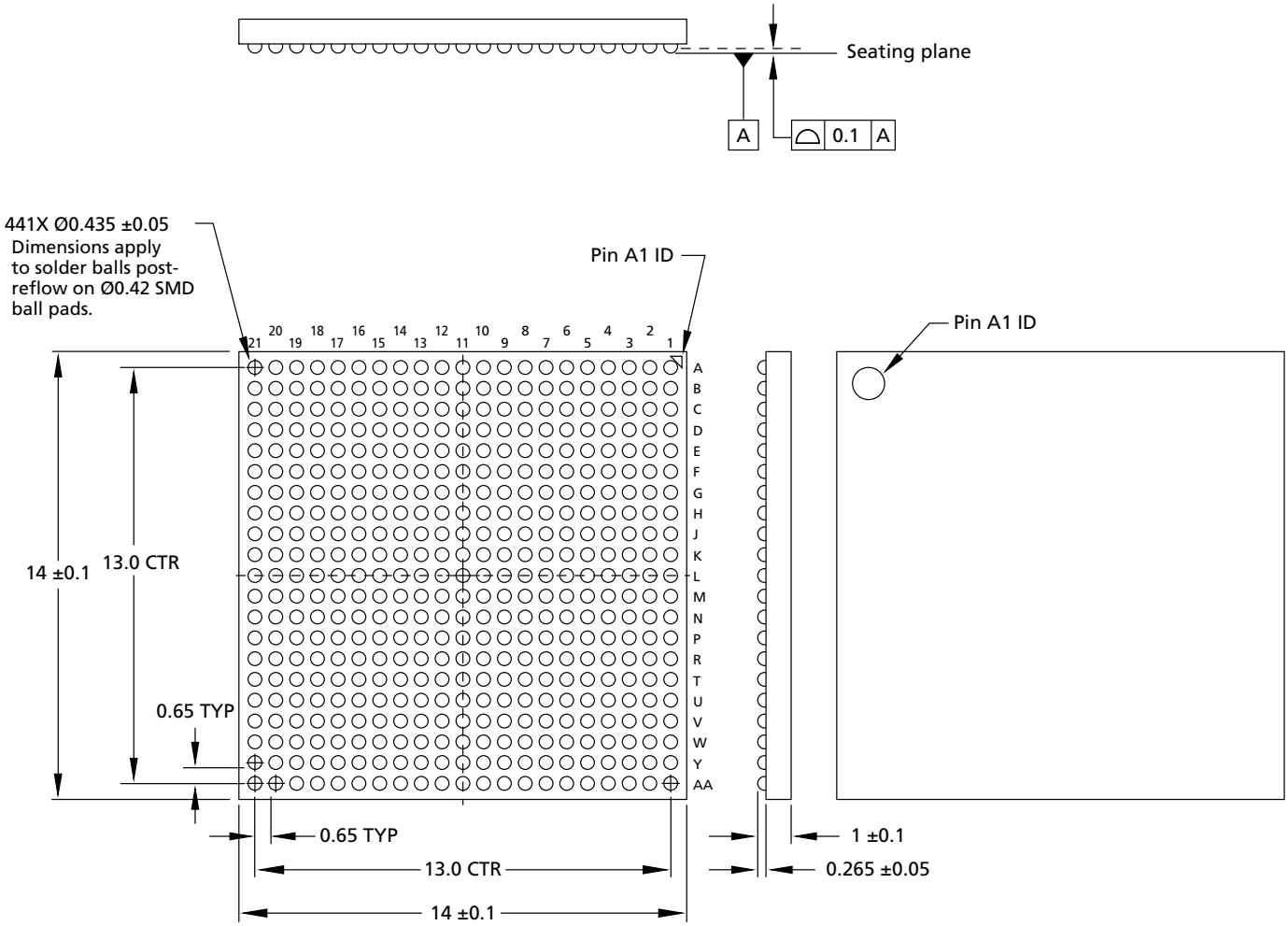
**Figure 10: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)**




Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

## 441-Ball Package (Package Code: EK)

**Figure 11: 441-Ball TFBGA – 14.0mm (TYP) × 14.0mm (TYP) × 1.1mm (MAX) (Package Code: EK)**




Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni)

# Product-Specific Mode Register Definition

**Table 7: Mode Register Contents**

| Mode Register | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR0 | **Per-pin DFE** | **Pre-emphasis** | **Unified NT ODT behavior mode** | **DMI output behavior mode** | **Optimized refresh mode** | **Enhanced WCK always-on mode** | **Latency mode** | **NT ODT timing mode** |
| | OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS | | | | | | | |
| | OP[1] = 0b: Device supports x16 mode latency for 768M32, 1536M32, 768M64, 1536M64<br>OP[1] = 1b: Device supports x8 mode latency for 3G32 | | | | | | | |
| | OP[2] = 1b: Device supports enhanced WCK always-on mode | | | | | | | |
| | OP[3] = 1b: Device supports optimized refresh mode | | | | | | | |
| | OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection | | | | | | | |
| | OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior | | | | | | | |
| | OP[6] = 1b: Device supports pre-emphasis mode | | | | | | | |
| | OP[7] = 0b: Device does not support per-pin DFE | | | | | | | |
| MR1 | | | | | | | **ARFM support** | **CS ODT OP support** |
| | OP[0] = 0b: Device does not support CS ODT behavior OP | | | | | | | |
| | OP[1] = 0b: Device does not support ARFM | | | | | | | |
| MR5 | **Manufacturer ID** | | | | | | | |
| | 1111 1111b: Micron | | | | | | | |
| MR6 | **Revision ID1** | | | | | | | |
| | 0000 0111b | | | | | | | |
| MR8 | **I/O width** | | **Density** | | | | **Type** | |
| | OP[7:6] = 00b: x16 for 768M32, 1536M32, 768M64, 1536M64<br>OP[7:6] = 01b: x8 for 3G32 | | OP[5:2] = 0101b: 12Gb | | | | OP[1:0] = 01b: LPDDR5X SDRAM | |
| MR13 | | | | | | **VRO** | | |
| | OP[2] = 0b: Normal operation (default)<br>1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6 | | | | | | | |
| MR19 | | | **WCK2DQ OSC FM** | | | | | |
| | OP[5] = 1b: WCK2DQ OSC FM supported | | | | | | | |
| MR21 | **WXS** | | | | **ODTD-CSFS** | **WXFS** | **RDCFS** | **WDCFS** |
| | OP[0] = 1b: WRITE DATA COPY function supported | | | | | | | |
| | OP[1] = 1b: READ DATA COPY function supported | | | | | | | |
| | OP[2] = 1b: WRITE X function supported | | | | | | | |
| | OP[3] = 1b: Device ODTD-CS is supported | | | | | | | |
| | OP[7] = 1b: Data to be written can be selected with 0 and 1 | | | | | | | |

**Table 7: Mode Register Contents (Continued)**

| Mode Register | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR22 | **RECC** | | **WECC** | | | | | |
| | OP[5:4] = 00b: Write link ECC disabled (default)<br>01b: Write link ECC enabled (See Note 3) | | | | | | | |
| | OP[7:6] = 00b: Read link ECC disabled (default)<br>01b: Read link ECC enabled (See Note 3) | | | | | | | |
| MR24 | **DFES** | | | | **Read DCA** | | | |
| | OP[3] = 0b: Device does not support Read DCA | | | | | | | |
| | OP[7] = 0b: Device supports DFE | | | | | | | |
| MR26 | | **RDQSTFS** | | | | | | |
| | OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported | | | | | | | |
| MR27 | **RAAMULT** | | **RAAIMT** | | | | | **RFM** |
| | OP[0] = 1b: RFM is required | | | | | | | |
| | OP[5:1] = 01110b: 112 | | | | | | | |
| | OP[7:6] = 01b: 4X | | | | | | | |
| MR43 | | **SBEC rule** | | | | | | |
| | OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted | | | | | | | |
| MR57 | | | | | **RFMSB** | | **RAADEC** | |
| | OP[1:0] = 10b: 2 × RAAIMT | | | | | | | |
| | OP[3:2] = 00b: 1 = Does not support single-bank mode | | | | | | | |
| MR63-R164 | Reserved MR bits MR63 through MR164 are RFU by JEDEC standard and should not be accessed by user. | | | | | | | |

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Write link ECC and read link ECC are supported.

# $I_{DD}$ Parameters

Refer to the $I_{DD}$ Specification Parameters and Test Conditions section in General LPDDR5 Specifications 2 for detailed conditions.

**Table 8: WT $I_{DD}$ Parameters – Single Die**

| Symbol | Supply | x8 Mode Speed Grade | | x16 Mode Speed Grade | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | 7500 Mb/s | 8533 Mb/s | 7500 Mb/s | 8533 Mb/s | | |
| $I_{DD01}$ | $V_{DD1}$ | 3.0 | 3.0 | 4.5 | 4.5 | mA | |
| $I_{DD02H}$ | $V_{DD2H}$ | 27.5 | 27.5 | 28.0 | 28.0 | | |
| $I_{DD02L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD0Q}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2P1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2P2H}$ | $V_{DD2H}$ | 2.0 | 2.0 | 2.0 | 2.0 | | |
| $I_{DD2P2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2PQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2PS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2PS2H}$ | $V_{DD2H}$ | 2.0 | 2.0 | 2.0 | 2.0 | | |
| $I_{DD2PS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2PSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2N1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2N2H}$ | $V_{DD2H}$ | 15.5 | 15.5 | 16.0 | 16.0 | | |
| $I_{DD2N2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2NQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2NS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2NS2H}$ | $V_{DD2H}$ | 15.5 | 15.5 | 16.0 | 16.0 | | |
| $I_{DD2NS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2NSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3P1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD3P2H}$ | $V_{DD2H}$ | 5.5 | 5.5 | 5.5 | 5.5 | | |
| $I_{DD3P2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3PQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3PS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD3PS2H}$ | $V_{DD2H}$ | 5.5 | 5.5 | 5.5 | 5.5 | | |
| $I_{DD3PS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3PSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |

**Table 8: WT $I_{DD}$ Parameters – Single Die**

| Symbol | Supply | x8 Mode Speed Grade | | x16 Mode Speed Grade | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | 7500 Mb/s | 8533 Mb/s | 7500 Mb/s | 8533 Mb/s | | |
| $I_{DD3N1}$ | $V_{DD1}$ | 1.7 | 1.7 | 1.7 | 1.7 | mA | |
| $I_{DD3N2H}$ | $V_{DD2H}$ | 20.5 | 20.5 | 21.0 | 21.0 | | |
| $I_{DD3N2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3NQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3NS1}$ | $V_{DD1}$ | 1.7 | 1.7 | 1.7 | 1.7 | mA | |
| $I_{DD3NS2H}$ | $V_{DD2H}$ | 20.5 | 20.5 | 21.0 | 21.0 | | |
| $I_{DD3NS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3NSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD4R1}$ | $V_{DD1}$ | 9.0 | 10.0 | 11.0 | 12.0 | mA | 3, 4 |
| $I_{DD4R2H}$ | $V_{DD2H}$ | 285.0 | 315.0 | 425.0 | 475.0 | | |
| $I_{DD4R2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD4RQ}$ | $V_{DDQ}$ | 58.0 | 63.0 | 116.0 | 126.0 | | |
| $I_{DD4W1}$ | $V_{DD1}$ | 8.0 | 9.0 | 10.0 | 11.0 | mA | 3 |
| $I_{DD4W2H}$ | $V_{DD2H}$ | 200.0 | 220.0 | 280.0 | 310.0 | | |
| $I_{DD4W2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD4WQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD51}$ | $V_{DD1}$ | 17.0 | 17.0 | 17.0 | 17.0 | mA | |
| $I_{DD52H}$ | $V_{DD2H}$ | 115.0 | 115.0 | 115.0 | 115.0 | | |
| $I_{DD52L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5Q}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD5AB1}$ | $V_{DD1}$ | 2.5 | 2.5 | 2.5 | 2.5 | mA | |
| $I_{DD5AB2H}$ | $V_{DD2H}$ | 23.5 | 23.5 | 24.0 | 24.0 | | |
| $I_{DD5AB2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5ABQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD5PB1}$ | $V_{DD1}$ | 2.5 | 2.5 | 2.5 | 2.5 | mA | |
| $I_{DD5PB2H}$ | $V_{DD2H}$ | 23.5 | 23.5 | 24.0 | 24.0 | | |
| $I_{DD5PB2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5PBQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |

Notes: 1. Published $I_{DD}$ values except $I_{DD4RQ}$ are the maximum $I_{DD}$ values speed grade considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. $I_{DD4RQ}$ value is reference only. Typical value. Output load = 5pF; $R_{ON}$ = 40 ohms; $T_C$ = 25°C
5. $V_{DD1}$ = 1.70–1.95V; $V_{DD2H}$ = 1.01–1.12V; $V_{DD2L}$ = 0.87–0.97V; $V_{DDQ}$ = 0.47–0.57V; $T_C$ = –25°C to +85°C

6. Notes 1 and 2 apply to entire table.

### Table 9: WT Full-Array Power-Down Self Refresh Current – Single Die

| Temperature | Symbol | Supply | Value | Unit |
|---|---|---|---|---|
| 25°C | $I_{DD61}$ | $V_{DD1}$ | 0.25 | mA |
| | $I_{DD62H}$ | $V_{DD2H}$ | 0.45 | |
| | $I_{DD62L}$ | $V_{DD2L}$ | - (See note 4) | |
| | $I_{DD6Q}$ | $V_{DDQ}$ | - (See note 4) | |
| 85°C | $I_{DD61}$ | $V_{DD1}$ | 3.00 | |
| | $I_{DD62H}$ | $V_{DD2H}$ | 9.00 | |
| | $I_{DD62L}$ | $V_{DD2L}$ | 0.20 | |
| | $I_{DD6Q}$ | $V_{DDQ}$ | 0.60 | |

Notes: 1. $I_{DD6}$25°C is the typical value in the distribution with nominal $V_{DD}$ and a reference-only value. $I_{DD6}$85°C is the maximum $I_{DD}$ guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. $V_{DD1}$ = 1.70–1.95V; $V_{DD2H}$ = 1.01–1.12V; $V_{DD2L}$ = 0.87–0.97V; $V_{DDQ}$ = 0.47–0.57V; $T_C$ = –25°C to +85°C
4. $V_{DD2L}$and $V_{DDQ}$ power rails are not used during power-down self refresh

### Table 10: IT $I_{DD}$ Parameters – Single Die

| Symbol | Supply | x8 Mode Speed Grade | | x16 Mode Speed Grade | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | 7500 Mb/s | 8533 Mb/s | 7500 Mb/s | 8533 Mb/s | | |
| $I_{DD01}$ | $V_{DD1}$ | 3.3 | 3.3 | 3.3 | 3.3 | mA | |
| $I_{DD02H}$ | $V_{DD2H}$ | 29.5 | 29.5 | 30.0 | 30.0 | | |
| $I_{DD02L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD0Q}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2P1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2P2H}$ | $V_{DD2H}$ | 2.2 | 2.2 | 2.2 | 2.2 | | |
| $I_{DD2P2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2PQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2PS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2PS2H}$ | $V_{DD2H}$ | 2.2 | 2.2 | 2.2 | 2.2 | | |
| $I_{DD2PS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2PSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD2N1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2N2H}$ | $V_{DD2H}$ | 16.5 | 16.5 | 17.0 | 17.0 | | |
| $I_{DD2N2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2NQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |

**Table 10: IT $I_{DD}$ Parameters – Single Die**

| Symbol | Supply | x8 Mode Speed Grade | | x16 Mode Speed Grade | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | 7500 Mb/s | 8533 Mb/s | 7500 Mb/s | 8533 Mb/s | | |
| $I_{DD2NS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD2NS2H}$ | $V_{DD2H}$ | 16.5 | 16.5 | 17.0 | 17.0 | | |
| $I_{DD2NS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD2NSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3P1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD3P2H}$ | $V_{DD2H}$ | 6.0 | 6.0 | 6.0 | 6.0 | | |
| $I_{DD3P2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3PQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3PS1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | 1.5 | mA | |
| $I_{DD3PS2H}$ | $V_{DD2H}$ | 6.0 | 6.0 | 6.0 | 6.0 | | |
| $I_{DD3PS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3PSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3N1}$ | $V_{DD1}$ | 1.7 | 1.7 | 1.7 | 1.7 | mA | |
| $I_{DD3N2H}$ | $V_{DD2H}$ | 21.5 | 21.5 | 22.0 | 22.0 | | |
| $I_{DD3N2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3NQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD3NS1}$ | $V_{DD1}$ | 1.7 | 1.7 | 1.7 | 1.7 | mA | |
| $I_{DD3NS2H}$ | $V_{DD2H}$ | 21.5 | 21.5 | 22.0 | 22.0 | | |
| $I_{DD3NS2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD3NSQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD4R1}$ | $V_{DD1}$ | 9.0 | 10.0 | 11.0 | 12.0 | mA | 3, 4 |
| $I_{DD4R2H}$ | $V_{DD2H}$ | 290.0 | 320.0 | 430.0 | 480.0 | | |
| $I_{DD4R2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD4RQ}$ | $V_{DDQ}$ | 58.0 | 63.0 | 116.0 | 126.0 | | |
| $I_{DD4W1}$ | $V_{DD1}$ | 8.0 | 9.0 | 10.0 | 11.0 | mA | 3 |
| $I_{DD4W2H}$ | $V_{DD2H}$ | 205.0 | 225.0 | 285.0 | 315.0 | | |
| $I_{DD4W2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD4WQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD51}$ | $V_{DD1}$ | 17.0 | 17.0 | 17.0 | 17.0 | mA | |
| $I_{DD52H}$ | $V_{DD2H}$ | 115.0 | 115.0 | 115.0 | 115.0 | | |
| $I_{DD52L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5Q}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |

### Table 10: IT $I_{DD}$ Parameters – Single Die

| Symbol | Supply | x8 Mode Speed Grade | | x16 Mode Speed Grade | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | 7500 Mb/s | 8533 Mb/s | 7500 Mb/s | 8533 Mb/s | | |
| $I_{DD5AB1}$ | $V_{DD1}$ | 2.5 | 2.5 | 2.5 | 2.5 | mA | |
| $I_{DD5AB2H}$ | $V_{DD2H}$ | 23.5 | 23.5 | 24.0 | 24.0 | | |
| $I_{DD5AB2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5ABQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |
| $I_{DD5PB1}$ | $V_{DD1}$ | 2.5 | 2.5 | 2.5 | 2.5 | mA | |
| $I_{DD5PB2H}$ | $V_{DD2H}$ | 23.5 | 23.5 | 24.0 | 24.0 | | |
| $I_{DD5PB2L}$ | $V_{DD2L}$ | 0.2 | 0.2 | 0.2 | 0.2 | | |
| $I_{DD5PBQ}$ | $V_{DDQ}$ | 0.6 | 0.6 | 0.6 | 0.6 | | |

Notes: 1. Published $I_{DD}$ values except $I_{DD4RQ}$ are the maximum $I_{DD}$ values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. $I_{DD4RQ}$ value is reference only. Typical value. Output load = 5pF; $R_{ON}$ = 40 ohms; $T_C$ = 25°C
5. $V_{DD1}$ = 1.70–1.95V; $V_{DD2H}$ = 1.01–1.12V; $V_{DD2L}$ = 0.87–0.97V; $V_{DDQ}$ = 0.47–0.57V; $T_C$ = –40°C to +95°C
6. Notes 1 and 2 apply to entire table.

### Table 11: IT Full-Array Power-Down Self Refresh Current – Single Die

| Temperature | Symbol | Supply | Value | Unit |
|---|---|---|---|---|
| 25°C | $I_{DD61}$ | $V_{DD1}$ | 0.25 | mA |
| | $I_{DD62H}$ | $V_{DD2H}$ | 0.45 | |
| | $I_{DD62L}$ | $V_{DD2L}$ | - (See note 4) | |
| | $I_{DD6Q}$ | $V_{DDQ}$ | - (See note 4) | |
| 95°C | $I_{DD61}$ | $V_{DD1}$ | 3.70 | |
| | $I_{DD62H}$ | $V_{DD2H}$ | 12.00 | |
| | $I_{DD62L}$ | $V_{DD2L}$ | - (See note 4) | |
| | $I_{DD6Q}$ | $V_{DDQ}$ | - (See note 4) | |

Notes: 1. $I_{DD6}$25°C is the typical value in the distribution with nominal $V_{DD}$ and a reference-only value. $I_{DD6}$95°C is the maximum $I_{DD}$ guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. $V_{DD1}$ = 1.70–1.95V; $V_{DD2H}$ = 1.01–1.12V; $V_{DD2L}$ = 0.87–0.97V; $V_{DDQ}$ = 0.47–0.57V; $T_C$ = –40°C to +95°C
4. $V_{DD2L}$and $V_{DDQ}$ power rails are not used during power-down self refresh.

# Revision History

## Rev. D – 08/2022

- Corrected the package Z height on page#1
- Correct 3G32 Die Addressing in Table#3
- Clarify the 3G32 MPN on page#1
- Update VDDQ support on page#1
- General clarifications, namely on page#1
- Correct FBGA code in the Part Number Chart on page#2

## Rev. C – 04/2022

- Updated WT and IT IDD tables

## Rev. B – 12/2021

- Updated Mode Register table

## Rev. A – 10/2021

- Initial Preliminary release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006
208-368-4000, micron.com/support

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## Micron Technology:

MT62F1536M64D8CZ-023 AAT:C MT62F1536M64D8CZ-023 WT ES:C MT62F1536M64D8CZ-023 WT ES:C TR MT62F1536M64D8CZ-023 WT:C MT62F1536M64D8CZ-023 WT:C TR MT62F1536M64D8CZ-026 WT:C MT62F1536M64D8CZ-026 WT:C TR MT62F1536M64D8EK-023 WT ES:C MT62F1536M64D8EK-023 WT ES:C TR MT62F1536M64D8EK-023 WT:C MT62F1536M64D8EK-023 WT:C TR MT62F1536M64D8EK-026 WT:C MT62F1536M64D8EK-026 WT:C TR MT62F3G32D8DV-023 WT ES:C MT62F3G32D8DV-023 WT ES:C TR MT62F3G32D8DV-023 WT:C MT62F3G32D8DV-023 WT:C TR MT62F768M32D2DS-023 AIT:C MT62F768M32D2DS-023 AIT:C TR MT62F768M32D2DS-023 AUT:C MT62F768M32D2DS-023 AUT:C TR MT62F768M32D2DS-023 FAAT:C MT62F768M32D2DS-023 FAAT:C TR MT62F768M32D2DS-023 WT ES:C MT62F768M32D2DS-023 WT ES:C TR MT62F768M32D2DS-023 WT:C MT62F768M32D2DS-023 WT:C TR MT62F768M32D2DS-026 WT:C MT62F768M32D2DS-026 WT:C TR MT62F768M64D4CZ-023 WT ES:C TR MT62F768M64D4CZ-023 WT:C MT62F768M64D4CZ-023 WT:C TR MT62F768M64D4CZ-026 WT:C MT62F768M64D4CZ-026 WT:C TR MT62F768M64D4EK-023 AAT:C MT62F768M64D4EK-023 AAT:C TR MT62F768M64D4EK-023 AIT:C MT62F768M64D4EK-023 AIT:C TR MT62F768M64D4EK-023 AUT:C MT62F768M64D4EK-023 AUT:C TR MT62F768M64D4EK-023 FAAT:C MT62F768M64D4EK-023 FAAT:C TR MT62F768M64D4EK-023 WT ES:C MT62F768M64D4EK-023 WT ES:C TR MT62F768M64D4EK-023 WT:C MT62F768M64D4EK-023 WT:C TR MT62F768M64D4EK-026 WT:C MT62F768M64D4EK-026 WT:C TR