



The xRSB-80T05 Series are isolated DC/DC converters. These secondary side control units will provide up to 100 W of output power from a nominal 48 V input.

These converters are provided in an industry standard sixteenth brick package.





Key Features & Benefits

- 36 75 VDC Input
- 5 VDC @ 20 A Output
- 1/16th Brick Converter
- Isolated
- Fixed Frequency (500 kHz)
- High Efficiency
- High Power Density
- Low Cost
- Input Under-Voltage Lockout
- Start-up into Pre-biased Load
- Over Temperature Protection
- Remote On/Off
- Output Voltage Trim
- Positive/Negative Remote Sense
- Output Over-Voltage Protection with Auto-recovery
- Approved to IEC/EN 62368-1
- Approved to UL/CSA 62368-1
- Class II, Category 2, Isolated DC/DC Converter (refer to IPC-9592B)

Applications

- Networking
- Computers and Peripherals
- Telecommunications

Option

- Remote ON/OFF Logic
- Through hole and SMT



1. MODEL SELECTION

MODEL NUMBER	OUTPUT VOLTAGE	INPUT VOLTAGE	MAX. OUTPUT CURRENT	MAX. OUTPUT POWER	TYPICAL EFFICIENCY
0RSB-80T05LG					
0RSB-80T050G					
SRSB-80T05LG	5 VDC	36 - 75 VDC	20 A	100 W	92%
SRSB-80T050G	2 ADC	30 - 75 VDC	20 A	100 W	92%
SRSB-80T05LR					
SRSB-80T050R					

PART NUMBER EXPLANATION

x	R	SB	-	80	Т	05	х	у
Mounting Type	RoHS Status	Series Name		Output Power	Input Range	Output Voltage	Active Logic	Package Type
0 - Through Hole Mount	RoHS	1/16 th		100 W	36 – 75 V	5 V	L – Active Low	G - Tray Package
S - Surface Mount	nuno	Brick		100 00	30 - 75 V	5 V	0 – Active High	R - Tape and Reel Package

2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
Continuous non-operating Input V	oltage	-0.3	-	75	V
Input Transient Voltage	100 ms maximum	-	-	100	V
Remote On/Off		-0.3	-	18	V
I/O Isolation Voltage		-	-	1500	V
Ambient Temperature		-40	-	85	°C
Storage Temperature		-55	-	125	°C
Altitude		-	-	2000	m

NOTE: Ratings used beyond the maximum ratings may cause a reliability degradation of the converter or may permanently damage the device.



3. INPUT SPECIFICATIONS

All specifications are typical at 25°C unless otherwise stated.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Operating Input Voltage		36	48	75	V
Input Current (full load)		-	-	2	Α
Input Current (no load)		-	40	70	mA
Remote Off Input Current		-	2	5	mA
Input Reflected Ripple Current (rms) Input Reflected Ripple Current (pk-pk)	With simulated source impedance of 10 μ H, 5 Hz to 20 MHz. Use a 150 μ F, ESR< 0.1 Ω @ 100 kHz, 20°C Al-electrolytic capacitor and 3*2.2 μ F/100 V ceramic capacitor with ESR < 0.01 Ω @ 100 kHz, 20°C.	-	6 20	12 30	mA mA
I ² t Inrush Current Transient		-	-	1	A^2s
Turn-on Voltage Threshold		32.5	34	35.5	V
Turn-off Voltage Threshold		31	32	34	V
Input UV Lockout Hysteresis		1.5	2	2.5	V

CAUTION: This converter is not internally fused. An input line fuse must be used in application. Recommend a fast-acting fuse with maximum rating of 5 A on system board. Refer to the fuse manufacture's datasheet for further information.



4. OUTPUT SPECIFICATIONS

All specifications are typical at nominal input, full load at 25°C unless otherwise stated.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Output Voltage Set Point	Vin = 48 V, $Io = 0\%$ load at 25°C ambient.	4.925	5.000	5.075	V
Load Regulation	Io = 0 A to full load	-	±8	±15	mV
Line Regulation	Vin =36 to 75 V	-	±8	±15	mV
Regulation Over Temperature	Ambient temperature = -40°C to 85°C	-	±30	±50	mV
Total Output Voltage Range	Over sample load, line and temperature	4.85	-	5.15	V
Ripple and Noise (pk-pk)	Vin = 48 V,0-20 MHz BW, with 500 μ F	-	35	70	mV
Ripple and Noise (rms)	ceramic capacitor and 2200 µF Al-electrolytic capacitor at output.	-	3	10	mV
Output Current Range		0	-	20	А
Output DC Current Limit		24	27	32	А
Short Circuit Surge Transient		-	-	3	A^2s
Rise Time		3	5	8	ms
	From Vin to 90% of Vout.	-	15	30	ms
Turn on Time	From on/off to 90% of Vout.	-	30	50	ms
Overshoot at Turn on		-	0	1	%
Output Capacitance	100 µF Tan capacitor for minimal capacitor. Typically 50% ceramic+50% electrolytic capacitors for maximum capacitor.	100	-	5000	μF
Transient Response					
\triangle V 50%~75% of Max Load		-	130	180	mV
Settling Time	di/dt = 1 A/ μ s, Vin = 48 VDC, Ta = 25°C, with 500 μ F ceramic capacitor and 2200 μ F	-	100	200	μs
△V 75%~50% of Max Load	Al-electrolytic capacitor at output.	-	130	180	mV
Settling Time	•	-	100	200	μs



5. GENERAL SPECIFICATIONS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT	
Efficiency	The efficiency is measured at Vin = 48 V, full load and Ta = 25°C.	90	92	-	%	
Switching Frequency		-	500	-	kHz	
FIT	Calculated Per Telcordia SR-332	-	146	-	-	
MTBF	(Vin=48 V, Vo=4.8 V, Io=16 A, Ta = 25°C, FIT= 10 ⁹ /MTBF	-	6.8	-	Mhrs	
Over Temperature Protection		-	125	-	°C	
Over Voltage Protection (Static)	This voltage is achieved by trimming up output slowly.	5.8	6.2	6.4	V	
Weight		-	15.5	-	g	
	Through Hala Marint	1.0	inch			
Dimensions (L., M., LI)	Through Hole Mount	33.0	mm			
Dimensions (L × W × H)	Surface Mount	1.3	inch			
	Surface Mount	33.0	33.02 x 22.86 x 10.72			
Isolation Characteristics						
Input to Output		-	-	1500	VDC	
Isolation Resistance		10M	-	-	Ohm	
Isolation Capacitance		-	1000	-	pF	

6. EFFICIENCY DATA

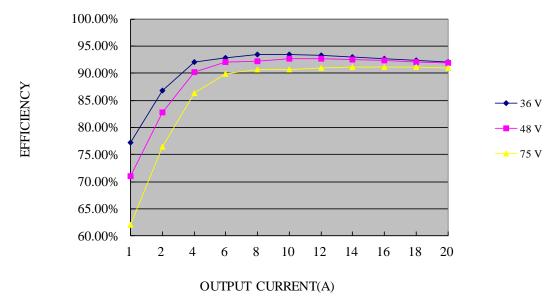


Figure 1. Efficiency data



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7. REMOTE ON/OFF

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
Signal Low (Unit On)	Active Low	Devents On 10ff a in in a good the good like in aff	-0.3	-	0.8	V
Signal High (Unit Off)	Active Low	Remote On/Off pin is open, the module is off.	2.4	-	18	V
Signal Low (Unit Off)	Active Lligh	Demonts On (Officialis and on the granded in an	-0.3	-	0.8	V
Signal High (Unit On)	Active High	Remote On/Off pin is open, the module is on.	2.4	-	18	V
Current Sink			0	-	1	mA

Recommended remote on/off circuit for active low

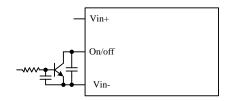


Figure 2. Control with open collector/drain circuit

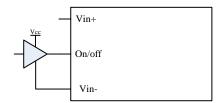


Figure 4. Control with logic circuit

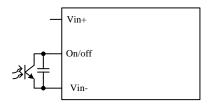


Figure 3. Control with photocoupler circuit

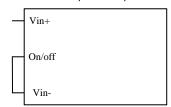


Figure 5. Permanently on

Recommended remote on/off circuit for active high

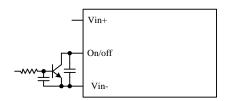


Figure 6. Control with open collector/drain circuit

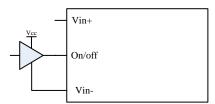


Figure 8. Control with logic circuit

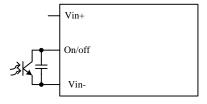


Figure 7. Control with photocoupler circuit

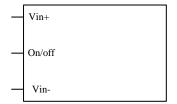


Figure 9. Permanently on



8. REMOTE SENSE

This module has remote sense compensation feature which can minimize the effects of resistance between output and load in system layout and facilitate accurate voltage regulation at load terminals or other selected point.

- 1. The remote sense lines carry very little current and hence do not require a large cross-sectional area.
- 2. This module compensates for a maximum drop of 10% of the nominal output voltage.
- 3. If the unit is already trimmed up, the available remote sense compensation range should be correspondingly reduced. The total voltage increased by trim and remote sense should not exceed 10% of the nominal output voltage.
- 4. When using remote sense compensation, all the resistance, parasitic inductance and capacitance of the system are incorporated within the feedback loop of this module which can make an effect on the module's compensation, affecting the stability and dynamic response. A 0.1µF ceramic capacitor can be connected at the point of load to de-couple noise on the sense wires.
- 5. Recommend the connection of remote sense compensation as below figure. There are a resistor RS+ (100 ohm) from Vo+ to Sense+ and a resistor RS- (11.3 ohm)) from Vo- to Sense- inside of this module.

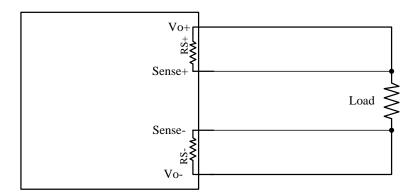


Figure 10.

6. If not using remote sense compensation, please connect sense directly to output at module's pin, that is, connect sense+ to Vo+ and sense- to Vo- at module's pin, the shorter the better. see below figure.

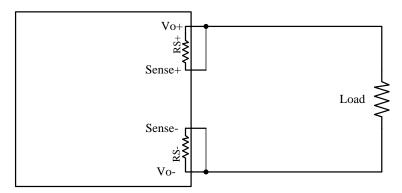


Figure 11.



9. THERMAL DERATING CURVE

Maximum junction temperature of semiconductors derated to 120 °C.

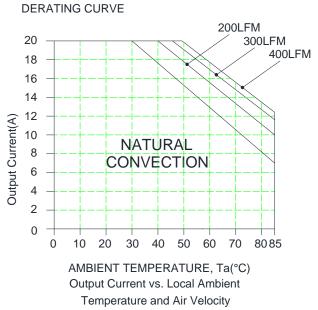


Figure 12. Derating curve under normal input

10. RIPPLE AND NOISE

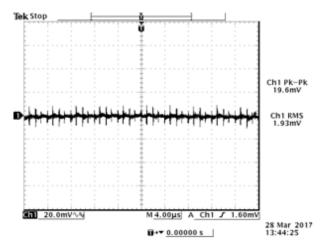


Figure 13. Ripple and noise waveform
Ripple and noise at full load, 48 VDC input, 5 VDC / 20 A output and Ta = 25 °C, and with 500 μ F ceramic capacitor and 2200 μ F Al-electrolytic capacitor at output.



11. OUTPUT TRIM EQUATIONS

Equations for calculating the trim resistor are shown below. The Trim Down resistor should be connected between the Trim pin and Sense (-) pin. The Trim Up resistor should be connected between the Trim pin and the Sense (+). Only one of the resistors should be used for any given application.

Minimum trim down voltage is 4.5 V.

Maximum trim up voltage is 5.5 V.

The total voltage increased by trim and remote sense should not exceed 10% of the nominal output voltage.

Trim down test circuit

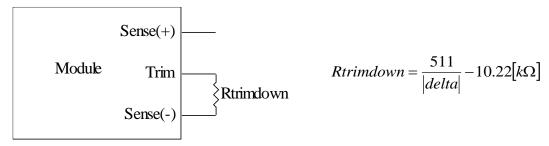


Figure 14. Trim down test circuit

Trim up test circuit

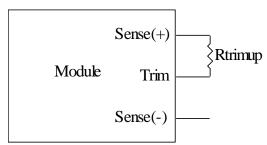


Figure 15. Trim up test circuit

$$Rtrimup = \frac{(100 + delta) \cdot Vo \cdot 5.11 - 626}{1.225 \cdot delta} - 10.22 \big[k\Omega \big]$$

NOTE: Vo_req = Desired (trimmed) output voltage [V] Output voltage Vo = 5.0 V



12. UNDER VOLTAGE LOCKOUT

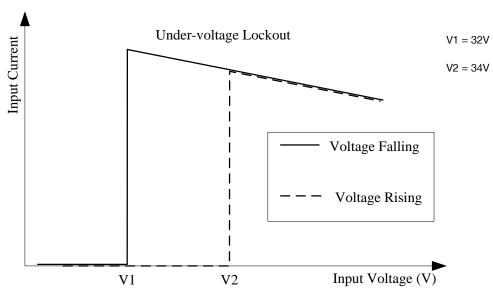


Figure 16. Under voltage lockout

13. INPUT NOISE

Input reflected ripple current Testing setup

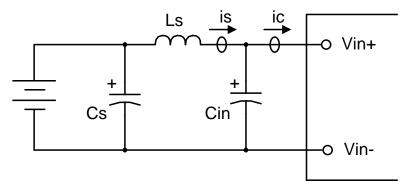


Figure 17.

Notes and values in testing.

is: Input Reflected Ripple Current

ic: Input Terminal Ripple Current

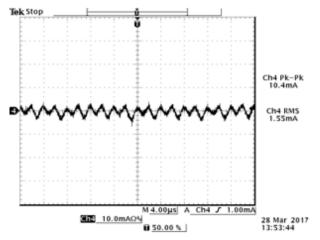
Ls: Simulated Source Impedance (10 $\,\mu H$)

Cs: Offset possible source Impedance (none)



Cin: Electrolytic capacitor, should be as close as possible to the power module to damp ic ripple current and enhance stability. Recommendation: 150 μ F, ESR < 0.1 Ω @ 100 kHz, 20 °C Al-electrolytic capacitor and 3*2.2 μ F/100 V ceramic capacitor with ESR < 0.01 Ω @ 100 kHz, 20 °C.

Below measured waveforms are based on above simulated and recommended inductance and capacitance.



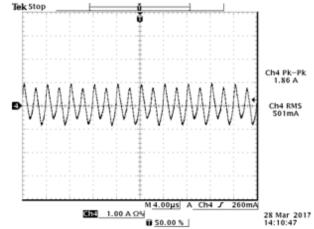


Figure 18. is (input reflected ripple current), AC component

Figure 19. ic (input terminal ripple current), AC component

Test condition: 48 VDC input, 5 VDC / 20 A output and Ta = 25 $^{\circ}$ C, with 500 μ F ceramic capacitor and 2200 μ F Al-electrolytic capacitor at output.

14. TRANSIENT RESPONSE WAVEFORMS

Transient Response: di/dt=1 A/µs

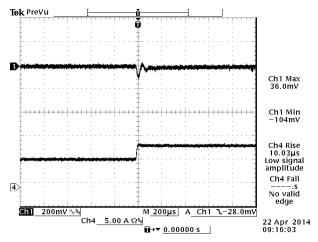


Figure 20. Vout = 5 V, 50%-75% Load Transients at Vin = 48 V @ Ta = 25 °C, with 500 μF ceramic capacitor and 2200 μF Al-electrolytic capacitor at output.

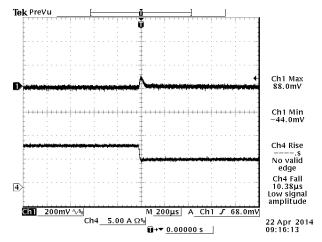


Figure 21. Vout = 5 V, 75%-50% Load Transients at Vin = 48 V @ Ta = 25 °C, with 500 μF ceramic capacitor and 2200 μF Al-electrolytic capacitor at output



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15. STARTUP & SHUTDOWN

RISE TIME

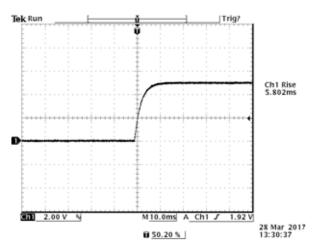


Figure 22. Test Condition: 48 Vin, 5 V, 20 A output, Cout = 500 μF ceramic + 2200 μF electrolytic

STARTUP TIME

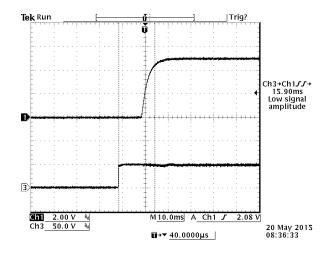


Figure 23. Startup from Vin
Ch1: Vo
Ch2: Vin
Test Condition: Vin = 48 V, Vo = 5 V, 20 A output
Cout = 500 μF ceramic + 2200 μF electrolytic

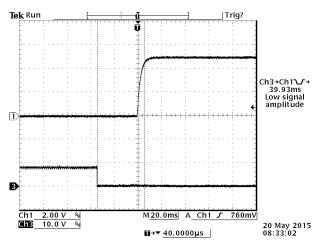
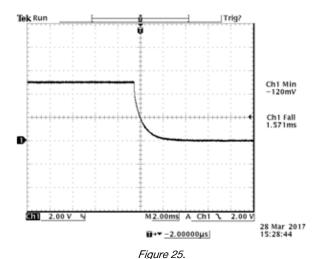


Figure 24. Startup from on/off
Ch1: Vo
Ch2: on/off
Test Condition: Vin =48 V, Vo = 5 V, 20 A output
Cout = 500 µF ceramic + 2200 µF electrolytic



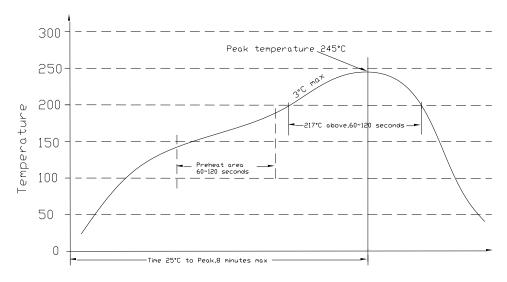
SHUTDOWN



Test Condition: 48 Vin, 5 V, 20 A output, Cout = 500μ F ceramic + 2200μ F electrolytic

16. SOLDERING INFORMATION

The SRSB-80T05x modules are designed to be compatible with a Paste-In-Hole assembly process. The suggested Pb-free solder paste is Sn/Ag/Cu(SAC). The recommended reflow profile using Sn/Ag/Cu solder is shown in the following. Recommended reflow peak temperature is 245°C while the part can withstand peak temperature of 260°C maximum for 10seconds. This profile should be used only as a guideline. Many other factors influence the success of SMT reflow soldering. Since your production environment may differ, please thoroughly review these guidelines with your process engineers.



Reflow Time (Seconds)



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Figure 26. Soldering temperature

17. MSL RATING

The SRSB-80T05x modules have a MSL rating of 3.

18. STORAGE AND HANDLING

The SRSB-80T05x modules are designed to be compatible with J-STD-033 Rev:A (Handling, Packing, Shipping and Use of Moisture /Reflow Sensitive surface Mount devices). Moisture barrier bags (MBB) with desiccant are applied. The recommended storage environment and handling procedure is detailed in J-STD-033.

19. PRE-BAKING

This component has been designed, handled, and packaged ready for pb-free reflow soldering. If the assembly shop follows J-STD-033 guidelines, no pre-bake of this component is required before being reflowed to a PCB. However, if the J-STD-033 guidelines are not followed by the assembler, Bel recommends that the modules should be pre-baked @ 120~125°C for a minimum of 4 hours (preferably 24 hours) before reflow soldering.



20. MECHANICAL DIMENSIONS 0RSB-80T05x OUTLINE

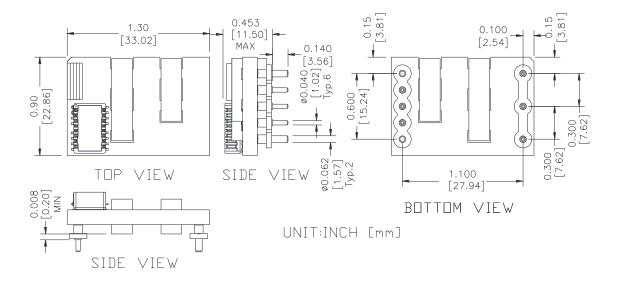


Figure 27. 0RSB-80T05x outline

NOTE: These parts are not however compatible with the higher temperatures associated with lead free solder processes and must be soldered using a reflow profile with a peak temperature of no more than 260 °C.

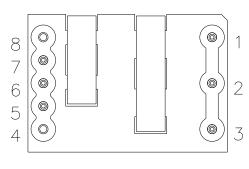
NOTES:

- 1) All Pins: Material Copper Alloy;
 - Finish 3 micro inches minimum Gold over 50 micro inches minimum Nickel plate.
- 2) Un-dimensioned components are shown for visual reference only.
- 3) All dimensions in inch [mm]; Tolerances: x.xx +/-0.02 inch [0.51 mm].

x.xxx +/-0.010 inch [0.25 mm]. Unless otherwise stated



ORSB-80T05x PIN DEFINITIONS



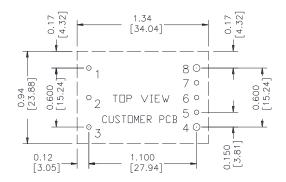
BOTTOM VIEW

Figure 28. ORSB-80T05x pins

PIN	FUNCTION	PIN	FUNCTION
1	Vin (+)	5	Sense (-)
2	Remote On/Off	6	Trim
3	Vin (-)	7	Sense (+)
4	Vout (-)	8	Vout (+)

ORSB-80T05x RECOMMENDED PAD LAYOUT

RECOMMENDED PCB PAD LAYOUT



HOLE SIZE: 1-3, 5-7 Ø0.047[1.19], 4,8 Ø0.07 [1.78] PAD SIZE: 1-3, 5-7 Ø0.08[2.03] 4,8 Ø0.10 [2.54]

Figure 29. 0RSB-80T05x Recommended pad layout



SRSB-80T05x OUTLINE

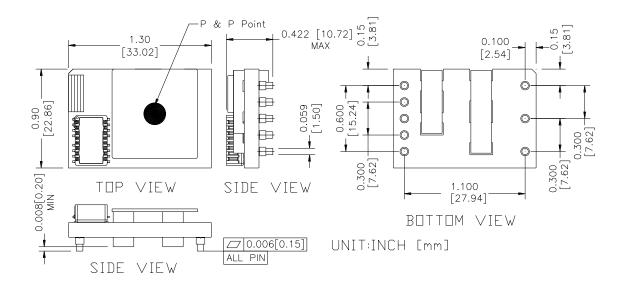


Figure 30. SRSB-80T05x outline

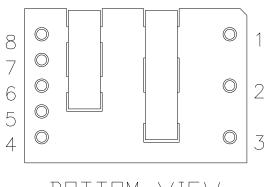
NOTES:

- 1) All Pins: Material Copper Alloy;
 - Finish 3 micro inches minimum Gold over 50 micro inches minimum Nickel plate.
- 2) Un-dimensioned components are shown for visual reference only.
- 3) All dimensions in inch [mm]; Tolerances: x.xx +/-0.02 inch [0.51 mm].

x.xxx +/-0.010 inch [0.25 mm]. Unless otherwise stated



SRSB-80T05x PIN DEFINITIONS



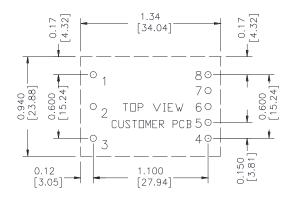
BOTTOM VIEW

Figure 31. SRSB-80T05x pin

PIN	FUNCTION	PIN	FUNCTION
1	Vin (+)	5	Sense (-)
2	Remote On/Off	6	Trim
3	Vin (-)	7	Sense(+)
4	Vout (-)	8	Vout (+)

SRSB-80T05x RECOMMENDED PAD LAYOUT

RECOMMENDED PCB PAD LAYOUT



PAD SIZE: 1-8 Ø0.08[2.03]

Figure 32. SRSB-80T05x Recommended pad layout



21. PACKAGING INFORMATION

SRSB-80T05LR / SRSB-80T050R

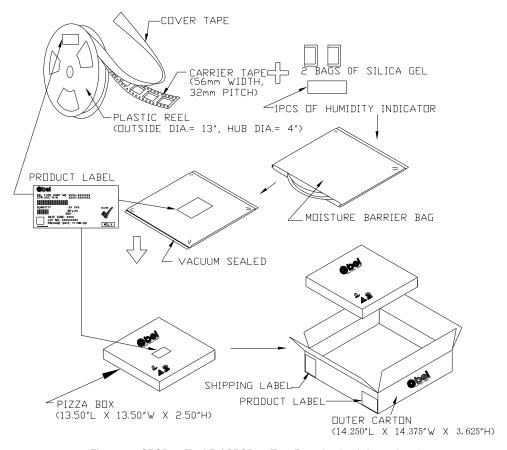
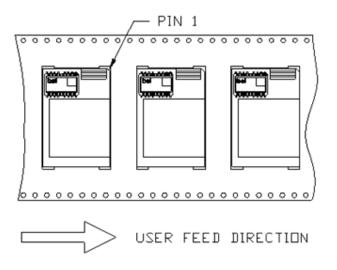


Figure 33. SRSB-80T05LR / SRSB-80T050R packaging information-1





DRIENTATION OF COMPONENT INSIDE POCKET

TAPE WIDTH	56mm
POCKET PITCH	32mm
QUANTITY OF COMPONENTS PER REEL	160
PLASTIC REEL DUTER DIAMETER	13 INCHES
PLASTIC REEL HUB DIAMETER	4 INCHES
CDMPLY WITH EIA 481-2-A	

Figure 34. SRSB-80T05LR / SRSB-80T050R packaging information-2



0RSB-80T05xG / SRSB-80T05xG

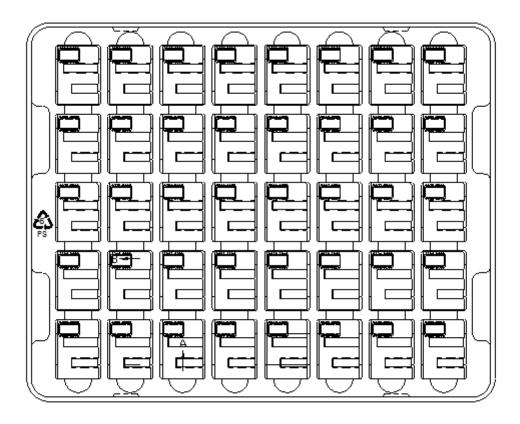


Figure 35. 0RSB-80T05xG / SRSB-80T05xG packaging information

22. REVISION HISTORY

DATE	REVISION	CHANGES DETAIL	APPROVAL
2017-06-29	AA	First release	J.Yan
2017-08-30	AB	Update soldering information	J.Yan
2018-7-23	AC	Update mechanical dimensions and change max output current to 20A	J.Yao
2019-07-16	AD	Update output capacitance	XF.Jiang
2019-08-06	AE	Update derating curve	XF.Jiang
2021-05-28	AF	Add object ID. Update safety certificate. Update SRSB-80T05x mechanical outline for changing the height.	XF.Jiang

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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