Bel Power Solutions point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The DM73XX is a fully programmable digital power manager that utilizes the industry-standard I²C communication bus interface to control, manage, program and monitor up to 32 dP-series POL converters and 4 independent power devices. The DM73XX completely eliminates the need for external components for power management and programming and monitoring of the d-pwer™ POL converters and other industry standard power and peripheral devices.

Parameters of the DM73XX are programmable via the I²C bus and can be changed by a user at any time during product development and deployment.

Key Features & Benefits

- RoHS compliant for all six substances
- Compatible with both lead-free and standard reflow processes
- Programs, controls, and manages up to 32 independent dPOL converters via an industry standard I²C interface (both 100 kHz and 400 kHz)
- JTAG IEEE 1149.1 compliant programming interface
- Controls and monitors industry standard power supplies and other peripheral devices (fans, etc)
- Programs output voltage, protections, optimal voltage positioning, turn-on and turn-off delays and slew rates, switching frequency, interleave (phase shift), and feedback loop compensation of the d-pwer™ POL converters
- User friendly GUI interface for programming, monitoring, and performance simulation
- Four independent OK lines for flexible fault management and fast fault propagation
- Four interrupt inputs with programmable hot swap support capabilities
- Intermediate bus voltage monitoring and protection
- AC Fail input
- Non-volatile system configuration data memory
- 1K Byte of user accessible non-volatile memory
- Control of industry standard DC-DC front ends
- Crowbar output to trigger the optional crowbar protection
- Run-time counter
- Small footprint semiconductor industry standard QFN64 package: 9x9 mm
- Wide industrial operating temperature range

Asia-Pacific	Europe, Middle East	North America
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DM73XX Series

1. MODEL SELECTION

DPM TYPE	NUMBER OF D-PWER™ POLS AND AUXILIARY DEVICES THAT CAN BE CONTROLLED	ACTIVE ADDRESSES	NUMBER OF GROUPS	NUMBER OF INTERRUPTS	NUMBER OF PARALLEL BUSES	NUMBER OF AUXILIARY DEVICES
DM7304G	4	00…03	2	2	2	4
DM7308G	8	00…07	2	2	4	4
DM7316G	16	00…15	3	3	4	4
DM7332G	32	00…31	4	4	8	4

2. STANDARD 5-DIGIT IDENTIFIERS

DPM TYPE	DPM PRELOADED WITH DEFAULT CONFIGURATION FILE	DPM CONFIGURED FOR JTAG PROGRAMMING	PACKAGING OPTIONS
DM7304G	65511	65515	B1, R100
DM7308G	65512	65516	B1, R100
DM7316G	65513	65517	B1, R100
DM7332G	65514	65518	B1, R100

3. ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed may cause permanent damage to the DPM. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the DPM at absolute maximum ratings or conditions beyond those indicated in the operational sections of this specification is not implied.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Ambient Temperature Range		-40	85	°C
Storage Temperature (Ts)		-55	150	°C
Junction Temperature (T_J)			125	°C
Input Voltage	VDD pin	-0.3	3.6	VDC
Input Voltage	Any pin other than VDD	-0.5	VDD+0.5	VDC
Pin Current	DC		40	mA

4. MECHANICAL SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Peak Reflow Temperature	40 sec maximum duration			260	°C
Lead Plating			100% matte tin		
Moisture Sensitivity Level	JEDEC J-STD-020C		3		

5. RELIABILITY SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Failure Rate	Demonstrated at 55°C, 60% Confidence Level	2.26			FIT
Non-Volatile Memory Endurance	-40°C to 85°C ambient	10000			Read-Write cycles

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6. ELECTRICAL SPECIFICATIONS

Specifications apply at VDD from 3 V to 3.6 V, ambient temperature from -40°C to 85°C, and utilizing proper decoupling as shown in Figure 3 unless otherwise noted.

6.1 POWER SPECIFICATIONS

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNITS
Input Supply Voltage	VDD pin	3.0		3.6	VDC
Undervoltage Lockout	Hardware reset is triggered below this threshold	2.3	2.5	2.7	VDC
Input Supply Current	VDD pin = 3.3 V		12	20	mA
VREF voltage	AREF pin	2.3	2.56	2.7	VDC
IBVS input voltage range		GND		VREF	VDC
IBVS input resistance			100		MΩ

6.2 FEATURE SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
Intermediate Voltage Bus Protections					
Overvoltage Protection Threshold	With external 5.7:1 ratio divider	IBV		14.6	V
Undervoltage Protection Threshold	With external 5.7:1 ratio divider	0		IBV	V
Threshold Hysteresis	With external 5.7; 1ratio divider. Symmetrical relative to average threshold value		±114		mV
Accuracy of Protection Thresholds	Internal voltage reference, 1% resistive divider	-10		10	%V_{TH}
Internal ADC Conversion Error	With external 5.7:1 ratio divider	-43		43	mV
Front End Enable (FE_EN)					
V_{FE_EN}	Front End logic level enabled		High		
V_{FE_EN}	Front End logic level disabled		Low		
Isrc	Source Current, V_{FE_EN} = V_{DD}-0.5 V	5			mA
Isink	Sink Current, V_{FE_EN} = 0.5V	5			mA
Crowbar (CB)					
V_{CB}	Crowbar Enable		High		
V_{CB}	Crowbar Disable		Low		
Isrc	Source Current, V_{CB} = V_{DD}-0.5 V	5			mA
Isink	Sink Current, V_{CB} = 0.5 V	5			mA
T_{CB}	Duration of Enabling Pulse		1		ms

6.3 SIGNAL SPECIFICATIONS

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNITS
SYNC/DATA Line					
SDpu	SD pull up resistor		5		kΩ
SDthrL	SD input low voltage threshold	0.31·VDD		0.52·VDD	V
SDthrH	SD input high voltage threshold	0.45·VDD		0.81·VDD	V
SDhys	SD input hysteresis	0.37		1.1	V
SDsink	SD sink capability (V_{SD} = 0.5 V)			30	mA
Freq_sd	Clock frequency	450		550	kHz
Tsynq	Sync pulse duration	22		28	% of clock cycle
T0	Data = 0 pulse duration	72		78	% of clock cycle
Interrupt Inputs (INT_N[3:0])					
Rpu3	Pull up resistor		30		kΩ
VthrL3	Input low voltage threshold	0.31·VDD		0.52·VDD	V
VthrH3	Input high voltage threshold	0.45·VDD		0.81·VDD	V
Vhys3	Input hysteresis	0.37		1.1	V
ADDR[3:0], ACFAIL_N, RES_N, LCK_N, PG[3:0] Inputs					
Rpu1	Pull up resistor	20		50	kΩ
VthrL1	Input low voltage	-0.5		0.2·VDD	V
VthrH1	Input high voltage	0.7·VDD		VDD+0.5	V
HRES_N Input					
Rpu2	HRES_N pull up resistor (with series diode, see note[1])	30		60	kΩ
VthrL2	HRES_N input low voltage	-0.5		0.2·VDD	V
VthrH2	HRES_N input high voltage	0.9·VDD		VDD+0.5	V
Inputs/Outputs (OK_A, OK_B, OK_C, OK_D)					
OKpu	OK pull up resistor		5		kΩ
OKthrL	OK input low voltage threshold	0.31·VDD		0.52·VDD	V
OKthrH	OK input high voltage threshold	0.45·VDD		0.81·VDD	V
OKhys	OK input hysteresis	0.37		1.1	V
OKsink	OK sink capability (V_{OK} = 0.5 V)			30	mA
Enable Outputs (EN[3:0])					
V_{EN}	EN logic level enabled		High		
V_{EN}	EN logic level disabled		Low		
$V_{EN}H$	EN output high voltage (I_{OH} = -10 mA)	VDD-0.6			V
$V_{EN}L$	EN output low voltage (I_{OL} = 5 mA)			0.5	V

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[1] HRES_N Input - Because the input does not have an internal ESD protection diode connected to VDD, the user needs to add an external diode between the HRES_N and VDD pins as shown in Figure .

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6.4 I²C INTERFACE

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
ViL	Input low voltage	-0.5		0.3·VDD	V
ViH	Input high voltage	0.7·VDD		VDD+0.5	V
Vhys	Input hysteresis	0.05·VDD			V
VoL	Output low voltage, I_{SINK}=3mA	0		0.4	V
t_r	Rise time for SDA and SCL	$20+0.1C_b^2$		300	ns
t_{of}	Output fall time from ViHmin to ViLmax	$20+0.1C_b^2$		250	ns
Ii	Input current each I/O pin, $0.1V_{DD} < V_i < 0.9 V_{DD}$	-10		10	µA
Ci	Capacitance for each I/O pin			10	pF
f_{SCL}	SCL clock frequency	0		400	kHz
Standard-Mode I²C (f_{SCL} ≤ 100kHz)					
R_{PU}	External pull-up resistor	1		$1000/C_b^2$	kΩ
t_{HDSTA}	Hold time (repeated) START condition	4.0			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HIGH}	High period of the SCL clock	4.0			µs
t_{SUSTA}	Setup time for a repeated START condition	4.7			µs
t_{HDDAT}	Data hold time	0		3.45	µs
t_{SUDAT}	Data setup time	250			ns
t_{SUSTD}	Setup time for STOP condition	4.0			µs
t_{SUF}	Bus free time between a STOP and START condition	4.7			µs
Fast-Mode I²C (100kHz < f_{SCL} ≤ 400kHz)					
R_{PU}	External pull-up resistor	1		$300/C_b^2$	kΩ
t_{HDSTA}	Hold time (repeated) START condition	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
t_{SUSTA}	Setup time for a repeated START condition	0.6			µs
t_{HDDAT}	Data hold time	0		0.9	µs
t_{SUDAT}	Data setup time	100			ns
t_{SUSTD}	Setup time for STOP condition	0.6			µs
t_{SUF}	Bus free time between a STOP and START condition	1.3			µs

[2] C_b – bus capacitance in pF, typically from 10 pF to 400 pF
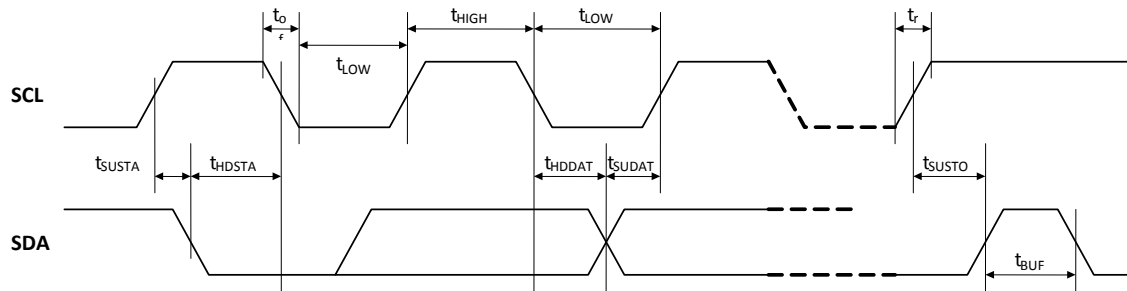
DM73XX Series

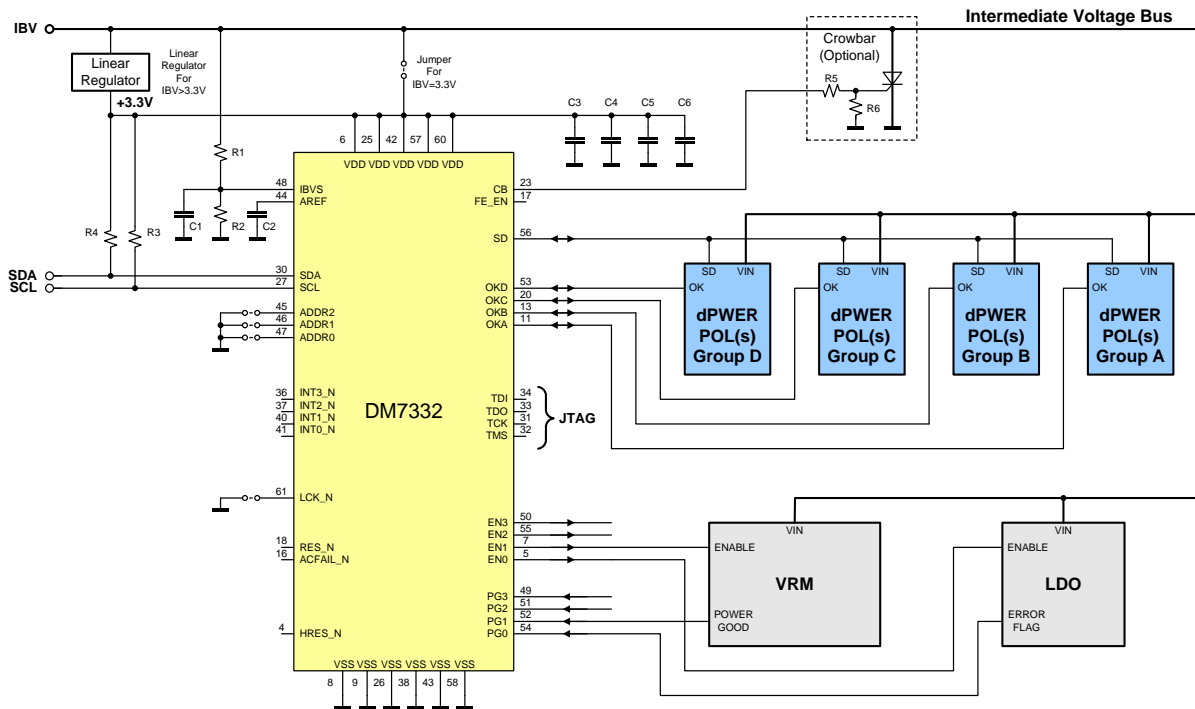Figure 1. I²C Timing Parameters

7. TYPICAL APPLICATION

Figure 2. Typical Application Schematic of Multiple Output System with Digital Power Manager and I²C Interface

The schematic of a typical application of a DM73XX digital power manager (DPM) is shown in Figure 3. The system includes four groups of d-pwer Point Of Load converters (POLs). A group is defined as one or more POL converters interconnected via OK pins. Grouping of the POLs enables users to program advanced fault management schemes and define margining functions, monitoring, start-up behavior, and reporting conventions.

All d-pwer POL converters are connected to the DPM and to each other via a single-wire synchronization/data (SD) line. The line provides synchronization of all POL converters to the master clock generated by the DPM and simultaneously carries bidirectional data transfer between POL converters and the DPM. The DPM communicates via the I²C bus with the host system and/or the Graphical User Interface.

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In this application, besides POL converters, the DPM also controls and monitors two auxiliary devices – a Voltage Regulation Module (VRM) and a Low Dropout Regulator (LDO). While these devices are not d-pwer compliant and may not even be manufactured by Bel Power Solutions, they are integrated into the system by communicating with the DPM via their Enable pins connected to ENX outputs of the DPM. In addition, the DPM monitors status of the auxiliary devices via its PGX inputs connected to Power Good and Error Flag outputs of the auxiliary devices. The DPM can control and monitor four or more independent auxiliary devices.

The DPM can also trigger an optional crowbar circuit and provide undervoltage and overvoltage protections of the intermediate bus voltage. In addition, the DPM can be controlled by a host system via the interrupt inputs, RES_N and the ACFAIL_N inputs.

8. DESCRIPTION

The DM73XX series DPMs perform translation between the I²C interface connected to a host system or the Graphical User Interface and the SD communication bus connected to dPOL converters. In addition, DPMs carry out programming, monitoring, data storage, POL group management, hot-swap control, protection, and control and monitoring of auxiliary devices.

The DPMs can be controlled via the GUI or directly via the I²C bus by using specific commands described in the "DPM Programming Manual".

8.1 DPM MEMORY

The DPM memory consists of RAM and non-volatile memory (Flash). The RAM is used for programming operations and manipulation of the various blocks of configuration, setup, status, and monitoring registers. Non-volatile memory is used to store programming and configuration data. Flash memory holds DPM set-up registers, POL set-up registers, monitoring data, and user memory data. Setup registers for the DPM and the POL converters are protected by CRCs that are checked during programming of POL converters and at the power-up of the DPM.

The LCK_N pin and the write protection register WP limit the write access to the memory blocks in the DPM and POL converters. The WP register content is defaulted to write protect upon powering up the DPM.

8.1.1 WRITE PROTECTION

There are hardware-based and software-based memory write protections. The hardware protection takes precedence over the software protection.

8.1.1.1 HARDWARE PROTECTION

The LCK_N pin enables the hardware memory write protection. If the pin is pulled low, the hardware lock is active and the memory blocks are then read-only. I²C write commands to the DPM return an error code (0x00). The write commands to the POL converters bypassing the DPM are also disabled. If the pin is left floating, the hardware lock is disabled and the software write protection is active.

8.1.1.2 SOFTWARE PROTECTION

Software write protection allows users to protect the various memory blocks from being overwritten through the I²C bus. At the power-up the WP register is defaulted to write protect.

Software write protection can be disabled by checking appropriate boxes in the Write Protection subsection of the DPM/Program/Advanced dialog shown in Figure 4 or via the I²C bus by writing directly into the register. Write protections are automatically restored when the DPM's input power is recycled.
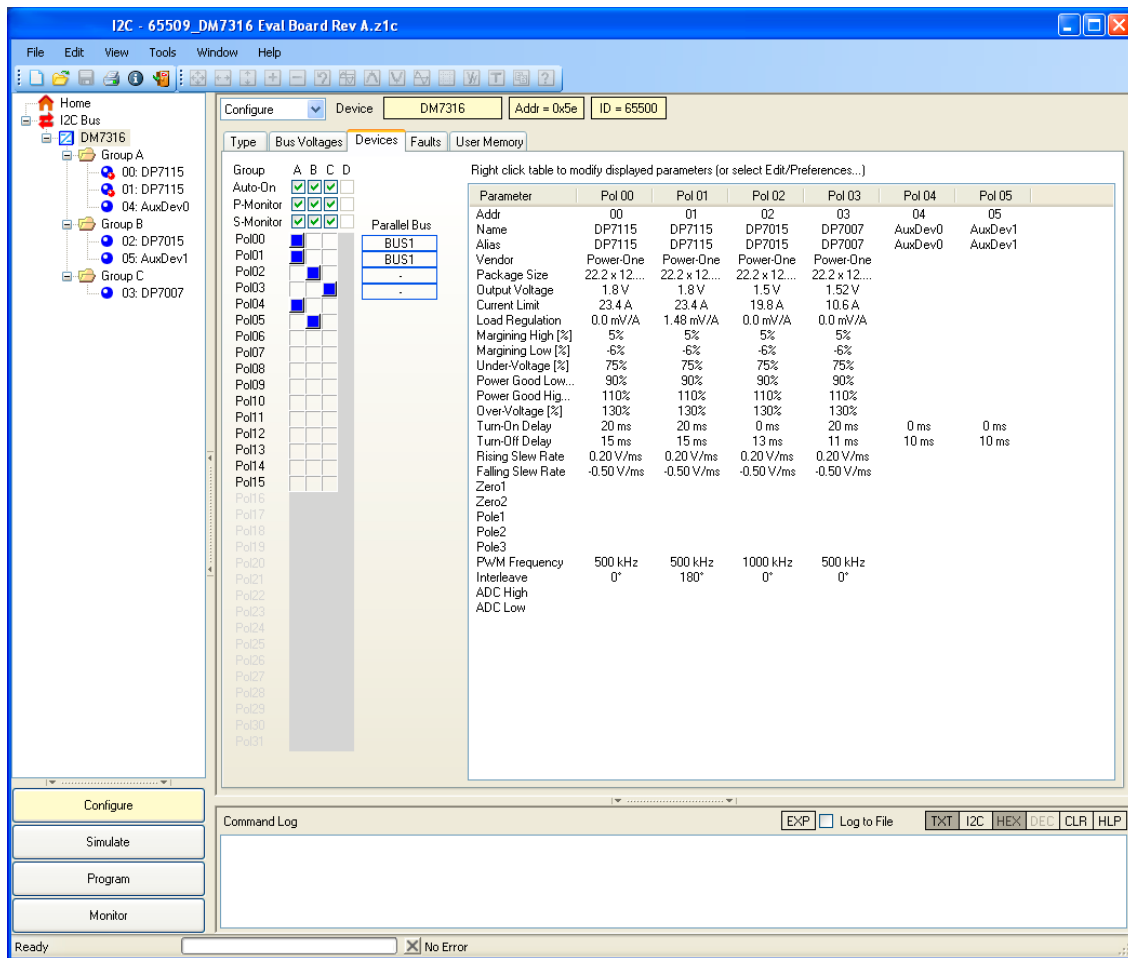
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Figure 3. GUI DPM Advanced Programming Dialog

8.1.2   DPM REGISTERS

The DPM setup registers occupy 70 bytes and contain all necessary information to set up the DPM functionality, define POL converters and Auxiliary Devices, group membership and behavior, margining, interrupt configurations, etc. they DPM registers are listed in. The table relates to the DPM model number DM7332 capable of supporting up to 32 POL converters. For other DPM models some of the registers and/or bits in the registers are not activated depending on the number of supported POLs/Groups/Interrupts/Parallel Buses for the specific DPM. Writing into an unsupported register or bit will have no effect, reading from an unsupported register or bit will return an error code (0x00).

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ADDRESS OFFSET[3]	REGISTER NAME	CONTENT	REGISTER TYPE	USER ACCESS	WRITE PROTECT	INITIAL VALUE
0x00	GD1[3:0]	Group Definition Register 1	Static	R/W	yes	0x00000000
0x04	GD2[3:0]	Group Definition Register 2	Static	R/W	yes	0x00000000
0x08	GAC	Group A Configuration	Static	R/W	yes	0x00
0x09	GBC	Group B Configuration	Static	R/W	yes	0x00
0x0A	GCC	Group C Configuration	Static	R/W	yes	0x00
0x0B	GDC	Group D Configuration	Static	R/W	yes	0x00
0x0C	FPC1	Fault Propagation Configuration 1	Static	R/W	yes	0x00
0x0D	FPC2	Fault Propagation Configuration 2	Static	R/W	yes	0x00
0x0E	EPC	Error Propagation Configuration	Static	R/W	yes	0x00
0x0F	IC1	Interrupt Configuration 1	Static	R/W	yes	0x00
0x10	IC2	Interrupt Configuration 2	Static	R/W	yes	0x00
0x11	IBL[1:0]	IBV Low threshold	Static	R/W	yes	0x00
0x13	IBH[1:0]	IBV high threshold	Static	R/W	yes	0xFF
0x15	ID[1:0]	DPM Customer Identification	Static	OTP	N/A	0xFFFF
0x17	PB1[3:0]	Parallel Bus Register 1	Static	R/W	yes	0x00000000
0x1B	PB2[3:0]	Parallel Bus Register 2	Static	R/W	yes	0x00000000
0x1F	PB3[3:0]	Parallel Bus Register 3	Static	R/W	yes	0x00000000
0x23	PB4[3:0]	Parallel Bus Register 4	Static	R/W	yes	0x00000000
0x27	PMC	Power Manager Configuration	Static	R/W	yes	0x00
0x28	PID[31:0]	POL Identification Register	Static	R/W	yes	0x00
0x80	RTC[3:0]	Run Time Counter	Run time	R	Read only	value at last shut-down
0x84	PPS[3:0]	POL Programming Status	Run time	R		(4x) 0x00
0x88	EST	Event Status	Run time	R		0x00
0x89	IBV[1:0]	IB Voltage	Run time	R		0x00
0x8B	STA	Status of Group A	Run time	R		0x00
0x8C	STB	Status of Group B	Run time	R		0x00
0x8D	STC	Status of Group C	Run time	R		0x00
0x8E	STD	Status of Group D	Run time	R		0x00
0x8F	REL[1:0]	DPM Software Release	Static	R		According to DPM type
0x91	PSS[3:0]	POL Status Summary	Run time	R		0x00
0x95	DPMS	DPM Status	Run time	R		0x01
0x96	WP	Write Protection	Volatile	R/W		0x00

Table 1. DPM Setup Registers

The static registers are saved in the non-volatile memory and used to store the system configuration data. The run-time registers contain status information and are evaluated during run-time. The Write Protection register WP is a volatile register that defaults to write protect at power-up.

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[3] Writing into memory locations beyond address offset 0x96 must be avoided

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8.1.3   POL SETUP REGISTERS

Since the POL converters contain only RAM, the data defining performance parameters for each POL and Auxiliary Device, such as the output voltage, protection thresholds, feedback loop compensation, turn-on and turn-off delays, fault management settings, etc., is stored in the POL setup registers in the DPM. The POL setup registers consist of 23 data bytes and 2 CRC bytes. The Auxiliary Device setup registers occupy the same amount of bytes as a POL converter, but only 3 registers have meaningful data. The other registers should be filled with 0x00. The POL setup registers are listed in Table 2. Register significance is different in some cases between the new DP and older ZY series POLs which are still supported. Differences are in **bold** for the DP series devices.

ADDRESS OFFSET	REGISTER+)	CONTENT	ADDRESS OFFSET	REGISTER		CONTENT
	DP7000/ DP8000 POL			Z7000/ Z8000 POL	AUX DEVICE	
00h	PC1_x	Protection Configuration 1	00h	PC1_x	EC_x	Protection Configuration 1
01h	PC2_x	Protection Configuration 2	01h	PC2_x	reserved	Protection Configuration 2
02h	PC3_x	Protection Configuration 3	02h	PC3_x	reserved	Protection Configuration 3
03h	TC_x	Tracking Configuration	03h	TC_x	reserved	Tracking Configuration
04h	INT_x	Interleave Configuration and Frequency Selection	04h	INT_x	reserved	Interleave Configuration and Frequency Selection
05h	DON_x	Turn-On Delay	05h	DON_x	EON_x	Turn-On Delay
06h	DOF_x	Turn-Off Delay	06h	DOF_x	EOF_x	Turn-Off Delay
07h	**VLC**	**Voltage Loop Configuration**	07h	VOS_x	reserved	Output Voltage Set-point
08h	CLS_x	Current Limit Set-point	08h	CLS_x	reserved	Current Limit Set-point
09h	DCL_x	Duty Cycle Limit	09h	DCL_x	reserved	Duty Cycle Limit
0Ah	**PC4**	**Protection Configuration Register 4**	0Ah	B1_x	reserved	Dig Controller Denominator z^{-1} Coefficient
0Bh	**V1H**	**Output Voltage Setpoint 1 High**	0Bh	B2_x	reserved	Dig Controller Denominator z^{-2} Coefficient
0Ch	**V1L**	**Output Voltage Setpoint 1 Low**	0Ch	B3_x	reserved	Dig Controller Denominator z^{-3} Coefficient
0Dh	**V2H**	**Output Voltage Setpoint 2 High**	0Dh	C0L_x	reserved	Dig Controller Numerator z^{0} Coefficient Low Byte
0Eh	**V2L**	**Output Voltage Setpoint 2 Low**	0Eh	C0H_x	reserved	Dig Controller Numerator z^{0} Coefficient High Byte
0Fh	**V3H**	**Output Voltage Setpoint 3 High**	0Fh	C1L_x	reserved	Dig Controller Numerator z^{-1} Coefficient Low Byte
10h	**V3L**	**Output Voltage Setpoint 3 Low**	10h	C1H_x	reserved	Dig Controller Numerator z^{-1} Coefficient High Byte
11h	**CP**	**Controller Proportional Coefficient**	11h	C2L_x	reserved	Dig Controller Numerator z^{-2} Coefficient Low Byte
12h	**CI**	**Controller Integral Coefficient**	12h	C2H_x	reserved	Dig Controller Numerator z^{-2} Coefficient High Byte
13h	**CD**	**Controller Derivative Coefficient**	13h	C3L_x	reserved	Dig Controller Numerator z^{-3} Coefficient Low Byte
14h	**CV**	**Controller Derivative Roll-Off Coefficient**	14h	C3H_x	reserved	Dig Controller Numerator z^{-3} Coefficient High Byte
15h	reserved		15h	reserved	reserved	
16h	reserved		16h	reserved	reserved	
17h	reserved		17h	reserved	reserved	
18h	reserved		18h	reserved	reserved	
19h	reserved		19h	reserved	reserved	

1Ah	reserved		1Ah	reserved	reserved	
1Bh	reserved		1Bh	reserved	reserved	
1Ch	MRH	**Margining High Selection**	1Ch	VOML_x [#]	reserved	Output Voltage Margining Low Value
1Dh	MRL	**Margining Low Selection**	1Dh	VOMH_x [#]	reserved	Output Voltage Margining High Value
1Eh	CRC0_x [#]	Cyclic Redundancy Check Register 0	1Eh	CRC0_x [#]	CRC0_x [#]	Cyclic Redundancy Check Register 0
1Fh	CRC1_x [#]	Cyclic Redundancy Check Register 1	1Fh	CRC1_x [#]	CRC1_x [#]	Cyclic Redundancy Check Register 1

Notes:
[+] x denotes the POL address [0..31]
[#] not downloaded to the POL during programming

Table 2. POL Setup Registers

8.1.4   MONITORING DATA

The DPMs can retrieve current, temperature, output voltage, and status information from each of the POL converters and status information only from Auxiliary Devices. Monitoring data is stored in RAM and can be accessed via the I²C bus. Monitoring registers are read only.

The monitoring data consists of 5 Bytes for each POL converter and Auxiliary Device as shown in Table 3. When the status monitoring is enabled, the ST registers get continuously updated. When the parametric monitoring is enabled, the VOH, VOL, IO, and TMP registers get continuously updated. Scaling data from the registers is specific to each DP and ZY series POL. Refer to the DM73XX Programming manual for calculation information.

POL CONVERTER		AUXILIARY DEVICE	
Register	*Content*	*Register*	*Content*
ST	Status Register	ST	Status Register
VOH	Output Voltage High Byte	reserved	
VOL	Output Voltage Low Byte	reserved	
IO	Output Current	reserved	
TMP	Temperature	reserved	

Table 3. Monitoring Data Registers

8.1.5   USER MEMORY

This non-volatile memory block is reserved for users' notes and not related to other functions in the DPM. It can be used to save user-specific information such as manufacturing data and location, serial number, application code, configuration file version, warranty or repair information, etc. A total of 1024 Bytes organized in 4 pages is provided. The user memory can be accessed via the GUI System Configuration window shown in Figure 8 or directly via the I²C bus using specific commands. Content of the user memory is saved into the configuration file when the file is saved. Note that this does not change the current DPM contents until the DPM is programmed with the file currently in memory.

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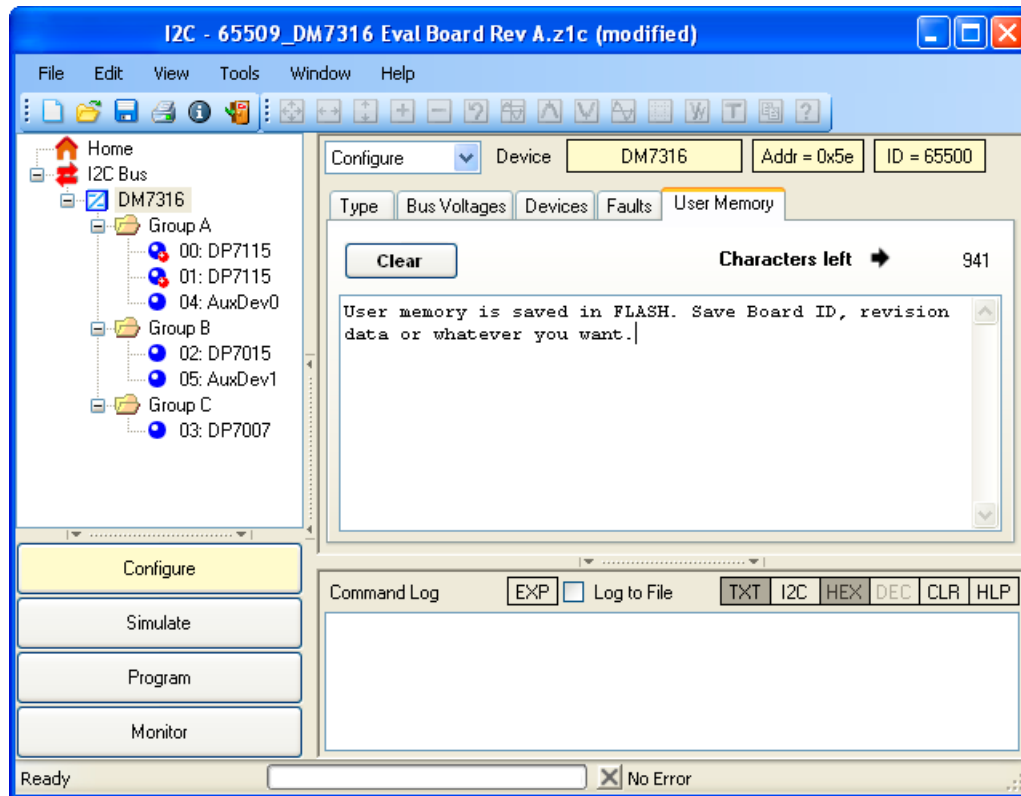**belpowersolutions.com**

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Figure 4. User Memory Window

8.2 AUXILIARY DEVICES

The DM73XX DPM includes all necessary circuitry to control and monitor four Auxiliary Devices. Virtually any device which has an on/off input and a monitoring output can be an Auxiliary Device. Typical examples of Auxiliary Devices include analog POL converters, linear regulators, and fans. Auxiliary Devices are controlled and monitored via the Graphical User Interface.

The DPM treats Auxiliary Devices as d-pwer™ POL converters: each Auxiliary Device has an address and is assigned to one of the groups as shown in Figure 8 (device at addresses 03). Turn-on and off delays can be programmed, and faults can be propagated from POL converters to the devices. Auxiliary Devices are controlled through standard group turn-on and off commands and are fully synchronized with turn-on/off timing of POL converters.

Four enable outputs EN0…EN3 control the Auxiliary Devices. Four monitoring inputs PG0…PG3 read status of the Auxiliary Devices. The enable outputs and monitoring inputs are paired together and permanently assigned to specific pins of the DPM as shown in Figure 6. Adding an AUX device is done the same way as adding a POL, select an uncommitted address and then the AUX device desired. In this example two AUX devices are already present.

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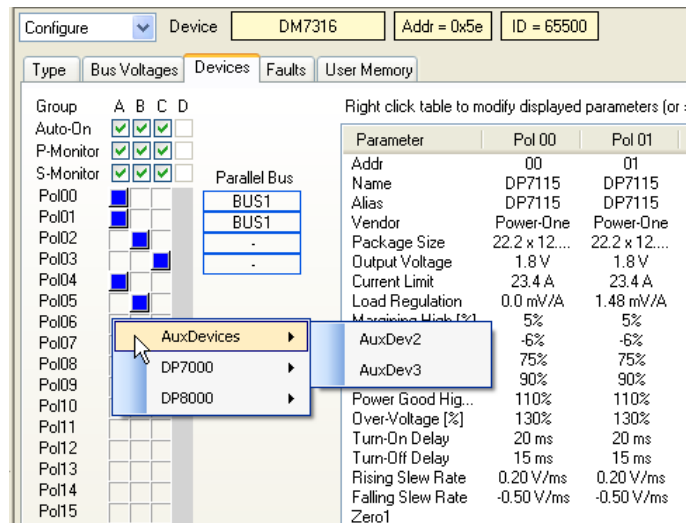
Figure 5. Auxiliary Device Type Window

Turn-on and turn-off delays can be programmed for each Auxiliary Device as shown in Figure 7. Timing of turn-on and turn-off events can be synchronized between Auxiliary Devices and POL converters by programming appropriate delays for specific types of devices.
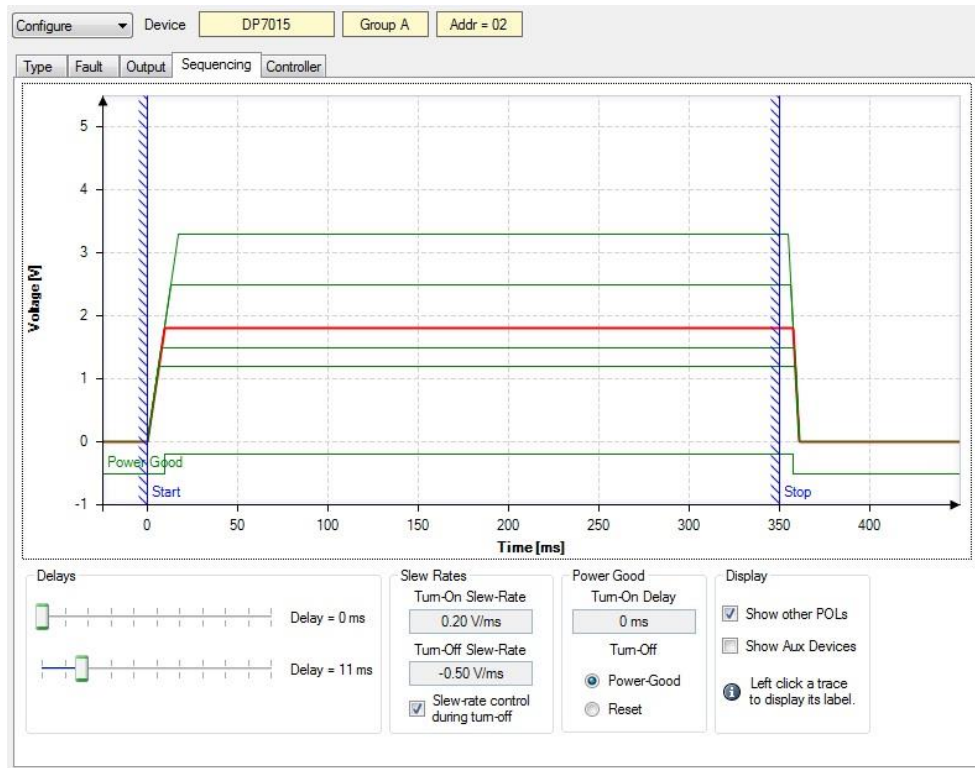

Figure 6. Sequencing Tracking Window

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8.3 DPM FUNCTIONS

8.3.1   POL PROGRAMMING

POL programming is the process of downloading the content of POL setup registers stored in DPM's non-volatile memory via the SD bus to the POL converters.

Programming of POL converters is performed upon power-up, or when the Program button is pressed in the GUI System Configuration window shown in Figure 8, or when the specific command is sent directly via the I²C bus.
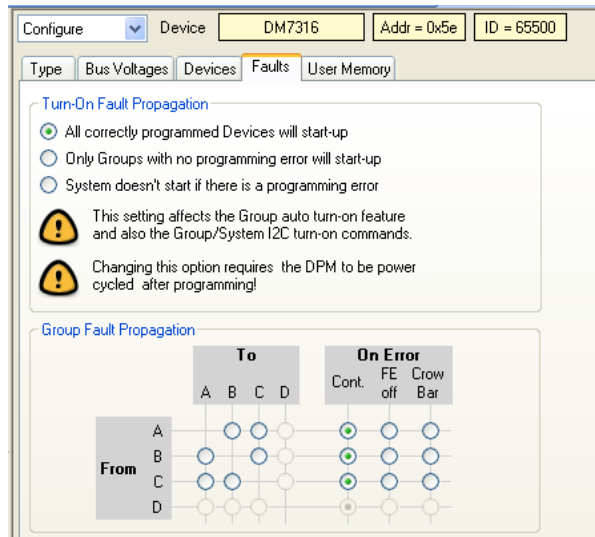
Figure 7. System Configuration Window

The programming is performed in several steps. Once the supply voltage on the VDD pins of the DPM exceeds the UVLO protection threshold, the DPM will start copying setup registers from its non-volatile memory into RAM and execute the cyclic redundancy check (CRC) to ensure integrity of the programming data. When the voltage on the IBVS pin exceeds the IBV undervoltage protection threshold, the DPM will download POL setup registers to the respective POL converter via the SD line. Every data transfer is protected by parity check and followed by the POL acknowledgement and read data back procedure. If both acknowledgement and readback operations are successful, the POL-specific bit in the POL Programming Status registers will be set. The DPM considers the POL converter to be programmed, and continues programming the next POL converter.

Upon completion of the programming, the DPM will turn-on the POL converters, if the Auto Turn-On is enabled in the POL Group configuration window shown in Figure 9 (topmost group of square buttons just below "Bus Voltages" tab. Otherwise, the user will need to send the turn-on command via the I²C bus.
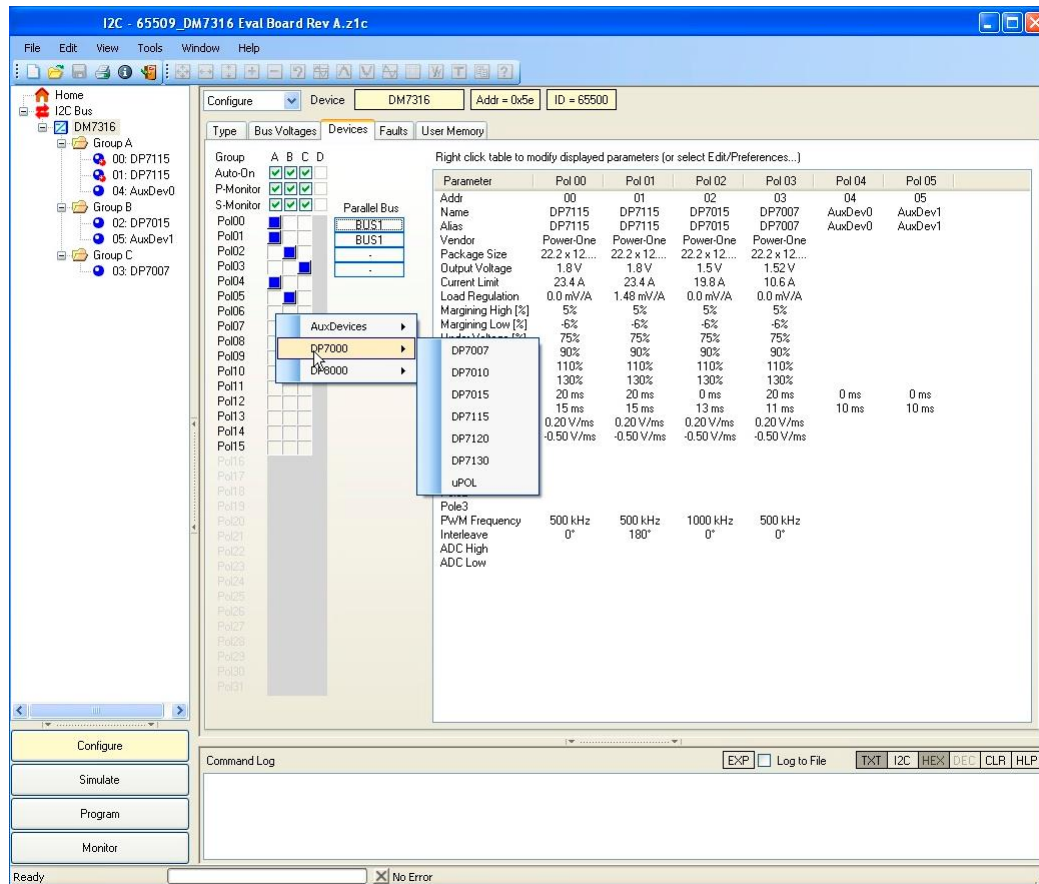
Figure 8. POL Configuration Window

8.3.2   PROGRAMMING TIME

Total system programming time can be determined from the following equation:

Where:

TPROGR - time interval from the instant when the DPM supply voltage exceeds DPM's UVLO threshold until the DPM
        issues the turn-on command. If the Auto Power-Up is enabled, and the turn-on delay is set to zero, the
        output voltages start ramping up at the end of TPROGR interval

TINIT -   DPM initialization interval after the DPM supply voltage exceeds the UVLO threshold. TINIT = 11.5ms.

TPOL -   Time required for programming and verifying of one POL converter. TPOL=26.5ms.

TAD -   Time required for programming and verifying of one Auxiliary Device. TAD = 7.5ms.

nPOL -   Number of POL converters in the system.

nAD -   Number of Auxiliary Devices in the system.

The programming data (DPM and POL setup registers and the user memory) can be preloaded into DPMs by Bel Power Solutions or the DPMs can be programmed by the user via the GUI, I²C bus, or JTAG programming interface. The DPMs can be programmed either before or after installation on a host board.

To modify POL converter settings, the user can directly access the registers of a POL converter via the I²C bus, bypassing DPM's POL setup registers. The I²C commands are translated by the DPM and converted into appropriate SD commands to read / write from / into the registers of a POL converter. Writing into these registers is limited by the hardware (LCK_N) and/or software write protections. Since POL converters do not have non-volatile memory, data written directly into POL converter registers will be lost when the input voltage is removed.

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8.4 MONITORING

8.4.1 POL MONITORING

d-pwer^{TM} and Z-one™ POL converters continuously monitor their own performance parameters such as output voltage, output current, and temperature. The monitored parameters are stored locally in the POL converters and updated every 1ms. If monitoring feature is enabled, the DPM will be continuously copying status and parametric data from POL converters into DPM's monitoring data registers.

The monitoring is enabled by checking the appropriate Retrieve Monitoring bits in the GUI Group Configuration window shown in Figure 9 or directly via the I²C bus by specific commands.

If the status monitoring is enabled, the status of each protection (overcurrent, overvoltage, etc.) is being reported. If the parametric monitoring is enabled, then real-time values of voltage, current, and temperature are being reported.

Status and parametric monitoring data of a single POL converter and groups of POL converters can be examined in the GUI IBS Monitoring Window shown in Figure 10 or directly via the I²C bus using specific commands. Status data for each group of POL converters is presented in the Group Status block in the left top corner of the window. Parametric data for individual POL converters is shown in Voltage [V], Current [A], and Temp [T] screens.

DPMs also monitor and report programming status of each POL converter and results of CRC operations.

8.4.2 MONITORING OF AUXILIARY DEVICES

The DPM can read status information of the Auxiliary Devices via the PG0…PG3 inputs. The PG0…PG3 are digital 3.3V compliant inputs with internal pull-up resistors. Logic high input on a PGX pin should correspond to normal operation of an Auxiliary Device.

Status monitoring data of Auxiliary Devices is stored in the DPM and displayed in the IBS Monitoring Window shown in Figure 10.
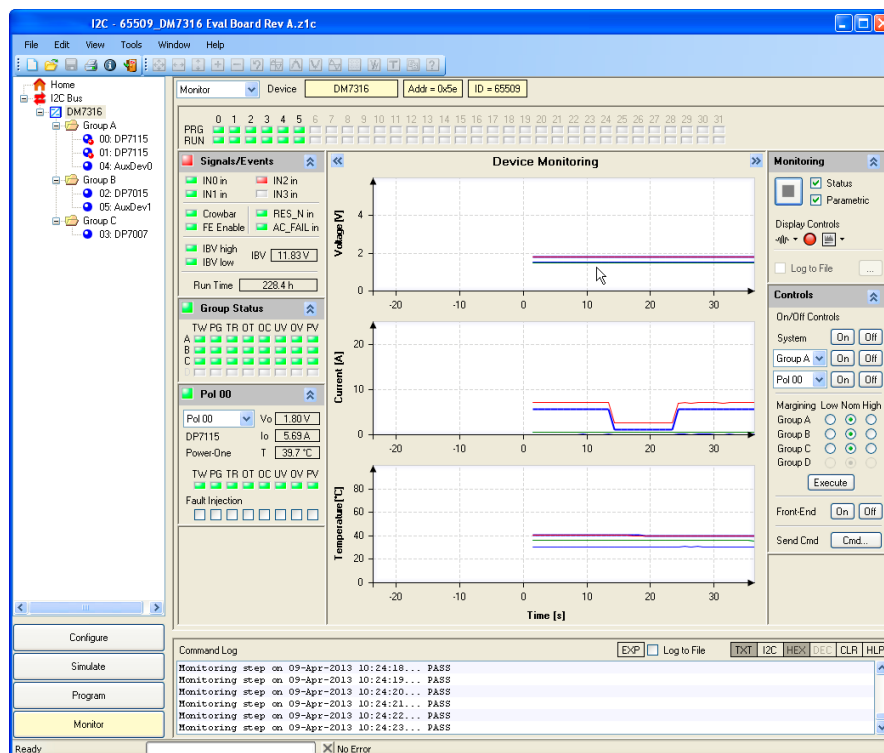

Figure 9. IBS Monitoring Window

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8.4.3   RUN TIME COUNTER

The DPM also monitors the duration of time that it has been in operation. The 4 bytes Run Time Counter is active whenever the DPM is powered up. The count rate is 1 second. The counter is loaded into RAM upon power-up and the new count state is periodically saved to the non-volatile memory. Contents of the counter can be examined in the GUI IBS Monitoring Window shown in Figure 10 or directly via the I²C bus using specific commands.

8.4.4   IBV MONITORING

The DPM continuously monitors the intermediate bus voltage via the IBVS input and the built-in 10-bit ADC. The digital representation of the bus voltage is stored in RAM and reported in the IBS Monitoring window shown in Figure 10.
In addition, the DPM continuously compares the value of IBV to the Undervoltage and Overvoltage thresholds programmed in the GUI Intermediate Bus Configuration Window shown in Figure 11.
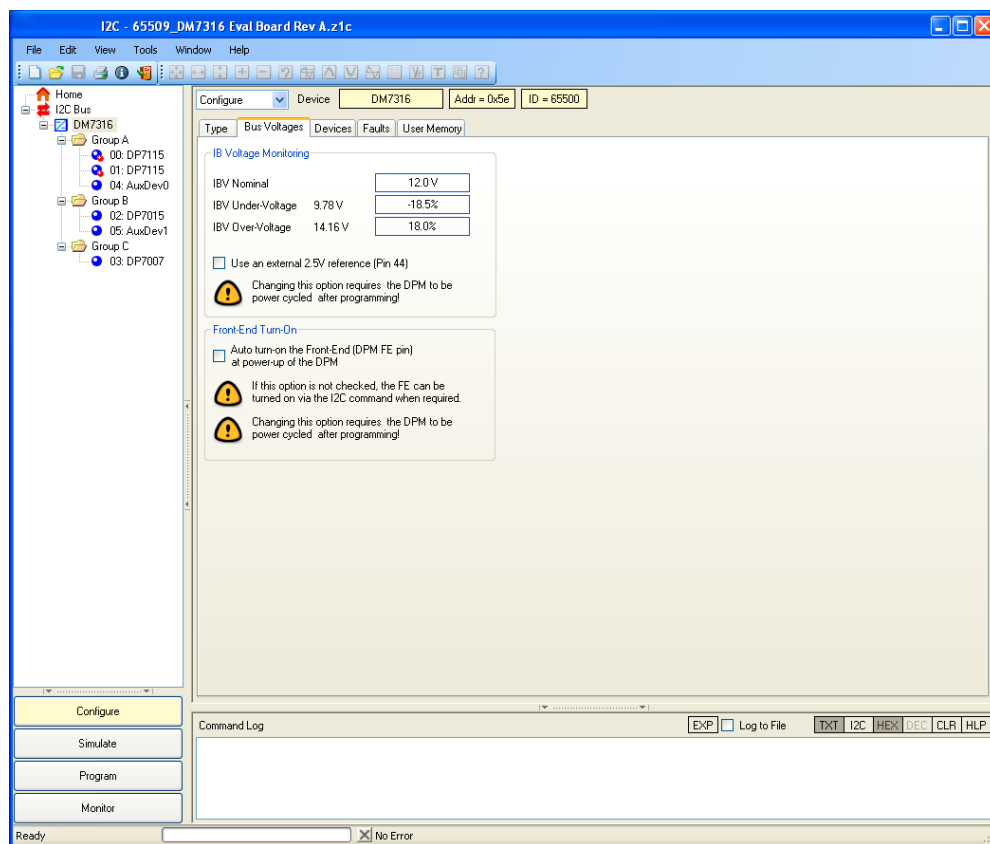

Figure 10. Intermediate Bus Configuration Window

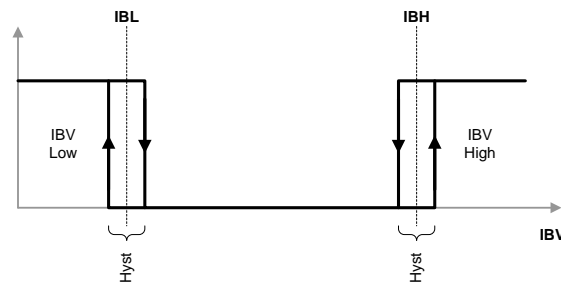The thresholds have a symmetric, fixed size hysteresis as shown in Figure 12.

Figure 11. Undervoltage (IBL) and Overvoltage (IBH) Protections Hysteresis

When the IBV decreases below the IBL threshold minus the hysteresis, the DPM will pull OK lines low turning off all POL converters. The POL converters will execute regular turn-off ramping their output voltages down according to the turn-off delay and falling slew rate settings. In addition, the DPM will clear all bits in the POL Programming Status registers and save the content of the Run Time Counter into the non-volatile memory. The IBV Low bit in the IBS Monitoring Window will change to red. When the IBV recovers above the IBL threshold plus the hysteresis, the DPM will first program all POL converters and then turn them on, if the Auto Turn-On is enabled in the POL Group configuration window shown in Figure 9. Otherwise, the user will need to send the turn-on command via the I²C bus.

When the IBV exceeds the IBH threshold plus the hysteresis, the DPM will pull OK lines low turning off all POL converters. The POL converters will execute regular turn-off ramping their output voltages down according to the turn-off delay and falling slew rate settings. In addition, the DPM will save the contents of the Run Time Counter into the non-volatile memory. If the IBV does not decrease below the IBH threshold minus the hysteresis within the next 50ms, the DPM will pull low the FE_EN output and clear all bits in the POL Programming Status registers. The IBV High bit in the IBS Monitoring Window will change to red. If the IBV still does not change, in 50ms the DPM will pull the CB pin high for 1ms to trigger an optional crowbar protection.

One second after the IBV decreases below the IBH threshold minus the hysteresis, the DPM will pull the FE_EN high and program all POL converters. Upon completion of the programming process, the DPM will turn on the POL converters, if the Auto Turn-On is enabled in the POL Group configuration window shown in Figure 9.

The propagation delay between the IBV increasing/decreasing above/below corresponding thresholds and the DPM pulling down OK lines and triggering the turn-off process is approximately 1ms.

8.4.4.1   VOLTAGE REFERENCE

For the purposes of IBV monitoring the user can select either the DPM's internal voltage reference or an external 2.5V voltage reference. The selection is made by clicking an appropriate radio button in the DPM Configuration/Bus Voltages dialog as shown previously in Figure 11.
The DPM's internal 2.56V voltage reference is effective accuracy of the IBV protection thresholds to 15%. If the accuracy is sufficient, the user does not need to make any changes to the schematic shown in Figure 3. If higher accuracy of the IBV monitoring is desired, then a 2.5V external reference can be added as shown in Figure 13. The GUI automatically changes values of the IBL and IBH thresholds when the reference selection is changed.

Note: If the Reference Voltage setting is changed during operation of the DPM, then the power to the DPM needs to be cycled or the HRES_N pin needs to be pulled low and released.
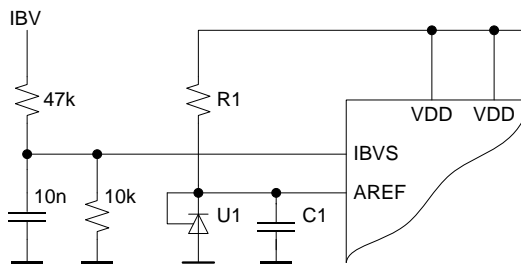

Figure 12. External Voltage Reference Connections

U1 and R1 are additional components. U1 is an industry standard 2.5V voltage reference such as TL431 or similar. C1 is an existing component but its value changes depending on the type of voltage reference. Common voltage reference part numbers and values of associated components are shown in Table 4.

U1 Part Number	TL431	ZR431
Manufacturer	TI	Zetex
Accuracy, %	0.5, 1, 2	0.5, 1, 2
R1, Ohms	100-620	510-2000
C1, µF	≥ 10	≥ 0.01

Table 4. Component Values for External Reference

Accuracy of the protection thresholds in the case of external reference is determined by the sum of accuracy of the voltage reference, accuracy of the 10k/47k resistive divider shown in Figure 13, and conversion error of the internal ADC specified in 7.2.

8.5 POL GROUP MANAGEMENT

POL converters and Auxiliary Devices can be arranged in up to four groups. A group of POL converters is defined as a number of POL converters with interconnected OK pins. Auxiliary Devices are added to a group in the GUI, without any external connections. A group can include from 1 to 32 POL converters, but a POL converter can be a member of only one group. In addition, the OK lines can be connected to the DPM to facilitate propagation of faults and errors between groups. One DPM can manage up to four independent groups: A, B, C, and D, depending on model of the DPM.

Group management includes fault and error propagation, margining, turn-on and turn-off, monitoring setup, and interrupt configuration.

8.5.1   FAULT AND ERROR PROPAGATION

dP-series POL converters protect outputs by triggering either a fault or an error depending on the severity of the problem (see POL converter datasheets). Fault propagation between POL converters belonging to the same group is a programmable function of POL converters. The DPM allows propagating faults and errors between groups of POL converters and, in case of an error, to a DC/DC front-end and an optional crowbar. The propagation delay for fault/error propagations is less than 10µs.

To enable fault and error propagation, the respective bits needs to be checked in the GUI Fault and Error Propagation window shown in Figure 14. Note that cross propagation of faults/errors (means fault in Group X propagates to Y and vice versa) should be avoided.
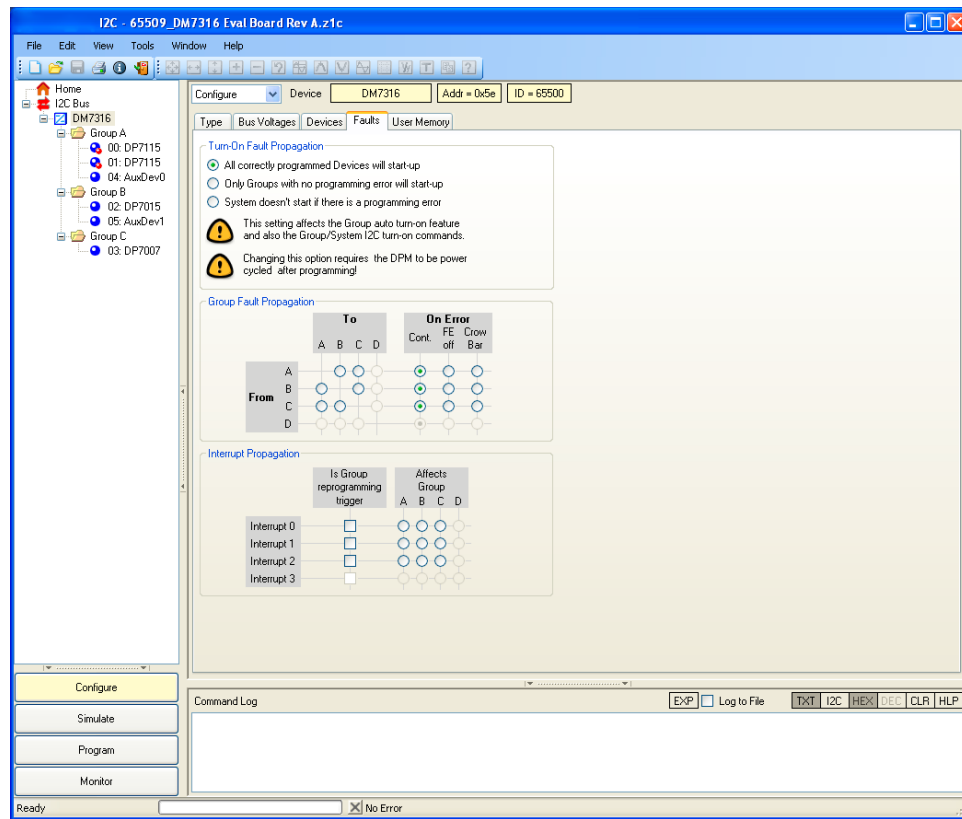
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Figure 13. Fault and Error Propagation Window

The fault propagation from POL converters to the auxiliary devices can be disabled by checking the bit in the Auxiliary Device Fault Management window as shown in Figure 15. It is not possible to propagate a fault from an Auxiliary Device to POL converters.
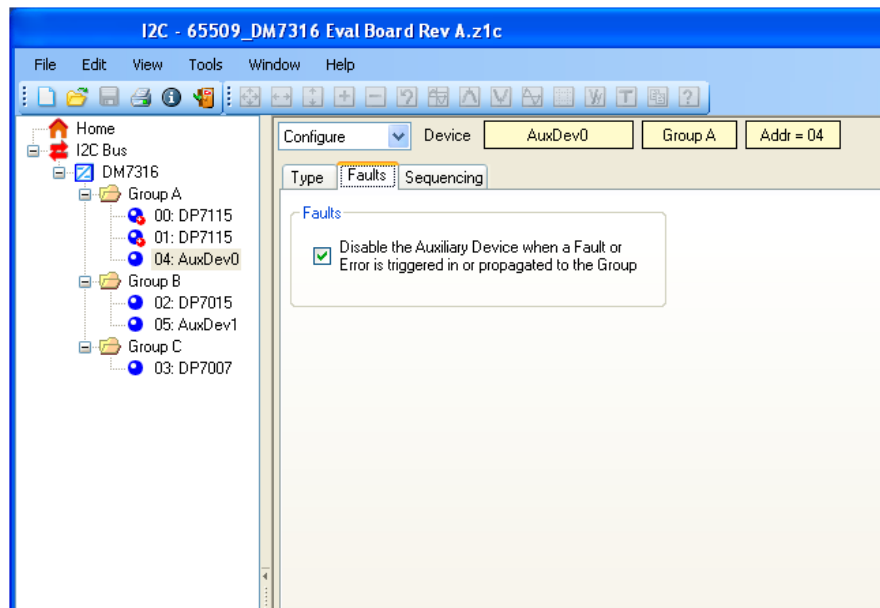
Figure 14. Auxiliary Device Fault Management Window

Protection Triggered	Propagation Between POLs	Propagation To Auxiliary Devices in the Same Group as the Faulty POL	Propagation To Auxiliary Devices in Other Groups	Propagation Between Groups of POLs	Faulty POL	POLs in the Same Group as the Faulty POL	Auxiliary Devices in the Same Group as the Faulty POL	POLs in Other Groups	Auxiliary Devices in Other Groups
UVP or OTP	Enabled	Disabled	Any	Disabled	Regular turn-off	Regular turn-off	Continue operating	Continue operating	Continue operating
UVP or OTP	Enabled	Enabled	Any	Disabled	Regular turn-off	Regular turn-off	Turn-off with turn-off delay	Continue operating	Continue operating
UVP or OTP	Enabled	Enabled	Disabled	Enabled	Regular turn-off	Regular turn-off	Turn-off with turn-off delay	Regular turn-off	Continue operating
UVP or OTP	Enabled	Enabled	Enabled	Enabled	Regular turn-off	Regular turn-off	Turn-off with turn-off delay	Regular turn-off	Turn-off with turn-off delay
Tracking or OCP	Enabled	Disabled	Any	Disabled	Fast turn-off	Regular turn-off	Continue operating	Continue operating	Continue operating
Tracking or OCP	Enabled	Enabled	Any	Disabled	Fast turn-off	Regular turn-off	Turn-off with turn-off delay	Continue operating	Continue operating
Tracking or OCP	Enabled	Enabled	Disabled	Enabled	Fast turn-off	Regular turn-off	Turn-off with turn-off delay	Regular turn-off	Continue operating
Tracking or OCP	Enabled	Enabled	Enabled	Enabled	Fast turn-off	Regular turn-off	Turn-off with turn-off delay	Regular turn-off	Turn-off with turn-off delay
OVP or Phase Voltage	Enabled	Disabled	Any	Disabled	Fast turn-off, low side FET is ON	Fast turn-off	Continue operating	Continue operating	Continue operating
OVP or Phase Voltage	Enabled	Enabled	Any	Disabled	Fast turn-off, low side FET is ON	Fast turn-off	Turn-off without turn-off delay	Continue operating	Continue operating
OVP or Phase Voltage	Enabled	Enabled	Disabled	Enabled	Fast turn-off, low side FET is ON	Fast turn-off	Turn-off without turn-off delay	Regular turn-off	Continue operating
OVP or Phase Voltage	Enabled	Enabled	Enabled	Enabled	Fast turn-off, low side FET is ON	Fast turn-off	Turn-off without turn-off delay	Regular turn-off	Turn-off with turn-off delay

Table 5. Fault and Error Propagation Scenarios

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When propagation is enabled, the faulty POL converter pulls its OK pin low. A low OK line initiates turn-off of other POL converters in the group and signals the DPM to pull other OK lines low to initiate turn-off of other POL converters as programmed.

The regular turn-off of a POL converter means that the output voltage is ramping down according to its turn-off delay and falling slew rate settings. If a POL converter triggers an undervoltage or overtemperature fault, it will initiate the regular turn-off. In the case of an overcurrent or tracking fault, the POL converter initiates the fast turn-off by opening both high and low side switches instantaneously. If either output overvoltage or phase voltage errors are triggered, the faulty POL converter initiates the fast turn-off and turns on its low side switch. In addition, when an error is propagated, the DPM can generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) and trigger an optional crowbar protection to accelerate removal of the intermediate bus voltage (IBV).

Once the fault has recovered in the faulty POL converter, the other POL converters will turn on in a controlled manner according to their turn-on delay and rising slew rate settings.

8.5.2   MARGINING

Margining can be executed separately for each group by clicking an appropriate radio button in the GUI IBS monitoring window shown in Figure 10 or directly via the I²C bus by the margining command. All POL converters in a group are margined in the same direction (up or down) by the percentage programmed individually for each POL converter.

8.5.3   TURN-ON AND TURN-OFF

Automatic turn–on upon application of the input voltage is enabled by checking the Auto Turn-On bit in the GUI Group Configuration window shown in Figure 9. Turn-on and turn-off of various groups during the operation is controlled from the GUI IBS Monitoring window or directly via the I²C bus by specific commands.

8.5.4   INTERRUPT CONFIGURATIONS

The DPM has four interrupt inputs that can be programmed to:
- Inhibit the operation of one or several Groups of POL converters when pulled low or
- Act as a Group Reprogramming Trigger.

The two functions are mutually exclusive – an interrupt can be either programmed as an Inhibit or as a Group Reprogramming Trigger.

The interrupts are programmed in the GUI Interrupt Configuration window shown in Figure 16 or directly via the I²C bus by specific commands. In Figure 16 the Interrupt 0 is programmed as the inhibit for group A and the Interrupt 2 is programmed as the group C reprogramming trigger.

8.5.4.1   GROUP INHIBIT

An interrupt input can be programmed to act as an inhibit on a single or multiple groups of POL converters. When the interrupt input is pulled low, the DPM will pull the appropriate OK lines low. The affected POL converters will execute regular turn-off ramping their output voltages down according to the turn-off delay and falling slew rate settings. Once the interrupt is released, the POL converters will automatically turn-on according to their turn-on delay and rising slew rates settings.

The inhibit function can be used for a variety of applications, such as
- Hardware-based control of groups of POL converters and Auxiliary Devices
- Delayed turn-on at power-up (Automatic Turn-On is enabled but the interrupts are held low during power-up. Note that POL converters can be programmed even when an interrupt is held low.)

The interrupt inputs should be controlled with open collector devices. The propagation delay between the external device pulling the interrupt input low and the DPM pulling down OK lines and triggering the turn-off process is approximately 10µs. This option is set as part of DPM/Configure/Faults dialogs.
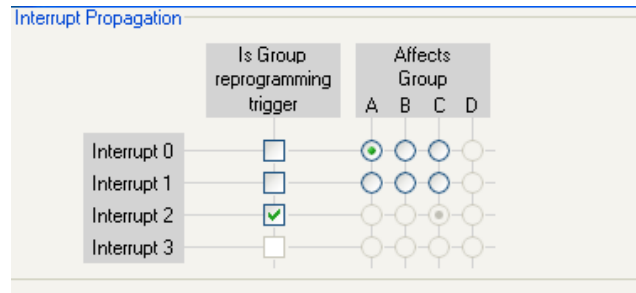
Figure 15. Interrupt Configuration Dialog

8.5.4.2   GROUP REPROGRAMMING TRIGGER

An interrupt that is programmed as a group reprogramming trigger always acts only on one group of POL converters. Interrupt 0 acts on Group A, Interrupt 1 acts on Group B and so on. The assignment is fixed and cannot be changed by the user.

When the interrupt is pulled low, the DPM will program the group of POL converters. Upon completion of the programming, the DPM will turn-on the POL converters, if the Auto Turn-On is enabled. When the interrupt input is released, the DPM will pull the appropriate OK line low. The POL converters in the group will execute regular turn-off ramping their output voltages down according to the turn-off delay and falling slew rate settings. In addition, the DPM will clear all bits in the POL Programming Status registers.

The group reprogramming trigger is mostly used to support hot swap of boards and daughter cards that do not have a DPM installed on them as shown in Figure 17.
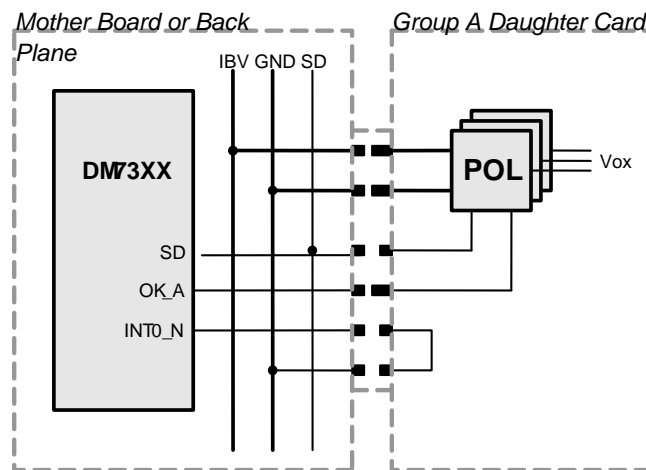

Figure 16. INT0 Configured as Group A Reprogramming Trigger

In this configuration the Interrupt 0 (INT0_N) is configured as the group A reprogramming trigger. The DPM is installed on a mother board or a backplane. A daughter card with a group of POL converters is being inserted in the system during normal operation. At first, the long pins carrying power and the OK_A line signal make contact. Then the short pins carrying the SD and interrupt signals make contact. Once the interrupt senses low input voltage, it will command the DPM to program all POL converters in the group A. Upon completion of the programming, the DPM will turn-on the POL converters, if the Auto Turn-On is enabled.

When the daughter card is being removed, the interrupt input is released as soon as the short pins break the contact. The DPM will immediately pull the OK_A line low turning off all POL converters in the group A according to the turn-off delay and falling slew rate settings.

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8.6 CONTROLS

8.6.1 ACFAIL_N AND RES_N

The ACFAIL_N and RES_N are active low digital inputs. When one of the inputs is pulled low, the DPM will pull all OK lines low turning off all the POL converters and the Auxiliary Devices in all groups. The POL converters will execute regular turn-off ramping their output voltages down according to the turn-off delay and falling slew rate settings. In addition, the DPM will clear all bits in the POL Programming Status Registers and save the contents of the Run Time Counter into the non-volatile memory. The AC_FAIL in or RES_N in bit in the IBS Monitoring Window will change to red. When the input is released, the DPM will first program all POL converters and then turn them on, if the Auto Turn-On is enabled. Otherwise, the user will need to send the turn-on command via the I²C bus.

The ACFAIL_N is typically connected to an AC-DC front end. Whenever the AC voltage disappears, the ACFAIL_N signal will be set low. If there is no battery backup, it usually means the DC output will disappear after 20ms. If the turn-off delays and falling slew rates of each POL converter are set to the values such that all POL converters will have fully turned off within the hold time of the AC-DC front end, then output voltage tracking during turn-off is guaranteed.

The RES_N input has the same functionality as the ACFAIL_N input and can be connected to a simple turn on/off switch or to a sensor that shuts the entire system down when it is activated.

The ACFAIL_N and RES_N inputs should be controlled with open collector devices. The propagation delay between the external device pulling the input low and the DPM pulling down OK lines and triggering the turn-off process is approximately 1ms.

8.6.2 FRONT END ENABLE

The FE_EN pin is dedicated to the control of a DC-DC Front End. The Front End is typically used to convert the 48V into the intermediate bus voltage (IBV). If the DPM is powered from an auxiliary source, not from the IBV, it can control the DC-DC Front End.

When FE_EN is internally pulled up to 3.3V, the Front End is enabled. The FE_EN output can provide up to 5mA of current. When the FE_EN goes low, the Front End is disabled. The Front End can be enabled and disabled via the GUI IBS Monitoring Window or directly via the I²C bus using specific commands.

The FE_EN pin should not be directly connected to the Enable pin of the DC-DC Front End. Typically, the Enable pin is referenced to the primary side of the Front End that is isolated from the low voltage secondary side. In addition, the Enable pin can be pulled up internally to a voltage potentially damaging to the DPM FE_EN output. The best method is to interface the DPM with the Front End through an optocoupler as shown in Figure 18. This configuration provides interface for negative logic front ends.
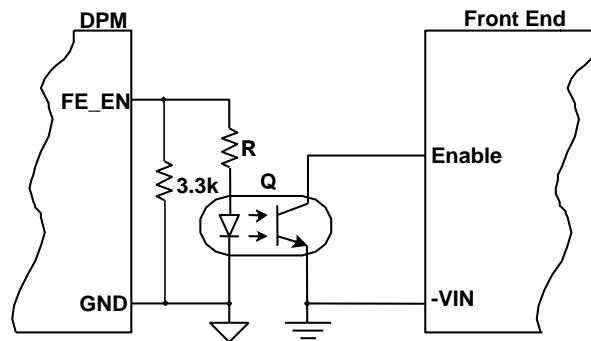

Figure 17. Interface between DPM and DC-DC Front End

8.6.3 CROWBAR

When the crowbar protection is enabled, the CB pin is internally pulled up to 3.3V for 1ms. It is capable of supplying 5mA to turn on a crowbar circuit.

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8.6.4   HRES_N

The HRES_N is an active low digital input. When it is pulled low, the DPM will perform full hardware reset including processor, memory, and communication interface. The POL converters and auxiliary devices will be turned off although sequencing and tracking during the turn-off are not guaranteed. Communication with a host processor or GUI (if established) will be lost. When the input is released, the DPM will first program all POL converters and then turn them on, if the Auto Turn-On is enabled.

Unlike all other I/O pins on the DM73XX DPM, the HRES_N does not have an internal ESD protection diode connected to VDD. Therefore, it is necessary to add the diode externally as shown in Figure 3.

The HRES_N function is intended as an emergency reset and except as indicated below, should not be used in normal system operation.

It is **necessary** to use an external reset circuit (see Fig. 3) to hold the HRES_N line low until the VDD supply reaches steady state conditions. Bel Power Solutions Inc. successfully tested the On-Semi voltage detector p/n NCP303LSN27T1 although other similar devices can also be utilized. Alternatively, the HW_RES pin can be connected to the output of a CPLD (or similar device) and controlled via the system supervisory circuitry.

8.7 COMMUNICATION INTERFACES

8.7.1   I²C INTERFACE

The DM73XX series DPMs have the industry standard I²C interface fully meeting the requirements of the I²C -Bus Specification Version 2.1 from Philips Semiconductors. The I²C interface is working in the following configurations:

- standard (100kbs) and fast (400kbs) data transfer rates
- 7-bit addressing: 4 MSBs fixed, 3 LSBs programmable by ADDR [2:0]. The address prefix of the DM73XX is 0x50. This allows encoding DPM addresses 0x50, 0x52, …, 0x5E (Bit0 is the read/write bit)

The DPM always acts as the I²C slave while the host processor always acts as the I²C master. Refer to the "DPM Programming Manual" for the detailed description of the I²C communications.

Note: It is recommended to use Bel Power Solutions ZM00056-KIT USB to I²C Adapter kit for the communication between a DPM and a computer with the Bel Power Solutions I²C Graphical User Interface.

8.7.1.1   WATCHDOG TIMER

In order to prevent occasional hanging of the I²C bus, a watchdog timer is started whenever an I²C command is initiated. If the command is not executed before the watchdog times out, the DPM will assume that the I²C bus is in an error condition (e.g. the SCL or SDA lines are pulled low continuously) and it will reset the I²C bus. The watchdog timeout is 1000ms. Since the watchdog function is not a part of the standard I²C specifications, it can be disabled by the user.

8.7.2   JTAG INTERFACE

The DM73XX series DPMs feature the JTAG interface that can be used for programming the DPM with user-specific configuration settings. JTAG boundary-scan capabilities are not currently supported.

JTAG-programmable DPMs have unique 5-digit identifiers listed in Table 6.

BASE PART NUMBER	5- DIGIT IDENTIFIER
DM7304G	65515
DM7308G	65516
DM7316G	65517
DM7332G	65518

Table 6. JTAG Programmable DPM Part Numbers

Only the DPM part numbers listed in the table can be programmed via the JTAG interface.

Note: The DPMs can be programmed via the JTAG only once. After initial programming via the JTAG, the DPMs may be reprogrammed via I²C as necessary.

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8.7.2.1 SVF FILE

In order to program a DPM via the JTAG interface, the Serial Vector Format (SVF) file needs to be generated. Click Generate SVF button in the System Configuration window shown in Figure 8. It will open the SVF Generator window shown in Figure 19.

The window allows specifying the location of the target DPM in the JTAG chain and setting delays to generate the appropriate Serial Vector Format file. The resulting file is used to program the DPMs through the JTAG interface.

Refer to "Programming DM73XX DPMs via JTAG Interface" Application Note for more details.
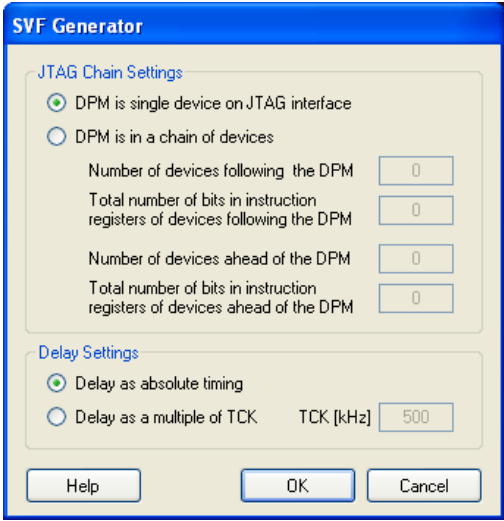

Figure18. SVF File Generator Window

8.7.2.2 JTAG INSTRUCTIONS

DM73XX series DPMs support only BYPASS and IDCODE instructions defined by IEEE 1149.1. SAMPLE/PRELOAD and EXTEST instructions are not currently supported. Summary of the supported instructions is shown in Table 7.

INSTRUCTION	OPCODE	REGISTER	FUNCTION
BYPASS	1111	Bypass	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the DPM to other devices in the JTAG chain
IDCODE	0001	JTAG ID	Selects the ID register and places it between the TDI and TDO

Table 7. JTAG Instructions

Note: The Instruction Register is 4-bit wide

8.7.2.3 IDENTIFICATION REGISTER

Format and contents of the JTAG Identification Register are shown in Table 8.

	MSB					LSB	
BIT	31	28	27	12	11	1	0
DESCRIPTION	Version		Part Number		Manufacturer's Identity		1
CONTENTS	0000		1001010100000010		00000011111		1

Table 8. JTAG ID Register

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9. PINOUT TABLE

PIN NAME	PIN NO.	PIN TYPE	BUFFER TYPE	PIN DESCRIPTION	NOTES
VDD	6, 25, 42, 57, 60	Supply	---	Positive Supply	
VSS	8, 9, 26, 38, 43, 58	Supply	---	Ground	
SD	56	I/O	ST/OCPU	Sync-Data Line	
OKA OKB OKC OKD	11 13 20 53	I/O	ST/OCPU	OK Lines	
FE_EN	17	O	CMOS	Front-End Enable	
CB	23	O	CMOS	Crowbar Trigger	
SDA	30	I/O	ST/OC	I²C Interface	
SCL	27	I/O	ST/OC	I²C Interface	
ADDR0 ADDR1 ADDR2	47 46 45	I	STPU	I²C Interface Address	
IN0_N IN1_N IN2_N IN3_N	41 40 37 36	I	STPU	Interrupts	
TCK TMS TDO TDI	31 32 33 34			JTAG Interface	Leave open, if JTAG interface is not utilized
EN0 EN1 EN2 EN3	5 7 55 50	O	CMOS	Auxiliary Device Enables	
PG0 PG1 PG2 PG3	54 52 51 49	I	STPU	Auxiliary Device Power Good	
RES_N	18	I	STPU	System Soft Reset	
ACFAIL_N	16	I	STPU	AC-Fail Trigger	
LCK_N	61	I	STPU	Write Protect Lock	
HRES_N	4	I	STPU	Cold Reset	See important usage instructions in paragraph 10.6.4
IBVS	48	I	A	Intermediate Bus Voltage Sense	
AREF	44	-	A	Analog Reference	
IR	63			Internal Reset	Connect to VSS via 10k
NC	1, 2, 3, 10, 12, 14, 15, 19, 21, 22, 24, 28, 29, 35, 39, 59, 62, 64	-	-	No Connect	Leave floating

Legend: I = input, O = output, I/O = input/output, P = power, ST = Schmitt-trigger, OCPU = open collector with pull-up, OC = open collector, CMOS = CMOS output stage, STPU = Schmitt-trigger with pull-up, A = analog

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10. PINS DESCRIPTION

ACFAIL_N, AC Fail Input (Pin 16):
Schmitt-Trigger input with internal pull-up resistor (active low). Pulling low the input indicates to the DPM that an AC-DC front-end has lost the mains and that a system shut down should immediately be initiated.

ADDR[0:2], I²C Address Inputs (Pins 47, 46, 45):
Inputs with internal pull-up resistor. The 3 bit encoded address determines the DPM communication address for the I²C interface.

AREF, Analog Reference (Pin 44):
An analog reference which is used internally. A 10nF capacitor should be connected as close as possible to the package between AREF and VSS. See 9.4.4.1.

CB, Crowbar Output (Pin 23):
A CMOS output which is used to trigger a crowbar (SCR) in case of overvoltage on the Intermediate Voltage Bus.

EN[0:3], Enable Outputs for Auxiliary Devices (Pins 5, 7, 55, 50):
CMOS outputs to control Auxiliary Devices like linear regulators, analog POLs, fans or other devices.

FE_EN, Front-End Enable (Pin 17):
A CMOS output which is used to turn-on/off the DC/DC converter generating the IBV.

HRES_N, Hardware Reset (Pin 4):
Input with internal pull-up resistor. When pulled low a cold start of the Digital Power Manager is initiated. Refer to paragraph 10.6.4 for important information regarding connections of this pin.

IBVS, Intermediate Voltage Bus Sense (Pin 48):
Analog input to an internal ADC circuit to measure the Intermediate Bus Voltage. The full scale range of the input is 2.56V and the IBV should be scaled down by a factor of 5.7 for proper reporting of the IBV with the d-pwer™ GUI.

INT[0:3], Interrupts (Pins 41, 40, 37, 36):
Four active low inputs with internal pull-ups. Each of the inputs can be configured for two functions: first, the interrupt input acts on the OK line(s) to stop momentarily the operation of group of POLs and Auxiliary Devices, second the interrupt can be used as a hot swap trigger. In this function the interrupt input triggers the programming of a group. When released, POLs are assumed to be disconnected from the DPM.

IR, Internal Reset (Pin 63):
Connect to VSS via a 10kOhm resistor.

LCK_N, Memory Lock (Pin 61):
Active low input with internal pull-up. When LCK_N is pulled low, all memory within the DPM is write-protected. The write protection cannot be disabled by software.

OKA, OKB, OKC, OKD, Group OK Signals (Pins 11, 13, 20, 53):
An open drain input/output with internal pull-up resistor. Pulling low the OK input will indicate to the DPM a fault in a Group, the DPM can also pull an OK line low to disable a Group.

PG[0:3], Power Good (Pins 54, 52, 51, 49):
Input with internal pull-up resistor. The pin is used to read the status of an Auxiliary Device.

RES_N, Active Low Reset In/Out (Pin 18):
Input with internal pull-up resistor. When pulled low a soft reset of the system (sequenced turned off of all POLs and Auxiliary Devices) is initiated. When released the whole system is reprogrammed and started if necessary.

SD, Sync Data Line (Pin 56):
An open drain input / output with internal pull-up resistor. Communication line to distribute a master clock to all converters and at the same time to communicate with all POLs.

JTAG Interface (Pins 34, 33, 32, 31):
Connect to a JTAG IEEE-1149.1-compliant programmer supporting SVF files or leave open, if not used.

VDD, Positive Supply (Pins 6, 25, 42, 57, 60):
Supply voltage. At least 4x100nF decoupling capacitors should be connected between VDD and VSS pins. All VDD pins must be connected.

VSS, Ground (Pins 8, 9, 26, 38, 43, 58):
Ground. Decoupling capacitors need to be connected as close as possible to the pins. All VSS pins must be connected.

NC, No Connect (Pin 1, 2, 3, 10, 12, 14, 15, 19, 21, 22, 24, 28, 29, 35, 39, 59, 62, 64):
All nc pins must remain floating.
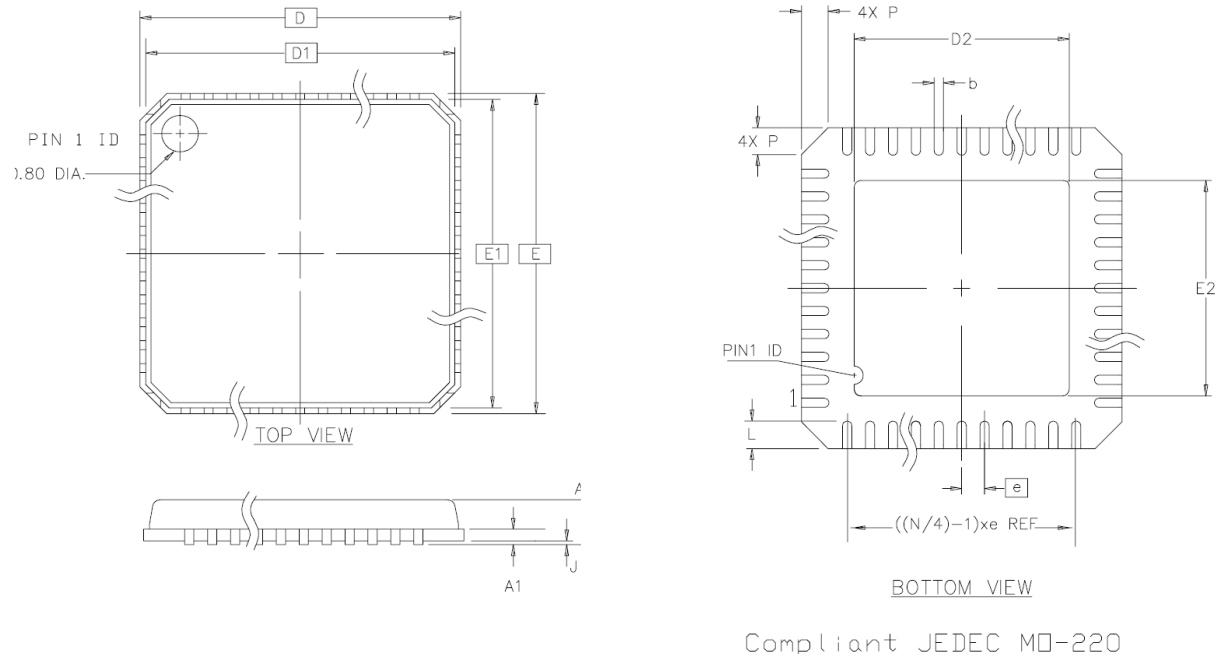
DM73XX Series

11. MECHANICAL DRAWINGS

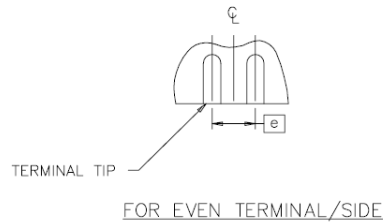Figure 19. DM73XX Mechanical Drawing

Figure 20. DM73XX Terminals

	mm			inch		
	MIN	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.80	-	1.00	0.032	-	0.040
J	0.0	0.01	0.05	0.000		0.002
A1	0.20 ref			0.008 ref		
D/E	9.00 BSC			0.354 BSC		
D1/E1	8.75 BSC			0.344 BSC		
D2/E2	4.50	4.70	4.90	0.177	0.185	0.193
N	64					
P	0.24	0.42	0.60	0.009	0.016	0.024
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.55	0.012	0.016	0.022
b	0.18	0.25	0.30	0.007	0.010	0.012

Notes: Compliant to JEDEC standard MO-220 variation VMMD-3

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Note:
- all "nc" - pins must remain floating
- all "VSS" - pins need to be connected together
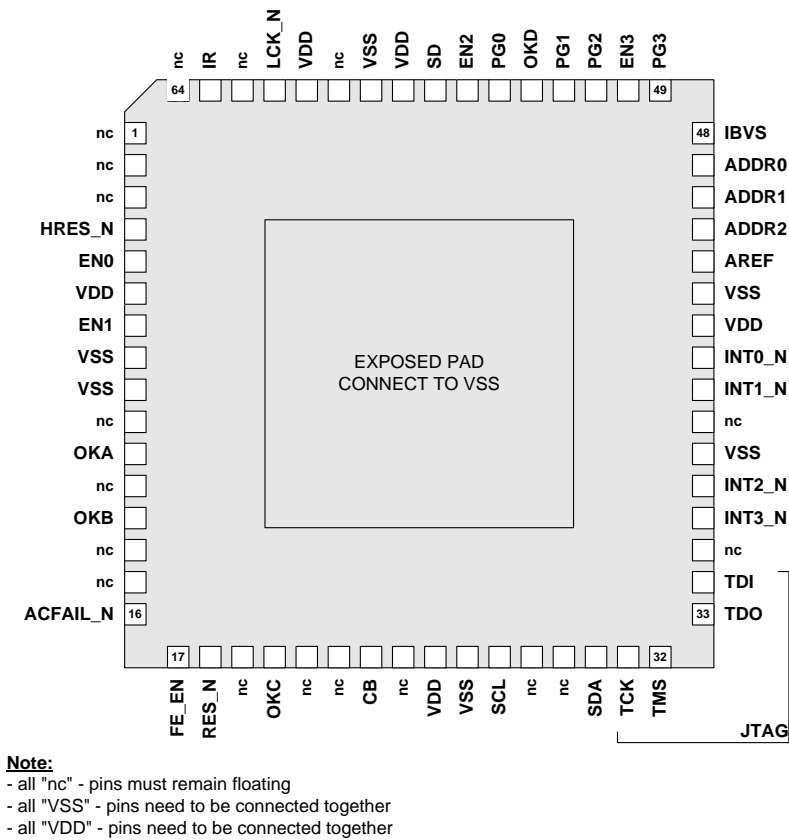- all "VDD" - pins need to be connected together

Figure 21. DM73XX Mechanical Drawing – Top View

Note: I²C is a trademark of Philips Corporation

12. ORDERING INFORMATION

DM	73	xx	G	–	yyyyy	–	zz
PRODUCT FAMILY	**SERIES**	**NUMBER OF D-PWER™ POLS AND AUXILIARY DEVICES:**	**ROHS COMPLIANCE**				**PACKAGING OPTION¹**
d-pwer Power Management Devices	Digital Power Manager	**04** – 4 devices **08** – 8 devices **16** – 16 devices **32** – 32 devices	**G** - RoHS compliant for all six substances		5-digit identifier assigned by Bel Power Solutions for each unique configuration file		**B1** – 50pcs Tube **R100** – 100pcs T&R

Notes:
¹ Packaging option is used only for ordering and not included in the part number printed on the DPM label.
² The evaluation board is available in only one configuration: DM73XX-KIT-HKS

Example: **DM7316G-12345-R100**: A 100-piece reel of 16-node DPMs with preloaded configuration file code 12345.
Each DPM is labelled DM7316G-12345. Refer to Figure 1 for label marking information.

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Line 1: Part Number

(7 Char. Alpha Numeric)

Line 3: Firmware Rev.

(3 Char. Alpha Numeric)

DM73**xx**G

XXXXX X

XXX

XXXXXXX

Line 2: Customer Config. Number,
Customer Config. Rev.

(5 digits Plus Rev Letter)

Line4: Programming

(Location, Date, Batch Code)
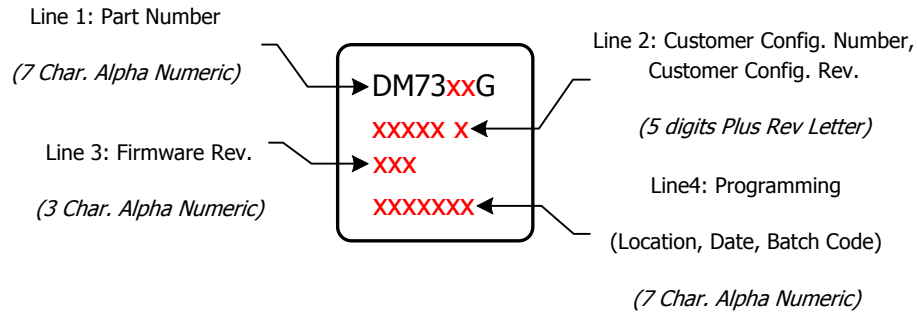
(7 Char. Alpha Numeric)

Figure 22. Label Drawing

Reference Documents

- DP7XXX / DP8XXX Point of Load Regulator Data Sheets
- DM73XX Digital Power Manager. Programming Manual, Revision A09 or later
- Graphical User Interface, Revision 6.3.5 or later
- Programming DM73XX DPMs via JTAG Interface. Application Note
- ZM00056-KIT USB to I²C Adapter Kit. User Manual

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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