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Enabling an Intelligent Planet

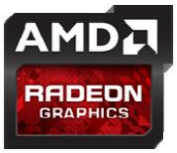
AMD HD5450 1GB PCIEx16

ADVANTECH MODEL: GFX-AH5450L16-3C

MPN NUMBER: 1A1-E000134ADP

Performance PCIe Graphics

1 x DVI-I, 1 x HDMI, 1 x CRT



CONTENTS

1. Specification 3
2. Functional Overview 4
   2.1. Memory Interface 4
   2.2. Memory Aperture Size 4
   2.3. Avivo™ Display System 6
   2.4. DVI/HDMI Features 6
   2.5. DisplayPort Features 6
   2.6. Integrated HD-Audio Controller and Codec 7
   2.7. CRT DAC 8
   2.8. Bus Support Features 8
3. PIN Assignment and Description 9
4. Board configuration 13
   4.1 Board Dimension ..... 錯誤! 尚未定義書籤。
   4.2 Display Interface ..... 錯誤! 尚未定義書籤。
5. Thermal Mechanism 144
   5.1 Fan-Sink Thermal Module 14

1. Specification

Model Name	GFX-AH5450L16-3C
Graphics Engine	AMD Radeon HD 5450
Process Node	40 nm
Engine Clock (max)	650 MHz
Graphics Memory	64-bit, 1 GB DDR3
Memory Clock (max)	500 MHz / 1.0 Gbps
Bus Interface	PCI Express® 2.1 (x16)
Shader Processing Units	80 Shaders
Floating Point Performance	104 GFLOPs
DirectX® Capability	DirectX® 11
Shader Model	Shader Model 5.0
OpenGL™	OpenGL™ 4.1
OpenCL™	OpenCL™ 1.1
Unified Video Decoder (UVD)	UVD3 for H.264, VC-1, MPEG-2 MPEG-4 part 2 decode
Display Interface	1 x DVI-I, 1 x HDMI, 1 x CRT
Multi display	X2
Power Consumption	25 W
Operating Temperature	Base on chassis air flow
Dimension	168 x 69 mm

2. Functional Overview

2.1. Memory Interface

Memory configuration support

AMd Radeon HD 5450 has two DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel, and must run at the same voltage.

Supported DRAM Component Organizations:

- 4, 8, or 16 banks (2-, 3-, or 4-bank bits). Single- or dual-rank.
- Rows: 1024, 2048, 4096, 8192, or 16384 (10, 11, 12, 13, or 14 bits).
- Columns: 256, 512, or 1024
- CS (chip select):1 or 2

2.2. Acceleration Features

Fully DirectX® 11 compliant, including full-speed 32-bit floating point per component operation:

- Shader Model 5.0 geometry and pixel support in a unified-shader architecture:
  - Vertex, pixel, geometry, compute, domain, and hull shaders.
  - 32- and 64-bit floating-point processing per component.
  - High-performance dynamic branching and flow control.
  - Nearly unlimited shader-instruction store, using an advanced caching system.
  - Advanced shader design, with ultra-threading sequencer for high efficiency operations.
  - Advanced, high-performance branching support, including static and dynamic branching.
  - High dynamic-range rendering with floating-point blending, texture filtering and anti-aliasing support.
  - 16- and 32-bit floating-point components for high dynamic-range computations.

- Full anti-aliasing on render surfaces up to and including 128-bit floating-point formats.

- Support for OpenGL 3.2.
- Support for OpenCL™ 1.0.

Anti-Aliasing Filtering:

- 2x/4x modes.
- Multi- and super-sample algorithms with gamma correction, programmable sample patterns, and centroid sampling.
- Custom filter anti-aliasing with up to 12-samples per pixel.
- Adaptive anti-aliasing mode.
- Lossless color compression (up to 8:1) at all resolutions, up to and including wide-screen HDTV.

Anisotropic Filtering:

- 2x/4x/8x/16x modes.
- Up to 128-tap texture filtering.
- Anisotropic biasing to allow trading quality for performance.
- Improved quality mode due to improved sub-pixel precision and higher precision LOD computations.
- Advanced texture compression (3Dc+™).
- High-quality 4:1 compression for normal and luminance maps.
- Angle-invariant algorithm for improved quality.
- Works with any single- or two-channel data format

Hardware support to overcome "small batch" issues in CPU limited applications.

- 3D resources virtualized to a 32-bit addressing space for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel textures are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.

- Lossless z-buffer compression for both z and stencil.

- Fast z-buffer clear.
- Fast color-buffer clear.
- Z cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.3. Avivo™ Display System

The AMD Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on six independent display controllers.

The full features of the AMD Avivo display system are outlined in the following sections.

2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output.
- Supports industry-standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person.
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—162 MP/s (megapixels per second) per link for 30-bpp dual link; double for 24-bpp dual-link
  - HDMI—148.5 MP/s.
- Compliant with the DVI electrical specification.
- The HDMI specification meets the Windows Vista® logo

2.5. DisplayPort 1.2 Features

- Supports all the mandatory features of the *DisplayPort Version 1.1a*

  30-bit support.

  YCbCr 444 up to 30-bpp and 422 up to 20-bpp support.

  HDCP support.

  DisplayPort extension for test-automation features, including test-pattern generation.

  DisplayPort Audio.

- Each DisplayPort link can transport up to six video streams; one from each display engine.
- Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
  - Four, two, or one lane(s).
  - 2.7-, or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution for four lanes at -GHz link rate:
    - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
    - 2560 × 2048 @ 60Hz, 30 bpp is supported.
  - Examples of supported pixel-rate/resolution for two lanes at 2.7-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 179 MP/s for 24 bpp or 143 MP/s for 30 bpp.
    - 1920 × 1200 @ 60Hz, 24 bpp is supported.
  - The following table shows the maximum pixel rates for four, two, or one lane(s) at 2.7-GHz link rate.

	18 bpp	24 bpp	30 bpp
One lane	119 MP/s	89 MP/s	71 MP/s
Two lanes	239 MP/s	179 MP/s	143 MP/s
Four lanes	478 MP/s	359 MP/s	287 MP/s

2.6. Integrated HD-Audio Controller and Codec

The integrated HD-Audio codec supports linear PCM and Dolby Digital (7.1) audio formats for HDMI and DisplayPort outputs.

Note: Player applications may limit audio output capabilities.

- Separate logical-chip function.
- Can encrypt data onto one associated HDMI output.
- Compatible Microsoft® UAA driver support for basic audio.
  - For advanced functionality, a 3rd party driver is required.
- Internally connected to the integrated HDMI interface, hence no external cable is required.
- Supports Dolby True HD, DTS-HD, Dolby Digital (AC3), and DTS.
- LPCM and high-bit rate audio support — up to 24 bits/sample and up to 192-kHz sampling rate.

- Support for up to eight channels.
- HDCP content-protection support for software-audio stack.
- True audio plug-and-play capability for enhanced-audio modes.
- Audio DRM supported.

2.7. CRT DAC

- One integrated triple 10-bit DAC with built-in reference circuit, which takes output from either one of the internal display controllers (primary or secondary).
- A single RGB-CRT output.
- Support for the stereo-sync signal to drive a 3D display.
- A maximum pixel frequency of 400 MHz.
- An individual power-down feature for each of the three guns.
- Compliant with the VSIS electrical specification.
- Integrated with a built-in bandgap reference circuitry.
- A static detection circuitry (S_detect) for hot-plug/unplug capability
- An integrated static monitor-detection circuit

2.8. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 2.1
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

3. PIN Assignment and Description

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	

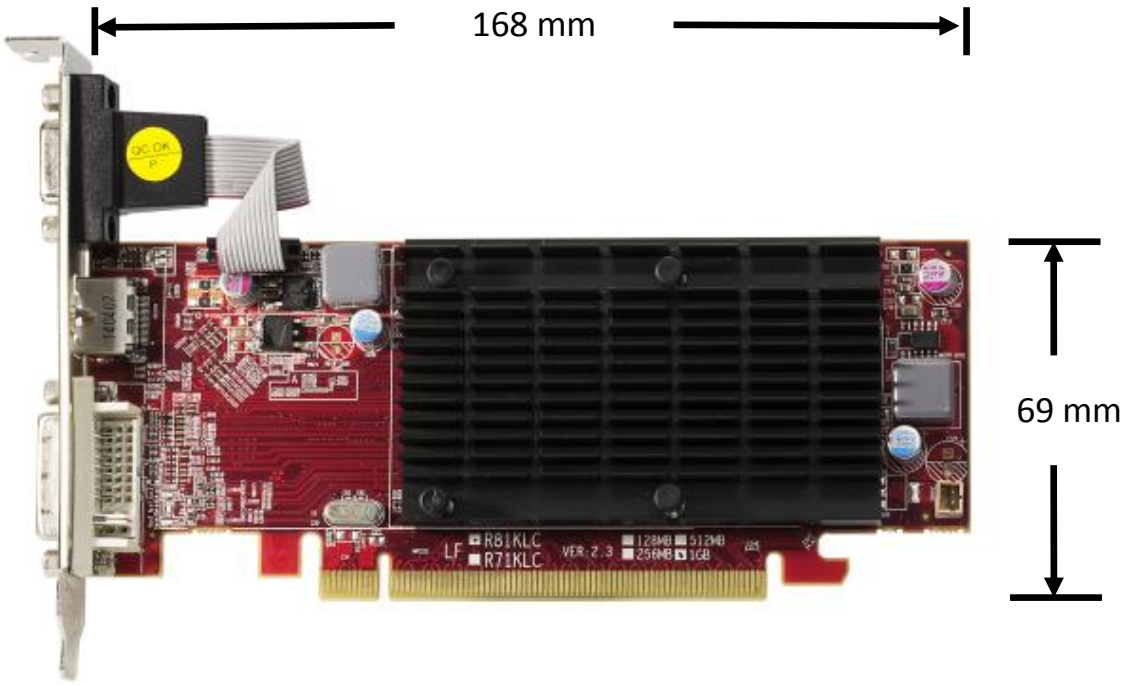
Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground
50	HSOp(8)	Transmitter Lane 8, Differential pair	RSVD	Reserved
51	HSOn(8)		GND	Ground
52	GND	Ground	HSIp(8)	Receiver Lane 8, Differential pair
53	GND	Ground	HSIn(8)	
54	HSOp(9)	Transmitter Lane 9, Differential pair	GND	Ground
55	HSOn(9)		GND	Ground
56	GND	Ground	HSIp(9)	Receiver Lane 9, Differential pair
57	GND	Ground	HSIn(9)	
58	HSOp(10)	Transmitter Lane 10, Differential pair	GND	Ground
59	HSOn(10)		GND	Ground
60	GND	Ground	HSIp(10)	Receiver Lane 10, Differential pair
61	GND	Ground	HSIn(10)	
62	HSOp(11)	Transmitter Lane 11, Differential pair	GND	Ground
63	HSOn(11)		GND	Ground
64	GND	Ground	HSIp(11)	Receiver Lane 11, Differential pair
65	GND	Ground	HSIn(11)	
66	HSOp(12)	Transmitter Lane 12, Differential pair	GND	Ground
67	HSOn(12)		GND	Ground
68	GND	Ground	HSIp(12)	Receiver Lane 12, Differential pair
69	GND	Ground	HSIn(12)	
70	HSOp(13)	Transmitter Lane 13, Differential pair	GND	Ground
71	HSOn(13)		GND	Ground
72	GND	Ground	HSIp(13)	Receiver Lane 13, Differential pair
73	GND	Ground	HSIn(13)	

Pin	Side B Connector		Side A Connector	
#	**Name**	**Description**	**Name**	**Description**
74	HSOp(14)	Transmitter Lane 14, Differential pair	GND	Ground
75	HSOn(14)		GND	Ground
76	GND	Ground	HSIp(14)	Receiver Lane 14, Differential pair
77	GND	Ground	HSIn(14)	
78	HSOp(15)	Transmitter Lane 15, Differential pair	GND	Ground
79	HSOn(15)		GND	Ground
80	GND	Ground	HSIp(15)	Receiver Lane 15, Differential pair
81	PRSNT#2	Hot plug present detect	HSIn(15)	
82	RSVD#2	Hot Plug Detect	GND	Ground

4. Board Configuration

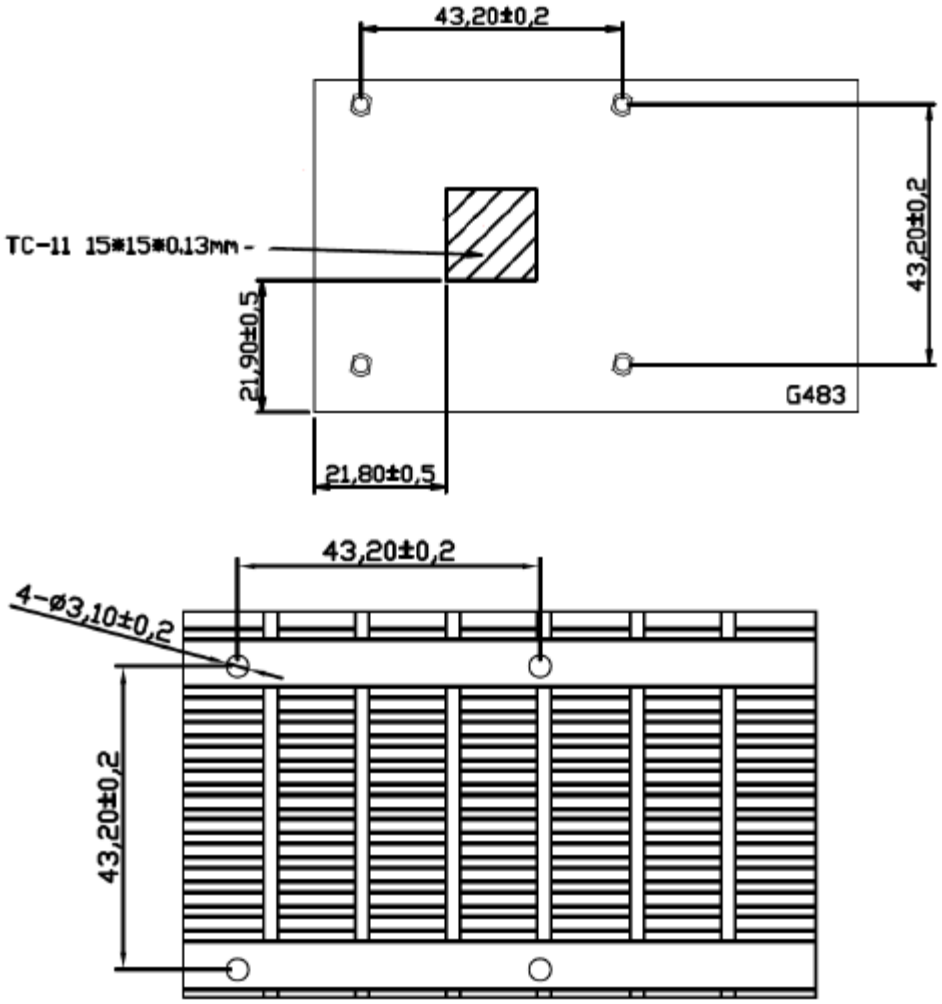
4.1. Board Dimension

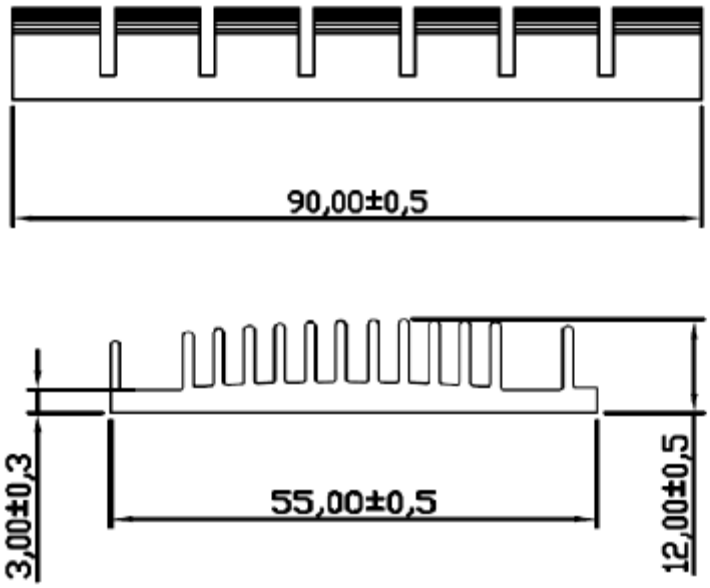


4.2. Display Interface

5. Thermal Mechanism

(Unit : mm)




90,00±0,5
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Change log list

Rev.	Date	Description
2.3	2015/3/27	ER81KLC-LI3ZA datasheet

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