RDIMM DDR4 3200 32GB Datasheet

(SQR-RD4N32G3K2SZAB)

CONTENTS

Revision History

Rev	Date	Modification
1.0	1ST Apr., 2021	Official release

1. Feature

- Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=19	CL=21	CL=22			
PC4-3200	2666	2933	3200	13.75	13.75	45.75

- JEDEC Standard 288-pin Registered Dual In-Line Memory Module
- Intend for PC4-3200 applications
- Inputs and Outputs are SSTL-12 compatible
- Cl-tRCD-tRP: 22-22-22
- VDD=VDDQ= 1.2 Volt(1.14V~1.26V)
- VPP=2.5 Volt (2.375V~2.75V)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18,19, 20,21,22, 24
- Operation temperature Tcase: 0°C~85 °C
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- ECC Function

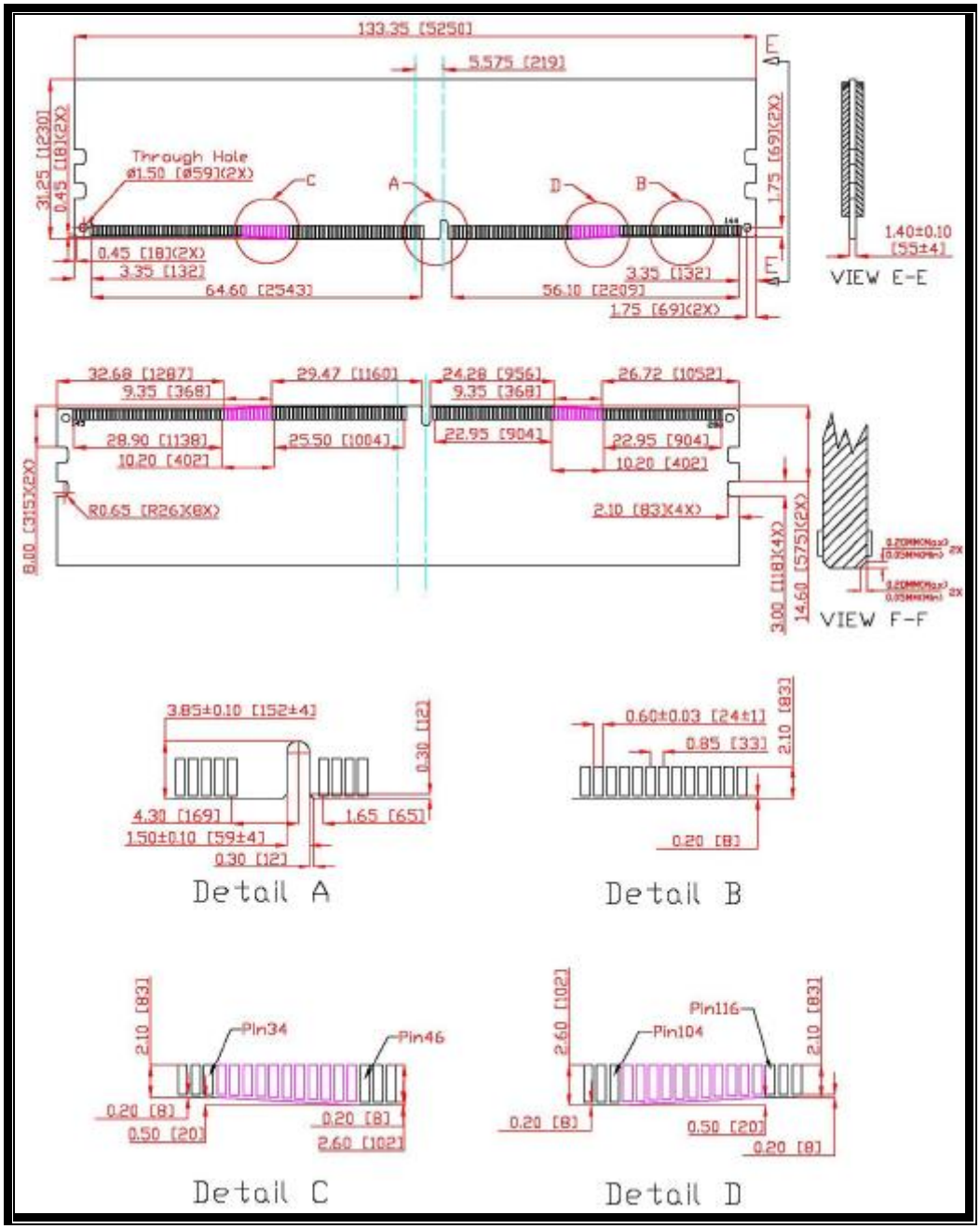
2. Ordering Information

DDR4 RDIMM W/T Sorting						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
SQR-RD4N32G3K2SZAB	32GB	PC4-3200	4Gx72	18	2	Y

Samsung 2Gx8 A-die

3. Dimension

- (32GB, 2Rank 2Gx8 DDR4 base SDRAMs)



Note: All dimensions are in millimeters and should be kept within a tolerance of ±0.15, unless otherwise specified

4. Pin Identification

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD/TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD/TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD/TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1,C2	Chip ID lines for SDRAMs
CS0_n, CS1_n CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t-TDQS17_t TDQS0_c-TDQS17_c	Dummy loads formixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

Note 1 Address A17 is only valid for 16 Gb x4 based SDRAMs.
Note 2 RAS_n is a multiplexed function with A16.
Note 3 CAS_n is a multiplexed function with A15.
Note 4 WE_n is a multiplexed function with A14.

5. Pin Configurations

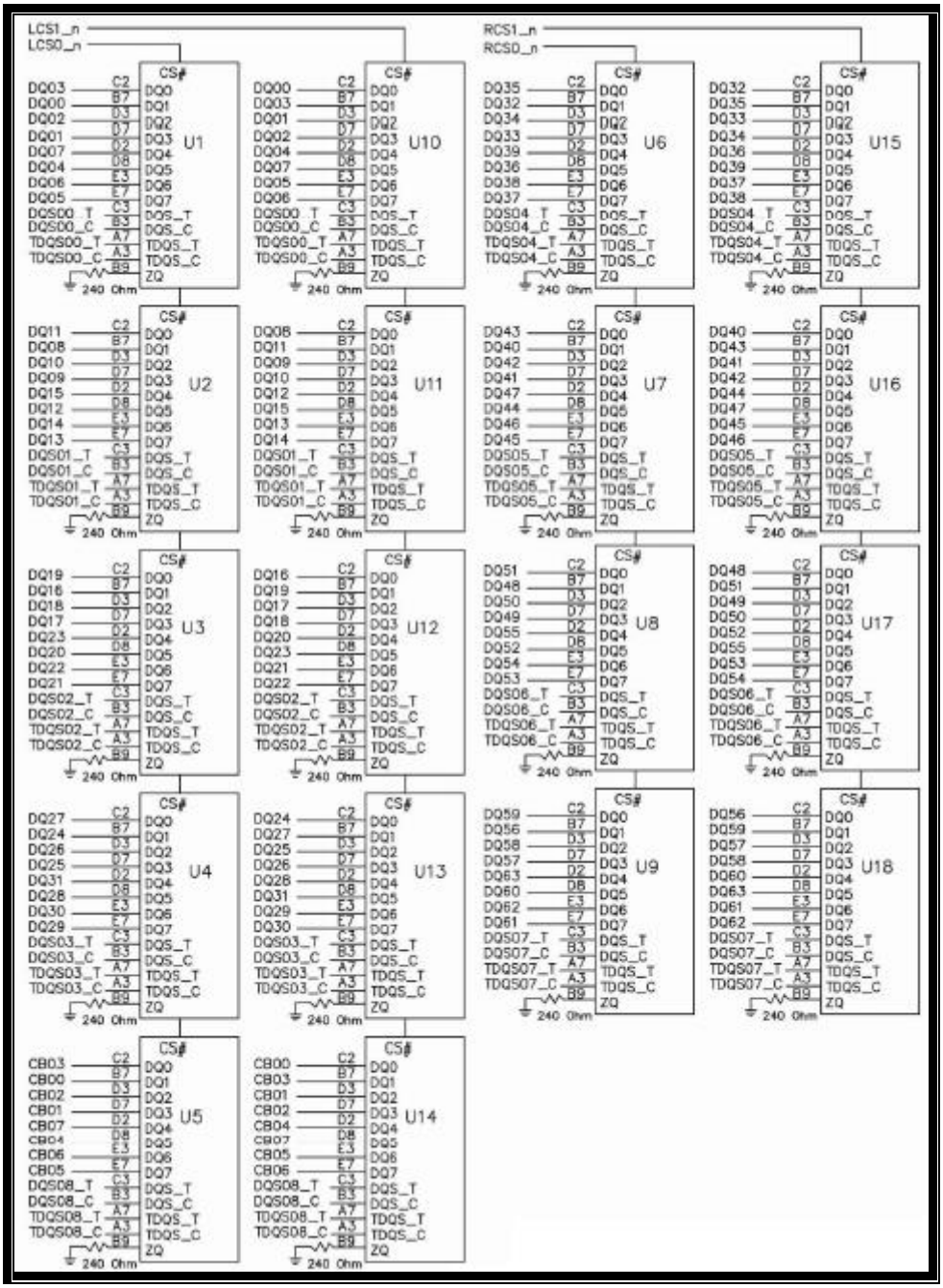
-(DDR4 base RDIMM)

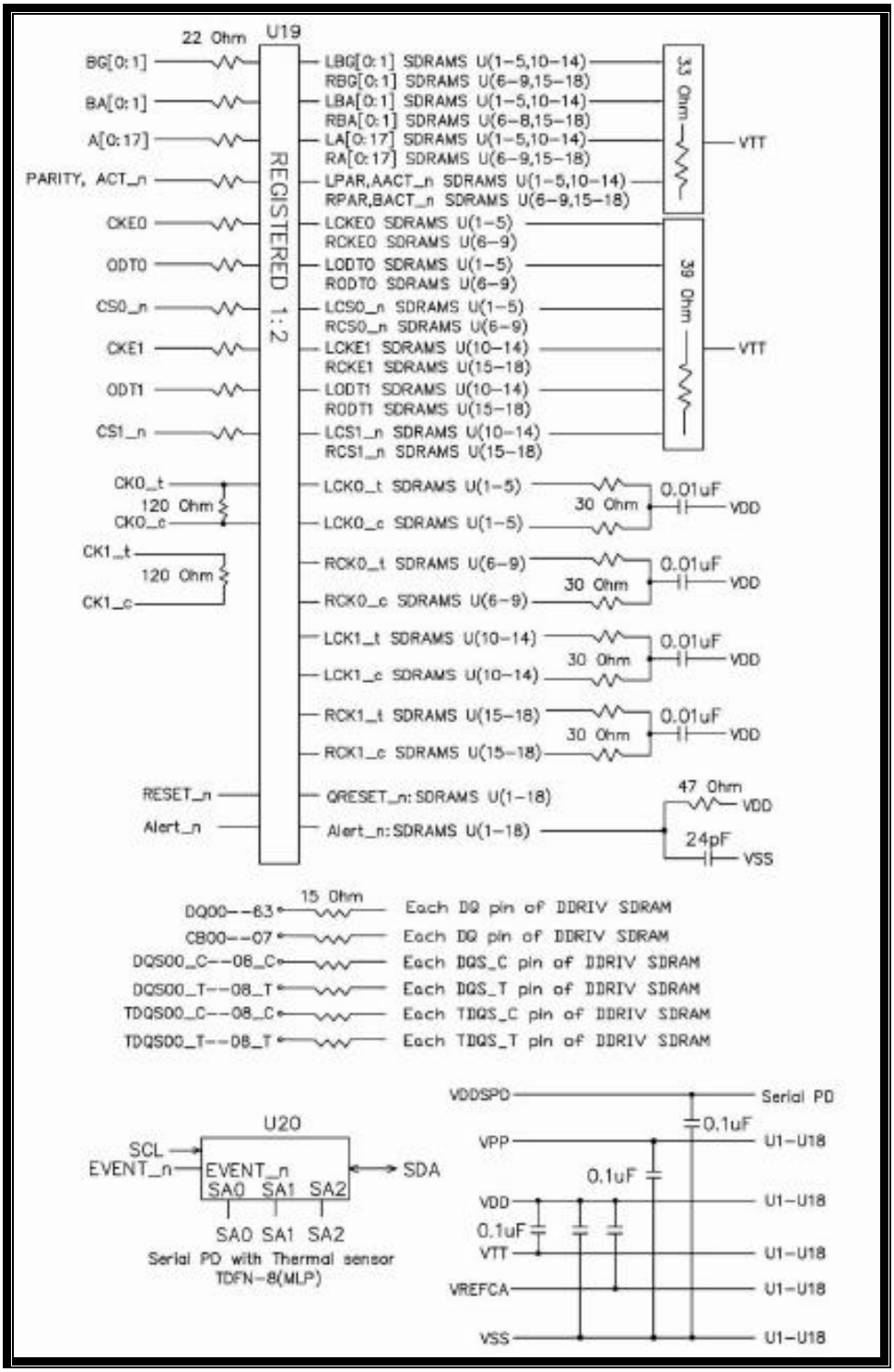
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	37	VSS	181	DQ29	73	VDD	217	VDD	109	VSS	253	DQ41
2	VSS	146	VREFCA	38	DQ24	182	VSS	74	CK0_t	218	CK1_t	110	DQS14_t/ TDQS14_t	254	VSS
3	DQ4	147	VSS	39	VSS	183	DQ25	75	CK0_c	219	CK1_c	111	DQS14_c/ TDQS14_c	255	DQS5_c
4	VSS	148	DQ5	40	DQS12_t/ TDQS12_t	184	VSS	76	VDD	220	VDD	112	VSS	256	DQS5_t
5	DQ0	149	VSS	41	DQS12_c/ TDQS12_c	185	DQS3_c	77	VTT	221	VTT	113	DQ46	257	VSS
6	VSS	150	DQ1	42	VSS	186	DQS3_t	78	EVENT_n	222	PARITY	114	VSS	258	DQ47
7	DQS9_t/ TDQS9_t	151	VSS	43	DQ30	187	VSS	79	A0	223	VDD	115	DQ42	259	VSS
8	DQS09_c/ TDQS9_c	152	DQS0_c	44	VSS	188	DQ31	80	VDD	224	BA1	116	VSS	260	DQ43
9	VSS	153	DQS0_t	45	DQ26	189	VSS	81	BA0	225	A10/AP	117	DQ52	261	VSS
10	DQ6	154	VSS	46	VSS	190	DQ27	82	RAS_n /A16	226	VDD	118	VSS	262	DQ53
11	VSS	155	DQ7	47	CB4	191	VSS	83	VDD	227	RFU	119	DQ48	263	VSS
12	DQ2	156	VSS	48	VSS	192	CB5	84	CS0_n	228	WE_n/ A14	120	VSS	264	DQ49
13	VSS	157	DQ3	49	CB0	193	VSS	85	VDD	229	VDD	121	DQS15_t/ TDQS15_t	265	VSS
14	DQ12	158	VSS	50	VSS	194	CB1	86	CAS_n/ A15	230	NC	122	DQS15_c/ TDQS15_c	266	DQS6_c
15	VSS	159	DQ13	51	TDQS17_t/ TDQS17_t	195	VSS	87	ODT0	231	VDD	123	VSS	267	DQS6_t
16	DQ8	160	VSS	52	DQS17_c/ TDQS17_c	196	DQS8_c	88	VDD	232	A13	124	DQ54	268	VSS
17	VSS	161	DQ9	53	VSS	197	DQS8_t	89	CS1_n	233	VDD	125	VSS	269	DQ55
18	DQS10_t/ TDQS10_t	162	VSS	54	CB6	198	VSS	90	VDD	234	A17	126	DQ50	270	VSS
19	DQS10_c/ TDQS10_c	163	DQS1_c	55	VSS	199	CB7	91	ODT1	235	NC/C2	127	VSS	271	DQ51
20	VSS	164	DQS1_t	56	CB2	200	VSS	92	VDD	236	VDD	128	DQ60	272	VSS
21	DQ14	165	VSS	57	VSS	201	CB3	93	CS2_n/C0,NC	237	CS3_n C1,NC	129	VSS	273	DQ61
22	VSS	166	DQ15	58	RESET_n	202	VSS	94	VSS	238	SA2	130	DQ56	274	VSS
23	DQ10	167	VSS	59	VDD	203	CKE1	95	DQ36	239	VSS	131	VSS	275	DQ57
24	VSS	168	DQ11	60	CKE0	204	VDD	96	VSS	240	DQ37	132	DQS16_t/ TDQS16_t	276	VSS
25	DQ20	169	VSS	61	VDD	205	RFU	97	DQ32	241	VSS	133	DQS16_c /TDQS16_c	277	DQS7_c
26	VSS	170	DQ21	62	ACT_n	206	VDD	98	VSS	242	DQ33	134	VSS	278	DQS7_t
27	DQ16	171	VSS	63	BG0	207	BG1	99	DQS13_t/ TDQ13_t	243	VSS	135	DQ62	279	VSS
28	VSS	172	DQ17	64	VDD	208	ALERT_n	100	DQS13_c/ TDQS13_c	244	DQS4_c	136	VSS	280	DQ63
29	DQS11_t/ TDQS11_t	173	VSS	65	A12/BC_n	209	VDD	101	VSS	245	DQS4_t	137	DQ58	281	VSS
30	DQS11_c/ TDQS11_c	174	DQS2_c	66	A9	210	A11	102	DQ38	246	VSS	138	VSS	282	DQ59
31	VSS	175	DQS2_t	67	VDD	211	A7	103	VSS	247	DQ39	139	SA0	283	VSS
32	DQ22	176	VSS	68	A8	212	VDD	104	DQ34	248	VSS	140	SA1	284	VDDSPD
33	VSS	177	DQ23	69	A6	213	A5	105	VSS	249	DQ35	141	SCL	285	SDA
34	DQ18	178	VSS	70	VDD	214	A4	106	DQ44	250	VSS	142	VPP	286	VPP
35	VSS	179	DQ19	71	A3	215	VDD	107	VSS	251	DQ45	143	VPP	287	VPP
36	DQ28	180	VSS	72	A1	216	A2	108	DQ40	252	VSS	144	RFU	288	VPP

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

6. Block Diagram

- (32GB, 2 rank 1Gx8 DDR4 SDRAMs)





Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

7. Parameter & Operating Conditions

Environmental Requirements

DDR4 RDIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +85	℃	3
TSTG	Storage Temperature	-50 to +100	℃	1
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Note 2 Up to 9850 ft.
Note 3 The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR4 DRAM component specification, JESD79-4.
Follow JEDEC spec.

SDRAM Parameters by device density

RTT_Nom Setting	Parameter		16Gb	Units
tREFI	Average periodic refresh interval	0°C≦ TCASE≦ 85°C	7.8	µs
		85°C<TCASE≦ 95°C	3.9	µs

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDD	Supply Voltage	1.14	1.2	1.26	V	1
VPP	DRAM activating power supply	2.375	2.5	2.75	V	2
VREFCA(DC)	Input reference voltage command/ address bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
VTT	Termination Voltage	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

Operating, Standby, and Refresh Currents

- 32GB RDIMM (2rank 1Gx8 DDR4 SDRAMs)

Symbol	Proposed Conditions	IDD Max.	IPP Max.	Units
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	846	72	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	918	72	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	936	72	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	990	72	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	540	54	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	540	54	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	558	54	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	450	54	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	522	54	mA

IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	486	54	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	558	54	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	396	54	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	504	54	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	738	72	mA
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	756	72	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	558	72	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2304	72	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	2484	72	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	2394	72	mA

IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	2016	72	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	2160	72	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	1998	72	mA
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	1854	72	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	2250	72	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	6210	540	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	4590	414	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	3690	396	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	774	108	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	1206	162	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	558	90	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	774	108	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	3456	252	mA
IDD8	Maximum Power Down Current TBD	396	54	mA

10. Timing Parameters

Clock Timing				
Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.625	<0.682	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-32	32	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-16	16	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-25	25	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	62		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	50		ps
Cumulative error across 2 cycles	tERR(2per)	-46	46	ps
Cumulative error across 3 cycles	tERR(3per)	-55	55	ps
Cumulative error across 4 cycles	tERR(4per)	-61	61	ps
Cumulative error across 5 cycles	tERR(5per)	-65	65	ps
Cumulative error across 6 cycles	tERR(6per)	-69	69	ps
Cumulative error across 7 cycles	tERR(7per)	-73	73	ps
Cumulative error across 8 cycles	tERR(8per)	-76	76	ps
Cumulative error across 9 cycles	tERR(9per)	-78	78	ps
Cumulative error across 10 cycles	tERR(10per)	-80	80	ps
Cumulative error across 11 cycles	tERR(11per)	-83	83	ps
Cumulative error across 12 cycles	tERR(12per)	-84	84	ps
Cumulative error across 13 cycles	tERR(13per)	-86	86	ps
Cumulative error across 14 cycles	tERR(14per)	-87	87	ps
Cumulative error across 15 cycles	tERR(15per)	-89	89	ps
Cumulative error across 16 cycles	tERR(16per)	-90	90	ps
Cumulative error across 17 cycles	tERR(17per)	-92	92	ps
Cumulative error across 18 cycles	tERR(18per)	-93	93	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	40	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	130	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) /	tIH(base)	65	-	ps

Vil(dc) levels				
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	130	-	ps
Control and Address Input pulse width for each input	tIPW	340	-	ps
Command and Address Timing				
Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/ 2K)	Max(4nCK,2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,10ns)	-	ns
Delay from start of internal write transaction to internal read com-mand for different bank group	tWTR_S	max(2nCK,2.5ns)	-	
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	1024	-	nCK

Mode Register Set command cycle time	tMRD	8	-	nCK
Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	UI
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	max(3 nCK, 3.748 ns)	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.20	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	0.70	-	tCK(avg) /2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.64	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device's out-put	tDVWp	0.72	-	UI
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-250	160	Ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	160	ps
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9		tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-250	160	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	160	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK

DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-160	160	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		260	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				
Exit Reset from CKE HIGH to a valid command	command tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+1 0ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands	tXP	(4nCK,6ns)	-	

not requiring a locked DLL				
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,1 0ns)		
Mode Register Set command up-date delay in PDA mode	tMOD_PDA	tMOD		
ODT Timing				
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.26	0.74	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE		2	ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when	tPAR_ALER T_PW	96	192	nCK

asserted				
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	85	nCK
Parity Latency	PL	6		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns
	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	550	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	350	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	260	-	ns

11. Serial Presence Detect

Byte	Description	Function Supported	Hex Value
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	512B Total, 384B Used	23
1	SPD Revision	Ver 1.2	12
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	RDIMM	01
4	SDRAM Density and Banks	16Gb, 4BG&4Banks	86
5	SDRAM Addressing	Row : 17, Column :10	29
6	SDRAM Device Type	Monolithinc Device	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Option	Reserved	00
9	Other SDRAM Optional Features	sPPR supported	60
10	Reserved	Reserved	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	2Rx8	09
13	Module Memory Bus Width	64bit,ECC	0B
14	Module Thermal Sensor	With TS	80
15~16	Reserved	Reserved	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM Minimum Cycle Time(tckavg min)	0.625ns	05
19	SDRAM Minimum Cycle Time(tckavg max)	1.6ns	0D
20	Cas Latency Supported, First Byte	10,11,12,13,14,15,16,17,18,19,20,21,22,24	F8
21	Cas Latency Supported, Second Byte	10,11,12,13,14,15,16,17,18,19,20,21,22,24	FF
22	Cas Latency Supported, Third Byte	10,11,12,13,14,15,16,17,18,19,20,21,22,24	02
23	Cas Latency Supported, Fourth Byte	10,11,12,13,14,15,16,17,18,19,20,21,22,24	00
24	Minimum Cas Latency Time (tAAmin)	13.75ns	6E
25	Minimum RAS to CAS Delay Time(tRCD min)	13.75ns	6E
26	Minimum Raw Precharge Delay Time(tRP min)	13.75ns	6E
27	Upper Nibbles for tRASmin and tRCmin	tRAS=32ns, tRC=45.75ns	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	tRAS=32ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	tRC=45.75ns	6E
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	550ns	30
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	550ns	11
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	350ns	F0
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	350ns	0A

34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	260ns	20
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	260ns	08
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	13ns	00
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	21ns	A8
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	2.5ns	14
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	4.9ns	28
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	28
41	Upper Nibble for tWRmin	15ns	00
42	Minimum Write Recovery Time(tWRmin)	15ns	78
43	Upper Nibbles for tWTRmin	2.5ns	00
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3C
46~59	Reserved	Reserved	00
60	Connector to SDRAM Bit Mapping		0C
61	Connector to SDRAM Bit Mapping		2C
62	Connector to SDRAM Bit Mapping		0C
63	Connector to SDRAM Bit Mapping		2C
64	Connector to SDRAM Bit Mapping		0C
65	Connector to SDRAM Bit Mapping		2C
66	Connector to SDRAM Bit Mapping		0C
67	Connector to SDRAM Bit Mapping		2C
68	Connector to SDRAM Bit Mapping		0C
69	Connector to SDRAM Bit Mapping		2C
70	Connector to SDRAM Bit Mapping		0C
71	Connector to SDRAM Bit Mapping		2C
72	Connector to SDRAM Bit Mapping		0C
73	Connector to SDRAM Bit Mapping		2C
74	Connector to SDRAM Bit Mapping		0C
75	Connector to SDRAM Bit Mapping		2C
76	Connector to SDRAM Bit Mapping		0C
77	Connector to SDRAM Bit Mapping		2C
78~116	Reserved	Reserved	00
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	00
118	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group	4.9ns	9C
119	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group	3.0ns	00
120	Fine Offset for Minimum Activate to Acticate/Refresh Delay	45.75ns	00

	Time(tRCmin)		
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	13.75ns	00
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	13.75ns	00
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	13.75ns	00
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	1.6ns	E7
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	0.750ns	00
126	Cyclical Redundancy Code	-	25
127	Cyclical Redundancy Code	-	23
128	Raw Card Extension, Module Nominal Height	31 < height<= 32 mm	11
129	Module Maximum Thickness		11
130	Reference Raw Card Used	R/C E REV 3	64
131	DIMM Module Attributes	RCD02 1row 1register	15
132	RDIMM Thermal Heat Spreader Solution	W/O H/S	00
133	Register Manufacturer ID Code, Least Signficant Byte		86
134	Register Manufacturer ID Code, Most Signficant Byte		9D
135	Register Revision Number		22
136	Address Mapping from Register to DRAM		01
137	Register Ouput Drive Strength for Control		10
138	Register Output Strength for CK		40
139~253	Reserved	Reserved	00
254	Cyclical Redundancy Code	-	D3
255	Cyclical Redundancy Code	-	DD
256~319	Reserved	Reserved	00
320	Module Manufacturer's ID Code, Least Significant Byte	Advantech	8A
321	Module Manufacturer's ID Code, Most Significant Byte	Advantech	C8
322	Module Manufactoring Location	-	00
323	Module Manufactoring Date	Year	-
324	Module Manufactoring Date	Week	-
325~328	Module Serial Number	-	-
329~348	Module Part Number	SQR-RD4N32G3K2SZAB	53 51 52 2D 52 44 34 4E 33 32 47 33 4B 32 53 5A 41 42 20 20
349	Module Revision Code	-	00
350	DRAM Manufacturer's ID Code, Least Sgnificant Byte	Samsung	80
351	DRAM Manufacturer's ID Code, Most Sgnificant Byte	Samsung	CE
352	DRAM Stepping	Ver 0.0	00
353~380	Module Manufacturer's Specific Data	Reserved	-
381	Module Manufacturer's Specific Data	Reserved	-
382~383	Reserved	Reserved	00
384~511	End User Programmable	Reserved	00

12. Appendix: Part Number Table

Product	Advantech PN
SQRAM 32GB RDIMM-DDR4-3200 2Gx8 SAM	SQR-RD4N32G3K2SZAB

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

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