microSDSC and microSDHC Card

USD410M

Datasheet

Products	Product Description
TS32GUSDC410M	2GB microSD, MLC
TS16GUSD410M	4-32GB microSD UHS-I U1 A1, MLC
TS8GUSD410M	
TS4GUSD410M	**Datasheet version**
TS2GUSD410M	2.1

No.70, Xingzhong Rd., NeihuDist.,Taipei City 114, Taiwan, R.O.C.
Tel:+886-2-2792-8000 Fax:+886-2-2792-1614 www.transcend-info.com

Revision History

Revision No.	History	Released Date	Editor by
2.0	First version (SAMSUNG 14nm)	2021/07/14	TSD
2.1	Added New Item TS32GUSD410M Updated TS32GUSD410M Photo Added UKCA Compliance	2021/08/16	TSD

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Transcend USD410M Features

Part Name	Capacity
TS32GUSD410M	32GB
TS16GUSD410M	16GB
TS8GUSD410M	8GB
TS4GUSD410M	4GB
TS2GUSD410M	2GB

FEATURES

- 2D MLC NAND Flash
- Compatible with SD specification up to Ver.5.1
- Compatible with UHS-I speed
- Video Speed up to Class V10
- Application Performance up to Class 1(A1)
- Global wear-leveling function
- Early Move function
- Read Retry function
- Supports SPI Mode
- Power Loss Protection function
- Supports Password Protection and Secure Erase
- BCH ECC(Error Correction Code) function
- Supports ESD IEC 61000-4-2
- Supports IPX7 IEC 60529 Edition 2.2

PERFORMANCE[1)]

- Data Transfer Rate
  - Sequential Read Up to 95 MB/s
  - Sequential Write Up to 50 MB/s

RELIABILITY[1)]

- TBW
  - 32GB 86TB
  - 16GB 43TB
  - 8GB 21TB
  - 4GB 10TB
  - 2GB 5TB
- DWPD Up to 2.51 DWPD
- MTBF >3,000,000 hours
- Data Retention 1 year[2)]
- Warranty 3 years

ENVIRONMENTAL SPECIFICATIONS[1)]

- Temperature
  - Operating -25°C to 85°C
  - Non-operating -40°C to 85°C
- Humidity(non-condensing) 0%~95%
- Shock[2)] Refer [Table 13]
- Vibration[2)] 2G, 10~2000Hz
- Drop[2)] 1.5m free fall
- Durability(Plug Test)[2)] 10,000 Cycles
- Bending(Middle Point)[2)] 10N for 60s
- Torque(Max Angle ±2.5°)[2)] 0.15Nm for 30s

POWER REQUIREMENTS[1)]

- Supply voltage / Tolerance 2.7V to 3.6V
- Active (max) 2.88W
- Idle (max) 1.8mW

PHYSICAL DIMENSION

- Width 11.00±0.1mm
- Length 15.00±0.1mm
- Height(max) 0.7±0.1mm
- Weight Up to 2g

Note:
1) All tests are handled by TRANSCEND, the results are affected by different system operations and environments. Data is for reference only.
2) For detail information, please refer TRANSCEND Qualification Report

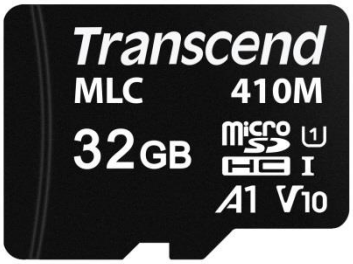
Table of Content

1.Introduction

1.1 General Feature Information

Hardware Feature

- 2D MLC NAND Flash
- Controller SM2705EN
- Compatible with SD specification up to Ver. 5.1
- Compatible with UHS-I speed
- Video speed up to Class V10
- Application performance up to Class1(A1)
- ESD IEC 61000-4-2
- RS IEC 61000-4-3
- PFM IEC 61000-4-8
- IPX7 IEC 60529 Edition 2.2



TS32GUSD410M

Firmware Feature

- Global wear-leveling function
- Early Move function
- Read Retry function
- Supports SPI Mode
- Power Loss Protection function
- Password Protection and Secure Erase function
- BCH ECC(Error Correction Code) function

Software Feature

- Transcend Scope Pro

1.2 Product List

Form Factor	Part Name	Capacity
microSDSC and microSDHC	TS32GUSD410M	32GB
	TS16GUSD410M	16GB
	TS8GUSD410M	8GB
	TS4GUSD410M	4GB
	TS2GUSD410M	2GB

1.3 Ordering Information

T S	**X X X**	**G**	**U S D**	**4 1 0 M**
1	2	3	4	5

1 – Transcend

2 – SD Density

3 – G: Gigabyte; T: Terabyte

4 – microSD Card

5 – Product series with 2D MLC NAND Flash

2. Product Specifications

2.1 Interface and Compliance

- Compatible with SD specification up to Ver. 5.1
- Compatible with UHS-I speed
- RoHS Compliance
- CE, UKCA, FCC and BSMI Compliance

2.2 Capacity

[Table 1] Usable Bytes

	2GB	4GB	8GB
Usable Bytes	2,007,629,824	3,923,771,392	7,808,745,472

	16GB	32GB
Usable Bytes	15,453,913,088	30,912,020,480

Note:

1) Usable Bytes: Total free space which could be used by user. (Actual usage space will vary according to different usage environments)

2.3 Data Transfer

[Table 2] Data Transfer Specification

	2GB	4GB	8GB	16GB	32GB
SD Specification	SD3.0	SD5.1			
SD Type	SDSC	SDHC	SDHC	SDHC	SDHC
Interface	High Speed	UHS-I SDR 104			
Speed Class[1)]	N/A	V10/U1	V10/U1	V10/U1	V10/U1
Application Performance Class[2)]	N/A	A1	A1	A1	A1

Note:

1) All parameters are determined by Testmetrix VTE4100. Only shows the fastest transferring bus mode

2) Enable users to run their smartphone apps from the installed memory card.

2.4 System Performance

[Table 3] Sequential Read / Write Performance

Read / Write	2GB	4GB	8GB	16GB	32GB
Sequential Read	24 MB/s	95 MB/s	95 MB/s	95 MB/s	95 MB/s
Sequential Write	8 MB/s	12 MB/s	20 MB/s	30 MB/s	50 MB/s

Note: Maximum transfer speed recorded

1) 25°C, test on 4GB DRAM, Windows® 10 with Transcend RDF5, benchmark utility Crystal Disk Mark , copied file 1GB, unit MB/s

[Table 4] Random Read / Write Performance

Read / Write	2GB	4GB	8GB	16GB	32GB
Random Read IOPS (4KB QD32)	1800	3500	3800	3500	3500
Random Write IOPS (4KB QD32)	400	700	800	900	1200

Note: Maximum transfer speed recorded

1) 25°C, test on 4GB DRAM, Windows® 10 , with Transcend RDF5, benchmark IO Meter 2008 , copied 4GB size ,unit IOPS

2.5 Supply Voltage

2.5.1 DC Characteristics

[Table 5] Supply Voltage

Parameter/Condition	Requirements
V_{DD} Supply Voltage	2.7V to 3.6V

[Table 6] Recommended Operating Conditions

Parameter/Condition	Symbol	Min(V)	Type(V)	Max(V)
Supply Voltage	V_{DD}	2.7	3.3	3.6
Regulator Supply Voltage for 1.8V Signaling	V_{DDIO}	1.7	1.8	1.95
Ground Supply Voltage	V_{SS}	0	0	0

[Table 7] DC Voltage Characteristics for 3.3V Signaling

Parameter	Symbol	Min(V)	Max(V)	Note
Input Low Voltage	V_{IL}	V_{SS}- 0.3	0.25x V_{DD}	-
Input High Voltage	V_{IH}	0.625x V_{DD}	V_{DD}+ 0.3	-
Output Low Voltage	V_{OL}	-	0.125x V_{DD}	I_{OL} = 2 mA@ V_{DD} (Min)
Output High Voltage	V_{OH}	0.75x V_{DD}	-	I_{OH} = -2 mA@ V_{DD} (Min)

[Table 8] DC Voltage Characteristics for 1.8V Signaling

Parameter	Symbol	Min(V)	Max(V)	Note
Input Low Voltage	V_{IL}	V_{SS}- 0.3	0.58	-
Input High Voltage	V_{IH}	1.27	2	-
Output Low Voltage	V_{OL}	-	0.45	I_{OL} = 2 mA@ V_{DD} (Min)
Output High Voltage	V_{OH}	1.4	-	I_{OH} = -2 mA@ V_{DD} (Min)

2.5.2 AC Characteristics

Timing specifications including clock timing, input and output timings for all bus modes are defined in SDA. Refer to Section 6.6 and 6.7 of Part1, Physical Layer Specification, Version 6.0 for detail information.

2.6 System Power Consumption

[Table 9] Power Consumption

Bus Mode	Read / Write	Power Consumption
Default Mode (25MHz)	Active Write (Max.)[1)]	0.36W
	Active Read (Max.)[1)]	0.36W
	Idle	1.8mW
High Speed mode (50MHz)	Active Write (Max.)[1)]	0.72W
	Active Read (Max.)[1)]	0.72W
	Idle	1.8mW
UHS-I SDR50 mode (100MHz)	Active Write (Max.)[1)]	1.44W
	Active Read (Max.)[1)]	1.44W
	Idle	1.8mW
UHS-I DDR50 mode (50MHz)	Active Write (Max.)[1)]	1.44W
	Active Read (Max.)[1)]	1.44W
	Idle	1.8mW
UHS-I SDR104 mode (208MHz)	Active Write (Max.)[1)]	2.88W
	Active Read (Max.)[1)]	2.88W
	Idle	1.8mW

Note:

1) Power consumption is referred to Section 6.6.3 of the SDA Physical Layer Specification, Version 5.1

2.7 Electrostatic Discharge(ESD)

[Table 10] Contacts Discharge to Pads

Condition	Test Procedure	Note
Human Body Model	Up to ±4KV	Refer IEC60749-26(JESD22-A114-D)

[Table 11] Non-Contacts Discharge to Pads Area

Condition	Test Procedure	Note
Air Discharge	Up to ±8KV	Refer IEC61000-4-22(CE Certification)

2.8 Water Resistance

[Table 12] International Protection Marking

IP Level	Test Procedure	Note
IPX7	The lowest point of enclosures with a height less than 850mm is located 1000mm below the surface of water for 30mins	Refer IEC60529 Edition2.2

Note:

1) The sample should be dried before use.

2.9 Environment Specifications

[Table 13] Environment Specification

Features	Operating[1)]	Non-Operating[2)]
Temperature	-25°C to +85°C	-40°C to 85°C
Temperature Gradient	60°C/Hr	60°C/Hr
Humidity	0% to 95%, non-condensing	
Shock	Acceleration: 50G(490 m/s^2) Semi-Sine Wave, velocity change: 3.44$m/s^{3)5)}$	
Vibration	2G, 10~2000Hz, 3 axis, 10 cycles/5 mins[4)5)]	
Drop	1.5m, free fall[5)]	
Durability	10,000 cycles plug test[5)]	
Bending	10N for 60 sec and 3 times test[5)]	
Torque	0.15Nm for 30 sec[5)]	

Note:

1) The operating specification is regarded as Ambient Temperature. Standard grade (-25°C to +85°C) and Industrial grade (-40°C to +85°C) indicate the temperature conditions for testing devices on programmable temperature and humidity chamber room.

2) The non-operating specification is regarded as storage specification.

3) Refer IEC 60512-6-3 standard.

4) Refer IEC 60512-6-4 standard.

5) The results are affected by different system operations and environments. Data is for reference only. For detail information, please refer TRANSCEND Qualification Report.

2.10 System Reliability

[Table 14] TelcordiaSR332 issue 4 MTBF Specifications

Parameter	2GB	4GB	8GB	16GB	32GB
MTBF	>3,000,000 hours				

Note:

1) The calculation is based on 25°C.

[Table 15] TBW (Terabytes Written) Specifications

Parameter	2GB	4GB	8GB	16GB	32GB
TBW	5 TB	10 TB	21 TB	43 TB	86 TB

Note:

1) TBW is based on Transcend internal standard to calculate how much data can be written in to SD card. Actual Value may depend on different application.

2) TBW calculation is referred by JSD219A formula.

[Table 16] Drive Write Per Day (DWPD) Specifications

Parameter	2GB	4GB	8GB	16GB	32GB
DWPD[1)]	2.34 (3 Years)		2.46 (3 Years)	2.51 (3 Years)	

Note:

1) DWPD is based on [Table 19] Warranty year to calculate.

[Table 17] Data Retention Specifications

Parameter	2GB	4GB	8GB	16GB	32GB
Data Retention	1 year				

Note:

1) Data retention was measured by assuming that SD reaches the maximum rated endurance at 30°C under power-off state.

2) The data retention is defined in JESD47 Requirements for standard classes of SDs.

[Table 18] Power Scheme

Parameter	2GB	4GB	8GB	16GB	32GB
Power Scheme	Refer Section 8(Power Scheme)				

[Table 19] Warranty

Parameter	2GB	4GB	8GB	16GB	32GB
Warranty	3 years limited				

[Table 20] Regulations

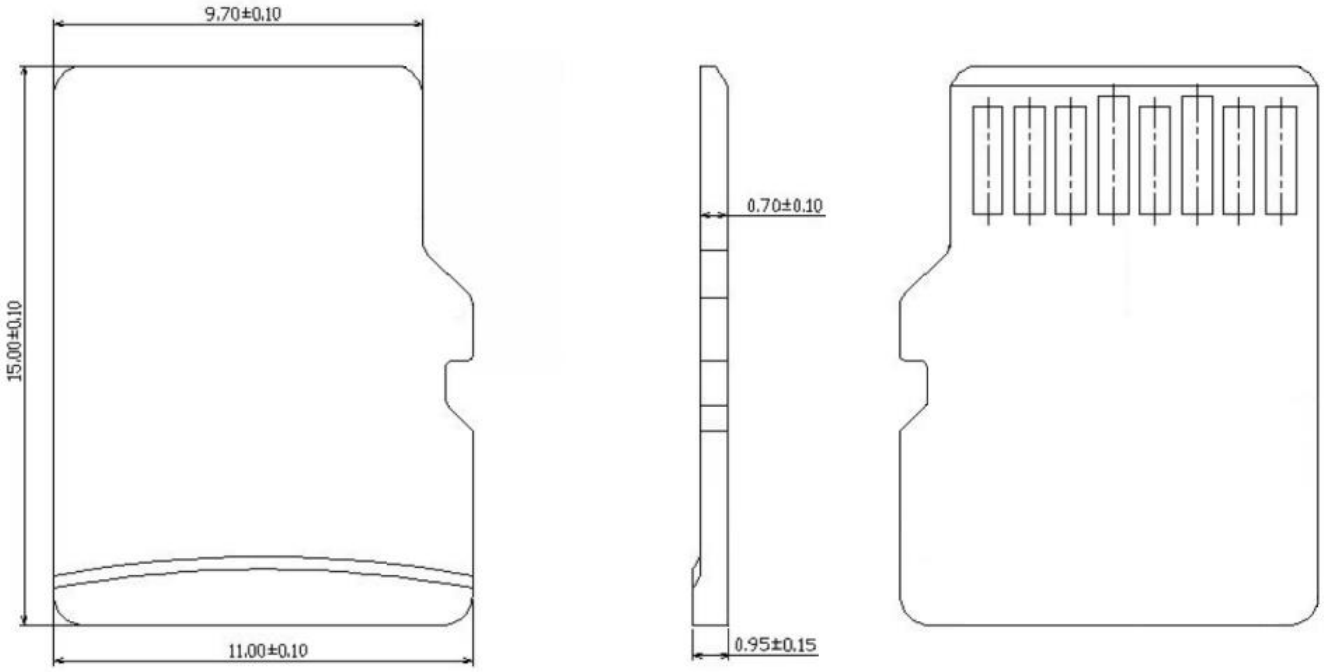
Parameter	2GB	4GB	8GB	16GB	32GB
Compliance	CE, UKCA, FCC and BSMI				

3. Mechanical Specification

The figure below illustrates the Transcend microSD cards.
(Refer SD card Mechanical Addendum)

[Table 21] Physical Dimensions and Weight

Model	Height (mm)	Width (mm)	Length (mm)	Weight (gram)
2GB/4GB/8GB/16GB/32GB	0.70±0.1	15.00±0.1	11.00±0.1	Up to 2g



4. Pin Assignments

4.1 Pin Assignments

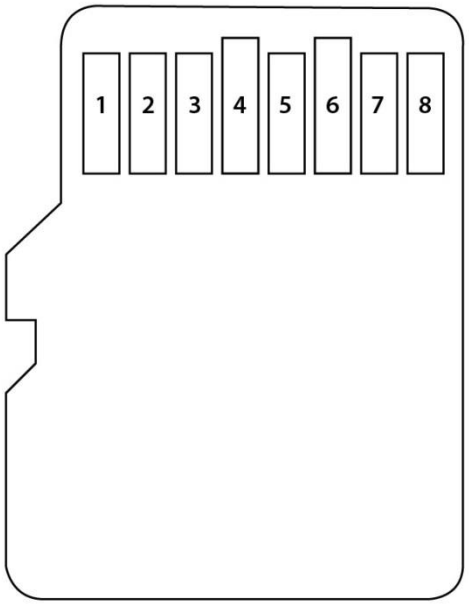
[Table 22] Pin Assignments

Mode	SD Mode			SPI Mode		
Pin No.	**Name**	**IO Type**	**Description**	**Name**	**IO Type**	**Description**
01	DAT2	I/O/PP	Data Line [Bit2]	RSV	-	Reserved
02	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit3]	CS	I	Chip Select
03	CMD	PP	Command / Response	DI	I	Data In
04	V_{DD}	S	Supply voltage	VDD	S	Supply Voltage
05	CLK	I	Clock	SCLK	I	Clock
06	V_{SS}	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
07	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data out
08	DAT1	I/O/PP	Data Line [Bit1]	RSV	-	Reserved

Note:

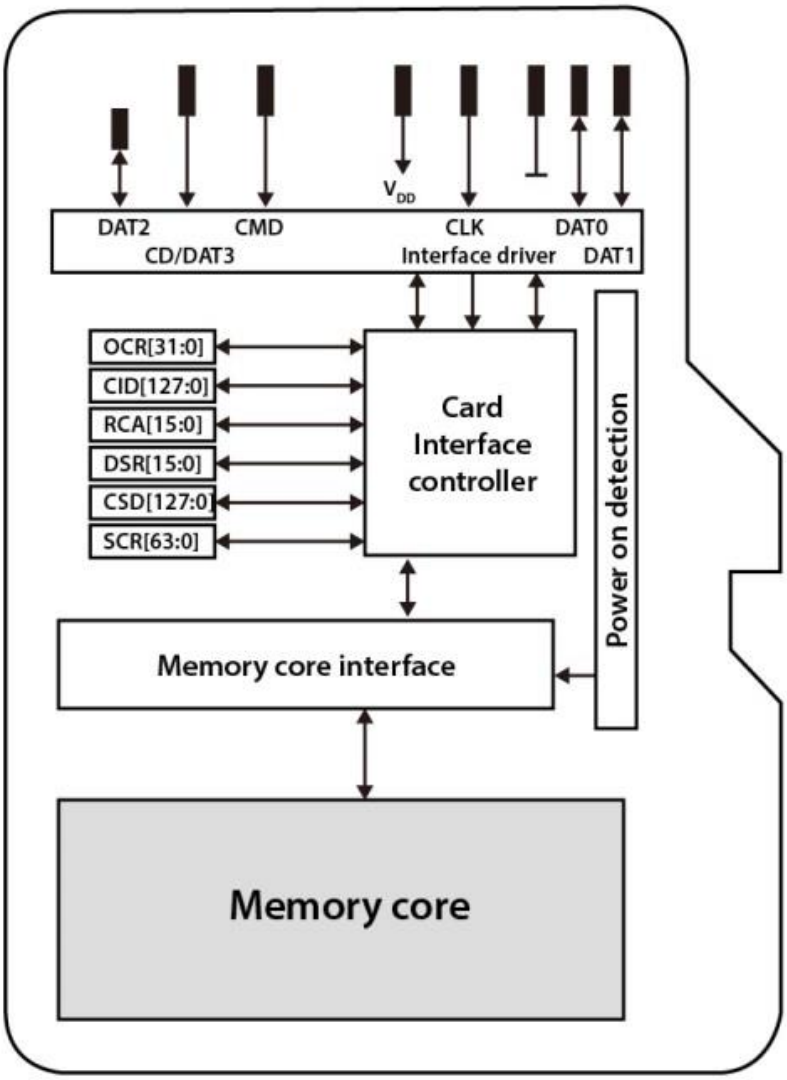
1) S: Power Supply, I: Input, O: Output, I/O: Bi-Directional, PP: IO Using Push-Pull Drivers

2) CMD and DAT pins should be pulled up by the host side with 10-100K Ohm resistance.



5. Block Diagram and Function Explanations

5.1 Block Diagram



5.2 Function Explanations

5.2.1 Global Wear Leveling Function

Global wear leveling ensures that every block has an even erase count. This helps to extend the life expectancy of an SD.

There are three main processes in global wear leveling:

(1) Record the block erase count and save this in the wear-leveling table.

(2) Find the static-block and save this in the wear-leveling pointer.

(3) Check the erase count when a block is pulled from the pool of spare blocks. If the block erase count is larger than WEARCNT, then swap the static-block and the over-count-block.

5.2.2 Early Move Function

Transcend SD/microSD cards enhance data reliability with error-correction code (ECC) written into the firmware. In addition, Transcend SD/microSD cards set the first threshold that monitors data correctness based on the amount of error bits that must be less than maximum ability of the ECC. If error bits showing error within a block reach the threshold, the data will be moved to a good block and the original block erased. In this way, we may ensure data can always be protected by ECC engine.

5.2.3 Read Retry Function

During read operations, the voltage is monitored. In the event of charge loss, cells being disturbed, or read/write cycling, bit errors can occur, causing read errors. To improve error correction, Transcend SD/microSD cards feature read-retry function in the firmware algorithm, which adjusts the read reference voltage to decrease or eliminate read errors.

5.2.4 Built in BHC ECC Engine

In event of errors, the combined data allow the recovery of the original data. The number of errors that can be recovered depends on the algorithm used. With powerful BHC ECC engine, SD card can provide high reliable quality

5.2.5 Bus Topology

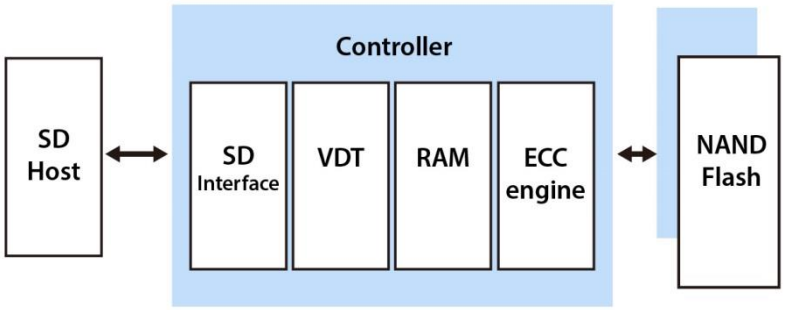
The SD Memory Card system defines two alternative communication protocols:SD and SPI. The host system can choose either one of modes. The card detects which mode is request by host when the reset command is received and expects all further communication to be in the same communication mode.

SD Bus: For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 6.0.

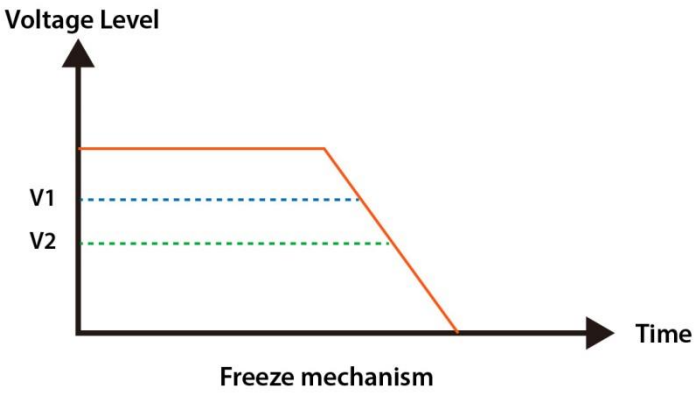
SPI Bus: For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 6.0.

5.2.6 Power Loss Protection Function

Power Loss Protection Function is a basic technology supported by all Transcend's embedded SD/microSD cards to prevent internal NAND flash data loss in event of a sudden power outage. The internal voltage detection circuit (VDT) of the controller monitors the external power supply show as below Figure.



Design the Freeze mechanism then set two Freeze threshold, Logic-Freeze Threshold and NAND-Freeze Threshold as show in below Figure. When the power loss takes place and once the voltage drop reaches the first threshold (Logic-Freeze Threshold), Transcend SD/microSD cards will stop the communication with the host. This action is prevent the host sending further instruction such like command or data that may be corrupted. If the voltage keep dropping then reach the second threshold (NAND-Freeze Threshold), Transcend SD/microSD cards stop writing data into NAND flash memory.



Note:

1. V1 is defined as voltage level of Logic-Freeze Threshold. When power provided to the card is below to V1, SD controller stop to receive any new data.
2. V2 is defined as voltage level of NAND-Freeze Threshold. When power provided to the card is below to V2, the card will not have enough power to finish data programming. SD controller should stop writing any data into flash and prevent writing error data into flash.

At the same time, there may remain temporarily data store in RAM buffer. Those data be written complete between Logic-Freeze Threshold and NAND-Freeze Threshold without error.

However, the power loss protection does not guarantee whole data stored in the SD card from damage due to abnormal power loss. The main purpose is to ensure the SD card from function failure.

5.2.7 Password Protection and Secure Erase Function

Support for password protected locking and unlocking of SD devices. It uses the LOCK/UNLOCK command(CMD42) which is available in SD command sets.The host sets the password and sends it to the card, after which the card will be locked. Data will be read and write protected, and can be viewed and changed only by entering the correct password. Where an incorrect password is provided, the card will remain locked.A password-protected card will be automatically locked after power reset. To permanently unlock a card, the password must be removed. The Scope Pro has SD LOCK function which uses CMD42 to LOCK/UNLOCK the SD/microSD cards.
Secure Erase permanently erases all user data in the SD/microSD cards when SD LOCK function is enable.

5.2.8 Transcend Scope Pro

Transcend's Scope Pro is a convenient software package that helps users monitor and manage SD status via an intuitive interface. It offers various useful features, including drive information and S.M.A.R.T. status monitoring, performance test, and health indication. It must be noted that Scope Pro is available when used with the TS-RDF5 card reader in Windows system. Scope Pro needs to be used with SDIO interface in Linux system. For more information, please refer the website link.
https://us.transcend-info.com/Embedded/Software/Monitor

5.2.9 Other Functions

Transcend SD embedded a lot of cutting-edge technology. Should you have any technical request, please contact the local support team or send us an e-mail.

6.Technology Term Explanations

6.1 TBW

Terabytes Written (TBW) directly measures how much you can write cumulatively into the drive over its lifetime. Essentially, it just includes the multiplication conducted above in the measurement itself.
For example, if your drive is rated for 365 TBW, that means you can write 365 TB into it before a replacement is required.
If its warranty period is 5 years, that works out to 365 TB ÷ (5 years × 365 days/year) = 200 GB of writes per day. If your drive was 200 GB in size, that's equivalent to 1 DWPD. Correspondingly, if your drive was rated for 3.65 PBW = 3,650 TBW, that works out to 2 TB of writes per day, or 10 DWPD.
As you can see, if you know the drive's size and warranty period, you can always calculate TBW from DWPD and vice-versa with simple multiplications or divisions. The two measurements are very similar.

6.2 DWPD

Drive Writes Per Day (DWPD) measures how many times you could overwrite the drive's entire size each day of its life. For example, suppose your drive is 200 GB and its warranty period is 5 years. If its DWPD is 1, that means you can write 200 GB (its size, one time) into it every single day for the next five years.
If you multiply that out, that's 200 GB per day × 365 days/year × 5 years = 365 TB of cumulative writes before you may need to replace it.
If the DWPD is 10 instead of 1, that means you can write 10 × 200 GB = 2 TB (its size, ten times) into it every day. Correspondingly, that's 3,650 TB = 3.65 PB of cumulative writes over 5 years.

6.3 MTBF – Telcordia SR332

MTBF (mean time between failures) is a measure of how reliable a hardware product or component is. For most components, the measurement is typically in thousands or even tens of thousands of hours between failures. For example, a SD may have a mean time between failures of 200,000 hours. A desired MTBF can be used as a quantifiable objective when designing a new product. The MTBF figure can be developed as the result of intensive testing, based on actual product experience, or predicted by analyzing known factors. The manufacturer may provide it as an index of a product's or component's reliability and, in some cases, to give customers an idea of how much service to plan for. In Transcend MTBF data, we use Telcordia SR-332 Issue 4 method to do estimated calculation.

7.SD Card Register information

7.1 OCR Register

The OCR 32-bit operation conditions register stores the VDD voltage profile of the non UHS-II card and VDD1 voltage profile of the UHS-II card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit

Note:

1) This bit is valid only when the card power up status bit is set.

2) This bit is set to LOW if the card has not finished the power up routine.

[Table 24] ORC Register Structure

OCR Bit Position	OCR Fields Definition
0-3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved for Low Voltage Range
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24	Switching to 1.8V Accepted(S18A)
25-28	Reserved
29	UHS-II Card Status
30	Card Capacity Status(CCS)1
31	Card Power Up Status bit(BUSY)2

7.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

[Table 25] CID Register Structure

Name	Field	Width	CID-Slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product Name	PNM	40	[103:64]
Product Revision	PRV	8	[63:56]
Product Serial Number	PSN	32	[55:24]
Reserved	-	4	[23:20]
Manufacturing Date	MDT	12	[19:8]
CRC7 Checksum	CRC	7	[7:1]
Not Used, Always"1"	-	1	[0:0]

7.2.1 MID

An 8-bit binary number that identifies the card manufacturer.

7.2.2 OID

A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards).

7.2.3 PNM

The product name is a string, 5 ASCII characters long.
PNM can be customized by Transcend.

7.2.4 PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m” is the least significant nibble.
As an example, the PRV binary value field for product revision “6.2” will be: 0110 0010.
PRV can be customized by Transcend.

7.2.5 PSN

The Serial Number is 32 bits of binary number.
PSN can be customized by Transcend.

7.2.6 MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The “m” field [11:8] is the month code. 1 = January.
The “y” field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date “April 2001” will be: 00000001 0100.
MDT can be customized by Transcend.

7.2.7 CRC

CRC7 checksum (7 bits).

7.3 CSD Register

The following sections describe the CSD fields and the relevant data types for the standard and High Capacity SD Memory Card. CSD Version 1.0 is applied Capacity SD Memory Card and CSD Version is applied to 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

7.3.1 CSD Register Structure

[Table 26] CSD Register Structure

CSD_STRUCTURE	CSD Structure version	Card capacity
0	CSD Version1.0	Standard Capacity
1	CSD Version2.0	High Capacity and Extended Capacity
2-3	reserved	-

7.3.2 CSD Register Structure(CSD Version 1.0)

[Table 27] CID Register Structure(Version 1.0)

Name	Field	Width	Cell Type	CSD-Slice
CSD Structure	CSD_STRUCTURE	2	R	[127:126]
Reserved	-	6	R	[125:120]
Data Data Access-Time-1	TAAC	8	R	[119:112]
Data Read Access-Time-2 in CLK Cycles(NSAC*100)	NSAC	8	R	[111:104]
Max. Read Transfer Rate	TRAN-SPEED	8	R	[103:96]
Card Command Classes	CCC	12	R	[95:84]
Max. Read Data Block Length	READ_BL_LEN	4	R	[83:80]
Partial Blocks for Read Allowed	READ_BL_PARTIAL	1	R	[79:79]
Write Block Misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
Read Block Misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR Implemented	DSR_IMP	1	R	[76:76]
Reserved	-	2	R	[75:74]
Device Size	C_SIZE	12	R	[73:62]
Max. Read Current @VDD Min.	VDD_R_CURR_MIN	3	R	[61:59]
Max. Read Current @VDD Max.	VDD_R_CURR_MAX	3	R	[58:56]
Max. Write Current @VDD Min.	VDD_W_CURR_MIN	3	R	[55:53]
Max. Write Current @VDD Max.	VDD_W_CURR_MAX	3	R	[52:50]

7.3.3 CSD Register Structure(CSD Version 2.0)

[Table 28] CID Register Structure(Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-Slice
CSD Structure	CSD_STRUCTURE	2	01b	R	[127:126]
Reserved	-	6	00 0000b	R	[125:120]
Data Read Access-Time-1	TAAC	8	0Eh	R	[119:112]
Data Read Access-Time-2 in CLK Cycles(NSAC*100)	NSAC	8	00h	R	[111:104]
Max. Data Transfer Rate	TRAN-SPEED	8	32h or 5Ah	R	[103:96]
Card Command Classes	CCC	12	01x110110101b	R	[95:84]
Max. Read Data Block Length	READ_BL_LEN	4	9	R	[83:80]
Partial Blocks for Read Allowed	READ_BL_PARTIAL	1	0	R	[79:79]
Write Block Misalignment	WRITE_BLK_MISALIGN	1	0	R	[78:78]
Read Block Misalignment	READ_BLK_MISALIGN	1	0	R	[77:77]
DSR Implemented	DSR_IMP	1	X	R	[76:76]
Reserved	-	6	00 0000b	R	[75:70]
Device Size	C_SIZE	22	00 xxxxh	R	[69:48]
Reserved	-	1	0	R	[47:47]
Erase Single Block Enable	ERASE_BLK_EN	1	1	R	[46:46]
Erase Sector Size	SECTOR_SIZE	7	7Fh	R	[45:39]
Write Protect Group Size	WP_GRP_SIZE	7	000000b	R	[38:32]
Write Protect Group Enable	WP_GRP_ENABLE	1	0	R	[31:31]
Reserved	-	2	00b	R	[30:29]
Write Speed Factor	R2W_FACTOR	3	010b	R	[28:26]
Max. Write Data Block Length	WRITE_BL_LEN	4	9	R	[25:22]
Partial Blocks for Write Allowed	WRITE_BL_PARTIAL	1	0	R	[21:21]
Reserved	-	5	00000b	R	[20:16]
File Format Group	FILE_FORMAT_GRP	1	0	R	[15:15]
Copy Flag(OTP)	COPY	1	X	R/W(1)	[14:14]
Permanent Write Protection	PERM_WRITE_PROTECT	1	X	R/W(1)	[13:13]
Temporary Write Protection	TMP_WRITE_PROTECT	1	X	R/W	[12:12]
File Format	FILE_FORMAT	2	00b	R	[11:10]
Reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
Not Used, Always"1"	-	1	1	-	[0:0]

7.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the cardduring the card identification. This address is used for the addressed host-card communication after thecard identification procedure. The default value of the RCA

7.5 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD configuration Register, SCR provide information on the SD memory card's special feature that were configured into the given card.

The size of SCR register is 64 bits. This register shall be set in the factory by Transcend. The following table describes the SCR register content

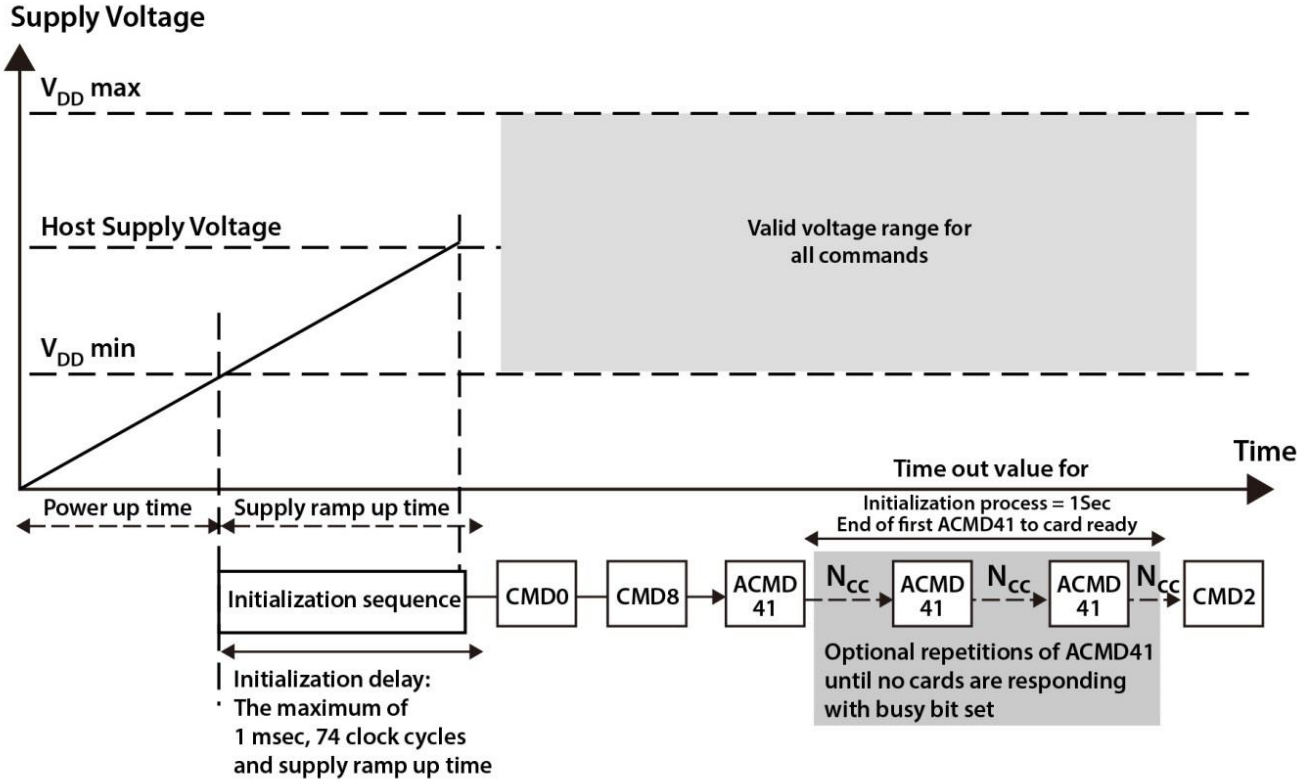
[Table 29] SCR Register Structure

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card- Spec. Version	SD_SPEC	4	R	[59:56]
Data_Status_After Erases	DATA_STAT_AFTER _ERASE	1	R	[55:55]
CPRM Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus Widths Supported	SD_BUS_WIDTHS	4	R	[51:48]
Spec. Version 3.00 or Higher	SD_SPEC3	1	R	[47:47]
Extended Security Support	EX_SECURITY	4	R	[46:43]
Spec. Version 4.00 or Higher	SD_SPEC4	1	R	[42:42]
Spec. Version 5.00 or Higher	SD_SPECX	4	R	[41:38]
Reserved	-	2	R	[37:36]
Command Support bits	CMD_SUPPORT	4	R	[35:32]
Reserved for Manufacturer Usage	-	32	R	[31:0]

8. Power Scheme

8.1 Power Up Time of Card

A card shall be ready to accept the first command within 1ms from detecting VDD min. The host may use up to 74 clocks for preparation before receiving the first command.



Power up time is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

Supply ramp up time provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the SD card can accept the first command,

The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

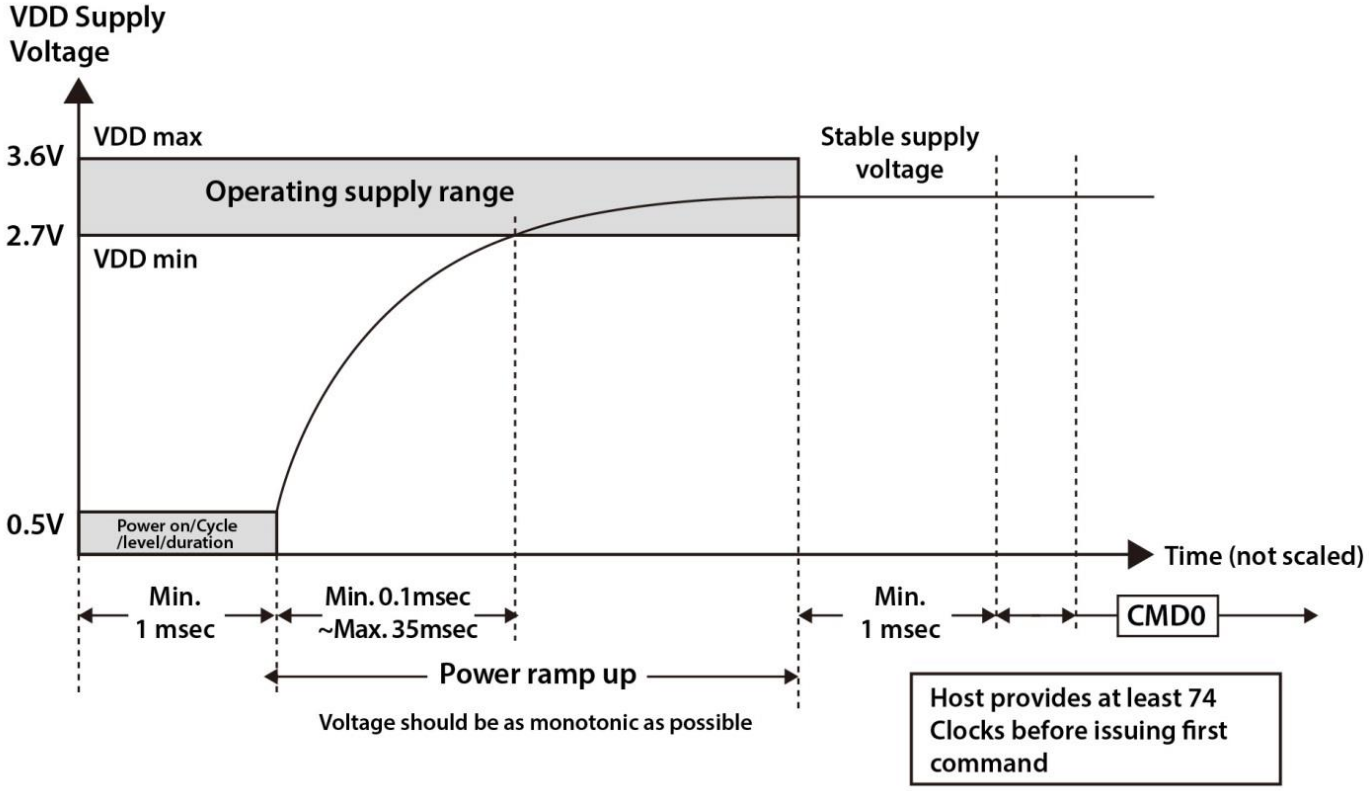
After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards,the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

8.2 Power Up Time to Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



8.3 Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.
(1) Voltage level shall be below 0.5V
(2) Duration shall be at least 1ms.

8.4 Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.
Followings are recommendation of Power ramp up:
(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
(4) Host shall wait until VDD is stable.
(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

8.5 Power Down and Power Cycle

When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

9.Contact Information

TAIWAN

No.70, XingZhong Rd., NeiHu Dist., Taipei, Taiwan, R.O.C

TEL +886-2-2792-8000

Fax +886-2-2793-2222

E-mail: sales-tw@transcend-info.com

Shanghai

E-mail: sales-cn@transcendchina.com

TEL: +86-21-6161-9388

Beijing

E-mail: sales-cn@transcendchina.com

TEL: +86-10-8265-9969

Shenzhen

E-mail: sales-cn@transcendchina.com

TEL: +86-755-2598-7200

Hong Kong

E-mail: sales-hk@transcend-info.com

TEL: +852-2331-8929

Los Angeles

E-mail: sales-us@transcend-info.com

TEL: +1-714-921-2000

Maryland

E-mail: sales-us@transcend-info.com

TEL: +1-410-689-4900

Silicon Valley

E-mail: sales-us@transcend-info.com

TEL: +1-408-785-5990

JAPAN

E-mail: sales-jp@transcend-info.com

TEL: +81-3-5820-6000

KOREA

E-mail: sales-kr@transcend-info.com

TEL: +82-2-782-8088

GERMANY

E-mail: sales-de@transcend-info.com

TEL: +49-40-538-907-0

NETHERLANDS

E-mail: sales-nl@transcend-info.com

TEL: +31-10-298-8500

United Kingdom

E-mail: sales-uk@transcend-info.com

TEL: +44-1442-202-880

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