ATP Industrial Grade
UHS-I microSDHC Card Specification

AF4GUDI-ADV002

AF8GUDI-ADV002

Revision 1.0_ADV

ATP Electronics, Inc.

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Revision History

Date	Version	Changes compared to previous issue
Dec. 20th, 2016	1.0	- Customized Specification for Advantech - OEM PN AF4GUDI-ADV002 added - OEM PN AF8GUDI-ADV002 added

1.0 Introduction

ATP UHS-I (Ultra High Speed 1) microSDHC card is compatible with SD Memory Card Specification Ver. 3.01, which supports up to 104MB/s Bus I/F Speed. The read speed of ATP UHS-I microSDHC memory card is up to 71MB/s; almost 3 times faster than conventional high speed microSDHC card (22.5MB/s read speed). ATP microSDHC UHS-I memory card is backward compatible to SD2.0 devices. However, the maximum transfer speed can be achieved along with UHS-I compliant devices.
ATP UHS-I microSDHC memory card implements advanced wear leveling algorithm and bad block management to prolong the life time of SD card. Nonetheless, the increased read speed and Read Disturb Protector – AutoRefresh technology enhance the read performance and assure the data integrity at the same time.
Considering high performance, reliability and compatibility, ATP UHS-I microSDHC memory card is highly recommended especially for navigation system, drive recorder, surveillance systems, DSLR and HD camcorder applications.

1.1 Main Features

- Compliant with SD Specification version 4.2 (USH-I card type)
- Supports SD mode, SPI mode
- High reliability, operating at -40^{o}C to 85^{o}C
- Single-Level Cell (SLC) / 1 bit-per-cell NAND Flash
- Supports dual voltage 3.3V and 1.8V I/O
- Bus Speed Mode (using 4 parallel data lines)

  - Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec

  - High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec

  - SDR12 - SDR up to 25MHz 1.8V signaling

  - SDR25 - SDR up to 50MHz 1.8V signaling

  - SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec

  - SDR104: 1.8V signaling, Frequency up to 208MHz, up to 104MB/sec

  - DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec

  Note: Timing in 1.8V signaling is different from that of 3.3V signaling.

- SIP (System In Package) process

- Water proof, Dust proof and ESD resistant
- Enhanced endurance by Advanced Static/Dynamic Wear-Leveling

- Read Disturb Protector - AutoRefresh technology to ensure data integrity especially in frequent read operations
- Data Retention – Dynamic Data Refresh Technology – Ensure Data Integrity
- Enhanced F/W algorithm to minimize the risk of a sudden power-off
- Support BCH ECC engine up to 72bits/1Kbyte
- Supports CPRM
- RoHS compliant
- CE & FCC certification
- Controlled BOM
- Customized service: adjustable CID registers, firmware & setting and logo by projects

1.2 Card Images

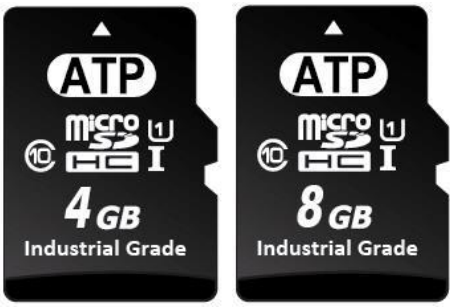


Figure 1-2: Product Pictures

1.3 Capacities

ATP P/N	CAPACITY
AF4GUDI-ADV002	4GB
AF8GUDI-ADV002	8GB

Table 1-3: Capacities

1.4 Icon Specification

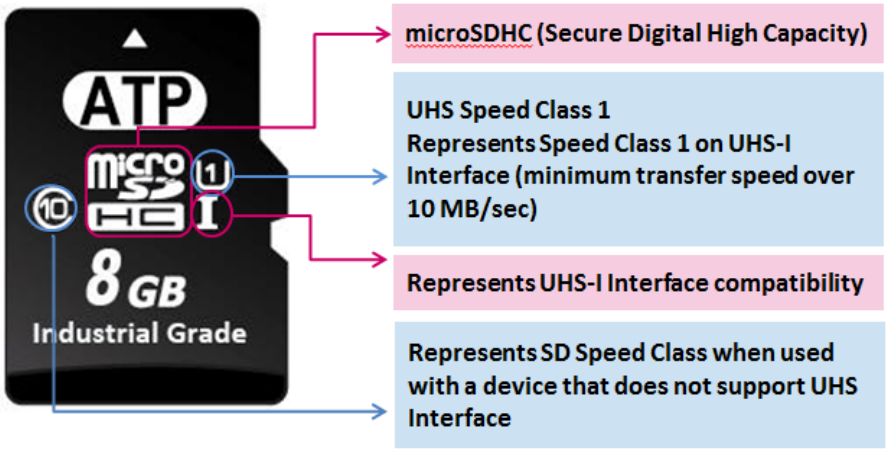


Figure 1-4: Icon Specification

2.0 microSD Card Hardware System

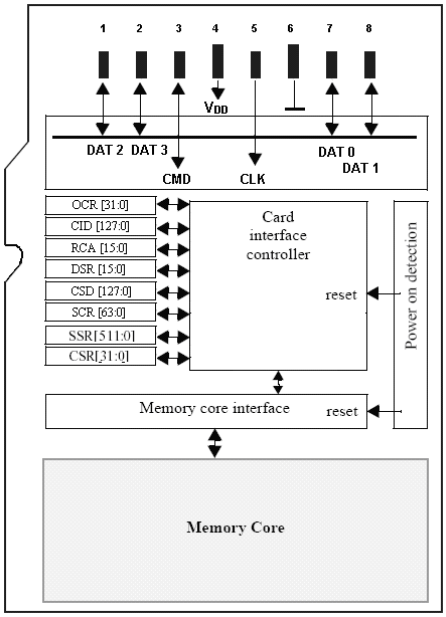


Figure 2-0: microSD Card Function Block Diagram

Pin #	SD Interface			SPI Interface		
	Name	Type[1]	Description	Name	Type[1]	Description
1	DAT2	I/O/PP	Data Line [Bit 2]	RSV		
2	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (Active Low)
3	CMD	PP	Command/ Response	DI	I	Data In
4	V_{DD}	S	Supply Voltage	V_{DD}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply Voltage Ground	V_{SS}	S	Supply Voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		

Table 2-0: Pad Assignment

Notes:
1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

2.1 Power Up

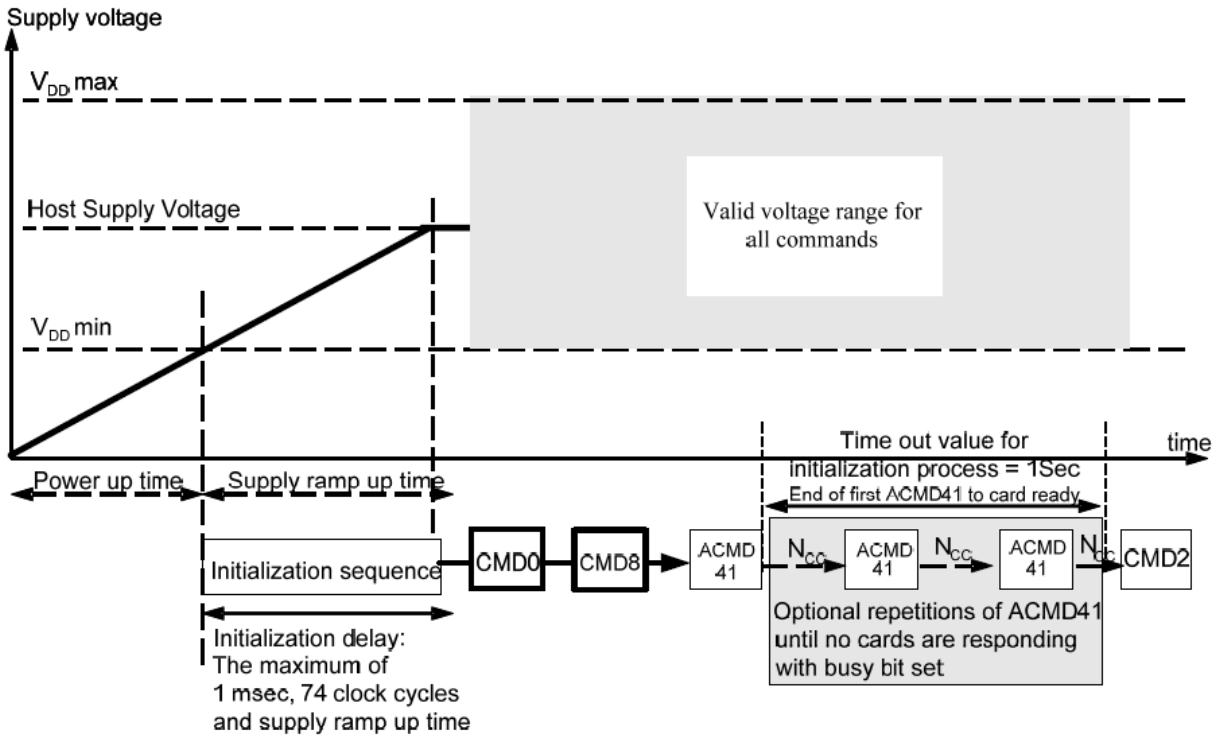


Figure 2-1 Power-Up Diagram

'Power up time' is defined as voltage rising time from 0 volt to VDD min (refer to 6.6) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.
'Supply ramp up time' provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the SD card can accept the first command,

- The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.
- After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the *idle state*. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.
- CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.
- ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

2.2 Power Up Time

Reset level is not described in Physical Layer Specification Version 2.00. Change of Figure 2-2 is applied.
Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

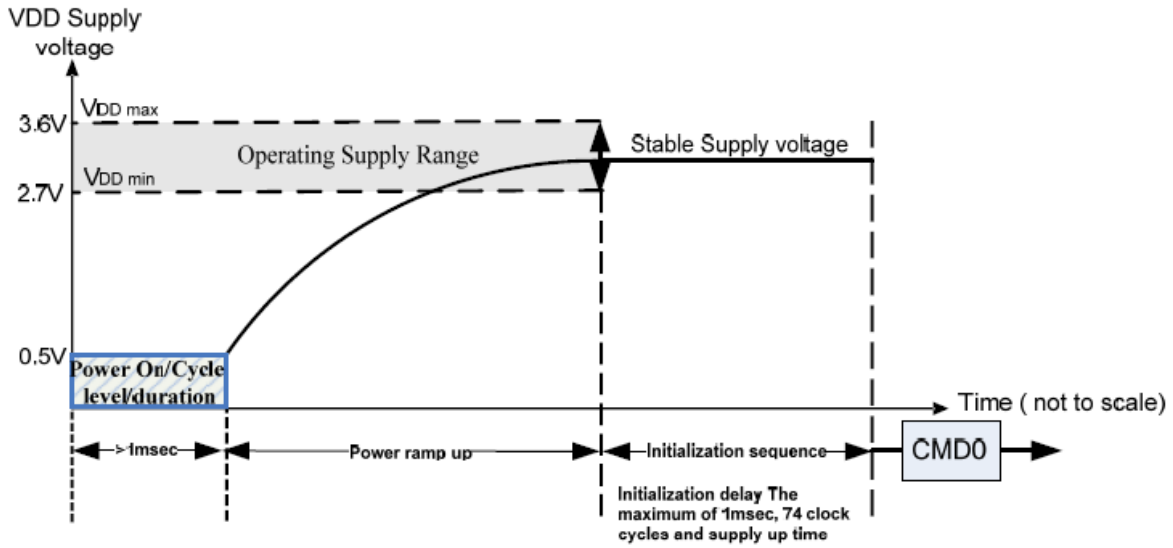


Figure 2-2 Change of Figure for power up

3.0 Product Specifications

3.1 Ultra High Speed Type I (UHS-I) Card

UHS-I provides up to 104MB/sec performance on 4-bit SD bus with the single end driver interface.

Card form factor is the same and existing connector can be used.

UHS-I Operation Modes

- DS - Default Speed up to 25MHz 3.3V signaling
- HS - High Speed up to 50MHz 3.3V signaling
- SDR12 - SDR up to 25MHz 1.8V signaling
- SDR25 - SDR up to 50MHz 1.8V signaling
- SDR50 - SDR up to 100MHz 1.8V signaling
- SDR104 - SDR up to 208MHz 1.8V signaling
- DDR50 - DDR up to 50MHz 1.8V signaling

Note: Timing in 1.8V signaling is different from that of 3.3V signaling.

3.2 UHS-I Card Types

UHS-I supports two card Types: UHS50 and UHS104

UHS-I is not applied to SDSC card but can be applied to SDHC and SDXC card.

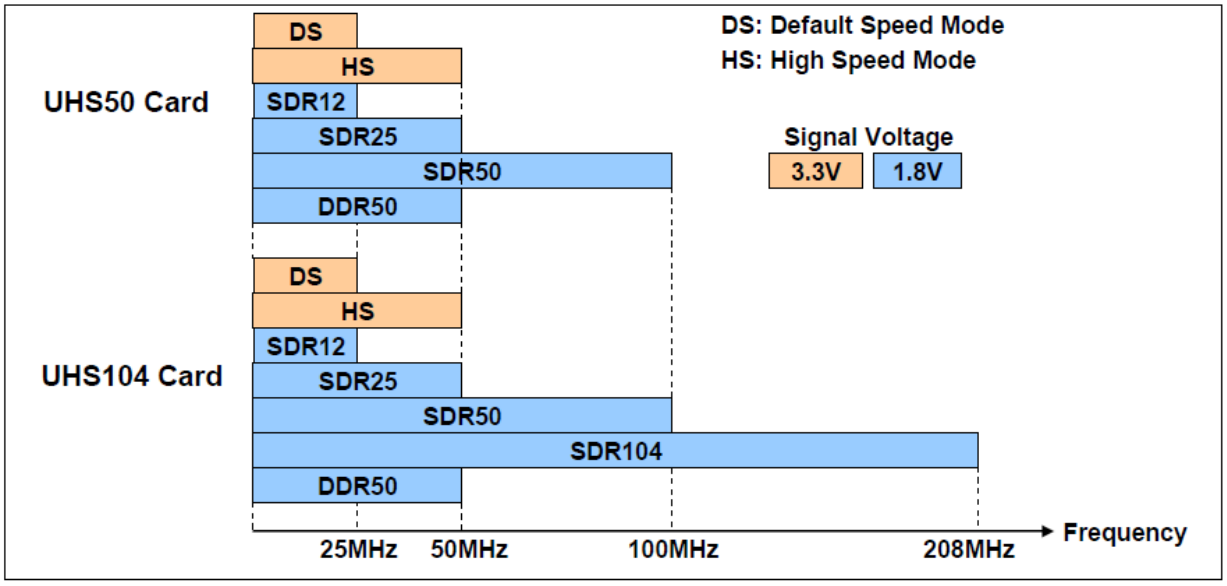


Figure 3-2-1 UHS-I Card Type Modes of Operation versus Frequency Range

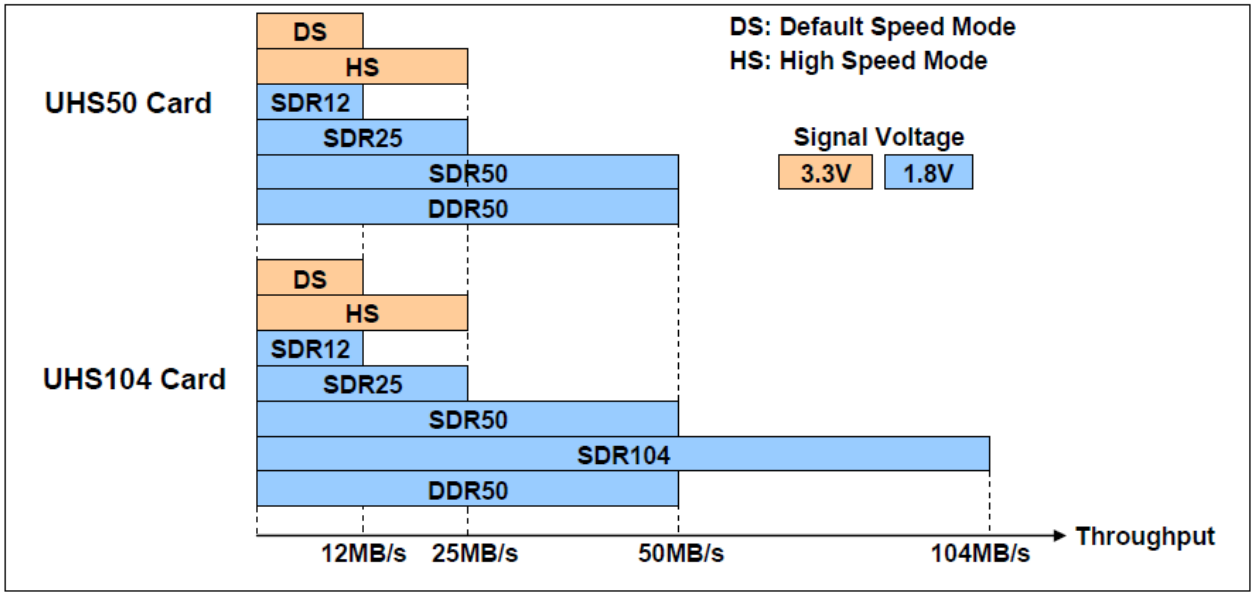


Figure 3-2-2 UHS-I Card Type Modes of Operation versus Throughout

3.3 Host and Card Combination

Table 3-3 shows usable UHS performance depends on the combination of host and card. UHS-I for removable card is presumed that one card is connected to a SD bus. Maximum performance of up to 104MB/s is possible only if host supports SDR104 mode and card is UHS104 Card (supports SDR104 mode). If card is a UHS50 Card or if host doesn't support SDR104 mode, performance is limited to 50MB/s (SDR104 mode cannot be used).
Host may use DDR50 mode with UHS50 Card and UHS104 Card in microSD form factors.

Host types:
SDR-FD – SDR signaling, fixed-delay (can't use tuning)
SDR-VD – SDR signaling, variable-delay (can use tuning)
DDR – DDR signaling

Host type / Card type	HOST-SDR-FD (SDR, fixed-delay)	HOST-SDR-VD (SDR, variable-delay)	HOST-DDR (DDR)
UHS50 card microSD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	DDR50 ≤ 50MHz
UHS104 card microSD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	DDR50 ≤ 50MHz
UHS50 card Full-size SD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	Optional
UHS104 card Full-size SD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	Optional

Table 3-3 host and card combination

Host can choose one of UHS-I modes by CMD6 Function Group 1. Each UHS-I mode is specified by the maximum frequency, sampling edges (rising-only or both) and maximum current consumption for compatibility with existing cards. Host can choose one of UHS-I mode depending on capability of generating SDCLK frequency and capacity of power supply host supported.

CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command.

3.4 Bus Speed Mode Selection Sequence

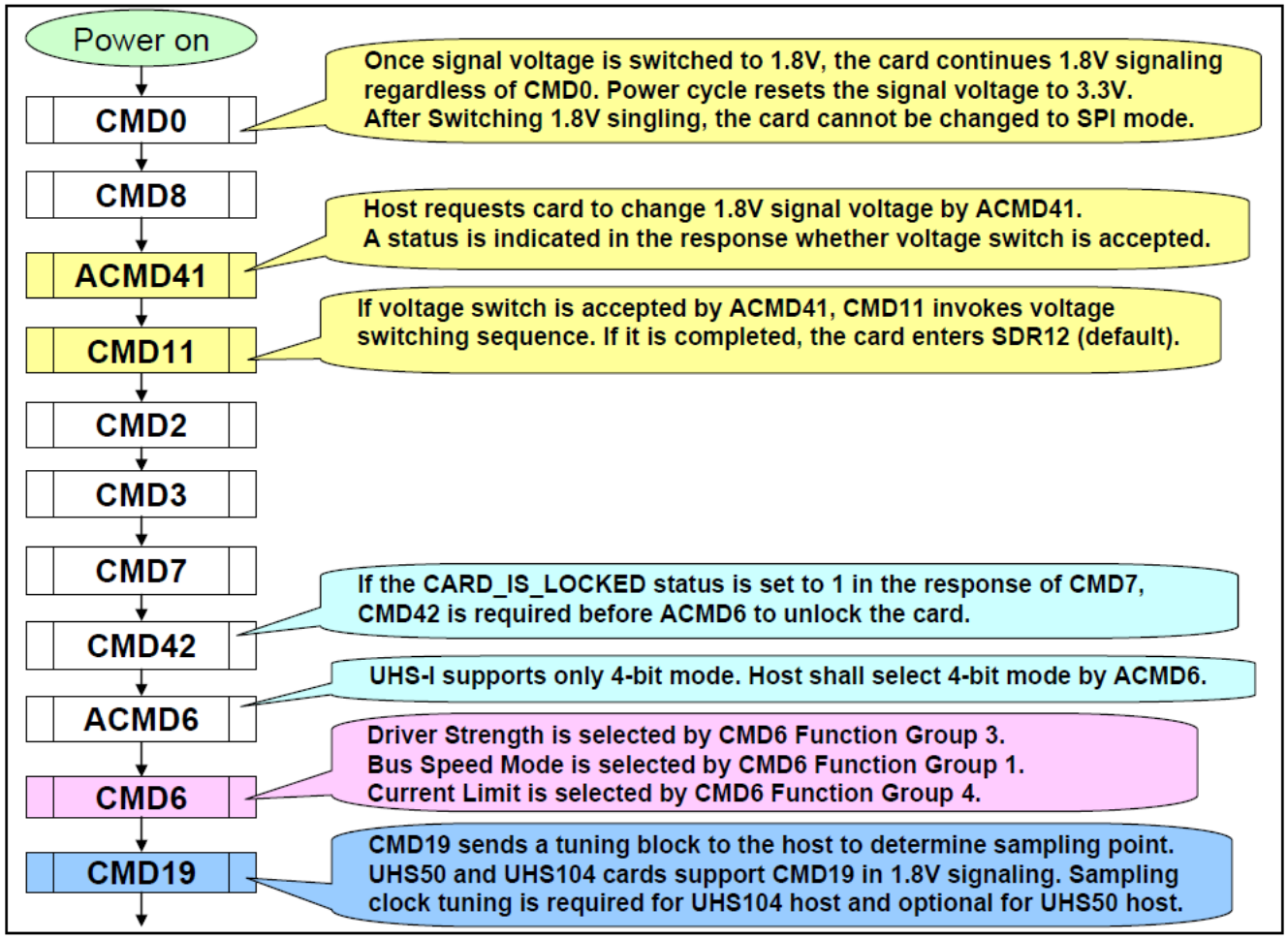


Figure 3-4 Command sequence to use UHS-I page

Figure 3-4 shows command sequence to use a UHS-I. After power cycle, card is in 3.3V signaling mode. The first CMD0 selects the bus mode; SD mode or SPI mode. 1.8V signaling mode can be entered only in SD mode. Once the card enters 1.8V signaling mode, the card cannot be switched to SPI mode or 3.3V signaling without power cycle. If the card receives CMD0, card returns to Idle state but still work with SDR12 timing. UHS-I is provided in SD mode but not in SPI mode.

As higher bus speed requires low level signaling, UHS-I adopts 1.8V signaling level for SDR50, DDR50 and SDR104 modes. Still card is supplied with 3.3V by the host and 1.8V signaling level for SDCLK, CMD and DAT[3:0] lines is converted from 3.3V power line. To avoid voltage mismatch between host and card, signaling level is changed by voltage switch sequence at the initialization. The host and card communicate using ACMD41 whether host and card support 1.8V signaling mode. Support of 1.8V signaling both host and card means UHS-I can be used. CMD11 invokes the voltage switch sequence. The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully. (Refer to Section 4.2.4 for more detail.)

Only 4-bit bus mode is supported in UHS-I except CMD42. If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.
Host can choose suitable output driver strength by CMD6 Function Group 3.

3.5 Comparison of SD Card

	SD3.0 Standard (Backward compatible to 2.0 host)	**SD3.0 SDHC (Backward compatible to 2.0 host)**
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support
CMD8 (SEND_IF_COND)	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)
Lock/Unlock Function	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support
Total Bus Capacitance for each signal line	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)

Table 3-5 Comparison of SD3.0 standard and SD3.0 SDHC

3.6 Environment Specifications

Type		Measurement
Temperature	Operation	-40°C to 85°C
	Non-Operation	-55°C to 90°C
Humidity	Operation	8%~95% relative humidity, non-condensing
	Non-Operation	
Random Vibration Test	Non-Operation	10~2000Hz, 6Grms, 30mins per axis
Bend Test	Non-Operation	10N to the center of the card
Torque Test	Non-Operation	0.1N-m or +/-2.5°
Salt Spray Test (MIL-STD-883G Method1009.8)	Non-Operation	35°C,Over 85% RH,3% Salt Concentration, 24 hours
UV Light Exposure Test (ISO 7816-1)	Non-Operation	254nm, 15Ws/cm2
Drop Test	Non-Operation	150cm/Free fall, total 6 drops

Table 3-6: Environment Specifications

3.7 Reliability

Type	Measurement		
Number of insertions	10,000 minimum		
Endurance	Advanced Dynamic / Static Wear Leveling algorithm 60K P/E cycles per block		
TBW (Total Bytes Written)	4GB	48	Terabytes Random Write
		96	Terabytes Sequential Write
	8GB	96	Terabytes Random Write
		192	Terabytes Sequential Write
MTBF(@ 25°C)	>5,000,000 hours		

Table 3-7: Reliability

Note 1:
TBW (total bytes written) is an index of how many TB (Terabytes) can be used for written under product life time.
The endurance for flash cards can be predicted based on the usage conditions applied to the device, the internal NAND flash cycles, the write amplification factor, and the wear leveling efficiency of the flash devices. Above TBW is for reference only. Please contact ATP for TBW in real applications.
1 TeraBytes = 1000 GigaBytes (Disk storage)

Note 2:
MTBF highly depends on testing method. All ATP products are tested with Bellcore Method II (Combines Method I <Parts Count> predictions with laboratory data).

3.8 Data Retention

Endurance Used	Number of P/E Cycles Used (block level)	Corresponding Data Retention at 55 °C use condition
≦10% P/E cycles	≦6,000 Cycles	5 years
＞10% P/E cycles	＞6,000 Cycles ～60,000 Cycles	1 year

Table 3-8: Data Retention

Note 1: Data retention refers to the ability of a memory bit to retain its data state over a period of time after the data is written in NAND Flash regardless of whether the part is powered on or powered off.
A data retention failure is when there is at least 1 bit of data that cannot be read or is read incorrectly.

Note 2: NAND Flash suppliers refer to JEDEC JESD47 & JESD22 for Data Retention testing. Assuming <10% of maximum P/E cycles, and UBER<1E-14 at minimum required ECC.

Note 3: ATP simulation test based on JEP122G and the parameters provided by NAND flash suppliers.

3.9 Performance

High Speed Mode		
Capacity	**Seq. Read (MB/s)**	**Seq. Write (MB/s)**
4GB	23.64	19.86
8GB	23.65	19.73

Table 3-9-1: High Speed Mode Performance

Note 1: High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/s
Note 2: Tested by CrystalDiskMark 3.0.2.e with 1000MB file size. The performance is for reference only since it may vary depending on the configuration, firmware, setting, application and test environment.

SDR50 Speed Mode		
Capacity	**Seq. Read (MB/s)**	**Seq. Write (MB/s)**
4GB	46.64	34.53
8GB	46.57	26.91
SDR104 Speed Mode		
Capacity	**Seq. Read (MB/s)**	**Seq. Write (MB/s)**
4GB	81.96	39.04
8GB	81.93	26.59

,

Table 3-9-2: UHS Mode Performance

Note 1: SDR50: One of UHS modes with single data rate. Up to 50MB/s at 100MHz
Note 2: SDR104: One of UHS modes with single data rate. Up to 104MB/s at 208MHz
Note 3: Tested by CrystalDiskMark 3.0.2.e with 1000MB file size. The performance may vary depending on the configuration, firmware, setting, application and test environment.

3.10 Extra Features

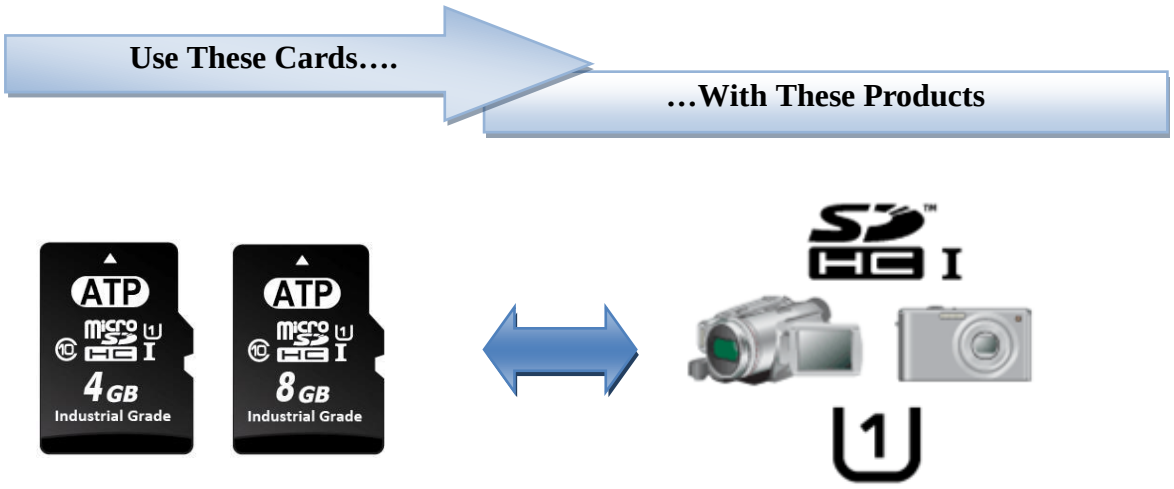
Type	Measurement
Water Proof	IEC 60529 Edition 2.1: 2001-02—IPX7, below 1000mm water, 30min
Dust Proof	IEC 60529 Edition 2.1: 2001-02—IP5X
ESD Resistant	IEC 61000-4-2: contact pad +/- 4KV, non-contact pad (Coupling plane discharge) +/- 8KV, non-contact pad (Air discharge) +/- 15KV
RoHS Compliant	Yes

Table 3-10: Extra Features

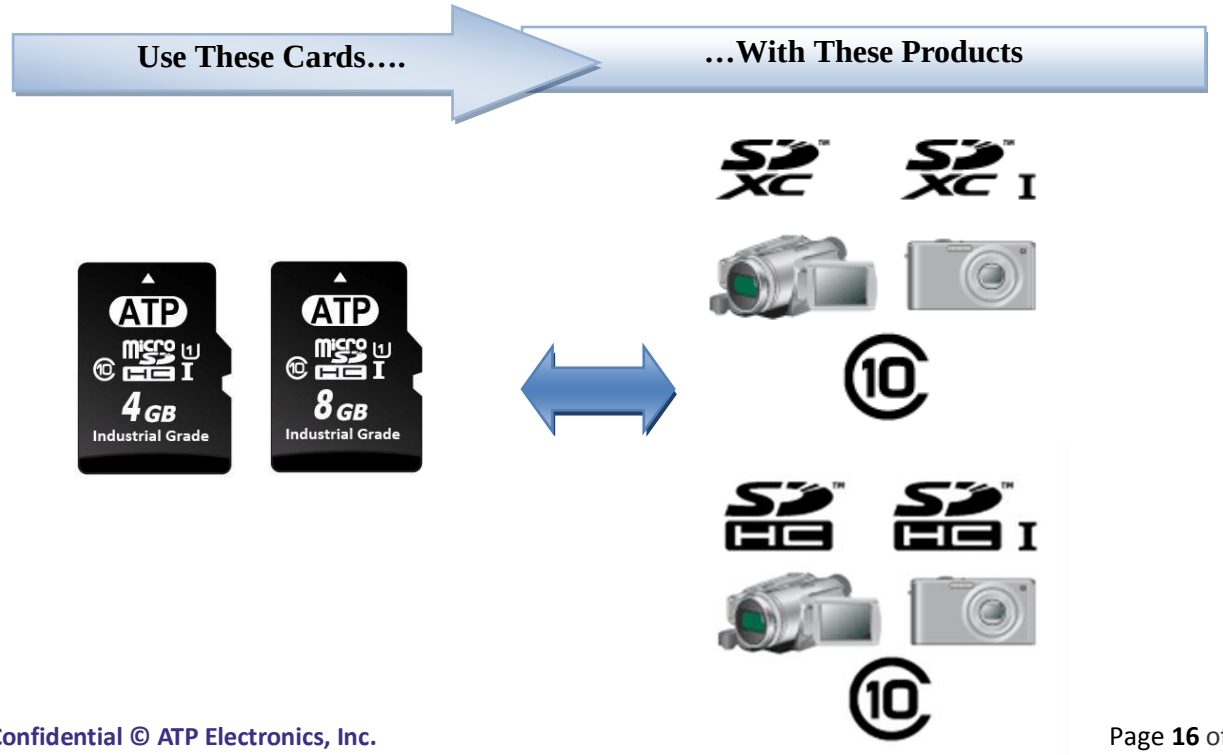
3.11 Host Device Compatibility: Optimize UHS Performance

Before choosing a card for your video-recording device, it is important that you understand how to use your memory card to its greatest ability. Speed Class and UHS Speed Class are two different speed indication symbols for different devices. However, a UHS-I memory card may also indicate a Speed Class. The UHS-I SDHC/microSDHC card can still apply on non-UHS (high speed) devices. Nonetheless, the Ultra-High-Speed SDHC/microSDHC card can reach its best performance along with UHS-I devices.

UHS Speed Class Compatibility



Speed Class Compatibility



3.12 Advanced Dynamic / Static Wear Leveling - Longer Life Expectancy

The program / erase cycle of each sector/page/block is finite. Writing constantly on the same spot will cause the flash to wear out quickly. Furthermore, bit errors are not proportioned to P/E cycles; sudden death may occur when the block is close to its P/E cycle limit. Then unrecoverable bit errors will cause fatal data loss (especially for system data or FAT).

Advanced Dynamic/ Static wear leveling algorithm evenly distributes the P/E cycles of each block to minimize the possibility of one block exceeding its max P/E cycles before the rest. In return, the life expectancy of memory storage device is prolonged and the chance/occurrence of unrecoverable bit errors could be reduced.

3.13 Read Disturb Protector – AutoRefresh Technology – Ensure Data Integrity

Over time the error bits accumulate to the threshold value in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the corrupted data is then moved to a different location within the flash cell.

This occurrence is alarming in frequent read applications, such as navigation systems or OS boot-up devices. The map or operation system is preloaded into the SD/microSD card and there may be a one-time write and followed by a read operation only. Read disturbance is the result of electrical interference from multiple read operations in surrounding pages. After a NAND flash accumulates 100,000 read cycles, uncorrectable ECC errors may occur in the affected pages, which results in data failure in the same block.

To prevent data corruption, the ATP SD/microSD card monitors the error bit levels in each read operation; when it reaches the preset threshold value, AutoRefresh is activated by programming the data into another block before the data is corrupted. After the re-programming operation is complete, the controller reads the data and compares the data/parity to ensure data integrity.

Owing to different user experiences, please contact ATP for AutoRefresh in real applications.

3.14 Data Retention – Dynamic Data Refresh Technology – Ensure Data Integrity

Different from AutoRefresh, which focuses on read disturbance mitigation for intensive-read areas, Dynamic Data Refresh focuses on long-term data retention assurance for non-read areas.

Dynamic Data Refresh is implemented to overcome data retention and data loss issues occurring from data stored in seldom accessed area for long periods of time.

Without affecting front-end read / write performance, Dynamic Data Refresh is a special firmware algorithm that runs automatically in the background ; bit by bit, it sequentially scans for seldom accessed areas with flag records. If the amount of error bit / read count exceeds threshold, a Data refresh mechanism is then triggered - by moving data to healthy blocks to prevent data loss risk.

Ideally, the whole user area will be scanned and refreshed periodically without having additional trigger or modification from the host side.

3.15 Physical Dimension (Units in mm)

Type	Measurement
Length	15mm +/- 0.1mm
Width	11mm +/- 0.1mm
Thickness	1.0mm +/- 0.1mm
Weight	0.4 g Max.

Table 3-14: Physical Dimension

3.16 Mechanical Form Factor (Units in mm)

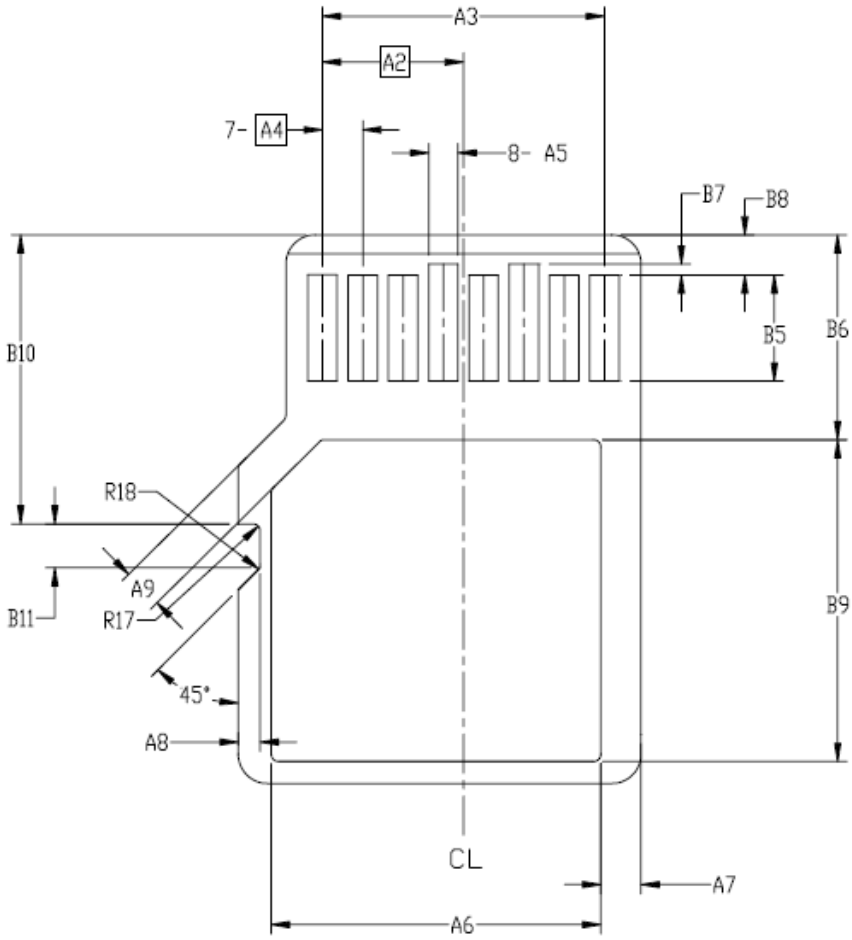


Figure 3-15 -1 Dimensions of microSD (Bottom View)

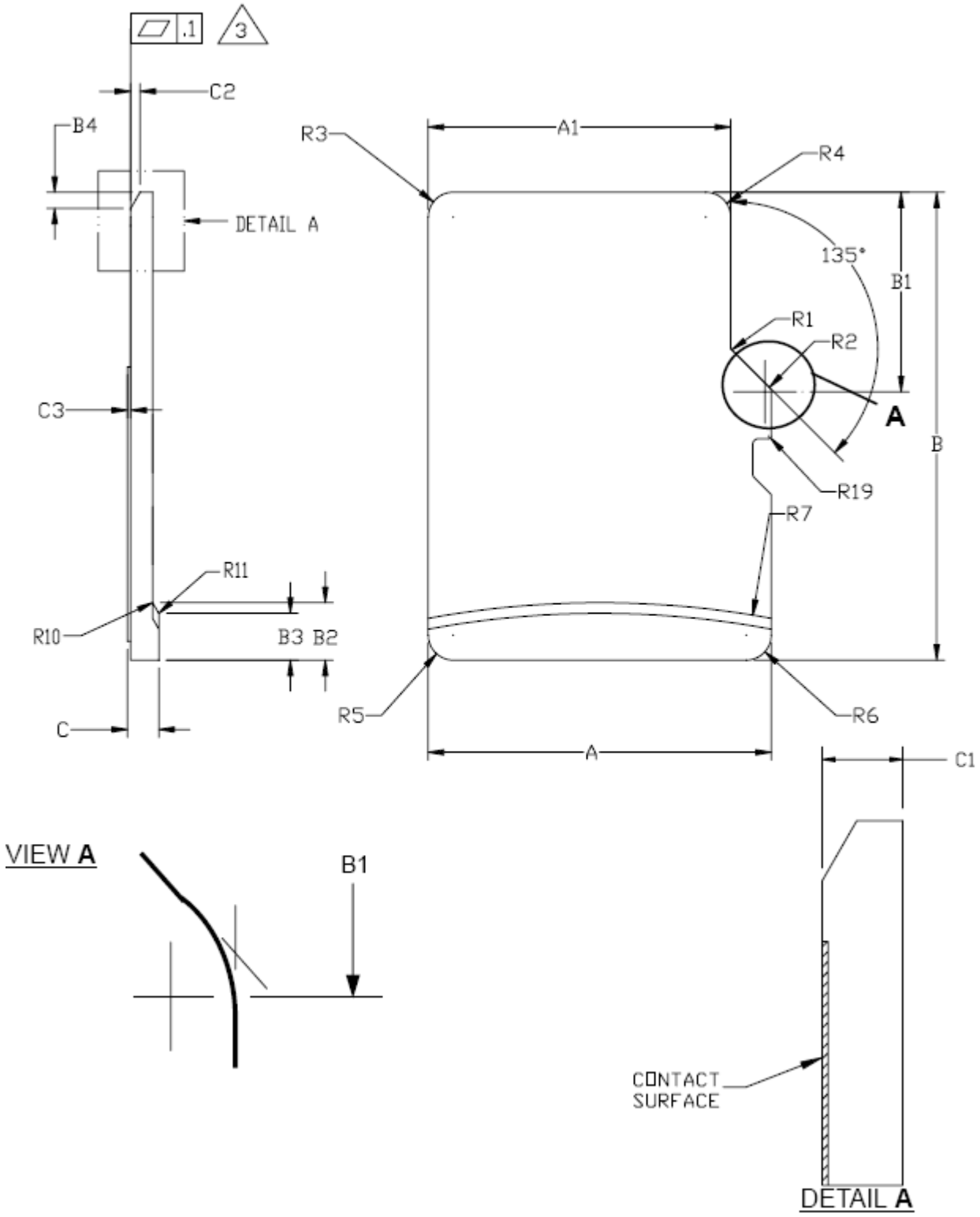


Figure 3-15-2: Dimensions Of microSD (Top View)

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	

R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

4.0 Electrical Characteristics

4.1 DC Characteristics

Bus Operating Conditions for 3.3V Signaling

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75x V_{DD}	-	V	I_{OH}=-2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}	-	0.125 x V_{DD}	V	I_{OL}=-2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625x V_{DD}	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.25 x V_{DD}	V	
Operating Current* (4GB)	Icc	50	120	mA	High Speed Mode
	Icc	100	160	mA	UHS-I Mode
Operating Current* (8GB)	Icc	50	160	mA	High Speed Mode
	Icc	110	200	mA	UHS-I Mode
Power Up Time		-	250	ms	From 0V to $V_{DD\ min}$
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 4-1-1 DC Characteristics Under 3.3V Signaling

*Note: Operation current might subject to working configuration and applications, and is highly dependent on the density and the operation mode. Please contact ATP for detailed information.

The current consumption is measured by averaging over 1 second.

- Before first command: Maximum 15 mA
- During initialization: Maximum 100 mA
- Operation in Default Speed Mode: Maximum 100 mA for SDSC and SDHC
  100 mA (XPC=0) or 150 mA (XPC=1) for SDXC
- Operation in High Speed Mode: Maximum 200 mA
- Operation in UHS-I Mode: Maximum 400 mA (UHS50,DDR50) or 800 mA (UHS104)
- Operation with other functions: Maximum 500 mA

Some functions can be added by CMD6 and SDIO (ex. McEX, ASSD and Combo Card). Host needs to select functions so that the total current of selected functions shall be up to 500mA. In case of UHS-I card, host should not select UHS-I mode and the other functions at the same time.

Bus Operating Conditions For 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=-2mA
Input High Voltage	V_{IH}	1.27	2.0	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.58	V	

Table 4-1-2 DC Characteristics Under 1.8V Signaling

4.2 Summary of Bus Speed Mode and Maximum Current

The maximum frequency and the maximum current are determined by CMD6.

Bus Speed Mode*1	Max. Bus Speed [MB/s]	Max. Clock Frequency [MHz]	Signal Voltage [V]	Max. Current*2 [mA/3.6V VDD]		
				SDSC*3	SDHC*4	SDXC*5
SDR104	104	208	1.8	-	800*6	800*6
SDR50	50	100	1.8	-	400	400
DDR50	50	50	1.8	-	400	400
SDR25	25	50	1.8	-	200	200
SDR12	12.5	25	1.8	-	100	100/150*7
High Speed	25	50	3.3	200	200	200
Default Speed	12.5	25	3.3	100	100	100/150*7

*1: The card supports a UHS-I mode shall support all lower UHS-I modes.
*2: Host can control current by the current limit function in CMD6.
*3: SDSC stands for SD Standard Capacity Memory Card and
*4: SDHC stands for SD High Capacity Memory Card.
*5: SDXC stands for SD Extended Capacity Memory Card.
*6: Detail of socket handling 800mA will be specifying in mechanical addenda.
*7: Host can select either max. current by XPC in ACMD41.
In SPI mode, XPC is not supported and the current shall be up to 100mA.

Table 1-2 : Bus Speed Modes

4.3 AC Characteristics

High Speed Mode Bus Timing (3.3V Signaling)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	3	ns	C_{card} <= 10 pF(1 card)
Clock fall time	t_{THL}	-	3	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	2	-	ns	C_{card} <= 10 pF(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF(1 card)
Output Hold time	t_{OH}	2.5	-	ns	C_L <= 15 pF(1 card)
Total System capacitance for each line[1]	C_L	-	40	pF	1 card

Table 4-3-1: Bus Timing - Parameter Values (High Speed Mode)

Notes: In order to satisfy severe timing, host shall drive only one card.

Default Bus Timing (3.3V Signaling)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card} <= 10 pF(1 card)
Clock frequency Identification Mode	f_{OD}	0[1]/100	400	KHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	10	ns	C_{card} <= 10 pF(1 card)
Clock fall time	t_{THL}	-	10	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	5	-	ns	C_{card} <= 10 pF(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF(1 card)
Output Delay time during Identification Mode	t_{ODLY}	-	50	ns	C_L <= 40 pF(1 card)

Table 4-3-2: Bus Timing - Parameter Values (Default)

Notes: 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4- Clock Control).

High Speed Mode Bus Timing (1.8V Signaling) For SDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input SDCK					
Clock frequency Data Transfer Mode	f_{PP}	0	100	MHz	C_L <= 10 pF(1 card)
Clock low time	t_{WL}	3	-	ns	C_L <= 10 pF(1 card)
Clock high time	t_{WH}	3	-	ns	C_L <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	2	ns	C_L <= 10 pF(1 card)
Clock fall time	t_{THL}	-	2	ns	C_L <= 10 pF(1 card)
Inputs DAT (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_L <= 10 pF(1 card)
Input hold time	t_{IH}	0.8	-	ns	C_L <= 15 pF(1 card)
Outputs DAT (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	7.5	ns	C_L <= 30 pF(1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_L <= 15 pF(1 card)

Table 4-3-3: Bus Timing - Parameter Values (SDR50 mode)

High Speed Mode Bus Timing (1.8V Signaling) For SDR104 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input SDCK					
Clock frequency Data Transfer Mode	f_{PP}	0	208	MHz	C_L <= 10 pF(1 card)
Clock low time	t_{WL}	1.5	-	ns	C_L <= 10 pF(1 card)
Clock high time	t_{WH}	1.5	-	ns	C_L <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	0.96	ns	C_L <= 10 pF(1 card)
Clock fall time	t_{THL}	-	0.96	ns	C_L <= 10 pF(1 card)
Inputs DAT (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	1.4	-	ns	C_L<= 10 pF(1 card)
Input hold time	t_{IH}	0.8	-	ns	C_L<= 5 pF(1 card)
Outputs DAT (referenced to CLK rising edge)					
Card Output Phase	t_{OP}	0	2	UI	C_L <= 15 pF(1 card)

Table 4-3-4: Bus Timing - Parameter Values (SDR104 mode)

SD Dual Data Rate (DDR50) Mode Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Clock frequency Data Transfer Mode(PP)	f_{PP}	0	50	MHz	C_L<= 10 pF(1 card)
Clock Duly Cycle	-	25	55	%	-
Clock rise time	t_{TLH}	-	4	ns	C_L<= 10 pF(1 card)
Clock fall time	t_{THL}	-	4	ns	C_L <= 10 pF(1 card)
CMD Inputs and Output (referenced to CLK rising edge)					
CMD Input set-up time	t_{ISU}	6	-	ns	C_L<= 10 pF(1 card)
CMD Input hold time	t_{IH}	0.8	-	ns	C_L <= 10 pF(1 card)
CMD Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L<= 30 pF(1 card)
CMD Output Hold time	t_{OH}	1.5		ns	C_L <= 15 pF(1 card)
DAT Inputs and Output (referenced to CLK rising and falling edge)					
DAT Input set-up time	t_{ISU}	3	-	ns	C_L<= 10 pF(1 card)
DAT Input hold time	t_{IH}	0.8	-	ns	C_L <= 10 pF(1 card)
DAT Output Delay time during Data Transfer Mode	t_{ODLY}	-	7	ns	C_L<= 25 pF(1 card)
DAT Output Hold time	t_{OH}	1.5		ns	C_L <= 15 pF(1 card)

Table 4-3-5: SD Dual Data Rate(DDR50) Mode Timing

4.4 Bus Signal Line Load

The total capacitance C_L of each line of the SD bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:
$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$
N is the number of connected cards.

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	10	100	Kohm	to prevent bus floating
Pull-up resistance for DAT	R_{DAT}	10	100	Kohm	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 20 MHz
Pull-up resistance inside card (pin1)	RDAT3	10	90	Kohm	May be used for card detection

Table 4-4: Bus Signal Line Load

5.0 Card Registers

Within the card interface seven registers are defined: OCR, CID, CSD, RCA, SCR, SSR and CSR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA register is configuration register storing actual configuration parameters and SSR and CSR are two status fields.

Register	SD 2.x	SD 3.0x
Operation Condition Register (OCR)	V	V
Card Identification Register (CID)	V	V
Driver Stage Register (DSR)	NA	NA
Relative Card Address Register (RCA)	V	V
Card Specific Data Register (CSD)	V	V
SD Card Configuration Register (SCR)	V	V

5.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.
The 32-bit operation conditions register stores the VDD voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to1. Additionally, this register includes 2 more status information bits.
Bit 31 - Card power up status bit, this status bit is set if the card power up procedure has been finished.
Bit 30 - Card Capacity Status bit, 0 indicates that the card is SDSC. 1 indicates that the card is SDHC or SDXC. The Card Capacity Status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify SDSC Card or SDHC/SDXC Card.
The OCR register shall be implemented by the cards.

OCR bit position	OCR Fields Definition
0-3	reserved
4	reserved
5	reserved
6	reserved
7	Reserved for Low Voltage Range
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24[3]	Switching to 1.8V Accepted (S18A)
25-29	reserved
30	Card Capacity Status (CCS)[1]
31	Card power up status bit (busy)[2]

VDD Voltage Window

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.
3) Only UHS-I card supports this bit.

The supported voltage range is coded as shown in Table5-1. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

Table5-1: OCR Register Definition

5.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

Table 5-2: The CID fields

- **MID**

An 8 bit binary number identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

- **OID**

A 2 ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

- **PNM**

The product name is a string, 5 ASCII characters long.

- **PRV**

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble. As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010

- **PSN**

The Serial Number is 32 bits of binary number.

• **MDT**

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m). The “m” field [11:8] is the month code. 1 = January.

The “y” field [19:12] is the year code. 0 = 2000. As an example, the binary value of the Date field for production date “April 2001” will be: 00000001 0100.

• **CRC**

CRC7 checksum (7 bits). This is the checksum of the CID contents.

5.3 CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be hanged by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Table 5-3-1 shows Definition of the CSD Version 2.0 for High Capacity SD Memory Card and Extended Capacity SD Memory Card.

The following sections describe the CSD fields and the relevant data types for SDHC and SFXC Cards.

CSD Version 2.0 is applied to SDHC and SDXC Cards. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R= readable, W(1)= writable once, W= multiple writable.

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h, 5Ah, 0Bh or 2Bh	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	xxxxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

Table 5-3-1: The CSD Register fields

• **CSD_STRUCTURE**

Version number of the related CSD structure

CSD_STRUCTURE	CSD structure version	Valid for SD Card Physical Specification Version
0	CSD version 1.0	Version 1.0-1.10
1	CSD version 2.0	Version 2.00 /High Capacity
2-3	reserved	

Table 5-3-2: CSD register structure

- **TAAC**

This field is fixed to 0Eh, which indicates 1 ms. The host should not use TAAC, NSAC, and R2W_FACTOR to calculate timeout and should uses fixed timeout values for read and write operations (See 4.6.2).

- **NSAC**

This field is fixed to 00h. NSAC should not be used to calculate time-out values.

- **TRAN_SPEED**

Definition of this field is same as in CSD Version1.0.
UHS50 Card sets TRAN_SPEED to 0Bh (100Mbit/sec), for both SDR50 and DDR50 modes.
UHS104 Card sets TRAN_SPEED to 2Bh (200Mbit/sec).

- **CCC**

Definition of this field is same as in CSD Version1.0.

- **READ_BL_LEN**

This field is fixed to 9h, which indicates READ_BL_LEN=512 Byte.

- **READ_BL_PARTIAL**

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

- **WRITE_BLK_MISALIGN**

This field is fixed to 0, which indicates that write access crossing physical block boundaries is always disabled in SDHC and SDXC Cards.

- **READ_BLK_MISALIGN**

This field is fixed to 0, which indicates that read access crossing physical block boundaries is always disabled in SDHC and SDXC Cards.

- **DSR_IMP**

Definition of this field is same as in CSD Version1.0.

- **C_SIZE**

This field is expanded to 22 bits and can indicate up to 2 TBytes (It is the same as the maximum memory space specified by a 32-bit block address.)
This parameter is used to calculate the user data area capacity in the SD memory card (not include the protected area). The user data area capacity is calculated from C_SIZE as follows:
memory capacity = (C_SIZE+1) * 512K byte

The Minimum user area size of SDHC Card is 4,211,712 sectors (2GB + 8.5MB).
The Minimum value of C_SIZE for SDHC in CSD Version 2.0 is 001010h (4112).
The maximum user area size of SDHC Card is (32GB - 80MB)
The maximum value of C_SIZE for SDHC in CSD Version 2.0 is 00FF5Fh (65375).
The Minimum user area size of SDXC Card is 67,108,864 sectors (32GB).
The Minimum value of C_SIZE for SDXC in CSD Version 2.0 is 00FFFFh (65535).

- **ERASE_BLK_EN**

This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

- **SECTOR_SIZE**

This field is fixed to 7Fh, which indicates 64 KBytes. This value is not related to erase operation. SDHC and SDXC Cards indicate memory boundary by AU size and this field should not be used.

- **WP_GRP_SIZE**

This field is fixed to 00h. SDHC and SDXC Cards do not support write protected groups.

- **WP_GRP_ENABLE**

This field is fixed to 0. SDHC and SDXC Cards do not support write protected groups.

- **R2W_FACTOR**

This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout

- **WRITE_BL_LEN**

This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.

- **WRITE_BL_PARTIAL**

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

- **FILE_FORMAT_GRP**

This field is set to 0. Host should not use this field.

- **COPY**

Definition of this field is same as in CSD Version1.0.

- **PERM_WRITE_PROTECT**

Definition of this field is same as in CSD Version1.0.

- **TMP_WRITE_PROTECT**

Definition of this field is same as in CSD Version1.0.

- **FILE_FORMAT**

This field is set to 0. Host should not use this field.

- **CRC**

Definition of this field is same as in CSD Version1.0.

5.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

5.5 DSR Register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

5.6 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacturer.
The following table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
CPRM Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
Spec. Version 3.00 or higher	SD_SPEC3	1	R	[47]
Extended Security Support	EX_ SECURITY	4	R	[46:43]
Reserved		9	R	[42:34]
Command Support bits	CMD_SUPPORT	2	R	[33:32]
reserved for manufacturer usage	-	32	R	[31:0]

Table 5-6-1: The SCR Fields

SCR_STRUCTURE	SCR structure version	SD Physical Layer Specification Version
0	SCR version 1.0	Version 1.01-3.01
1-15	reserved	

Table 5-16-2: SCR Register Structure Version

5.7 SSR Register

SD Status; information about the card proprietary features (See 6.5)

5.8 CSR Register

Card Status; information about the card status

6.0 SD Card Functional Description

6.1 SD BUS Protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

• **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

• **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

• **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

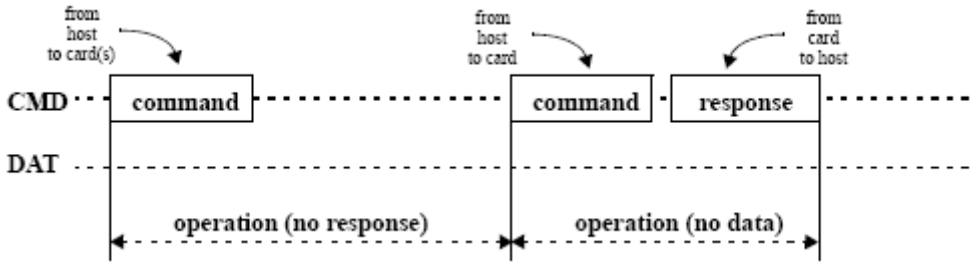


Figure 6-1-1: "no response" And "no data" Operations

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction. This type of bus transactions transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Card are done in blocks. Data blocks always were succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

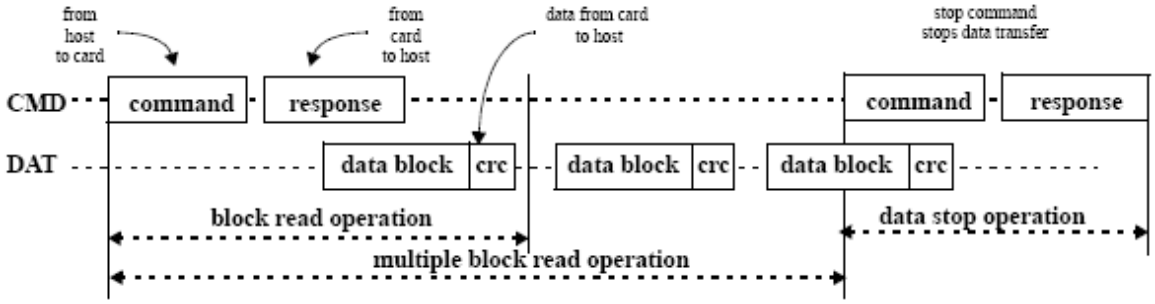


Figure 6-1-2: (Multiple) Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line regardless of the number of data lines used for transferring the data

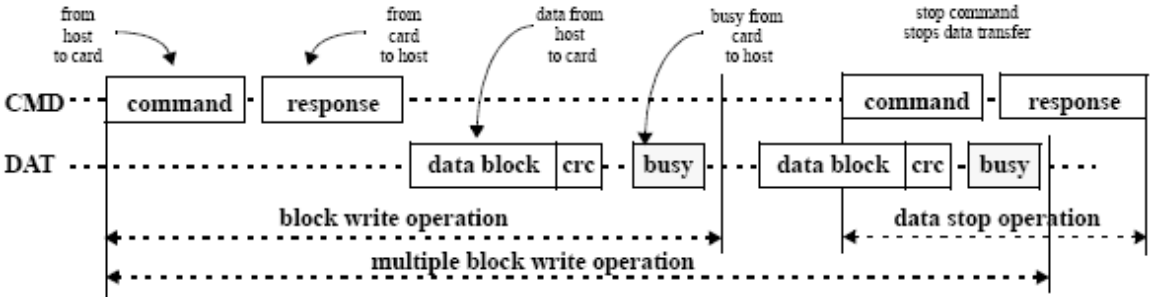


Figure 6-1-3: (Multiple) Block Write Operation

Command tokens have the following coding scheme:

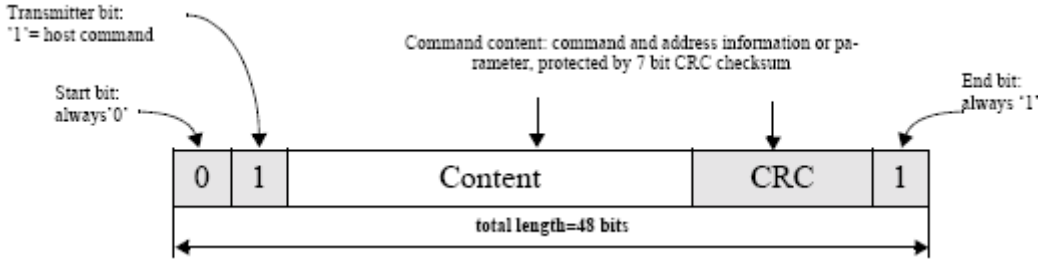


Figure 6-1-4: Command Token Format

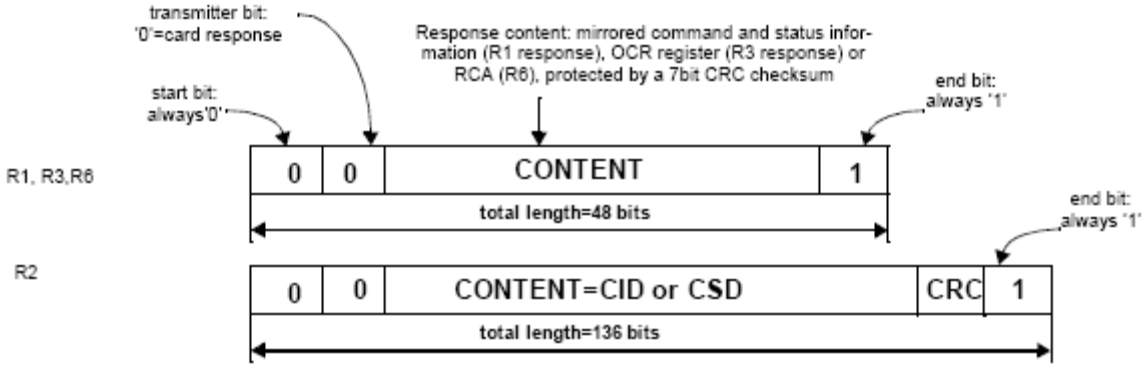


Figure 6-1-5: Response Token Format

In the CMD line the MSB bit is transmitted first the LSB bit is the last. When the wide bus option is used, the data is transferred 4 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).
There are two types of Data packet format for the SD card.
(1) Usual data (8 bit width) The usual data (8 bit width) are sent in LSB (Least Significant Byte) first, MSB (Most Significant Byte) last manner. But in the individual byte it is MSB (Most Significant Bit) first, LSB (Least Significant Bit) last.

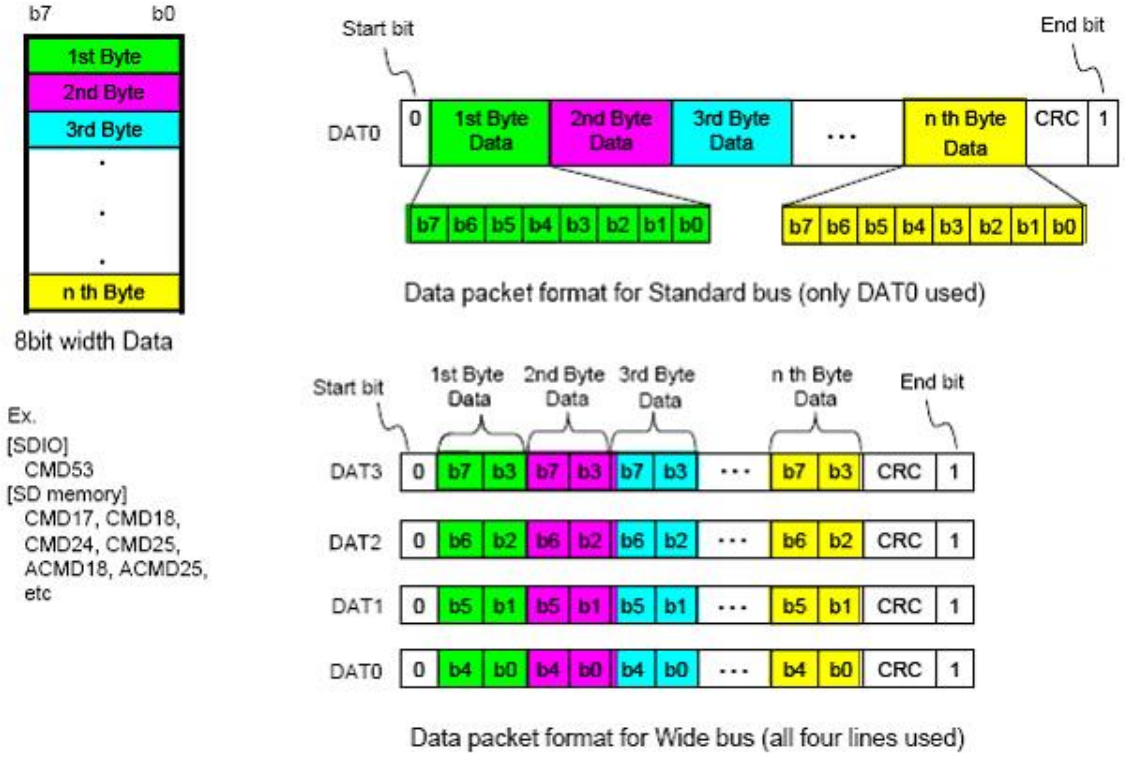


Figure 6-1-6: Data packet format - Usual data

(2) Wide width data (SD Memory Register) The wide width data is shifted from MSB bit.

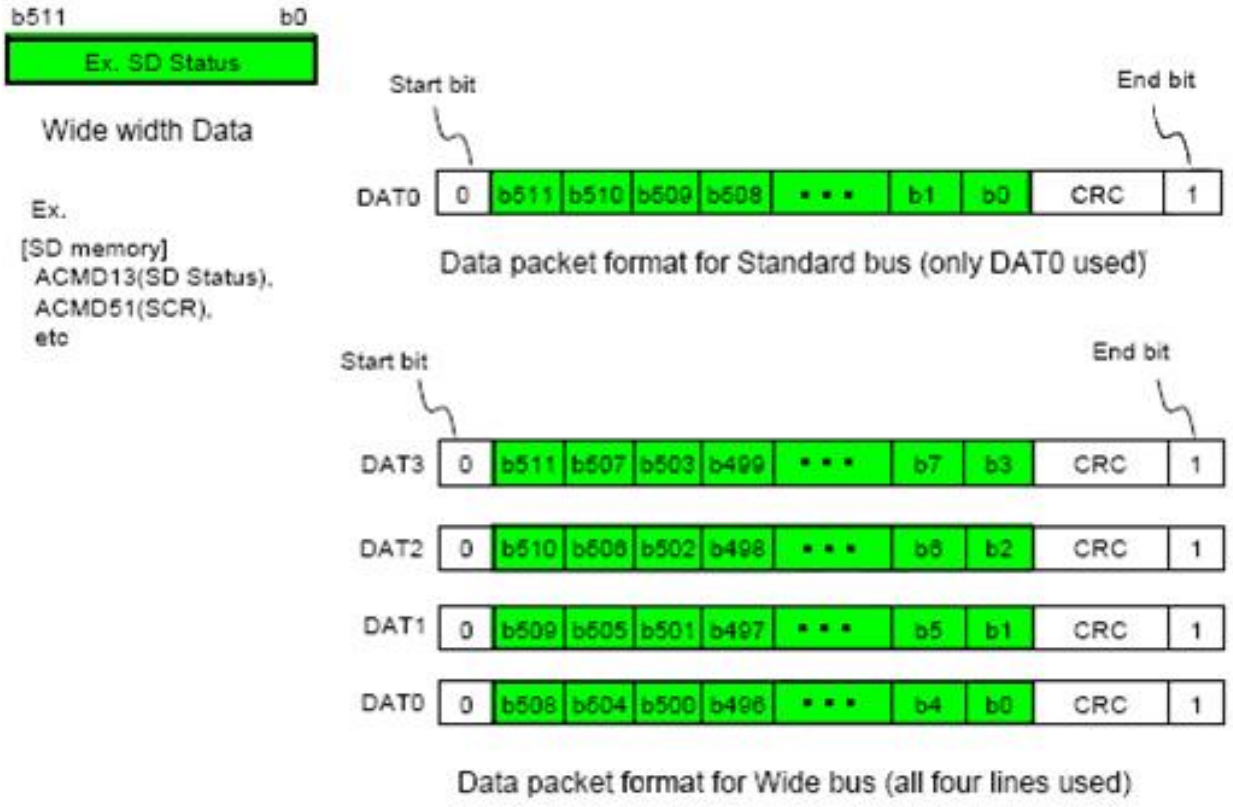


Figure 6-1-7: Data packet format - Wide width data

6.2 Command

6.2.1 Command Types and Format

All communication between host and cards is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

• Broadcast commands

Broadcast commands are intended for all cards. Some of these commands require a response.

• Addressed (point-to-point) commands

The addressed commands are sent to the addressed card and cause a response from this card.

• Command Format

All commands have a fixed code length of 48 bits, needing a transmission time of 2.4 µs @ 20 MHz

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	command index	argument	CRC7	end bit

Table 6-2-1: Command Format

A command always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (host = '1'). The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by 'x' in the table above indicates this variable is dependent on the command. All commands are protected by a CRC. Every command codeword is terminated by the end bit (always '1'). All commands and their arguments are listed in Table 6-3-Table 6-11.

6.2.2 Command Classes

The command set of the SD Card system is divided into several classes (See Table 6-2). Each class supports a set of card functionalities.

Class 0, 2, 4, 5 and 8 are mandatory supported by ATP SD Cards. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each card, providing the host with information on how to access the card.

	CARD COMMAND CLASS	0	1	2	3	4	5	6	7	8	9	10	11
SUPPORTED COMMANDS	class description	basic	reserved	block read	Reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD2	Mandatory	+											
CMD3	Mandatory	+											
CMD4	Mandatory	+											
CMD5	Optional										+		
CMD6	Mandatory											+	
CMD7	Mandatory	+											
CMD8	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD15	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory					+							
CMD25	Mandatory					+							
CMD27	Mandatory					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory						+						
CMD33	Mandatory						+						
CMD34-37	Optional											+	
CMD38	Mandatory						+						
CMD42	Optional								+				
CMD50	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57	Optional											+	
ACMD6	Mandatory									+			

ACMD13	Mandatory									+			
ACMD22	Mandatory									+			
ACMD23	Mandatory									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Table 6-2-2: Card Command Classes (CCCs)

6.2.3 Detailed Command Description

The following tables define in detail all SD Card bus commands.

CMD INDEX	type	argument	resp	abbreviation	command description
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	Resets all cards to idle state
CMD1	Reserved				
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks any card to send the CID numbers on the CMD line (any card that is connected to the host will respond)
CMD3	bcr	[31:0] stuff bits	R6	SEND_RELATIVE_ ADDR	Ask the card to publish a new relative address (RCA)
CMD4	bc	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of all cards
CMD5	reserved for I/O cards (refer to the "SDIO Card Specification")				
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1b (only from the selected card)	SELECT/DESELECT_ CARD	Command toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases, the card is selected by its own relative address and gets deselected by any other address; address 0 deselects all. In the case that the RCA equals 0, then the host may do one of the following: - Use other RCA number to perform card de-selection. - Re-send CMD3 to change its RCA number to other than 0 and then use CMD7 with RCA=0 for card de-selection.
CMD8	bcr	[31:12]reserved bits [11:8]supply voltage(VHS) [7:0]check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to '0'.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	Addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	Addressed card sends its card identification (CID) on CMD the line.
CMD11	ac	[31:0] reserved bits (all 0)	R1	VOLTAGE_SWITCH	Switch to 1.8V bus signaling level.
CMD12	ac	[31:0] stuff bits	R1b	STOP_ TRANSMISSION	Forces the card to stop transmission
CMD13	ac	[31:16] RCA [15:0] stuff bits	R1	SEND_STATUS	Addressed card sends its status register.
CMD14	Reserved				
CMD INDEX	type	argument	resp	abbreviation	command description
CMD15	ac	[31:16] RCA [15:0] reserved bits	-	GO_INACTIVE_ STATE	Sends an addressed card into the *Inactive State*. This command is used when the host explicitly wants to deactivate a card. Reserved bits shall be set to '0'.

Table 6-2-3: Basic commands (class 0)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of SDHC and SDXC Cards, block length set by CMD16 command doen't affect memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit. In DDR50 mode, data is sampled on both edges of the clock. Therefore, block length shall always be even.
CMD17	adtc	[31:0] data address[2]	R1	READ_SINGLE_ BLOCK	In the case of a Standard Capacity SD Memory Card, this command, this command reads a block of the size selected by the SET_BLOCKLEN command.[1] In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD18	adtc	[31:0] data address[2]	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command. Block length is specified the same as READ_SINGLE_BLOCK command.
CMD19	adtc	[31:0] reserved bits (all 0)	R1	SEND_TUNING_ BLOCK	64 bytes tuning pattern is sent for SDR50 and SDR104.
CMD20	ac	[31:28]Speed Class Control [27:0]Reserved (all-0)	R1b	SPEED_CLASS_CON TROL	Speed Class control command. Refer to Section 4.13.2.8.
CMD21 CMD22	Reserved				
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.

Table 6-2-4: Block oriented read commands (class 2)

1) The data transferred shall not cross a physical block boundary unless READ_BLK_MISALIGN is set in the CSD.
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 Bytes unit).

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in Table 6-2-4
CMD20	ac	[31:28]Speed Class Control [27:0]Reserved (all-0)	R1b	SPEED_CLASS_CONTROL	Speed Class control command.
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.
CMD24	adtc	[31:0] data address	R1	WRITE_BLOCK	In case of SDSC Card, block length is set by the SET_BLOCKLEN command1. In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows. Block length is specified the same as WRITE_BLOCK command.
CMD26	Reserved For Manufacturer				
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	programming of the programmable bits of the CSD.

Table 6-2-5: Block oriented write commands (class 4)

1) The data transferred shall not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD. In the case that write partial blocks is not supported, then the block length=default block length (given in CSD).
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes **unit).**

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD28	ac	[31:0] data address	R1b	SET_WRITE_PROT	if the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29	ac	[31:0] data address	R1b	CLR_WRITE_PROT	if the card provides write protection features, this command clears the write protection bit of the addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	if the card provides write protection features, this command asks the card to send the status of the write protection bits.[1]
CMD31	reserved				

Table 6-2-6: Block oriented write protection commands (class 6)

1) 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to 0.
2) Data address is in byte units in a Standard Capacity SD Memory Card.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD32	ac	[31:0] data address	R1	ERASE_WR_BLK_START	Sets the address of the first write-block to be erased.
CMD33	ac	[31:0] data address	R1	ERASE_WR_BLK_END	Sets the address of the last write block of the continuous range to be erased.
CMD38	ac	[31:0] stuff bits	R1b	ERASE	Erases all previously selected write blocks.
CMD39	reserved				
CMD41	reserved				

Table 6-2-7: Erase commands (class 5)

1) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).
2) CMD40 is moved to Class 7.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in table 6-2-4
CMD40	adtc	Reserved for Security Specification			
CMD42	adtc	[31:0] stuff bits.	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43-49 CMD51	reserved				

Table 6-2-8: Lock card (class 7)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather than a standard command
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR1	R1	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose/application specific commands. In case of a SDSC Card, block length is set by the SET_BLOCK_LEN command. In case of SDHC and SDXC Cards, block length is fixed to 512 bytes. The host sets RD/WR=1 for reading data from the card and sets to 0 for writing data to the card
CMD58-59	reserved				
CMD60-63	reserved for manufacturer				

Table 6-2-9: Application specific commands (class 8)

All the application-specific commands (given in Table 6-2-9) are supported if Class 8 is allowed (mandatory in SD Memory Card).

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD52. CMD54	reserved for I/O mode (refer to "SDIO Card Specification")				

Table 6-2-10: I/O mode commands (class 9)

All future reserved commands shall have a codeword length of 48 bits, as well as their responses (if there are any).

The following table describes all the application specific commands supported/reserved by the SD Card. All the following ACMDs shall be preceded with APP_CMD command (CMD55).

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
ACMD1-5	Reserved				
ACMD6	ac	[31:2] stuff bits [1:0]bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4 bits bus) to be used for data transfer. The allowed data bus widths are given in SCR register.
ACMD7-12	Reserved				
ACMD13	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD Card status.
ACMD14-16	Reserved for Security Specification				
ACMD17	reserved				
ACMD18	Reserved for SD security applications1				
ACMD19 - 21	reserved				
ACMD22	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_BLOCKS	Send the number of the written (without errors) write blocks. Responds with 32bit+CRC data block. If WRITE_BL_PARTIAL='0', the unit of ACMD22 is always 512 byte. If WRITE_BL_PARTIAL='1', the unit of ACMD22 is a block length which was used when the write command was executed.
ACMD23	ac	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block)(2).
ACMD24	reserved				
ACMD25	Reserved for SD security applications1				
ACMD27-28	Reserved for Security Specification				
ACMD29	Reserved				
ACMD30-35	Reserved for Security Specification				
ACMD38	Reserved for SD security applications1				
ACMD39 to ACMD40	reserved				
ACMD41	bcr	[31]reserved bit [30]HCS(OCR[30]) [29:24]reserved bits	R3	SD_SEND_OP_COND	Sends host capacity support information (HCS) and asks the accessed card to send its operating condition register

		[23:0] VDD Voltage Window(OCR[23:0])			(OCR) content in the response on the CMD line. HCS is effective when card receives SEND_IF_COND command. Sends request to switch to 1.8V signaling (S18R). Reserved bit shall be set to '0'. CCS bit is assigned to OCR[30]. XPC controls the maximum current in the default speed mode of SDXC card. XPC=0 means 100mA (max.) but speed class is not supported. XPC=1 means 150mA (max.) and speed class is supported.
ACMD42	ac	[31:1] stuff bits [0]set_cd	R1	SET_CLR_CARD_DETECT	Connect[1]/Disconnect[0] the 50KOhm pull-up resistor on CD/DAT3 (pin 1) of the card.
ACMD43 ACMD49	--	--	--	--	Reserved for SD security applications1
ACMD51	adtc	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).
ACMD52-54	Reserved for security specification				
ACMD55	Not Exist				Equivalent to CMD55.
ACMD56-59	Reserved for Security Specification				

Table 6-2-11: Application Specific Commands used/reserved by SD Card

1) Refer to the "Part3 Security Specification" for a detailed explanation about the SD Security Features
2) Command STOP_TRAN (CMD12) shall be used to stop the transmission in Write Multiple Block whether or not the pre erase (ACMD23) feature is used.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD6	adtc	[31] Mode 0:Check function 1:Switch function [30:24] reserved (All '0') [23:20] reserved for function group 6 (0h or Fh) [19:16] reserved for function group 5 (0h or Fh) [15:12] function group 4 for current limit [11:8] funciton group 3 for drive strength [7:4] function group 2 for command system [3:0] function group 1 for access mode	R1	SWITCH_ FUNC	Checks switchable function (mode 0) and switch card function (mode 1).
CMD34	Reserved for each command system set by switch function command (CMD6). Detailed definition is referred to each command system specification.				
CMD35					
CMD36					
CMD37					
CMD50					
CMD57					

Table 6-2-12: Switch function commands (class 10)

6.3 Card State Transition Table

Table 6-3 defines the card state transitions in dependency of the received command.

	CURRENT STATE									
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**
TRIGGER OF STATE CHANGE	**changes to**									
CLASS INDEPENDENT										
"Operation Complete"	-	-	-	-	-	-	-	tran	stby	-
class 0										
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	-
CMD2	-	ident	-	-	-	-	-	-	-	-
CMD3	-	-	stby	stby	-	-	-	-	-	-
CMD4	-	-	-	stby	-	-	-	-	-	-
CMD7, card is addressed	-	-	-	tran	-	-	-	-	prg	-
CMD7, card is not addressed	-	-	-	stby	stby	stby	-	dis	-	-
CMD8	idle	-	-	-	-	-	-	-	-	-
CMD9	-	-	-	stby	-	-	-	-	-	-
CMD10	-	-	-	stby	-	-	-	-	-	-
CMD12	-	-	-	-	-	tran	prg	-	-	-
CMD13	-	-	-	stby	tran	data	rcv	prg	dis	-
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	-
class 2										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD17	-	-	-	-	data	-	-	-	-	-
CMD18	-	-	-	-	data	-	-	-	-	-
class 4										
CMD16	see class 2									
CMD24	-	-	-	-	rcv	-	-	-	-	-
CMD25	-	-	-	-	rcv	-	-	-	-	-
CMD27	-	-	-	-	rcv	-	-	-	-	-
class 6										
CMD28	-	-	-	-	prg	-	-	-	-	-
CMD29	-	-	-	-	prg	-	-	-	-	-
CMD30	-	-	-	-	data	-	-	-	-	-
class 5										
CMD32	-	-	-	-	tran	-	-	-	-	-
CMD33	-	-	-	-	tran	-	-	-	-	-
CMD38	-	-	-	-	prg	-	-	-	-	-
class 7										
CMD42	-	-	-	-	rcv	-	-	-	-	-
class 8										
CMD55	idle	-	-	stby	tran	data	rcv	prg	dis	-
CMD56; RD/WR = 0	-	-	-	-	rcv	-	-	-	-	-
CMD56; RD/WR = 1	-	-	-	-	data	-	-	-	-	-
ACMD6	-	-	-	-	tran	-	-	-	-	-
ACMD13	-	-	-	-	data	-	-	-	-	-

	CURRENT STATE									
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**
ACMD22	-	-	-	-	data	-	-	-	-	-
ACMD23	-	-	-	-	tran	-	-	-	-	-
ACMD18,25,26,38, 43,44,45,46,47,48,49	Refer to “SD Card Security Specification” for explanation about the SD Security Features									
ACMD41, card VDD range compatible	ready	-	-	-	-	-	-	-	-	-
ACMD41, card is busy	idle	-	-	-	-	-	-	-	-	-
ACMD41, card VDD range not compatible	ina	-	-	-	-	-	-	-	-	-
ACMD42	-	-	-	-	tran	-	-	-	-	-
ACMD51	-	-	-	-	data	-	-	-	-	-
class 9										
CMD52-CMD54	refer to "SDIO Card Specification"									
class 10										
CMD6	-	-	-	-	data	-	-	-	-	-
CMD34-37,50,57	-	-	-	-	tran	-	-	-	-	-
class 11										
CMD41; CMD43...CMD49, CMD58-CMD59	reserved									
CMD60...CMD63	reserved for manufacturer									

Table 6-3: Card state transition table

6.4 Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit string corresponding to the response codeword. The code length depends on the response type.
A response always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (card = 0). A value denoted by 'x' in the tables below indicates a variable entry. All responses except the type R3 (see below) are protected by a CRC (see Chapter 4.5 for the definition of CRC7). Every command codeword is terminated by the end bit (always 1).
There are five types of responses for the SD Memory Card. The SDIO Card supports additional response types named R4 and R5. Refer to SDIO Card Spec for detailed information on the SDIO commands and responses. Their formats are defined as follows:

6.4.1 R1 (Normal Response Command)

Code length is 48 bits. The bits 45:40 indicate the index of the command to be responded to, this value being interpreted as a binary coded number (between 0 and 63). The status of the card is coded in 32 bits. Note that if a data transfer to the card is involved, then a busy signal may appear on the data line after the transmission of each block of data. The host shall check for busy after data block transmission.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	card status	CRC7	end bit

Table 6-4-1 Response R1

6.4.2 R1b

R1b is identical to R1 with an optional busy signal transmitted on the data line. The card may become busy after receiving these commands based on its state prior to the command reception. The Host shall check for busy at the response.

6.4.3 R2 (CID, CSD register)

Code length is 136 bits. The contents of the CID register are sent as a response to the commands CMD2 and CMD10. The contents of the CSD register are sent as a response to CMD9. Only the bits [127...1] of the CID and CSD are transferred, the reserved bit [0] of these registers is replaced by the end bit of the response.

Bit position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	reserved	CID or CSD register incl. internal CRC7	end bit

Table 6-4-3: Response R2

6.4.4 R3 (OCR Register)

Code length is 48 bits. The contents of the OCR register are sent as a response to ACMD41.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	reserved	OCR register	reserved	end bit

Table 6-4-4: Response R3

6.4.5 R6 (Published RCA response)

Code length is 48 bit. The bits 45:40 indicate the index of the command to be responded to - in that case, it will be '000011' (together with bit 5 in the status bits it means = CMD3). The 16 MSB bits of the argument field are used for the Published RCA number.

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	x	x	x	x	'1'
Description	start bit	transmission bit	command index ('000011')	New published RCA [31:16] of the card	[15:0] card status bits: 23,22,19,12:0 (see Table 4-36)	CRC7	end bit

Table 6-4-5: Response R6

6.4.6 R7 (Card interface condition)

Code length is 48 bits. The card support voltage information is sent by the response of CMD8. Bits 19-16 indicate the voltage range that the card supports. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument.

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	'0'	'0'	'001000'	'00000h'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Reserved bits	Voltage accepted	Echo-back of check pattern	CRC7	End bit

Table 6-4-6: Response R7

Voltage accepted	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

Table 6-4-61 shows the format of 'voltage accepted' in R7.

6.5 SD Card Status

The SD Memory Card supports two status fields as follows:
- '*Card Status*': Error and state information of a executed command, indicated in the response
- *'SD Status*': Extended status field of 512 bits that supports special features of the SD Memory Card and future Application-Specific features.

6.5.1 Card Status

The response format R1 contains a 32-bit field named *card status*. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command. The semantics of this register is according to the CSD entry SPEC_VERS, indicating the version of the response formats (possibly used for later extensions). Table 6-19 defines the different entries of the status. The type and clear condition fields in the table are abbreviated as follows:

- **Type:**

E: Error bit.
S: Status bit.
R: Detected and set for the actual command response.

X: Detected and set during command execution. The host must poll the card by issuing the status command in order to read these bits.

• **Clear Condition:**

A: According to the card current state.
B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
C: Clear by read.

Bits	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R X	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	E R X	'0'= no error '1'= error	A misaligned address which did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R X	'0'= no error '1'= error	The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E R X	'0'= no error '1'= error	An invalid selection of write-blocks for erase occurred.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	Attempt to program a write protected block.	C
25	CARD_IS_LOCKED	S X	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A
24	LOCK_UNLOCK_ FAILED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command.	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card state	B
24	LOCK_UNLOCK_ FAILED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command.	C
21	CARD_ECC_FAILED	E R X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E R X	'0'= no error '1'= error	Internal card controller error	C
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
17,18	reserved				
16	CSD_OVERWRITE	E R X	'0'= no error '1'= error	can be either one of the following errors: - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C

15	WP_ERASE_SKIP	S X	'0'= not protected '1'= protected	Only partial address space was erased due to existing write protected blocks.	C
14	CARD_ECC_DISABLED	S X	'0'= enabled 1'= disabled	The command has been executed without using the internal ECC.	A
13	ERASE_RESET	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C
12:9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data; 6 = rcv; 7 = prg 8 = dis 9-14 = reserved 15 = reserved	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	'0'= not ready '1'= ready	corresponds to buffer empty signaling on the bus	A
7,6	reserved				
5	APP_CMD	S R	'0' = Disabled '1' = Enabled	The card will expect ACMD, or indication that the command has been interpreted as ACMD	C
4	reserved				
3	AKE_SEQ_ERROR	E R	'0' = no error '1' = error	Error in the sequence of authentication process	
2,1,0	reserved				

Table 6-5-1: Card status

The following table defines for each command responded by a R1 response the affected bits in the status field. An 'x' means the error/status bit may be set in the response to the respective command.

CMD#	Response Format 1 Status bit #																					
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :9	8	5
3									x	x			x							x		
6	x						x		x	x	x	x	x	x	x					x		
7					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
12	x	x				x	x		x	x	x	x	x	x	x			x		x		
13	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	
16			x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
17	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
18	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
24	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
25	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
26					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
27					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
28	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
29	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
30	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
32	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
33	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
38				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
42					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
55					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
56					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ACMD6	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD13					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD22					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD23					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD42					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD51					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x

Table 6-5-2: Card status field / command - cross reference

6.5.2 SD Status

The SD Status contains status bits that are related to the SD Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16 bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in '*tran_state*' (card is selected). SD Status structure is described in bellow. The same abbreviation for 'type' and 'clear condition' were used as for the Card Status above.

Bits	Identifier	Type	Value	Description	Clear Condi-tion
511: 510	DAT_BUS_WIDTH	S R	'00'= 1 (default) '01'= reserved '10'= 4 bit width '11'= reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command	A
509	SECURED_MODE	S R	'0'= Not in the mode '1'= In Secured Mode	Card is in Secured Mode of operation	A
508: 496	reserved				
495: 480	SD_CARD_TYPE	SR	'00xxh'= SD Memory Cards as defined in Physical Spec Ver1.01-2.00 ('x'=don't care). The following cards are currently defined: '0000'= Regular SD RD/WR Card. '0001'= SD ROM Card	In the future, the 8 LSBs will be used to define different variations of an SD Memory Card (Each bit will define different SD Types). The 8 MSBs will be used to define SD Cards that do not comply with current	A
479: 448	SIZE_OF_PROTEC TED_AREA	SR	in units of MULT*BLOCK_LEN refer to CSD register	The actual area = (SIZE_OF_PROTECTED_AREA) * MULT * BLOCK_LEN.	A
447: 440	SPEED_CLASS	SR	Speed Class of the card (See below)	(See below)	A
439: 432	PERFORMANCE_M OVE	SR	Performance of move indicated by 1 [MB/s] step. (See below)	(See below)	A
431: 428	AU_SIZE	SR	Size of AU (See below)	(See below)	A
427:	reserved				
424					
423: 408	ERASE_SIZE	SR	Number of AUs to be erased at a time	(See below)	A
407: 402	ERASE_TIMEOUT	SR	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See below)	A
401: 400	ERASE_OFFSET	SR	Fixed offset value added to erase time.	(See below)	A
399:312	reserved				
311:0	reserved				

Table 6-5-3: SD Card Status

• SIZE_OF_PROTECTED_AREA

Setting this field differs between Standard and High Capacity Cards.
In the case of a Standard Capacity Card, the capacity of protected area is calculated as follows:
Protected Area = SIZE_OF_PROTECTED_AREA_* MULT * BLOCK_LEN.
SIZE_OF_PROTECTED_AREA is specified by the unit in MULT*BLOCK_LEN.
In the case of a High Capacity Card, the capacity of protected area is specified in this field:
Protected Area = SIZE_OF_PROTECTED_AREA
SIZE_OF_PROTECTED_AREA is specified by the unit in byte.

• SPEED_CLASS

This 8-bit field indicates the Speed Class and the value can be calculated by Pw/2.

SPEED_CLASS	Value Definition
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h – FFh	Reserved

Table 6-5-4: Speed Class Code Field

• PERFORMANCE_MOVE

This 8-bit field indicates Pm and the value can be set by 1 [MB/sec] step. If the card does not move used RUs, Pm should be considered as infinity. Setting to FFh means infinity. The minimum value of Pm
is defined by in Table 6-21.

PERFORMANCE_MOVE	Value Definition
00h	Not Defined
01h	1 [MB/sec]
02h	2 [MB/sec]
…….	……
FEh	254 [MB/sec]
FFh	Infinity

Table 6-5-5: Performance Move Field

• **AU_SIZE**

This 4-bit field indicates AU Size and the value can be selected in power of 2 from 16 KB.

AU_SIZE	Value Definition
0h	Not Defined
1h	16 KB
2h	32 KB
3h	64 KB
4h	128 KB
5h	256 KB
6h	512 KB
7h	1 MB
8h	2 MB
9h	4 MB
Ah – Fh	Reserved

Table 6-5-6: AU_SIZE Field

The maximum AU size, depends on the card capacity, is defined in
Table 6-23. The card can set any AU size between RU size and maximum AU size.

Capacity	16 MB – 64 MB	128 MB-256 MB	512 MB	1 GB – 32 GB
Maximum AU Size	512 KB	1 MB	2 MB	4 MB

Table 6-5-7: Maximum AU size

• **ERASE_SIZE**

This 16-bit field indicates NERASE. When NERASE numbers of AUs are erased, the timeout value is specified by ERASE_TIMEOUT (Refer to ERASE_TIMEOUT). The host should determine proper number of AUs to be erased in one operation so that the host can indicate progress of erase operation. If this field is set to 0, the erase timeout calculation is not supported.

ERASE_SIZE	Value Definition
0000h	Erase Time-out Calculation is not supported.
0001h	1 AU
0002	2 AU
0003	3 AU
…….	…….
FFFFh	65535 AU

Table 6-5-8: Erase Size Field

• **ERASE_TIMEOUT**

This 6-bit field indicates the TERASE and the value indicates erase timeout from offset when multiple AUs are erased as specified by ERASE_SIZE. The range of ERASE_TIMEOUT can be defined as up to 63 seconds and the card manufacturer can choose any combination of ERASE_SIZE and ERASE_TIMEOUT depending on the implementation. Once ERASE_TIMEOUT is determined, it determines the ERASE_SIZE. The host can determine timeout for any number of AU erase by the Equation (6). Refer to 4.14 for the concept of calculating erase timeout. If ERASE_SIZE field is set to 0, this field shall be set to 0.

ERASE_TIMEOUT	Value Definition
00	Erase Time-out Calculation is not supported.
01	1 [sec]
02	2 [sec]
03	3 [sec]
…….	…….
63	63 [sec]

Table 6-5-9: Erase Timeout Field

• **ERASE_OFFSET**

This 2-bit field indicates the TOFFSET and one of four values can be selected. The erase offset adjusts the line by moving in parallel on the upper side. Refer to Figure 4-33 and Equation (6) in 4.14. This field is meaningless if ERASE_SIZE and ERASE_TIMEOUT fields are set to 0.

ERASE_OFFSET	Value Definition
0h	0 [sec]
1h	1 [sec]
2h	2 [sec]
3h	3 [sec]

Table 6-5-10: Erase Offset Field

6.6 Card Identification Mode and Data Transfer Mode

Two operation modes are defined for the SD Card system:

• Card identification mode

The host will be in card identification mode after reset and while it is looking for new cards on the bus. Cards will be in this mode after reset until the SEND_RCA command (CMD3) is received.

• Data transfer mode

Cards will enter data transfer mode once their RCA is first published. The host will enter data transfer mode after identifying all the cards on the bus. The following table shows the dependencies between operation modes and card states. Each state in the SD Card state diagram (see Figure 6-8) is associated with one operation mode:

Card state	Operation mode
Inactive State	inactive
Idle State	card identification mode
Ready State	
Identification State	
Stand-by State	data transfer mode
Transfer State	
Sending-data State	
Receive-data State	
Programming State	
Disconnect State	

Table 6-6-1: Overview of Card States vs. Operation modes

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only.

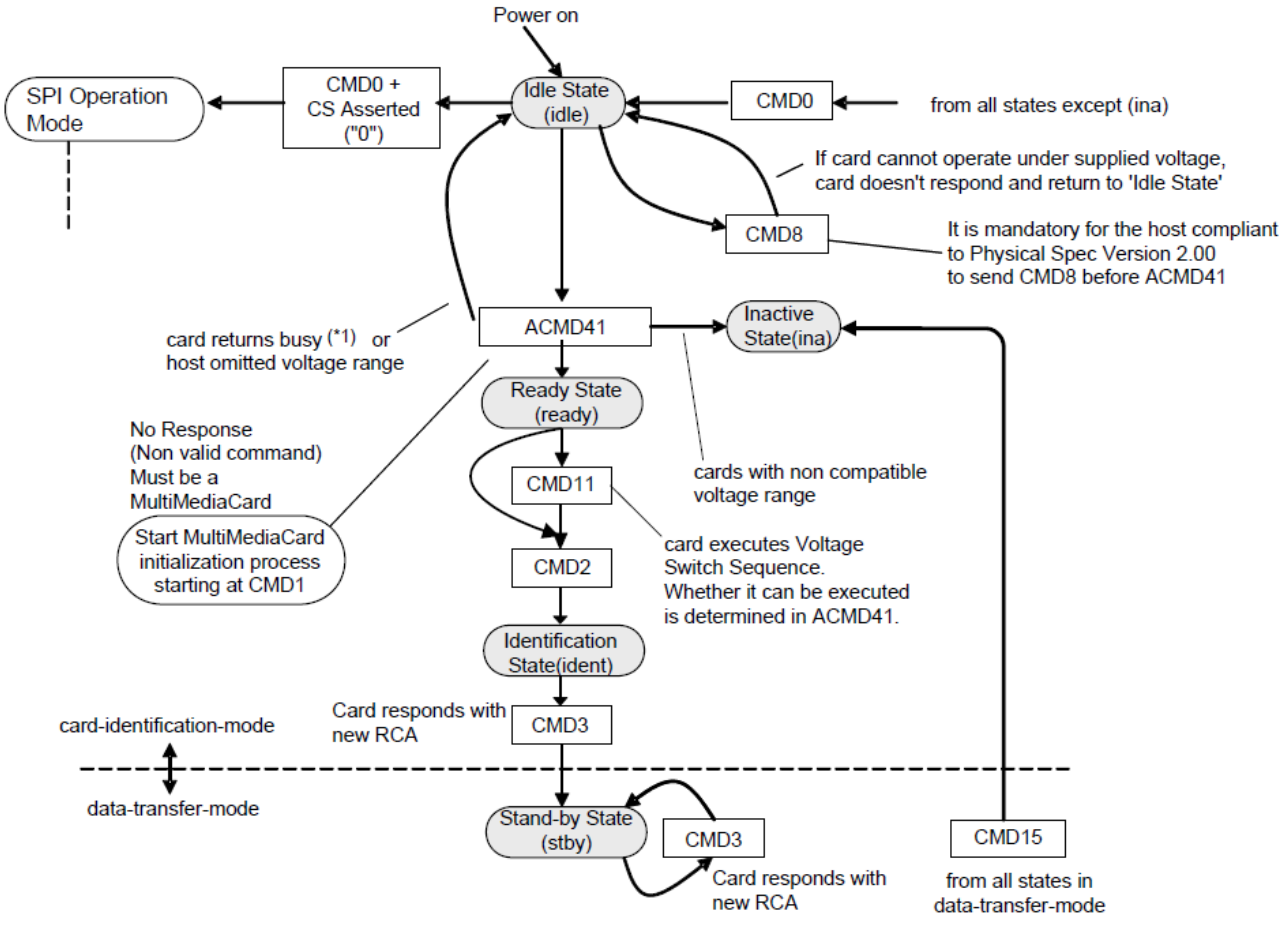
6.6.1 Card Identification Mode

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only. During the card identification process, the card shall operate in the SD clock frequency of the identification clock rate fOD.

The command GO_IDLE_STATE (CMD0) is the software reset command and sets each card into Idle State regardless of the current card state. Cards in Inactive State are not affected by this command. After power-on by the host, all cards are in Idle State, including the cards that have been in Inactive State before.
After power-on or CMD0, all cards' CMD lines are in input mode, waiting for start bit of the next command.
The cards are initialized with a default relative card address (RCA=0x0000) and with a default driver strength with 400KHz clock frequency. In case of 3.3V signaling, default driver strength is specified by the Driver Stage Register (DSR) if supported and selected highest driving current capability. In case of 1.8V signaling, default driver strength is specified by type B driver.

At the start of communication between the host and the card, the host may not know the card supported voltage and the card may not know whether it supports the current supplied voltage. The host issues a reset command (CMD0) with a specified voltage while assuming it may be supported by the card. To verify the voltage, a following new command (CMD8) is defined in the Physical Layer Specification Version 2.00. SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. The supplied voltage is indicated by VHS filed in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be set to 1 at any given time. Both CRC and check pattern are used for the host to check validity of communication between the host and the card.
If the card can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument. If the card cannot operate on the supplied voltage, it returns no response and stays in idle state. It is mandatory to issue CMD8 prior to first ACMD41 to initialize SDHC or SDXC Card.
Receipt of CMD8 makes the cards realize that the host supports the Physical Layer Version 2.00 or later and the card can enable new functions. SD_SEND_OP_COND (ACMD41) is designed to provide SD Memory Card hosts with a mechanism to identify and reject cards which do not match the VDD range desired by the host. This is accomplished by the host sending the required VDD voltage window as the operand of this command.
Cards which cannot perform data transfer in the specified range shall discard themselves from further bus operations and go into Inactive State. The levels in the OCR register shall be defined accordingly Note that ACMD41 is application specific command; therefore APP_CMD (CMD55) shall always precede ACMD41. The RCA to be used for CMD55 in idle_state shall be the card's default RCA = 0x0000.
After the host issues a reset command (CMD0) to reset the card, the host shall issue CMD8 prior to ACMD41 to re-initialize the SD Memory card

By setting the OCR to zero in the argument of ACMD41, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State (query mode). This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired. The card does not start initialization and ignores HCS in the argument if ACMD41 is issued as a query. Afterwards, the host may choose a voltage for operation and reissue ACMD41 with this condition, sending incompatible cards into the Inactive State.
During the initialization procedure, the host is not allowed to change the operating voltage range.



(*1) Note: Card returns busy when
- Card executes internal initialization process
- Card is High or Extended capacity SD Memory Card and host doesn't support High or Extended capacity
  This means that CMD8 is mandatory to initialize High capacity SD Memory Card

Figure 6-6-1: SD memory card diagram

6.6.2 Card Initialization and Identification Process

Inactive State Inactive State Inactive State Ready
State Identification State Stand-by State.
After the bus is activated the host starts card initialization and identification process (See Figure 6-6-2).
The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports SDHC or SDXC Card. The HCS (Host Capacity Support) bit set to 0 indicates that the host supports neither SDHC nor SDXC Card.
Receiving of CMD8 expands the ACMD41 function; HCS in the argument and CCS (Card Capacity Status) in the response. HCS is ignored by cards, which didn't respond to CMD8. However the host should set HCS to 0 if the card returns no response to CMD8. Standard Capacity SD Memory Card ignores HCS. If HCS is set to 0, SDHC and SDXC Cards never return ready status (keep busy bit to 0).
The busy bit in the OCR is used by the card to inform the host whether initialization of ACMD41 is completed. Setting the busy bit to 0 indicates that the card is still initializing. Setting the busy bit to 1 indicates completion of initialization. Card initialization shall be completed within 1 second from the first
ACMD41. The host repeatedly issues ACMD41 for at least 1 second or until the busy bit are set to 1.
The card checks the operational conditions and the HCS bit in the OCR only at the first ACMD41 with setting voltage window in the argument. While repeating ACMD41, the host shall not issue another command except CMD0.
If the card responds to CMD8, the response of ACMD41 includes the CCS field information. CCS is valid when the card returns ready (the busy bit is set to 1). CCS=0 means that the card is SDSC.
CCS=1 means that the card is SDHC or SDXC.
The host performs the same initialization sequence to all of the new cards in the system. Incompatible cards are sent into *Inactive State*. The host then issues the command ALL_SEND_CID (CMD2), to each card to get its unique card identification (CID) number. Card that is unidentified (i.e. which is in *Ready State*) sends its CID number as the response (on the CMD line). After the CID was sent by the card it goes into *Identification State*. Thereafter, the host issues CMD3 (SEND_RELATIVE_ADDR) asks the card to publish a new relative card address (RCA), which is shorter than CID and which is used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the *Stand-by State.* At this point, if the host wants to assign another RCA number, it can ask the card to publish a new number by sending another CMD3 command to the card. The last published RCA is the actual RCA number of the card.
The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 for each card in the system.
Initialization of SDXC is identical to SDHC. User area capacity of SDXC card is specified by C_SIZE and it shall be more than or equal to 32GB.

Application Notes:
The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

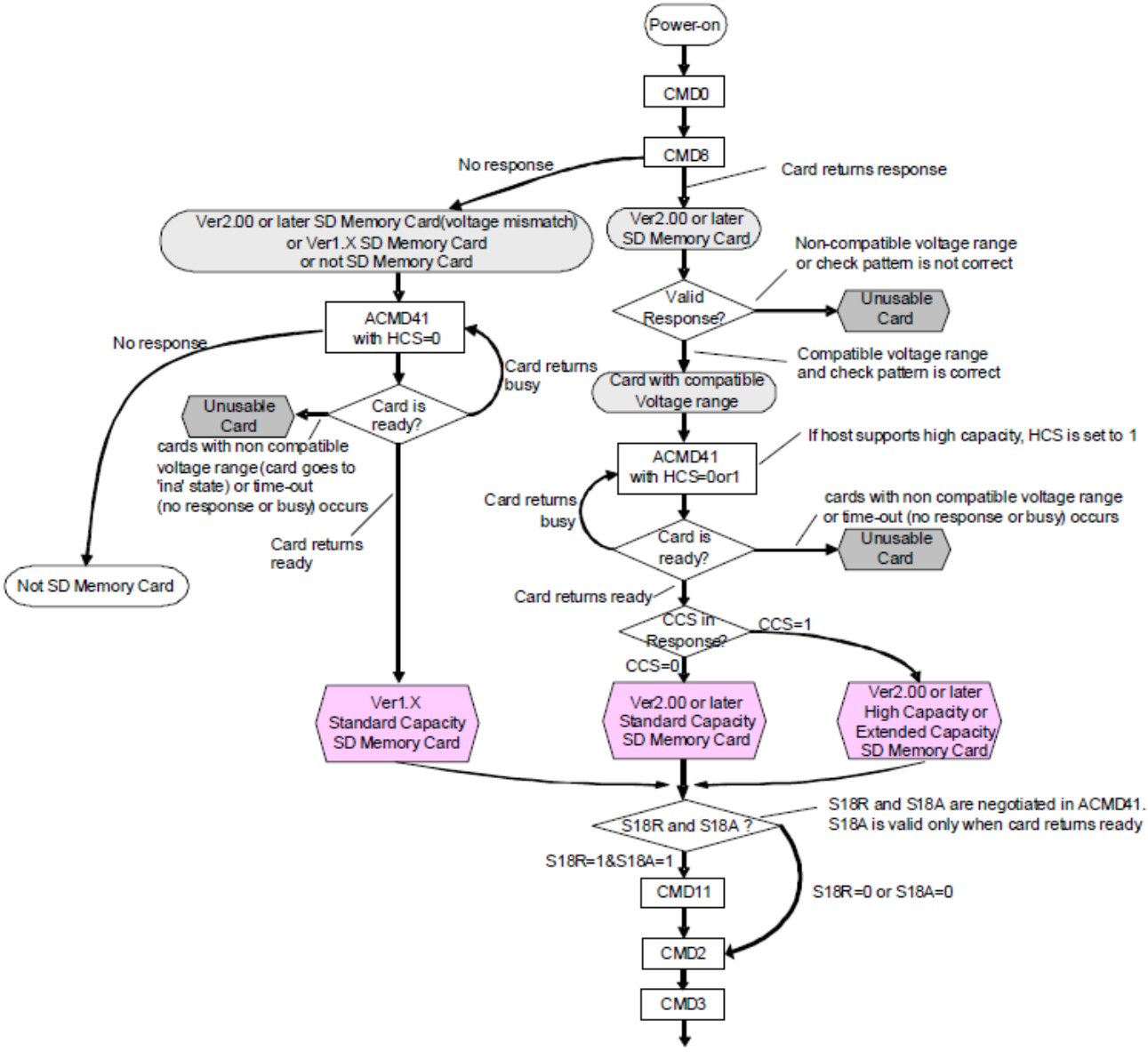
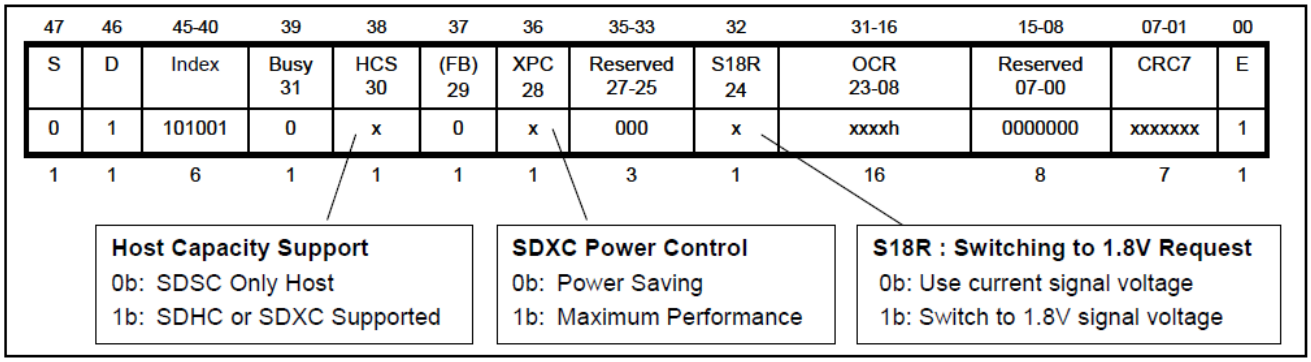


Figure 6-6-2: Card Initialization and Identification Flow (SD mode)

6.6.3 Initialization Command (ACMD41)

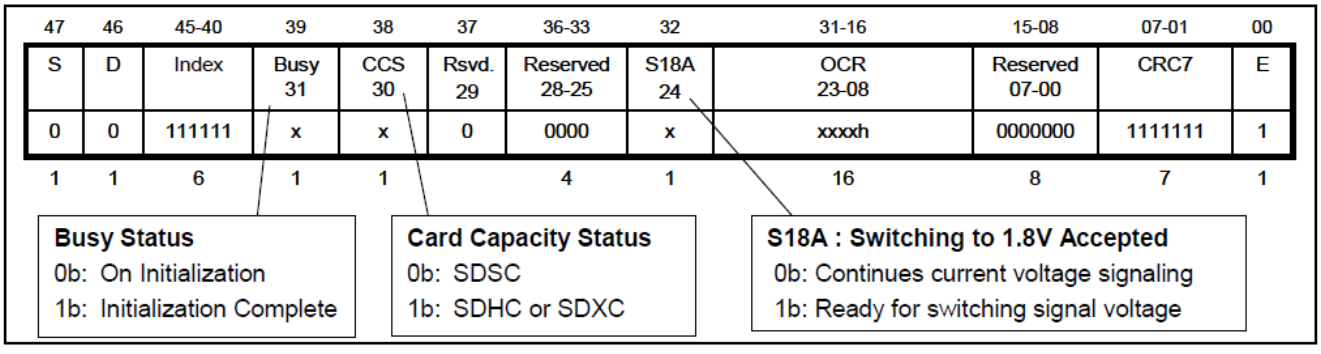
Followings are general rules of the argument of ACMD41:
(1) If the voltage window field (bit 23-0) in the argument is set to zero, it is called "inquiry CMD41" that does not start initialization and is use for getting OCR. The inquiry ACMD41 shall ignore the other field (bit 31-24) in the argument.
(2) If the voltage window field (bit 23-0) in the argument is set to non-zero at the first time, it is called "first ACMD41" that starts initialization. The other field (bit 31-24) in the argument is effective.
(3) The argument of following ACMD41 shall be the same as that of the first ACMD41. Figure 6-6-3 shows argument format and Figure 6-6-4 shows response format. Two new fields are added to the argument of ACMD41.
If a SDXC Card is initialized with XPC=0, the card is operating less than 100mA in Default Speed or SDR12, and if the card does not support Speed Class, Class 0 is indicated in SD Status. If a SDXC Card is initialized with XPC=1, the card is operating less than 150mA in Default Speed or SDR12, and the card supports Speed Class. Re-initialization is required to change XPC selection. UHS-I supported host sets S18R=1 in the argument of ACMD41 to request the card to switch 1.8V signaling level. UHS-I supports card respond with S18A=1 in the response of ACMD41 and then host can issue voltage switch command.

(1) Argument of ACMD41



Note: Fast Boot (Bit 29) is reserved for eSD

Figure 6-6-3: Argument of ACMD41



CCS (Bit 30) and S18A (Bit 24) are valid when Busy (Bit 31) is set to 1.

Figure 6-6-4: Response of ACMD41

6.6.4 Bus Signal Voltage Switch Sequence

Figure 6-6-5 shows sequence of commands to perform voltage switch and Figure 6-6-6 shows initialization flow chart for UHS-I hosts. Red and yellow boxes are new procedure to initialize UHS-I card.

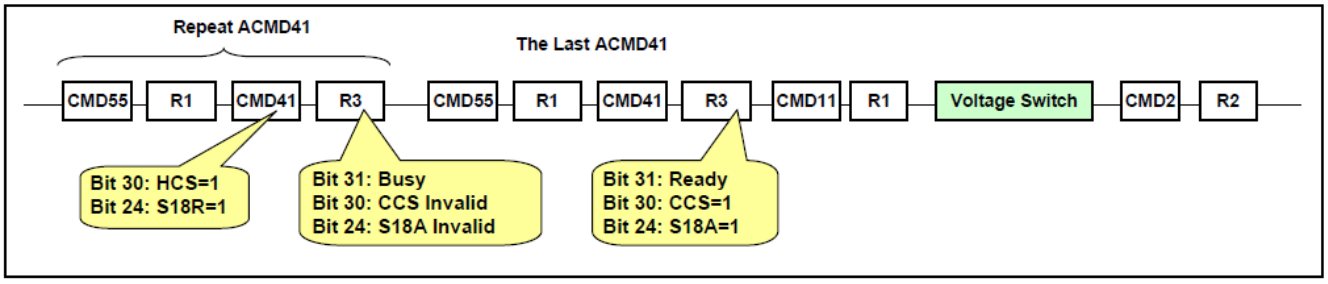


Figure 6-6-5 : ACMD41 Timing Followed by Voltage Switch Sequence

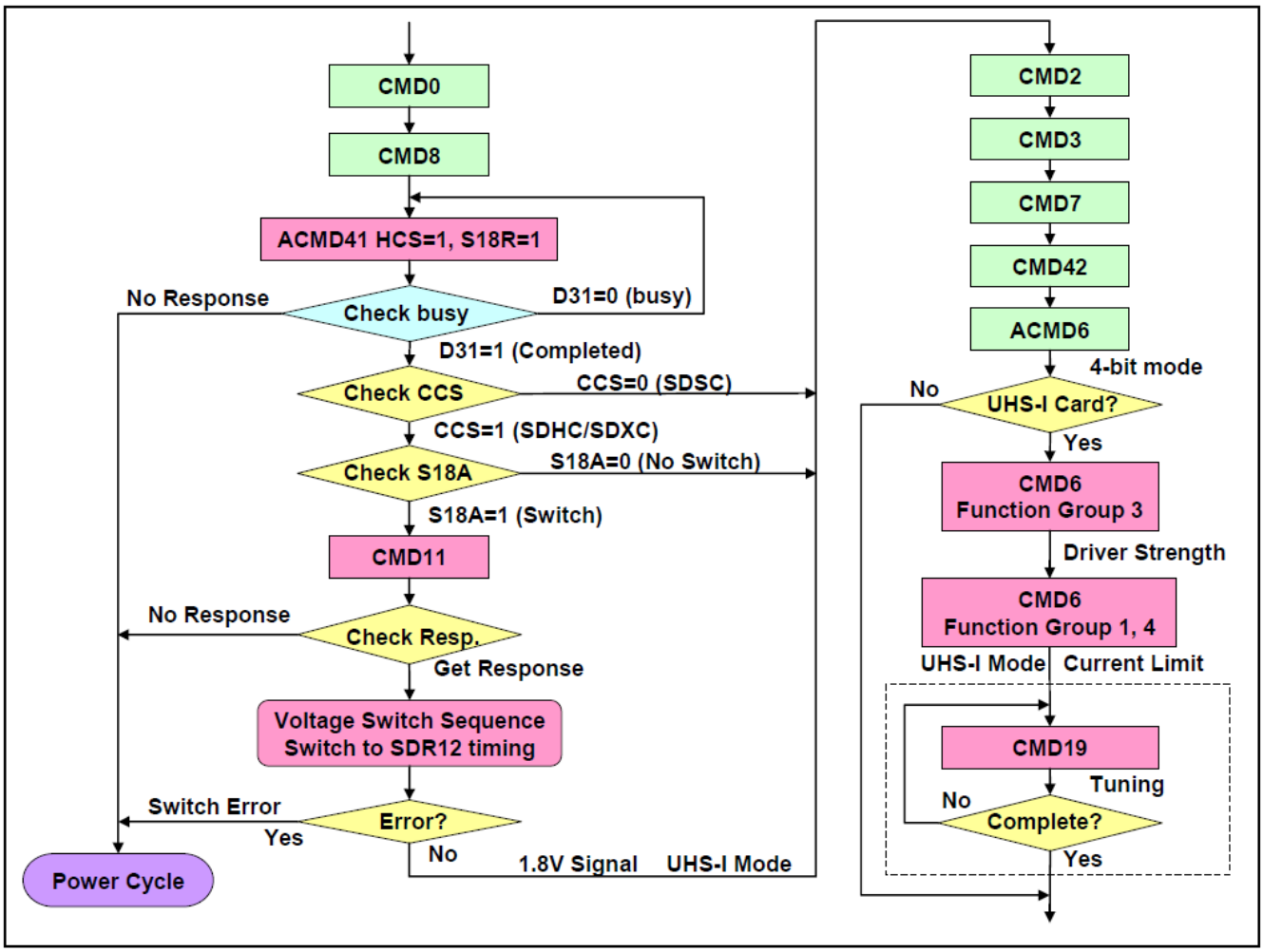


Figure 6-6-6 : UHS-I Host Initialization Flow Chart

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument. If Bit 31 indicates ready, host needs to check CCS and S18A. The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level. S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence. By receiving CMD11, the card returns R1 response and start voltage switch sequence. No response of CMD11 means that S18A was 0 and therefore host should not

DAT[3:0] can be checked depends on ability of the host. When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7). If the card is locked, CMD42 is required to unlock the card. If the card is unlocked, CMD42 can be skipped.
In case of UHS-I card, appropriate driver strength is selected by CMD6 Function Group 3 and one of UHS-I modes is selected by CMD6 Function Group 1.
In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed.

6.6.5 Timing to Switch Signal Voltage

Clock frequency range shall be 100 KHz-400 KHz during initialization sequence. Table 6-6-2 shows command (S18R) – response (S18A) combinations to switch signal voltage in ACMD41. S18A is defined in the command argument and indicates signal voltage switch acceptance by the card (voltage is not switched here). If signaling level is already 1.8V, S18R is ignored and signal voltage switch sequence is not started. S18A=0 means that current signaling level is maintained. Refer to Section 6.6.4 about new fields defined in ACMD41.

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

Table 6-6-2: S18R and S18A Combinations

To change signaling level at the same time between host card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 6-6-7. CMD11 is issued only when S18A=1 in the response of ACMD41.

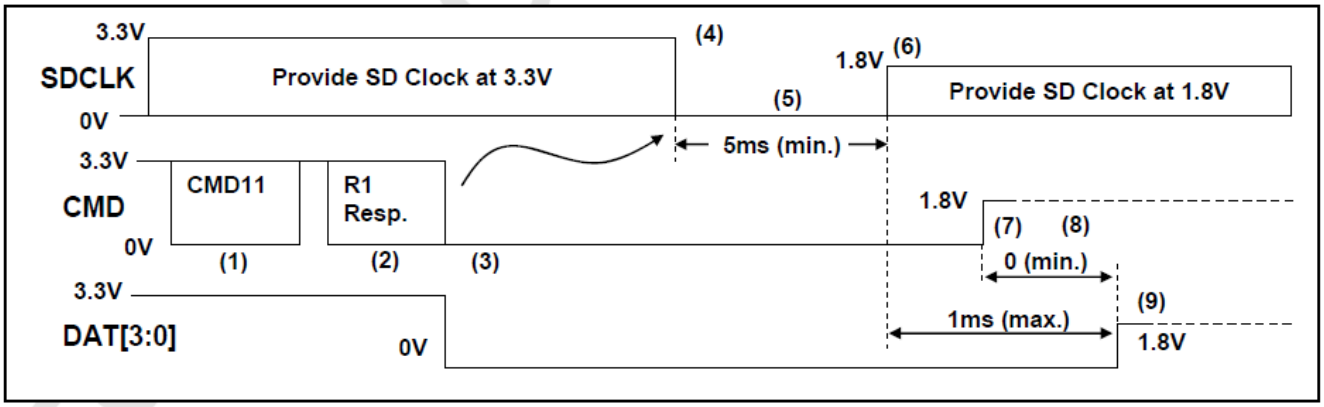


Figure 6-6-7: Signal Voltage Switch Sequence

(1) Host issues CMD11 to start voltage switch sequence.
(2) The card returns R1 response.
(3) The card drives CMD and DAT[3:0] to low immediately after the response.
(4) The host stops supplying SDCLK. The card shall start switching voltage after host stops SDCLK.
The time to stops SDCLK is not specified.
The host can detect whether the sequence starts by checking signal level of either one of CMD, DAT[3:0]. Which signal should be checked depends on ability of the host. If low level is not detected, the host should abort the sequence and execute power cycle.
(5) 1.8V output of voltage regulator in card shall be stable within 5ms. Host keeps SDCLK low at least **5ms.** This means that 5ms is the maximum for the card and the minimum for the host.
(6) After 5ms from (4) and host voltage regulator is stable, the host starts providing SDCLK at 1.8V.

The card can check whether SDCLK voltage is 1.8V.
(7) By detecting SDCLK, the card drives CMD to high at 1.8v at least one clock and then stop driving (tri-state). CMD is triggered by rising edge of SDCLK (SDR timing).
(8) The card can check whether host drives CMD to 1.8V through the host pull-up resister.
(9) If switching to 1.8V signaling is completed successfully, the card drives DAT[3:0] to high at 1.8V at least one clock and then stop driving (tri-state). DAT[3:0] is triggered by rising edge of SDCLK (SDR timing). DAT[3:0] shall be high within **1ms** from start of providing SDCLK. Host check whether DAT[3:0] is high after 1ms from supplying SDCLK. This means that 1ms is the maximum for the card and minimum for the host.

SD clock is provided at either 3.3V or 1.8V before and after period (5) and its frequency is 100KHz-400KHz. Stopping clock is allowed only in the period (5) during voltage switching sequence.
After the sequence is completed, the host and the card start communication in SDR12 timing.

6.6.6 Timing of Voltage Switch Error Detection

Figure 6-6-8 shows the timing when an error occurs during signal voltage switch sequence.

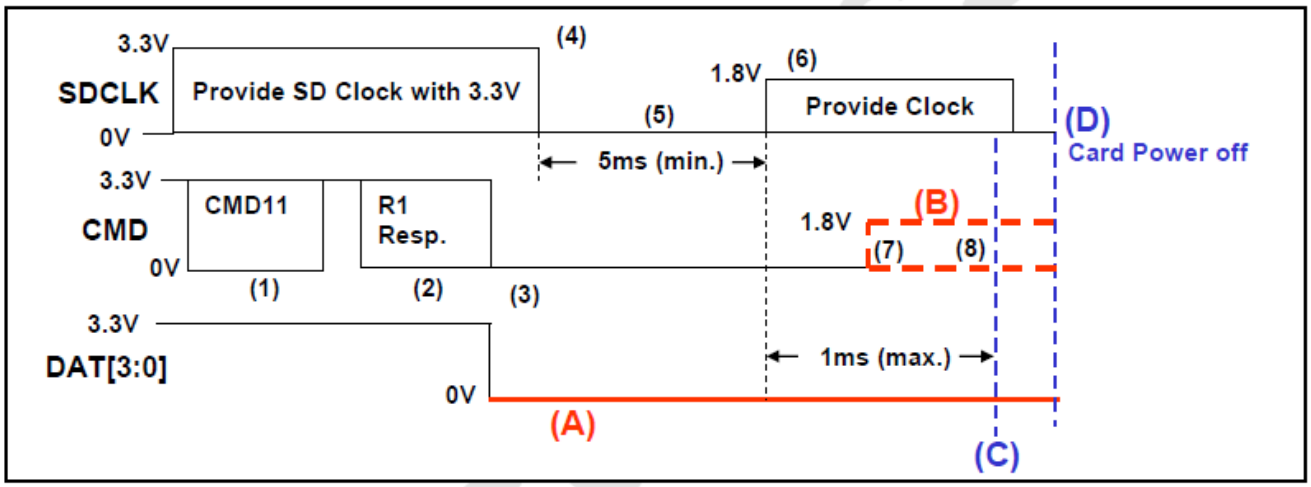


Figure 6-6-8: Error Indication Timing

(A) If the card detects voltage error at any point in (5)-(8), the card keeps driving DAT[3:0] to low until card power off.
(B) CMD may be low or tri-state.
(C) The host checks whether DAT[3:0] is high after **1ms** from starting to provide SDCLK.
(D) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

The card shall check voltages of own regulator output and host signals to be less than 2.5V. Error occurrences are indicated by (A) and (B).

6.6.7 Voltage Switch Command

Figure 6-6-9 shows Voltage Switch Command (CMD11) definition. CMD11 can be executed in ready state and doesn't change the state. Even if the card is locked, CMD11 can be executed. Returning R1 type response means the card starts voltage switch sequence. If the host detects no response, power cycle should be executed.
There are four cases that the card indicates no response to CMD11.
(1) The card does not support voltage switch.
(2) The card supports voltage switch but ACMD41 is received with S18R=0.
(3) The card receives CMD11 not in ready state.
(4) Signaling level is already switched to 1.8V.
For all above cases, CMD11 is treated as an illegal command.

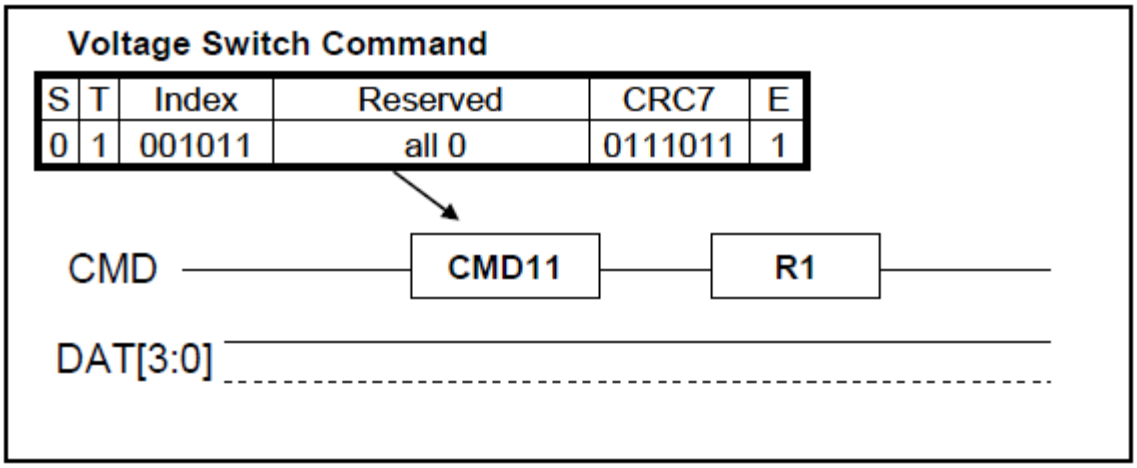


Figure 6-6-9 : Voltage Switch Command

6.6.8 Tuning Command

Tuning capability of sampling point is mandatory for HOST-SDR-VD and optional for HOST-SDR-FD.
This procedure gives the system optimal timing for each specific host and card combination and compensates for static delays in the timing budget including process, voltage and different PCB loads and skews.
CMD19 is defined for Send Tuning Block Command. R1 type response is defined. CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command. Data block, carried by DAT[3:0], contains a pattern for tuning sampling position to receive data on the CMD and DAT[3:0] line. The block length of CMD19 is fixed and CMD16 is not required

The tuning command (CMD19) follows the timing of the single block read command as described in Figure 6-6-10.

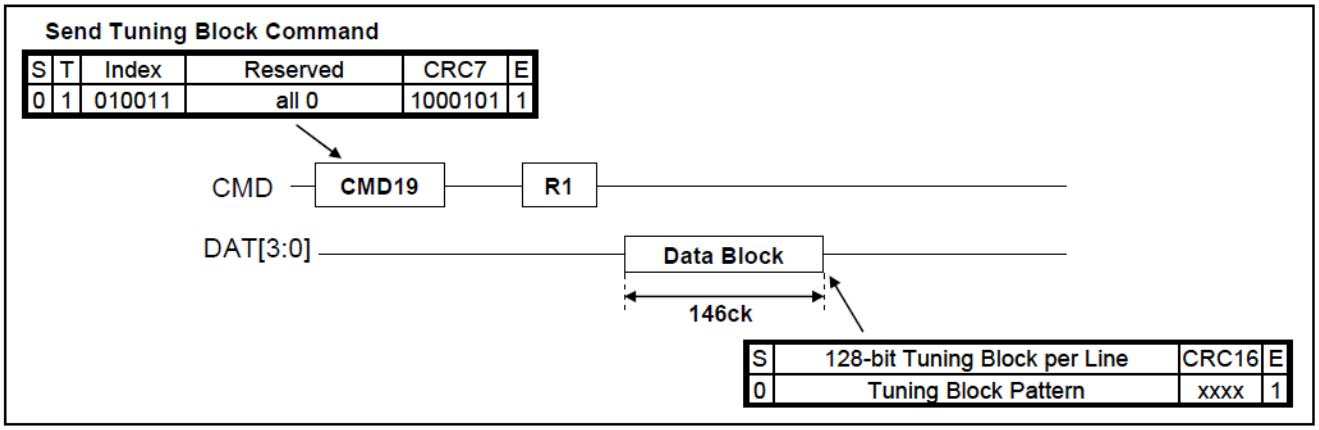


Figure 6-6-10: Send Tuning Block Command

This sequence is defined as multiple, consecutive executions of CMD19 that are sent from the host and responded by the card, without any other command mixed between them.
The card shall complete a sequence of 40 times CMD19 executions in no more than 150ms. The tuning process is normally shorter than 40 executions of CMD19, and therefore should be shorter than 150 ms.
The sequence period definition does not include any host processing time. If host needs time to process CMD19 between executions, the sequence may be longer by this amount of time.

6.6.9 Data Transfer Mode

Until the end of Card Identification Mode the host shall remain at fOD frequency because some cards may have operating frequency restrictions during the card identification mode. In Data Transfer Mode the host may operate the card in fPP frequency range. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc.
The broadcast command SET_DSR (CMD4) configures the driver stages of all identified cards. It programs their DSR registers corresponding to the application bus layout (length) and the number of cards on the bus and the data transfer frequency. The clock rate is also switched from fOD to fPP at that point. SET_DSR command is an option for the card and the host.
CMD7 is used to select one card and put it into the *Transfer State*. Only one card can be in the *Transfer State* at a given time. If a previously selected card is in the *Transfer State* its connection with the host is released and it will move back to the *Stand-by State*. When CMD7 is issued with the reserved relative card address "0x0000", all cards are put back to *Stand-by State* (Note that it is the responsibility of the Host to reserve the RCA=0 for card de-selection - refer to CMD7.

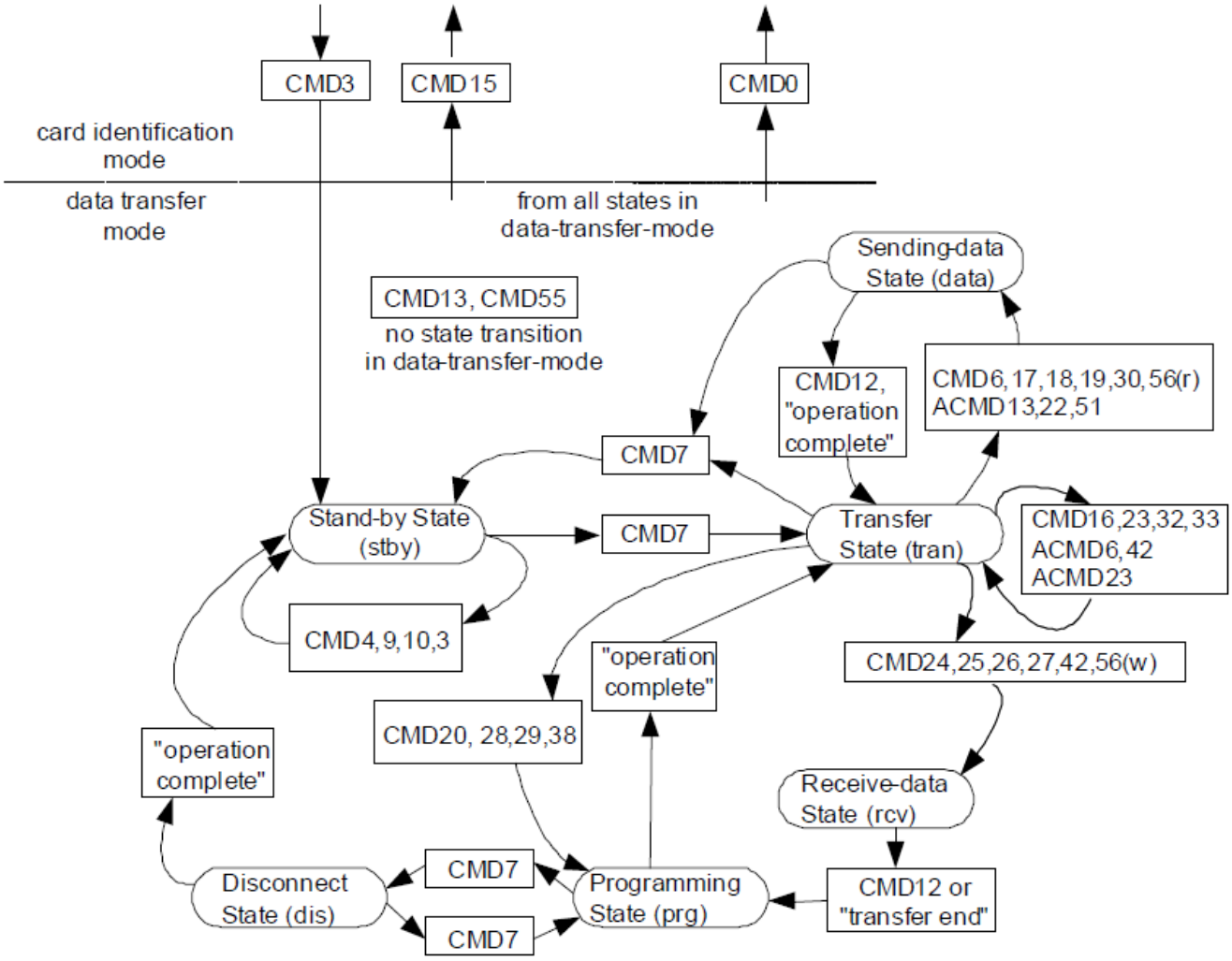


Figure 6-6-11: SD Memory Card State Diagram (data transfer mode)

This may be used before identifying new cards without resetting other already registered cards. Cards which already have an RCA do not respond to identification commands (ACMD41, CMD2, see Chapter 6.6) in this state.

Important Note: The card de-selection is done if certain card gets CMD7 with un-matched RCA. That happens automatically if selection is done to another card and the CMD lines are common. So, in SD Memory Card system it will be the responsibility of the host either to work with common CMD line (after initialization is done) - in that case the card de-selection will be done automatically or if the CMD lines are separate then the host shall be aware to the necessity to de-select cards.

All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

6.7 Write Protect Management

Three write protect methods are supported in the SD Memory Card as follows:
- Mechanical write protect switch (Host responsibility only)
- Card internal write protect (Card's responsibility)

- Password protection card lock operation.

6.7.1 Mechanical Write Protect Switch

A mechanical sliding tablet on the side of the card (refer to the Part 1 Mechanical Addenda) will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the window is open it means that the card is write protected. If the window is close the card is not write-protected.
A proper, matched, switch on the socket side will indicate to the host that the card is write-protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is unknown to the internal circuitry of the card.

6.7.2 Card's Internal Write Protection (Optional)

Card data may be protected against either erase or write. The entire card may be permanently write-protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. For cards which support write protection of groups of sectors by setting the WP_GRP_ENABLE bit in the CSD, portions of the data may be protected (in units of WP_GRP_SIZE sectors as specified in the CSD), and the write protection may be changed by the application. The SET_WRITE_PROT command sets the wirte protection of the addressed write-protect group and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.
The SEND_WIRTE_PROT command is similar to single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The card will ignore all LSB's below the group size.
The Password Card Lock protection is described in the following section.
Note that SDHC and SDXC Cards do not support Write Protection and do not respond to wirte-protection commands (CMD28, CMD29 and CMD30)

6.7.3 Card Lock/Unlock Operation

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size are kept in a 128-bit PWD and 8-bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.
Locked cards respond to (and execute) all commands in the "basic" command class (class 0), ACMD41, CMD16 and "lock card" command class. Thus, the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0), the card will be locked automatically after power on.
Similar to the existing CSD register write commands, the lock/unlock command is available in "transfer state" only. This means that it does not include an address argument and the card shall be

selected before using it.
The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). Table 4-5 describes the structure of the command data block. Note that the host compliant to the Physical Specification Version 2.00 or later shall set reserved bits (Bit7-4) to 0 when issuing CMD42.

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved (shall be set to 0)				ERASE	LOCK_ UNLOCK	CLR_ PWD	SET_ PWD
1	PWDS_LEN							
2	Password data							
...								
PWDS_LEN + 1								

Table 6-7: Lock Card Data Structure

ERASE: 1 Defines Forced Erase Operation. In byte 0, bit 3 will be set to 1 (all other bits shall be 0). All other bytes of this command will be ignored by the card.

- **LOCK/UNLOCK**: 1 = Locks the card. 0 = Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).
- **CLR_PWD**: 1 = Clears PWD.
- **SET_PWD**: 1 = Set new password to PWD
- **PWDS_LEN**: Defines the following password(s) length (in bytes). In case of a password change, this field includes the total password lengths of old and new passwords. The password length is up to 16 bytes. In case of a password change, the total length of the old password and the new password can be up to 32 bytes.
- **Password data:** In case of setting a new password, it contains the new password. In case of a password change, it contains the old password followed by the new password. The data block size shall be defined by the host before it sends the card lock/unlock command. The block length shall be set to greater than or equal to the required data structure of the lock/unlock command. In the following explanation, changing block size by CMD16 is not a mandatory requirement for the lock/unlock command.

  Since block length shall always be even in DDR50 mode, the block length for CMD42 shall always be rounded up to an even size. If CMD16 is used prior to CMD42 to set the block length, it shall always specify an even length.

The following paragraphs define the various lock/unlock command sequences:

Setting the Password

- Select a card (CMD7), if not previously selected.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bits password size (in bytes), and the number of bytes of the new password. In the case that a password *replacement* is done, then the block size shall consider that both passwords-the old and the new one-are sent with the command.

• Send the Card Lock/Unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWDS_LEN) and the password itself. In the case that a password *replacement* is done, then the length value (PWDS_LEN) shall include both passwords (the old and the new one) and the password data field shall include the old password (currently used) followed by the new password. Note that the card shall handle the calculation of the new password length internally by subtracting the old password length from PWDS_LEN field.

• In the case that the sent old password is not correct (not equal in size and content), then the LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In the case that the sent old password is correct (equal in size and content), then the given new password and its size will be saved in the PWD and PWD_LEN registers, respectively.

Note that the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0, there is no password set. If the value of PWD_LEN is not equal to zero, the card will lock itself after power up. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending an additional command for card lock.

Reset the Password:

• Select a card (CMD7), if not previously selected.

• Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

• Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWDS_LEN), and the password itself. If the PWD and PWD_LEN content match the sent password and its size, then the content of the PWD register is cleared and PWD_LEN is set to 0. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

Locking the Card:

• Select a card (CMD7), if not previously selected.

• Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

• Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWDS_LEN) and the password itself.

If the PWD content is equal to the sent password, then the card will be locked and the card-locked status bit will be set in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

Note that it is possible to set the password and to lock the card in the same sequence. In such a case, the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent.

If the password was previously set (PWD_LEN is not 0), then the card will be locked automatically after

An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during a password definition or change operations.

Unlocking the Card:

- Select a card (CMD7), if not previously selected.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
- Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWDS_LEN) and the password itself.

If the PWD content is equal to the sent password, then the card will be unlocked and the card-locked
status bit will be cleared in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that unlocking is done only for the current power session. As long as the PWD is not cleared, the card will be locked automatically on the next power up. The only way to unlock the card is by clearing the password.
An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during a password definition or change operation.

Parameter and the Result of CMD42

The block length shall be greater than or equal to the required data structure of CMD42; otherwise, the result of CMD42 is undefined and the card may be in the unexpected locked state. Table 6-7 clarifies the behavior of CMD42. The reserved bits in the parameter (bit7-4) of CMD42 shall be don't care. In the case that CMD42 requires the password, it is assumed that the old password and the new password are set correctly; otherwise the card indicates an error regardless of Table 6-7. If the password length is 0 or greater than 128 bits, the card indicates an error. If errors occur during execution of CMD42, the LOCK_UNLOCK_FAILED (Bit24 of Card Status) shall be set to 1 regardless of Table 6-7. The CARD_IS_LOCKED (Bit25 of Card Status) in the response of CMD42 shall be the same as Current Card State in Table 6-7. In the field of Card Status, 0 to 1 means the card changes to Locked and 1 to 0 means the card changes to Unlocked after execution of CMD42. It can be seen in the response of CMD13 after the CMD42. The LOCK_UNLOCK_FAILED (Bit24 of Card Status) as the result of CMD42 can be seen in the response of either CMD42 or the following CMD13.

Commands Accepted for Locked Card

The locked card shall accept commands listed below and return response with setting CARD_IS_LOCKED.

1) Basic class (0)
2) Lock card class (7)
3) CMD16
4) ACMD41
5) ACMD42

All other commands including security commands are treated as illegal commands.

Note: CMD11 (Class 0) and CMD40 (Class 7) are new commands accepted in the locked card state. CMD40 is reserved for Security Specification.
Application Note:
After power on, the host can recognize the card lock/unlock state by the CARD_IS_LOCKED in the response of CMD7 or CMD13.

6.8 Error Handling

To correct defects in the memory field inside card the card include error correction codes in the payload data (ECC). This correction is intended to correct static errors. Additionally two methods of detecting errors generated during the data transfer (dynamic errors) via a cyclic redundancy check (CRC) are implemented

6.8.1 Error Correction Code (ECC)

The ATP SD Card is free of static errors. All errors are covered inside the card, even errors occurring during the lifetime of the card are covered for the user. The only effect which may be notified by the end user is, that the overall memory capacity may be reduced by small number of blocks. All flash handling is done on card, so that no external error correction is needed.

6.8.2 Cyclic Redundancy Check (CRC)

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block is generated. The CRC is generated and checked as described in the following.

- **CRC7**

The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:

generator polynomial: $G(x) = x^7 + x^3 + 1$.
$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$
$CRC[6...0] = \text{Remainder } [(M(x) * x^7) / G(x)]$

The first bit is the most left bit of the corresponding bit string (of the command, response, CID or CSD). The degree n of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

- **CRC16**

In case of one DAT line usage (as in MultiMediaCard) than the CRC16 is used for payload protection in block transfer mode. The CRC check sum is a 16-bit value and is computed as follows:

generator polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$
$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$
$CRC[15...0] = \text{Remainder } [(M(x) * x^{16}) / G(x)]$

The first bit is the first data bit of the corresponding block. The degree *n* of the polynomial denotes the number of bits of the data block decreased by one (e.g. n = 4095 for a block length of 512 bytes). The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2048 Bytes (n <= 16383). The same CRC16 method is used in single DAT line mode and in wide bus mode. In wide bus mode, the CRC16 is done on each line separately.

6.8.3 CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed card's CRC check fails, the card does not respond and the command is not executed. The card does not change its state, and COM_CRC_ERROR bit is set in the status register. Similarly, if an illegal command has been received, the card will not change its state, will not response and will set the ILLEGAL_COMMAND error bit in the status register. Only the non-erroneous state branches are shown in the state diagrams contains a complete state transition description.

There are different kinds of illegal commands:

• Commands which belong to classes not supported by the card (e.g. write commands in read only cards).
• Commands not allowed in the current state (e.g. CMD2 in Transfer State).
• Commands which are not defined (e.g. CMD5).

6.8.4 Read, Write and Erase Time-out

The times after which a time-out condition for read operations occurs are (card independent) **either 100 times longer** than the typical access times for these operations given below **or 100ms (the lower of them)**. The times after which a time-out condition for Write/Erase operations occurs are (card independent) **either 100 times longer** than the typical program times for these operations given below **or 250ms (the lower of them).** A card shall complete the command within this time period, or give up and return an error message. If the host does not get any response with the given time out it should assume the card is not going to respond anymore and try to recover (e.g. reset the card, power cycle, reject, etc.). The typical access and program times are defined as follows:

• Read

The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC . These card parameters define the typical delay between the end bit of the read command and the start bit of the data block. This number is card dependent and should be used by the host to calculate throughput and the maximal frequency for stream read.

- **Write**

The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write/erase commands (e.g. SET(CLR)_WRITE_PROTECT, PROGRAM_CSD and the block write commands).

- **Erase**

The duration of an erase command will be (order of magnitude) the number of write blocks (WRITE_BL) to be erased multiplied by the block write delay.

7.0 SPI Mode

7.1 Introduction

The SPI mode consists of a secondary communication protocol which is offered by SD Cards. This mode is a subset of the SD Card protocol, designed to communicate with a SPI channel, The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

7.2 SPI BUS Topology

The ATP SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the ATP SD Card SPI channel consists of the following four signals:

CS: Host to card Chip Select signal.

CLK: Host to card clock signal

DataIn: Host to card data signal.

DataOut: Card to host data signal.

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal (see Figure 7-1).

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

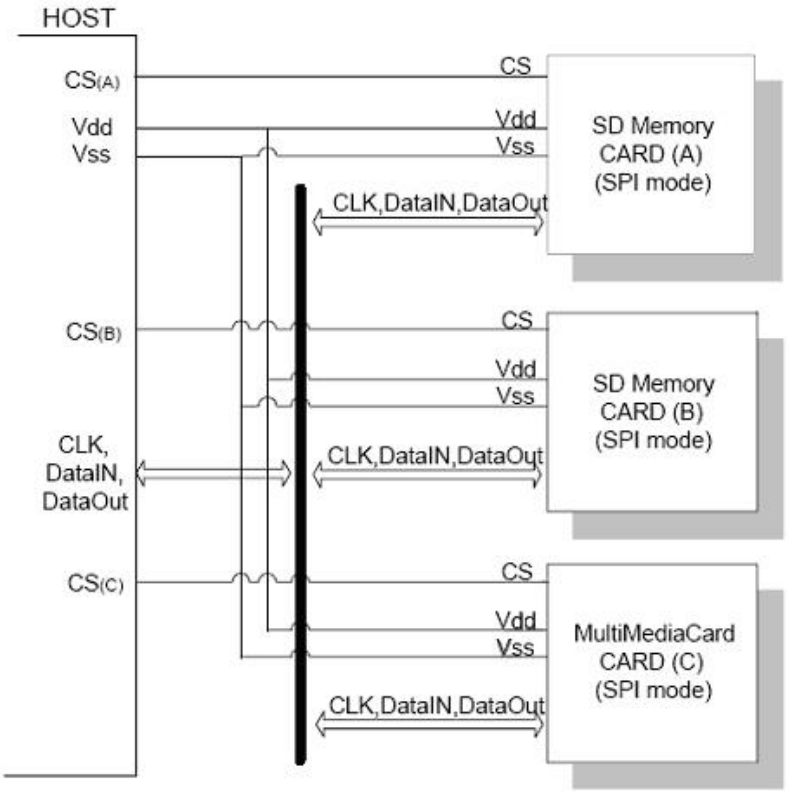


Figure 7-1: SD Card system (SPI mode) bus topology

7.3 SPI Bus Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned to 8-clock cycle boundary. Similar to the SD Memory Card protocol, the SPI messages consist of command, response and datablock tokens. All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low. The selected card always responds to the command as opposed to the SD mode. When the card encounters a data retrieval problem in a read operation, it will respond with an error response (which replaces the expected data block) rather than by a timeout as in the SD mode. Additionally, every data block sent to the card during write operations will be responded with a data response token.

In the case of a Standard Capacity Memory Card, a data block can be as big as one card write block and as small as a single byte. Partial block read/write operations are enabled by card options specified in the CSD register. In the case of a High Capacity SD Memory Card, the size of data block is fixed to 512 bytes. The block length set by CMD16 is only used for CMD42 and not used for memory data

transfer. So, partial block read/write operations are also disabled. Furthermore, Write Protected commands (CMD28, CMD29 and CMD30) are not supported.

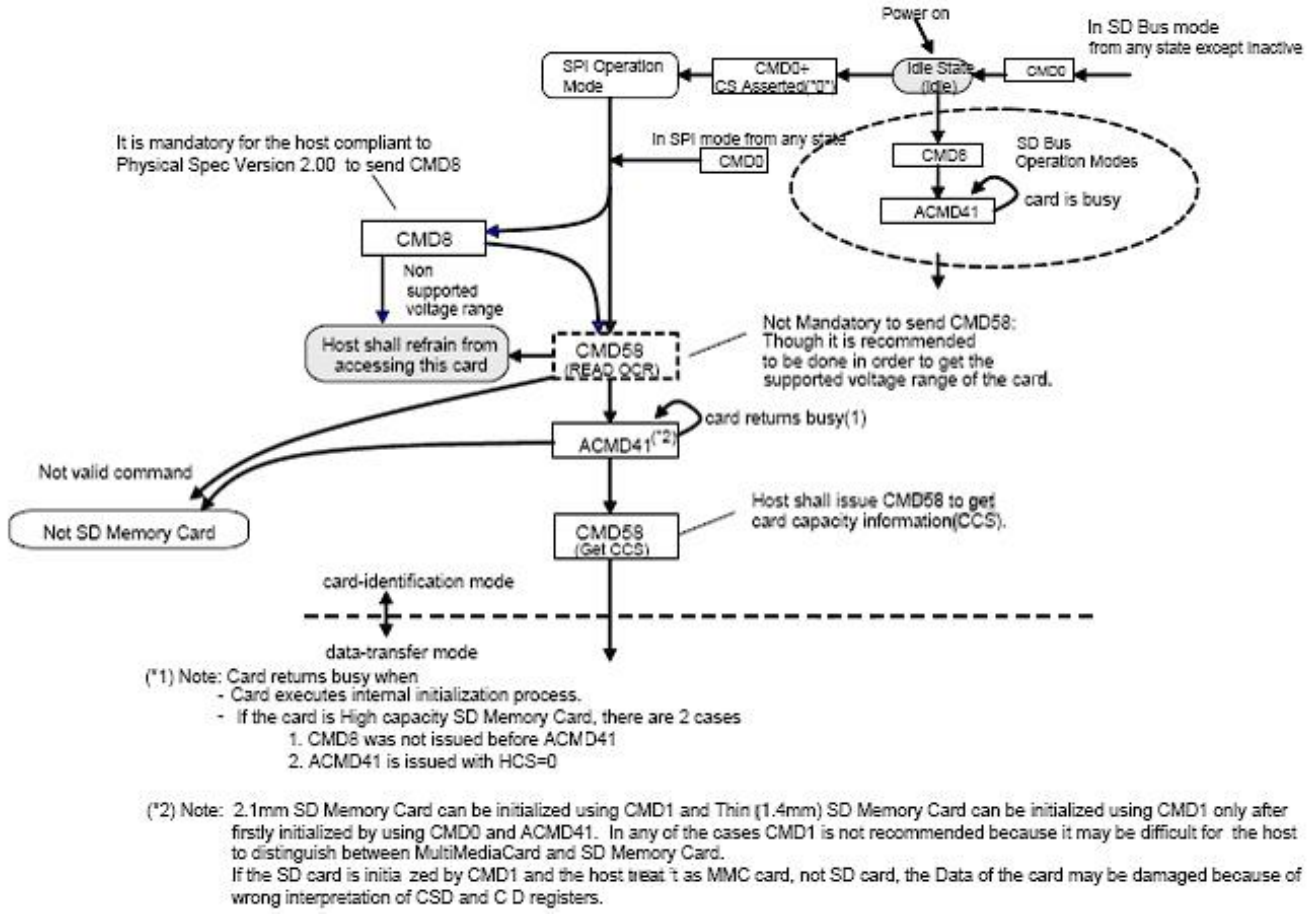


Figure 7-2: state diagram (SPI mode)

7.3.1 Mode Selection and Initialization

The SD Card is powered up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response. The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available. Figure 7-3 shows the initialization sequence of SPI mode. SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The argument format of CMD8 is the same as defined in SD mode and the response format of CMD8 is defined in Section 7.3.2.6. The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. The supplied voltage is indicated by VHS filed in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be set to

1 at any given time. Check pattern is used for the host to check validity of communication between the host and the card. If the card indicates an illegal command, the card is legacy and does not support CMD8. If the card supports CMD8 and can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument. If VCA in the response is set to 0, the card cannot operate on the supplied voltage. If check pattern is not matched, CMD8 communication is not valid. In this case, it is recommended to retry CMD8 sequence.

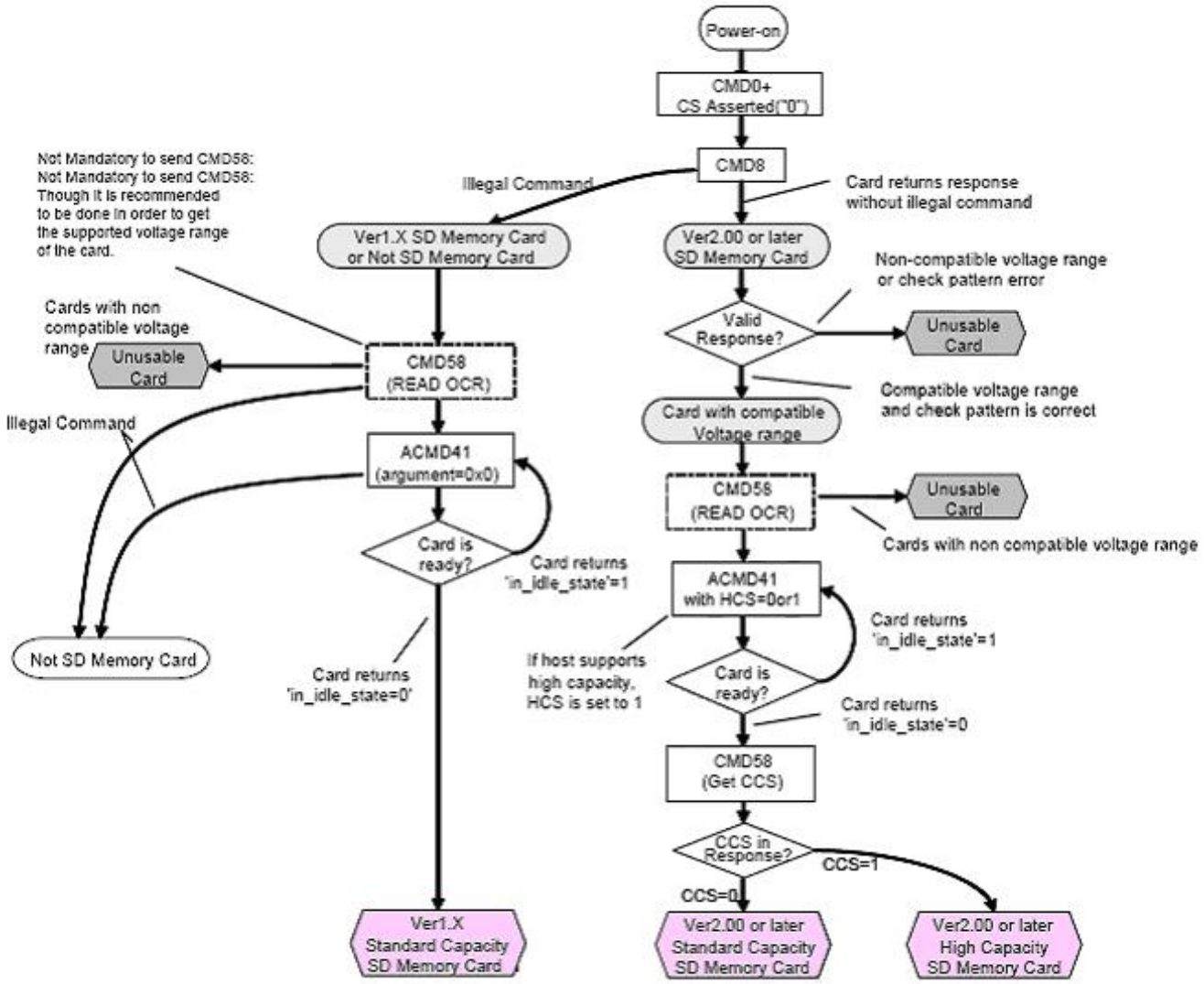


Figure 7-3: SPI Mode Initialization Flow

READ_OCR (CMD58) is designed to provide SD Memory Card hosts with a mechanism to identify cards that do not match the VDD range desired by the host. If the host does not accept voltage range, it shall not proceed further initialization sequence. The levels in the OCR register shall be defined accordingly. SD_SEND_OP_COND (ACMD41) is used to start initialization and to check if the card has completed initialization. It is mandatory to issue CMD8 prior to the first ACMD41. Receiving of CMD8 expands the CMD58 and ACMD41 function; HCS (High Capacity Support) in the argument of ACMD41 and CCS (Card Capacity Status) in the response of CMD58. HCS is ignored by the card, which didn't accept CMD8. Standard Capacity SD Memory Card ignores HCS. The "in idle state" bit in the R1 response of ACMD41 is used by the card to inform the host if initialization of ACMD41 is completed.

Setting this bit to “1” indicates that the card is still initializing. Setting this bit to “0” indicates completion of initialization. The host repeatedly issues ACMD41 until this bit is set to “0”. The card checks the HCS bit in the OCR only at the first ACMD41. While repeating ACMD41, the host shall not issue another command except CMD0. After initialization is completed, the host should get CCS information in the response of CMD58. CCS is valid when the card accepted CMD8 and after the completion of initialization. CCS=1 means that the card is a High Capacity SD Memory Card. CCS=0 means that the card is a Standard Capacity SD.

7.3.2 Bus Transfer Protection

Every SD Card token transferred on the bus is protected by CRC bits. In SPI mode, the SD Card offers a non protected mode which enables systems built with reliable data links to exclude the hardware or firmware required for implementing the CRC generation and verification functions. In the non-protected mode the CRC bits of the command, response and data tokens are still required in the tokens. However, they are defined as ‘don’t care’ for the transmitter and ignored by the receiver.

The SPI interface is initialized in the non-protected mode. However, the RESET command (CMD0) which is used to switch the card to SPI mode, is received by the card while in SD mode and, therefore, must have a valid CRC field.
Since CMD0 has no arguments, the content of all the fields, including the CRC field, are constants and need not be calculated in run time. A valid reset command is:

0x40, 0x0, 0x0, 0x0, 0x0, 0x95

The host can turn the CRC option on and off using the CRC_ON_OFF command (CMD59).

7.3.3 Data Read

The SPI mode supports single block read and Multiple Block read operations (CMD17 or CMD18 in the SD Card protocol). Upon reception of a valid read command the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command (refer to Figure 7-4).

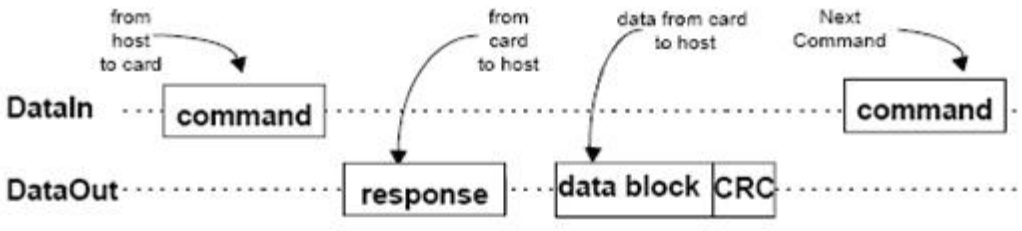


Figure 7-4: Single Block Read operation

In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 7-5 shows a data read operation which terminated with an error token rather than a data block.

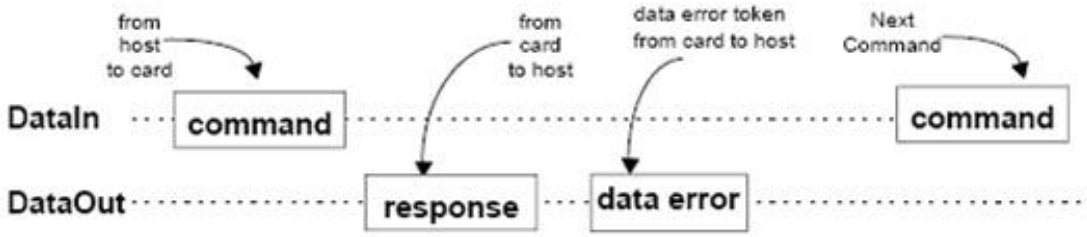


Figure 7-5: Read operation - data error

In case of Multiple block read operation every transferred block has its suffixed of 16 bit CRC. Stop transmission command (CMD12) will actually stop the data transfer operation (the same as in SD Card operation mode).

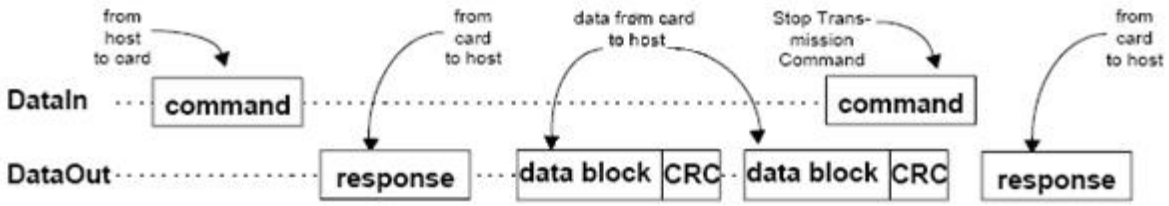


Figure 7-6: Multiple Block Read operation

7.3.4 Data Write

In SPI mode the SD Card supports single block and Multiple block write commands. Upon reception of a valid write command (CMD24 or CMD25 in the SD Card protocol), the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are (with the exception of the CSD parameter WRITE_BL_PARTIAL controlling the partial block write option) identical to the read operation.

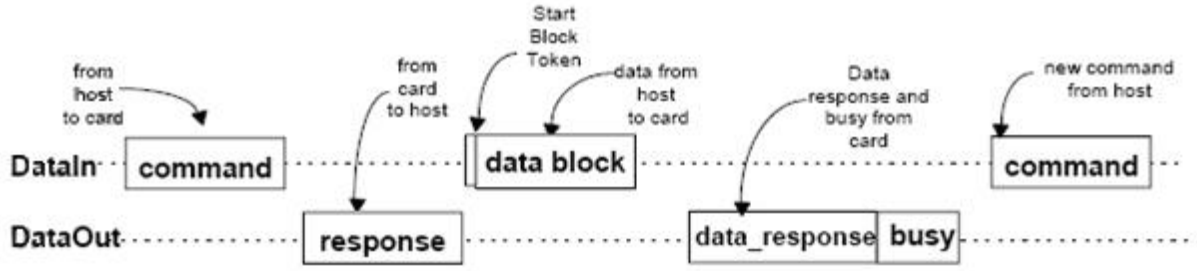


Figure 7-7: Single Block Write operation

Every data block has a prefix of 'Start Block' token (one byte).

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

In Multiple Block write operation the stop transmission will be done by sending 'Stop Tran' token instead of 'Start Block' token at the beginning of the next block. In case of Write Error indication (on the data response) the host shall use SEND_NUM_WR_BLOCKS (ACMD22) in order to get the number of well written write blocks.

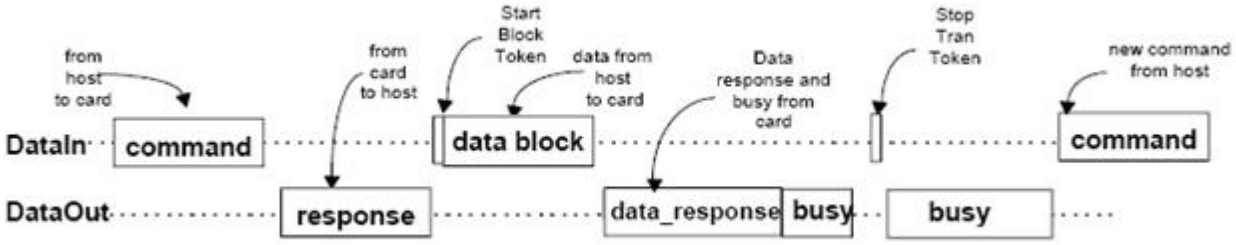


Figure 7-8: Multiple Block Write operation

While the card is busy, resetting the CS signal will not terminate the programming process. The card will release the DataOut line (tri-state) and continue with programming. If the card is reselected before the programming is finished, the DataOut line will be forced back to low and all commands will be rejected. Resetting a card (using CMD0) will terminate any pending or active programming operation. This may destroy the data formats on the card. It is in the responsibility of the host to prevent it.

7.3.5 Erase & Write Protect Management

The erase and write protect management procedures in the SPI mode are identical to those of the SD mode. While the card is erasing or changing the write protection bits of the predefined sector list, it will be in a busy state and hold the DataOut line low. Figure 7-9 illustrates a 'no data' bus transaction with and without busy signaling.

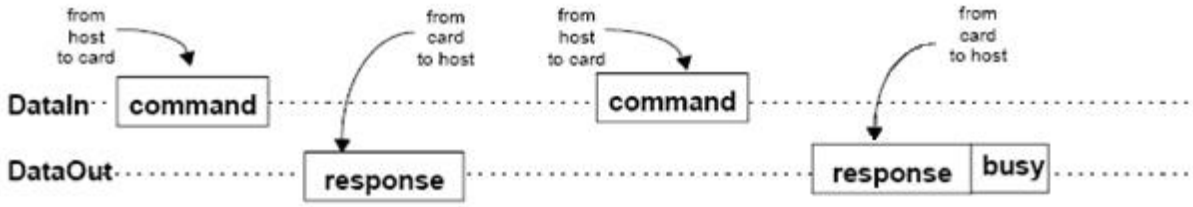


Figure 7-9: 'No data' operations

7.3.6 Read CID/CSD Registers

Unlike the SD Card protocol (where the register contents is sent as a command response), reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by a data block of 16 bytes suffixed with a 16 bit CRC. The data time out for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore the standard response time-out value (NCR) is used for read latency of the CSD register.

7.3.7 Reset Sequence

The SD Card requires a defined reset sequence. After power on reset or CMD0 (software reset) the card enters an idle state. At this state the only valid host commands are ACMD41 (SD_SEND_OP_COND), CMD58 (READ_OCR) and CMD59 (CRC_ON_OFF). CMD1 (SEND_OP_COND) is also valid - that means that in SPI mode CMD1 and ACMD41 have the same behavior. After Power On, once the card accepted valid ACMD41, it will be able to accept also CMD1 even if used after re-initializing (CMD0) the card.

The host must poll the card (by repeatedly sending CMD1 or ACMD41) until the 'in-idle-state' bit in the card response indicates (by being set to 0) that the card completed its initialization processes and is ready for the next command.

In SPI mode, as opposed to SD mode, ACMD41 (or CMD1 as well) has no operands and does not return the contents of the OCR register. Instead, the host may use CMD58 (available in SPI mode only) to read the OCR register. Furthermore, it is in the responsibility of the host to refrain from accessing cards that do not support its voltage range. The usage of CMD58 is not restricted to the initializing phase only, but can be issued at any time.

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