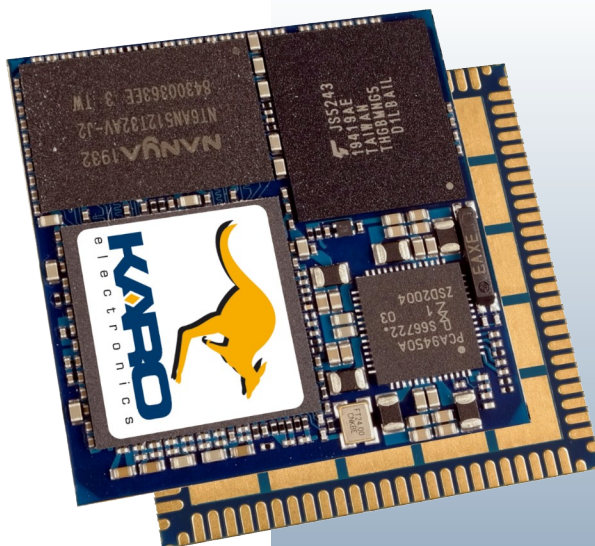


## QFN Style Solder-Down Computer On Module

- QSX – extended 2<sup>nd</sup> generation QS module series
- QS pin-compatible
- Solder-down version
- 29mm square
- 2.6mm total height
- QFN type lead style
  - 1mm pitch
  - 108 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V-5V power supply (-5%/+10%)



## Key Features

- NXP i.MX 8M Mini Quad Cortex-A53 up to 1.6 GHz  
Cortex-M4 up to 400 MHz
- RAM 2 GB LPDDR4
- ROM 4 GB eMMC
- Grade Industrial
- Temperature -25°C to 85°C
- Display support
  - MIPI DSI (4-lane)
  - GC328 2D GPU
  - GCNanoUltra 3D GPU
  - 1080p60 video de-/encode
- Connectivity
  - 2x USB 2.0
  - 1x Gb Ethernet, RGMII
  - 1x eMMC/SD
  - 1x PCIe® Gen 2, 1-lane
  - 4x UART, 3x I<sup>2</sup>C, 2x SPI, 4x PWM, SAI
  - Up to 60x 3.3V General Purpose I/O
  - MIPI-CSI (4-lane)

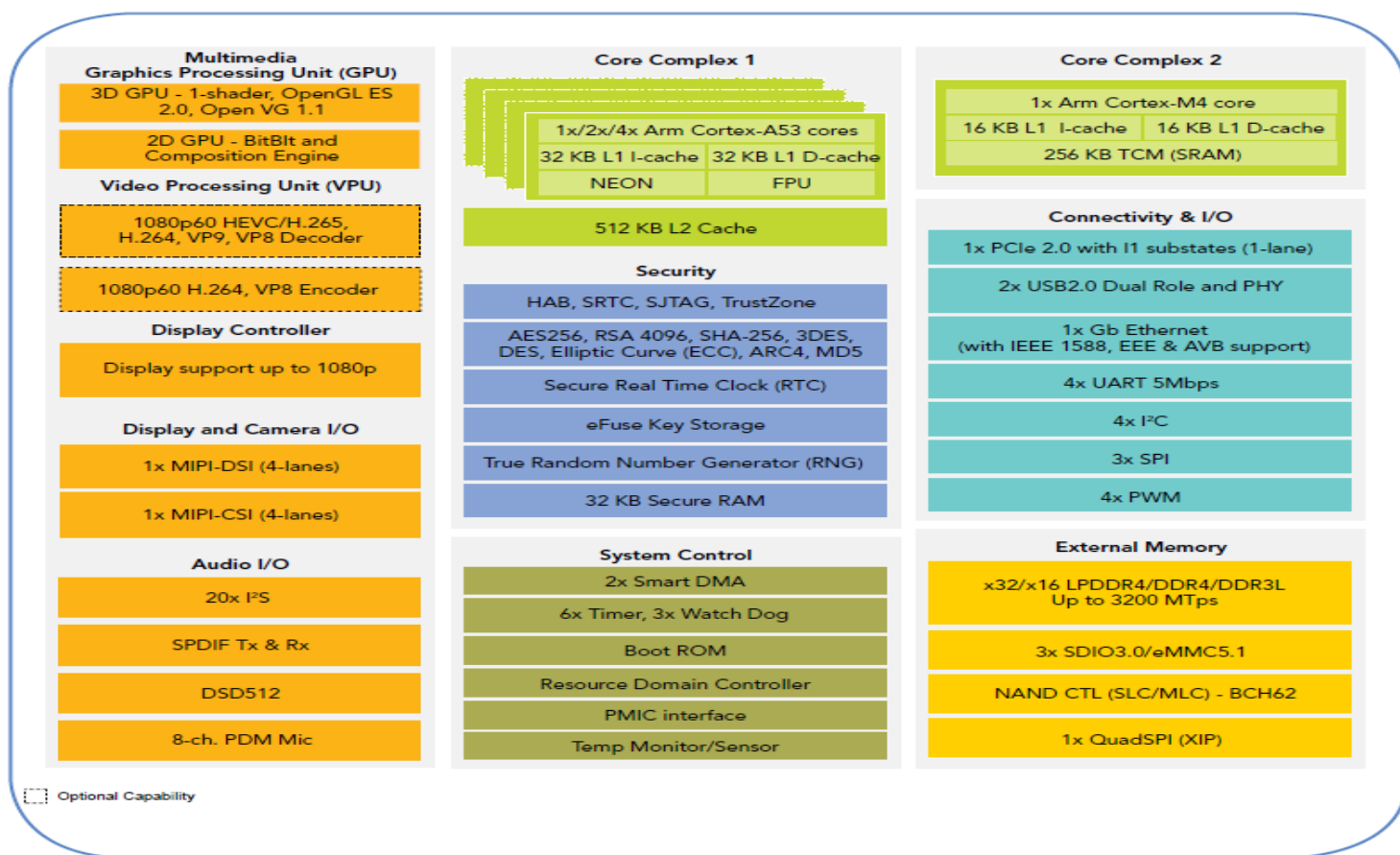
**i.MX 8M Mini**

## OS Support

- Linux
- Windows 10 IoT



## i.MX 8M MINI FAMILY BLOCK DIAGRAM



### QS8M – QSXM – QSXP – Differentiated Features and Ordering Information

|                      | QS8M - i.MX 8M Mini                   | QSXM - i.MX 8M Mini   | QSXP - i.MX 8M Plus                                            |
|----------------------|---------------------------------------|-----------------------|----------------------------------------------------------------|
| Primary Arm® Core    | 4x Cortex®-A53 1.6 GHz                |                       |                                                                |
| Secondary Arm® Core  | Cortex-M4 400 MHz                     |                       | Cortex-M7 800 MHz                                              |
| RAM                  | 1 GB DDR3L x16                        | 2 GB LPDDR4 x32       |                                                                |
| ROM                  | 4 GB eMMC                             |                       | 8 GB eMMC                                                      |
| 3D GPU               | GCNanoUltra (1 shader, OpenGL ES 2.0) |                       | GC7000UL (2 shaders, OpenGL ES 2.0/3.0/3.1 OpenCL 1.2, Vulkan) |
| 2D GPU               | GC520L                                |                       |                                                                |
| AI/ML/DSP            | -                                     |                       | NN Accel 2.3 TOPS<br>Hi-Fi4 DSP 800 MHz                        |
| Video De-/Encode     | 1080p60 H.264                         |                       | 1080p60 H.264, H.265                                           |
| Connectivity         | 2x USB 2.0                            | 2x USB 2.0, PCIe      | USB 2.0, USB 3.0, PCIe                                         |
| QS Size              | 100 pins 27mm square                  | 108 pins 29mm square  |                                                                |
| Grade / Temperature  | Industrial -25°C to 85°C              |                       | Industrial -30°C to 85°C                                       |
| Ordering Information | QS8M/MQ/1GS/4GF/E85                   | QSXM/MM6C/2GS/4GF/E85 | QSXP/ML8/2GS/4GF/E85                                           |

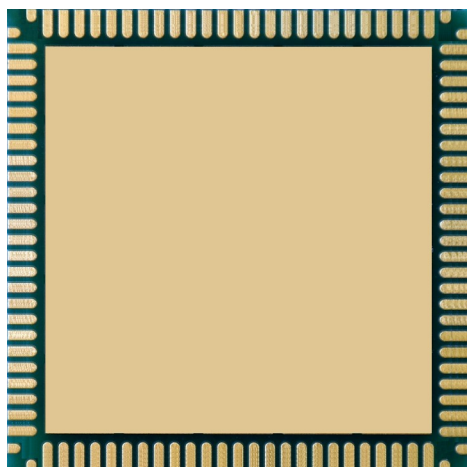
## QFN Style Computer On Module Advantages

### Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



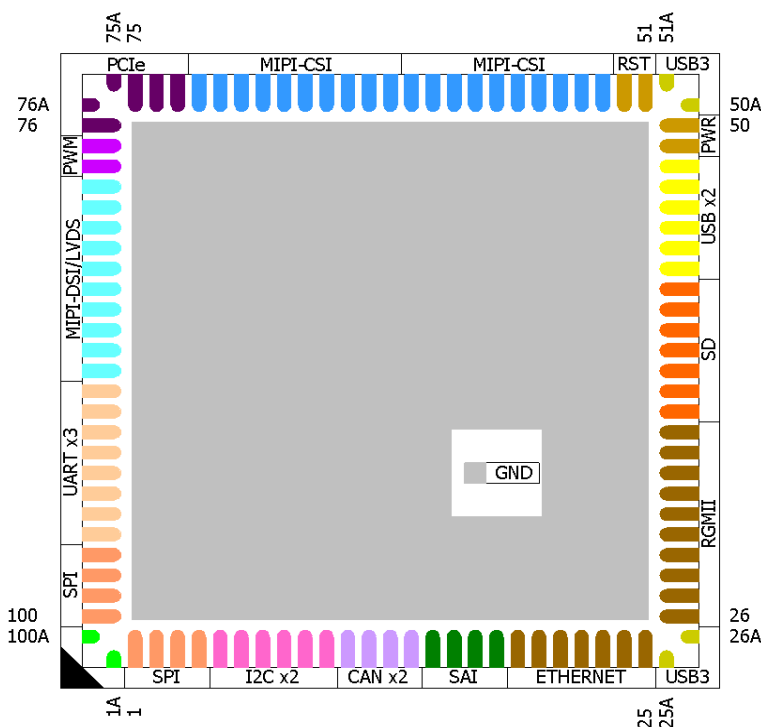
### Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

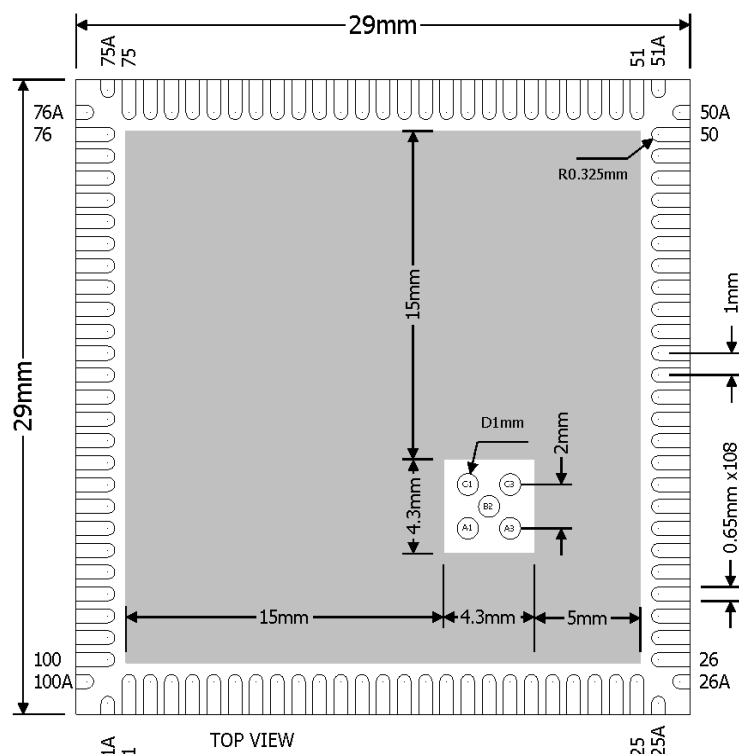
## Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

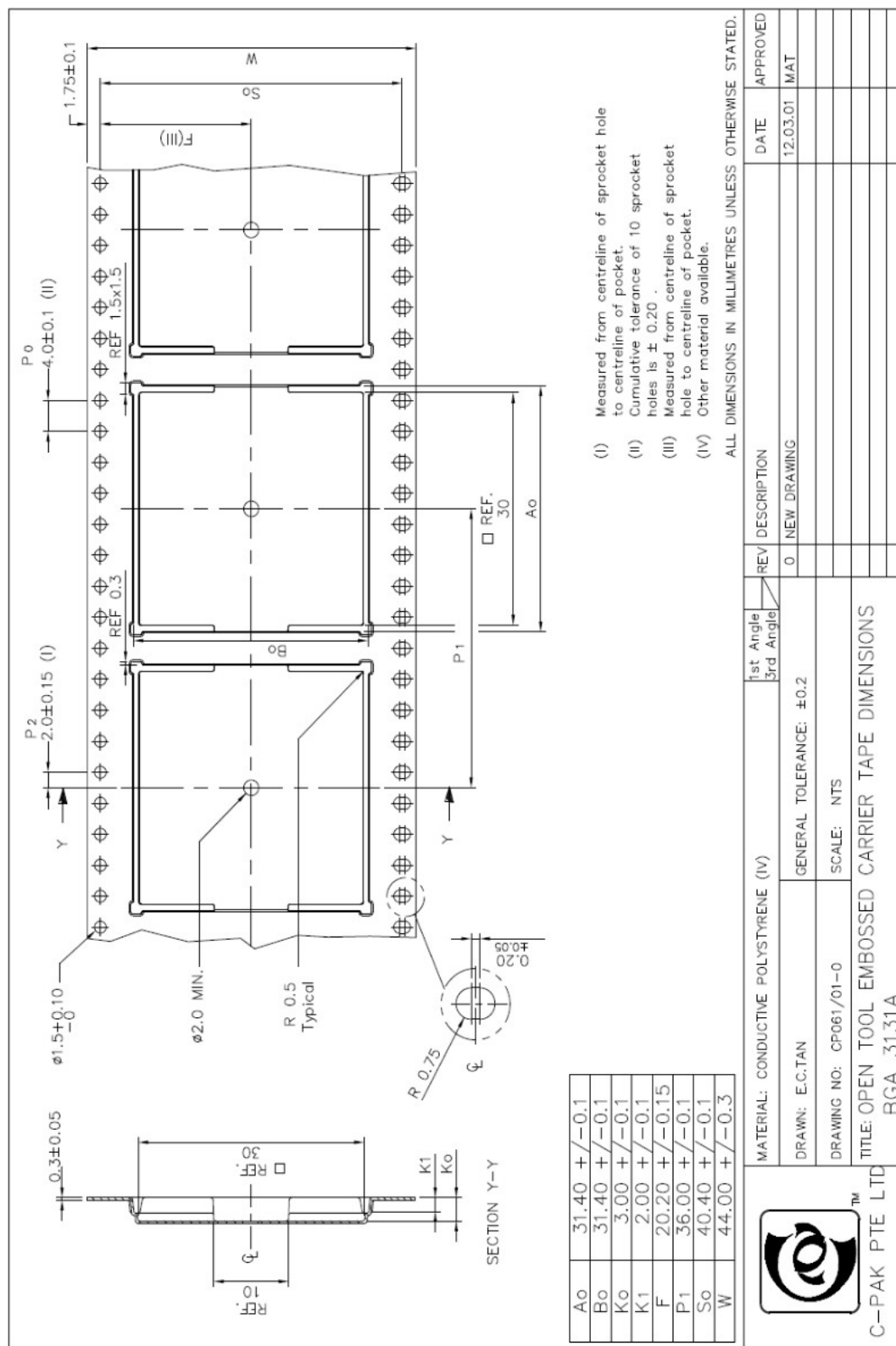
## Standard Contact Assignments



## Package Information



## Packaging



## Pinout

| PIN                       | QSCOM STANDARD | i.MX8MM Pad Name | Alternate functions                                              | GPIO      | Description (refer to i.MX8MM manuals for details)                                 |
|---------------------------|----------------|------------------|------------------------------------------------------------------|-----------|------------------------------------------------------------------------------------|
| <b>1<sup>st</sup> SPI</b> |                |                  |                                                                  |           |                                                                                    |
| 1                         | SPIA_NSS       | ECSPI2_SS0       | UART4_RTS_B                                                      | GPIO5[13] |                                                                                    |
| 2                         | SPIA_MISO      | ECSPI2_MISO      | UART4_CTS_B                                                      | GPIO5[12] |                                                                                    |
| 3                         | SPIA_MOSI      | ECSPI2_MOSI      | UART4_TX                                                         | GPIO5[11] |                                                                                    |
| 4                         | SPIA_SCK       | ECSPI2_SCLK      | UART4_RX                                                         | GPIO5[10] |                                                                                    |
| <b>I2C</b>                |                |                  |                                                                  |           |                                                                                    |
| 5                         | I2CA_SCL       | I2C2_SCL         | ENET1_1588_EVENT1_IN<br>USDHC3_CD_B                              | GPIO5[16] |                                                                                    |
| 6                         | I2CA_SDA       | I2C2_SDA         | ENET1_1588_EVENT1_OUT<br>USDHC3_WP                               | GPIO5[17] |                                                                                    |
| 7                         | INTA           | I2C4_SCL         | PWM2_OUT<br>PCIE1_CLKREQ_B                                       | GPIO5[20] |                                                                                    |
| 8                         | I2CA_SCL       | I2C3_SCL         | PWM4_OUT<br>GPT2_CLK                                             | GPIO5[18] |                                                                                    |
| 9                         | I2CA_SDA       | I2C3_SDA         | PWM3_OUT<br>GPT3_CLK                                             | GPIO5[19] |                                                                                    |
| 10                        | INTA           | I2C4_SDA         | PWM1_OUT                                                         | GPIO5[21] |                                                                                    |
| <b>SPDIF</b>              |                |                  |                                                                  |           |                                                                                    |
| 11                        | CANA_RX        | SPDIF_TX         | SPDIF1_OUT<br>PWM3_OUT                                           | GPIO5[03] |                                                                                    |
| 12                        | CANA_TX        | SPDIF_RX         | SPDIF1_IN<br>PWM2_OUT                                            | GPIO5[04] |                                                                                    |
| 13                        | CANA_RX        | SPDIF_EXT_CLK    | PWM1_OUT                                                         | GPIO5[05] |                                                                                    |
| 14                        | CANA_TX        | SAI2_MCLK        | SAI5_MCLK                                                        | GPIO4[27] |                                                                                    |
| <b>SAI</b>                |                |                  |                                                                  |           |                                                                                    |
| 15                        | SAI_TX         | SAI2_TXD0        | SAI2_TX_DATA0<br>SAI5_TX_DATA3                                   | GPIO4[26] |                                                                                    |
| 16                        | SAI_RX         | SAI2_RXD0        | SAI2_RX_DATA0<br>SAI5_TX_DATA0<br>UART1_RTS_B                    | GPIO4[23] |                                                                                    |
| 17                        | SAI_SCK        | SAI2_TXC         | SAI2_TX_BCLK<br>SAI5_TX_DATA2                                    | GPIO4[25] |                                                                                    |
| 18                        | SAI_FS         | SAI2_TXFS        | SAI2_TX_SYNC<br>SAI5_TX_DATA1<br>SAI2_TX_DATA1<br>UART1_CTS_B    | GPIO4[24] |                                                                                    |
| <b>ETHERNET</b>           |                |                  |                                                                  |           |                                                                                    |
| 19                        | ENET_RST       | SAI2_RXC         | SAI2_RX_BCLK<br>SAI5_TX_BCLK<br>UART1_RX                         | GPIO4[22] |                                                                                    |
| 20                        | ENET_CK125     | GPIO1_IO00       | CCM_ENET_PHY_REF_CLK_ROOT<br>XTALOSC_REF_CLK_32K<br>CCM_EXT_CLK1 | GPIO1[00] |                                                                                    |
| 21                        | ENET_INT       | GPIO1_IO10       | USB1_OTG_ID                                                      | GPIO1[10] |                                                                                    |
| 22                        | ENET_MDIO      | ENET_MDIO        | ENET1_MDIO<br>IOMUXC_ENET1_MDIO_                                 | GPIO1[17] |                                                                                    |
| 23                        | ENET_MDC       | ENET_MDC         | ENET1_MDC                                                        | GPIO1[16] |                                                                                    |
| 24                        | ENET_RXC       | ENET_RXC         | ENET1_RGMII_RXC<br>ENET1_RX_ER                                   | GPIO1[25] | For RMII—ENET_RXC works as RMII.RX_ERR<br>For RGMII—ENET_RXC works as RGMII.RX_CLK |
| 25                        | ENET_RX_CTL    | ENET_RX_CTL      | ENET1_RGMII_RX_CTL                                               | GPIO1[24] | RMII.RX_EN (CRS_DV); RGMII.RC_CTL                                                  |
| 26                        | ENET_RXD0      | ENET_RD0         | ENET1_RGMII_RD0                                                  | GPIO1[26] | RMII and RGMII.RD0                                                                 |
| 27                        | ENET_RXD1      | ENET_RD1         | ENET1_RGMII_RD1                                                  | GPIO1[27] | RMII and RGMII.RD1                                                                 |
| 28                        | ENET_RXD2      | ENET_RD2         | ENET1_RGMII_RD2                                                  | GPIO1[28] | Only used for RGMII                                                                |
| 29                        | ENET_RXD3      | ENET_RD3         | ENET1_RGMII_RD3                                                  | GPIO1[29] | Only used for RGMII                                                                |
| 30                        | ENET_TX_CTL    | ENET_TX_CTL      | ENET1_RGMII_TX_CTL                                               | GPIO1[22] | RMII.TX_EN; RGMII.TX_CTL                                                           |
| 31                        | ENET_TXC       | ENET_TXC         | ENET1_RGMII_TXC<br>ENET1_TX_ER                                   | GPIO1[23] | For RMII—ENET_TXC works as RMII.TX_ERR<br>For RGMII—ENET_TXC works as RGMII.TX_CLK |
| 32                        | ENET_TXD3      | ENET_TD3         | ENET1_RGMII_TD3                                                  | GPIO1[18] | Only used for RGMII                                                                |

| PIN                             | QSCOM STANDARD | i.MX8MM Pad Name | Alternate functions                                                   | GPIO          | Description (refer to i.MX8MM manuals for details)                                                                                                                                            |
|---------------------------------|----------------|------------------|-----------------------------------------------------------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 33                              | ENET_TXD2      | ENET_TD2         | ENET1_RGMII_TD2<br>INPUT=ENET1_TX_CLK<br>OUTPUT=CCM_ENET_REF_CLK_ROOT | GPIO1[19]     | Used as RMII clock and RGMII data, there are two RGMII clock schemes.<br>• MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock.<br>• MAC use external 50M clock. |
| 34                              | ENET_TXD1      | ENET_TD1         | ENET1_RGMII_TD1                                                       | GPIO1[20]     | RMII and RGMII.TD1                                                                                                                                                                            |
| 35                              | ENET_TXD0      | ENET_TD0         | ENET1_RGMII_TD0                                                       | GPIO1[21]     | RMII and RGMII.TD0                                                                                                                                                                            |
| <b>SD</b>                       |                |                  |                                                                       |               |                                                                                                                                                                                               |
| 36                              | SD_CD          | SD2_CD_B         | USDHC2_CD_B                                                           | GPIO2[12]     |                                                                                                                                                                                               |
| 37                              | SD_D1          | SD2_DATA1        | USDHC2_DATA1                                                          | GPIO2[16]     |                                                                                                                                                                                               |
| 38                              | SD_D0          | SD2_DATA0        | USDHC2_DATA0                                                          | GPIO2[15]     |                                                                                                                                                                                               |
| 39                              | SD_CLK         | SD2_CLK          | USDHC2_CLK                                                            | GPIO2[13]     |                                                                                                                                                                                               |
| 40                              | SD_CMD         | SD2_CMD          | USDHC2_CMD                                                            | GPIO2[14]     |                                                                                                                                                                                               |
| 41                              | SD_D3          | SD2_DATA3        | USDHC2_DATA3                                                          | GPIO2[18]     |                                                                                                                                                                                               |
| 42                              | SD_D2          | SD2_DATA2        | USDHC2_DATA2                                                          | GPIO2[17]     |                                                                                                                                                                                               |
| <b>USB</b>                      |                |                  |                                                                       |               |                                                                                                                                                                                               |
| 43                              | USBH_VBUS      | USB2_VBUS        |                                                                       |               |                                                                                                                                                                                               |
| 44                              | USBH_DN        | USB2_DN          |                                                                       |               |                                                                                                                                                                                               |
| 45                              | USBH_DP        | USB2_DP          |                                                                       |               |                                                                                                                                                                                               |
| 46                              | USBOTG_VBUS    | USB1_VBUS        |                                                                       |               |                                                                                                                                                                                               |
| 47                              | USBOTG_DN      | USB1_DN          |                                                                       |               |                                                                                                                                                                                               |
| 48                              | USBOTG_DP      | USB1_DP          |                                                                       |               |                                                                                                                                                                                               |
| <b>POWER SUPPLY &amp; RESET</b> |                |                  |                                                                       |               |                                                                                                                                                                                               |
| 49                              | VIN            |                  |                                                                       |               | 3.3V Module power supply input.                                                                                                                                                               |
| 50                              |                |                  |                                                                       |               |                                                                                                                                                                                               |
| 51                              | #POR           |                  | POR_B                                                                 | 10K-PU to 1V8 | Power On Reset — 1.8V active low input / open drain output signal. Also connected to PMIC RESET0. Leave unconnected, if not used.                                                             |
| 52                              | BOOT_MODE      |                  |                                                                       |               | Boot mode select L: Boot from eMMC / H: Boot from UART/USB                                                                                                                                    |
| <b>MIPI-CSI</b>                 |                |                  |                                                                       |               |                                                                                                                                                                                               |
| 53                              | CSI_D3P_A      | MIPI_CSI_DATA3_P |                                                                       |               |                                                                                                                                                                                               |
| 54                              | CSI_D3N_A      | MIPI_CSI_DATA3_N |                                                                       |               |                                                                                                                                                                                               |
| 55                              | CSI_D2P_A      | MIPI_CSI_DATA2_P |                                                                       |               |                                                                                                                                                                                               |
| 56                              | CSI_D2N_A      | MIPI_CSI_DATA2_N |                                                                       |               |                                                                                                                                                                                               |
| 57                              | CSI_D1P_A      | MIPI_CSI_DATA1_P |                                                                       |               |                                                                                                                                                                                               |
| 58                              | CSI_D1N_A      | MIPI_CSI_DATA1_N |                                                                       |               |                                                                                                                                                                                               |
| 59                              | CSI_D0P_A      | MIPI_CSI_DATA0_P |                                                                       |               |                                                                                                                                                                                               |
| 60                              | CSI_D0N_A      | MIPI_CSI_DATA0_N |                                                                       |               |                                                                                                                                                                                               |
| 61                              | CSI_CLKP_A     | MIPI_CSI_CLK_P   |                                                                       |               |                                                                                                                                                                                               |
| 62                              | CSI_CLKN_A     | MIPI_CSI_CLK_N   |                                                                       |               |                                                                                                                                                                                               |

| PIN                    | QSCOM<br>STANDARD | i.MX8MM Pad Name | Alternate functions                                                        | GPIO      | Description (refer to i.MX8MM manuals for details) |
|------------------------|-------------------|------------------|----------------------------------------------------------------------------|-----------|----------------------------------------------------|
| <b>GPIO</b>            |                   |                  |                                                                            |           |                                                    |
| 63                     |                   | GPIO1_IO02       | WDOG1_WDOG_B<br>WDOG1_WDOG_ANY<br>SJC_DE_B                                 | GPIO1[02] | PMIC Watchdog – connected to PMIC WDOG_B           |
| 64                     |                   | GPIO1_IO04       | USDHC2_VSELECT<br>SDMA1_EXT_EVENT1                                         | GPIO1[04] |                                                    |
| 65                     |                   | GPIO1_IO05       | M4_NMI<br>CCM_PMIC_READY                                                   | GPIO1[05] |                                                    |
| 66                     |                   | GPIO1_IO06       | ENET1_MDC<br>USDHC1_CD_B<br>CCM_EXT_CLK3                                   | GPIO1[06] |                                                    |
| 67                     |                   | GPIO1_IO07       | ENET1_MDIO<br>USDHC1_WP<br>CCM_EXT_CLK4                                    | GPIO1[07] |                                                    |
| 68                     |                   | GPIO1_IO08       | ENET1_1588_EVENT0_IN<br>USDHC2_RESET_B                                     | GPIO1[08] |                                                    |
| 69                     |                   | GPIO1_IO09       | ENET1_1588_EVENT0_OUT<br>USDHC3_RESET_B<br>SDMA2_EXT_EVENT0                | GPIO1[09] |                                                    |
| 70                     |                   | GPIO1_IO11       | USB2_OTG_ID<br>USDHC3_VSELECT<br>CCM_PMIC_READY                            | GPIO1[11] |                                                    |
| 71                     |                   | GPIO1_IO12       | USB1_OTG_PWR<br>SDMA2_EXT_EVENT1                                           | GPIO1[12] |                                                    |
| 72                     |                   | GPIO1_IO13       | USB1_OTG_OC<br>PWM2_OUT                                                    | GPIO1[13] |                                                    |
| 73                     |                   | GPIO1_IO14       | USB2_OTG_PWR<br>USDHC3_CD_B<br>PWM3_OUT<br>CCM_CLK01                       | GPIO1[14] |                                                    |
| 74                     |                   | PCIE_CLK_P       |                                                                            |           |                                                    |
| 75                     |                   | PCIE_CLK_N       |                                                                            |           |                                                    |
| 76                     |                   | SD2_WP           | USDHC2_WP                                                                  | GPIO2[20] |                                                    |
| <b>Display Control</b> |                   |                  |                                                                            |           |                                                    |
| 77                     | <b>DISP_EN</b>    | SAI2_RXFS        | SAI2_RX_SYNC<br>SAI5_TX_SYNC<br>SAI5_TX_DATA1<br>SAI2_RX_DATA1<br>UART1_TX | GPIO4[21] |                                                    |
| 78                     | <b>DISP_BL</b>    | GPIO1_IO01       | <b>PWM1_OUT</b><br>XTALOSC_REF_CLK_24M<br>CCM_EXT_CLK2                     | GPIO1[01] |                                                    |
| <b>MIPI-DSI</b>        |                   |                  |                                                                            |           |                                                    |
| 79                     | DSI_D3P           | MIPI_DSI_DATA3_P |                                                                            |           |                                                    |
| 80                     | DSI_D3N           | MIPI_DSI_DATA3_N |                                                                            |           |                                                    |
| 81                     | DSI_D2P           | MIPI_DSI_DATA2_P |                                                                            |           |                                                    |
| 82                     | DSI_D2N           | MIPI_DSI_DATA2_N |                                                                            |           |                                                    |
| 83                     | DSI_D1P           | MIPI_DSI_DATA1_P |                                                                            |           |                                                    |
| 84                     | DSI_D1N           | MIPI_DSI_DATA1_N |                                                                            |           |                                                    |
| 85                     | DSI_D0P           | MIPI_DSI_DATA0_P |                                                                            |           |                                                    |
| 86                     | DSI_D0N           | MIPI_DSI_DATA0_N |                                                                            |           |                                                    |
| 87                     | DSI_CLKP          | MIPI_DSI_CLK_P   |                                                                            |           |                                                    |
| 88                     | DSI_CLKN          | MIPI_DSI_CLK_N   |                                                                            |           |                                                    |
| <b>UART</b>            |                   |                  |                                                                            |           |                                                    |

| PIN                 | QSCOM<br>STANDARD | i.MX8MM Pad Name | Alternate functions                              | GPIO      | Description (refer to i.MX8MM manuals for details) |
|---------------------|-------------------|------------------|--------------------------------------------------|-----------|----------------------------------------------------|
| 89                  | UARTA_RXD         | <b>UART1_RXD</b> | UART1_RX<br>ECSPI3_SCLK                          |           |                                                    |
| 90                  | UARTA_TXD         | <b>UART1_TXD</b> | UART1_TX<br>ECSPI3_MOSI                          |           |                                                    |
| 91                  | UARTB_RXD         | <b>UART3_RXD</b> | UART3_RX<br>UART1_CTS_B<br>USDHC3_RESET_B        |           |                                                    |
| 92                  | UARTB_TXD         | <b>UART3_TXD</b> | UART3_TX<br>UART1_RTS_B<br>USDHC3_VSELECT        |           |                                                    |
| 93                  | UARTC_RXD         | <b>UART2_RXD</b> | UART2_RX<br>ECSPI3_MISO                          | GPIO5[24] |                                                    |
| 94                  | UARTC_TXD         | <b>UART2_TXD</b> | UART2_TX<br>ECSPI3_SS0                           | GPIO5[25] |                                                    |
| 95                  | UARTC_RTS         | UART4_TXD        | UART4_TX<br><b>UART2_RTS_B</b>                   | GPIO5[29] | NXP: Request to Send <b>input</b> signal           |
| 96                  | UARTC_CTS         | UART4_RXD        | UART4_RX<br><b>UART2_CTS_B</b><br>PCIE1_CLKREQ_B | GPIO5[28] | NXP: Clear to Send <b>output</b> signal            |
| 2 <sup>nd</sup> SPI |                   |                  |                                                  |           |                                                    |
| 97                  | SPIB_NSS          | ECSPI1_SS0       | UART3_RTS_B                                      | GPIO5[09] |                                                    |
| 98                  | SPIB_MISO         | ECSPI1_MISO      | UART3_CTS_B                                      | GPIO5[08] |                                                    |
| 99                  | SPIB_MOSI         | ECSPI1_MOSI      | UART3_TX                                         | GPIO5[07] |                                                    |
| 100                 | SPIB_SCK          | ECSPI1_SCLK      | UART3_RX                                         | GPIO5[06] |                                                    |
| USB3                |                   |                  |                                                  |           |                                                    |
| 25A                 | not connected     |                  |                                                  |           |                                                    |
| 26A                 | not connected     |                  |                                                  |           |                                                    |
| 50A                 | not connected     |                  |                                                  |           |                                                    |
| 51A                 | not connected     |                  |                                                  |           |                                                    |
| PCIe                |                   |                  |                                                  |           |                                                    |
| 75A                 |                   | PCIE_TXN_P       |                                                  |           |                                                    |
| 76A                 |                   | PCIE_TXN_M       |                                                  |           |                                                    |
| 100A                |                   | PCIE_RXN_P       |                                                  |           |                                                    |
| 1A                  |                   | PCIE_RXN_M       |                                                  |           |                                                    |

**Pins used for manufacturing and debugging – leave unconnected**

| PIN |            | PIN |          | PIN |          |
|-----|------------|-----|----------|-----|----------|
| C1  | JTAG_TDI   |     |          | C3  | JTAG_TCK |
|     |            | B2  | JTAG_TDO |     |          |
| A1  | JTAG_BSCAN |     |          | A3  | JTAG_TMS |

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