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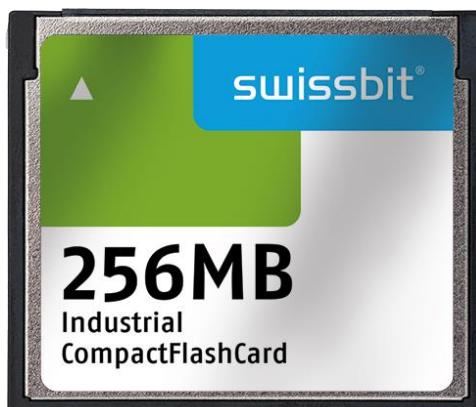
Product Data Sheet

**Industrial  
CompactFlash™ Card**

**C-350 Series**  
up to UDMA4 / MDMA4 / PIO6, SLC

Commercial and Industrial  
Temperature Grade

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# C-350 Series – Industrial CompactFlash™ Card, SLC

## 32 MBytes up to 256 MBytes

### 1. Product Summary

- **Capacities:** 32 MBytes, 64 MBytes, 128 MBytes, 256 MBytes
- **Form Factor:** CompactFlash Card Type I (36.4 mm x 42.8 mm x 3.3 mm)
- **Compliance<sup>1</sup>:** CompactFlash™ specification 3.0 (4.1 compatible)
- **Command Sets:** CFA feature set, HPA, Power Management, S.M.A.R.T.
- **High Performance:**
  - Burst Transfer Rate: Up to 66 MBytes/s UDMA4
  - Read Performance: Sequential Read up to 19.8 MBytes/s, Random Read IOPS up to 2,900
  - Write Performance: Sequential Write up to 11.4 MBytes/s, Random Write IOPS up to 20
- **Operating Temperature Range:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -50 °C to 100 °C
- **Operating Voltage:** 3.3V ± 10% / 5V ± 10%
- **Power (Max Capacity):**
  - Read (Active): 110mA
  - Write (Active): 115mA
  - Idle: 2mA
- **Data Retention:** 10 Years @ Life Begin; 1 Year @ Life End
- **Endurance in TeraBytes Written (TBW):**
  - Sequential WL: up to 25 TBW
  - Enterprise WL: up to 0.76 TBW
- **Shock/Vibration:** 1,500 g / 20 g
- **High-Performance 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Single-Level Cell (SLC) NAND Flash
  - Hardware RS-Code ECC (4 Bytes/528 Bytes correction)
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 3,000,000 hours @ 25°C
  - Data Reliability: < 1 non-recoverable error per 10<sup>14</sup> bits read

<sup>1</sup> The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.

## 2. Product Features

- SLC NAND Flash with long-term availability
- Highly-integrated memory controller
  - Fully compliant with CompactFlash™ specification 3.0, compatible with specification 4.1
  - Fully compatible with PCMCIA specification
  - PC Card ATA Interface supported
  - True IDE mode compatible
  - Up to PIO mode 6 supported
  - Up to MDMA4 supported
  - Up to UDMA4 supported
  - Hardware RS-code ECC (4 Bytes/528 Bytes correction)
  - Fix drive (IDE mode) & removable drive (PCMCIA mode) as default in the same card
- Small form factor
  - CFC Type I: 36.4 mm x 42.8 mm x 3.3 mm
- Low-power CMOS technology
- 3.3V or 5.0V power supply
- Power saving mode (with automatic wake-up)
- S.M.A.R.T. support
- Wear Leveling: equal wear leveling of static and dynamic data
 

The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Patented power-off reliability
  - No data loss of older sectors
  - All data written to the flash if card status is ready after write command
- Hot swappable in PCMCIA modes
- Operating System support
  - Standard Software Drivers operation CompactFlash
- Life Cycle Management
- Controlled "Locked" BOM
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)



### 3. Ordering Information

**Table 1: Standard Product List**

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
32 MBytes	SFCF0032HxBK1WI-C-MS-5y3-STD	SFCF0032HxBK1WI-I-MS-5y3-STD
64 MBytes	SFCF0064HxBK1WI-C-MS-5y3-STD	SFCF0064HxBK1WI-I-MS-5y3-STD
128 MBytes	SFCF0128HxBK1WI-C-MS-5y3-STD	SFCF0128HxBK1WI-I-MS-5y3-STD
256 MBytes	SFCF0256HxBK1WI-C-MS-5y3-STD	SFCF0256HxBK1WI-I-MS-5y3-STD

x = product generation and y = firmware revision

**Table 2: Available Part Numbers**

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
32 MBytes	SFCF0032H1BK1WI-C-MS-513-STD	SFCF0032H1BK1WI-I-MS-513-STD
64 MBytes	SFCF0064H1BK1WI-C-MS-513-STD	SFCF0064H1BK1WI-I-MS-513-STD
128 MBytes	SFCF0128H1BK1WI-C-MS-513-STD	SFCF0128H1BK1WI-I-MS-513-STD
256 MBytes	SFCF0256H1BK1WI-C-MS-513-STD	SFCF0256H1BK1WI-I-MS-513-STD

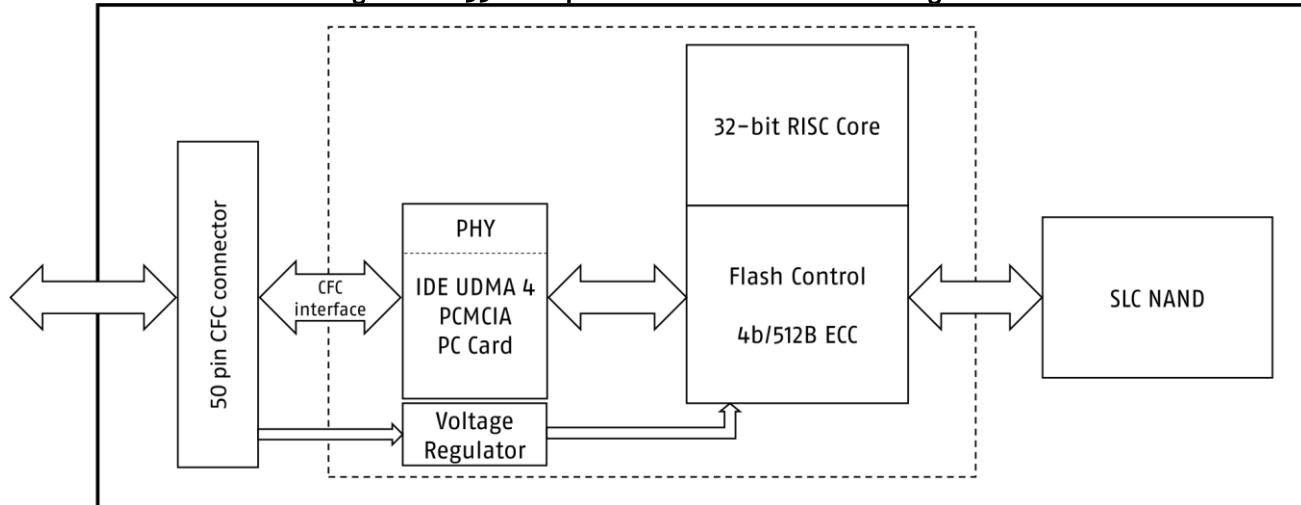
## 4. Product Description

The Swissbit C-350 series continues the successful CompactFlash™ C-300 series. It clearly pursues the goal of an equivalent product with long-term availability and reliability.

The CompactFlash™ card is an established removable device for industrial and NetCom applications as boot device or data storage.

The C-350 has an internal intelligent 32-bit RISC controller, which manages interface protocols, data storage and retrieval as well as hardware RS-code Error Correction Code (ECC), defect handling, diagnostics and clock control. The wear leveling mechanism assures an equal usage of the Flash memory cells to extend the lifetime.

**Figure 1: C-350 CompactFlash Functional Block Diagram**



The C-350 operates in three basic modes:

- PC card ATA I/O mode
- PC card ATA memory mode
- True IDE mode up to UDMA4, MDMA4, PIO4

The CompactFlash™ also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.

Standard cards are configured as max. PIO6 and MDMA4 (80ns) and UDMA4 (30ns).

If the cards should be used in extended speed modes, they should be qualified on the target system and the system should fulfill the signal requirements.

It conforms to the PCMCIA Card Specification 2.1 when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.

Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware RS-code ECC allows to detect and correct 4 symbols per 528 Bytes.

The Card has a voltage detector and a powerful power-loss management feature to prevent data corruption after power-down.

The specification has been realized and approved by the CompactFlash Association (CFA).

This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design.

### Related Documentation

- CF+ and CompactFlash™ Specification Revision 3.0
- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994

Detailed description in the CompactFlash specification

<https://www.compactflash.org/cfa-specifications>

## 4.1 Performance Specifications

The C-350 read/write sequential and random performance benchmarks are detailed in Table 3.

**Table 3: Read/Write Performance<sup>2</sup>**

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
32 MBytes	19.8	11.4	2,900	20
64 MBytes	19.8	11.4	2,900	20
128 MBytes	19.8	11.4	2,900	20
256 MBytes	19.8	11.4	2,900	20

## 4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in Table 4.

The current is about the same at 3.3V as for 5V.

**Table 4: Typical Current Consumption for max transfer speed at 5V (and 3.3V)<sup>3</sup>**

Drive Capacity	Sequential Read	Sequential Write	Random Read 4k	Random Write 4k	Idle	Unit
32 MBytes	110	115	95	80	2	mA
64 MBytes	110	115	95	80	2	
128 MBytes	110	115	95	80	2	
256 MBytes	110	115	95	80	2	

<sup>2</sup> The values are measured using CrystalDiskMark 6.0.2 x64 (CDM) at IDE interface in UDMA4 mode (Seq Q32T1 and 4KiB Q8T8). Performance depends on flash type and number, file/cluster size, and burst speed.

<sup>3</sup> All values are the typical recorded at 25 °C, with 5V supply voltage at fastest CrystalDiskMark 6.0.2 x64 at IDE interface.

## 4.3 Environmental Specifications

### 4.3.1 Recommended Operating Conditions

The recommended operating conditions for the C-350 CompactFlash Cards are provided in Table 5.

**Table 5: Recommended Operating Conditions**

Parameter	Value
Commercial Operating Temperature	0 °C to 70 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V <sub>CC</sub> Voltage	3.3 V ± 10% or 5V ± 10%

### 4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in Table 6.

**Table 6: Recommended Storage Conditions<sup>4</sup>**

Parameter	Value
Commercial Storage Temperature	-50 °C to 100 °C
Industrial Storage Temperature	-50 °C to 100 °C

### 4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in Table 7.

**Table 7: Shock, Vibration and Humidity**

Parameter	Value
Non-Operating Shock	1,500 g Peak (JESD22-B110)
Non-Operating Vibration	20 g Peak, 20-2000 Hz
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs (JESD22-A101)

<sup>4</sup> The data retention time at temperature above 40°C is reduced. Swissbit can provide more data and support on request.

#### 4.4 Regulatory Compliance

The C-350 devices comply with the regulations / standards listed in Table 8.

**Table 8: Regulatory Compliance**

Abbreviation	Regulation/ Standard
EMC	(EU) 2014/30 (FCC) 47 CFR Part 15
RoHS	(EU) 2011/65/EU with 2015/863 and 2017/2102
REACH	(EU) 1907/2006 and 207/2011
WEEE	(EU) 2012/19

#### 4.5 Mechanical Specifications

The C-350 Card has a female 50-pin CompactFlash™ connector. Physical dimensions are detailed in Table 9 below. Figure 2 at page 14 illustrates the C-350 dimensions and connector location.

**Table 9: Measured Physical Dimensions**

Physical Dimensions		Unit
Length	36.40±0.15	mm
Width	42.80±0.10	
Thickness (Max)	3.30±0.10	
Weight (Max Capacity)	10	g

## 4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

**Table 10: Reliability**

Parameter	Value
MTBF (at 25 °C)	> 3,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per $10^{14}$ Bits Read
Data Retention	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) for two different application scenarios is provided in Table 11.

**Table 11: Endurance<sup>5, 6</sup>**

Drive Capacity <sup>7</sup>	Sequential		Enterprise	
	TBW	DWPD <sup>8</sup>	TBW	DWPD <sup>8</sup>
32 MBytes	3.3	57	0.11	1.8
64 MBytes	6.5	55	0.20	1.7
128 MBytes	12	54	0.37	1.6
256 MBytes	25	54	0.76	1.6

## 4.7 Drive Geometry Specification

The C-350 CompactFlash card geometry is set to LBA settings as shown below in Table 12.

**Table 12: Drive Geometry**

Card Capacity	Cylinders	Heads	Sectors / track	Sectors (LBA)	Total addressable capacity (Bytes)
32 MBytes	496	4	32	63,488	32,505,856
64 MBytes	490	8	32	125,440	64,225,280
128 MBytes	937	8	32	239,872	122,814,464
256 MBytes	980	16	32	501,760	256,901,120

<sup>5</sup> Enterprise workload follows the JEDEC JESD219 standard. Enterprise workload values are measured based on 168 hours of runtime.  
<sup>6</sup> 1 MByte =  $10^6$  bytes

<sup>6</sup> According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. Swissbit recommends to calculate the service life based on target system mission profile.

<sup>7</sup> Based on 256 MBytes NAND size

<sup>8</sup> DWPD values are based on a service life of 5 years

## 5. Electrical Interface

### 5.1 Electrical Description

The CompactFlash™ Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode with MWDMA and UDMA, which is compatible with most disk drives

The signal/pin assignments are listed in Table 13. Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output.

The configuration of the Card is controlled using the standard PC card configuration registers starting at address 200h in the Attribute Memory space of the memory card. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.

All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specification" for definitions of Input and Output type.

Detailed description in the CompactFlash specification

<https://www.compactflash.org/cfa-specifications>

**Table 13: Pin Assignment and Pin Type**

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>(4)</sup>		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	D <sub>3</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>3</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>3</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
3	D <sub>4</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>4</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>4</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
4	D <sub>5</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>5</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>5</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
5	D <sub>6</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>6</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>6</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
6	D <sub>7</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>7</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>7</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
7	-CE1	I	I <sub>3</sub> U	-CE1	I	I <sub>3</sub> U	-CS0	I	I <sub>3</sub> Z
8	A <sub>10</sub>	I	I <sub>1</sub> Z	A <sub>10</sub>	I	I <sub>1</sub> Z	A <sub>10</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
9 <sup>(1)</sup>	-OE	I	I <sub>3</sub> U	-OE	I	I <sub>3</sub> U	-ATASEL	I	I <sub>3</sub> U
10	A <sub>9</sub>	I	I <sub>1</sub> Z	A <sub>9</sub>	I	I <sub>1</sub> Z	A <sub>9</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
11	A <sub>8</sub>	I	I <sub>1</sub> Z	A <sub>8</sub>	I	I <sub>1</sub> Z	A <sub>8</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
12	A <sub>7</sub>	I	I <sub>1</sub> Z	A <sub>7</sub>	I	I <sub>1</sub> Z	A <sub>7</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A <sub>6</sub>	I	I <sub>1</sub> Z	A <sub>6</sub>	I	I <sub>1</sub> Z	A <sub>6</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
15	A <sub>5</sub>	I	I <sub>1</sub> Z	A <sub>5</sub>	I	I <sub>1</sub> Z	A <sub>5</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
16	A <sub>4</sub>	I	I <sub>1</sub> Z	A <sub>4</sub>	I	I <sub>1</sub> Z	A <sub>4</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
17	A <sub>3</sub>	I	I <sub>1</sub> Z	A <sub>3</sub>	I	I <sub>1</sub> Z	A <sub>3</sub> <sup>(2)</sup>	I	I <sub>1</sub> Z
18	A <sub>2</sub>	I	I <sub>1</sub> Z	A <sub>2</sub>	I	I <sub>1</sub> Z	A <sub>2</sub>	I	I <sub>1</sub> Z
19	A <sub>1</sub>	I	I <sub>1</sub> Z	A <sub>1</sub>	I	I <sub>1</sub> Z	A <sub>1</sub>	I	I <sub>1</sub> Z
20	A <sub>0</sub> <sup>(11)</sup>	I	I <sub>1</sub> Z	A <sub>0</sub> <sup>(11)</sup>	I	I <sub>1</sub> Z	A <sub>0</sub>	I	I <sub>1</sub> Z
21	D <sub>0</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>0</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>0</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
22	D <sub>1</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>1</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>1</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
23	D <sub>2</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>2</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>2</sub>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
24	WP	0	0T <sub>3</sub>	-I0IS16 <sup>(10)</sup>	0	0T <sub>3</sub>	-I0IS16	0	0N <sub>3</sub>
25	-CD <sub>2</sub>	0	Ground	-CD <sub>2</sub>	0	Ground	-CD <sub>2</sub>	0	Ground
26	-CD <sub>1</sub>	0	Ground	-CD <sub>1</sub>	0	Ground	-CD <sub>1</sub>	0	Ground
27	D <sub>11</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>11</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>11</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
28	D <sub>12</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>12</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>12</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
29	D <sub>13</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>13</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D <sub>13</sub> <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>(4)</sup>		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
30	D14 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D14 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D14 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
31	D15 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D15 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D15 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
32	-CE2 <sup>(1)</sup>	I	I <sub>3</sub> U	-CE2 <sup>(1)</sup>	I	I <sub>3</sub> U	-CS <sub>1</sub> <sup>(1)</sup>	I	I <sub>3</sub> Z
33	-VS1	0	Ground	-VS1	0	Ground	-VS1	0	Ground
34	-IORD	I	I <sub>3</sub> U	-IORD	I	I <sub>3</sub> U	-IORD <sup>(7)</sup>	I	I <sub>3</sub> Z
							HSTROBE <sup>(8)</sup>		
							-HDMARDY <sup>(9)</sup>		
35	-IOWR	I	I <sub>3</sub> U	-IOWR	I	I <sub>3</sub> U	-IOWR <sup>(7)</sup>	I	I <sub>3</sub> Z
							STOP <sup>(8)(9)</sup>		
36	-WE	I	I <sub>3</sub> U	-WE	I	I <sub>3</sub> U	-WE <sup>(3)</sup>	I	I <sub>3</sub> U
37	READY	0	0T <sub>1</sub>	-IREQ	0	0T <sub>1</sub>	INTRQ	0	0Z <sub>1</sub>
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL <sup>(5)</sup>	I	I <sub>2</sub> Z	-CSEL <sup>(5)</sup>	I	I <sub>2</sub> Z	-CSEL	I	I <sub>2</sub> U
40	-VS2	0	OPEN	-VS2	0	OPEN	-VS2	0	OPEN
41	RESET	I	I <sub>2</sub> U	RESET	I	I <sub>2</sub> U	-RESET	I	I <sub>2</sub> U
42	-WAIT -DDMARDY <sup>(10)</sup> -DSTROBE <sup>(11)</sup>	0	0T <sub>1</sub>	-WAIT -DDMARDY <sup>(10)</sup> -DSTROBE <sup>(11)</sup>	0	0T <sub>1</sub>	IORDY <sup>(7)</sup> -DDMARDY <sup>(8)</sup> DSTROBE <sup>(9)</sup>	0	0N <sub>1</sub>
43	-INPACK -DMARQ <sup>(12)</sup>			-INPACK -DMARQ <sup>(12)</sup>			DMARQ		
44	-REG -DMACK <sup>(12)</sup>	I	I <sub>3</sub> U	-REG -DMACK <sup>(12)</sup>	I	I <sub>3</sub> U	-DMACK <sup>(6)</sup>	I	I <sub>3</sub> U
45	BVD2	I/O	I <sub>1</sub> U,0T <sub>1</sub>	-SPKR	I/O	I <sub>1</sub> U,0T <sub>1</sub>	-DASP	I/O	I <sub>1</sub> U,0N <sub>1</sub>
46	BVD1	I/O	I <sub>1</sub> U,0T <sub>1</sub>	-STSCHG	I/O	I <sub>1</sub> U,0T <sub>1</sub>	-PDIAG	I/O	I <sub>1</sub> U,0N <sub>1</sub>
47	D8 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D8 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D8 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
48	D9 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D9 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D9 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
49	D10 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D10 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>	D10 <sup>(1)</sup>	I/O	I <sub>1</sub> Z,0Z <sub>3</sub>
50	GND		Ground	GND		Ground	GND		Ground

- These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
- The signal should be grounded by the host.
- The signal should be tied to VCC by the host.
- The mode is required for CompactFlash™ Storage Cards.
- The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
- If DMA operations are not used, the signal must be held high or tied to VCC by the host, also for read registers.
- Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
- Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
- Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
- Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.
- Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.
- Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.
- Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

## 5.2 Electrical Specification

Table 14 defines the DC Characteristics for the CompactFlash Memory Card. Unless otherwise stated, conditions are:

- $V_{CC} = 5V \pm 10\%$
- $V_{CC} = 3.3V \pm 5\%$
- $0^\circ C$  to  $+85^\circ C$

Table 14 shows that the Card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.

The current is measured by connecting an amp meter in series with the  $V_{CC}$  supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms.

Table 15 shows the Input Leakage Current, Table 16 the Input Characteristics, Table 17 the Output Drive Type and Table 18 the Output Drive Characteristics.

**Table 14: Absolute Maximum Conditions**

Parameter	Symbol	Conditions
Input Power	$V_{CC}$	-0.3V to 6.5V
Voltage on any pin except $V_{CC}$ with respect to GND	$V$	-0.5V to $V_{CC} + 0.5V$

**Table 15: Input Leakage current(1)**

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	$V_{IH} = V_{CC}$	-10		10	$\mu A$
			$V_{IL} = GND$				
IxU	Pull Up Resistor	RPU1	$V_{CC} = 5.0V$	50		500	kohm
IxD	Pull Down Resistor	RPD1	$V_{CC} = 5.0V$	50		500	kohm

(1) x refers to the characteristics described in Table 16. For example,  $I_{U1}$  indicates a pull up resistor with a type 1 input characteristic.

**Table 16: Input characteristics**

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			$V_{CC} = 3.3V$			$V_{CC} = 5.0V$			
1, 2, 3	Input Voltage CMOS	$V_{IH}$	2.0		3.6	2.0		5.3	V
		$V_{IL}$	-0.3		0.8	-0.3		0.8	

**Table 17: Output Drive Type(1)**

Type	Output Type	Valid Conditions
Otx	Totempole	$I_{OH} \& I_{OL}$
Ozx	Tri-State N-P Channel	$I_{OH} \& I_{OL}$
Opx	P-Channel Only	$I_{OH}$ only
Onx	N-Channel Only	$I_{OL}$ only

(1) x refers to the characteristics described in Table 16. For example, OT3 refers to totem pole output with a type 3 output drive characteristic.

**Table 18: Output Drive Characteristics**

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1, 2, 3	Output Voltage	$V_{OH}$	$I_{OH} = -1mA$	2.4		VCC	V
		$V_{OL}$	$I_{OL} = 4mA$	0			
X	Tri-State	$I_{OZ}$	$V_{OL} = Gnd$	-10		10	$\mu A$
			$V_{OH} = V_{CC}$				

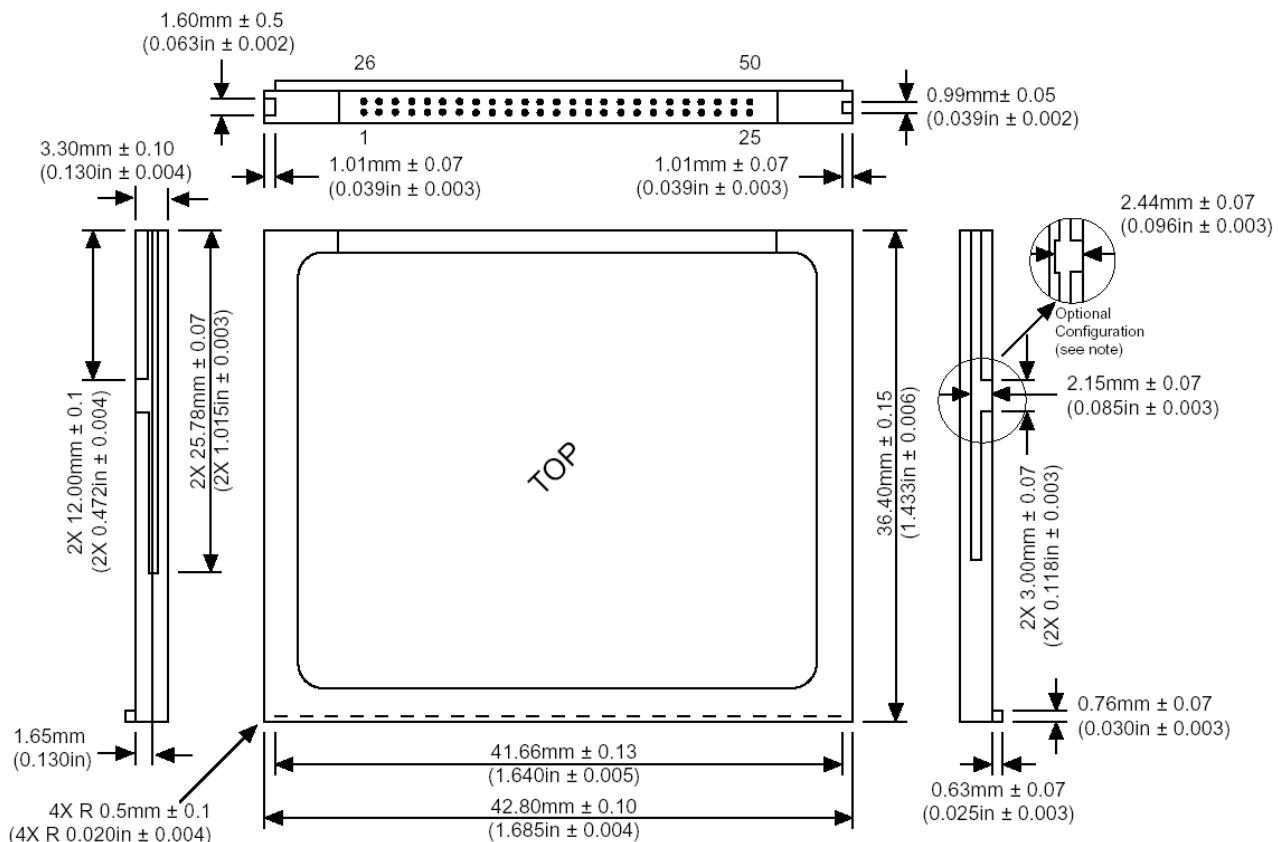
## 5.3 Additional requirements for CompactFlash Advanced Timing mode

When operating in a CompactFlash Advanced timing mode, the following conditions must be respected:

- Only one CompactFlash Card must be connected to the CompactFlash bus.
- The load capacitance (cable included) for all signals must be lower than 40pF.
- The cable length must be lower than 0.15m (6 inches). The cable length is measured from the Card connector to the host controller. 0.46m (18 inches) cables are not supported.

## 6. Package Mechanical

Figure 2: Type I CompactFlash™ Memory Card Dimensions in mm (inch)



## 7. CF-ATA Commands

This section defines the software requirements and the format of the commands the Host sends to the Card. Commands are issued to the Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Card is not busy (BSY is '0').

- **Class 1:** Upon receipt of a Class 1 command, the Card sets BSY within 400ns.
- **Class 2:** Upon receipt of a Class 2 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3:** Upon receipt of a Class 3 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP. Table 19 summarizes the CF-ATA command.

**Table 19: ATA Command Set**

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h					D	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Execute Drive Diagnostic	90h					D	
1	Flush cache	E7h					D	
2	Format track	50h		Y		Y	Y	Y
1	Identify Drive	Ech					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read DMA	C8		Y	Y	Y	Y	Y
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read native max address	F8h					D	
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
1	Set max address	F9h		Y	Y	Y	Y	Y
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	S.M.A.R.T.	B0h	Y	Y		Y	D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	E0h or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
1	Wear Level	F5h					Y	

2	Write Buffer	E8h					D	
2	Write DMA	CA		Y	Y	Y	Y	Y
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers,

DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use),

Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Memory Card and head parameters are used.

D – only the Compact Flash Memory Card parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

## 8. Identify Device Information

The following table describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

**Table 20: Identify Device Information**

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah*	2	General Configuration (REMOVABLE, signature of the CompactFlash Memory Card) In PCMCIA mode the HxBK cards have normally the value 848Ah but other configurations are possible
	045Ah*	2	Alternate Configuration FIX, In IDE mode the HxBK cards have normally the value 045Ah but other configurations are possible
1	XXXXh	2	Default number of cylinders
2	000oh	2	Reserved
3	00XXh	2	Default number of heads
4	000oh	2	Obsolete
5	0200h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per Card (Word 7 = MSW, Word 8 = LSW)
9	000oh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Reserved
23-26	aaaa*	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa*	40	Model number in ASCII (right justified) Big Endian Byte Order in Word ("SFCFxxxxHxBKxxx-x-xx-xxx-xxx")
47	800Xh	2	Maximum number of sectors on Read/Write Multiple command X=1 for cards with 1 flash, X=2 for cards with more flash
48	000oh	2	Reserved
49	0Fooh* 0Eooh*	2	Capabilities with DMA without DMA (also in PCMCIA mode)
50	000oh	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	000oh	2	Obsolete
53	0007h*	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	0100h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	000oh	2	Reserved.
63	0007h* 000oh*	2	Multi-Word DMA transfer. In PCMCIA mode, this value is '000oh'.
64	0003h	2	Advanced PIO modes supported
65	0078h* 000oh*	2	Minimum Multi-Word DMA transfer cycle time per Word. In PCMCIA mode, this value is '000oh'.
66	0078h* 000oh*	2	Recommended Multi-Word DMA transfer cycle time. In PCMCIA mode, this value is '000oh'.
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	000oh	22	Reserved
80-81	0020h 000oh	4	ATA version 5

Word Address	Default Value	Total Bytes	Data Field Type Information
82 -84	740Xh* 5004h* 4000h*	6	Features/command sets supported
85-87	740Xh* 1004h* 4000h*	6	Features/command sets enabled
88	101Fh*	2	Ultra DMA Mode Supported and Selected 0,1,2,3,4 (changes in operation)
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92-127	0000h*	72	Reserved
128	0000h	2	Security status
129-159	0000h	62	Vendor unique bytes
160	A064h*	2	Power requirement description (max. 100mA)*
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	0012h* 0000h*	2	CF Advanced True IDE Timing Mode Capability and Setting (PIO6/MDMA4)* In PCMCIA mode, this value is '0000h'.
164	001Bh* 0000h*	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability In PCMCIA mode, this value is '0000h'.
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

\* Standard values for full functionality, depending on Configuration

XXXX Depending on Card capacity and drive geometry

## 9. S.M.A.R.T. Functionality

The C-350 CF cards support the following SMART commands, determined by the Feature Register value.

**Table 21: S.M.A.R.T. Features Supported**

Feature	Operation
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute
D8h	SMART Enable Operations
D9h	Autosave SMART Disable Operations
DAh	SMART Return Status

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

### 9.1 S.M.A.R.T. Enable / Disable operations

This command enables / disables access to the SMART capabilities of the CF card. The state of SMART (enabled or disabled) is preserved across power cycles.

**Table 22: S.M.A.R.T. Enable / Disable operations (Feature D8h / D9h)**

Task File Register	7	6	5	4	3	2	1	0				
COMMAND	Boh											
DRIVE/HEAD	1	1	1	D	nu							
CYLINDER HI	C2h											
CYLINDER LOW	4Fh											
SECTOR NUM	nu											
SECTOR COUNT	nu											
FEATURES	D8h / D9h											

### 9.2 S.M.A.R.T. Enable / Disable Attribute Autosave

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the CF card.

**Table 23: S.M.A.R.T. Enable / Disable Attribute Autosave (Feature D0h)**

Task File Register	7	6	5	4	3	2	1	0				
COMMAND	Boh											
DRIVE/HEAD	1	1	1	D	nu							
CYLINDER HI	C2h											
CYLINDER LOW	4Fh											
SECTOR NUM	nu											
SECTOR COUNT	ooh or F1h											
FEATURES	D2h											

### 9.3 S.M.A.R.T. Read data

This command returns one sector of SMART data.

**Table 24: S.M.A.R.T. read data (Feature Doh)**

Task File Register	7	6	5	4	3	2	1	0				
COMMAND	Boh											
DRIVE/HEAD	1	1	1	D	nu							
CYLINDER HI	C2h											
CYLINDER LOW	4Fh											
SECTOR NUM	nu											
SECTOR COUNT	nu											
FEATURES	Doh											

The data structure returned is:

**Table 25: S.M.A.R.T. Data Structure**

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	ooh	Off-line data collection status (no off-line data collection)
363	ooh	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	ooh	
367	ooh	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	ooh	Error logging capability (no error logging)
371	ooh	
372	ooh	Short self-test routine recommended polling time
373	ooh	Extended self-test routine recommended polling time
374..385	ooh	Reserved
386..387	0002h	SMART Swissbit Structure Version
388..391		"Commit" counter
392..395		Wear Level Threshold
396		Global Bad Block management active
397		Global Wear Leveling active
398..510	ooh	
511		Data structure checksum

There are six attributes that are defined in the CF card. These return their data in the attribute section of the SMART data, using a 12 byte data field.

The field at offset 386 gives a version number for the contents of the SMART data structure. In version 0, the spare block counts (offsets 4 to 11) in the Spare Block Count attribute need to be byte-swapped.

In versions 0 and 1, the information at offsets 396 and 397 is not available.

The byte at offset 396 is 0 if the wear leveling has not yet started its global operation, and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold (typically 100000).

The byte at offset 397 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

### 9.3.1 Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

**Table 26: Spare Block Count Attribute**

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1..2	0003h	Flags – Pre-fail type, value is updated during normal operation
3		Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips ( $100 \times$ current spare blocks / initial spare blocks)
4..5		Initial number of spare blocks of the flash chip that has been used for the attribute value calculation
6..7		Current number of spare blocks of the flash chip that has been used for the attribute value calculation
8..9		Sum of the initial number of spare blocks for all flash chips
10..11		Sum of the current number of spare blocks for all flash chips

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

### 9.3.2 Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

**Table 27: Erase Count Attribute**

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block.
4..11		Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

### 9.3.3 Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

**Table 28: Total ECC Errors Attribute**

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC errors (correctable and uncorrectable)
8..11		-

### 9.3.4 Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

**Table 29: Correctable ECC Errors Attribute**

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of correctable ECC errors
8..11		-

### 9.3.5 UDMA CRC Errors Attribute

This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

**Table 30: UDMA CRC Errors Attribute**

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of UDMA CRC errors
8..11	-	

### 9.3.6 Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

**Table 31: Total Number of Reads Attribute**

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..11		Total number of flash read commands

## 9.4 S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute thresholds.

**Table 32: S.M.A.R.T. read data (Feature D1h)**

Task File Register	7	6	5	4	3	2	1	0				
COMMAND	Boh											
DRIVE/HEAD	1	1	1	D	nu							
CYLINDER HI	C2h											
CYLINDER LOW	4Fh											
SECTOR NUM	nu											
SECTOR COUNT	nu											
FEATURES	D1h											

The data structure returned is:

**Table 33: S.M.A.R.T. Data Structure**

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute threshold entries 1 to 30 (12 bytes each)
362..379	ooh	Reserved
380..510	ooh	-
511		Data structure checksum

**Table 34: Spare Block Count Attribute Threshold**

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1		Spare Block Count Threshold
2..11	ooh	Reserved

**Table 35: Erase Count Attribute Threshold**

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1		Erase Count Threshold
2..11	ooh	Reserved

**Table 36: Total ECC Errors Attribute Threshold**

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1	ooh	No threshold for the Total ECC Errors Attribute
2..11	ooh	Reserved

**Table 37: Correctable ECC Errors Attribute**

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1	ooh	No threshold for the Correctable ECC Errors Attribute
2..11	ooh	Reserved

**Table 38: UDMA CRC Errors Attribute**

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1	ooh	No threshold for the UDMA CRC Errors Attribute
2..11	ooh	Reserved

**Table 39: Total Number of Reads Attribute**

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1	ooh	No threshold for the Total Number of Reads Attribute
2..11	ooh	Reserved

## 9.5 S.M.A.R.T. Return Status

This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

**Table 40: S.M.A.R.T. read data (Feature D1h)**

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Boh							
DRIVE/HEAD	1 1 1 D nu							
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	DAh							

## 10. CIS Information (typical)

In PC-Card mode the C-350 card returns the Card information structure (CIS) with detailed information about the properties.

0000: Code 01, link 03

D9 01 FF

- 
- Device Info Tuple
  - Link is 3 bytes
  - I/O Device, No WPS, speed=250ns if no wait
  - (One) 2 Kilobytes of address space
  - End of CISTPL\_DEVICE
- 

000A: Code 1C, link 04

02 D9 01 FF

- 
- Other Conditions Info Tuple
  - Link is 4 bytes
  - Conditions: 3V operation is allowed, and WAIT is used
  - I/O Device, No WPS, speed = 250 ns if no wait
  - (One) 2 Kilobytes of address space
  - End of CISTPL\_DEVICE
- 

0016: Code 18, link 02

DF 01

- 
- JEDEC programming info Tuple
  - Link is 2 bytes
  - Device Manufacturer ID
  - Manufacturer specific info
- 

001E: Code 20, link 04

00 00 00 00

- 
- Manufacturer ID tuple
  - Link length is 4 bytes
  - PC Card manufacturer code
  - Manufacturer specific info
- 

002A: Code 21, link 02

04 01

- 
- Function ID tuple
  - Link length is 2 bytes
  - Fixed disk drive
  - R=0: no expansion ROM; P=1: configure at POST
- 

0032: Code 22, link 02

01 01

- 
- Function Extension tuple
  - Link length is 2 bytes
  - Disk interface information
  - PC card ATA interface
-

003A: Code 22, link 03

02 04 07

- Function Extension tuple
  - Link length is 3 bytes
  - PC card ATA basic features
  - D=0:single drive on card; U=0: no unique serial number; S=1: silicon device; V=0: no VPP required
  - I=0: twin IOIS16# unspecified; E=0: index bit not emulated; N=0: I/O includes ox3F7;
  - P=7: sleep, standby, idle supported
- 

0044: Code 1A, link 05

01 07 00 02 0F

- Configuration Tuple
  - Link length is 5 bytes
  - RFS: reserved; RMS: 1 byte register mask; RAS: 2 bytes base address
  - Last configuration entry is 07H
  - Configuration registers are located at 0200h
  - Configuration registers 0 to 3 are present
- 

0052: Code 1B, link 0B

C0 C0 A1 27 55 4D 5D 75 08 00 21

- Configuration tuple
  - Link length is 11 bytes
  - Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
  - W=1: wait required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=0: Memory interface
  - M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
  - DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
  - Nominal voltage 5.0V
  - Minimum voltage 4.5V
  - Maximum voltage 5.5V
  - Peak current 80 mA
  - Length of memory space is 2 Kbyte
  - X=0: no more misc fields; P=1: power-down supported; R0=0: read/write media; A=0: audio not supported; T=1: max twins is 1
- 

006C: Code 1B, link 06

00 01 21 B5 1E 4D

- Configuration tuple
  - Link length is 6 bytes
  - Memory mapped configuration, index=0
  - Power=1: VCC info, no VPP
  - PI=1: peak current info; NV=1: nominal voltage info
  - X=1: extension byte present
  - Nominal voltage 3.30V
  - Peak current 45 mA
- 

007C: Code 1B, link 0D

C1 41 99 27 55 4D 5D 75 64 F0 FF FF 21

- Configuration tuple
  - Link length is 11 bytes
  - Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
  - W=1: wait required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=0: Memory interface
  - M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
  - DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
-

- Nominal voltage 5.0V
  - Minimum voltage 4.5V
  - Maximum voltage 5.5V
  - Peak current 80 mA
  - Length of memory space is 2 Kbyte
  - X=0: no more misc fields; P=1: power-down supported; R0=0:read/write media; A=0: audio not supported; T=1: max twins is 1
- 

009A: Code 1B, link 06  
 01 01 21 B5 1E 4D

- Configuration tuple
  - Link length is 6 bytes
  - I/O mapped, index=1
  - Power=1: VCC info, no VPP
  - PI=1: peak current info; NV=1: nominal voltage info
  - X=1: extension byte present
  - Nominal voltage 3.30V
  - Peak current 45 mA
- 

00AA: Code 1B, link 12  
 C2 41 99 27 55 4D 5D 75 EA 61 F0 01 07 F6 03 01 EE 21

- Configuration tuple
  - Link length is 18 bytes
  - I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
  - W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=1: I/O interface
  - M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
  - DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
  - Nominal voltage 5.0V
  - Minimum voltage 4.5V
  - Maximum voltage 5.5V
  - Peak current 80 mA
  - R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; I0=10: 10 lines decoded
  - LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
  - Address range 1 ox1F0 to ox1F7
  - Address range 2 ox3F6 to ox3F7
  - S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported; M=0: masks V..N not present; IRQN=14: use interrupt 14
  - X=0: no more misc fields; P=1: power-down supported; R0=0:read/write media; A=0: audio not supported; T=1: max twins is 1
- 

00D2: Code 1B, link 06  
 02 01 21 B5 1E 4D

- Configuration tuple
  - Link length is 6 bytes
  - I/O mapped, index=2
  - Power=1: VCC info, no VPP
  - PI=1: peak current info; NV=1: nominal voltage info
  - X=1: extension byte present
  - Nominal voltage 3.30V
  - Peak current 45 mA
- 

00E2: Code 1B, link 12  
 C3 41 99 27 55 4D 5D 75 EA 61 70 01 07 76 03 01 EE 21

- Configuration tuple
  - Link length is 18 bytes
  - I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
-

- W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used;
  - Type=1: I/O interface
  - M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used;
  - T=0: no timing info specified; Power=1: VCC info, no VPP
  - DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
  - Nominal voltage 5.0V
  - Minimum voltage 4.5V
  - Maximum voltage 5.5V
  - Peak current 80 mA
  - R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; IO=10: 10 lines decoded
  - LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
  - Address range 1 ox170 to ox177
  - Address range 2 ox376 to ox377
  - S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported;
  - M=0: masks V..N not present; IRQN=14: use interrupt 14
  - X=0: no more misc fields; P=1: power-down supported; R0=0:read/write media;
  - A=0: audio not supported; T=1: max twins is 1
- 

010A: Code 1B, link 06

03 01 21 B5 1E 4D

- Configuration tuple
  - Link length is 6 bytes
  - I/O mapped, index=3
  - Power=1: VCC info, no VPP
  - PI=1: peak current info; NV=1: nominal voltage info
  - X=1: extension byte present
  - Nominal voltage 3.30V
  - Peak current 45 mA
- 

011A: Code 1B, link 04

07 00 28 D3

- Configuration tuple
  - Link length is 4 bytes
  - I/O mapped, index=7
  - No feature descriptions follow
  - Swissbit specific data
  - Swissbit specific data
- 

0126: Code 14, link 00

- 
- No link control tuple
  - Link length is 0 bytes
- 

012A: Code 15, link 14\*)

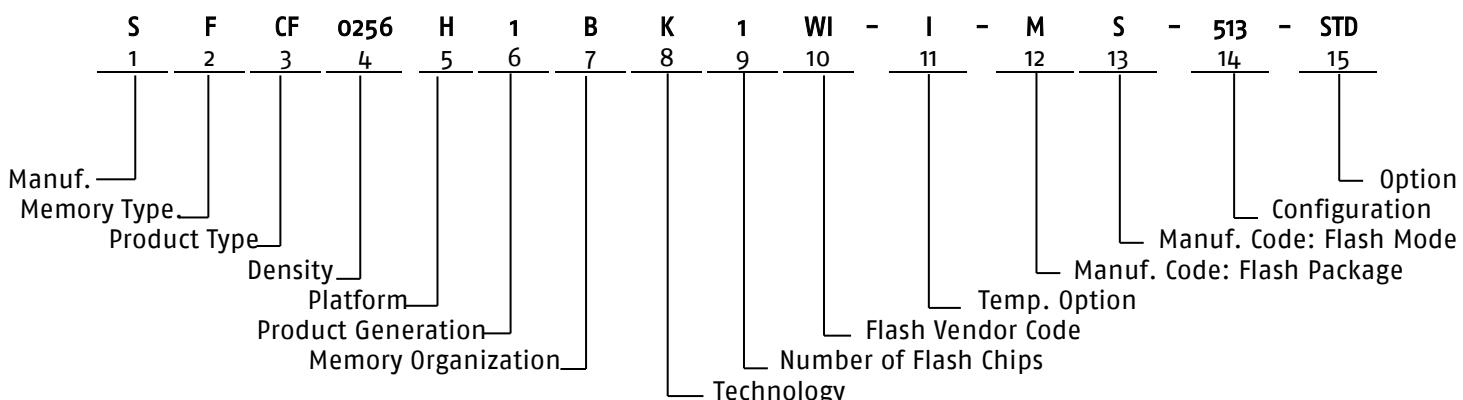
04 01 53 77 69 73 73 62 69 74 00 43 46 20 43 61 72 64 00 FF \*)

- Level 1 version/product info
  - Link length is 21 bytes
  - PCMCIA2.0/JEIDA4.1
  - PCMCIA2.0/JEIDA4.1
  - Product name: "Swissbit" "CF Card" \*) can vary in different configurations
  - The length of the strings will affect the following start addresses
- 

0156: Code FF, link FF

- 
- End of CISTPL\_VERS\_1
  - End of CIS
-

## 11. Part Number Decoder



### 11.1 Manufacturer

Swissbit code	S
---------------	---

### 11.2 Memory Type

Flash	F
-------	---

### 11.3 Product Type

CompactFlash	CF
--------------	----

### 11.4 Density

32 MBytes	0032
64 MBytes	0064
128 MBytes	0128
256 MBytes	0256

### 11.5 Platform

CompactFlash	H
--------------	---

### 11.6 Product Generation

First generation	1
------------------	---

### 11.7 Memory Organization

x8	A
----	---

### 11.8 Technology

C-350 Series	X
--------------	---

### 11.9 Number of Flash Chips

1 Flash	1
---------	---

### 11.10 Flash Code

Winbond	WI
---------	----

## 11.11 Temperature Option

Commercial Temperature Range: 0 °C to 70 °C	C
Industrial Temperature Range: -40 °C to 85 °C	I

## 11.12 Die Classification

SLC MONO (single die package)	M
-------------------------------	---

## 11.13 Pin Mode

Single nCE and Single R/nB	S
----------------------------	---

## 11.14 Drive configuration XYZ

X = Type

True IDE Mode	PC Card Mode	PIO	DMA support	X
Removable		yes	yes	1
	Fix	yes	yes	2
	Fix	yes	-	3
Removable		yes	-	4
Fix	Removable	yes	yes	5*
Fix	Removable	yes	-	6

\*default

Y = Firmware Revision

FW Revision	Y
First FW Revision	1

Z = Max Transfer Mode

Max PIO Mode / CIS	Z
PIO4 (MDMA2 if enabled)	1
PIO6 (MDMA4 if enabled)	2
UDMA4 (PIO6, MDMA4)	3*

\*default

## 11.15 Option

Standard	STD
Customer specific	XXX

## 12. Marking Specification

### 12.1 Top View

Figure 3: C-350 top view



### 12.2 Bottom View



### 12.3 Label Content

- Swissbit logo
- CF logo
- Part number (defined by the data sheet)
- Barcode as assembly lot number (Code128)
- Lot number
- CE logo
- RoHS logo
- WEEE logo
- Manufacturing date
- "Made in Germany"

## 13. Revision History

**Table 41: Document Revision History**

Date	Revision	Description	Revision Details
09-Oct-2020	0.90	Preliminary release	-
21-Oct-2020	1.00	Initial release	Doc. req. no. 4084

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