

Intel[®] Stratix[®] 10 DX FPGA Development Kit User Guide



ID: 683561 Version: 2020.11.16

UG-20255

Contents

1. Getting Started	4
1.1. About this Document	
1.2. Installing the Intel Quartus [®] Prime Pro Edition Software	
1.2.1. Activating Your License 1.3. Downloading the Board Package	
1.4. Installing the Driver for Intel FPGA Download Cable II	
2. Development Kit Overview	
2.1. Supported Features	
2.1. Supported reactines	
2.3. Handling the Board	
3. Power Up the Development Kit	9
3.1. Default Switch Settings	
3.2. Connectors and LEDs.	
3.3. Performing Board Restore through Board Test System (BTS)	
3.4. Controlling On-board Clock	.14
4. Board Test System (BTS)	15
4.1. Preparing the Development Kit	
4.2. Running the Board Test System	
4.3. Using the Board Test System	
4.3.1. Configure Menu	
4.3.2. Sys Info Tab 4.3.3. GPIO Tab	
4.3.4. QSFP Tab	
4.3.5. Component DDR4 CH0 Tab	
4.3.6. Component DDR4 CH1 Tab	
4.3.7. DDR ⁴ DIMM CH0 Tab	
4.3.8. DDR4 DIMM CH1 Tab	
4.3.9. Power Monitor	
4.3.10. Clock Controller	
4.4. Smart VID Setting	
5. Development Kit Hardware and Configuration	
5.1. FPGA Configuration	
5.2. Programming the FPGA Over Intel FPGA Download Cable	
5.3.1. Avalon Streaming Interface x8 Mode	
5.3.2. JTAG Mode	
6. Document Revision History for Intel Stratix 10 DX FPGA Development Kit User Guide	47
A. Development Kit Components	
A.1. Components Overview A.2. Power, Thermal, and Mechanical Considerations	
A.2. Power, mermar, and Mechanical Considerations A.2.1. Power Guidelines	
A.2.2. Thermal Requirements	
A.2.3. Mechanical Requirements	

A.3. Clock Circuits	
A.4. Memory Interface	
A.5. PCIe Interface	
A.6. UPI Interface	
A.7. Transceiver Signals: PCIe and UPI Interface	60
A.8. SlimSAS Connector	63
A.9. QSFP Network Interface	64
A.9.1. Dual Port Controller	65
A.10. I ² C Interface	
A.11. QSPI Flash Memory	67
A.11.1. Configuration QSPI Flash Memory	
A.11.2. NIOS QSPI Flash Memory	
B. Safety and Regulatory Information	
B.1. Safety Warnings	
B.2. Safety Cautions	
C. Compliance and Conformity Information	73



intel

1. Getting Started

1.1. About this Document

This document provides comprehensive guidelines for designing with Intel[®] Stratix[®] 10 DX FPGA Development Kit. It covers information about the software installation, board components, and configuration.

Table 1. Ordering Information

Product	Ordering Code	Device Part Number	
Intel Stratix 10 DX FPGA Development Kit (Production version)	DK-DEV-1SDX-P-A	1SD280PT2F55E1VG	

1.2. Installing the Intel Quartus[®] Prime Pro Edition Software

The Intel Quartus[®] Prime Pro Edition software includes everything you need to design for Intel Stratix 10 FPGA from design entry and synthesis to optimization, verification, and simulation. For more information about downloading the Intel Quartus Prime Pro Edition software, refer to the Download Center for Intel FPGAs.

1.2.1. Activating Your License

Before using the Intel Quartus Prime Pro Edition software, you must activate your license. If you already have a licensed version installed, you can use that license file with this development kit. Otherwise, follow these steps:

- 1. Log into your My Intel account.
- 2. Click on the Intel FPGA Self Service Licensing Center.
- 3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
- 4. On the Intel FPGA Self Service Licensing Center page, click the Find it with your License Activation Code link.
- 5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.

1.3. Downloading the Board Package

Download the appropriate board package for your Intel Stratix 10 DX FPGA Development Kit from the Intel FPGA Development Kits webpage. Unzip the package.

Figure 1. Directory Structure

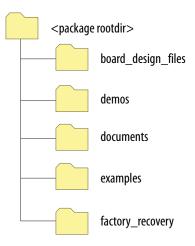


Table 2.Directory Description

Directory	Content Description		
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.		
demos	Contains demonstration applications when available.		
documents	Contains documentation.		
examples	Contains sample design files for this development kit.		
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board to its original factory settings.		

1.4. Installing the Driver for Intel FPGA Download Cable II

The development board includes integrated Intel FPGA Download Cable circuits for FPGA programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the Intel FPGA Download Cable II driver for your operating system are available on the Cable and Adapter Drivers Information webpage.



intel

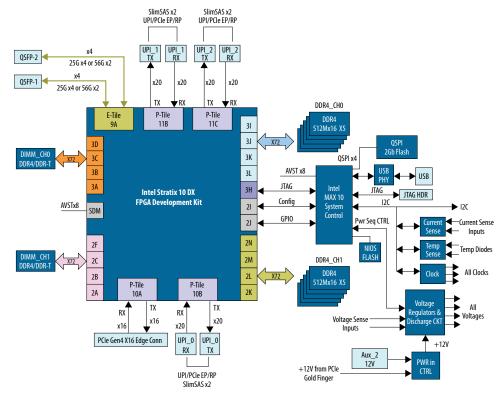


2. Development Kit Overview

The Intel Stratix 10 DX FPGA Development Kit allows you to evaluate the performance, features, and operation of the Intel Stratix 10 DX device in the F2912 BGA package. It features P-tile transceivers with PCIe Gen4 x16 and Intel Ultra Path Interconnect (UPI) interfaces and E-tile transceivers with 25Gx4 or 56Gx2 quad small form-factor pluggable (QSFP) interfaces. It also supports 4xDDR4 x72 channels with two channels supporting the Intel Optane[®] DC Persistent memory module.

The UPI functionality is enabled by a combination of the appropriate P-Tile settings and UPI protocol IP core. The FPGA interface to Intel Optane DC Persistent memory module requires an Intel memory controller IP core. Both IP cores are available in Intel Quartus Prime Pro Edition software (additional licensing and enablement may apply).

Figure 2. Intel Stratix 10 DX FPGA Development Kit Block Diagram



Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered



2.1. Supported Features

Table 3.Supported Features

Category	Features	
Intel Stratix 10 DX FPGA	 0.85-0.89V/VID-adjustable VCC core, 2912 pin BGA package P-Tile transceivers supporting PCIe Gen4 or UPI E-Tile transceivers supporting 28Gbps NRZ and 56Gbps PAM4 	
FPGA configuration	 Partial reconfiguration support CVP configuration support 2Gb QSPI Flash Storage for one configuration image in flash JTAG header for device programming Built-in Intel FPGA Download Cable for device programming 	
Programmable clock sources	 312.53125 Mhz and 156.25 MHz Differential LVDS for QSFP 100 Mhz Differential LVDS for PCIe 133 Mhz Differential LVDS for Memory 125 Mhz Configuration clock 100 Mhz Differential LVDS for IO banks 	
Transceiver interfaces	 PCIe x16 interface supporting Gen4 End-Point mode connected to a x16 PCIe edge connector (gold edge fingers) 2x standard QSFP56 optical module interfaces connected to the E-tile transceivers 3x UPI or PCIe interface supporting UPI x20 at 11.2Gbps or PCIe x16 at 16Gbps via SlimSAS connectors (cables shipped separately) 	
Memory interfaces	 Two on-board independent single rank DDR4 x72 (ECC) channels operating at 1200 (DDR4-2400) Two DIMM sockets supporting DDR4 DIMM or Intel's Optane DC Persistent memory module 	
Communication ports	 2xQSFP28 optical interface port JTAG header USB (Micro USB) on-board Intel FPGA Download Cable II System I2C header 	
Buttons, Switches, and LEDs	 System Reset Push button CPU Reset Push button PCIe Reset Push button Four dedicated User LEDs Link LED of each QSFP28 port to indicate the link and data transceiver Two dedicated configuration status LEDs 	
Heatsink and Fan	Air-cooled heatsink assemblyRed Over-Temperature Warning LED Indicator	
Power	 PCIe input power including required 2x4 AUX power connector Blue Power-On LED On/Off Slide Power Switch for benchtop operation On board power and temperature measurement circuitry 	
Mechanical	 PCIe standard height form factor 4.376" x 10.0" board size 2 Slots height with heatsink 	

2.2. Recommended Operating Conditions

Follow these operating range or limit for different physical parameters:





- Ambient operating temperature range: 0°C to 35°C
- Maximum ICC load current: 192 A
- Maximum ICC load transient percentage: 30%
- FPGA maximum power supported by the supplied heatsink/fan: 192 W

2.3. Handling the Board

When handling the board, it is important to observe static discharge precautions.

- **Caution:** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.
- *Important:* This development kit should not be operated in a vibrating environment.



intel

3. Power Up the Development Kit

The Intel Stratix 10 DX FPGA development kit is designed to operate in two modes:

- As a PCIe* add-in card
- Bench-top mode

When operating the card as a PCIe system, insert the card into an available PCIe slot and connect a 2x4 pin PCIe power cable from the system to power connectors at **J42** of the board.

Note: When operating as a PCIe add-in card, the board does not power on unless power is supplied to **J42**.

In Bench-top mode, you must supply the board with 240 W of power supply connected to the power connector **J42**.

This development kit ships with its switches preconfigured to support the design examples in the kit. If you suspect that your board may not be correctly configured with the default settings, refer to the *Default Switch and Jumper Settings* section of this chapter.

Follow these instructions:

1. Connect the supplied power supply to an outlet and the DC Power Jack (J42) on the FPGA board.

Note: Use only the supplied power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage.

2. Set the power switch (SW31) to the ON position.

When the board powers up, the blue LED illuminates and the board is ready for use. The Orange LED (**D56**) should also illuminate indicating that all the power rails on the board are good. If the POWER GOOD LED (**D56**) is not illuminated, it indicates that the power supply is malfunctioned and the board will not power up.

Note: The standby powers are always present as soon as the AUX power is applied to **J42**. Use power switch **SW31** to start the board.

3.1. Default Switch Settings

This development kit ships with its switches preconfigured to support the design examples in the kit. If you suspect that your board may not be correctly configured with the default settings, refer to the following table to return to its factory settings before proceeding.

Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.

Table 4.	Default Switch Settings
----------	-------------------------

Switch	Default Position	Description							
		Configuration mode setting bits:							
		Mode	MSEL0		MSEL1		MSEL2		QSPI_AVS
SW1[1:4]	ON/OFF/OFF/X	JTAG	OFF (Op	en)	en) OFF (Op		OFF (Open)		Х
		Avalon-ST	ON (Clo	se)	OFF (Open)	OFF	(Open)	X
		JTAG, MAX10,	UPI contr	rols:					
		SW33			ON (C	lose)		F (Open)	
		1 - JTAG Debu	g		G Heade icated f	er (J2) or Max1	0	Normal	JTAG (Default
SW33[1:4]	OFF/X/ON/ON	2 - JTAG SOUP	RCE	Not	used			Not use	d
		3 - UPI Mode		2 So	ockets			4 Socke	ts
		4 – M10 JTAG	EN	M10) JTAG E	Enabled		M10 JTA	AG Disabled
		PCIe PRSNT X	1/x4/x8/x	(16 se	ettings:				
SW2[1:4]	ON/ON/ON/ON	PCIe PRSNT 3	K1 PCIe	CIe PRSNT X4		PCIe P	PCIe PRSNT X8		PCIe PRSNT X16
		ON (Close)	ON (Close) ON (Close) ON (Clo		(Close	e)	ON (Close)		
SW28	ON (Close)	PCIe Edge connector PERSTn selection: • ON: Endpoint (Default) • OFF: Root Port							
SW27	ON (Close)	Intel Stratix 10 DX PERSTn selection: • ON: Endpoint (Default) • OFF: Root Port							
SW16	ON (Close)	UPI0 PERSTn selection - UPI0 connector side: • ON: PERSTn from PCIe Edge connector to FPGA • OFF: PERSTn from FPFA to CPU (Default)							
SW24	ON (Close)	UPIO PERSTn selection - FPGA side: • ON: PERSTn from FPGA to CPU (Default) • OFF: PERSTn from PCIe Edge connector to FPGA							
SW17	ON (Close)	UPI1 PERSTn selection - UPI1 connector side: • ON: PERSTn from PCIe Edge connector to FPGA • OFF: PERSTn from FPFA to CPU (Default)							
SW25	ON (Close)	 UPI1 PERSTn selection - FPGA side: ON: PERSTn from FPGA to CPU (Default) OFF: PERSTn from PCIe Edge connector to FPGA 							
SW18	ON (Close)	UPI2 PERSTn selection - UPI2 connector side: • ON: PERSTn from PCIe Edge connector to FPGA • OFF: PERSTn from FPFA to CPU (Default)							
SW26	ON (Close)	UPI2 PERSTn selection - FPGA side:							
									continued

3. Power Up the Development Kit 683561 | 2020.11.16

intel

Switch	Default Position	Description	
		 ON: PERSTn from FPGA to CPU (Default) OFF: PERSTn from PCIe Edge connector to FPGA 	
SW14	ON (Close)	 PCIe REFCLK source selection: ON: 100MHz REFCLK internal generated OFF: 100MHz REFCLK from PCIe Edge Connector (Default) 	
SW31	ON (Close) or OFF (Open)	 Power switch: ON: Turn on power (set to this position for use in PCIe slot) OFF: Turn off power This switch must be ON when the card is plugged into a PCIe slot Note: (with 2x4 Aux power connected) or on the bench with external ATX power supply. 	

Figure 3. Location of Switches and Push Buttons



Table 5. Push Buttons

Push Buttons		Descriptions	
S1 PCIe Reset		Push to reset PCIe bus	
S2	MAX10 Reset	Push to reset Max10	
S3	CPU Reset	Push to reset FPGA	
S4	USER Push Button	Push button for user assigned function	



3.2. Connectors and LEDs

Figure 4. Location of Connectors and LEDs

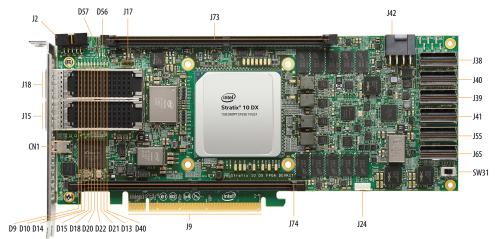


Table 6.Connectors

	Connector	Description
J2	External JTAG connector	For use with Intel FPGA Download Cable
J42	AUX Power connector	For external 12V AUX power supply or power adapter
J97	I2C/PMBus connector	For accessing the core power controller
J17	I2C connector	To access I2C bus
J15	QSFP 1 connector	
J18	QSFP 2 connector	For using the QSFP interface
CN1	USB connector	For programming FPGA using on-board Intel FPGA Download Cable
J73	DIMM 0 connector	For DDR4/DDR-T memory channel 0
J74	DIMM 1 connector	For DDR4/DDR-T memory channel 1
J9	PCIe x16 Gold Finger	For using the PCIe interface
J38	UPI 1 Transmit	For UPI Link 1 connection from FPGA to CPU
J40	UPI 1 Receive	For UPI Link 1 connection from CPU to FPGA
J39	UPI 2 Transmit	For UPI Link 2 connection from FPGA to CPU
J41	UPI 2 Receive	For UPI Link 2 connection from CPU to FPGA
J55	UPI 0 Transmit	For UPI Link 0 connection from FPGA to CPU
J65	UPI 0 Receive	For UPI Link 0 connection from CPU to FPGA
J24	Fan connector	For connecting to the heatsink cooling fan

•	
Inte	
	> ®

Table 7.LEDs

	LEDs	Description
D18	QSFP 1 Link LED for 25G	Green LED: • ON: link • Blinks: Activities
D20	QSFP 1 Link LED for 10G	Yellow LED: • ON: link • Blinks: Activities
D22	QSFP 2 Link LED for 25G	Green LED: • ON: link • Blinks: Activities
D21	QSFP 2 Link LED for 10G	Yellow LED: • ON: link • Blinks: Activities
D9	USER LED 0	Green LED for USER LED 0
D10	USER LED 1	Green LED for USER LED 1
D14	USER LED 2	Green LED for USER LED 2
D15	USER LED 3	Green LED for USER LED 3
D56	POWER GOOD LED	Yellow LED: • ON: All power is good • OFF: Power failure
D57	CONFIG DONE LED	Green LED: • ON: FPGA configuration successful • OFF: FPGA configuration failed
D13	MAX10 CONFIG DONE LED	Green LED: • ON: MAX10 configuration successful • OFF: MAX10 configuration failed
D40	Over Temp LED	Red LED: • ON: • OFF:
D53	POWER LED	Blue LED: • ON: Devkit power is on • OFF: Devkit power is off

3.3. Performing Board Restore through Board Test System (BTS)

The development kit ships with FPGA design examples stored in the QSPI flash device and pre-programmed Intel MAX[®] 10 system. If you want to restore the board QSPI flash with the default factory image, follow these steps:

- 1. Connect USB cable between CN1 USB connector and your computer.
- 2. Open Intel Quartus Prime Pro Edition Programmer.
- 3. Detect JTAG chain and attach factory default image on system Intel MAX 10 device.
- 4. Select programming options and click **Program** button.



3.4. Controlling On-board Clock

The clock controller application can change the on-board Si53XX programmable oscillators to any customized frequency between 0.2 MHz and 800 MHz.

The clock control application (ClockControl.exe) runs as a stand-alone application and resides in the location <package dir>\examples\board_test_system. The clock control application communicates with the system Intel MAX 10 device through either USB port CN1 or 10pin JTAG header J2. The system Intel MAX 10 device controls these programmable clock parts through a two-wire serial bus.





4. Board Test System (BTS)

The Intel Stratix 10 DX FPGA Development Kit includes an application called Board Test System (BTS) to test the functionality of this board. The BTS provides an easy-to-use Graphical User Interface (GUI) to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

The BTS communicates over the JTAG bus to a test design running in the Intel Stratix 10 DX FPGA device. You can use the BTS to reconfigure the FPGA with test designs specific to the functionality that you are testing.

The BTS is also useful as a reference for designing systems.

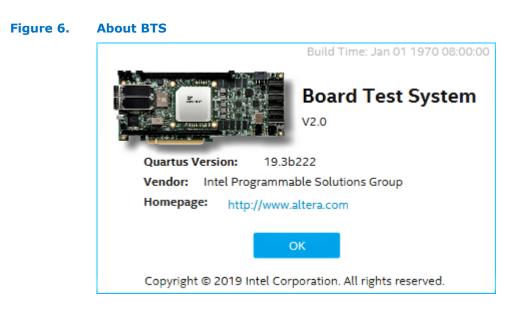
Figure 5. BTS GUI Home



Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered





4.1. Preparing the Development Kit

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The **Configure Menu** identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, an appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The BTS and Power Monitor share the JTAG bus with other applications like the Nios[®] II debugger and the Signal Tap II Embedded Logic Analyzer. Because the BTS is designed based on the Intel Quartus Prime software, be sure to close other applications before you use the BTS.

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, open the Intel Quartus Prime software to automatically set the environment variable \$QUARTUS_ROOTDIR. The BTS uses this environment variable to locate the Intel Quartus Prime library. The version of Intel Quartus Prime software set in the QUARTUS_ROOTDIR environment variable should be newer than version 14.1. For example, the Development Kit Installer version 15.1 requires that the Intel Quartus Prime software 14.1 or later version is installed.

Additionaly, to ensure that the FPGA is configured successfully, you should install the latest Intel Quartus Prime software that can support the silicon on the development kit. For this board, Intel recommends installing the Intel Quartus Prime version 19.3 b222.

Refer to the README.txt file under \examples\board_test_system directory.

4.2. Running the Board Test System

With the power to the board turned off, follow these steps:



- 1. Connect the USB cable to your PC and the board.
- 2. Check whether the board switches and jumpers are set according to your preferences.
- 3. Turn on the power to the board.

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached and the board is powered on.

To run the BTS, navigate to the <package dir>\examples\board_test_system directory and run the BoardTestSystem.exe application. A GUI appears, displaying the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, you will receive a message prompting you to configure your board with a valid BTS design. Refer to the Configure Menu on page 17 for configuring your board.

If some design is running in the FPGA, the BTS GUI loads the design file (.sof) in the image folder to check the current running design in the FPGA. Therefore, the design running in the FPGA must be the same as the design file in the image folder.

4.3. Using the Board Test System

This section describes each tab in the BTS.

4.3.1. Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different board features. Select a design from this menu and the corresponding tabs become active for testing.

Figure 7. Configure Menu



To configure the FPGA with a test system design, perform the following steps:





- 1. On the **Configure** menu, click the configure command that corresponds to the functionality you want to test.
- 2. In the dialog box that appears, click **Configure** to download the corresponding design to the FPGA.

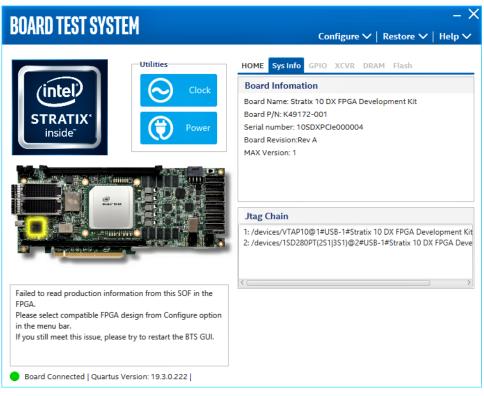
When configuration finishes, close the Intel Quartus Prime software GUI if it's already open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

Note: If you use the Intel Quartus Prime Programmer for configuration rather than the BTS GUI, you may need to restart the GUI.

4.3.2. Sys Info Tab

The Sys Info tab shows the board's current configuration. The tab displays the contents of the Intel MAX 10 registers, the JTAG chain, the Ethernet port numbers, and other details stored on the board.

Figure 8. Sys Info Tab



The following sections describe the controls of the Sys Info tab.

Board Information

Displays static information about your board:



- Board Name: Indicates the official name of the board given by the BTS.
- **Board P/N**: Indicates the part number of the board.
- Serial Number: Indicates the serial number of the board.
- **Board Revision**: Indicates the revision of the board.
- **MAX Version**: Indicates the version of Intel MAX 10 code currently running on the board.

JTAG Chain

Shows devices which are currently in the JTAG chain.

4.3.3. GPIO Tab

The **GPIO** tab allows you to interact with all the genral purpose user I/O components on your board. You can turn LEDs on or off.

Figure 9. GPIO Tab

BOARD TEST SYSTEM	Configu	− X ıre ∨ Restore ∨ Help ∨		
Utilities Utilities Clock Clock Over Clock Over	HOME Sys Info GPIO XCV User LEDs LED0 LED1 LE	R DRAM Flash		
	Qsys Memory Map			
	Block Description	Address		
	12C_0	0x0000.00C0 - 0000.00FF		
	I2C_1	0x0000.0100 - 0000.013F		
	I2C_2	0x0000.0140 - 0000.017F		
	I2C_dimm.csr	0x0000.0180 - 0000.01BF		
Detected bts_config.sof on FPGA.				
Board Connected Quartus Version: 19.3.0.222				

The following sections describe the controls on the GPIO tab:

User LEDs

Displays the current state of user LEDs. Toggle the LED buttons to turn the board LEDs on and off.





Qsys Memory Map

Shows the memory map of the GPIO or FLASH Platform Designer system on your board.

4.3.4. **QSFP** Tab

This tab allows you to perform loopback tests on the QSFP ports.

Figure 10.	QSFP Tab	
	BOARD TEST SYSTEM	– Ⅹ Configure ❤ Restore ❤ Help ❤
	<image/> <image/> <image/> <image/>	HOME Sys Info GPIO QSFP DRAM Flash Status PLL Lock: All Locked Detail Detail Pattern Sync: Not Synced Detail Detail Control PMA Setting Port PMA Setting Oata Type Error Control i Inserted Errors : 0 Inserted Errors : 0 Inserted Errors at : 0 Bit Error Rate : 0 Error Rate : 0 0% 0% DataRate Detarate
	Board Connected Quartus Version: 19.3.0.222	

The following sections describe the controls on the **QSFP** tab:

Status

Displays the following status information during a loopback test:



- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern sync:** Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern sync status:

Figure 11. PLL and Pattern Status

PLL and	Pattern Status	- 0	×
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
з	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

• QSFP x8

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
 - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
 - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
 - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
 - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- Equalizer: Specifies the RX tuning mode for receiver equalizer.

Figure 12. PMA Setting

PMA SET	TING												->
	Serial Loopback			Pre-er	npha	sis tap							
	LOOPDUCK	VOD		Pre-ta	ap 1	Pre-ta	ap 2	Pre-ta	ap 3	Post-	tap 1	Equalizer	
All CH	I		Ŧ		Ŧ		Ŧ		Ŧ		Ŧ		Ŧ
C110													
CH0		8	•	0	•	0	•	0		10	•	Stop	
CH1		8		0	-	0	-	0	-	10		Stop	-
CH2		8	•	0	•	0	•	0	•	10	•	Stop	•
CH3		8	*	0	*	0	*	0	•	10	•	Stop	•
CH4		8	•	0	•	0	•	0	•	10	•	Stop	*
CH5		8	-	0	•	0	•	0	•	10	•	Stop	*
CH6		8	•	0	•	0	•	0	•	10	•	Stop	•
CH7		8	*	0	•	0	•	0	•	10	•	Stop	•
								Oł	ĸ	С	ancel	Ap	ply

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7:** Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- **PRBS 31:** Selects pseudo-random 31-bit sequences.
- **HF:** Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transmit data stream.
- **Insert:** Inserts a one-word error into the transmit data stream each time you click the button. Insert is only enabled during transaction performance analysis.
- Clear: Resets the detected errors and inserted errors counters to zero.





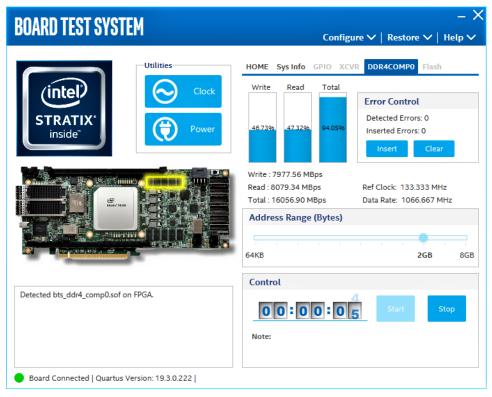
Loopback

- **Start:** Initiates the selected ports transaction performance analysis. Always click **Clear** before Start.
- Stop: Terminates transaction performance analysis.
- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

4.3.5. Component DDR4 CH0 Tab

This tab allows you to read and write Component DDR4 CH0 memory on your board.

Figure 13. Component DDR4 CH0 Tab



The following sections describe the controls on the **Component DDR4 CH0** tab:

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicator

These controls display current transaction performance analysis information collected since you last clicked Start:





- Write, Read and Total performance bars: Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Write (MBps), Read (MBps) and Total (MBps): Shows the number of bytes analyzed per second.
- **Data Bus:** 72-bits (8-bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum banwidth of 136,512 Mbps or 17,064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors:** Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zero.

Address Range

Determines the number of addresses to use in each iteration of reads and writes.

4.3.6. Component DDR4 CH1 Tab

This tab allows you to read and write Component DDR4 CH1 memory on your board.

Figure 14. Component DDR4 CH1 Tab

<complex-block> Vilies Image: System of DPD XCR DR4COMP1 Image: System of DPD XCR DR4COMP1 Image: System of DPD XCR Image: System</complex-block>	BOARD TEST SYSTEM	_ > Configure ❤ Restore ❤ Help ❤
		HOME Sys Info GPIO XCVR DDR4COMP1 Flash Write Read Total Error Control Detected Errors: 0 46.73% 47.32% 94.05% Inserted Errors: 0 Inserted Errors: 0 Write: 7977.58 MBps Ref Clock: 133.333 MHz Data Rate: 1066.667 MHz Address Range (Bytes) 64KB 2GB 8GB Control Start Stop

The following sections describe the controls on the **Component DDR4 CH1** tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked Start:

- Write, Read and Total performance bars: Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Write (MBps), Read (MBps) and Total (MBps): Shows the number of bytes analyzed per second.
- **Data Bus:** 72-bits (8-bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum banwidth of 136,512 Mbps or 17,064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:





- **Detected errors:** Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- Clear: Resets the detected error and inserted error counters to zero.

Address Range

Determines the number of addresses to use in each iteration of reads and writes.

4.3.7. DDR4 DIMM CH0 Tab

This tab allows you to read and write Dual Inline Memory Module (DIMM) DDR4 CH0 memory on your board.

Figure 15. DDR4 DIMM CH0 Tab

BOARD TEST SYSTEM	Configu	
<image/>	HOME Sys Info GPIO XCVF Write Read Total 46,73% 47,32% 94,05% Write : 7977.57 MBps Read : 8079.30 MBps Total : 16056.87 MBps Address Range (Bytes) 64KB Control OO = OO = O 4 Note:	Rdimm0 Flash Error Control Detected Errors: 0 Inserted Errors: 0 Inserted Errors: 0 Insert Clear Ref Clock: 133.333 MHz Data Rate: 1066.667 MHz IGB 8GB
Board Connected Quartus Version: 19.3.0.222		

The following sections describe the controls on the **DDR4 DIMM CH0** tab:

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.



Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked Start:

- Write, Read and Total performance bars: Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Write (MBps), Read (MBps) and Total (MBps): Shows the number of bytes analyzed per second.
- **Data Bus:** 72-bits (8-bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum banwidth of 136,512 Mbps or 17,064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zero.

Address Range

Determines the number of addresses to use in each iteration of reads and writes.

4.3.8. DDR4 DIMM CH1 Tab

This tab allows you to read and write Dual Inline Memory Module (DIMM) DDR4 CH1 memory on your board.





Figure 16. DDR4 DIMM CH1 Tab

BOARD TEST SYSTEM	> Configure ✔ Restore ✔ Help ✔
<image/> <image/>	
Detected bts_rdimm1.sof on FPGA.	00:00:05 Start Stop
Board Connected Quartus Version: 19.3.0.222	

The following sections describe the controls on the **DDR4 DIMM CH1** tab:

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked Start:

- Write, Read and Total performance bars: Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Write (MBps), Read (MBps) and Total (MBps): Shows the number of bytes analyzed per second.
- Data Bus: 72-bits (8-bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum banwidth of 136,512 Mbps or 17,064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:



- **Detected errors:** Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear:** Resets the detected error and inserted error counters to zero.

Address Range

Determines the number of addresses to use in each iteration of reads and writes.

4.3.9. Power Monitor

The Power Monitor measures and reports current power information and communicates with the Intel MAX 10 device on the board through the JTAG bus. A power monitor circuit attached to the Intel MAX 10 device allows you to measure the power that the Intel Stratix 10 DX FPGA is consuming.

To start the application, click the **Power Monitor** icon in the BTS. You can also run the Power Monitor as a stand-alone application. The PowerMonitor.exe resides in the cpackage dir>\examples\board_test_system directory.

Note: You cannot run the stand-alone power application and the BTS simultaneously. Also, you cannot run power and clock interface at the same time.

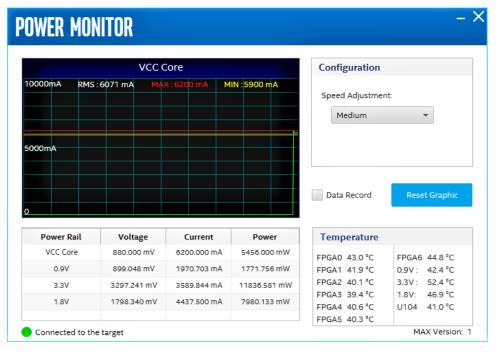


Figure 17. Power Monitor Interface



4.3.10. Clock Controller

The Clock Controller application sets the Si5391 programmable oscillators to any frequency between 0.16 MHz and 710 MHz.

The Clock Controller application sets the Si5332 programmable oscillators to any frequency between 0.1 MHz and 712.5 MHz.

The Clock Control communicates with the Intel MAX 10 on the board through the JTAG bus. The programmable oscillator are connected to the Intel MAX 10 device through a 2-wire serial bus.

Figure 18. Clock Controller - Si5391

Freque	ency(MH	z)				
OUTOA	Enable	•	156.25000	OUT5	Enable 🔹	100.00000
OUT0	Enable	•	156.25000	OUT6	Enable 🔹	100.00000
OUT1	Enable	•	312.50000	OUT7	Enable 🔹	100.00000
OUT2	Enable	•	312.50000	OUT8	Enable 🔹	100.00000
OUT3	Enable	•	312.50000	OUT9	Disable 🔹	312.50000
OUT4	Disable	•	312.50000	OUT9A	Enable 🔻	100.00000
_vco: 3750.00	000 MHz		Default	Read	Set	Import
	to the tai					

Figure 19. Clock Controller - Si5332

CLOCI	K CON	ITR	OLLER				- 3
Si5391	Si5332						
Frequ	iency(M	Hz)					
OUTO	Enable	•	100.00000	OUT4	Enable	•	133.33333
OUT1	Enable	•	125.00000	OUT5	Enable	•	133.33333
OUT2	Enable	•	133.33333	OUT6	Enable	•	100.00000
OUT3	Enable	•	133.33333	OUT7	Enable	•	100.00000
F_vco: 2	400.000 1	ИНz					
				Read		Set	Import
Connecte	ed to the t	arget					

Si5391 tab and Si5332 tab display the same GUI controls for each clock generators. Each tab allows for separate control. The Si5391 is capable of synthesizing four independent user-programmable clock frequencies up to 710 MHz.

The controls of the clock controller are described below:

F_vco

Displays the generating signal value of the voltage-controlled oscillator.

Register

Display the current frequencies for each oscillator.

Frequency

Allows you to specify the frequency of the clock in MHz.

Read

Reads the current frequency setting for the oscillator associated with the active tab.



Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK3 controls for the Si5391. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

Import

Import register map file generated from Silicon Laboratories ClockBuilder Desktop.

4.4. Smart VID Setting

If you are creating your own design and want to generate programming .sof file, you must add the correct Smart VID Setting into Intel Quartus Prime project for Intel Stratix 10 DX FPGA Development Kit to make configuration successfully. Before you add the following Smart VID setting into the .qsf file, you must change the configuration scheme to Avalon[®] streaming interface x8 for your project. You can also extract the Smart VID setting from the Golden Top file.

For Intel Stratix 10 DX FPGA Development Kit (Production):

<pre>set_global_assignment set_global_assignment set_global_assignment</pre>	-name -name -name -name -name -name -name -name -name -name -name -name	USE_CONF_DONE SDM_IO16 USE_CVP_CONFDONE SDM_IO5 VID_OPERATION_MODE "PMBUS MASTER" USE_PWRMGT_SCL SDM_IO0 USE_PWRMGT_SDA SDM_IO12 PWRMGT_BUS_SPEED_MODE "100 KHZ" PWRMGT_SLAVE_DEVICE_TYPE ED8401 PWRMGT_SLAVE_DEVICE0_ADDRESS 49 PWRMGT_SLAVE_DEVICE1_ADDRESS 00 PWRMGT_SLAVE_DEVICE2_ADDRESS 00 PWRMGT_SLAVE_DEVICE3_ADDRESS 00 PWRMGT_SLAVE_DEVICE5_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00 PWRMGT_SLAVE_DEVICE6_ADDRESS 00
<pre>set_global_assignment set_global_assignment set_global_assignment</pre>	-name -name -name	PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT" PWRMGT_LINEAR_FORMAT_N "-13" PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS PWRMGT PAGE COMMAND ENABLE OFF
sec_grobar_assignment	manie	FWINGT_FAGE_CONNAND_ENABLE OFF

For Intel Stratix 10 DX FPGA Development Kit (ES1):

set_global_assignment	-name	USE_CONF_DONE SDM_I016
set_global_assignment	-name	USE_CVP_CONFDONE SDM_105
set_global_assignment	-name	VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment	-name	USE_PWRMGT_SCL SDM_IO0
set_global_assignment	-name	USE_PWRMGT_SDA SDM_I012
set_global_assignment	-name	PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE_TYPE OTHER
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE0_ADDRESS 60
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE3_ADDRESS 00
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE4_ADDRESS 00
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE5_ADDRESS 00
set_global_assignment	-name	PWRMGT_SLAVE_DEVICE6_ADDRESS 00



set_global_assignment -name	PWRMGT_SLAVE_DEVICE7_ADDRESS 00
set_global_assignment -name	PWRMGT_VOLTAGE_OUTPUT_FORMAT "DIRECT FORMAT"
set_global_assignment -name	PWRMGT_DIRECT_FORMAT_COEFFICIENT_M 1
set_global_assignment -name	PWRMGT_DIRECT_FORMAT_COEFFICIENT_R 3
set_global_assignment -name	PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name	PWRMGT_PAGE_COMMAND_ENABLE OFF



5. Development Kit Hardware and Configuration

5.1. FPGA Configuration

Prerequisites:

- Install the Intel Quartus Prime Pro Edition and Intel FPGA Download Cable II driver on the host computer.
- Connect the micro-USB cable to the Intel Stratix 10 DX FPGA Development Kit.
- Power-on the board. Ensure that no running application is using the JTAG chain.

Follow these steps to configure the FPGA with your SRAM Object File (.sof) using the Intel Quartus Prime Pro Edition Programmer:

- 1. Start the Intel Quartus Prime Pro Edition Programmer.
- 2. Click **Auto Detect** to display the devices in the JTAG chain.
- 3. Click **Change File** and select the path to the desired *.sof file.
- 4. Turn on the **Program or Configure** option for the added file.
- 5. Click **Start** to download the selected file to the FPGA. The configuration is completed successfully when the progress bar reaches 100%.

Using the Intel Quartus Prime Pro Edition Programmer to configure a device on the board causes other JTAG- based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after the configuration is complete.

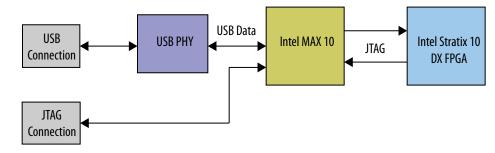
Note: While using the Intel Quartus Prime Pro Edition software version 19.3, you may observe occasional crash. Contact Intel support to access additional patch (0.01) for Intel Quartus Prime Pro Edition Programmer to mitigate this issue.

5.2. Programming the FPGA Over Intel FPGA Download Cable

The figure below shows the high-level conceptual block diagram for programming the Intel Stratix 10 DX FPGA over the embedded Intel FPGA Download Cable or external Intel FPGA Download Cable.



Figure 20. Programming Concept Block Diagram



5.3. Configuration Modes

The Intel Stratix 10 DX FPGA Development Kit supports two configuration modes:

- Avalon Streaming Interface x8 using the 2Gb QSPI Flash device (U66)
- **JTAG** using either the embedded Intel FPGA Download Cable or external Intel FPGA Download Cable.

5.3.1. Avalon Streaming Interface x8 Mode

The SDM block in the Intel Stratix 10 DX FPGA device controls the configuration process and interface. The Intel MAX 10 System Controller (U11) interfaces to Intel Stratix 10 DX FPGA in Avalon Streaming Interface X8 mode.

For Avalon Streaming Interface x8 mode, the MSEL[2:0] configuration pin strapping (SW1) must be set to [110] (which means SW1.1: ON (Close), SW1.2: OFF (Open), SW1.3: OFF (Open)).

5.3.1.1. Avalon Streaming Interface x8 Configuration Guideline

Ensure the following conditions are met before you proceed:

- The Intel Quartus Prime Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- If you are using an external JTAG programmer, ensure the Intel FPGA Download Cable II is connected to the board through the 10-pin female connector. Verfiy that the Intel FPGA Download Cable II LED for proper connection to the host computer through a micro-USB cable.
- Power to the board is on, and no other applications that use the JTAG chain are running.

Avalon Streaming Interface x8 Programmer Object File (.pof) Generation using the Intel Quartus Prime Pro Edition software version 20.1 or later

Note: If you already have the Programmer Object File (.pof), you can skip this section.

- Open the Intel Quartus Prime Pro Edition software and click on File > Programming File Generator to launch Programming File Generator tool.
- 2. In the **Device Family** list, select **Stratix 10**, and in the **Configuration mode** list, select **AVST x8** to specify the device and configuration mode.





- 3. In the **Output directory** tab, click **Browse** to specify the output directory for .pof file, in the **Name** column, input filename for .pof file.
- 4. In the **Description** column, select the **Programmer Object File (.pof)** and **Memory Map File (.map)** option.

Figure 21. Step 2 to 4 Illustration

Programming File Generator - [avstx8_mt25ql02.pfg]		-		
ile <u>W</u> indow		Search Intel FPGA		
Device family: Stratix 10 Configuration mode: AVST x8			•	
Output Files Input Files Configuration Device				
Specify one or more programming files to generate.				
Output directory: D:/S10_DX_FPGA/pcie_test/led_blinking_i	nt_clk		Browse	
Name: [led_blinking_int_clk_pfg				
Name: led_blinking_int_clk_pfg Description	File Name		Edit	
			Edit	
Description			Edit	
Description <u>Hexadecimal (Intel-Format) Output File for SRAM (.hex</u>	cout) led blinking int clk pfg.hexout		Edit	
Description Hexadecimal (Intel-Format) Outout File for SRAM (here ✓ Ørogrammer Object File (pof)	<pre>kout) led blinking int clk pfg.hexout led_blinking_int_clk_pfg.pof</pre>		Edit	
Description Hexadecimal (Intel-Format) Outout File for SRAM (.hex ✓ V Programmer Object File (.pof) V Memory Map File (.map)	kouth led_blinking_int_clk_pfg.hexout led_blinking_int_clk_pfg.pof led_blinking_int_clk_pfg_pof.map		Edit	
Description Hexadecimal (Intel-Format) Output File for SRAM (hex V V Programmer Object File (pof) V Memory Map File (map) Raw Binary File (rbf)	<u>kouti led blinking int clk pfg.hexout</u> led_blinking_int_clk_pfg.pof led_blinking_int_clk_pfg_pof.map led_blinking_int_clk_pfg.rbf		Edit	
Description Hexadecimal (Intel-Format) Output File for SRAM (hex V Programmer Object File (pof) V Memory Map File (map) Raw Binary File (rbf) Raw Binary File for CvP Core Configuration (.rbf)	kouti led blinking int clk pfg.hexout led_blinking_int_clk_pfg.pof led_blinking_int_clk_pfg_pof.map led_blinking_int_clk_pfg.rbf led_blinking_int_clk_pfg.core.rbf		Edit	

5. Click on **Input Files**>**Add Bitstream** tab to specify a .sof that contains the configuration bitstream.

Figure 22. Step 5 Illustration

Programming File Gene	rator - [avstx8_mt25ql02.pfg]					- 🗆 ×
Eile <u>W</u> indow					Sea	arch Intel FPGA
Device family:	Stratix 10					•
Configuration mod	e: AVST x8					•
Output Files	put Files <u>C</u> onfigura	tion Device				
Specify one or mor	e input files to convert					
Fil	e Path	Device	Compression	Encryption	HPS File	Add Bitstream
 Bitstream_1 led_blinkin 	g_int_clk.sof	1SD280PT2F55S1	On	Off		Add Raw Data
						Add File
						Remove
						Properties
4					•	
•					,	
						Reset <u>G</u> enerate

 Click on Configuration Device>Add Device to specify the flash device. In the Device list of the pop-up window, select CFI_2Gb for the configuration flash device.



 Click on OPTIONS row, and then click on Edit option to modify the start address. In the Address Mode list of the pop-up window, select Start; in the Start address list, input 0x00010000.

Figure 23. Step 7 Illustration

Programming File Gener	rator			- 0
e <u>W</u> indow				Search Intel FPGA
Device family:	Stratix 10			•
Configuration mode	e: AVST x8			•
Output Files	out Files	ration Device		
pecify the partition	n layout of the flash	image. Specify th	e flash loader if required.	
Device	Start	End	Input File	Add Device
CFI_2Gb				Add Partition.
OPTIONS P1	0x00010000 0x00000000	<auto> <auto></auto></auto>	None Bitstream_1 (led_blinking_osc_c	Edit
				Remove
lash loader:				Select
				<u>R</u> eset <u>G</u> enera

 Click on CFI_2Gb row, and then click Add Partition option. In the Input file list of pop-up window, select Bitstream (input_sof_file.sof); in the Address Mode list of pop-up window, select Start; in the Start address list, input 0x00100000.

Figure 24. Step 8 Illustration

🚏 Programming File Generate	or - [avstx8_mt25ql02.pf	g]		- 🗆 X
<u>File</u> <u>W</u> indow				Search Intel FPGA
Device family: Configuration mode: Qutput Files Inpu		ration Device		•
Specify the partition l	layout of the flash	image. Specify th	e flash loader if required.	
Device	Start	End	Input File	Add Device
CFI_2Gb				Add Partition
OPTIONS	0x00010000	<auto></auto>	None	Add Partition
P1	0x00100000	<auto></auto>	Bitstream_1 (led_blinking_int_cl	Edit
				Remove
Flash loader:				Select
				<u>R</u> eset <u>G</u> enerate

9. Click Generate to generate the .pof file.





Avalon Streaming Interface x8 Programmer Object File (.pof) Generation using the Intel Quartus Prime Pro Edition software version 19.3 or 19.4

The <code>avstx8.cof</code> and <code>avstx8.cdf</code> are included in the <code>factory_recovery</code> folder of installer package.

Note: If you already have the Programmer Object File (.pof), you can skip this section.

- 1. Open avstx8.cof using the text editor.
- 2. Change the .pof file name and directory based on your local output file name and directory, the location is marked as **1** in the figure below.
- 3. Change the .sof file name and directory based on your local input file name and directory, the location is marked as **2** in the figure below.

Figure 25. Step 2 and 3 Illustration

avstx8.cof ×
1 xml version="1.0" encoding="US-ASCII" standalone="yes"?
2⊟ <cof>Ş</cof>
3 <eprom name="">CFI 2GB</eprom> \$
4 <output_filename>C:/Laptop/Debug/S10_DX_FPGA/led_blinking/19.2/avstx8.pof{/output_filename></output_filename>
5 <n_pages>1</n_pages> 0
6 <width>1</width> \$
7 <mode>20</mode> 5
8日 <sof_data>0</sof_data>
<pre>9 <start_address>00100000</start_address>0</pre>
10 <user_name>Page_0</user_name> \$
11 <page_flags>1</page_flags> 0
<pre>13 <sof_filename< pre="">C:/Laptop/Debug/S10_DX_FPGA/led_blinking/19.2/bts_config.sof</sof_filename<></pre> /sof_filename> 14 - S
15 - 5 2
16
<pre>17 <create cvp="" file="">0</create>0</pre>
18 <create hps="" iocsr="">0/create hps iocsr>5</create>
<pre>is create rpd>000</pre>
20 <rr></rr> <rr> 21 22 23 24 24 24 24 25 26 27 27 28 29 20 </rr>
21 doptions>
22 <map file="">1</map> 9
23 <option address="" start="">10000</option> 9
24 <dynamic compression="">0</dynamic> 9
25 -
26 divanced options>3
27 <ignore check="" epcs="" id="">1</ignore> 3
<pre>28 <ignore_condone_check>2</ignore_condone_check>3</pre>
<pre>29 <plc_adjustment>0</plc_adjustment>00</pre>
<pre>30 <post_chain_bitstream_pad_bytes>-1</post_chain_bitstream_pad_bytes>\$</pre>
<pre>31 <pre></pre></pre>
32 <bitslice_pre_padding>1</bitslice_pre_padding> 0
33 - ©
34 L

- 4. Save the change and close the avstx8.cof file.
- Open the Intel Quartus Prime Pro Edition software 19.3 or later version, and click on File > Convert Programming Files to launch Convert Programming File tool.
- 6. Click on **Open Conversion Setup Data** to locate the recently saved avstx8.cof file and open it.

Figure 26. Step 6 Illustration

e Tools Window							
ecify the input files to co ou can also import input f	nvert and the type of progra file information from other fil		setup information creat	ted here for		Search Intel F	PGA
ure use. nversion setup files							
inversion setup mes	Open Conversion Setup	Data		Save Conver	rsion Setup		
itput programming file							
Programming file type:	Programmer Object File	(.pof)					
Options/Boot info	Configuration device:	CFI_2Gb		▼ <u>M</u> ode:	AVST x8		Ŧ
ile <u>n</u> ame:	./test.pof						
Advanced							
Advanced	Remote/Local update diff Create Memory Map F Create CVP files (Gene	ile (Generate test.map)	NONE				
	Create Memory Map F						
out files to convert	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test	Lcore.rbf) Start Address			Add Heg	*
but files to convert	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test D (Generate test_auto.rpd)	.core.rbf)			Add Heg Add Sof	Data
ut files to convert File/ Options	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test D (Generate test_auto.rpd) Properties	Start Address 0x00010000				; Dat
ut files to convert File/ Options ▼ SOF Data	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test D (Generate test_auto.rpd) Properties Page_0	Start Address 0x00010000			Add <u>S</u> of	; Dati i Pag
ut files to convert File/ Options ▼ SOF Data	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test D (Generate test_auto.rpd) Properties Page_0	Start Address 0x00010000			Add <u>S</u> of Add <u>F</u> i	; Data i Page ile vve
put files to convert File/ Options ▼ SOF Data	Create Memory Map F	ile (Generate test.map) rate test.periph.pof and test D (Generate test_auto.rpd) Properties Page_0	Start Address 0x00010000			Add <u>S</u> of Add <u>F</u> i Remo	; Data ; Page ile

7. Click Generate to generate the .pof file.

QSPI Flash Programming with Avalon Streaming Interface x8 Configuration Testing

- 1. Open avstx8.cdf using the text editor.
- 2. Change the .pof file name and directory based on your local output file name and directory, the location is marked as **1** in the figure below. Ensure to save the file.

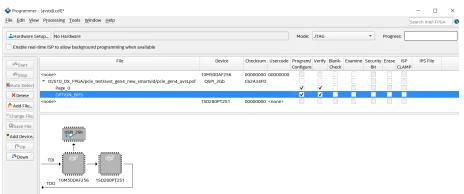
Figure 27. Step 2 Illustration

avstv8.cdf × quartus.ini ×
<pre>1 /* Quartus Prime Version 19.3.0 Internal Build 185 08/01/2019 SC Pro Edition */0 2 GedecChain; 3 FileRevision(JESD32A); 4 DefaultMfr(6E); 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5</pre>
<pre>P ActionCode(Ign) Perice PartName(1050DAP256) MfrSpec(OpMask(0) SEC_Device(QSPI_2GB) Child_OpMask(3 0 3 3) PFLPath[*D:/S10_DX_FPGA/avstx8/pcie_ep_u10.po P ActionCode(Ign) P ActionCode(Ign) Povice PartName(ISD2S0PT2S1) MfrSpec(OpMask(0)); </pre>
us S 11 ChainEnd; S

- 3. Change switch **SW33.1** to OFF (1'b0:far from board edge) position for normal JTAG mode.
- 4. Plug in the USB dongle to external JTAG header (**J2**) or plug in the USB cable into micro USB port (**CN1**).
- 5. Plug ATX Power into **J42**, switch **SW31** to turn ON the Intel Stratix 10 FPGA power.
- 6. Open the Intel Quartus Prime Pro Edition software 19.3 or later version, and open avstx8.cdf file.



Figure 28. Step 6 Illustration



7. Click on **Hardware Setup** in the Intel Quartus Prime Programmer to change **Hardware frequency** to 16 MHz.

Use the following command to change TCK frequency to 16 MHz:

jtagconfig --setparam <cable_number> JtagClock 16M

- 8. Click on **Start** to start QSPI Flash programming.
- After programming is successful, change switch SW31 to power OFF, and unplug the ATX power from J42 to completely power down the development kit. Change the MSEL(SW1) to 110 (AVSTx8, SW1.1: ON (Close), SW1.2: OFF (Open), SW1.3: OFF (Open))

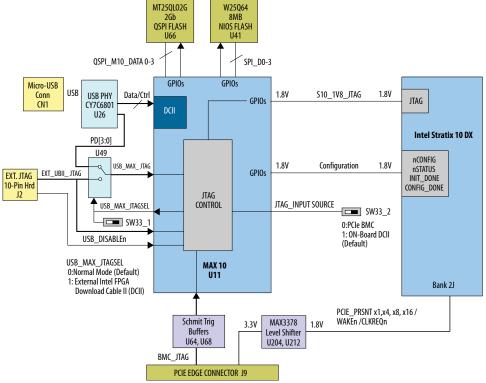
Note: If the development kit is installed in the server, you must power off the server and power it on to completely power cycle the development kit.

10. Plug ATX Power into J42 and change switch **SW31** to power ON the development kit. Observe whether the **D57** is ON (ON means the AVST x8 configuration is successful).

5.3.2. JTAG Mode

The JTAG Switch implemented in the Intel MAX 10 System Control (U11) allows the selection of the device(s) to be included in the JTAG chain. It is done by the settings of the DIP switch SW33. The embedded Intel FPGA Download Cable (or external Intel FPGA Download Cable) or PCIe JTAG can be selected as the source for programming the device(s) on the chain. The embedded Intel FPGA Download Cable is the default setting for this configuration mode.

Figure 29. JTAG Chain



The on-board Intel FPGA Download Cable is implemented in a Intel MAX 10 device. A micro-USB connector connecting to a CY7C68013A USB2 PHY provides the data to Intel MAX 10 device. This allows you to configure the FPGA using a USB cable, which is directly connected to a host PC running Intel Quartus Prime Pro Edition software without requiring the external Intel FPGA Download Cable.

You can also use the external Intel FPGA Download Cable on J2 to configure the FPGA.



Send Feedback



6. Document Revision History for Intel Stratix **10 DX FPGA** Development Kit User Guide

Document Version	Changes
2020.11.16	Clarified the Smart VID Setting for ES1 and Production version of the Intel Stratix 10 DX FPGA Development Kit.
2020.11.04	Sections updated: About this Document on page 4 Default Switch Settings on page 9 Connectors and LEDs on page 12 Smart VID Setting on page 32 Development Kit Components on page 43 Components Overview on page 44 Power Distribution on page 49 Power Measurement on page 52 I2C Interface on page 66
2020.08.17	Clarified the default position for Switch Settings.
2020.04.20	Updated steps in section: Avalon Streaming Interface x8 Programmer Object File (.pof) Generation.
2019.12.09	Initial release.



A. Development Kit Components

This appendix provides detailed information about the Intel Stratix 10 DX FPGA Development Kit components.

Figure 30. Development Kit Front

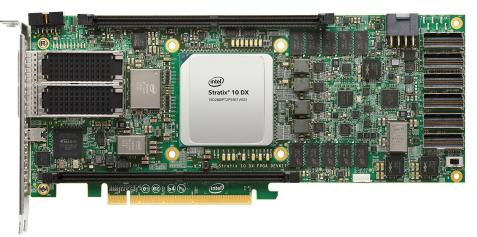


Figure 31. Development Kit Back



Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

A.1. Components Overview

Table 8. Intel Stratix 10 DX FPGA Development Kit Components

Board Reference	Component	Description
	Featur	red Devices
U1	Intel Stratix 10 DX FPGA	 Logic elements: 2.8M DSP blocks: 5760 M20K memory blocks: 11721 Package type: 2912 BGA Transceiver count: 84 4x P-Tile supporting PCIe X16 Gen4 (16 Gb/s) or UPI X 20 (1up to 11.2 GT/s) 1x E-Tile transceiver supporting 2x 56Gbps PAM4 or 4x 25Gbps NRZ
U11	Intel MAX 10	 Logic elements: 50K Package type: 256 FBGA 1.8V VCCINT
	Cloc	k Circuits
X4	Intel MAX 10 Reference Clock	The crystal oscillator provides the reference clock for Intel MAX 10 device: • Out= 125.00 MHz
U7	Programmable Clock Generator Si5332A	Default frequencies: • Out0 = 100.00 MHz • Out1 = 125.00 MHz • Out2 = 133.333MHz • Out3 = 133.333MHz • Out4 = 133.333 MHz • Out5 = 133.333MHz • Out6 = 100.00 MHz • Out7 = 100.00MHz
U9	Programmable Clock Generator Si5391A	Default frequencies: • CLK0 = 156.25MHz • CLK0A = 156.25 MHz • CLK1 = 312.50 MHz • CLK2 = 312.50 MHz • CLK3 = 312.50 MHz • CLK4 = Not used • CLK5 = Not used • CLK5 = Not used • CLK6 = 100.00 MHz • CLK8 = 100.00 MHz • CLK9 = 100.00 MHz • CLK9A = 100.00 MHz
	Transceiv	ver Interfaces
39	PCIe x16 gold fingers	PCIe TX/RX x16 interface from FPGA P-tile 10A
J38	PCIe x16 or UPI x20, Link 1	PCIe/UPI Transmit interface from FPGA P-tile 11B
J40	PCIe x16 or UPI x20, Link 1	PCIe/UPI Receive interface from FPGA P-tile 11B
J39	PCIe x16 or UPI x20, Link 2	PCIe/UPI Transmit interface from FPGA P-tile 11C continued

Board Reference	Component	Description
J41	PCIe x16 or UPI x20, Link 2	PCIe/UPI Receive interface from FPGA P-tile 11C
J55	PCIe x16 or UPI x20, Link 0	PCIe/UPI Transmit interface from FPGA P-tile 10B
J65	PCIe x16 or UPI x20, Link 0	PCIe/UPI Receive interface from FPGA P-tile 10B
J15	QSFP 1 connector	Four TX/RX channels from FPGA Bank 4F
J18	QSFP 2 connector	Four TX/RX channels from FPGA Bank 4F
	General Us	er Input/Output
D9, D10, D14, D15	User defined LEDs	Four green-color user LEDs. Illuminates when driven low
	M	lemory
J73	DDR4 x72 DIMM connector	 One X72 memory interface supporting DDR4 (x72) or Intel Optane DC Persistent memory module: DDR4 memory (x72) 1333 MHz Intel Optane DC Persistent memory (requires memory controller IP core)
J74	DDR4 x72 DIMM connector	 One X72 memory interface supporting DDR4 (x72) or Intel Optane DC Persistent memory module: DDR4 memory (x72) 1333 MHz Intel Optane DC Persistent memory (requires memory controller IP core)
U142, U143, U144, U145, U146	On-board DDR4 x72 Memory interface	This on-board DDR4 x72 memory supports 8 GB at up to 1200 MHz
U152, U153, U154, U155, U156	On-board DDR4 x72 Memory interface	This on-board DDR4 x72 memory supports 8 GB at up to 1200 MHz
U41	NIOS Flash 64K-bit	This on-board Flash is for Intel MAX 10
U66	QSPI 2 Gbit NOR Flash	This on-board Flash is for image storage for FPGA
	Commur	nication Ports
J9	PCI Express x16 edge connector	Gold-plated edge fingers for up to x16 signaling in either Gen1, Gen2, Gen3, or Gen4 mode
J15	QSFP 1 Interface	Provides four transceiver channels for a 100G QSFP module
J18	QSFP 2 Interface	Provides four transceiver channels for a 100G QSFP module
J97	I2C/PMBus connector	For accessing core power controller
J17	I2C connector	For cccessing the I2C1 bus
32	External JTAG Port	This port allows the use of Intel FPGA Download Cable II dongle to access the JTAG links on the board. Connection to this port automatically disables the internal Intel FPGA Download Cable II JTAG.
CN1	Micro-USB connector	Embedded Intel Intel FPGA Download Cable II JTAG for programming the FPGA via USB cable.
	Pow	er Supply
J9	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard for 12V power source
J42	DC input jack	Accepts a 12 V DC power supply when powering the board from the provided power brick for lab bench operation.
		continued

A. Development Kit Components 683561 | 2020.11.16



Board Reference	Component	Description
		When operating from the PCIe slot, this input must also be connected to the 8-pin Aux PCIe power connector provided by the PC system along with J42, or else the board will not power on.
SW31	Power switch	Switch to power ON or OFF the board when supplied from the DC input jack
U217	12V Hot Swap Controller	Provide protection for AUX power input (J42)
U96	12V Hot Swap Controller	Provide protection for PCIe slot power input (J9)
U93	Controlled power FET	Perform power bridging function between AUX2 and PCIe slot when the board is not used in PCIe system
U101	3.3V Voltage regulator	Provides 3.3V to power system
U99	5V Voltage regulator	Provides 5V to power system
U47,U240,U77,U24 1,U242	4-phase VCC Core Voltage regulator	Provides power to VCC core of Intel Stratix 10 FPGA
U230	0.9V Voltage regulator	Provides power to all power rails in Group 1
U113	1.8V Voltage regulator	Provides power to VCCPT and other rails in Group 2
U186	1.8V Voltage regulator	Provides power to VCCH and VCCCLK for P-tiles
U184	1.1V Voltage regulator	Provides power to VCCH for E-tile
U78	2.5V Voltage regulator	Provides power to VCCCLK for E-tile
U76	2.4V Voltage regulator	Provides power to VCCFUSEWR_SDM of Intel Stratix 10 FPGA
U188	1.8V Voltage regulator	Provides power to VCCIO of Intel Stratix 10 FPGA
U116	1.2V and 2.5V Voltage regulator	Provides power to Intel MAX 10 core and other rails
U79	1.8V Voltage regulator	Provides power to VCCIO of Intel MAX 10
U163	2.5V Voltage regulator	Provides power to DDR4 Channel 0
U164	0.6V Voltage regulator	Provides power to DDR4 VTT Channel 0
U159	1.2V Voltage regulator	Provides power to DDR4 Channel 0
U165	2.5V Voltage regulator	Provides power to DDR4 Channel 1
U166	0.6V Voltage regulator	Provides power to DDR4 VTT Channel 1
U157	1.2V Voltage regulator	Provides power to DDR4 Channel 1
U192, U193	0.6V Precision voltage reference	Provides reference voltage to DDR4 Channel 0 and Channel 1
U136	Controlled power FET	Control power to all memory voltage regulators
U51	Power protector	Provides power protection to QSFP 1 (J16)
U52	Power protector	Provides power protection to QSFP 2 (J18)



A.2. Power, Thermal, and Mechanical Considerations

A.2.1. Power Guidelines

This section describes the power supply for Intel Stratix 10 DX FPGA Development Kit.

A laptop-style DC power supply is provided with the development kit. Use only the supplied power supply. The power supply has an auto-sensing input voltage of 100-240 V AC power and will output 12 V DC power at 20 A to the development board. The 12 V DC input power is then stepped down to various power rails used by the board components.

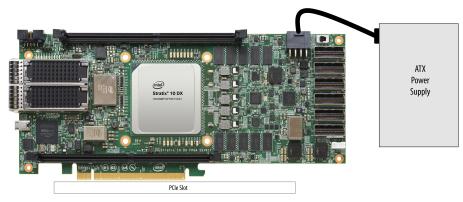
An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed on a graphical user interface (GUI) that can graph power consumption versus time.

The Intel Stratix 10 DX FPGA Development Kit has two modes of operation:

• Standard PCIe compliant system

In this mode, plug the board into an available PCI Express slot and connect the standard 2x4 power cords available from the PC's ATX power supply to J11 on the board. The PCIe slot together with the auxiliary PCIe power cords are required to power the entire board. If you do not connect the 2x4 auxiliary power connection, the board does not power on. The power switch SW3 is ignored when the board is used in the PCIe system.

Figure 32. Setup Example





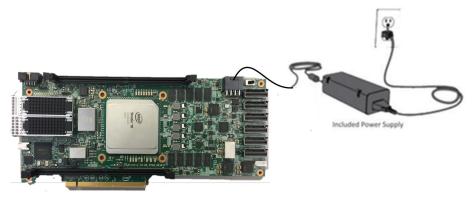


Standalone evaluation board powered by included power supply

In this mode, plug the included power supply into the 2x4 pin connector (J42) and the AC power cord of the power supply into a power outlet. This power supply provides the entire power to the board without the need to obtain power from the PCIe slot. The power switch SW31 controls powering of the board.



•



A. Development Kit Components 683561 | 2020.11.16



A.2.1.1. Power Distribution

The power distribution system on the Intel Stratix 10 DX FPGA Development Kit is shown below.



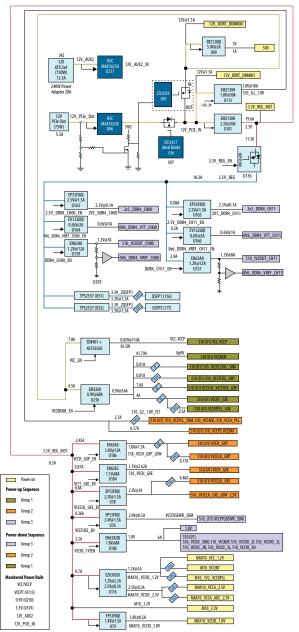






Table 9. Power Supply List

Source Name	Power Name	Maximum Output Current (A)	Description
	VCC	100	Core logic power
ED8401(U47)	VCCP	160	Periphery power
	S10_VCCERAM		Embedded memory and digital transceiver power
	VCCPLLDIG_SDM		Digital PLL power for SDM
	S10_VCCFUSE_GXP		Fuse power for P-Tile
EN2260 (U230) 0.9V	S10_VCCRT_GXP	53	Analog power for high speed circuits P-Tile
	S10_VCCRT_GXE		Analog power for high speed circuits E-Tile
	S10_VCCRTPLL_GXE		PLL power for E-Tile
	S10_VCCPLL_SDM		SDM PLL power
	S10_VCCADC		ADC power
EN2130H (U113) 1.8V	S10_VCCA_PLL	18	Analog power for PLL
	S10_VCCPT		
	S10_VCCBAT		
	S10_VCCH_GXP	12	Analog power for P-Tile
EN63A0 (U186) 1.8V	S10_VCCCLK_GXP	12	Clock power for P-Tile
EN63A0 (U184) 1.1V	S10_VCCH_GXE	8	Analog power for E-Tile
	S10_VCCCLK_GXE	1.5	Clock power for E-Tile
EP53F8QI (U78) 2.5V	2.5V	1.5	2.5V for others on board
EP53F8QI (U76) 2.4V	S10_VCCFUSEWR_SDM	0.5	Fuse power for SDM
EN6382QII (U188) 1.8V	S10_VCCIO	6	Power for IO banks of Intel Strat 10
E7620201 (1116) 1 2V	M10_VCC_1.2V	1	Core power for Intel MAX 10
EZ6303QI (U116) 1.2V	M10_VCCDPLL	1	PLL power for Intel MAX 10
EZ6303QI (U116) 2.5V	M10_VCCA/VCC_ADC	0.2	Power for Intel MAX 10 ADC circuits
FP53F8QI (U79) 1.8V	M10_VCCIO	1	Power for 1.8V IOs of Intel MAX 10
EM2130H(U101) 3.3V	3.3V_REG_INST	30	System 3.3V rail
EV1320QI (U164) 0.6V	0p6V_DDR4_VTT_CH00	0.02	Termination power for on-board DDR4
EP53F8QI (U163) 2.5V	2V5_DDR4_CH00	0.1	2.5V rail for DDR4
EN63A0 (U159) 1.2V	S10_1v2OUT_CH00	12	Memory IO power for Ch00
EV1320QI (U166) 0.6V	0p6V_DDR4_VTT_CH11	0.02	Termination power for on-board DDR4
EP53F8QI (U165) 2.5V	2V5_DDR4_CH11	0.1	2.5V rail for DDR4





Source Name	Power Name	Maximum Output Current (A)	Description
EN63A0 (U157) 1.2V	S10_1v2OUT_CH11	12	Memory IO power for Ch00
MAX16550 (U217) 12V	12V_AUX2_IN	20	12V rail from AUX Power connector
MAX16550 (U96) 12V	12V_PCIe_SLOT	5.5	12V rail from PCIe Edge Connector

A.2.1.2. Power Sequence

The Intel Stratix 10 DX FPGA device requires proper power up and power down sequences.

Table 10.	Power	Sequencing	Groups
		ocqueneng	Gioapo

Group 1	Group 2	Group 3			
V _{CCL} /V _{CC} (0.89) V _{CCERAM} (0.9) V _{CCPLLDIG_SDM} (0.9) V _{CCRT_GXP} (0.9) V _{CCRT_GXE} (0.9) V _{CCRTPLL_GXE} (0.9) V _{CCFUSE_GXP} (0.9)	V _{CCH_GXE} (1.1) V _{CCH_GXP} (1.8) V _{CCADC} (1.8) V _{CCPLL_SDM} (1.8) V _{CCAPLL} (1.8) V _{CCIO} (2.5) V _{CCIO} (1.8)	V _{CCIO} (1.2, 1.25, 1.35, 1.5, 1.8) V _{CCFUSEWR_SDM} (2.4) V _{CCN_SDM} (1.8) V _{CCIO3} (1.5, 1.8, 2.5, 3.0)			

- Required power up sequence: **Group 1** > **Group 2** > **Group 3**
- Required power down sequence: **Group 3** > **Group 2** > **Group 1**
- I/O pins are tri-stated during power-up or down sequence when the proper power sequence is followed. I/O pins should not be driven externally during this time or excess I/O pin current can result.
- Power supplies in each group can be ramped up in any order.
- The total power supply ramp-down time must not exceed 100 ms.
- Ramp-up the last power supply of Group 1 to 90% (0.72) before ramping up the Group 2 supplies. Ramp up the last power supply of Group 2 to 90% (1.62V) before ramping up the Group 3 supplies.
- V_{CCBAT SDM} can be powered up anytime.
- To use CvP/autonomous hard IP, the total time must be within 10 ms, from the first power supply ramp-up to the last power supply ramp-up.

Note: The POR delay time in Intel Stratix 10 DX FPGA is always within 2ms.

- V_{CCL} and V_{CC} should be tied together at customer board.
- V_{CCPLL HPS} and V_{CCPLL SDM} should be tied together at customer board.
- V_{CCPLLDIG SDM} and V_{CCERAM} should be tied together at customer board with a filter.
- V_{CCADC} and V_{CCA} should be tied together at customer board with or without a filter.
- V_{CCERT}, V_{CCERT_PLL} and V_{CCERAM} should be tied together at customer board with or without a filter and should ramp up together for better current control.
 - Noise mask specifications must be met.
 - Use of an LC Filter is proposed to enable sourcing $V_{CCERT},\,V_{CCERT_PLL}$ from $V_{CCERAM}.$



- V_{CCN_SDM} has to stay in Group 3. It cannot be moved to Group 2 or merged with any Group 2 regulator.
- V_{CCFUSE_GXP} is always connected to V_{CCERAM} on customer board. For only internal testing purposes, V_{CCFUSE_GXP} is connected to V_{CCR}.
- All power rails must ramp up monotonically.
- All power rails must ramp up to full rail in Tramp specified in the Intel Stratix 10 Device Datasheet.
- Ensure (V_{CCIO} V_{CCPT}) is less than 1.92 to avoid damage to the device
- Hot socket is not supported in Intel Stratix 10 DX FPGA.

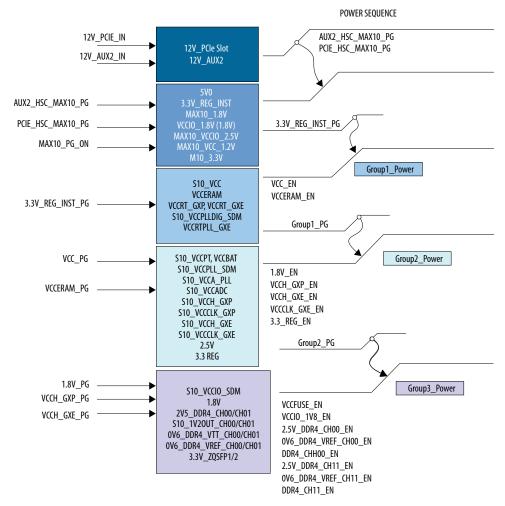


Figure 35. Power Sequence Flow Diagram

A.2.1.3. Power Measurement

Power measurements are provided for six FPGA power rails by using an ADC and sense resistors. The sense resistors are connected in series to the power regulator output. The I²C interface of the ADC or the regulators are used to sense the voltages. The I²C are connected to the Intel MAX 10 device for reading the voltage. The current

Intel[®] Stratix[®] 10 DX FPGA Development Kit User Guide



(A) reading is achieved by a PAC1931 (U233) reading the voltage drop across the sense resistor and software converts the voltage readings to current for each measured rail. The following power rails are monitored:

- VCC, VCCP (Power sensing by I²C on ED8401
- 0.9V (Power sensing by I2C on EN2260, U230)
- 1.8V (Power sensing by I2C on EN2310, U113)
- 3.3V (Power sensing by I2C on EN2310, U101)
- VCCRT_GXE (Sense resistor R6685, monitoring via PAC1931, U233)
- VCCRT_GXP (Sense resistor R6688, monitoring via PAC1931, U233)
- 12V PCIe slot (Power sensing by I2C on MAX16550, U217)
- 12V AUX2 (Power sensing by I2C on MAX16550, U96)

A.2.2. Thermal Requirements

The thermal solution is an active cooling system designed to cool up to 250W total power of the board. The heatsink is designed to meet the height constraints of a 2-slot PCIe card form-factor as defined by the PCIe CEM specification revision 3.0.

The heatsink is securely mounted to the board using screws for easy assembly and removal. The thermal material used between FPGA and heatsink also ensures good thermal contact.

Figure 36. Air-cooled Heatsink Setup



A.2.2.1. Operating Conditions

The Intel Stratix 10 DX FPGA Development Kit is designed to operate within the following conditions while keeping the FPGA die temperature within its recommended operating T_i as defined in the Intel Stratix 10 DX FPGA data sheet (usually 100°C):

- Maximum power dissipation 250 W
- Maximum ambient temperature 0°C 35°C
- FPGA Junction Temperature 85°C

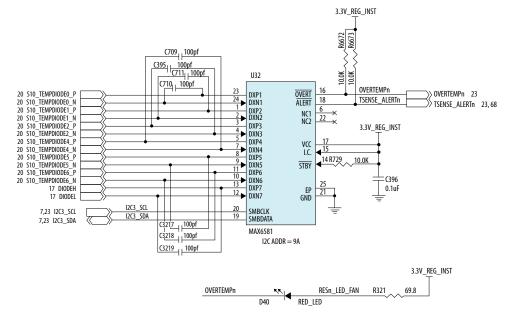


A.2.2.2. Temperature Monitoring

A temperature sensing device (MAX6581) monitors the temperature of the Intel Stratix 10 DX FPGA device. The Intel Stratix 10 DX FPGA device has seven die temperature diodes. The MAX6581 device senses these diodes and convert the signals to a digital form for the Intel MAX 10 device that can be read via a I^2C bus.

Additionally, the OVERTEMPn and ALERTn signals from the MAX6581 allow Intel MAX 10 device to immediately sense a temperature fault condition. The Intel MAX 10 device controls the over temperature warning LED (D40, red-colored) to indicate an over temperature fault condition. Temperature fault set points can be programmed into the MAX6581 device.

Figure 37. MAX6581 Temperature Sensor Circuit

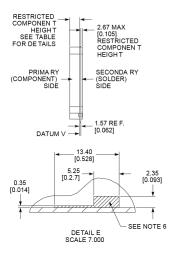


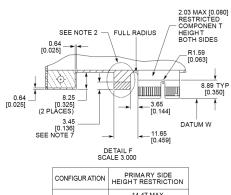
A.2.3. Mechanical Requirements

The Intel Stratix 10 DX FPGA Development Kit has a PCIe standard-height (4.376 in tall), 10.8" long, dual-slot (1.37 in high above the top surface of the PCB) form factor as defined by the PCIe CEM specification Revision 3.0. Additionally, this development kit includes the feature for retaining a high-mass card in the PCIe slot.



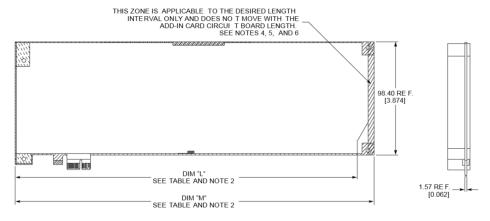
Figure 38. Sectional Profile





	HEIGHT RESTRICTION
SINGLE SLO T	14.47 MAX [0.570]
DUAL SLOT	34.80 MAX [1.370]
TRIPLE SLO T	55.12 MAX [2.170]

Figure 39. Top and Side Profile



LENGTH INTE RVAL	DIM "L"	DIM "M"
HALF LENGTH	162.57 [6.400]	167.65 MAX [6.600]
THREE-QUA RTER LENGTH	248.92 [9.800]	254.00 MAX [10.00]
FULL LENGTH	306.92 [12.083]	312.00 MAX [12.283]



A.3. Clock Circuits

All clocks are supplied by two on-board low-jitter programmable clock generator circuits. The following figure depicts the clock connection to the Intel Stratix 10 DX FPGA:

Figure 40. Clock Connection

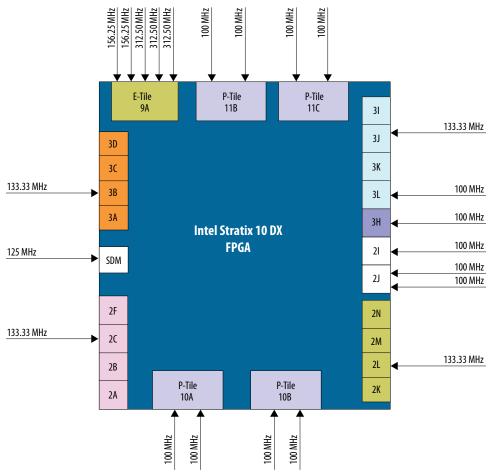


Table 11.On-board Oscillators

Signal Name	Frequency (MHz)	I/O Standard	Application							
Source: U7 (Si5332A)										
CLK_100M_FPGA_3H_P	100	LVDS	FPGA Fabric Clock							
CLK_100M_FPGA_3H_N	- 100	LVDS	Bank 3H							
CLK_125M_LVC1_CONFIG	125	LVCMOS	FPGA Config Clock							
CLK_133M_DDR4_0_P	- 133.33	LVDS	FPGA Fabric Clock							
CLK_133M_DDR4_0_N		LVDS	Bank 3J							
		•	continued							

A. Development Kit Components 683561 | 2020.11.16

intel.

Signal Name	Frequency (MHz)	I/O Standard	Application
CLK_133M_DDR4_1_P	122.22	LVDS	FPGA Fabric Clock
CLK_133M_DDR4_1_N	- 133.33	LVDS	Bank 2L
CLK_133M_DIMM_1_P	122.22	LVDS	FPGA Fabric Clock
CLK_133M_DIMM_1_N	- 133.33	LVDS	Bank 3B
CLK_133M_DIMM_0_P	122.22	LVDS	FPGA Fabric Clock
CLK_133M_DIMM_0_N	- 133.33	LVDS	Bank 2C
CLK_100M_FPGA_3L_0_P	100	LVDS	FPGA Fabric Clock
CLK_100M_FPGA_3L_0_N	- 100	LVDS	Bank 3L
CLK_100M_TEST_P		HCSL	
CLK_100M_TEST_N	- 100	HCSL	Clock for bench test
	Source	e: U9 (Si5391A)	-
CLk_156M.25M_QSFP1_P	456.05	LVPECL	
CLk_156M.25M_QSFP1_N	- 156.25	LVPECL	Reference Clock for Transceivers 9A
CLk_156M.25M_QSFP0_P	456.25	LVPECL	
CLk_156.25M_QSFP0_N	- 156.25	LVPECL	Reference Clock for Transceivers 9A
CLk_312M.50M_QSFP0_P	242.50	LVPECL	
CLk_312M.50M_QSFP0_N	- 312.50	LVPECL	Reference Clock for Transceivers 9A
CLk_312M.50M_QSFP1_P		LVPECL	
CLk_312M.50M_QSFP1_N	- 312.50	LVPECL	Reference Clock for Transceivers 9A
CLk_312M.50M_QSFP2_P		LVPECL	
CLk_312M.50M_QSFP2_N	- 312.50	LVPECL	Reference Clock for Transceivers 9A
CLK_100M_FPGA_21_P		LVDS	FPGA Fabric Clock
CLK_100M_FPGA_21_N	- 100	LVDS	Bank 2I
CLK_100M_FPGA_2J_1_P		LVDS	FPGA Fabric Clock
CLK_100M_FPGA_2J_1_N	- 100	LVDS	Bank 2J
CLK_100M_FPGA_2J_0_P		LVDS	FPGA Fabric Clock
CLK_100M_FPGA_2J_0_N	- 100	LVDS	Bank 2J
CLK_100M_Si5391_P		LVDS	Clock to U7
CLK_100M_Si5391_N	- 100	LVDS	Input 2

The default clock frequencies are as listed in the table. All the clock frequencies can be changed by using the Clock GUI.

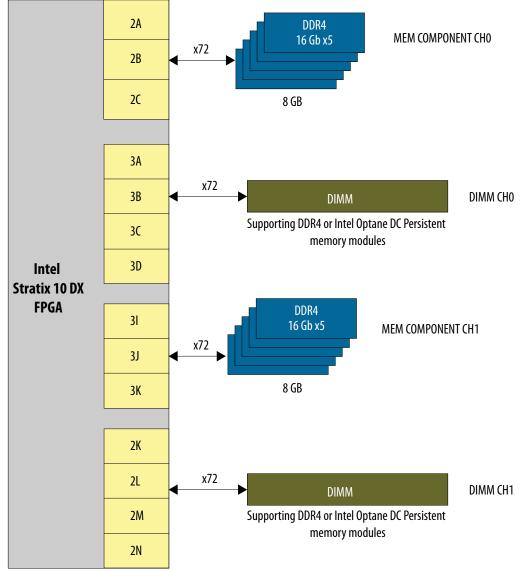


A.4. Memory Interface

The Intel Stratix 10 DX FPGA device supports four independent memory interfaces:

- Two independent on-board DDR4
- Two DIMM sockets for DDR4 or Intel Optane DC Persistent memory modules

Figure 41. Memory Interface



The on-board DDR4 uses five 16Gb DDR4 single rank devices connecting to bank 2K, 2L, 2M for memory component channel 1 and bank 3I, 3J, 3K for memory component channel 0. The total memory size of each channel is 8 GB running at 1200 MHz.





The 288-pin DIMM socket interfaces to bank 3I, 3J, 3K, 3L for DIMM channel 0 and to bank 2K, 2L, 2M, 2N for DIMM channel 1. This socket accepts DDR4 or Intel Optane DC Persistent memory module (requires Intel memory controller IP core). It supports dual rank at frequency 1067 MHz, 16 GB per channel. It also supports single rank at frequency 1200 MHz, 8 GB per channel.

A.5. PCIe Interface

The Intel Stratix 10 DX FPGA Development Kit supports four PCIe Gen4 x16 interfaces using the four P-Tile of the Intel Stratix 10 DX FPGA device.

- One P-Tile (10A) supports PCIe x16 connecting to the devkit's PCIe edge connector. This interface supports PCIe x1, x4, x8, and x16 PCIe End point.
- Three P-Tile (11B, 11C, 10B) each connecting to their corresponding SlimSAS connector can be used as UPI (x20) or PCIe x16 interface in Endpoint or Root Port mode.

The PCIe Edge Connector has PCIe Wake signal (pin B11) and PCIe Clock request (pin B12) routed to the GPIO of the Intel Stratix 10 FPGA device.

A.6. UPI Interface

The Intel Stratix 10 DX FPGA Development Kit supports three individual UPI interfaces. The UPI functionality is enabled by a combination of the appropriate P-Tile settings and UPI protocol IP core available in Intel Quartus Prime Pro Edition software (additional licensing and enablement may apply). Each interface consists of two SlimSAS connectors, one for transmit signals and one for receive signals. Each UPI interface provides node ID for the host CPU to identify. Node ID can be set by strapping resistors on the board.

The Slim SAS connectors also carry SMBus/I2C, clock, GPIO, and PCIe signals.



A.7. Transceiver Signals: PCIe and UPI Interface

Figure 42. PCIe X16 End point - PCIe Slot Interface

				1
55 PCIE_EP_TX0_N 55 PCIE_EP_TX0_P	BJ51 BJ52	GXPL10A_RX_CHON GXPL10A_RX_CHOP	GXPL10A_TX_CHON GXPL10A_TX_CHOP	BJ47 BJ48 PCIE_EP_RX0_N 55 PCIE_EP_RX0_P 55
55 PCIE_EP_TX1_N	BH53 BH54	GXPL10A_RX_CH1N GXPL10A_RX_CH1P	GXPL10A_TX_CH1N GXPL10A_TX_CH1P	BH49 BH50 PCIE_EP_RX1_N 55 PCIE_EP_RX1_P 55
55 PCIE_EP_TX2_N	BG51 BG52	GXPL10A_RX_CH2N GXPL10A_RX_CH2P	GXPL10A_TX_CH2N GXPL10A_TX_CH2P	BG47 PCIE_EP_RX2_N 55 BG48 PCIE_EP_RX2_P 55
55 PCIE_EP_TX3_N	BF53 BF54	GXPL10A_RX_CH3N GXPL10A_RX_CH3P	GXPL10A_TX_CH3N GXPL10A_TX_CH3P	BF49 BF50 PCIE_EP_RX3_N 55 PCIE_EP_RX3_P 55
55 PCIE_EP_TX4_N	BE51 BE52	GXPL10A_RX_CH4N GXPL10A_RX_CH4P	GXER9A_TX_CH4N GXER9A_TX_CH4P	BE47 PCIE_EP_RX4_N 55 BE48 PCIE_EP_RX4_P 55
55 PCIE_EP_TX5_N	BD53 BD54	GXPL10A_RX_CH5N GXPL10A_RX_CH5P	GXER9A_TX_CH5N GXER9A_TX_CH5P	BD49 BD50 PCIE_EP_RX5_N 55 PCIE_EP_RX5_P 55
55 PCIE_EP_TX6_N	BC51 BC52	GXPL10A_RX_CH6N GXPL10A_RX_CH6P	GXER9A_TX_CH6N GXER9A_TX_CH6P	BC47 PCIE_EP_RX6_N 55 BC48 PCIE_EP_RX6_P 55
55 PCIE_EP_TX7_N	BB53 BB54	GXPL10A_RX_CH7N GXPL10A_RX_CH7P	GXER9A_TX_CH7N GXER9A_TX_CH7P	BB49 PCIE_EP_RX7_N 55 BB50 PCIE_EP_RX7_P 55
55 PCIE_EP_TX8_N	BA51 BA52	GXPL10A_RX_CH8N GXPL10A_RX_CH8P	GXPL10A_TX_CH8N GXPL10A_TX_CH8P	BA47 BA48 PCIE_EP_RX8_N 55 PCIE_EP_RX8_P 55
55 PCIE_EP_TX9_N	AY53 AY54	GXPL10A_RX_CH9N GXPL10A_RX_CH9P	GXPL10A_TX_CH9N GXPL10A_TX_CH9P	AY49 AY50 PCIE_EP_RX9_N 55 PCIE_EP_RX9_P 55
55 PCIE_EP_TX10_N 55 PCIE_EP_TX10_P	AW51 AW52	GXPL10A_RX_CH10N GXPL10A_RX_CH10P	GXPL10A_TX_CH10N GXPL10A_TX_CH10P	AW47 PCIE_EP_RX10_N 55
55 PCIE_EP_TX11_N	AV53 AV54	GXPL10A_RX_CH11N GXPL10A_RX_CH11P	GXPL10A_TX_CH11N GXPL10A_TX_CH11P	AV49 PCIE_EP_RX11_N 55 AV50 PCIE_EP_RX11_P 55
55 PCIE_EP_TX12_N	AU51 AU52	GXPL10A_RX_CH12N GXPL10A_RX_CH12P	GXER9A_TX_CH12N GXER9A_TX_CH12P	AU47 PCIE_EP_RX12_N 55 AU48 PCIE_EP_RX12_P 55
55 PCIE_EP_TX13_N	AT53 AT54	GXPL10A_RX_CH13N GXPL10A_RX_CH13P	GXER9A_TX_CH13N GXER9A_TX_CH13P	AT49 AT50 PCIE_EP_RX13_N 55 PCIE_EP_RX13_P 55
55 PCIE_EP_TX14_N	AR51 AR52	GXPL10A_RX_CH14N GXPL10A_RX_CH14P	GXER9A_TX_CH14N GXER9A_TX_CH14P	AR47 PCIE_EP_RX14_N 55
55 PCIE_EP_TX15_N	AP53 AP54	GXPL10A_RX_CH15N GXPL10A_RX_CH15P	GXER9A_TX_CH15N GXER9A_TX_CH15P	AP49 AP50 PCIE_EP_RX15_N 55 PCIE_EP_RX15_P 55
PCIE_EP_I0_RE8REF	AN41	U10_P_I0_RE8REF_0		
PCIE_EP_85332_REFCLK0_N PCIE_EP_85332_REFCLK0_P	AT44 AT45	REFCLK_GXPL10A_CHO REFCLK_GXPL10A_CHO		
PCIE_EP_85332_REFCLK1_N PCIE_EP_85332_REFCLK1_P	AP44 AP45	REFCLK_GXPL10A_CH2 REFCLK_GXPL10A_CH2		
		XCVR BA	NK 10A	

Figure 43. UPI 0 Link or PCIe Interface

39 PECL UP12, FFGA, BR0, P AM31 OPR1 10B, BX, CHNP										
29 PRED_UP12_FGA_RED_N A455 GPL 108 RX (HIN GPL 108 TX (HIN A449 PRED_UP12_FGA_RD_N PRED_UP12_FGA_RD_N </td <td></td> <td>PCIE2_UP12_FPGA_RX0_N PCIE2_UP12_FPGA_RX0_P</td> <td>AN51 AN52</td> <td>GXPL 10B_RX_CHON GXPL 10B_RX_CHOP</td> <td></td> <td>AN47 AN48</td> <td>\square</td> <td></td> <td></td> <td></td>		PCIE2_UP12_FPGA_RX0_N PCIE2_UP12_FPGA_RX0_P	AN51 AN52	GXPL 10B_RX_CHON GXPL 10B_RX_CHOP		AN47 AN48	\square			
9 P(EE_UPT1_FPGA_R02_N A151 COP. 108_RX (CHN) CAP. 108_RX (CHN) CAP. 108_RX (CHN) P(EE_UPT1_FPGA_R03_N) 9 9 P(EE_UPT1_FPGA_R03_N) A453 CAP. 108_RX (CHN) CAP. 108_RX (CHN) A469 P(EE_UPT1_FPGA_R03_N) 9 9 P(EE_UPT1_FPGA_R03_N) A453 CAP. 108_RX (CHN) CAP. 108_RX (CHN) A459 P(EE_UPT1_FPGA_R03_N) 9 9 P(EE_UPT1_FPGA_R03_N) A453 CAP. 108_RX (CHN) CAP. 108_RX (CHN) A449 P(EE_UPT1_FPGA_R03_N) 9 9 P(EE_UPT1_FPGA_R03_N) A453 CAP. 108_RX (CHN) A447 P(EE_UPT1_FPGA_R03_N) 9 P(EE_UPT1_FPGA_R03_N)		PCIE2_UP12_FPGA_RX1_N	AM53 AM54	GXPL 10B_RX_CH1N GXPL 10B_RX_CH1P				PCIE2_UP12_FPGA_TX1	_N 2	29
29 P(DL2_UP12_FP6A_RN3_N AM35 GCPL 108_R. CH3N GCPL 108_R. CH3N AM39 P(DL2_UP12_FP6A_RN3_N P(DL2_			AL51 ⊾		GXPL 10B_TX_CH2N			PCIE2_UP12_FPGA_TX2	N 2	29
29 P(12_UP12_PF6A_R84_N A151 COP1 108_RX (H4H) A477 P(12_UP12_PF6A_R18_N) P	29	PCIE2_UP12_FPGA_RX3_N	AK53	GXPL 10B_RX_CH3N	GXPL 10B_TX_CH3N			PCIE2_UP12_FPGA_TX	3_N 2	29
29 P(12, UP12, PFGA, R85, N AH33 CKP1 108, RX, CHN GKP1 108, RX, CHN	29		AJ51	GYPLIOR BY CHAN	GXPL 10B_TX_CH4N			PCIE2_UP12_FPGA_TX4	1_N 2	29
29 PICL2_UP12_FFGA_RXS_N PICL2_UP12_FFGA_RXS_N <td< th=""><th>29</th><th>PCIE2_UP12_FPGA_RX5_N</th><th>AH53</th><th>GXPL 10B_RX_CH5N</th><th>GXPL 10B_TX_CH5N</th><th>AH49</th><th></th><th>PCIE2_UP12_FPGA_TX5</th><th>5_N 2</th><th>29</th></td<>	29	PCIE2_UP12_FPGA_RX5_N	AH53	GXPL 10B_RX_CH5N	GXPL 10B_TX_CH5N	AH49		PCIE2_UP12_FPGA_TX5	5_N 2	29
29 PRIZ_UP12_FF04, RX7_N PRIZ_UP12_FF04, RX7_N PRIZE_UP12_FF04, RX7_N<	29	PCIE2_UP12_FPGA_RX6_N	AG51	GXPL 10B_RX_CH6N	GXPL 10B_TX_CH6N	AG47		PCIE2_UP12_FPGA_TX6	5_N 2	29
29 PRIZ_UP12_PF04_RX8_N CMPL 108_RX_CH/P CARL 108_TX_CH8P PRIZ PRIZ_UP12_PF04_TX8_N PRIZ 29 PRIZ_UP12_PF04_RX8_N A451 CMPL 108_RX_CH8P CMPL 108_RX_CH8P A443 PRIZ_UP12_PF04_TX8_N PP01Z_UP12_PF04_TX8_N PP01Z_UP12_FF04_TX8_N P01Z_UP12_FF04_TX8_N PP01Z_UP12_FF04_TX	29	PCIE2_UP12_FPGA_RX7_N	AF53	GXPL 10B_RX_CH7N		AF49				
29 P(L2_UP12_FPGA_R83_P) AD33 CMP1 108_RX_CH89 CMP1 108_RX_CH199 CMP1		PCIEZ_UP1Z_FPGA_KX/_P	-	GXPL TOB_RX_CH/P			»	PCIE2_UP12_FPGA_TX7	/_P 2	:9
29 PCIE2_UP12_EP6A_RX9_N AD53 PCIE2_UP12_EP6A_RX10_N AD53 PCIE2_UP12_EP6A_RX10_N PCIE2_UP12_EP6A_RX10_N PCIE2_UP12_E		PCIEZ_UP1Z_FPGA_KX8_P		GXPL 10B_RX_CH8P						
29 PCIE2_UP12_EFGA_RX10_N AC31 AC32 GXPL 108_RX_CH10N_GXPL 108_TX_CH10N_AC417 AC47 AC48 PCIE2_UP12_EFGA_TX10_P 29 29 PCIE2_UP12_EFGA_RX11_N A633 AB53 GXPL 108_RX_CH10N_GXPL 108_TX_CH10N_AE48 AE47 AC48 PCIE2_UP12_EFGA_TX11_P 29 29 PCIE2_UP12_FFGA_RX11_N AB53 GXPL 108_RX_CH10N_GXPL 108_TX_CH10N_AE48 AE49 PCIE2_UP12_FFGA_TX11_P PCIE2_UP12_FFGA_TX11_N 29 29 PCIE2_UP12_FFGA_RX12_N AA51 GXPL 108_RX_CH12N_GXPL 108_TX_CH12N_A448 PCIE2_UP12_FFGA_TX11_P 29 29 PCIE2_UP12_FFGA_RX13_N GXPL 108_RX_CH12N_GXPL 108_TX_CH12N_A448 PCIE2_UP12_FFGA_TX11_P 29 29 PCIE2_UP12_FFGA_RX13_N GXPL 108_RX_CH12N_GXPL 108_TX_CH12N_A448 PCIE2_UP12_FFGA_TX11_P 29 29 PCIE2_UP12_FFGA_RX13_N GXPL 108_RX_CH13N_GXPL 108_TX_CH13N_GXPL 108_TX_CH13N_Y 29 PCIE2_UP12_FFGA_RX14_N 29 29 PCIE2_UP12_FFGA_RX15_N UP12_FFGA_RX15_N_GXPL 108_RX_CH14N_GXPL 108_TX_CH13N_Y 29 PCIE2_UP12_FFGA_RX15_N_Z 29 20 PCIE2_UP12_FFGA_RX15_N_Z UP12_FFGA_RX15_N_Z UP12_FFGA_RX15_N_Z 29 PCIE2_UP12_FFGA_RX15_N_Z 29 210 PCIE2_UP12_FFGA_RX15_N_Z UP1		PCIE2_UP12_FPGA_RX9_N	AD53	GXPL 10B_RX_CH9N				PCIE2_UP12_FPGA_TX9)_N 2	
29 PCIE2_UP12_FPGA_RX11_N AB534 AB544 GXPL 108_RX_CH11N_GXPL 108_TX_CH12N GXPL 108_RX_CH11P_GXPL 108_TX_CH12N GXPL 108_RX_CH12P_GXL 108_TX_CH12N GXPL 108_RX_CH12P_GXL 108_TX_CH12N GXPL 108_RX_CH12P_GXL 108_TX_CH12N GXPL 108_RX_CH12N_GXPL 108_	29	PCIE2_UP12_FPGA_RX10_N	AC51	GXPL 10B_RX_CH10N	GXPL 10B_TX_CH10N			PCIE2_UP12_FPGA_TX1	N	29
29 PCIE_UP12_FPGA_RX11_P			AB53 ⊾	CVDI 10R DV CH11N	CVDI 10R TV CH11N	AB49				
22 PCIE2_UP12_IP6A_RX13_P AA32 GXPL 108_RX_CH12P_GXPL 108_RX_CH12P_GXPL 108_RX_CH12P_GXPL 108_RX_CH12P_FXPL 108_RX_C	29	PCIE2_UP12_FPGA_RXT1_P	AAC1	GXPL 10B_RX_CH11P	GXPL 10B_IX_CH11P					
29 PCIE2_UP12_IP6A_RX14_N VI <			AA52	GXPL 10B_RX_CH12P	GXPL 10B_TX_CH12P		$ \blacksquare $			
29 PCIE2_UP12_EP6A_RX14_P W12 GXPL 108_RX_CH14N_GXPL 108_TX_CH14P W47 PCIE2_UP12_EP6A_RX14_P 29 29 PCIE2_UP12_EP6A_RX15_N W12 GXPL 108_RX_CH14P GXPL 108_RX_CH14P W47 PCIE2_UP12_EP6A_RX14_P 29 29 PCIE2_UP12_EP6A_RX15_N W13 GXPL 108_RX_CH14P GXPL 108_RX_CH14P W48 PCIE2_UP12_EP6A_RX15_N 29 29 PCIE2_UP12_EP6A_RX15_N W13 GXPL 108_RX_CH15P GXPL 108_RX_CH15P GXPL 108_RX_CH15P GXPL 108_RX_CH15P GXPL 108_RX_CH15P GXPL 108_RX_CH16P			Y53 Y54	GXPL 10B_RX_CH13N GXPL 10B_RX_CH13P	GXPL 10B_TX_CH13N GXPL 10B_TX_CH13P		\square			
29 PCIE2_UP12_FPGA_RX15_P 29 PCIE2_UP12_FPGA_RX15_P 29 PCIE2_UP12_FPGA_RX15_P 29 PCIE2_UP12_FPGA_RX15_P 29 PCIE2_UP12_FPGA_RX16_P 20 PCIE2_UP12_FPGA_RX16_P 20 PCIE2_UP12_FPGA_RX16_P 29 PCIE2_UP12_FPGA_RX16_P 29 PCIE2_UP12_FPGA_RX17_P 29 PCIE2_UP12_FPGA_RX17_P 29 PCIE2_UP12_FPGA_RX18_P 29 PCIE2_UP12_FPGA_RX18_P 20 PCIE2_UP12_FPGA_RX18_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 20 PCIE2_UP12_FPGA_RX19_P 21 PCIE2_UP12_REFCLKO_P 22 PCIE2_UP12_REFCLKO_P 23 PCIE2_UP12_REFCLKO_P 24 PCIE2_UP12_REFCLKO_P 24 PCIE2_UP12_REFCLKO_P 25 PCIE2_UP12_REFCLKO_P 25 PCIE2_UP12_REFCLKO_P 27 PCIE2_UP12_REFCLKO_P			W51	GXPL 10B_RX_CH14N	GXPL 10B_TX_CH14N					
29 PCIE2_UP12_FPGA_RX16_P US1 GXPL 108_RX_CH16N_CXPL 108_TX_CH16N_U47 U47 PCIE2_UP12_FPGA_RX16_P 29 29 PCIE2_UP12_FPGA_RX16_P US2 GXPL 108_RX_CH16P_GXPL 108_TX_CH16N_U48 PCIE2_UP12_FPGA_RX16_P PCIE2_UP12_FPGA_RX16_P PCIE2_UP12_FPGA_RX17_N_I72_P 29 29 PCIE2_UP12_FPGA_RX17_P T53 GXPL 108_RX_CH17P_GXPL 108_TX_CH17P_GXPL 108_TX_CH17P_I74 PCIE2_UP12_FPGA_RX17_P 29 29 PCIE2_UP12_FPGA_RX18_N R51 R51 GXPL 108_RX_CH17P_GXPL 108_TX_CH17P_I74 P29 29 PCIE2_UP12_FPGA_RX18_P R51 GXPL 108_RX_CH18N_GXPL 108_TX_CH17P_I74 P29 29 PCIE2_UP12_FPGA_RX18_P R52 GXPL 108_RX_CH18P_GXPL 108_TX_CH18P_GXPL 108_TX_CH17P_I74 P29 29 PCIE2_UP12_FPGA_RX18_P PS3 GXPL 108_RX_CH19P_GXPL 108_TX_CH19P_GXPL 108_TX_CH19P_I74 P49 PCIE2_UP12_FPGA_TX18_P_29 29 PCIE2_UP12_RFGA_RX19_P P53 GXPL 108_RX_CH19P_GXPL 108_TX_CH19P_GXPL 108_TX_CH19P_I74 P49 PCIE2_UP12_FPGA_TX19_P_29 29 PCIE2_UP12_RFGA_RX19_P PCIE2_UP12_RFGA_RX19_P P29 PCIE2_UP12_RFGA_TX19_P_29 P29 20 PCIE2_UP12_RFGA_RX19_P P34 GXPL 108_RX_CH19P_G	29	PCIE2_UP12_FPGA_RX15_N	V53	GXPL 10B RX CH15N	GXPL 10B TX CH15N			PCIE2_UP12_FPGA_TX1	15_N	29
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	29	PCIE2_UP12_FPGA_RX16_N	051					PCIE2_UP12_FPGA_TX1	16_N	29
29 PCIE2_UP12_PF6A_RX18_P R51 GXPL 108_RX_CH19P GXPL 108_RX_CH18N GXPL 108_RX_CH19N			-							
29 PCIE2_UP12_FPGA_RX18_N R51 GXPL 10B_RX_CH18N GXPL 10B_RX_CH18N GXPL 10B_RX_CH18N R47 PCIE2_UP12_FPGA_RX18_N 29 29 PCIE2_UP12_FPGA_RX18_P R52 GXPL 10B_RX_CH18P GXPL 10B_RX_CH18P GXPL 10B_RX_CH18P R47 PCIE2_UP12_FPGA_RX18_N 29 29 PCIE2_UP12_FPGA_RX19_P P53 GXPL 10B_RX_CH19P GXPL 10B_RX_CH19P GXPL 10B_RX_CH19P PGIE2_UP12_FPGA_RX19_N 29 29 PCIE2_UP12_FPGA_RX19_P P54 GXPL 10B_RX_CH19P GXPL 10B_RX_CH19P GXPL 10B_RX_CH19P PGIE2_UP12_FPGA_RX19_P 29 20 PCIE2_UP12_FPGA_RX19_P PGIE2_UP12_IO_REBREF AC41 AC41 PGIE2_UP12_REFCLK0_N PGIE2_UP12_FPGA_RX19_P 29 21 PCIE2_UP12_REFCLK0_N PGIE2_UP12_REFCLK_GXPL 10B_CH0P REFCLK_GXPL 10B_CH0P REFCLK_GXPL 10B_CH0P PGIE2_UP12_REFCLK2_N PGIE2_UP12_REFCLK_GXPL 10B_CH2P 17 PCIE2_UP12_REFCLK2_N RE1CLK_GXPL 10B_CH2P REFCLK_GXPL 10B_CH2P REFCLK_GXPL 10B_CH2P REFCLK_GXPL 10B_CH2P 17 PCIE2_UP12_REFCLK2_N PGIE3_UP17_DNI PGIE3_UP17_DNI PGIE3_UP17_DNI PGIE3_UP17_DNI PGIE3_UP17_DNI				GXPL TOB_RX_CHT/P	GXPL 10B_1X_CH1/P					
29 PCIE2_UP12_FPGA_RX19_N P33 P54 GXPL 108_RX_CH19N_GXPL 108_TX_CH19N_ GXPL 108_RX_CH19P P49 PCIE2_UP12_FPGA_TX19_N 29 29 PCIE2_UP12_FPGA_RX19_P P54 GXPL 108_RX_CH19P GXPL 108_RX_CH19P PCIE2_UP12_FPGA_TX19_P 29 PCIE2_UP12_REFCLK0_N PCIE2_UP12_O_REBREF_AC411 U11_P_IO_REBREF_0 REFCLK_GXPL 108_CH0N REFCLK_GXPL 108_CH2N REFCLK_GXPL 108_CH2N REFCLK_GXPL 108_CH2N REFCLK_GXPL 108_CH2N U11_P_IO_REBREF_0 REFCLK_GXPL 108_CH2N REFCLK_GXPL 108_CH2N REFCLK_GXPL 108_CH2N PCIE2_UP12_REFCLK2_N REFCLK_GXPL 108_CH2N 17 PCIE2_UP12_REFCLK2_N PCIE2_UP12_CEFCLK2_N REFCLK_GXPL 108_CH2N PCIE2_UP12_REFCLK2_N PCIE2_UP12_REFCLK2_N			R51	GXPL 10B_RX_CH18N	GXPL 10B_TX_CH18N		\square			
PCIE2_UP12_10_RESREF_AC41 PCIE2_UP12_0_RESREF_AC41 17 PCIE2_UP12_REFCLK0_P 17 PCIE2_UP12_REFCLK0_P 17 PCIE2_UP12_REFCLK0_P 17 PCIE2_UP12_REFCLK2_P R216 REFCLK_GXPL 10B_CH0P REFCLK_GXPL 10B_CH0P REFCLK_GXPL 10B_CH2P REFCLK_GXPL 10B_CH2P REFCLK_GXPL 10B_CH2P			P53	GXPL 10B_RX_CH19N						29
17 PCIE2_UP12_REFCLKO_P A444 REFCLK_GXPL 10B_CHON REFCLK_GXPL 10B_CHOP 17 PCIE2_UP12_REFCLK2_P R216 REFCLK_GXPL 10B_CHOP 17 PCIE2_UP12_REFCLK2_P R217 DNI	29	PCIE2_UP12_FPGA_RX19_P		GXPL 10B_RX_CH19P	GXPL 10B_TX_CH19P	U	»	PCIE2_UP12_FPGA_TX1	9_P	29
17 PCIE2_UP12_REFCLKO_P A444 REFCLK_GXPL 10B_CHON REFCLK_GXPL 10B_CHOP 17 PCIE2_UP12_REFCLK2_P R216 REFCLK_GXPL 10B_CHOP 17 PCIE2_UP12_REFCLK2_P R217 DNI		PCIE2 UP12 IO RE8REF	AC41.							
17 PCIE2_UP12_REFCLK0_P Image: Constraint of the second s										
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		17 PCIE2_UP12_REFCLK0_P	AJ45	REFCLK GXPL 10B CH	OP					
		17 PCIE2_UP12_REFCLK2_N	AG45	REFCLK_GXPL 10B_CH REFCLK_GXPL 10B_CH	2N 2P					
XCVR BANK 10B		R217 ČĎNI								
				XCVR	SANK 10B					



Figure 44. UPI 1 Link or PCIe Interface

27 27	PCIEO_UP10_FPGA_RX0_N PCIEO_UP10_FPGA_RX0_P	BB2 BB1	GXPR11B_RX_CHON GXPR11B_RX_CHOP	GXPR11B_TX_CHON GXPR11B_TX_CHOP	BA8 BA7		PCIEO_UP10_FPGA_TXO_N PCIEO_UP10_FPGA_TXO_P	27 27
27 27	PCIEO_UP10_FPGA_RX1_N PCIEO_UP10_FPGA_RX1_P	BA4 BA3	GXPR11B_RX_CH1N GXPR11B_RX_CH1P	GXPR11B_TX_CH1N GXPR11B_TX_CH1P	AY6 AY5		PCIEO_UP10_FPGA_TX1_N PCIEO_UP10_FPGA_TX1_P	
27 27	PCIEO_UP10_FPGA_RX2_N PCIEO_UP10_FPGA_RX2_P	AY2 AY1	GXPR11B_RX_CH2N GXPR11B_RX_CH2P	GXPR11B_TX_CH2N GXPR11B_TX_CH2P	AW8 AW7		PCIEO_UP10_FPGA_TX2_N PCIEO_UP10_FPGA_TX2_P	
27 27	PCIEO_UP10_FPGA_RX3_N PCIEO_UP10_FPGA_RX3_P	AW4 AW3	GXPR11B_RX_CH3N GXPR11B_RX_CH3P	GXPR11B_TX_CH3N GXPR11B_TX_CH3P	AV6 AV5	\geq	PCIEO_UP10_FPGA_TX3_N	
27 27	PCIEO_UP10_FPGA_RX4_N PCIEO_UP10_FPGA_RX4_P	AV2 AV1	GXPR11B_RX_CH4N GXPR11B_RX_CH4P	GXPR11B_TX_CH4N GXPR11B_TX_CH4P	AU8 AU7		PCIEO_UP10_FPGA_TX4_N PCIEO_UP10_FPGA_TX4_P	
27 27	PCIEO_UP10_FPGA_RX5_N PCIEO_UP10_FPGA_RX5_P	AU4 AU3	GXPR11B_RX_CH5N GXPR11B_RX_CH5P	GXPR11B_TX_CH5N GXPR11B_TX_CH5P	AT6 AT5	\gg		27
27 27	PCIEO_UP10_FPGA_RX6_N PCIEO_UP10_FPGA_RX6_P	AT2 AT1	GXPR11B_RX_CH6N GXPR11B_RX_CH6P	GXPR11B_TX_CH6N GXPR11B_TX_CH6P	AR8 AR7			27 27
27 27	PCIEO_UP10_FPGA_RX7_N PCIEO_UP10_FPGA_RX7_P	AR4 AR3	GXPR11B_RX_CH7N GXPR11B_RX_CH7P	GXPR11B_TX_CH7N GXPR11B_TX_CH7P	AP6 AP5		PCIEO_UP10_FPGA_TX7_N PCIEO_UP10_FPGA_TX7_P	
27 27	PCIEO_UP10_FPGA_RX8_N PCIEO_UP10_FPGA_RX8_P	AP2 AP1	GXPR11B_RX_CH8N GXPR11B_RX_CH8P	GXPR11B_TX_CH8N GXPR11B_TX_CH8P	AN8 AN7			27 27
27 27	PCIEO_UP10_FPGA_RX9_N PCIEO_UP10_FPGA_RX9_P	AN4 AN3	GXPR11B_RX_CH9N GXPR11B_RX_CH9P	GXPR11B_TX_CH9N GXPR11B_TX_CH9P	AM6 AM5		PCIEO_UP10_FPGA_TX9_N PCIEO_UP10_FPGA_TX9_P	
27 27	PCIEO_UP10_FPGA_RX10_N PCIEO_UP10_FPGA_RX10_P	AM2 AM1	GXPR11B_RX_CH10N GXPR11B_RX_CH10P	GXPR11B_TX_CH10N GXPR11B_TX_CH10P	AL8 AL7		PCIEO_UP10_FPGA_TX10_N PCIEO_UP10_FPGA_TX10_P	
27 27	PCIE0_UP10_FPGA_RX11_N PCIE0_UP10_FPGA_RX11_P	AL4 AL3	GXPR11B_RX_CH11N GXPR11B_RX_CH11P	GXPR11B_TX_CH11N GXPR11B_TX_CH11P	AK6 AK5		PCIEO_UP10_FPGA_TX11_N PCIEO_UP10_FPGA_TX11_P	27 27
27 27	PCIEO_UP10_FPGA_RX12_N PCIEO_UP10_FPGA_RX12_P	AK2 AK1	GXPR11B_RX_CH12N GXPR11B_RX_CH12P	GXPR11B_TX_CH12N GXPR11B_TX_CH12P	AJ8 AJ7		PCIEO_UP10_FPGA_TX12_N PCIEO_UP10_FPGA_TX12_P	27 27
27 27	PCIEO_UP10_FPGA_RX13_N	AJ4 AJ3	GXPR11B_RX_CH13N GXPR11B_RX_CH13P	GXPR11B_TX_CH13N GXPR11B_TX_CH13P	AH6 AH5		PCIEO_UP10_FPGA_TX13_N PCIEO_UP10_FPGA_TX13_P	
27 27	PCIEO_UP10_FPGA_RX14_N PCIEO_UP10_FPGA_RX14_P	AH2 AH1	GXPR11B_RX_CH14N GXPR11B_RX_CH14P	GXPR11B_TX_CH14N GXPR11B_TX_CH14P	AG8 AG7		PCIEO_UP10_FPGA_TX14_N PCIEO_UP10_FPGA_TX14_P	27 27
27 27	PCIEO_UP10_FPGA_RX15_N	AG4 AG3	GXPR11B_RX_CH15N GXPR11B_RX_CH15P	GXPR11B_TX_CH15N GXPR11B_TX_CH15P	AF6 AF5	\supset	PCIEO_UP10_FPGA_TX15_N PCIEO_UP10_FPGA_TX15_P	27 27
27 27	PCIEO_UP10_FPGA_RX16_N PCIEO_UP10_FPGA_RX16_P	AF2 AF1	GXPR11B_RX_CH16N GXPR11B_RX_CH16P	GXPR11B_TX_CH16N GXPR11B_TX_CH16P	AE8 AE7		PCIEO_UP10_FPGA_TX16_N PCIEO_UP10_FPGA_TX16_P	27 27
27 27	PCIEO_UP10_FPGA_RX17_N PCIEO_UP10_FPGA_RX17_P	AE4 AE3	GXPR11B_RX_CH17N GXPR11B_RX_CH17P	GXPR11B_TX_CH17N GXPR11B_TX_CH17P	AD6 AD5		PCIEO_UP10_FPGA_TX17_N PCIEO_UP10_FPGA_TX17_P	27 27
27 27	PCIEO_UP10_FPGA_RX18_N PCIEO_UP10_FPGA_RX18_P	AD2 AD1	GXPR11B_RX_CH18N GXPR11B_RX_CH18P	GXPR11B_TX_CH18N GXPR11B_TX_CH18P	AC8 AC7		PCIEO_UP10_FPGA_TX18_N PCIEO_UP10_FPGA_TX18_P	27 27
27 27	PCIEO_UP10_FPGA_RX19_N	AC4 AC3	GXPR11B_RX_CH19N GXPR11B_RX_CH19P	GXPR11B_TX_CH19N GXPR11B_TX_CH19P	AB6 AB5		PCIEO_UP10_FPGA_TX19_N PCIEO_UP10_FPGA_TX19_P	27 27
	PCIE0_UP10_I0_RE8REF	AL14	U21_P_IO_RE8REF_0					
1	7 PCIEO_UP10_REFCLKO_N	AH11	REFCLK_GXPR11B_CH0	N				

_

	U21 P IO RE8REF 0
PCIEO_UP10_REFCLKO_N	REFCLK_GXPR11B_CHON
	REFCLK_GXPR11B_CHOP
	REFCLK_GXPR11B_CH2N
PCIEO_UP10_REFCLK2_P	REFCLK_GXPR11B_CH2P
R266 ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	
DNI	XCVR BANK 11B
	ACAK DAINK LID
	PCIEO_UP10_REFCLKO_P



Figure 45. UPI 2 Link or PCIe Interface

28 28	PCIE1_UP11_FPGA_RX0_N PCIE1_UP11_FPGA_RX0_P	AB2 AB1	GXPR11C_RX_CHON GXPR11C_RX_CHOP	GXPR11C_TX_CHON GXPR11C_TX_CHOP	AA8 AA7	> PCIE1_UP11_FPGA_TX0_N 28 > PCIE1_UP11_FPGA_TX0_P 28
28 28	PCIE1_UP11_FPGA_RX1_N	AA4 AA3	GXPR11C_RX_CH1N GXPR11C RX CH1P	GXPR11C_TX_CH1N GXPR11C_TX_CH1P	Y6 Y5	PCIE1_UP11_FPGA_TX1_N 28 PCIE1_UP11_FPGA_TX1_P 28
28 28	PCIE1_UP11_FPGA_RX2_N	Y2 Y1	GXPR11C_RX_CH2N GXPR11C_RX_CH2P	GXPR11C_TX_CH2N GXPR11C_TX_CH2P	W8 W7	 PCIE1_UP11_FPGA_TX2_N 28 PCIE1 UP11 FPGA TX2 P 28
28 28	PCIE1_UP11_FPGA_RX3_N	W4 W3	GXPR11C_RX_CH3N GXPR11C_RX_CH3P	GXPR11C_TX_CH3N GXPR11C_TX_CH3P	V6 V5	 PCIE1_UP11_FPGA_TX3_N 28 PCIE1_UP11 FPGA_TX3_P 28
28 28	PCIE1_UP11_FPGA_RX4_N	V2 V1	GXPR11C_RX_CH4N GXPR11C_RX_CH4P	GXPR11C_TX_CH4N GXPR11C_TX_CH4P	U8 U7	 PCIE1_UP11_FPGA_TX4_N 28 PCIE1 UP11 FPGA TX4 P 28
28 28	PCIE1_UP11_FPGA_RX5_N	U4 U3	GXPR11C_RX_CH5N GXPR11C_RX_CH5P	GXPR11C_TX_CH5N GXPR11C_TX_CH5P	T6 T5	 PCIE1_UP11_FPGA_TX5_N 28 PCIE1_UP11_FPGA_TX5_P 28
28 28	PCIE1_UP11_FPGA_RX6_N	T2 T1	GXPR11C_RX_CH6N GXPR11C_RX_CH6P	GXPR11C_TX_CH6N GXPR11C_TX_CH6P	R8	 PCIE1_UP11_FPGA_TX6_N 28 PCIE1_UP11_FPGA_TX6_P 28
28 28	PCIE1_UP11_FPGA_RX7_N	R4 R3	GXPR11C_RX_CH7N GXPR11C_RX_CH7P	GXPR11C_TX_CH7N GXPR11C_TX_CH7P	P6	 PCIE1_UP11_FPGA_TX7_N 28 PCIE1_UP11_FPGA_TX7_P 28
28 28	PCIE1_UP11_FPGA_RX8_N	P2 P1	GXPR11C_RX_CH8N GXPR11C_RX_CH8P	GXPR11C_TX_CH8N GXPR11C_TX_CH8P	N8 N7	 PCIE1_UP11_FPGA_TX8_N 28 PCIE1_UP11_FPGA_TX8_N 28 PCIE1_UP11_FPGA_TX8_P 28
28 28	PCIE1_UP11_FPGA_RX9_N	N4 N3	GXPR11C_RX_CH9N GXPR11C_RX_CH9P	GXPR11C_TX_CH9N GXPR11C_TX_CH9P	M6 M5	 PCIE1_UP11_FPGA_TX9_N 28 PCIE1_UP11_FPGA_TX9_N 28 PCIE1_UP11_FPGA_TX9_P 28
28 28	PCIE1_UP11_FPGA_RX10_N	M2 M1	CYDD11C DV CU10N	GXPR11C_TX_CH10N GXPR11C_TX_CH10P	L8 L7	 PCIE1_UP11_FPGA_TX10_N 28 PCIE1_UP11_FPGA_TX10_P 28
28 28	PCIE1_UP11_FPGA_RX11_N	L4 L3		GXPR11C_TX_CH11N GXPR11C_TX_CH11P	K6 K5	 PCIE1_UP11_FPGA_TX10_1 PCIE1_UP11_FPGA_TX11_N PCIE1_UP11_FPGA_TX11_P 28
28 28		K2 K1	GXPR11C_RX_CH12N GXPR11C_RX_CH12P	GXPR11C_TX_CH12N GXPR11C_TX_CH12P		PCIE1_UP11_FPGA_TX12_N 28 PCIE1_UP11_FPGA_TX12_N 28 PCIE1_UP11_FPGA_TX12_P 28
28 28 28	PCIE1_UP11_FPGA_RX13_N	J4 J3	GXPR11C_RX_CH13N GXPR11C_RX_CH13P	GXPR11C_TX_CH13N GXPR11C_TX_CH13P		PCIE1_UP11_FPGA_TX12_F 28 PCIE1_UP11_FPGA_TX13_N 28 PCIE1_UP11_FPGA_TX13_P 28
28 28	PCIE1_UP11_FPGA_RX14_N	H2 H1	GXPR11C_RX_CH14N GXPR11C_RX_CH14P	GXPR11C_TX_CH14N GXPR11C_TX_CH14N GXPR11C_TX_CH14P	<u>68</u> <u>67</u>	 PCIE1_UP11_FPGA_TX14_N 28 PCIE1_UP11_FPGA_TX14_P 28
28 28 28	PCIE1_UP11_FPGA_RX15_N	G4 G3	GXPR11C_RX_CH15N	GXPR11C_TX_CH15N GXPR11C_TX_CH15P	F6 F5	PCIE1_UP11_FPGA_TX14_F 28 PCIE1_UP11_FPGA_TX15_N 28 PCIE1_UP11_FPGA_TX15_P 28
28 28	PCIE1_UP11_FPGA_RX16_N	F2 F1	GXPR11C_RX_CH16N GXPR11C_RX_CH16N GXPR11C_RX_CH16P	GXPR11C_TX_CH16N GXPR11C_TX_CH16N GXPR11C_TX_CH16P	<u>E8</u> <u>E7</u>	 PCIE1_UP11_FPGA_TX16_N 28 PCIE1_UP11_FPGA_TX16_N 28 PCIE1_UP11_FPGA_TX16_P 28
28 28	PCIE1_UP11_FPGA_RX17_N	E4 E3		GXPR11C_TX_CH17N GXPR11C_TX_CH17N GXPR11C_TX_CH17P	D6	PCIE1_UP11_FPGA_TX17_N 28 PCIE1_UP11_FPGA_TX17_N 28 PCIE1_UP11_FPGA_TX17_P 28
28 28		D2 D1	GXPR11C_RX_CH18N GXPR11C_RX_CH18N GXPR11C_RX_CH18P	GXPR11C_TX_CH18N GXPR11C_TX_CH18N GXPR11C_TX_CH18P		 PCIE1_UP11_FPGA_TX18_N 28 PCIE1_UP11_FPGA_TX18_N 28 PCIE1_UP11_FPGA_TX18_P 28
28	PCIE1_UP11_FPGA_RX19_N	(4 (3	GXPR11C_RX_CH19N	GXPR11C_TX_CH19N	<u>B6</u> B5	PCIE1_UP11_FPGA_TX19_N 28
20			GXPR11C_RX_CH19P	GXPR11C_TX_CH19P		PCIE1_UP11_FPGA_TX19_P 28
1	PCIE1_UP11_IO_RE8 7 PCIE1 UP11 REFCLK0 N	V11		N		
	7 PCIE1_UP11_REFCLK0_P		REFCLK_GXPR11C_CHO	P		
	7 PCIE1_UP11_REFCLK2_N	~	REFCLK_GXPR11C_CH2 REFCLK_GXPR11C_CH2			
	1255	DNI	XCVR BA	NK 11C		

A.8. SlimSAS Connector

Each PCIe or UPI interface connects to two slim SAS connectors, one for transmit signals and one for receive signals. Cables are used to connect the UPI or PCIe links from the devkit to the host board.

For UPI interface:

- UPI 0 Link, P-tile (10B) is routed to J55(FPGA-to-CPU) and J65(CPU-to-FPGA)
- UPI 1 Link, P-tile (11B) is routed to J38(FPGA-to-CPU) and J40(CPU-to-FPGA)
- UPI 2 Link, P-tile (11C) is routed to J39(FPGA-to-CPU) and J41(CPU-to-FPGA)



Figure 46. SlimSAS Connector Pinout

	A		B Latch Side			A		B Latch Side	
1	GND		GND	1	1	GND		GND	1
2	TX_18_DN		TX_19_DN	2	2	RX_19_DN		RX_18_DN	2
3	TX_18_DP		TX_19_DP	3	3	RX_19_DP		RX_18_DP	3
4	GND		GND	4	4	GND		GND	4
5	TX_16_DN		TX_17_DN	5	5	RX_17_DN		RX_16_DN	5
6	TX_16_DP		TX_17_DP	6	6	RX_17_DP		RX_16_DP	6
7	GND		GND	7	7	GND		GND	7
8	TX_14_DN		TX_15_DN	8	8	RX_15_DN		RX_14_DN	8
9	TX_14_DP		TX_15_DP	9	9	RX_15_DP		RX_14_DP	9
10	GND		GND	10	 10	GND		GND	10
11	TX_12_DN		TX_13_DN	11	11	RX_13_DN		RX_12_DN	11
12	TX_12_DP		TX_13_DP	12	12	RX_13_DP		RX_12_DP	12
13	GND		GND	13	13	GND	_	GND	13
14	TX_10_DN	$\overline{}$	TX_11_DN	14	14	RX_11_DN	2	RX_10_DN	14
15	TX_10_DP	÷	TX_11_DP	15	15	RX_11_DP	÷	RX_10_DP	15
16	GND	e e	GND	16	 16	GND	e e	GND	16
17	TX_8_DN	d	TX_9_DN	17	17	RX_9_DN	р	RX_8_DN	17
18	TX_8_DP	<u>S</u>	TX_9_DP	18	18	RX_9_DP	<u>o</u> r	RX_8_DP	18
19	GND	TX Fixed Connector Pinout	GND	19	19	GND	RX Fixed Connector Pinout	GND	19
20	TX_6_DN	۲ä	TX_7_DN	20	20	RX_7_DN	Ct	RX_6_DN	20
21	TX_6_DP	9	TX_7_DP	21	21	RX_7_DP	or	RX_6_DP	21
22	GND	P:	GND	22	22	GND RX_5_DN	P:	GND RX_4_DN	22
23 24	TX_4_DN TX_4_DP	on	TX_5_DN TX_5_DP	23	23 24	RX_5_DN	no	RX_4_DN RX_4_DP	23 24
24	GND	ut	GND	24 25	24 25	GND	ut	GND	24
25	TX_2_DN		TX_3_DN	25	25	RX_3_DN		RX_2_DN	25
20	TX_2_DN TX_2_DP		TX_3_DN TX_3_DP	20	20	RX_3_DP		RX_2_DR	20
27	GND		GND	27	27	GND		GND	27
20	TX_0_DN		TX_1_DN	20	20	RX_1_DN		RX_0_DN	20
30	TX_0_DP		TX_1_DP	30	30	RX_1_DR		RX_0_DP	30
31	GND		GND	31	31	GND		GND	31
32	TX_MISC_2		TX_MISC_6	32	32	RX_MISC_6		RX_MISC_2	32
33	TX_MISC_1		TX_MISC_5	33	33	RX_MISC_5		RX_MISC_1	33
34	GND		GND	34	34	GND		GND	34
35	BCLK_OUT_DN		TX_MISC_4	35	 35	RX_MISC_4		BCLK_IN_DN	35
36	BCLK_OUT_DP		TX_MISC_3	36	36	RX_MISC_3		BCLK_IN_DP	36
37	GND		GND	37	37	GND		GND	37

A.9. QSFP Network Interface

The Intel Stratix 10 DX FPGA Development Kit supports two QSFP28 connectors each connecting to the E-Tile (9A) transceivers. Each port can operate at 2x50G or 4x25G. These two ports support ZQSFP56 SR Optical modules as well as 3M DAC electrical cables.

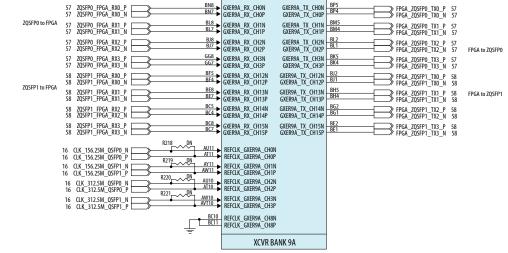
The FPC202 dual port controller (from Texas Instruments) serves as the low speed signal aggregator that makes up the Dual 100Gpbs Ethernet interfaces. The FPC202 aggregates all low speed and I2C signals across two ports and presents it as a single





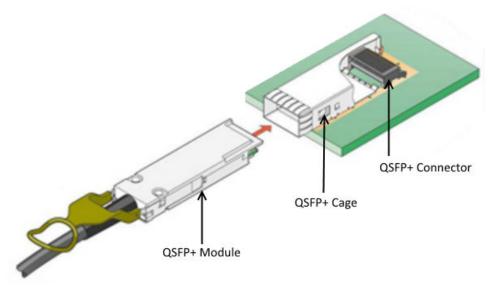
management interface to the host. The current limiters TP2557 (from Texas Instruments) also limit the current, in case if there is a short in the DAC electrical cables or Optical modules.

Figure 47. Transceiver QSFP-56 Two Ports of 25GbE



The E-tile (9A) of the Intel Stratix 10 DX FPGA provides eight transceiver channels, channel 0-3 are routed to QSFP0 and channel 12-15 are routed to QSFP1. The transceiver bank requires 156.25 MHz clocks for 28 Gbps NRZ and 325.50 MHz clocks for 56 Gbps PAM4. These clocks must have RPM jitter< 250 fs.

Figure 48. QSFP Connector

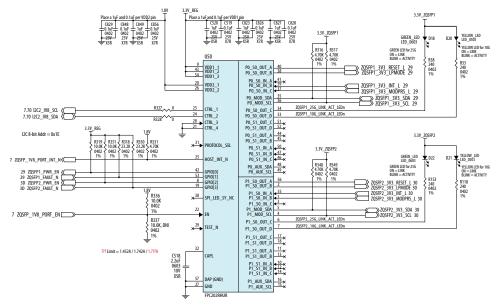


A.9.1. Dual Port Controller

The FPC202 dual port controller (from Texas Instruments) serves as the low speed signal aggregator for the two QSFP ports.



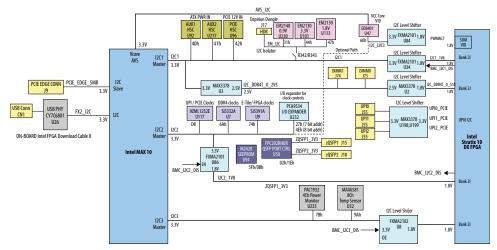
Figure 49. Dual Port Controller



A.10. I²C Interface

 $\rm I^2C$ interface supports communication between integrated circuits on a board. It is a simple two-wire bus that consists of a serial data line (SDA) and a serial clock (SCL). The Intel MAX 10 and Intel Stratix 10 devices use the I^2C interface for reading and writing to various components on the board such as programmable clock generators, VID regulators, ADC, and temperature sensors.

Figure 50. I²C Chain



You can use the Intel MAX 10 or Intel Stratix 10 device as the I^2C host to access these devices, change clock frequencies, or get status information of the board such as voltage and temperature readings.





Table 12.I²C Device Address

Туре	Bus	Address	Device
		0x31	EM2140 (U230)
	I2C1	0x44	EM2130 (U101)
		0x47	EM2130 (U113)
		0xD8/0x6C	97ML1252E (U117)
		0x6A	Si5332A (U7)
Intel Stratix 10 / Intel MAX 10 I ² C	I2C2	0x74	Si5391A (U9)
Address		0x4E/0x27	PCA9534 (U232)
		0x57	M24128 (U94)
		0x02	QSFP1 (U50)
-		0x1E	QSFP2 (U50)
	I2C3	0x4D/0x9A	MAX6581 (U32)
	PCIE_EP_3V3_I2C	TBD	PCIe End Point (J9)

A.11. QSPI Flash Memory

A.11.1. Configuration QSPI Flash Memory

The Intel Stratix 10 DX FPGA Development Kit has one 2-Gbit QSPI flash device for non-volatile storage of the FPGA configuration data, board information, test application data and user code space.

The flash device is implemented to achieve a 4-bit wide data bus. Only Intel MAX 10 CPLD can access this flash device. The Intel MAX 10 CPLD accesses are for AVST x8 configuration of the FPGA at power-on and board reset events. It uses the Parallel Flash Loader (PFL) II IP core.

Block	Access	Size	Address
Reserved	RW	17,920 KB	0x510.0000 - FFF.FFFF
Factory image	RW	81,920 KB	0x010.0000 - 50F.FFFF
PFL Option bits	RW	960 KB	0x001.0000 - 00F.FFFF
Reserved	RW	64 KB	0x000.0000 - 000.FFFF

Table 13.Memory Map of the QSPI 2G Flash

A.11.2. NIOS QSPI Flash Memory

The Intel Stratix 10 DX FPGA development board has a 64 Mb QSPI flash for non-volatile storage of the NIOS application data, board information, test application data, and user code space.

The quad-serial flash provided has a $\times 4$ data width, which can support an x1 access mode and $\times 4$ access mode. This memory provides non-volatile storage for Board Test System Scratch, Board Information, and other information.



Table 14. NIOS QSPI Flash Memory Map

Block	Size (KB)	Address	Description
Board Test System Scratch	512	078.0000 - 07F.FFFF	BTS System Testing
Board Information	64	077.0000 - 077.FFFF	Board Information
Reserved	7616	000.0000 - 076.FFFF	Reserved
Total	8192	-	-



intel

B. Safety and Regulatory Information

ENGINEERING EVALUATION KIT - THIS DEVICE IS INTENDED FOR EVALUATION ONLY! NOT FCC APPROVED FOR RESALE



This product has not been tested or approved by any agency or approval body for Electrical Safety, Electromagnetic Compatibility, Wired, or Wireless Telecommunications at the time of distribution.

Sales are limited to product developers, software developers, and system integrators; FCC NOTICE: This development kit is designed to allow:

- Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled, may not be resold or otherwise marketed unless all required.

FCC equipment authorizations are first obtained. Operation is subject to the condition that this product does not cause harmful interference to licensed radio stations and that this product does accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18, or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under FCC Part 5 of CFR Title 47.

Safety Certifications that may be required for installation and operation in your region have not been obtained.

B.1. Safety Warnings

Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts inside the power supply.

ISO 9001:2015 Registered

Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.



Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet shall be installed near the equipment and shall be readily accessible.

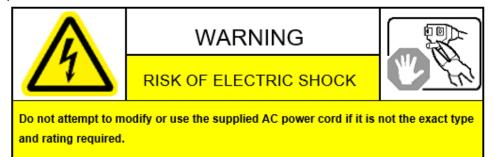
System Grounding (Earthing)

To avoid shock, ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug which is designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. For more information, refer to the website. If the power cord supplied with the system does not meet requirements for use in your region discard the cord, do not use with adapters.



Lightning or Electrical Storm

Do not connect or disconnect any cables or perform installation or maintenance of this product during an electrical storm.







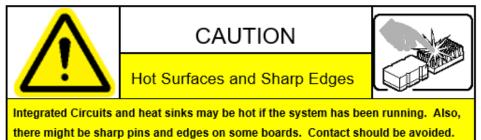
Risk of Fire

To reduce the risk of fire, keep all flammable materials at a safe distance from the boards and power supply and configure the development product on a flame-retardant surface.

B.2. Safety Cautions

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot, heatsink fans are not guarded, and power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front, and back of the development product for cooling purposes; do not block power supply ventilation holes and fan.







Electro Magnetic Interference

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy, which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, take measures to eliminate the interference.

Telecommunications Port Restrictions

The wireline telecommunication ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements has been obtained.

Electrostatic Discharge Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to do so can damage components within the system.



Please return this product to Intel for proper disposition. If it is not returned, refer to the local environmental regulations for proper recycling; do not dispose this product in any unsorted municipal waste.



C. Compliance and Conformity Information

CE EMI Conformity Caution

CE

Hereby, Intel Corporation declares that the Intel Stratix 10 DX FPGA Development Kit Board is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU. Because of the nature of programmable logic devices, it is possible for the end user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

For more information, refer to the EU declaration of conformity.

Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. *Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Altera:

DK-DEV-1SDX-P-A DK-DEV-1SDX-P-0ES