MAX® 10 FPGA Development Kit User Guide

Contents

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1. Overview

The MAX® 10 FPGA Development Kit provides a hardware platform for evaluating the performance and features of the MAX 10 device.

Table 1.   Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Starting Serial Number
MAX 10 FPGA Development Kit (Production)	DK-DEV-10M50-C	10M50DAF484I6G	10M50DA1000001
MAX 10 FPGA Development Kit (ES)	DK-DEV-10M50-A	10M50DAF484C6GES	10M50DA0000001

Figure 1.   MAX 10 FPGA Development Kit—Top View

Figure 2.   MAX 10 FPGA Development Kit—Bottom View

Note: To determine the revision of your board, look for the serial number at the bottom of the board.
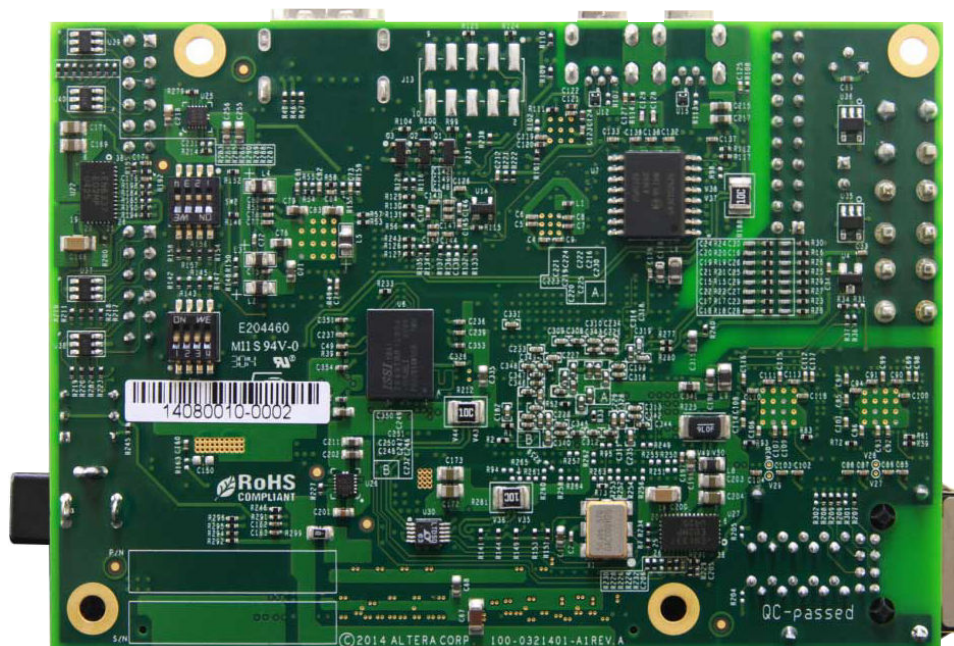
Refer to the *Appendix A—Development Kit Components* section for more details about the components on the MAX 10 FPGA Development Kit.

Related Information

Development Kit Components on page 33

1.1. Block Diagram

Figure 3.   MAX 10 FPGA Development Kit Block Diagram
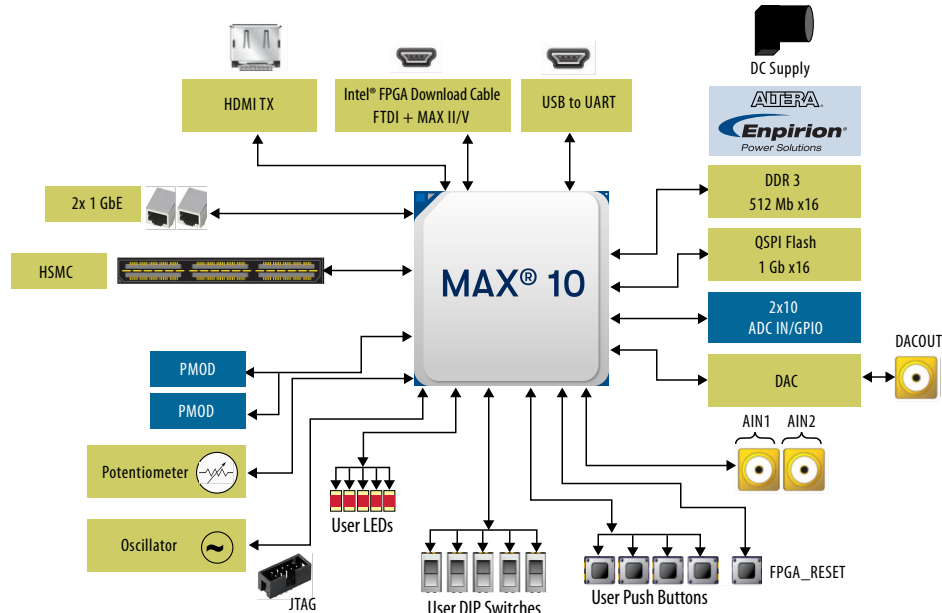
1.2. Feature Summary

The MAX 10 FPGA Development Kit includes a RoHS- and CE-compliant MAX 10 FPGA development board with the following components:

Featured Devices

- MAX 10 FPGA (10M50D, dual supply, F484 package)
- Enpirion® EN2342QI 4 A PowerSoC Voltage-Mode Synchronous Step-Down Converter with Integrated Inductor Enpirion
- EN6337QI 3 A High-Efficiency PowerSoC DC-DC Step-Down Converters with Integrated Inductor
- Enpirion EP5358xUI 600 mA PowerSoC DC-DC Step-Down Converters with Integrated Inductor
- MAX II CPLD – EPM1270M256C4N (On-board Intel® FPGA Download Cable II)

Programming and Configuration

- Embedded Intel FPGA Download Cable II (JTAG)
- Optional JTAG direct via 10-pin header

Memory Devices

- 64-Mx16 1 Gb DDR3 SDRAM with soft memory controller
- 128-Mx8 1 Gb DDR3 SDRAM with soft memory controller
- 512-Mb Quad serial peripheral interface (quad SPI) flash

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Communication Ports

- Two Gigabit Ethernet (GbE) RJ-45 ports
  - — Ethernet Port A (Bottom)
  - — Ethernet Port B (Top)
- One mini-USB2.0 UART
- One high-definition multimedia interface (HDMI) video output
- One universal high-speed mezzanine card (HSMC) connector
- Two 12-pin Digilent Pmod* compatible connectors

Analog

- Two MAX 10 FPGA analog-to-digital converter (ADC) SMA inputs
- 2x10 ADC header
- Potentiometer input to ADC
- One external 16 bit digital-to-analog converter (DAC) device with SMA output

Clocking

- 25 MHz single-ended, external oscillator clock source
- Silicon Labs clock generator with programmable frequency GUI

Cables

Mini-USB cable for on-board Intel FPGA Download Cable II

Power

2A power supply and cord

Software

Free Quartus® Prime software (download software and license from website)

1.3. Box Contents

- MAX 10 FPGA Development Kit
- Power adapter
- Mini-B USB to USB cable

Related Information

MAX 10 FPGA Development Kit Website

2. Getting Started

2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit of installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix C.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.

2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus Prime software
- MAX 10 FPGA Development Kit software
- Intel FPGA Download Cable II driver

2.3.1. Installing the Quartus Prime Software

1. Download the Quartus Prime software from the FPGA Software Download Center webpage of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Intel FPGA Software Installation and Licensing*.

Related Information

- Quartus Prime Standard Edition User Guide: Getting Started
- Intel FPGA Software Installation and Licensing

2.3.2. Installing the Development Kit

1. Download the MAX 10 FPGA Development Kit installer package from the MAX 10 FPGA Development Kit webpage on the Intel website.

2. Unzip the MAX 10 FPGA Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 4.   MAX 10 FPGA Development Kit Directory Structure
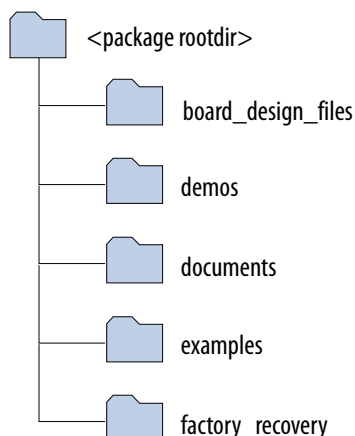
3. For the latest issues and release notes, Altera recommends that you review the readme.txt located in the root directory of the kit installation.

Table 2.   Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the MAX 10 FPGA Development Kit: • Board Test System: BTS GUI, Power GUI, and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO, ADC, and HDMI
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3.3. Installing the Intel FPGA Download Cable Driver

The development board includes integrated Intel FPGA Download Cable circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the On-Board Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

- Cable and Adapter Drivers Information
- Intel FPGA Download Cable II User Guide

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2.4. Board Update Portal

The Board Update Portal design example included in this development kit facilitates easy development of software and board flash memory updates, allowing you to access useful information on Intel website and to load software files into the Quad SPI flash memory on your board.The following steps ensure that you have the latest software available on both your computer and your board. The Board Update Portal design example, which includes a Nios® II embedded processor, an Ethernet media access control (MAC), and a web page, is stored in the "factory" portion of your board's flash memory. The source for this design is installed with the development kit software. When your board is connected to a DHCP-enabled network, the Nios II processor obtains an Internet protocol address and allows you to interface with your board over the network through a web page.

Before you begin, ensure that you have the following:

- A computer with a connection to a working Ethernet port on a DHCP-enabled network.

- A separate working Ethernet port connected to the same network for your board.

- The Ethernet, power cables, and development board included in your kit.

2.4.1. Step 1: Connect to the Board Update Portal

1. Install the Quartus Prime software. Refer to Installing the Quartus Prime Software for instructions.

2. With the board powered down, set the DIP switch SW2.2 to the ON position (factory default), which loads the factory default design from the MAX 10 FPGA internal flash image 0 on power up.

3. Attach the Ethernet cable from RJ-45 port A (the bottom one) to your network hub.

4. Power up the board. The board connects to your network server and obtains an Internet protocol address.

5. On installation directory of the Quartus Prime software, click **nios2eds ➤ Nios II Command Shell.bat**

6. In the Nios II command shell, type the following command:

   ```
   nios2-terminal.exe
   ```

   When the IP address has been assigned, the command shell displays the following information:

7. Launch a web browser on a computer that is connected to the same network and type the Internet protocol address displayed on the Nios II command shell. The Board Update Portal web page appears on your PC.

Note: If you cannot connect to the Board Update Portal, refer to the `readme.txt` file under *<package rootdir>*\`factory_recovery` directory on how you can recover the factory build.

2.4.2. Step 2: Update the User Software Portion

To update the user software portion of flash memory on your board, follow these steps:

1. Prepare your software image and change it to the `user_flash.flash file` with the **elf2flash** utility. Make sure that the "`--reset`" option is set to Flash memory base address + Reset Vector Offset (`0x0083_0000`).

2. Perform the steps in Step 1: Connect to the Board Update Portal to display the Board Update Portal web page.

3. In the **Software File Name** field, specify your `user_flash.flash` file.

4. Click **Upload**.

5. Reprogram the user dual configuration image into Configuration Flash Memory (CFM).

   - Image 0: BUP A build

   - Image 1: User Nios II processor-based build

   - Make sure the user Nios II processor-based build boots up from the reset vector offset "`0x0083_0000`".

6. Power off the board.

7. Change the SW2.2 to the OFF position (1) to make sure that it boots up from image 1.

8. Power on the board.

The new user software image and user hardware build are now running in the FPGA.

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3. Board Test System

This kit includes an application called the Board Test System (BTS).

The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

Figure 5.   Board Test System GUI
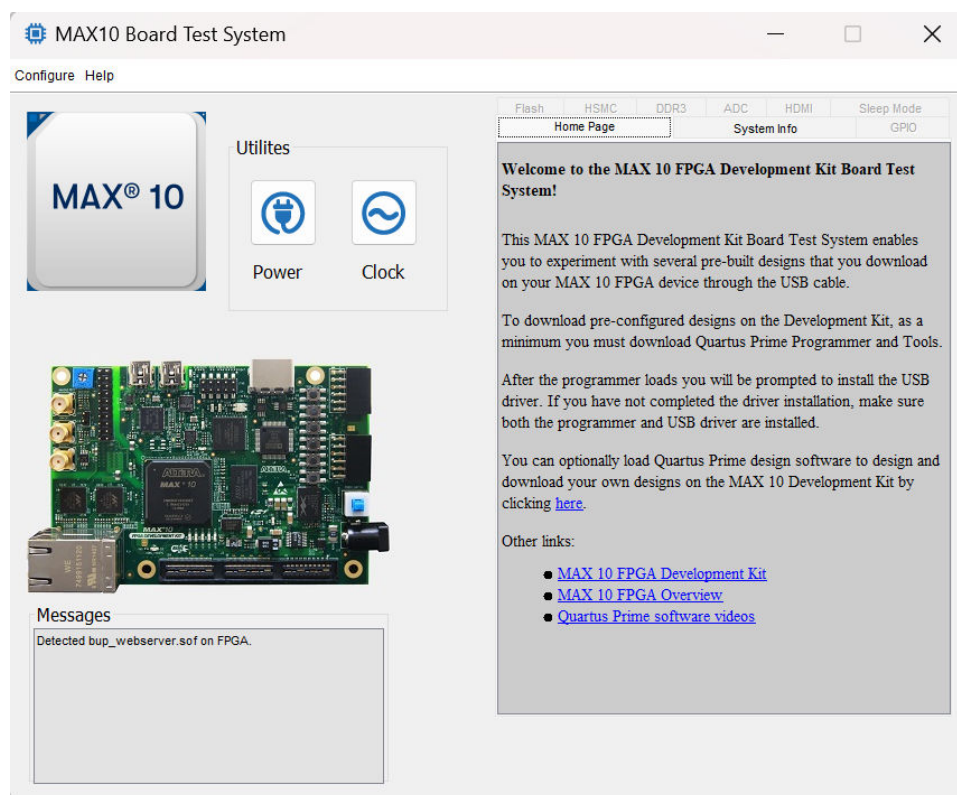
Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the Signal Tap Logic Analyzer. Because the Quartus Prime programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus Prime Programmer.

3.1. Using the Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

Figure 6.   The Configure Menu
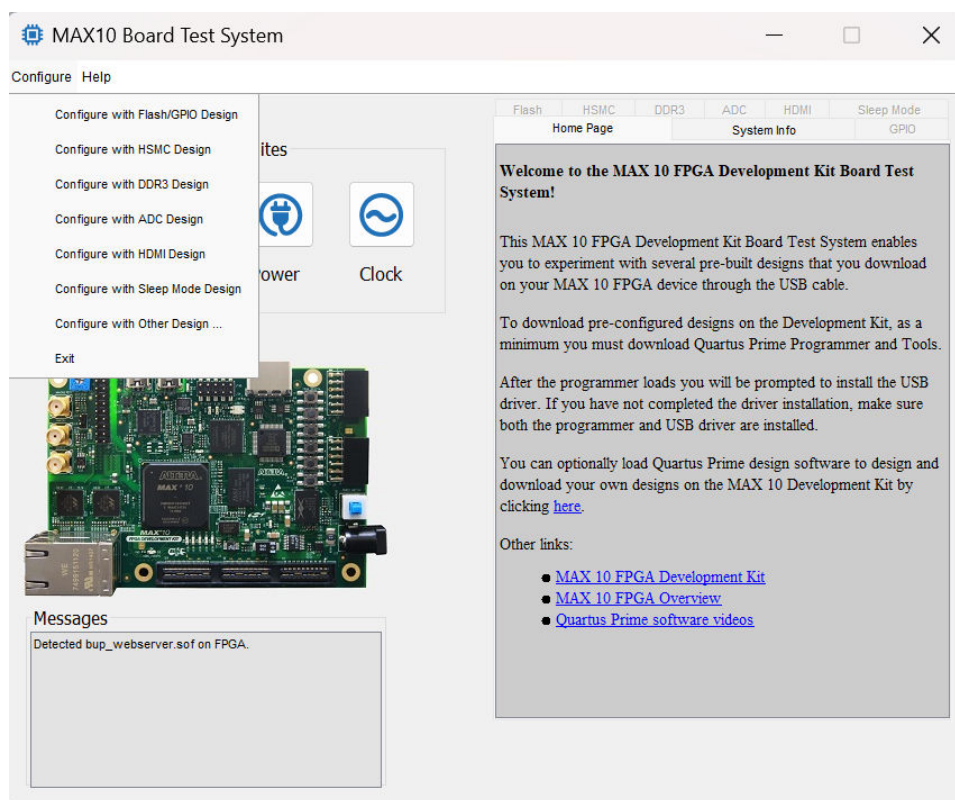
To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** menu, click the configure command that corresponds to the functionality you want to test.

2. In the dialog box that appears, click **Configure** to download the corresponding design to the FPGA.

3. When configuration finishes, close the Quartus Prime Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Quartus Prime Programmer for configuration, rather than the Board Test System GUI, you may need to restart the GUI.

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3.2. The System Info Tab

The **System Info** tab shows the board's current configuration. The tab displays the JTAG chain, the board's MAC address, the Qsys memory map, and other details stored on the board.

Figure 7.   The System Info Tab
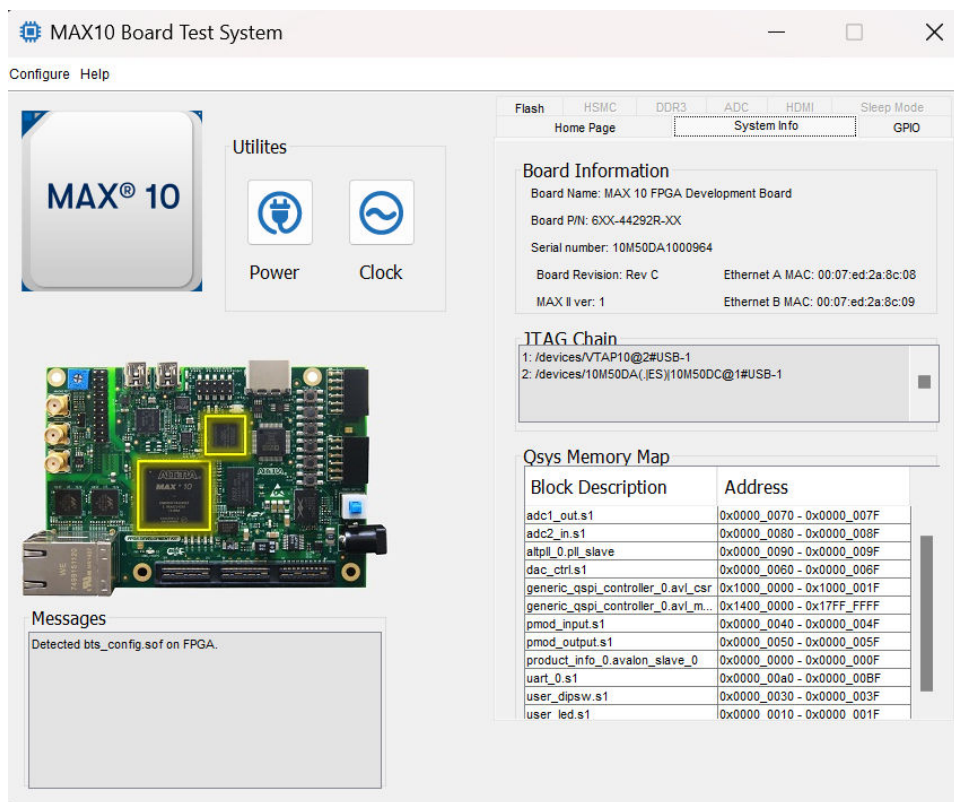
Table 3.   Controls on the System Info Tab

Controls	Description
Board Information Controls	The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board.
Board Name	Indicates the official name of the board, given by the Board Test System.
Board P/N	Indicates the part number of the board.
Serial Number	Indicates the serial number of the board.
Factory Test Version	Indicates the version of the Board Test System currently running on the board.
MAX Version	Indicates the version of MAX code currently running on the board.
Ethernet A MAC	Indicates the Ethernet A MAC address of the board.

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Controls	Description
Ethernet B MAC	Indicates the Ethernet B MAC address of the board.
JTAG Chain	Shows all the devices currently in the JTAG chain.
Qsys Memory Map	Shows the memory map of the Platform Designer (Standard) system on your board.

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3.3. The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 8.   The GPIO Tab
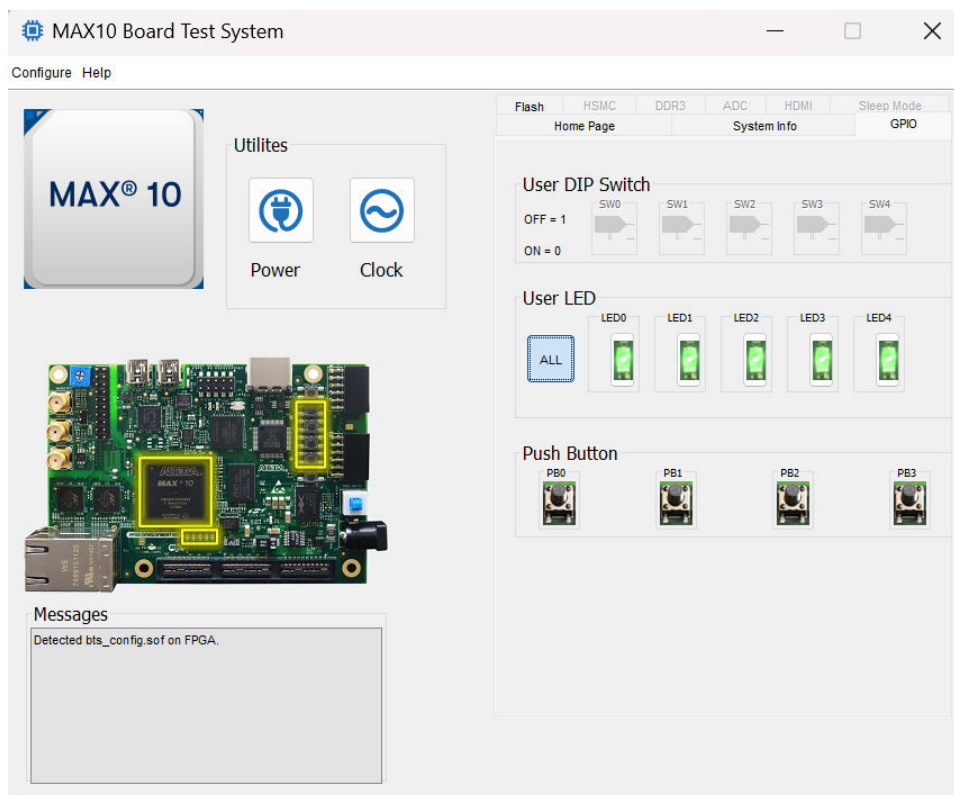
Table 4.   Controls on the GPIO Tab

Control	Description
User DIP Switch	Displays the current positions of the switches in the user DIP switch banks. Change the switches on the board to see the graphical display change accordingly.
User LED	Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click the **0** to **4** buttons to toggle red or green LEDs, or click the **All** button.
Push Button	Read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

3.4. The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board.

Figure 9.   The Flash Tab (Detail)
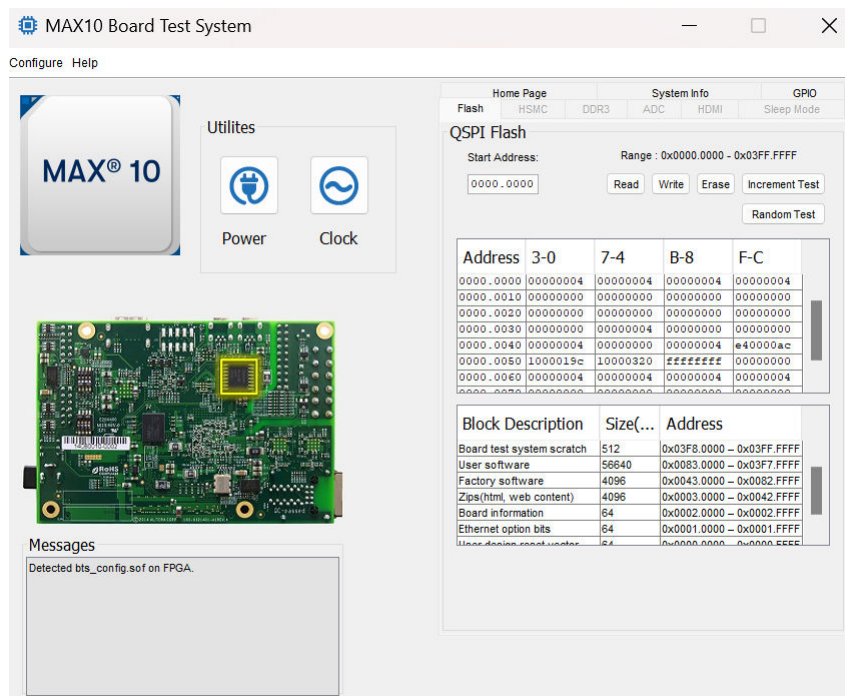
Table 5.   Controls on the Flash Tab

Control	Description
Read	Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table.
Write	Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.
Erase	Erases flash memory.
Increment Test	Starts an incrementing data pattern test to flash memory, limited to the 512 K test system scratch page.
Random Test	Starts a random data pattern test to flash memory, limited to the 512 K test system scratch page.
Flash Memory Map	Displays the flash memory map for the development board.

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3.5. The HSMC Tab

The **HSMC** tab allows you to test the CMOS port.

Figure 10.   The HSMC Tab
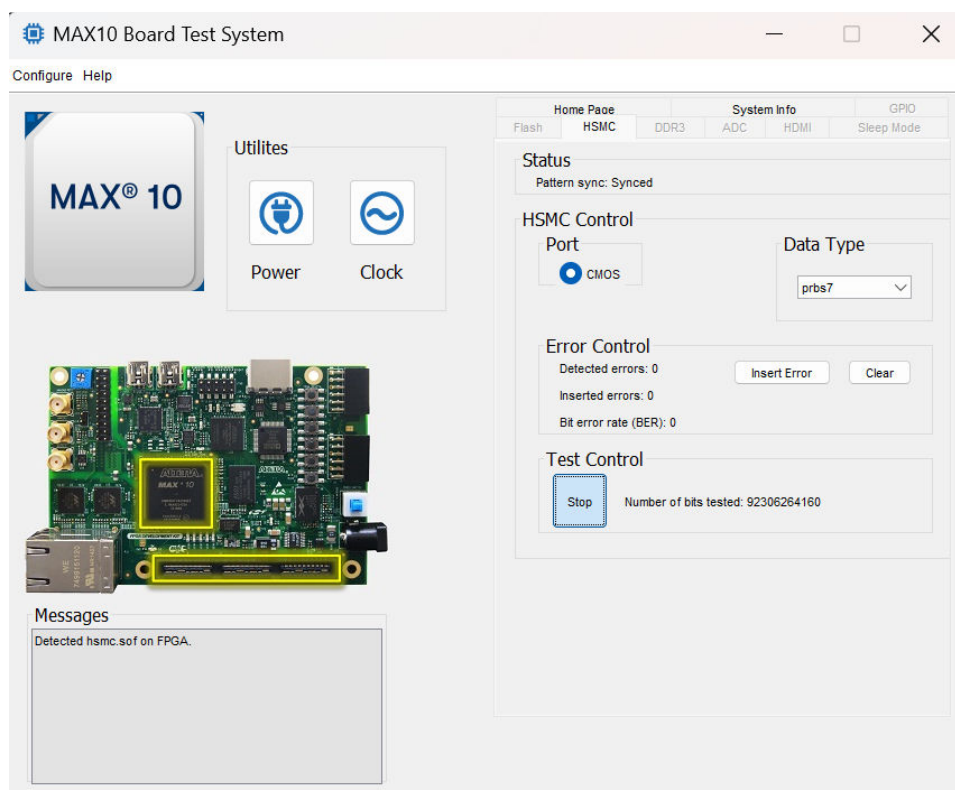
Table 6.   Controls on the HSMC Tab

Control	Description
Status	**Pattern sync**: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
Port	**CMOS**: The CMOS port is available for tests.
Data Type	The following data types are available for analysis: • **prbs7**: Selects pseudo-random 7-bit sequences. • **prbs15**: Selects pseudo-random 15-bit sequences. • **prbs23**: Selects pseudo-random 23-bit sequences.

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Control	Description
	• **prbs31**: Selects pseudo-random 31-bit sequences. • **high_frequency**: Divide by data pattern. • **low_frequency**: Divide by data pattern.
Error Control	• **Detected errors**: Displays the number of data errors detected in the hardware. • **Inserted errors**: Displays the number of errors inserted into the transmit data stream. • **Bit error rate (BER)**: Displays the bit error rate of the interface • **Insert Error**: Inserts a one-word error into the transmit data stream each time you click the button. • **Clear**: Resets the **Detected errors** and **Inserted errors** counters to zeroes.
Test Control	• **Stop**: Resets the test. • **Number of bits tested**: Displays the number of bits tested since the last reset.

3.6. The DDR3 Tab

The **DDR3** tab allows you to test the DDR3 by reading and writing to a selected amount of addresses.

Figure 11.   The DDR3 Tab
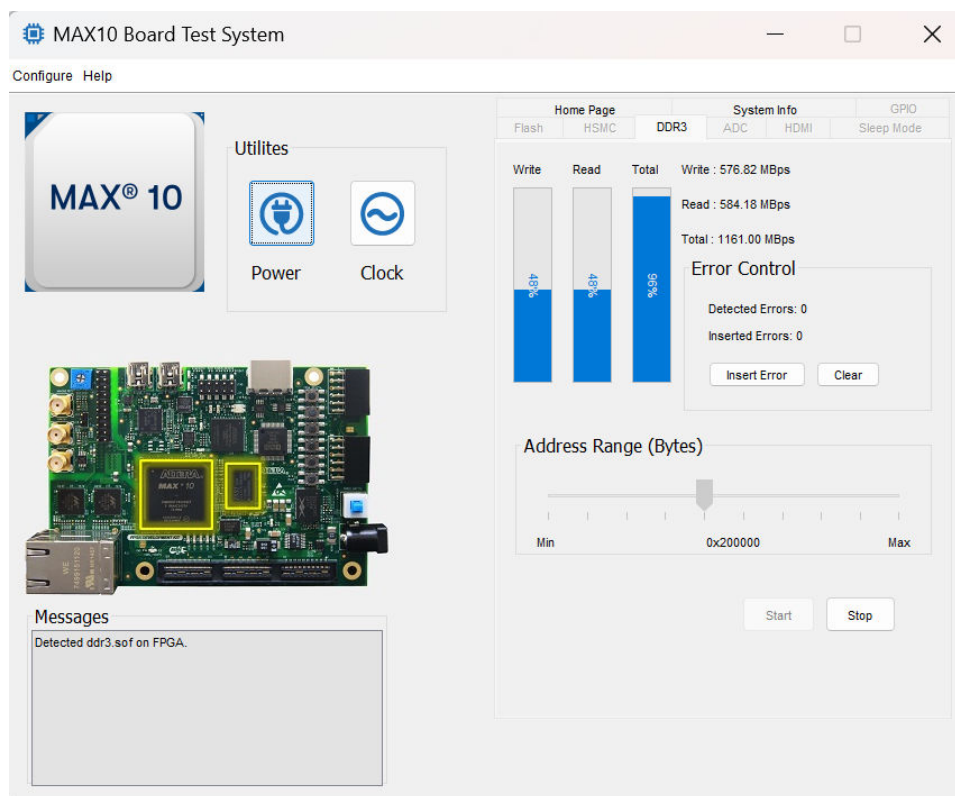
Table 7.   Controls on the DDR3 Tab

Control	Description
Performance Indicators	These controls display current transaction performance analysis information collected since you last clicked **Start**: • **Write**, **Read**, and **Total** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve. • **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**—Show the number of bytes of data analyzed per second. • Data bus: 72 bits (8 bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Megabits per second (Mbps) per pin. Equating to a theoretical maximum bandwidth of 136512 Mbps or 17064 MBps.
Error Control	This control displays data errors detected during analysis and allows you to insert errors:

continued...

Control	Description
	• **Detected errors**—Displays the number of data errors detected in the hardware. • **Inserted errors**—Displays the number of errors inserted into the transaction stream. • **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • **Clear**—Resets the Detected errors and Inserted errors counters to zeroes.
Address Range (Bytes)	Determines the number of addresses to use in each iteration of reads and writes.

3.7. The ADC Tab

The **ADC** tab (analog-to-digital) shows the real-time voltage values of all of the ADC input channels.

Figure 12.   The ADC Tab
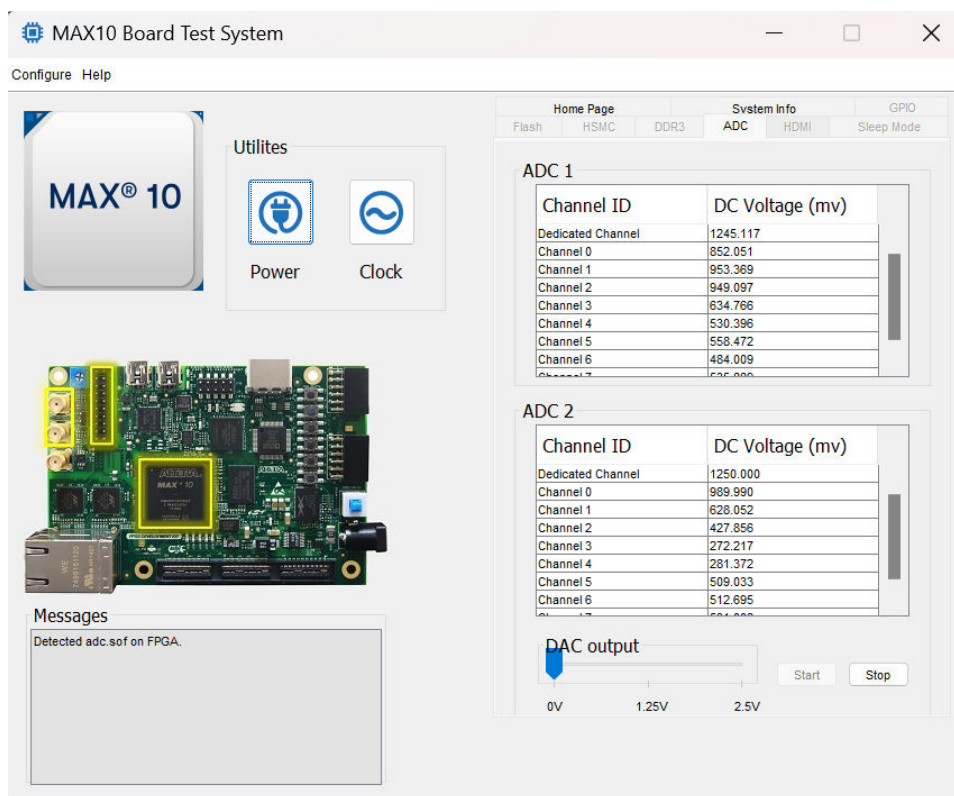
The two tables displayed on this tab, **ADC 1** and **ADC 2**, are not editable.

The following tables show where the channels connect to.

Table 8.   ADC 1 Channel Connection

Dedicated Channel	SMA Connector
ADC 1	**ANAIN1_SMA(J18)**
Channel 0	ADC1_CH0(J20.1)
Channel 1	ADC1_CH1(J20.3)
Channel 2	ADC1_CH2(J20.5)
Channel 3	ADC1_CH2(J20.7)
Channel 4	ADC1_CH4(J20.11)
Channel 5	ADC1_CH4(J20.13)
Channel 6	ADC1_CH6(J20.15 or POT1)
Channel 7	ADC1_CH7(J20.17)

Table 9. **ADC 2 Channel Connection**

Dedicated Channel	SMA Connector
ADC 2	**ANAIN2_SMA(J19)**
Channel 0	ADC1_CH0(J20.2)
Channel 1	ADC1_CH1(J20.4)
Channel 2	ADC1_CH2(J20.6)
Channel 3	ADC1_CH2(J20.8)
Channel 4	ADC1_CH4(J20.12)
Channel 5	ADC1_CH4(J20.14)
Channel 6	ADC1_CH6(J20.16)
Channel 7	ADC1_CH7(J20.18)

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3.8. The HDMI Tab

The **HDMI** tab displays a transmitter color bar pattern from the high-definition multimedia interface (HDMI).

Figure 13.   The HDMI Tab
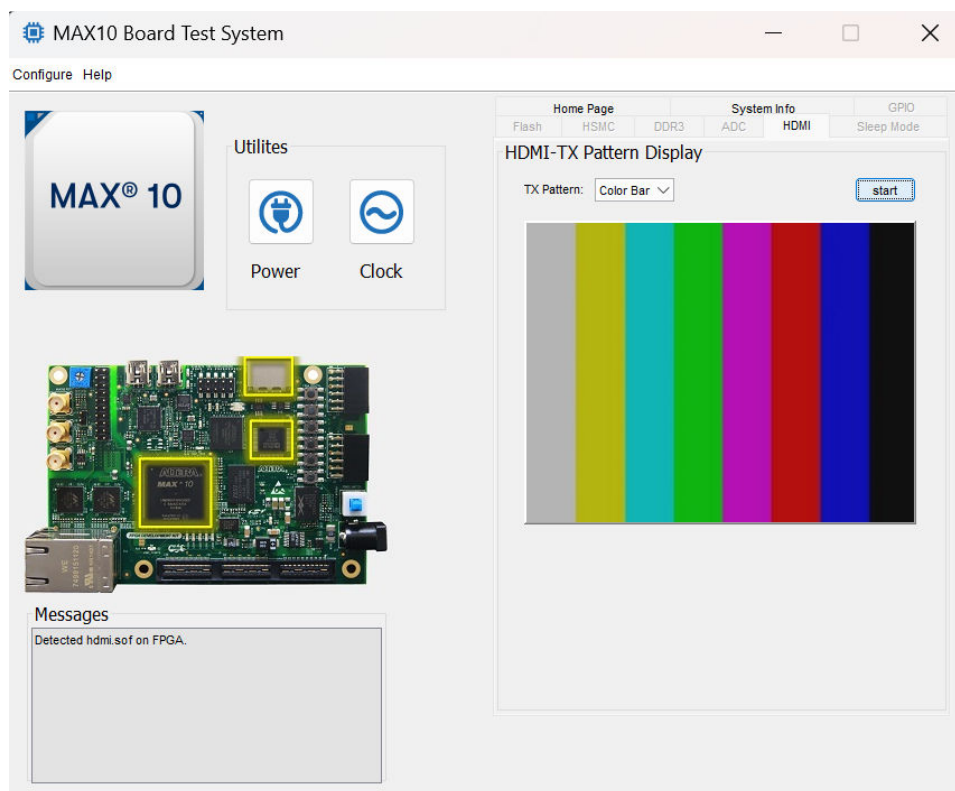
Table 10.   Controls on the HDMI Tab

Control	Description
TX Pattern	**Color Bar**: Use this control to choose TX patterns. The available choices are red, blue, green, white, and black. If you select the **Start** button, the TX pattern displays immediately.
Start	When you click this button, the selected TX pattern (from **Color Bar**) displays.

3.9. The Sleep Mode Tab

The **Sleep Mode** tab allows you to test the sleep mode aspect of the power management controller.

Figure 14.   The Sleep Mode Tab (Cropped View)
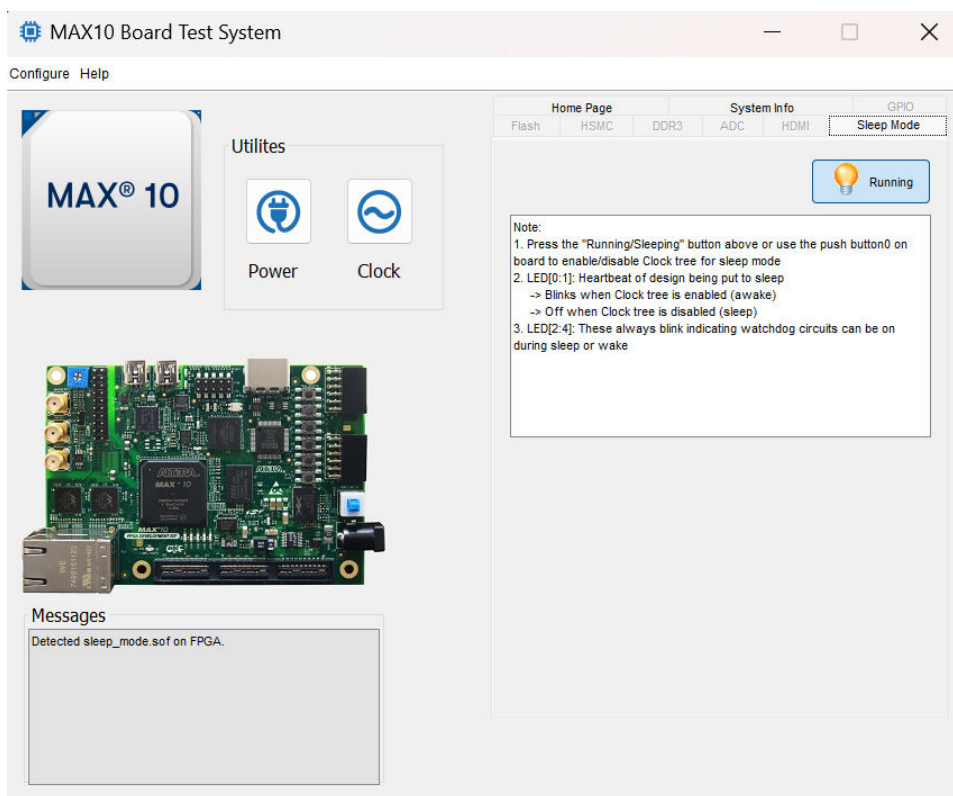
Table 11.   Controls on the Sleep Mode Tab

Control	Description
Running (or Sleeping)	This control displays the mode status as sleeping or running. It is not interactive.
Note	This control displays board LED events related to the sleep mode.

Related Information

MAX 10 FPGA Configuration User Guide
Provides detailed explanations and options for MAX 10 device configuration.

3.10. The Power Monitor

The **Power Monitor** measures and reports current power information and communicates with the MAX II device on the board through the JTAG bus. A power monitor circuit attached to the MAX II device allows you to measure the power that the FPGA is consuming.

To start the application, click the **Power Monitor** icon in the Board Test System application. You can also run the **Power Monitor** as a stand-alone application. The `PowerMonitor.bat` and `ClockController.bat` reside in the *<installer package>* `\examples\board_test_system` directory.

Note: You cannot run the stand-alone power application and the BTS application at the same time.

Figure 15. **The Power Monitor**
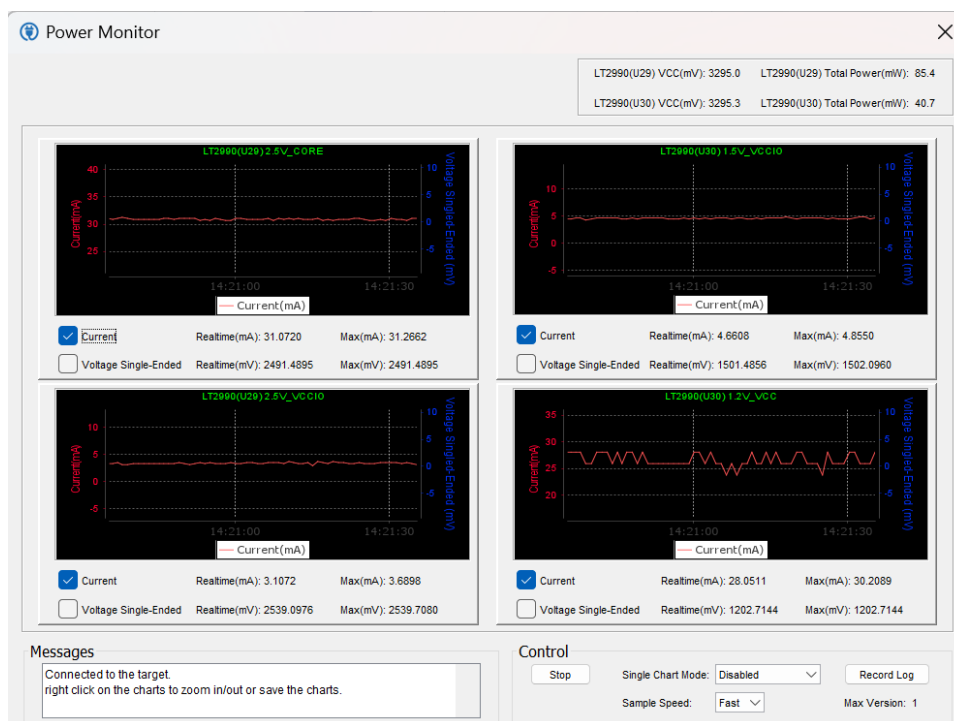
This window displays both LTC2990 current and temperature monitors. The left side top and bottom quadrant shows U29 and the opposite side shows U30. Use the available controls to show **Current** or **Voltage Single-Ended**, or both.

Single Chart Mode allows you to choose how you want the panes to display. You can show only a single large pane, if needed.

Voltage Single-Ended shows the voltage value of each power rail:

- 2.5 V $_{CORE}$
- 2.5 V $_{VCCIO}$
- 1.5 V $_{VCCIO}$
- 1.2 V $_{VCC}$

Single-ended shows the voltage of SENSE_P only.

The LT2990 also shows a differential voltage value of the sampling resistor SENSE_P and SENSE_N.

Sample Speed allows you to select **Slow** at 5 seconds, or **Fast** at 1 second (default).

Record Log saves a comma-separated values (CSV) format file `ltc2990.csv` in the `*\examples\board_test_system` directory.

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3.11. The Clock Controller

The MAX 10 FPGA development board **Clock Controller** application sets the programmable oscillators to any frequency between 10 MHz and 810 MHz. The frequencies support eight digits of precision to the right of the decimal point.

The **Clock Controller** communicates with the MAX II device on the board through the JTAG bus. The programmable oscillators are connected to the MAX II device through a 2-wire serial bus.

Figure 16.   The Si570 Tab
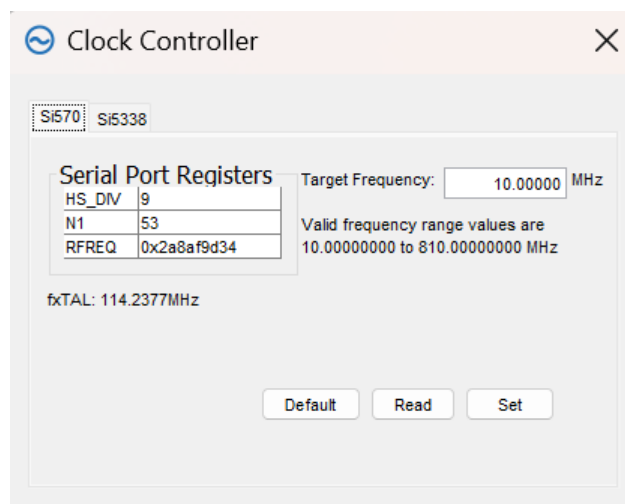
Table 12.   Controls on the Si570 Tab

Control	Description
Serial Port Registers	Shows the current values from the Si570 registers for frequency configuration.
Target Frequency	Allows you to specify the frequency (in MHz) of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target Frequency** control works in conjunction with the **Set** control.
fxTAL	Shows the calculated internal fixed-frequency crystal, based on the serial port register values.
Default	Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.
Read	Reads the current frequency setting for the oscillator associated with the active tab.
Set	Sets the programmable oscillator frequency for the selected clock to the value in the **Target Frequency** control for the programmable oscillators. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Figure 17.   The Si5338 Tab
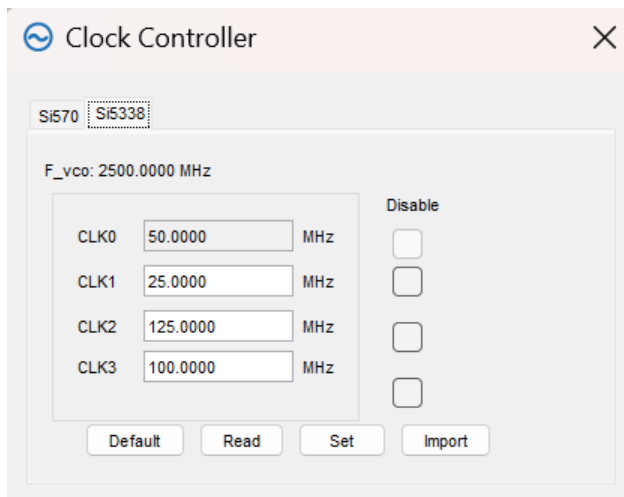
Table 13.   Controls on the Si5338 Tab

Control	Description
F_vco	Displays the generating signal value of the voltage-controlled oscillator.
Registers	Display the current frequencies for each oscillator.
Frequency	Allows you to specify the frequency (in MHz) of the clock.
Disable	Disable each oscillators as required.
Read	Reads the current frequency setting for the oscillator associated with the active tab.
Default	Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.
Set	Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK3 controls. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies. *Note:* Changing CLK0 of Si5338 affects the Clock Controller and Power Monitor GUIs. One clock from port CLK0 is used to drive the MAX II device which as a 2-wire serial bus interface connected to SI570, Si5338, and the power monitor.

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4. Document Revision History for the MAX 10 FPGA Development Kit User Guide

Document Version	Changes
2024.11.21	Corrected a typo in the starting serial number for the production version of the MAX 10 FPGA Development Kit.
2024.11.20	• Updated the *Overview* chapter: — Updated *Feature Summary*. — Added new topics: *Block Diagram* and *Box Content*. — Added new Table: *Ordering Information*. — Added new Figures: *MAX 10 FPGA Development Kit—Top View* and *MAX 10 FPGA Development Kit—Bottom View*. — Removed *General Description*. • Added new topics to the *Getting Started* chapter: — *Before You Begin* — *Handling the Board* — *Software and Driver Installation* — *Step 1: Connect to the Board Update Portal* — *Step 2: Update the User Software Portion* • Updated all figures in the *Board Test System* chapter. • Updated the following figures in the appendix chapter *Development Kit Components* for clarity: — Figure: *Jumper J7 on the Top of the Board (Detail)* — Figure: *Switches on the Bottom Board (Detail)* — Figure: *Power Distribution System* • Updated and retitled appendix chapter *Additional Information* to *Safety and Regulatory Compliance Information*: — Added new topics—*Safety and Regulatory Information*, *Safety Warnings*, and *Safety Cautions*. — Updated *Compliance Information*. • Restructured the document to improve clarity and for ease of reference. • Updated for the latest branding standards.

Date	Version	Changes
September 2017	2017.09.07	Updated I/O standard voltage values in the *On-Board Oscillators* table in *On-Board Oscillators*.
January 2017	2017.01.04	Corrected the following pin assignments in "10/100/1000 Ethernet PHY": • ENETA_TX_D1 on pin P5 • ENETA_RX_ER on pin U2 • ENET_MDIO on pin Y5 • ENETB_TX_D2 on pin U3 • ENETB_RS_D3 on pin R7
November 2015	2015.11.06	• Updated "USB to UART" section. • Added note to "General User Input/Output section".

continued...

Date	Version	Changes
June 2015	2015.06.26	• Updated "DDR3 Rev. B Board" section.
May 2015	2015.05.21	• Added quad SPI content for Rev. B & C boards. • Corrected two PMOD pin signal names for Rev. B & C boards. • Changed four MAX 10 pins for DDR3 for Rev. C board only. • Changed two switch/signal names for SW2 for Rev. C board only. • Updated *Switch and Jumper Settings* section with VTAP description.
March 2015	2015.03.31	Initial release.

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A. Development Kit Components

This chapter introduces all the important components on the development kit board.

A.1. Board Overview

This section describes all the components on the development board. A complete set of schematics, a physical layout database, and Gerber files for the development board reside in the development kit documents directory.

Figure 18.   Components in MAX 10 FPGA Development Kit (Top View)

Figure 19.   Components in MAX 10 FPGA Development Kit (Bottom View)

Note: To determine the revision of your board, look for the serial number at the bottom of the board.
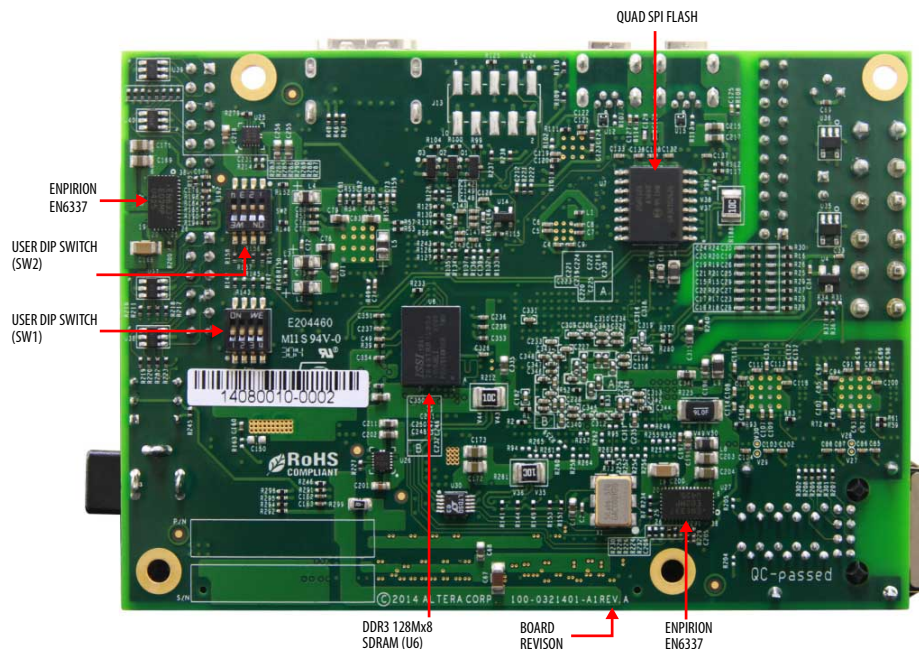
Table 14.   MAX 10 FPGA Development Kit—Board Components

Board Reference	Type	Description
Featured Devices		
U1	FPGA	MAX 10 FPGA 10M50DAF484I6G, 50K LEs, F484 package.
U13	CPLD	MAX II EPM1270 256-MBGA, 2.5 V/3.3 V, VCCINT for On-Board Intel FPGA Download Cable II.
U17	Power Regulator	Enpirion EN2342QI, PowerSoC voltage-mode synchronous step-down converter with integrated inductor.
U22, U23, U27	Power Regulator	Enpirion EN6337QI, PowerSoC DC-DC step-down converters with integrated inductor.
U26	Power Regulator	Enpirion EP5358LUI, 600 mA PowerSoC DC-DC step-down converters with integrated inductor.
U24, U25	Power Regulator	Enpirion EP5358HUI, 600 mA PowerSoC DC-DC step-down converters with integrated inductor.
Configuration and Setup Elements		
J12	On-Board (Embedded) Intel FPGA Download Cable II	Type-B USB connector for programming and debugging the FPGA.
J14	10-pin header	Optional JTAG direct via 10-pin header for external download cables.
J20	2x10-pin header	16 dual-purpose ADC channels are connected to the 2x10 header.

<div align="right">*continued...*</div>

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Board Reference	Type	Description
SW2	DIP configuration and user switch	SW2 Includes switches to control boot images, JTAG bypass and HSMC bypass.
J7	Jumper for the MAX 10 ADC	Connects potentiometer for providing adjustable voltage to the ADC.
S5	`Pulse_nconfig` push button	Emulates pulsing the `nCONFIG` pin low to trigger reconfiguration even though the physical pin is unaffected.
S6	CPU reset push button	Default reset for the FPGA logic.
Status Elements		
D1	Blue power LED	Illuminates when 12-V power is present.
D2	Green high-speed mezzanine card (HSMC) LED	Illuminates when the HSMC is present.
D13, D14	Green USB-UART LEDs	Illuminates when the USB-UART transmitter and receiver are in use.
D20	Configuration done LED	Illuminates when the FPGA is configured.
D21, D22, D23	Power LEDs	Indicates that 3.3 V, 2.5 V, 1.2 V are powered up successfully.
Clock Circuitry		
X1	Programmable Clock for ADC	Programmable oscillator for ADC with default frequency of 10 MHz.
U2	Programmable Clock	Four channel programmable oscillator with default frequencies of 25, 50, 100, and 125 MHz.
General User Input/Output		
S1, S2, S3, S4	General user push buttons	Four user push buttons. Driven low when pressed.
D15, D16, D17, D18, D19	User LEDs	Four user LEDs. Illuminates when driven low.
SW1, SW2.1	User DIP switches	Quad user DIP switches.
Memory Devices		
U5	DDR3 SDRAM A memory	64 Mx16.
U6	DDR3 SDRAM B memory	128 Mx8.
U7	Quad serial peripheral interface (quad SPI) flash	512 Mb.
Communication Ports		
J2	HSMC port	Provides 84 CMOS or 17 LVDS channels per HSMC specification.
U9, U10	Two Gigabit Ethernet ports • Ethernet A (Bottom) • Ethernet B (Top)	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 x 2 PHY and the FPGA-based Triple Speed Ethernet Intel FPGA IP function in RGMII mode.
J4, J5	Two Diligent Pmod* connectors	12-pin interface with 8 I/O signal pins used to connect low frequency, low I/O peripheral modules.
J11	Mini-USB 2.0 UART port	USB connector with USB-to-UART bridge for serial UART interface
J12	Mini-USB port	Embedded Intel FPGA Download Cable II.

continued...

Board Reference	Type	Description
Analog		
J18, J19	SMA inputs	Two FPGA analog-to-digital converter (ADC).
J20	Header	2x10 ADC.
POT1	Potentiometer	Input to ADC.
J1	SMA output	External 16 bit digital-to-analog converter (DAC) device.
Video and Display Ports		
U8	HDMI video output	19-pin HDMI connector which provides a HDMI v1.4 video output of up to 1080p through an ADI (Analog Devices, Inc) PHY.
Power Supply		
J15	DC input jack	Accepts 12 V DC power supply.
SW3	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

A.2. Featured Device

The MAX 10 FPGA development board features the MAX 10 10M50DAF484I6G device (U1) in a 484-pin FineLine BGA package.

Table 15.   MAX 10 FPGA 10M50DAF484I6G Features

ALMs	Equivalent LEs	M9K Memory (Kb)	Total RAM (Kb)	18-bit x 18-bit Multipliers	PLLs	Transceivers	Package Type
50,000	50	1,638	736	144	4	—	FineLine BGA 484 pins

A.3. Configuration

The MAX 10 FPGA Development Kit supports two configuration methods:

- Configuration by downloading a `.sof` file to the FPGA. Any power cycling of the FPGA or reconfiguration powers up the FPGA to a blank state.

- Programming of the on-die FPGA Configuration Flash Memory (CFM) via a `.pof` file. Any power cycling of the FPGA or reconfiguration powers up the FPGA in self-configuration mode, using the files stored in the CFM.

You can use two different Intel FPGA Download Cable hardware components to program the `.sof` or `.pof` files:

- Embedded Intel FPGA Download Cable II, type-B connector (J12).

- JTAG header (J14). Use an external Intel FPGA Download Cable, Intel FPGA Download Cable II, or Intel FPGA Ethernet Cable. The external download cable connects to the board through the JTAG header (J14).

A.3.1. Using the Quartus Prime Programmer

You can use the Quartus Prime Programmer to configure the FPGA with a `.sof`.

Before configuring the FPGA:

- Ensure that the Quartus Prime Programmer and the Intel FPGA Download Cable driver are installed on the host computer.

- The USB cable is connected to the kit.

- Power to the board is on, and no other applications that use the JTAG chain are running.

To configure the MAX 10 FPGA:

1. Start the Quartus Prime Programmer.

2. Click **Add File** and select the path to the desired `.sof`.

3. Turn on the **Program/Configure** option for the added file.

4. Click **Start** to download the selected file to the FPGA. The configuration is complete when the progress bar reaches 100%.

The Quartus Prime Convert Programming File (CPF) GUI can be used to generate a `.sof` file that can use for internal configuration. You can directly program the flash of the MAX 10 device, which included Configuration Flash Memory (CFM) and User Flash Memory (UFM), by using a download cable with the Quartus Prime software programmer.

A.3.2. Selecting the Internal Configuration Scheme

For all MAX 10 devices, except 10M02 device, there are total of 5 different modes you can select internal configuration.

The internal configuration scheme needs to be selected before design compilation.

To select the configuration mode:

1. Open the Quartus Prime software and load a project using MAX 10 device family.

2. On the **Assignments** menu, click **Device**. The **Device** dialog box appears.

3. In the **Device** dialog box, click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.

4. In the **Device and Pin Options** dialog box, select **Configuration** from the category pane.

5. In the Options list, do the following:.

   a. In the **Configuration scheme** list, select **Internal Configuration**

   b. In the **Configuration mode** list, select 1 out of 5 configuration modes. For the dual-boot feature:

- Must have a Dual Boot IP core in the design, for example, in a Platform Designer (Standard) component.

- Choose **Dual Compressed Images (512 Kbits UFM)** for the **Configuration Mode**.

- Generate two `.sof` files above and convert them into one POF file for CFM programming.

6. Turn on **Generate compressed bitstreams**, if needed.

7. Click **OK**.

A.3.3. Switch and Jumper Settings

This section is for the MAX 10 FPGA Development Kit. This section shows you how to restore the default factory settings and explains their functions.

The jumper (J7) connects the output of potentiometer (POT1.2) to ADC1_CH6. When the jumper (J7) is on, you can use the potentiometer to provide adjustable voltage (0–2.5 V) to the MAX 10 ADC through ADC1_CH6. When the jumper (J7) is off, ADC1_CH6 is connected to the 2x10 header as the other ADC channels.

Figure 20.   Jumper J7 on the Top of the Board (Detail)
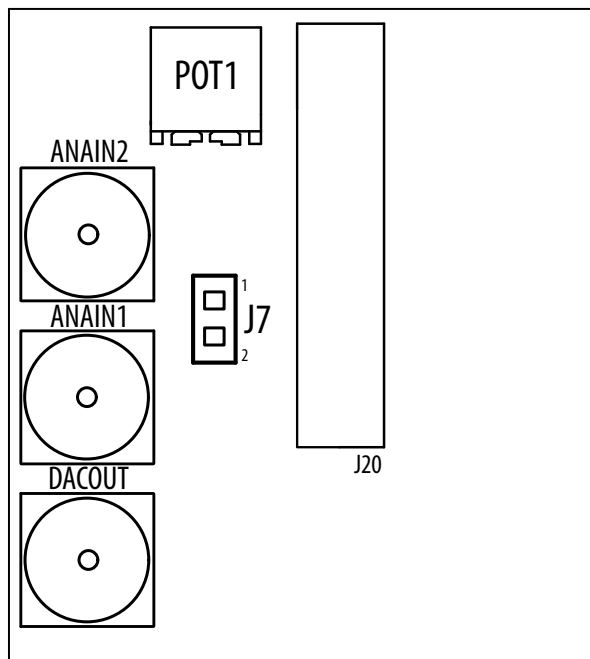
There are two switches (SW1 and SW2) on the bottom of the board. SW1 is for user functions, and SW2 allows for booting selection and bypassing some components.

Figure 21. Switches on the Bottom Board (Detail)

When a switch is ON, it means the FUNCTION SIGNAL is connected to GND. So it is a LOGIC LOW (0). When switch is OFF, it means the FUNCTION SIGNAL is disconnected from GND. So it is a LOGIC HIGH (1).

Note: The following figure shows the switch labels for the Rev. C board and a note for the Rev. B board. The change of name for SW2.3 is just a name change, not a functional change. Rev. B is labeled MAX10_BYPASS, but it is actually a VTAP bypass.

SW2	FUNCTION
1	USER_DIPSW4
2	CONFIG_SEL
3	VTAP_BYPASSN
4	HSMC_BYPASSN

For Rev. B:
2 = BOOT_SEL
3 = MAX10_BYPASSN

SW1	FUNCTION
1	USER_DIPSW0
2	USER_DIPSW1
3	USER_DIPSW2
4	USER_DIPSW3

4 3 2 1

OFF = 1

SW2

ON = 0

1 2 3 4

ON = 0

SW1

OFF = 1
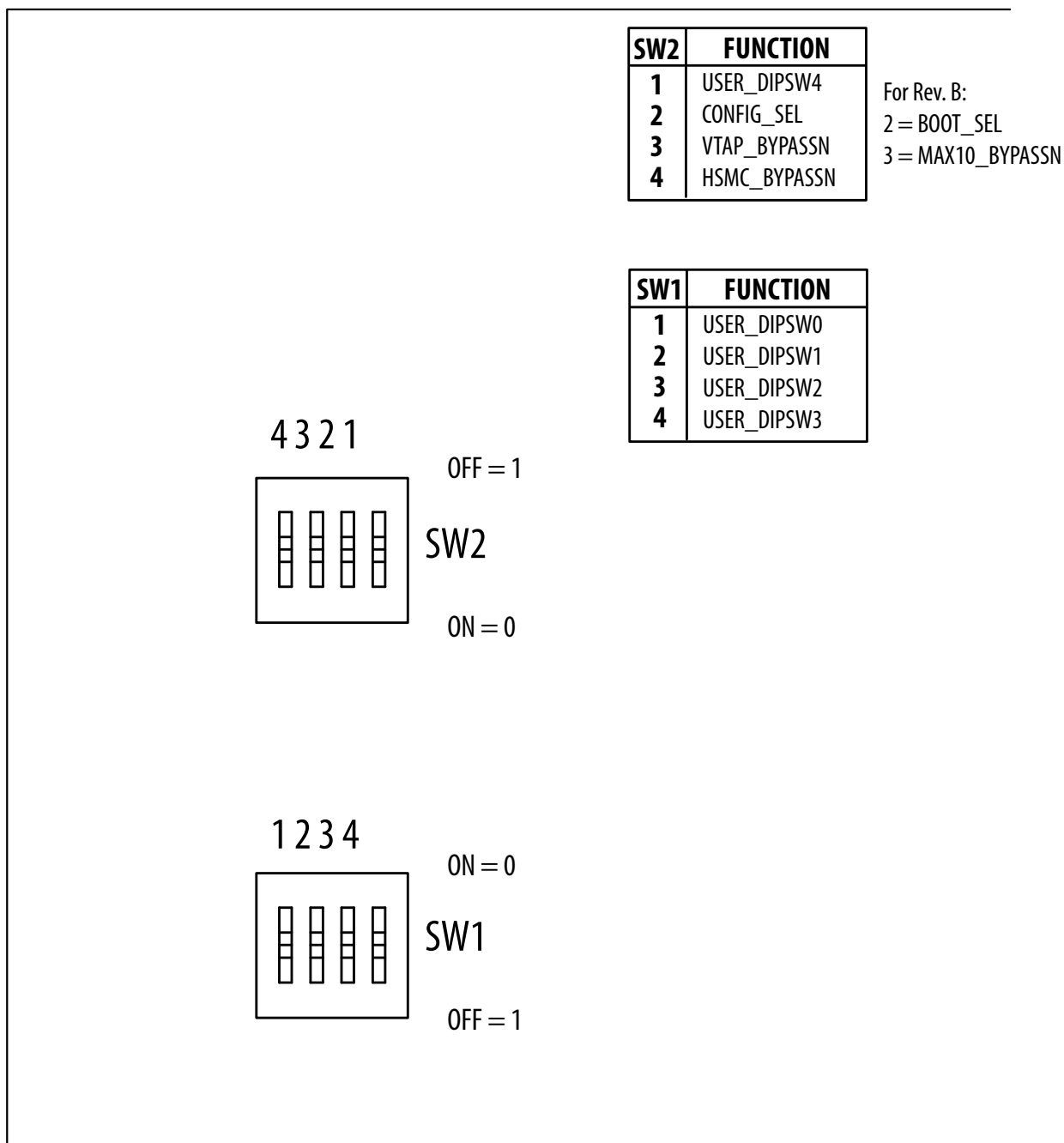
Table 16.   SW2 DIP Switch Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	USER_DIPSW4	User defined switch #4, #0/1/2/3 is on SW1. No default function.	—
2	BOOT_SEL (for Rev. B Board) CONFIG_SEL (for Rev. C board)	Use this pin to choose CFM0, CFM1 or CFM2 image as the first boot image in dual-image configuration. If the CONFIG_SEL is set to low, the first boot image is CFM0 image. If the CONFIG_SEL pin is set to high, the first boot image is CFM1 or CFM2 image. This pin is read before user mode and before the nSTATUS pin is asserted.	LOW
3	VTAP_BYPASSN	A virtual JTAG device is provided within the On-Board Intel FPGA Download Cable II, it provides access to diagnostic hardware and board identification information. The device shows up as an extra device on the JTAG chain with ID: 020D10DD. This switch removes the virtual JTAG device from the JTAG chain.	HIGH
4	HSMC_BYPASSN	Use this pin to bypass HSMC from JTAG chain. The default value of this signal is high so HSMC is in the JTAG chain. (However, there is no daughter cards connected to HSMC normally so it would not be detected by JTAG master). When it is set to low, HSMC is bypassed.	HIGH

A.4. Status Elements

This topic lists the non-user status elements for the MAX 10 FPGA development board.

Table 17.   General LED Signal Names

Board Reference	Signal Name	Description
D1	—	Blue Power LED
D2	HSMC_PRSNTn	Green LED
D13	UART_TXLED	Green LED for USB to UART
D14	UART_RXLED	Green LED for USB to UART

Table 18.   MAX II CPLD LED Signal Names

Board Reference	Signal Name	I/O Standard	MAX II CPLD Pin Number
D20	MAXII_CONF_DONE	3.3 V	W17
D21	3.3V_LED	3.3 V	U4
D22	2.5V_LED	3.3 V	U5
D23	1.2V_LED	3.3 V	U6

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A.5. Setup Elements

Table 19.   Board Settings DIP Switch and Jumper Schematic Signals

Board Reference	Signal Name	Device/Pin Number	I/O Standard
SW2.1	USER_DIPSW4	MAX 10 / H21	1.5 V
SW2.2	CONFIG_SEL	MAX 10 / H10	3.3 V
SW2.3	VTAP_BYPASSN	MAX II / P17	3.3 V
SW2.4	HSMC_BYPASSn	MAX II / P18	3.3 V
J7.1	—	POT1	2.5 V
J7.2	ADC1_CH6	2x10 Header / J20.15	2.5 V

Table 20.   General Push Button Signal Names

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
S5	PULSE_NCONFIG	H9	3.3 V
S6	CPU_RESETn	D9	3.3 V

A.6. General User Input/Output

User-defined I/O signal names, FPGA pin numbers, and I/O standards for the MAX 10 FPGA development board.

Table 21.   User-Defined Push Button Signal Names

Board Reference	Signal Name	MAX 10 FPGA Pin Number	I/O Standard
S1	USER_PB0	L22	1.5 V
S2	USER_PB1	M21	1.5 V
S3	USER_PB2	M22	1.5 V
S4	USER_PB3	N21	1.5 V

Table 22.   User-Defined DIP Switch Schematic Signal Names

Board Reference	Signal Name	MAX 10 Pin Number	I/O Standard
SW1.1	USER_DIPSW0	H21	1.5 V
SW1.2	USER_DIPSW1	H22	1.5 V
SW1.3	USER_DIPSW2	J21	1.5 V
SW1.4	USER_DIPSW3	J22	1.5 V
SW2.1	USER_DIPSW4	G19	1.5 V

Table 23.   User LED (Green) Schematic Signal Names

Board Reference	Signal Name	MAX 10 Pin Number	I/O Standard
D15	USER_LED0	T20	1.5 V
D16	USER_LED1	U22	1.5 V
D17	USER_LED2	U21	1.5 V
D18	USER_LED3	AA21	1.5 V
D19	USER_LED4	AA22	1.5 V

For a MAX 10 FPGA Development Kit baseline pinout design, visit the FPGA Design Store.

Related Information

FPGA Design Store

A.7. Clock Circuitry

The development board includes a four channel programmable oscillator with a default frequency of 25 MHz, 50 MHz, 100 MHz, and 125 MHz. The board also includes a 10 MHz programmable oscillator connected to the ADC.

A.7.1. On-Board Oscillators

Figure 22.   MAX 10 FPGA Development Board Clocks
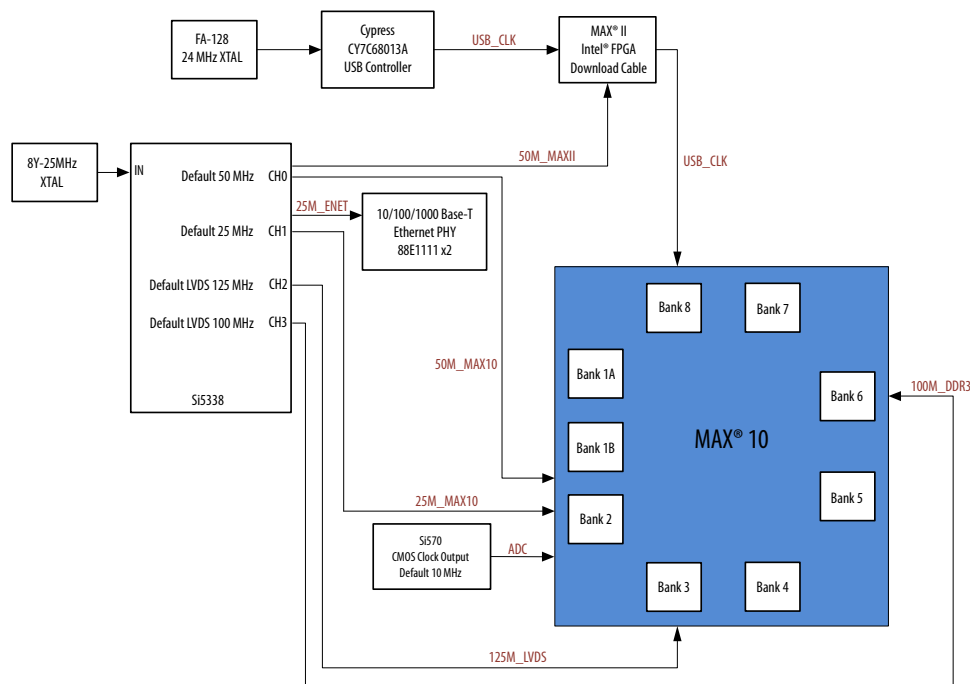
Table 24.   On-Board Oscillators

Source	Schematic Signal Name	Frequency (MHz)	I/O Standard	MAX 10 FPGA Pin Number	Application
X1	CLK_10_ADC	10.000	2.5 V CMOS	N5	Programmable default 10 MHz clock for ADC
U2	CLK_25_ENET	25.000	2.5 V CMOS	—	Ethernet clock
U2	CLK_25_MAX10	25.000	2.5 V CMOS	M8	MAX 10 clock
U2	CLK_50_MAXII	25.000	2.5 V/3.3V CMOS	—	Clock for On-Board Intel FPGA Download Cable II
U2	CLK_50_MAX10	50.000	2.5 V CMOS	M9	MAX 10 clock
U2	CLK_DDR3_100_N	100.000	Differential SSTL-15	N15	DDR3 clocks
					continued...

Source	Schematic Signal Name	Frequency (MHz)	I/O Standard	MAX 10 FPGA Pin Number	Application
U2	`CLK_DDR3_100_P`	100.000	Differential SSTL-15	N14	DDR3 clocks
U2	`CLK_LVDS_125_N`	125.000	2.5 V LVDS	R11	LVDS clocks
U2	`CLK_LVDS_125_P`	125.000	2.5 V LVDS	P11	LVDS clocks

Note: For signal CLK_50_MAXII, the output side voltage is 2.5 V and the input side voltage is 3.3 V. However, they are compatible electrically.

Note: For signals `CLK_DDR3_100_P` and `CLK_DDR3_100_N`, at the MAX 10 input side, Differential SSTL-15 is used as I/O standard because this bank's VCCIO is 1.5 V.

A.7.2. Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 25.   Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
HSMC	`HSMC_CLK_IN_N1`	2.5 V	AB21	LVDS input from the installed HSMC cable or board.
HSMC	`HSMC_CLK_IN_P1`	2.5 V	AA20	LVDS input from the installed HSMC cable or board.
HSMC	`HSMC_CLK_IN_N2`	2.5 V	V9	LVDS input from the installed HSMC cable or board.
HSMC	`HSMC_CLK_IN_P2`	2.5 V	V10	LVDS input from the installed HSMC cable or board.
HSMC	`HSMC_CLK_IN0`	2.5 V	N4	Single-ended input from the installed HSMC cable or board.

Table 26.   Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
HSMC	`HSMC_CLK_OUT_N1`	2.5 V	R13	LVDS output
HSMC	`HSMC_CLK_OUT_P1`	2.5 V	P13	LVDS output
HSMC	`HSMC_CLK_OUT_N2`	2.5 V	V14	LVDS output
HSMC	`HSMC_CLK_OUT_P2`	2.5 V	W15	LVDS output
HSMC	`HSMC_CLK_OUT0`	2.5 V	AA13	FPGA CMOS output (or GPIO)

A.8. Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the MAX 10 FPGA device.

A.8.1. 10/100/1000 Ethernet PHY

The MAX 10 FPGA Development Kit supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Triple-Speed Ethernet Intel FPGA IP MAC function.

Table 27.   Ethernet PHY A Pin Assignments, Signal Names, and Functions

Board Reference (U9)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U9.8	ENETA_GTX_CLK	2.5V CMOS	T5	125 MHz RGMII TX clock
U9.4	ENETA_TX_CLK	3.3V LVCMOS	E10	25/2.5 MHz MII TX clock
U9.11	ENETA_TX_D0	2.5V CMOS	R5	RGMII TX data 0
U9.12	ENETA_TX_D1	2.5V CMOS	P5	RGMII TX data 1
U9.14	ENETA_TX_D2	2.5V CMOS	W1	RGMII TX data 2
U9.16	ENETA_TX_D3	2.5V CMOS	W2	RGMII TX data 3
U9.9	ENETA_TX_EN	2.5V CMOS	R4	RGMII TX enable
U9.7	ENETA_TX_ER	2.5V CMOS	P4	MII TX error
U9.2	ENETA_RX_CLK	2.5V CMOS	P3	RGMII RX clock
U9.95	ENETA_RX_D0	2.5V CMOS	N9	RGMII RX data 0
U9.92	ENETA_RX_D1	2.5V CMOS	T1	RGMII RX data 1
U9.93	ENETA_RX_D2	2.5V CMOS	N1	RGMII RX data 2
U9.91	ENETA_RX_D3	2.5V CMOS	T3	RGMII RX data 3
U9.94	ENETA_RX_DV	2.5V CMOS	T2	RGMII RX valid
U9.3	ENETA_RX_ER	2.5V CMOS	U2	MII RX error
U9.28	ENETA_RESETN	2.5V CMOS	V8	Device reset
U9.23	ENETA_INTn	2.5V CMOS	V7	Management bus interrupt
U9.25	ENET_MDC	2.5V CMOS	Y6	MDI clock
U9.24	ENET_MDIO	2.5V CMOS	Y5	MDI data
U9.84	ENETA_RX_CRS	2.5V CMOS	N8	MII Carrier Sense
U9.83	ENETA_RX_COL	2.5V CMOS	P1	MII Collision
U9.55	CLK_25_ENET	2.5V CMOS	—	25 MHz Reference clock
U9.70	ENETA_LED_DUPLEX	2.5 V CMOS	—	Duplex or collision LED
U9.76	ENETA_LED_LINK10	2.5 V CMOS	—	10 Mb link LED
U9.74	ENETA_LED_LINK100	2.5V CMOS	R9	100 Mb link LED
U9.73	ENETA_LED_LINK1000	2.5V CMOS	—	1000 Mb link LED

continued...

Board Reference (U9)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U9.58, 69	ENETA_LED_RX	2.5V CMOS	—	RX data active LED
U9.61, 68	ENETA_LED_TX	2.5V CMOS	—	TX data active LED
U9.29	ENETA_MDI_P0	2.5V CMOS	—	MDI
U9.31	ENETA_MDI_N0	2.5V CMOS	—	MDI
U9.33	ENETA_MDI_P1	2.5V CMOS	—	MDI
U9.34	ENETA_MDI_N1	2.5V CMOS	—	MDI
U9.39	ENETA_MDI_P2	2.5V CMOS	—	MDI
U9.41	ENETA_MDI_N2	2.5V CMOS	—	MDI
U9.42	ENETA_MDI_P3	2.5V CMOS	—	MDI
U9.43	ENETA_MDI_N3	2.5V CMOS	—	MDI

Table 28.   Ethernet PHY B Pin Assignments, Signal Names and Functions

Board Reference (U10)	Schematic Signal Name	I/O Standard	Max 10 FPGA Pin Number	Description
U10.8	ENETB_GTX_CLK	2.5V CMOS	T6	125 MHz RGMII TX clock
U10.4	ENETB_TX_CLK	3.3V LVCMOS	E11	25/2.5 MHz MII TX clock
U10.11	ENETB_TX_D0	2.5V CMOS	U1	RGMII TX data 0
U10.12	ENETB_TX_D1	2.5V CMOS	V1	RGMII TX data 1
U10.14	ENETB_TX_D2	2.5V CMOS	U3	RGMII TX data 2
U10.16	ENETB_TX_D3	2.5V CMOS	U4	RGMII TX data 3
U10.9	ENETB_TX_EN	2.5V CMOS	V3	RGMII TX enable
U10.7	ENETB_TX_ER	2.5V CMOS	U5	MII TX error
U10.2	ENETB_RX_CLK	2.5V CMOS	R3	RGMII RX clock
U10.95	ENETB_RX_D0	2.5V CMOS	P8	RGMII RX data 0
U10.92	ENETB_RX_D1	2.5V CMOS	M1	RGMII RX data 1
U10.93	ENETB_RX_D2	2.5V CMOS	M2	RGMII RX data 2
U10.91	ENETB_RX_D3	2.5V CMOS	R7	RGMII RX data 3
U10.94	ENETB_RX_DV	2.5V CMOS	R1	RGMII RX valid
U10.3	ENETB_RX_ER	2.5V CMOS	R2	MII RX error
U10.28	ENETB_RESETn	2.5V CMOS	AB4	Device reset
U10.23	ENETB_INTn	2.5V CMOS	AA3	Management bus interrupt
U10.25	ENET_MDC	2.5V CMOS	Y6	MDI clock
U10.24	ENET_MDIO	2.5V CMOS	Y5	MDI data
U10.84	ENETB_RX_CRS	2.5V CMOS	N3	MII Carrier Sense

continued...

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Board Reference (U10)	Schematic Signal Name	I/O Standard	Max 10 FPGA Pin Number	Description
U10.83	ENETB_RX_COL	2.5V CMOS	N2	MII Collision
U10.55	CLK_25_ENET	2.5V CMOS	—	25 MHz Reference clock
U10.70	ENETB_LED_DUPLEX	2.5V CMOS	—	Duplex or collision LED
U10.76	ENETB_LED_LINK10	2.5V CMOS	—	10 Mb link LED
U10.74	ENETB_LED_LINK100	2.5V CMOS	P9	100 Mb link LED
U10.73	ENETB_LED_LINK1000	2.5V CMOS	—	1000 Mb link LED
U10.58, 69	ENETB_LED_RX	2.5V CMOS	—	RX data active LED
U10.61, 65, 68	ENETB_LED_TX	2.5V CMOS	—	TX data active LED
U10.29	ENETB_MDI_P0	2.5V CMOS	—	MDI
U10.31	ENETB_MDI_N0	2.5V CMOS	—	MDI
U10.33	ENETB_MDI_P1	2.5V CMOS	—	MDI
U10.34	ENETB_MDI_N1	2.5V CMOS	—	MDI
U10.39	ENETB_MDI_P2	2.5V CMOS	—	MDI
U10.41	ENETB_MDI_N2	2.5V CMOS	—	MDI
U10.42	ENETB_MDI_P3	2.5V CMOS	—	MDI
U10.43	ENETB_MDI_N3	2.5V CMOS	—	MDI

A.8.2. Digital-to-Analog Converter

The MAX 10 FPGA comes with one external 16 bit digital-to-analog converter (DAC) device with an SMA output.

The MAX 10 FPGA has two 12-bit successive approximation register (SAR) ADCs with sample rate of 1 MSps. One potentiometer is connected to ADC1_CH6 to function as a user-controlled DC, and it is connected to 2.5 V. To ensure performance evaluation of the ADCs, the MAX 10 FPGA Development Kit has separate analog supply and split partition for analog ground. An external 16-bit single channel DAC is connected to Bank 7 to enable closed loop evaluation. The DAC uses a 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with standard serial peripheral interface (SPI), quad SPI, Microwire, and digital signal processor (DSP) interfaces.

Table 29.   Digital-to-Analog Converter Signals

Board Reference (U33)	Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U33.5	DAC_SYNC	3.3 V	U1.B10	Level-triggered control input (active LOW). Frame synchronization signal for the input data.
U33.6	DAC_SCLK	3.3 V	A7	Serial clock input
U33.7	DAC_DIN	3.3 V	A8	Serial data input

A.8.3. HDMI Video Output

The MAX 10 FPGA Development Kit supports one HDMI transmitter and one HDMI receptacle.

The transmitter incorporates HDMI v1.4 features, and is capable of supporting an input data rate up to 165 MHz (1080p at 60 Hz, UXGA at 60 Hz). The connection between HDMI transmitter and MAX 10 is established in Bank 7, and the communication can be done via I^{2}C interface.

Table 30.   HDMI Pin Assignments, Signal Names and Functions

Board Reference (U8)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U8.62	HDMI_TX_D0	3.3 V	A17	HDMI digital video data bus
U8.61	HDMI_TX_D1	3.3 V	A18	HDMI digital video data bus
U8.60	HDMI_TX_D2	3.3 V	A12	HDMI digital video data bus
U8.59	HDMI_TX_D3	3.3 V	F16	HDMI digital video data bus
U8.58	HDMI_TX_D4	3.3 V	A16	HDMI digital video data bus
U8.57	HDMI_TX_D5	3.3 V	B12	HDMI digital video data bus
U8.56	HDMI_TX_D6	3.3 V	F15	HDMI digital video data bus
U8.55	HDMI_TX_D7	3.3 V	B11	HDMI digital video data bus
U8.54	HDMI_TX_D8	3.3 V	A13	HDMI digital video data bus
U8.52	HDMI_TX_D9	3.3 V	C15	HDMI digital video data bus
U8.50	HDMI_TX_D10	3.3 V	C11	HDMI digital video data bus
U8.49	HDMI_TX_D11	3.3 V	A11	HDMI digital video data bus
U8.48	HDMI_TX_D12	3.3 V	A20	HDMI digital video data bus
U8.47	HDMI_TX_D13	3.3 V	H13	HDMI digital video data bus
U8.46	HDMI_TX_D14	3.3 V	E14	HDMI digital video data bus
U8.45	HDMI_TX_D15	3.3 V	D12	HDMI digital video data bus
U8.44	HDMI_TX_D16	3.3 V	C12	HDMI digital video data bus
U8.43	HDMI_TX_D17	3.3 V	C19	HDMI digital video data bus
U8.42	HDMI_TX_D18	3.3 V	C18	HDMI digital video data bus
U8.41	HDMI_TX_D19	3.3 V	B19	HDMI digital video data bus
U8.40	HDMI_TX_D20	3.3 V	B17	HDMI digital video data bus
U8.39	HDMI_TX_D21	3.3 V	B16	HDMI digital video data bus
U8.38	HDMI_TX_D22	3.3 V	C16	HDMI digital video data bus
U8.37	HDMI_TX_D23	3.3 V	A15	HDMI digital video data bus
U8.53	HDMI_TX_CLK	3.3 V	D6	Video clock
U8.63	HDMI_TX_DE	3.3 V	C10	Video data enable

continued...

Board Reference (U8)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U8.64	HDMI_TX_HS	3.3 V	A19	Vertical Synchronization
U8.2	HDMI_TX_VS	3.3 V	J12	Horizontal Synchronization
U8.28	HDMI_TX_INT	3.3 V	D15	Interrupt Signal
U8.35	HDMI_SCL	3.3 V	A10	HDMI I2C clock
U8.36	HDMI_SDAX	3.3 V	B15	HDMI I2C data

A.8.4. HSMC

The high-speed mezzanine card (HSMC) interface is based on the Samtec 0.5 mm pitch, surface-mount QTH/QSH family of connectors. It is designed to support a full SPI-4.2 interface (17 LVDS channels) and 3 input and output clocks as well as SMBus and JTAG signals.

Since MAX 10 does not have transceiver channels, the HSMC clock-data-recovery channels are left unconnected.

The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5 V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

Table 31.   HSMC Schematic Signals

Board Reference (J2)	Schematic Signal Name	I/O Standard	MAX 10/MAX II Pin Number	Description
33	HSMC_SDA	2.5 V CMOS inout	AA19	Management serial data line
34	HSMC_SCL	2.5 V CMOS out	Y18	Management serial clock line
35	HSMC_JTAG_TCK	Part of chain	A9 (MAX II)	JTAG clock
36	HSMC_JTAG_TMS	Part of chain	A8 (MAX II)	JTAG mode select
37	HSMC_JTAG_TDO	Part of chain	A7 (MAX II)	JTAG data out
38	HSMC_JTAG_TDI	Part of chain	A6 (MAX II)	JTAG data in
39	HSMC_CLK_OUT0	2.5 V CMOS clock output	AA13	clock output 0
40	HSMC_CLK_IN0	2.5 V CMOS clock in	N4	Clock input 0
41	HSMC_D0	2.5 V CMOS inout	Y7	Data bus
42	HSMC_D1	2.5 V CMOS inout	Y8	Data bus
				continued...

Board Reference (J2)	Schematic Signal Name	I/O Standard	MAX 10/MAX II Pin Number	Description
43	HSMC_D2	2.5 V CMOS inout	AB2	Data bus
44	HSMC_D3	2.5 V CMOS inout	AB3	Data bus
47	HSMC_TX_D_P0	2.5 V CMOS inout or LVDS TX channels-p	W3	Data bus
48	HSMC_RX_D_P0	2.5 V CMOS inout or LVDS RX channels-p	V5	Data bus
49	HSMC_TX_D_N0	2.5 V CMOS inout or LVDS TX channels-n	W4	Data bus
50	HSMC_RX_D_N0[1]	2.5 V CMOS inout or LVDS RX channels-n	V4	Data bus
53	HSMC_TX_D_P1	2.5 V CMOS inout or LVDS TX channels-p	U7	Data bus
54	HSMC_RX_D_P1[1]	2.5 V CMOS inout or LVDS RX channels-p	Y2	Data bus
55	HSMC_TX_D_N1	2.5 V CMOS inout or LVDS TX channels-n	U6	Data bus
56	HSMC_RX_D_N1[1]	2.5 V CMOS inout or LVDS RX channels-n	Y1	Data bus
59	HSMC_TX_D_P2	2.5 V CMOS inout or LVDS TX channels-p	W6	Data bus
60	HSMC_RX_D_P2[1]	2.5 V CMOS inout or LVDS RX channels-p	AA20	Data bus
61	HSMC_TX_D_N2	2.5 V CMOS inout or LVDS TX channels-n	W5	Data bus
62	HSMC_RX_D_N2[1]	2.5 V CMOS inout or LVDS RX channels-n	AA1	Data bus
65	HSMC_TX_D_P3	2.5 V CMOS inout or LVDS TX channels-p	W8	Data bus
66	HSMC_RX_D_P3[1]	2.5 V CMOS inout or LVDS RX channels-p	AB8	Data bus
67	HSMC_TX_D_N3	2.5 V CMOS inout or LVDS TX channels-n	W7	Data bus
68	HSMC_RX_D_N3[1]	2.5 V CMOS inout or LVDS RX channels-n	AA8	Data bus
71	HSMC_TX_D_P4	2.5 V CMOS inout or LVDS TX channels-p	AA10	Data bus
72	HSMC_RX_D_P4[1]	2.5 V CMOS inout or LVDS RX channels-p	AB9	Data bus
73	HSMC_TX_D_N4	2.5 V CMOS inout or LVDS TX channels-n	Y10	Data bus
74	HSMC_RX_D_N4[1]	2.5 V CMOS inout or LVDS RX channels-n	AA9	Data bus
				continued...

[1] MAX 10 does not have internal termination for LVDS RX. Install a 100 ohm resistor to support LVDS RX on HSMC.

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Board Reference (J2)	Schematic Signal Name	I/O Standard	MAX 10/MAX II Pin Number	Description
77	HSMC_TX_D_P5	2.5 V CMOS inout or LVDS TX channels-p	AA7	Data bus
78	HSMC_RX_D_P5[1]	2.5 V CMOS inout or LVDS RX channels-p	AB7	Data bus
79	HSMC_TX_D_N5	2.5 V CMOS inout or LVDS TX channels-n	AA6	Data bus
80	HSMC_RX_D_N5[1]	2.5 V CMOS inout or LVDS RX channels-n	AB6	Data bus
83	HSMC_TX_D_P6	2.5 V CMOS inout or LVDS TX channels-p	P10	Data bus
84	HSMC_RX_D_P6[1]	2.5 V CMOS inout or LVDS RX channels-p	Y4	Data bus
85	HSMC_TX_D_N6	2.5 V CMOS inout or LVDS TX channels-n	R10	Data bus
86	HSMC_RX_D_N6[1]	2.5 V CMOS inout or LVDS RX channels-n	Y3	Data bus
89	HSMC_TX_D_P7	2.5 V CMOS inout or LVDS TX channels-p	W10	Data bus
90	HSMC_RX_D_P7[1]	2.5 V CMOS inout or LVDS RX channels-p	AB5	Data bus
91	HSMC_TX_D_N7	2.5 V CMOS inout or LVDS TX channels-n	W9	Data bus
92	HSMC_RX_D_N7[1]	2.5 V CMOS inout or LVDS RX channels-n	AA5	Data bus
95	HSMC_CLK_OUT_P1	2.5 V CMOS inout or LVDS clock out	P13	Clock output 1
96	HSMC_CLK_IN_P1	2.5 V CMOS inout or LVDS clock in	AA20	Clock input 1
97	HSMC_CLK_OUT_N1	2.5 V CMOS inout or LVDS clock out	R13	Clock output 1
98	HSMC_CLK_IN_N1	2.5 V CMOS inout or LVDS clock in	AB21	Clock input 1
101	HSMC_TX_D_P8	2.5 V CMOS inout or LVDS TX channels-p	W14	Data bus
102	HSMC_RX_D_P8[1]	2.5 V CMOS inout or LVDS RX channels-p	W13	Data bus
103	HSMC_TX_D_N8	2.5 V CMOS inout or LVDS TX channels-n	V13	Data bus
104	HSMC_RX_D_N8[1]	2.5 V CMOS inout or LVDS RX channels-n	W12	Data bus
107	HSMC_TX_D_P9	2.5 V CMOS inout or LVDS TX channels-p	Y14	Data bus
108	HSMC_RX_D_P9[1]	2.5 V CMOS inout or LVDS RX channels-p	AB15	Data bus
109	HSMC_TX_D_N9	2.5 V CMOS inout or LVDS TX channels-n	Y13	Data bus

continued...

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Board Reference (J2)	Schematic Signal Name	I/O Standard	MAX 10/MAX II Pin Number	Description
110	HSMC_RX_D_N9[1]	2.5 V CMOS inout or LVDS RX channels-n	AA14	Data bus
113	HSMC_TX_D_P10	2.5 V CMOS inout or LVDS TX channels-p	V16	Data bus
114	HSMC_RX_D_P10[1]	2.5 V CMOS inout or LVDS RX channels-p	Y16	Data bus
115	HSMC_TX_D_N10	2.5 V CMOS inout or LVDS TX channels-n	U15	Data bus
116	HSMC_RX_D_N10[1]	2.5 V CMOS inout or LVDS RX channels-n	AA15	Data bus
119	HSMC_TX_D_P11	2.5 V CMOS inout or LVDS TX channels-p	W16	Data bus
120	HSMC_RX_D_P11[1]	2.5 V CMOS inout or LVDS RX channels-p	AA16	Data bus
121	HSMC_TX_D_N11	2.5 V CMOS inout or LVDS TX channels-n	V15	Data bus
122	HSMC_RX_D_N11[1]	2.5 V CMOS inout or LVDS RX channels-n	AB16	Data bus
125	HSMC_TX_D_P12	2.5 V CMOS inout or LVDS TX channels-p	V17	Data bus
126	HSMC_RX_D_P12[1]	2.5 V CMOS inout or LVDS RX channels-p	AB18	Data bus
127	HSMC_TX_D_N12	2.5 V CMOS inout or LVDS TX channels-n	W17	Data bus
128	HSMC_RX_D_N12[1]	2.5 V CMOS inout or LVDS RX channels-n	AB17	Data bus
131	HSMC_TX_D_P13	2.5 V CMOS inout or LVDS TX channels-p	V12	Data bus
132	HSMC_RX_D_P13[1]	2.5 V CMOS inout or LVDS RX channels-p	Y11	Data bus
133	HSMC_TX_D_N13	2.5 V CMOS inout or LVDS TX channels-n	V11	Data bus
134	HSMC_RX_D_N13[1]	2.5 V CMOS inout or LVDS RX channels-n	W11	Data bus
137	HSMC_TX_D_P14	2.5 V CMOS inout or LVDS TX channels-p	P12	Data bus
138	HSMC_RX_D_P14[1]	2.5 V CMOS inout or LVDS RX channels-p	AB11	Data bus
139	HSMC_TX_D_N14	2.5 V CMOS inout or LVDS TX channels-n	R12	Data bus
140	HSMC_RX_D_N14[1]	2.5 V CMOS inout or LVDS RX channels-n	AB10	Data bus
143	HSMC_TX_D_P15	2.5 V CMOS inout or LVDS TX channels-p	AA12	Data bus
144	HSMC_RX_D_P15[1]	2.5 V CMOS inout or LVDS RX channels-p	AB13	Data bus

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Board Reference (J2)	Schematic Signal Name	I/O Standard	MAX 10/MAX II Pin Number	Description
145	HSMC_TX_D_N15	2.5 V CMOS inout or LVDS TX channels-n	AA11	Data bus
146	HSMC_RX_D_N15[1]	2.5 V CMOS inout or LVDS RX channels-n	AB12	Data bus
149	HSMC_TX_D_P16	2.5 V CMOS inout or LVDS TX channels-p	Y17	Data bus
150	HSMC_RX_D_P16[1]	2.5 V CMOS inout or LVDS RX channels-p	AB20	Data bus
151	HSMC_TX_D_N16	2.5 V CMOS inout or LVDS TX channels-n	AA17	Data bus
152	HSMC_RX_D_N16[1]	2.5 V CMOS inout or LVDS RX channels-n	AB19	Data bus
155	HSMC_CLK_OUT_P2	2.5 V CMOS inout or LVDS clock out	W15	Clock output 2
156	HSMC_CLK_IN_P2	2.5 V CMOS inout or LVDS clock in	V10	Clock input 2
157	HSMC_CLK_OUT_N2	2.5 V CMOS inout or LVDS clock out	V14	Clock output 2
158	HSMC_CLK_IN_N2	2.5 V CMOS inout or LVDS clock in	V9	Clock input 2
160	HSMC_PRSNTn	2.5 V	AB14	Present

Related Information

High Speed Mezzanine Card (HSMC) Specification

A.8.5. Pmod Connectors

The MAX 10 FPGA Development Kit features two Digilent Pmod* compatible headers, which are used to connect low frequency, low I/O pin count peripheral modules.

The 12-pin version Pmod connector used in this kit provides 8 I/O signal pins. The peripheral module interface also encompasses a variant using I^{2}C interface, and two or four wire MTE cables. The Pmod signals are connected to Bank 8.

Table 32. Pmod A Pin Assignments, Signal Names, and Functions

Schematic Signal Name	Schematic Share Bus Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
PMODA_D0	PMODA_IO0	3.3 V	C7	In/Out
PMODA_D1	PMODA_IO1	3.3 V	C8	In/Out
PMODA_D2	PMODA_IO2	3.3 V	A6	In/Out
PMODA_D3	PMODA_IO3	3.3 V	B7	In/Out
PMODA_D4	PMODA_IO4	3.3 V	D8	In/Out
PMODA_D5	PMODA_IO5	3.3 V	A4	In/Out
				continued...

Schematic Signal Name	Schematic Share Bus Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
PMODA_D6	PMODA_IO6	3.3 V	A5	In/Out
PMODA_D7	PMODA_IO7	3.3 V	E9	In/Out
—	VCC	3.3 V	—	Power
—	GND	—	—	Ground

Table 33.   Pmod B Pin Assignments, Signal Names, and Functions

Schematic Signal Name	Schematic Share Bus Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
PMODB_D0	PMODB_IO0	3.3 V	E8	In/Out
PMODB_D1	PMODB_IO1	3.3 V	D5	In/Out
PMODB_D2	PMODB_IO2	3.3 V	B5	In/Out
PMODB_D3	PMODB_IO3	3.3 V	C4	In/Out
PMODB_D4	PMODB_IO4	3.3 V	A2	In/Out
PMODB_D5	PMODB_IO5	3.3 V	A3	In/Out
PMODB_D6	PMODB_IO6	3.3 V	B4	In/Out
PMODB_D7	PMODB_IO7	3.3 V	B3	In/Out
—	VCC	3.3 V	—	Power
—	GND	—	—	Ground

A.8.6. USB to UART

The board uses a USB based UART bridge chip (FT232R) to bridge communication to a host for general software debug for Nios and non-Nios systems. This chip uses TXD and RXD for transmission and reception of data. A mini B plug receptacle is used to minimize board space. The related I/O utilization is implemented in Bank 4.

Table 34.   USB-UART Pin Assignments, Signal Names, and Functions

Board Reference (U11)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U11.2	UART_TX	2.5 V	W18	Transmit asynchronous data output
U11.30	UART_RX	2.5 V	Y19	Receive asynchronous data input

A.9. Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the FPGA.

A.9.1. DDR3 Rev. B Board

Note: For your board's revision, look for the board serial number on the back of the board at the bottom. Refer to the Components in MAX 10 FPGA Development Kit (Bottom View) figure for more information.

The MAX 10 FPGA provides full-speed support to a x16 DDR3 300-MHz interface by using a 1 Gbit x16 memory. Additionally, the MAX 10 supports the error correction code (ECC) feature.

Caution: The DDR3 address signals at F18, E19, F20, and F21 on Rev. B boards violate MAX 10 external memory guidelines when implementing DDR3 on the 10M50 F484 device. Altera recommends you follow the MAX 10 guidelines for your own board designs and utilize Quartus Prime software to verify pin location compliance. Contact Altera support if you received DDR3 pin location errors for your Rev. B kit designs.

Table 35.   DDR3 Pin Assignments, Signal Names, and Functions

Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U5.N3 - U6.K3	DDR3_A0	1.5 V SSTL	V20	Address bus
U5.P7 - U6.L7	DDR3_A1	1.5 V SSTL	F20	Address bus Refer to Caution statement above.
U5.P3 - U6.L3	DDR3_A2	1.5 V SSTL	F18	Address bus Refer to Caution statement above.
U5.N2 - U6.K2	DDR3_A3	1.5 V SSTL	U20	Address bus
U5.P8 - U6.L8	DDR3_A4	1.5 V SSTL	F21	Address bus Refer to Caution statement above.
U5.P2 - U6.L2	DDR3_A5	1.5 V SSTL	F19	Address bus
U5.R8 - U6.M8	DDR3_A6	1.5 V SSTL	E21	Address bus
U5.R2 -U6.M2	DDR3_A7	1.5 V SSTL	E19	Address bus Refer to Caution statement above.
U5.T8 - U6.N8	DDR3_A8	1.5 V SSTL	D22	Address bus
U5.R3 - U6.M3	DDR3_A9	1.5 V SSTL	E22	Address bus
U5.L7 - U6.H7	DDR3_A10	1.5 V SSTL	Y20	Address bus
U5.R7 - U6.M7	DDR3_A11	1.5 V SSTL	E20	Address bus
U5.N7 - U6.K7	DDR3_A12	1.5 V SSTL	J14	Address bus
U5.T3 - U6.N3	DDR3_A13	1.5 V SSTL	C22	Address bus
U5.M2 - U6.J2	DDR3_BA0	1.5 V SSTL	V22	Bank address bus
U5.N8 - U6.K8	DDR3_BA1	1.5 V SSTL	N18	Bank address bus

continued...

Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U5.M3 - U6.J3	DDR3_BA2	1.5 V SSTL	W22	Bank address bus
U5.K3 - U6.G3	DDR3_CASn	1.5 V SSTL	U19	Row address bus
U5.K9 - U6.G9	DDR3_CKE	1.5 V SSTL	W20	Clock enable
U5.J7 - U6.F7	DDR3_CLK_P	Differential 1.5 V SSTL	D18	Differential output clock
U5.K7 - U6.G7	DDR3_CLK_N	Differential 1.5 V SSTL	E18	Differential output clock
U5.L2 - U6.H2	DDR3_CSn	1.5 V SSTL	Y22	Chip select
U5.E7	DDR3_DM0	1.5 V SSTL	J15	Write mask byte lane 0
U5.D3	DDR3_DM1	1.5 V SSTL	N19	Write mask byte lane 1
U6.B7	DDR3_DM2	1.5 V SSTL	T18	Write mask byte lane 2
U5.E3	DDR3_DQ0	1.5 V SSTL	J18	Data bus byte lane 0
U5.F7	DDR3_DQ1	1.5 V SSTL	K20	Data bus byte lane 0
U5.F2	DDR3_DQ2	1.5 V SSTL	H18	Data bus byte lane 0
U5.F8	DDR3_DQ3	1.5 V SSTL	K18	Data bus byte lane 0
U5.H3	DDR3_DQ4	1.5 V SSTL	H19	Data bus byte lane 0
U5.H8	DDR3_DQ5	1.5 V SSTL	J20	Data bus byte lane 0
U5.G2	DDR3_DQ6	1.5 V SSTL	H20	Data bus byte lane 0
U5.H7	DDR3_DQ7	1.5 V SSTL	K19	Data bus byte lane 0
U5.D7	DDR3_DQ8	1.5 V SSTL	L20	Data bus byte lane 1
U5.C3	DDR3_DQ9	1.5 V SSTL	M18	Data bus byte lane 1
U5.C8	DDR3_DQ10	1.5 V SSTL	M20	Data bus byte lane 1
U5.C2	DDR3_DQ11	1.5 V SSTL	M14	Data bus byte lane 1
U5.A7	DDR3_DQ12	1.5 V SSTL	L18	Data bus byte lane 1
U5.A2	DDR3_DQ13	1.5 V SSTL	M15	Data bus byte lane 1
U5.B8	DDR3_DQ14	1.5 V SSTL	L19	Data bus byte lane 1
U5.A3	DDR3_DQ15	1.5 V SSTL	N20	Data bus byte lane 1
U6.B3	DDR3_DQ16	1.5 V SSTL	R14	Data bus byte lane 2
U6.C7	DDR3_DQ17	1.5 V SSTL	P19	Data bus byte lane 2
U6.C2	DDR3_DQ18	1.5 V SSTL	P14	Data bus byte lane 2
U6.C8	DDR3_DQ19	1.5 V SSTL	R20	Data bus byte lane 2
U6.E3	DDR3_DQ20	1.5 V SSTL	R15	Data bus byte lane 2
U6.E8	DDR3_DQ21	1.5 V SSTL	T19	Data bus byte lane 2
U6.D2	DDR3_DQ22	1.5 V SSTL	P15	Data bus byte lane 2

continued...

Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U6.E7	DDR3_DQ23	1.5 V SSTL	P20	Data bus byte lane 2
U5.F3	DDR3_DQS_P0	Differential 1.5 V SSTL	K14	Data strobe P byte lane 0
U5.G3	DDR3_DQS_N0	Differential 1.5 V SSTL	K15	Data strobe N byte lane 0
U5.C7	DDR3_DQS_P1	Differential 1.5 V SSTL	L14	Data strobe P byte lane 1
U5.B7	DDR3_DQS_N1	Differential 1.5 V SSTL	L15	Data strobe N byte lane 1
U6.C3	DDR3_DQS_P2	Differential 1.5 V SSTL	R18	Data strobe P byte lane 2
U6.D3	DDR3_DQS_N2	Differential 1.5 V SSTL	P18	Data strobe N byte lane 2
U5.K1 - U6.G1	DDR3_ODT	1.5 V SSTL	W19	On-die termination enable
U5.J3 - U6.F3	DDR3_RASn	1.5 V SSTL	V18	Row address select
U5.T2 - U6.N2	DDR3_RESETn	1.5 V SSTL	B22	Reset
U5.L3 - U6.H3	DDR3_WEn	1.5 V SSTL	Y21	Write enable
U5.L8	DDR3_ZQ1	1.5 V SSTL	—	ZQ impedance calibration
U6.H8	DDR3_ZQ2	1.5 V SSTL	—	ZQ impedance calibration

Related Information

Block Diagram on page 6

A.9.2. DDR3 Rev. C Board

Note: For your board's revision, look for the board serial number at the bottom of the board. Refer to the Components in MAX 10 FPGA Development Kit (Bottom View) figure for more information.

The MAX 10 FPGA provides full-speed support to a x16 DDR3 300 MHz interface by using a 1 Gbit x16 memory. Additionally, the MAX 10 supports the error correction code (ECC) feature.

Table 36.   DDR3 Pin Assignments, Signal Names, and Functions

Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U5.N3 - U6.K3	DDR3_A0	1.5 V SSTL	V20	Address bus
U5.P7 - U6.L7	DDR3_A1	1.5 V SSTL	D19	Address bus
U5.P3 - U6.L3	DDR3_A2	1.5 V SSTL	A21	Address bus
U5.N2 - U6.K2	DDR3_A3	1.5 V SSTL	U20	Address bus
U5.P8 - U6.L8	DDR3_A4	1.5 V SSTL	C20	Address bus

continued...

Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U5.P2 - U6.L2	DDR3_A5	1.5 V SSTL	F19	Address bus
U5.R8 - U6.M8	DDR3_A6	1.5 V SSTL	E21	Address bus
U5.R2 - U6.M2	DDR3_A7	1.5 V SSTL	B20	Address bus
U5.T8 - U6.N8	DDR3_A8	1.5 V SSTL	D22	Address bus
U5.R3 - U6.M3	DDR3_A9	1.5 V SSTL	E22	Address bus
U5.L7 - U6.H7	DDR3_A10	1.5 V SSTL	Y20	Address bus
U5.R7 - U6.M7	DDR3_A11	1.5 V SSTL	E20	Address bus
U5.N7 - U6.K7	DDR3_A12	1.5 V SSTL	J14	Address bus
U5.T3 - U6.N3	DDR3_A13	1.5 V SSTL	C22	Address bus
U5.M2 - U6.J2	DDR3_BA0	1.5 V SSTL	V22	Bank address bus
U5.N8 - U6.K8	DDR3_BA1	1.5 V SSTL	N18	Bank address bus
U5.M3 - U6.J3	DDR3_BA2	1.5 V SSTL	W22	Bank address bus
U5.K3 - U6.G3	DDR3_CASn	1.5 V SSTL	U19	Row address bus
U5.K9 - U6.G9	DDR3_CKE	1.5 V SSTL	W20	Clock enable
U5.J7 - U6.F7	DDR3_CLK_P	Differential 1.5 V SSTL	D18	Differential output clock
U5.K7 - U6.G7	DDR3_CLK_N	Differential 1.5 V SSTL	E18	Differential output clock
U5.L2 - U6.H2	DDR3_CSn	1.5 V SSTL	Y22	Chip select
U5.E7	DDR3_DM0	1.5 V SSTL	J15	Write mask byte lane 0
U5.D3	DDR3_DM1	1.5 V SSTL	N19	Write mask byte lane 1
U6.B7	DDR3_DM2	1.5 V SSTL	T18	Write mask byte lane 2
U5.E3	DDR3_DQ0	1.5 V SSTL	J18	Data bus byte lane 0
U5.F7	DDR3_DQ1	1.5 V SSTL	K20	Data bus byte lane 0
U5.F2	DDR3_DQ2	1.5 V SSTL	H18	Data bus byte lane 0
U5.F8	DDR3_DQ3	1.5 V SSTL	K18	Data bus byte lane 0
U5.H3	DDR3_DQ4	1.5 V SSTL	H19	Data bus byte lane 0
U5.H8	DDR3_DQ5	1.5 V SSTL	J20	Data bus byte lane 0
U5.G2	DDR3_DQ6	1.5 V SSTL	H20	Data bus byte lane 0
U5.H7	DDR3_DQ7	1.5 V SSTL	K19	Data bus byte lane 0
U5.D7	DDR3_DQ8	1.5 V SSTL	L20	Data bus byte lane 1
U5.C3	DDR3_DQ9	1.5 V SSTL	M18	Data bus byte lane 1
U5.C8	DDR3_DQ10	1.5 V SSTL	M20	Data bus byte lane 1
U5.C2	DDR3_DQ11	1.5 V SSTL	M14	Data bus byte lane 1

continued...

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Board Reference (U5 & U6)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U5.A7	DDR3_DQ12	1.5 V SSTL	L18	Data bus byte lane 1
U5.A2	DDR3_DQ13	1.5 V SSTL	M15	Data bus byte lane 1
U5.B8	DDR3_DQ14	1.5 V SSTL	L19	Data bus byte lane 1
U5.A3	DDR3_DQ15	1.5 V SSTL	N20	Data bus byte lane 1
U6.B3	DDR3_DQ16	1.5 V SSTL	R14	Data bus byte lane 2
U6.C7	DDR3_DQ17	1.5 V SSTL	P19	Data bus byte lane 2
U6.C2	DDR3_DQ18	1.5 V SSTL	P14	Data bus byte lane 2
U6.C8	DDR3_DQ19	1.5 V SSTL	R20	Data bus byte lane 2
U6.E3	DDR3_DQ20	1.5 V SSTL	R15	Data bus byte lane 2
U6.E8	DDR3_DQ21	1.5 V SSTL	T19	Data bus byte lane 2
U6.D2	DDR3_DQ22	1.5 V SSTL	P15	Data bus byte lane 2
U6.E7	DDR3_DQ23	1.5 V SSTL	P20	Data bus byte lane 2
U5.F3	DDR3_DQS_P0	Differential 1.5 V SSTL	K14	Data strobe P byte lane 0
U5.G3	DDR3_DQS_N0	Differential 1.5 V SSTL	K15	Data strobe N byte lane 0
U5.C7	DDR3_DQS_P1	Differential 1.5 V SSTL	L14	Data strobe P byte lane 1
U5.B7	DDR3_DQS_N1	Differential 1.5 V SSTL	L15	Data strobe N byte lane 1
U6.C3	DDR3_DQS_P2	Differential 1.5 V SSTL	R18	Data strobe P byte lane 2
U6.D3	DDR3_DQS_N2	Differential 1.5 V SSTL	P18	Data strobe N byte lane 2
U5.K1 - U6.G1	DDR3_ODT	1.5 V SSTL	W19	On-die termination enable
U5.J3 - U6.F3	DDR3_RASn	1.5 V SSTL	V18	Row address select
U5.T2 - U6.N2	DDR3_RESETn	1.5 V SSTL	B22	Reset
U5.L3 - U6.H3	DDR3_WEn	1.5 V SSTL	Y21	Write enable
U5.L8	DDR3_ZQ1	1.5 V SSTL	—	ZQ impedance calibration
U6.H8	DDR3_ZQ2	1.5 V SSTL	—	ZQ impedance calibration

A.9.3. Flash

The MAX 10 FPGA Development Kit provides a 512 Mb (megabit) quad SPI flash memory. The Generic Quad SPI controller core is used by default to erase, read, and write quad SPI flash in reference designs of the Board Test System (BTS) installer.

If you use the parallel flash loader (PFL) IP to program the quad SPI flash, you need to generate a `.pof` (Programmer Object file) to configure the device.

Perform the following steps to generate a `.pof` file:

1. Create a byte-order `Quartus.ini` file with the setting:

```
PGMIO_SWAP_HEX_BYTE_DATA=ON
```

2. Copy the `.ini` file to the project root directory and open the project with the Quartus Prime software.

3. Open **Convert Programming Files** tool to generate the `.pof` file.

Table 37.   Default Memory Map of the 512 Mb QSPI Flash

| Block Description	Size (KB)	Address Range
Board test system scratch	512	0x03F8.0000 − 0x03FF.FFFF
User software	56640	0x0083.0000 − 0x03F7.FFFF
Factory software	4096	0x0043.0000 − 0x0082.FFFF
Zips(html, web content)	4096	0x0003.0000 − 0x0042.FFFF
Board information	64	0x0002.0000 − 0x0002.FFFF
Ethernet option bits	64	0x0001.0000 − 0x0001.FFFF
User design reset vector	64	0x0000.0000 − 0x0000.FFFF

Table 38.   Flash Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U7)	Schematic Signal Name	I/O Standard	MAX 10 FPGA Pin Number	Description
U7.7	QSPI_CSn	3.3 V	C2	Chip select
U7.16	QSPI_CLK	3.3 V	B2	Clock
U7.3	QSPI_RESETn	3.3 V	W12 (MAX II)	Reset
U7.15	QSPI_IO0	3.3 V	C6	Address bus
U7.8	QSPI_IO1	3.3 V	C3	Address bus
U7.9	QSPI_IO2	3.3 V	C5	Address bus
U7.1	QSPI_IO3	3.3 V	B1	Address bus

A.10. Power Distribution System

The following figure shows the power tree drawing for the MAX 10 FPGA development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 23.   Power Distribution System
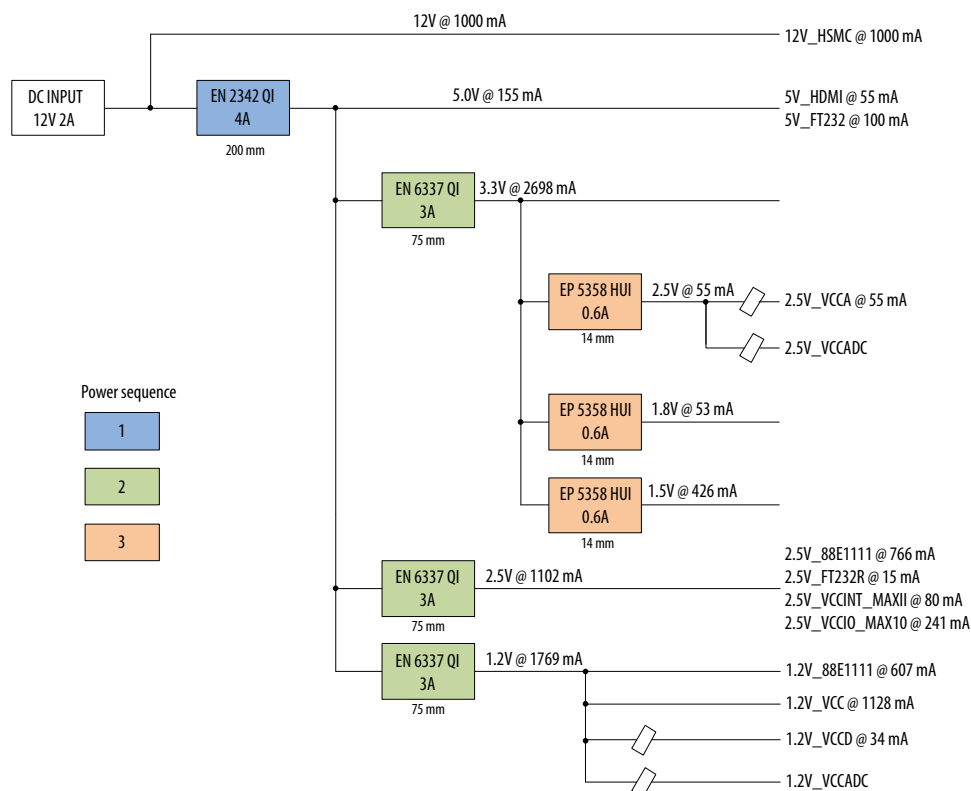
B. Developer Resources

Use the following links to check the Intel website for other related information.

Table 39.   MAX 10 FPGA Development Kit References

Reference	Description
MAX 10 FPGA Development Kit page	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
Rocketboard.org	Open-source community website supporting SoC development including Altera and Partner SoC development kit targets and related designs and documentation.
Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide	Installing the SoC EDS and Arm DS-5. Preloader user guide. Hard Processor System (HPS) Flash programmer. Bare Metal and Linux* Compilers. Debugging.
AN 958: Board Design Guidelines	Board design-related resources for Altera® devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
MAX 10 Power Management User Guide	Describes the MAX 10 device family's power-optimization features, power-up and power-down sequences, power distribution network, and power optimization techniques.
MAX 10 FPGA Configuration User Guide	Describes the features and guidelines to configure the MAX 10 configuration RAM. MAX 10 devices support configuration using the following interfaces: JTAG and internal flash.
Documentation: MAX 10	MAX 10 device documentation.
Cadence* Capture CIS Schematic Symbols	MAX 10 OrCAD symbols.

C. Safety and Regulatory Compliance Information

C.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.

- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

C.1.1. Safety Warnings

Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.
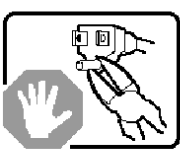
Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

> **WARNING**
>
> **RISK OF ELECTRIC SHOCK**
>
> **Connect only to a properly earth grounded outlet.**
>
> **Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.**

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

> **WARNING**
>
> **RISK OF ELECTRIC SHOCK**
>
> **Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.**

Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

C.1.2. Safety Cautions

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

廢電池請回收

(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

C.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

$$CE \quad \begin{matrix}UK\\CA\end{matrix}$$

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