Intel® Stratix® 10 TX Transceiver Signal Integrity Development Kit User Guide

Online Version
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Contents

1. Overview

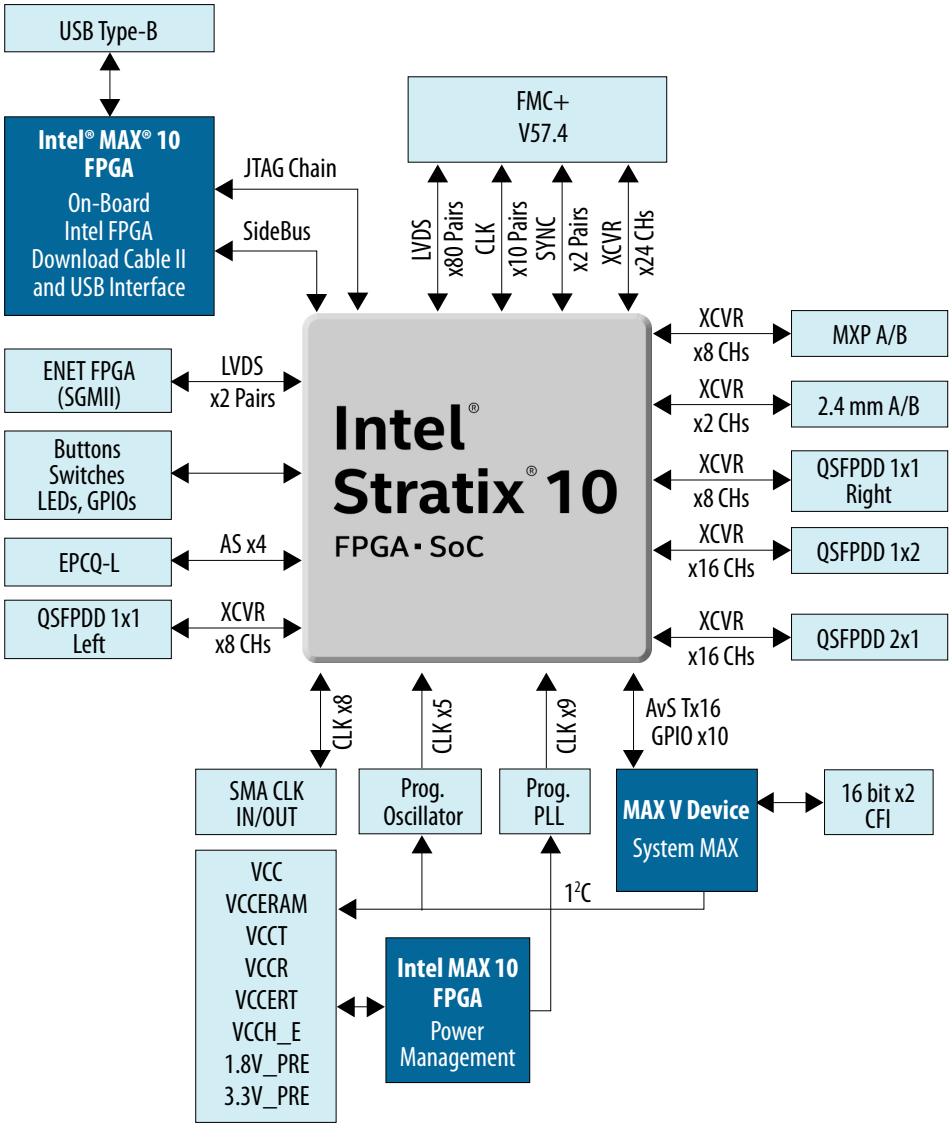
1.1. General Development Kit Description

The Intel® Stratix® 10 TX Transceiver Signal Integrity Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Stratix 10 TX FPGA designs.

The following list describes what you can accomplish with this kit:

- Evaluate transceiver performance up to 58 Gbps for E- Tile.
- Generate and check pseudo-random binary sequence (PRBS) patterns
- Dynamically change differential output voltage (VOD) pre-emphasis and equalization settings to optimize transceiver performance for your channel
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to PCI Express* (PCIe*), 10G/25G/50G/100G/200G/400G Ethernet and other major standards.

Figure 1. Intel Stratix 10 TX Development Kit Block Diagram



1.2. Recommended Operating Conditions

The recommended operating conditions for this development kit are:

- Recommended ambient operating temperature range: 0 °C to 45 °C
- Maximum I-VCCERT load current: 50 A
- Maximum ICC load transient percentage: 30 %
- FPGA maximum power supported by the supplied heatsink/fan: 200 W

1.3. Handling the Kit

When handling the board, it is important to observe static discharge precautions.

Note: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Note: You must not operate this kit in a Vibration environment.

2. Getting Started

2.1. About the Intel Quartus® Prime Software

The Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

The new Intel Quartus Prime design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation.

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition.

The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs.

The Intel Stratix 10 TX FPGA is only supported on Intel Quartus Prime Pro Edition. There is no paid license fee required for Intel Stratix 10 support in Intel Quartus Prime Pro Edition.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Intel Quartus Prime Pro Edition page from Intel's website.

2.2. Development Kit Package

Unzip the initial package which includes board design files, Documents and Factory Recovery files directories. The table below lists the file directory names and a description of their contents.

Table 1. Installed Development Kit Directory Structure

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
`documents`	Contains the development kit documentation
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents

Note: To view the the layout `*.brd` files in the board package, you can download the Cadence® Allegro®/OrCAD® Free Viewer from Cadence's website.

Related Information

Cadence Allegro Downloads

2.3. Installing the Intel FPGA Download Cable II Driver

The Intel Stratix 10 TX Transceiver Signal Integrity Development Kit includes embedded Intel FPGA Download Cable II circuits for FPGA and MAX® V programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

Cable and Adapter Drivers Information

3. Development Kit Setup

The instructions in this chapter explain how to setup the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit.

3.1. Setting up the Development Kit

To prepare and apply power to the board, perform the following steps:

1. The Intel Stratix 10 TX transceiver signal integrity development kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the Factory Default Switch and Jumper Settings on page 10 to return the board to its factory settings before proceeding forward.
2. The development kit ships with design examples stored in the flash device. The **POWER-ON** slide switch (**SW10**) is provided to turn the board **ON** or **OFF**.

   Note: When the power cord is plugged into connector **J46** of the Intel Stratix 10 transceiver signal integrity development kit, 12V_IN and 3.3V_STBY are present on to the board with switch **SW10** in the **OFF** position. These voltages are restricted to a small area of the board. When switch **SW10** is placed to **ON** position, all voltages planes have power at this point.
3. Set the **POWER-ON** switch **SW10** to the **ON** position. When power is supplied to the board, three green LEDs (**D23**, **D24** and **D25**) illuminate and an amber LED (**D5**) extinguishes indicating that the board has power. If the amber LED (**D5**) illuminates, it indicates that one or more power supply is incorrect.
4. **RESET** button (**S7**) is connected to the MAX V CPLD (MAX_RESETn pin) that is used for AvST configuration. When this button is pressed, the MAX V CPLD initiates a reloading of the stored image from the flash memory using AvST configuration mode. The image loaded right after power cycle or MAX V reset depends on FACTORY_LOAD **SW5.1** settings.
   - OFF(1) - factory load
   - ON (0) - user defined load #1

Page selection can be changed by the PGMSEL button (**S5**) when the board is powered on, and PGM_CONFIG (**S6**) is used to reconfigure FPGA with corresponding page which is indicated by PGM_LED0, PGM_LED1 or PGM_LED2.

Caution: Use only the supplied power supply. Power regulation circuits on the board can get damaged by power supplies with greater voltage.

The MAX V CPLD device on the board contains a parallel flash loader II (PFL II) megafunction. If AvST configuration mode is selected, after a **POWER-ON** or **RESET** (reconfiguration) event, the MAX V CPLD configures the Intel Stratix 10 FPGA in AvST mode with either factory design or user design depending on the setting of FACTORY_LOAD.

This development kit includes a MAX V CPLD design which contains the PFL II megafunction. The design resides in the <package dir>\examples\max5 directory. When configuration is complete, LED **D21** (CONF_DONE) illumintes signaling that the Intel Stratix 10 TX FPGA device is configured successfully. If the configuration fails, the LED **D19** (ERROR) illuminates.

3.2. Factory Default Switch and Jumper Settings

This section shows the factory default switch and jumper settings for the Intel Stratix 10 TX transceiver signal integrity development kit.

Table 2. Factory Default Switch Settings

Switch	Board Label	Default Position	Function
SW8	MSEL1	MSEL1=0	MSEL Setting = 0
	MSEL2	MSEL2=0	MSEL Setting = 0
SW1-1	Stratix 10	OPEN/OFF	Enable Intel Stratix 10 in JTAG Chain
SW1-2	MAX V	OPEN/OFF	Enable MAX V in JTAG chain
SW1-3	FMC A	CLOSE/ON	Bypass FMC from JTAG chain
SW1-4	UBMAX_DIP	OPEN/OFF	UB MAX V User Dipswitch
SW6-1	OFF = OSC ON = SMA	OPEN/OFF	Select Si549 clock source for U1
SW6-2/3/4	PWRMAX_DIP	OPEN/OFF	Power MAX V User Dipswitch
SW7-1	OFF=VCC ISOLATE	CLOSE/ON	U47/U48 (LTM4680) are enabled in I2C topology
SW7-2	ON=FULL CHAIN	CLOSE/ON	U47/U48 (LTM4680) are enabled in I2C topology
SW3-1	EN_VCCH_E	OPEN/OFF	Enable on-board VCCH_E regulator
SW3-2	EN_VCCERT	OPEN/OFF	Enable on-board VCCERT regulator
SW2-1	VCCR	OPEN/OFF	Enable on-board VCCR regulator
SW2-2	VCCT	OPEN/OFF	Enable on-board VCCT regulator
SW2-3	VCCERAM	OPEN/OFF	Enable on-board VCCERAM regulator
SW2-4	VCC	OPEN/OFF	Enable on-board VCC regulator
SW5-1	FACTORY_LOAD	OPEN/OFF	Factory Load Control
SW5-2	MAX5_SWITCH2	OPEN/OFF	MAX V user DIPSwitch
SW5-3	MAX5_SWITCH0	OPEN/OFF	MAX V user DIPSwitch
SW5-4	MAX5_SWITCH1	OPEN/OFF	MAX V user DIPSwitch

continued...

Switch	Board Label	Default Position	Function
SW4-1	S10_UNLOCK	OPEN/OFF	Intel Stratix 10 User DIPSwitch
SW4-2	USER_DIP2	OPEN/OFF	Intel Stratix 10 User DIPSwitch
SW4-3	USER_DIP1	OPEN/OFF	Intel Stratix 10 User DIPSwitch
SW4-4	USER_DIP0	OPEN/OFF	Intel Stratix 10 User DIPSwitch
SW10	SW10	OFF	On-board power switch

4. Development Kit Components

4.1. Development Kit Overview

Figure 2. Intel Stratix 10 TX Transceiver Signal Integrity Development Kit Picture

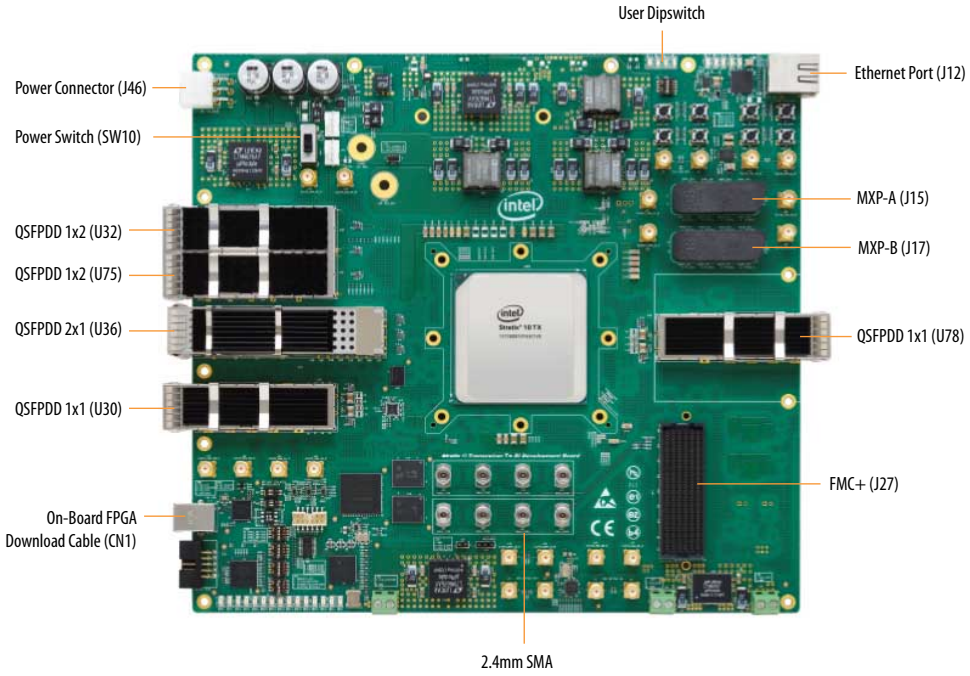


Table 3. Development Kit Components

Board Reference	Type	Description
Featured Devices		
U39	FPGA	Intel Stratix 10 TX 280 F2912 FPGA (1ST280EY2F55E1VG)
U13	CPLD	System MAX V CPLD (5M2210ZF256)
U4	FPGA	USB Intel MAX 10 FPGA (10M04SCU169)
U8	FPGA	PWR Intel MAX 10 FPGA (10M16SAU169)
General User Input and Output		
D12-D15	User LEDs (Green)	User LEDs (Green)
D16-D21	MAX V LEDs (Green)	MAX V LEDs (Green)

continued...

Board Reference	Type	Description
S1-S4	User Push Buttons	User Push Buttons
SW4	User DIP Switches	User DIP
SW5	MAX V DIP Switch	MAX V DIP Switch
S5-S8	MAX V Push Buttons	MAX V Push Buttons
Configuration, Status and Setup Elements		
J8	Embedded Intel FPGA Download Cable II Programming Header (uses JTAG mode only)	Header to interface external Intel FPGA Download Cable direct to FPGA (through USB Intel MAX 10)
D1-D2	Green LEDs	JTAG transmit-Receive Activity
D3-D4	Green LEDs	System Console transmit-Receive Activity
D5	Amber LEDs	System Power error indicator
D6	Amber LEDs	Temperature alert indicator
D7-D11	Ethernet LEDs	Ethernet LEDs (TX/RX/LINK)
Clock Circuits		
X2	50-MHz Oscillator	This 50-MHz oscillator is the clock source to clock buffer SL18860DC that provides three 50 MHz outputs to the FPGA, MAX V and UB2 Intel MAX 10
X1	50-MHz Oscillator	This 50-MHz oscillator provides clock to the PWR Intel MAX 10 FPGA
Y1	Transceiver Dedicated Reference Clock/ Programmable Oscillator	Feed clock for Intel Stratix 10 TX device and an LVDS trigger output at board reference J3/J4. The external input is available at board reference J1 and J2. The default frequency is 156.25 MHz.
U1	High-speed clock buffer	Fan-out REFCLKs for Intel Stratix 10 TX transceiver banks
U3	Transceiver Dedicated Reference Clock/ Programmable PLL	Feeds clocks for Intel Stratix 10 TX device and an LVDS trigger output at board reference J5/J6. The default frequencies are 156.25 MHz, 125 MHz, 100 MHz, 322.265625 MHz, 176.5625 MHz, 307.2 MHz.
J30,J32	External core clock input	SMA external input at `CLKIN_2L`
J31,J33	External core clock output	SMA external output at `PLL_2L_CLKOUT0`
J34-J35	External transceiver clock input	SMA external input at H-tile 1D bank
J36-J37	External transceiver clock input	SMA external input at E-tile 8B bank
J38-J39	External transceiver clock input	SMA external input at E-tile 8C bank
J40-J41	External transceiver clock input	SMA external input at E-tile 9A bank
J42-J43	External transceiver clock input	SMA external input at E-tile 9B bank
J44-J45	External transceiver clock input	SMA external input at E-tile 9C bank
Transceiver Interfaces		

continued...

Board Reference	Type	Description
J15/J17	MXP connector	NRZ 28.9 Gbps or PAM4 58 Gbps, 4 channels connected to each MXP connector
J19-J26	2.4 mm RF connector	NRZ 28.9 Gbps or PAM4 58 Gbps, 2 channels connected to 2.4 mm RF connector
U30/U78	QSFPDD 1x1 optical transceiver interface	PAM4 58 Gbps, 8 channels connected to 400 Gbps module
U32/U75	QSFPDD 1x2 optical transceiver interface	NRZ 28.9 Gbps, 8 channels per port connected 200 Gbps module
U36	QSFPDD 2x1 optical transceiver interface	NRZ 28.9 Gbps, 8 channels per port connected to both top and bottom 200 Gbps module
J27	FMC+ connector	NRZ 28 Gbps, 24 channels connected to FMC+ connector
Memory Devices		
U14-U15	Flash Memory	Two 1-Gbit Micron MT28EW01GABA1HPC CFI Flash device
Communication Ports		
J12	Gigabit Ethernet Port	RJ-45 connector which provides a 10/100/1000 Ethernet connection through a Marvell 88E1111 PHY
CN1	USB Type-B connector	Connects a type-B USB cable
Power Supply		
U47-U48	Two LTM4678s	Power regulators for VCC rail
U49	LTM4676A	Power regulator for VCCERAM rail
U51	LTM4678	Power regulator for VCCERT rail
U50	LTM4675	Power regulator for VCCR/VCCT rail
U52	LTM4676A	Power regulator for 1.8V/VCCH_E rail
U58	EP5348UI	Power regulator for 2.4V rail
U60	EN5339	Power regulator for 2.5V rail
U53	LTM4676A	Power regulator for 3.3V rail

4.2. Intel Stratix 10 TX FPGA

The development board features the Intel Stratix 10 TX FPGA (1ST280EY2F55E1VG).

Table 4. Intel Stratix 10 TX FPGA I/O Summary

Signal Name	I/O Count	Description
Configuration		
S10_JTAG_TDI/TDO/TCK/TMS	4	JTAG pins
FPGA_MSEL[2:0]	3	Configuration input pins to set configuration scheme

continued...

Signal Name	I/O Count	Description
FPGA_CONF_DONE	1	Configuration done pin
FPGA_nSTATUS	1	Configuration status pin
FPGA_INIT_DONE	1	Configuration pin to signify user mode
FPGA_nCONFIG	1	Configuration input pin to reset FPGA
FPGA_OSC_CLK_1	1	125 MHz Clock
FPGA_AS_CLK	1	Configuration Clock for AS configuration schemes
CPU_RESETn	1	Configuration input pin that clears all device registers
FPGA_CONFIG_D[15:0]	32	Configuration input pin that enables all I/Os
FPGA_AS_DATA[3:0]	4	EPCQL data bus
FPGA_AVST_READY	1	SDM ready for AvST configuration scheme
FPGA_AVST_VALID	1	Data valid for AvST configuration scheme
FPGA_AVST_CLK	1	Configuration Clock for AvST configuration scheme
FPGA_PR_DONE	1	Partial reconfiguration done pin
FPGA_PR_REQUEST	1	Partial reconfiguration request pin
FPGA_PR_ERROR	1	Partial reconfiguration error pin
NPERSTL0	1	Reset pin for left bottom PCIe HIP
FPGA_CvP_DONE	1	CvP configuration done pin
FPGA_SEU_ERR	1	SEU error indicate pin
VCC_SDA/SCL	2	SmartVID I^2C bus
VCC_ALERTn	1	SmartVID I^2C bus
Transceivers		
OIF_SCL[1:0]	2	Optical Management Data Clock 0
OIF_SDA[1:0]	2	Optical Management Data I/O Bi-Directional Data 0
DDQ1x1_modselL	1	DDQ1x1 module select control pin
DDQ1x1_resetL	1	DDQ1x1 module reset control pin
DDQ1x1_Initmode	1	DDQ1x1 initiate mode control pin
DDQ1x1_modprsL	1	DDQ1x1 module present indicator pin
DDQ1x1_intl[1:0]	2	DDQ2x1 module interrupt pin
DDQ1x1_1_modselL	1	DDQ1x1 module select control pin
DDQ1x1_1_resetL	1	DDQ1x1 module reset control pin
DDQ1x1_1_Initmode	1	DDQ1x1 initiate mode control pin

continued...

Signal Name	I/O Count	Description
DDQ1x1_1_modprsL	1	DDQ1x1 module present indicator pin
DDQ1x1_1_intl[1:0]	2	DDQ2x1 module interrupt pin
DDQ2x1_modselL[1:0]	2	DDQ2x1 module select control pin
DDQ2x1_resetL[1:0]	2	DDQ2x1 module reset control pin
DDQ2x1_Initmode[1:0]	2	DDQ2x1 initiate mode control pin
DDQ2x1_modprsL[1:0]	2	DDQ2x1 module present indicator pin
DDQ2x1_intl[1:0]	2	DDQ2x1 module interrupt pin
DDQ1x2_modselL[1:0]	2	DDQ1x2 module select control pin
DDQ1x2_resetL[1:0]	2	DDQ1x2 module reset control pin
DDQ1x2_Initmode[1:0]	2	DDQ1x2 initiate mode control pin
DDQ1x2_modprsL[1:0]	2	DDQ1x2 module present indicator pin
DDQ1x2_intl[1:0]	2	DDQ1x2 module interrupt pin
FALAp/n[31:0]	64	FMC+ A LA bank GPIOs
FALAp/n[33:32]_CON	4	FMC+ A LA bank GPIOs
FAHAp/n[23:0]	48	FMC+ A HA bank GPIOs
FAHBp/n[21:0]	44	FMC+ A HB bank GPIOs
FACLKM2CP/N[1:0]	4	FMC+ A general clocks
FACLKBIDIRP/N[3:2]	4	FMC+ A general clocks
FAREFCLKC2MP/N	2	FMC+ A general clocks
FAREFCLKM2CP/N	2	FMC+ A general clocks
FASYNCC2MP/N	2	FMC+ A general clocks
FASYNCM2CP/N	2	FMC+ A general clocks
RZQ_2N	1	RZQ pin for bank 2N
Other Bus		
USER_DIP[2:0]/S10_Unlock	4	User Dipswitch bits
USER_LED[3:0]	4	User LED bits
USER_IO[9:0]	10	User IO bits
USER_PB[3:0]	4	User Push Button bits
USB_DATA[7:0]	8	Side bus between Intel Stratix 10 and UB2Intel MAX 10
USB_ADDR[1:0]	2	Side bus between Intel Stratix 10 and UB2Intel MAX 10
USB_FULL/EMPTY/RESETn	3	Side bus between Intel Stratix 10 and UB2Intel MAX 10
USB_OEn/RDn/WRn	3	Side bus between Intel Stratix 10 and UB2Intel MAX 10

continued...

Signal Name	I/O Count	Description
USB_SCL/SDA	2	Side bus between Intel Stratix 10 and UB2Intel MAX 10
ENET_MDIO/MDC/RSTn/INTn	4	10/100/1000M Ethernet port
ENET_SGMII_TX_P/N	2	10/100/1000M Ethernet port
ENET_SGMII_RX_P/N	2	10/100/1000M Ethernet port
I2C_1V8_SCL	1	Intel Stratix 10 I^2C bus
I2C_1V8_SDA	1	Intel Stratix 10 I^2C bus
Temperature		
OVERTEMPn_1V8	1	Intel Stratix 10 over temperature indicator
TEMP_ALERTn_1V8	1	Intel Stratix 10 temperature alert indicator
Global Clocks		
CLK_50M_S10	1	50 MHz Global clock input
CLK_TOP_PLL_125M_p/n	2	125 MHz differential core clock for top
CLKIN_SMA_2L_p/n	2	Global Clock input from SMA
CLKOUT_SMA_2L_p/n	2	Dedicated Clock output to SMA
USB_FPGA_CLK	1	USB FPGA Clock
CLK_BOT_PLL_100M_p/n	2	100 MHz differential core clock for bottom
Transceiver Clocks		
CLK_9C_OSC_156M_p/n	2	Differential REFCLK to xcvr bank 9C
CLK_9B_OSC_156M_p/n	2	Differential REFCLK to xcvr bank 9B
CLK_9A_OSC_156M_p/n	2	Differential REFCLK to xcvr bank 9A
CLK_8C_OSC_156M_p/n	2	Differential REFCLK to xcvr bank 8C
CLK_8B_OSC_156M_p/n	2	Differential REFCLK to xcvr bank 8B
CLK_9C_PLL_322M_p/n	2	Differential REFCLK to xcvr bank 9C
CLK_9B_PLL_322M_p/n	2	Differential REFCLK to xcvr bank 9B
CLK_9A_PLL_176M_p/n	2	Differential REFCLK to xcvr bank 9A
CLK_8C_PLL _176M_p/n	2	Differential REFCLK to xcvr bank 8C
CLK_8B_PLL _307M_p/n	2	Differential REFCLK to xcvr bank 8B
CLK_1E_PLL_307M_p/n	2	Differential REFCLK to xcvr bank 1E
CLKIN_SMA_1D_p/n	2	Differential REFCLK to xcvr bank 1D
CLKIN_SMA_8B_p/n	2	Differential REFCLK to xcvr bank 8B
CLKIN_SMA_8C_p/n	2	Differential REFCLK to xcvr bank 8C
CLKIN_SMA_9A_p/n	2	Differential REFCLK to xcvr bank 9A

continued...

Signal Name	I/O Count	Description
CLKIN_SMA_9B_p/n	2	Differential REFCLK to xcvr bank 9B
CLKIN_SMA_9C_p/n	2	Differential REFCLK to xcvr bank 9C
FAGBTCLKM2CP/N[5:0]	12	Differential REFCLK to xcvr bank 8B

Note: SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through the Power Management Bus (PMBus™) or Pulse-Width Modulation (PWM) interface for proper performance.

4.3. MAX V CPLD

The Intel Stratix 10 TX transceiver signal integrity development kit consists of a MAX V CPLD (5M2210Z-F256), 256-pin FineLine BGA package. MAX V CPLD devices provide programmable solutions for applications such as FPGA reconfiguration from flash memory, I2C chain to manage power consumption, core temperature, fan speed, clock frequency. MAX V devices feature on-chip flash storage, internal oscillator and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirements.

The following list summarizes the features of MAX V CPLD devices:

- 2210 Logic Elements (LEs)
- 8192 bits of User Flash Memory
- 4 global clocks
- 1 internal oscillator
- 271 maximum user I/O pins
- Low-cost, low power and non-volatile CPLD architecture
- Fast propagation delays and clock-to-output times
- Single 1.8V external supply for device core
- Bus-friendly architecture including programmable slew rate, drive strength, bushold and programmable pull-up resistors

Table 5. MAX V I/O Summary

Signal Name	Description
FA_A[27:1]	Flash Address Bus
FM_D[15:0]	Flash Data Bus
FLASH_RESETn	Flash reset
FLASH_CEn[1:0]	Flash chip enable
FLASH_OEn	Flash output enable
FLASH_WEn	Flash write enable
FLASH_WPn	Flash write protection
FLASH_RDYBSYn	Flash chip ready/busy

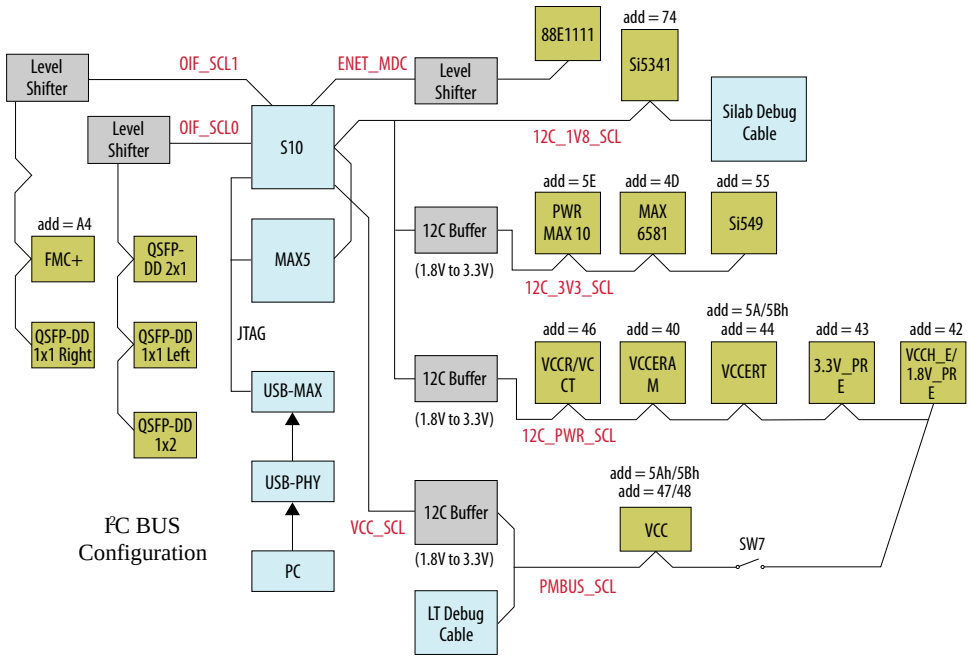
continued...

Signal Name	Description
FLASH_BYTEn	Flash byte enable
FPGA_CONFIG_D[15:0]	FPGA AvST Configuration Data Bus
FPGA_INIT_DONE	FPGA initialization complete
FPGA_nSTATUS	FPGA status
FPGA_CONF_DONE	FPGA configuration complete
FPGA_nCONFIG	FPGA configuration control pin to reset FPGA
FPGA_SEU_ERR	FPGA configuration SEU error
FPGA_CvP_DONE	FPGA CvP configuration done
FPGA_PR_REQUEST	FPGA partial reconfiguration request
FPGA_PR_DONE	FPGA partial reconfiguration done
FPGA_PR_ERROR	FPGA partial reconfiguration error
FPGA_MSEL[2:0]	FPGA configuration mode setting bits
FPGA_AVST_CLK	FPGA AvST Configuration clock
FPGA_AVST_VALID	FPGA AvST Configuration data valid
FPGA_AVST_READY	FPGA AvST Ready to receive data
I2C_1V8_SCL	MAX V I2C bus
I2C_1V8_SDA	MAX V I2C bus
SI5341_ENn	SI5341 1 enable
SI5341_INTn	SI5341 1 interrupt indicators
SI5341_RSTn	SI5341 1 reset
SI5341_LOLn	SI5341 1 loss of lock indicators
SI547_FS[1:0]	SI547 frequency selection bits when Si549 is replaced with Si547
PCIe_PERSTn_1V8	1.8V PCIe reset signal
PCIe_PERSTn_3V3	3.3V PCIe reset signal
PCIe_WAKEn_3V3	3.3V PCIe wake signal
FACLKDIR	FMC+ bi-directional clock direction selection bit
PMBUS_ALERTn	VCC regulator alert
I2C_PWR_ALERTn	Other regulators alert
VCC_ALERTn	1.8V VCC regulator alert
EN_MASTER[2:0]	Enable specific I^2C buffer
OVERTEMPn_1V8	FPGA over temperature input 1.8V
TEMP_ALERTn	FPGA temperature alert output
OVERTEMPn	FPGA over temperature output
TEMP_ALERTn_1V8	FPGA temperature alert input 1.8V

continued...

Signal Name	Description
USB_CFG[14:0]	Bus between USB MAX 10 and MAX V
USB_SYSMAX_CLK	Clock from USB PHY chip
MAX_OSC_CLK_1	25M/100M/125MHz clock input
SYSMAX_JTAG_TCK	MAX V TCK
SYSMAX_JTAG_TMS	MAX V TMS
SYSMAX_JTAG_TDI	MAX V TDI
SYSMAX_JTAG_TDO	MAX V TDO
FACTORY_LOAD	Factory image for configuration
MAX5_SWITCH[2:0]	System MAX V user dipswitch
PGM_SEL	Flash memory PGM select pushbutton
PGM_CONFIG	Flash memory PGM configuration pushbutton
MAX_RESETn	System MAX V reset pushbutton
CPU_RESETn	CPU reset pushbutton
PGM_LED[2:0]	Flash image PGM select indicators
MAXV_ERROR	Intel Stratix 10 configuration error indicator LED
MAXV_LOAD	Intel Stratix 10 configuration active indicator LED
MAXV_CONF_DONE	Intel Stratix 10 configuration done indicator LED
USER_IO[9:0]	User general I/Os
CLK_50M_SYSMAX	50 MHz Clock input
OPT_FAN_RPM	Optical interface fan speed control
FAN_RPM	FPGA fan speed control

Figure 3. I²C Diagram



4.4. FPGA Configuration

This section describes the FPGA, flash memory and MAX V CPLD System Controller device programming methods supported by the Intel Stratix 10 TX tranceiver signal integrity development kit.

Three configuration methods are mostly used on the Intel Stratix 10 TX transceiver signal integrity development kit.

Embedded Intel FPGA Download Cable II is the default method for configuring the FPGA at any time using the Intel Quartus Prime Programmer in JTAG mode with the supplied USB cable.

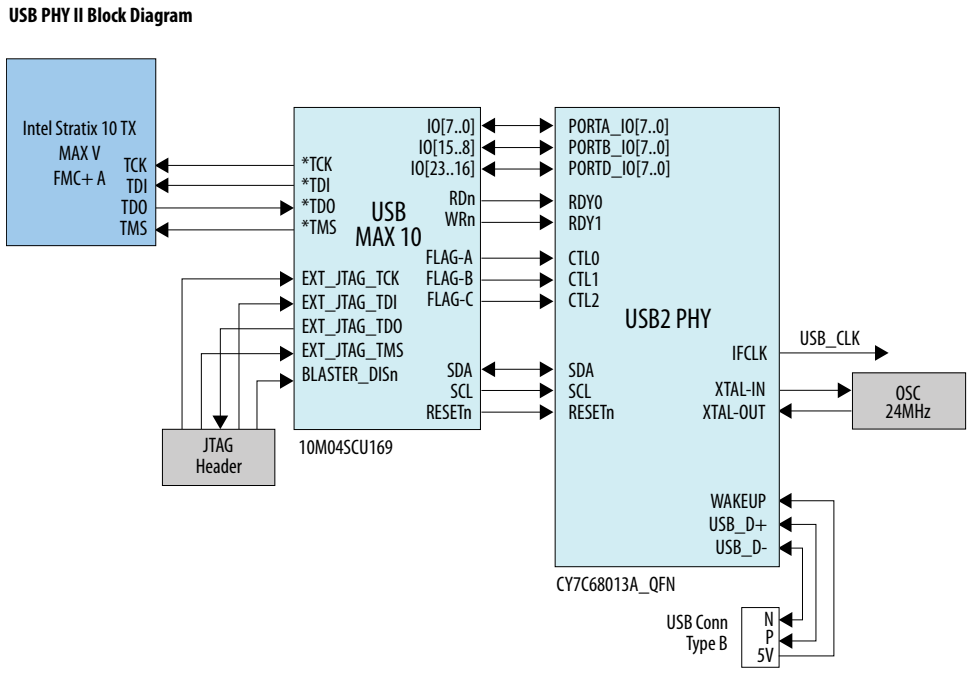
MAX V configures the FPGA device via AvST mode using stored images from CFI flash devices either at power-up or pressing the MAX_RESETn/PGM_CONFIG push button.

JTAG external header for debugging. Intel recommends that you use lower JTAG clock frequency value such as 16 MHz.

4.4.1. Configuring the FPGA over Embedded Intel FPGA Download Cable II

Embedded Intel FPGA Download Cable II is the default method for configuring the Intel Stratix 10 TX FPGA using the Intel Quartus Prime Programmer in the JTAG mode with the supplied USB cable.

Figure 4. Embedded Intel FPGA Download Cable II



The embedded Intel FPGA Download Cable II for USB-based configuration of the Intel Stratix 10 TX FPGA device is implemented using a Type-B USB connector, a CY7C68013A USB2 PHY device, and an Intel MAX 10 10M04SCU169 FPGA. This will allow configuration of the Intel Stratix 10 TX FPGA device using a USB cable directly connected to a computer running Intel Quartus Prime software without requiring the external Intel FPGA Download Cable dongle.

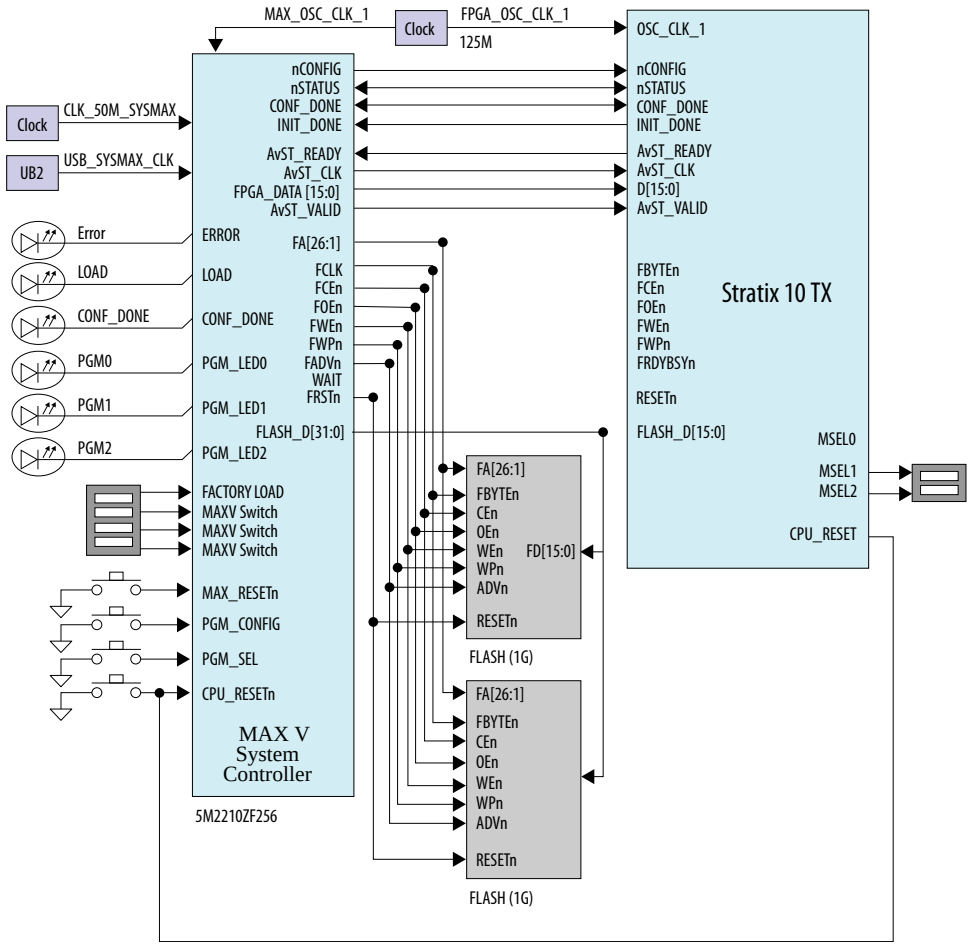
This design will convert USB data to interface with the Intel Stratix 10 TX FPGA's dedicated JTAG port. Four LEDs are provided to indicate embedded Intel FPGA Download Cable II activity. The embedded Intel FPGA Download Cable II is automatically disabled when an external Intel FPGA Download Cable dongle is connected to the JTAG header.

4.4.2. Configuring the FPGA through Flash Memory

The figure below shows a detailed schematic block diagram for the MAX V + Flash AvSTx16 mode configuration implementation.

Note: Typical JTAG clock frequency for CFI Flash programming via PFL II core is 16 MHz. You may try it with a lower frequency such as 6 MHz if it fails with 16 MHz.

Figure 5. MAX V Configuration Block Diagram



The PGMSEL dipswitch (S5) is provided to select between POF files (FACTORY and USER) stored on the Flash.

The Parallel Flash Loader II (PFL II) Megafunction is used to implement the AvSTx16 configuration in the MAX V CPLD. The PFL II Megafunction reads data from the flash and converts it to AvST format. This data is written into the Intel Stratix 10 TX FPGA device through dedicated AvST CLK and FPGA Config Data [15:0] pins at corresponding clock rate, such as 25 MHz, 50 MHz and 100 MHz.

Implementation will be done using an MAX V 5M2210ZF256FBGA CPLD acting as the AvST download controller and two 1G Flash devices.

If AvST configuration mode is selected, after a POWER-ON or RESET (reconfiguration) event, the MAX V device shall configure the Intel Stratix 10 TX FPGA in the AvST x16 mode with either the FACTORY POF or an USER DEFINED POF depnding on the FACTORY_LOAD setting.

The MSEL[2:0] pins indicate which configuration scheme is chosen. The manufacturing default condition is [001] for Fast AS x4 scheme.

For different configuration modes, MSEL [2:0] signals must be set acccording to the table below:

Table 6. Support Configuration Modes for Stratix 10 TX Transceiver Signal Integrity

Configuration Scheme	MSEL [2:0]
Avalon-ST (x16)	101
AS (Normal mode)	011
AS (Fast)	001
JTAG only	111
Not supported	Other Settings

4.4.3. Configuring the FPGA over External Intel FPGA Download Cable

The JTAG chain allows programming of both the Intel Stratix 10 TX FPGA and MAX V CPLD devices using an external Intel FPGA Download Cable dongle or the on-board Intel FPGA Download Cable II via the USB Interface Connector. During board bring-up, and as a back-up in case the on-board Intel FPGA Download Cable II has a problem, the external Intel FPGA Download Cable can be used to program both the Intel Stratix 10 and MAX V CPLD via the Intel FPGA Download Cable 2x5 pin 0.1" programming header (J8)

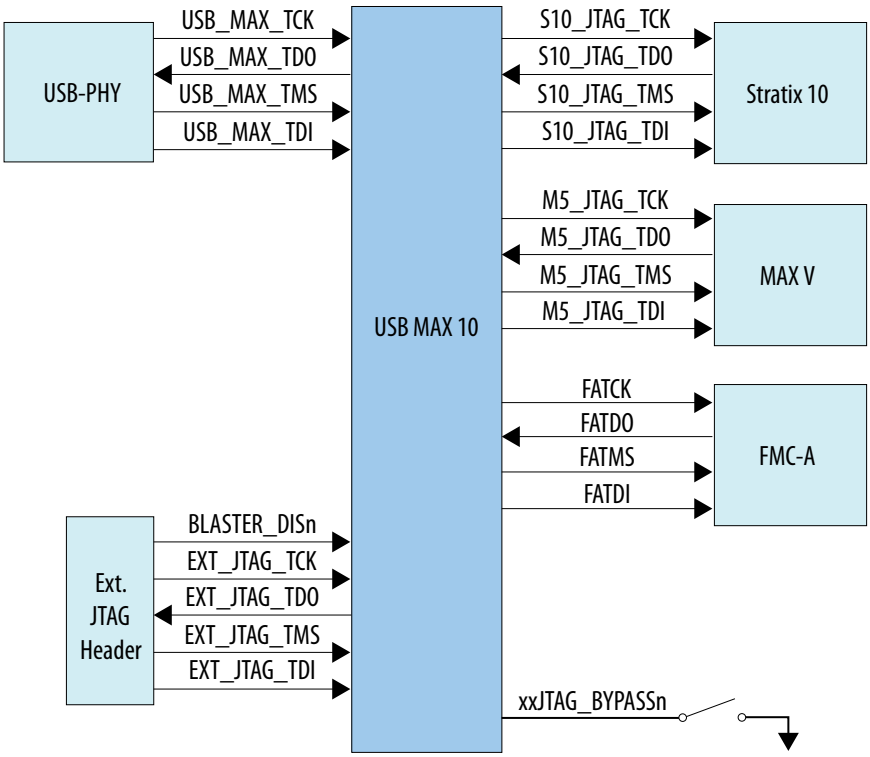
Another 2x5 pin 0.1" vertical non-shrouded header (J9) is provided on the board for programming the Intel MAX 10 FPGA for configuring the on-board Intel FPGA Download Cable II circuitry. Once the on-board Intel FPGA Download Cable II is configured and operational, the on-board Intel FPGA Download Cable II can be used for subsequent programming of the Intel Stratix 10 TX FPGA and MAX V CPLD.

The on-board Intel FPGA Download Cable II JTAG chain connects the downstream JTAG nodes in the following order, with the option to bypass the Intel Stratix 10, MAX V, FMC by a dip switch SW1 setting as follows:

- Switch closed/ON: Corresponding JTAG node is bypassed.
- Switch open/OFF: Corresponding JTAG node is enabled in the JTAG chain.

Pin 2 of the J8 Header is used to disable the embedded Intel FPGA Download Cable II by connecting it to the embedded Intel FPGA Download Cable II's low active disable pin with a pull-up resistor. Since Pin 2 from the mating Intel FPGA Download Cable dongle is GND, when the dongle is connected into the JTAG header, the embedded Intel FPGA Download Cable II is disabled to avoid contention with the external Intel FPGA Download Cable dongle.

Figure 6. JTAG



4.5. Status and Setup Elements

The development board includes board-specific status LEDs and switches for enabling and configuring various features on the board. This section describes these status elements.

Table 7. Board Specific LEDs

Board Reference	Signal Name	Description
D23	---	Green LED. Power 3.3 V present
D24	---	Green LED. Power 3.3 V PRE present
D25	---	Green LED. Power 12 V present
D5	PWR_ERR_LED	Amber LED. System Power error indicator
D1	JTAG_RX	Green LED. JTAG receiver activity indicator
D2	JTAG_TX	Green LED. JTAG transmitter activity indicator
D3	SC_RX	Green LED. System console receiver activity indicator
D4	SC_TX	Green LED. System console transmitter activity indicator
D7	ENET_LED_TX	Green LED. Blinks to indicate Ethernet PHY transmit activity

continued...

Board Reference	Signal Name	Description
D8	ENET_LED_RX	Green LED. Blinks to indicate Ethernet PHY receive activity.
D9	ENET_LED_LINK1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed
D10	ENET_LED_LINK100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed
D11	ENET_LED_LINK10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed
D6	OVERTEMP	Amber LED. Intel Stratix 10 FPGA over temperature indicator

This development board includes several different kinds of setup elements. This section describes the following setup elements:

- JTAG Chain Device Removal Switch
- Program Select Pushbutton
- MAX V Reset Pushbutton
- CPU Reset Pushbutton

JTAG Chain Device Removal Switch

The JTAG chain connects the Intel Stratix 10 TX FPGA, the MAX V CPLD, FMC in a chain, with the option to selectively bypass each JTAG node by four dip switch setting.

Program Select Pushbutton

If AvST configuration mode is selected, after a POWER-ON or RESET (reconfiguration) event, the MAX V configures the Intel Stratix 10 TX FPGA if configuration mode is AvST mode with either the FACTORY POF or a USERDEFINED POF depending on FACTORY_LOAD setting. The setting of the PGMSEL bit is selected by the PGMSEL pushbutton. Pressing this pushbutton and observing the program LEDs (FACTORY or USER) dictates the program selection. Then, the PGM_CONFIG pushbutton must be pressed to load the program.

MAX V Reset Pushbutton

This pushbutton is the development board's Master Reset. This pushbuttton is connected to the MAX V CPLD (MAX_RESETn pin) that is used for AvST configuration. When this button is pressed, the MAX V CPLD initiates a reloading of the stored image from flash memory using AvST configuration mode. The image that is reloaded depends on the PGMSEL setting.

CPU Reset Pushbutton

This pushbutton is the Nios II CPU Reset. This button is connected to a Intel Stratix 10 TX FPGA global signal input pin and can be used by Nios II implementations as a dedicated CPU Reset button. This button is also connected to the MAX V CPLD so that the FPGA device can be reset right after its configuration with AvST mode.

4.6. User Input-Output Components

This section describes the user I/O interface to the FPGA. The following I/O elements are described:

- User-defined Pushbuttons
- User-defined DIP Switches
- User-defined LEDs

User-Defined Pushbuttons

This development kit includes 4 user-defined pushbuttons and 4 system pushbuttons that allow you to interact with the Intel Stratix 10 TX FPGA. When you press and hold down the pushbutton, the device pin is set to logic 0; when you release the pushbutton, the device pin is set to logic 1. There is no board-specific function for these general user pushbuttons.

The table below lists the pushbuttons, schematic signal names and their corresponding Intel Stratix 10 TX FPGA device pin numbers.

Table 8. User-Defined Pushbuttons

Board Reference	Schematic Signal Name	Description	Intel Stratix 10 TX Pin Number
S1	USER_PB0	User Pushbutton	N19
S2	USER_PB1	User Pushbutton	P19
S3	USER_PB2	User Pushbutton	L23
S4	USER_PB3	User Pushbutton	M23
S5	PGM_SEL	System Pushbutton	N/A
S6	PGM_CONFIG	System Pushbutton	N/A
S7	MAX_RESETn	System Pushbutton	N/A
S8	CPU_RESETn	System Pushbutton	R35

User-Defined DIP Switch

Board reference **SW4** and **SW5** are two 4-pin DIP switches. The switches are user-defined and provides additional FPGA input control. When the switch is in the OPEN or OFF position, a logic **1** is selected. When the switch is in the CLOSED or ON position, a logic **0** is selected. There is no board-specific function for these switches.

The table below lists the schematic signal names of each DIP switch and their corresponding Intel Stratix 10 TX FPGA pin numbers.

Table 9. User-Defined DIP Switch

Board Reference	Schematic Signal Name	Intel Stratix 10 TX Pin Number
SW4.4	USER_DIP0	G23
SW4.3	USER_DIP1	G24
SW4.2	USER_DIP2	K23
SW4.1	S10_UNLOCK	K22

User-Defined LEDs

The development board includes 8 user-defined LEDs. Board references **D12** through **D19** are user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Intel Stratix 10 TX FPGA device. The LEDs illuminate when a logic **0** is driven and turns off when a logic **1** is driven. There is no board-specific function for these LEDs.

The table below lists the user-defined schematic signal names and their corresponding Intel Stratix 10 TX FPGA device pin numbers.

Table 10. User-Defined LEDs

Board Reference	Schematic Signal Name	Intel Stratix 10 TX Pin Number
D12	USER_LED0	G31
D13	USER_LED1	H31
D14	USER_LED2	G32
D15	USER_LED3	G33

4.7. Clocks

4.7.1. Transceiver Dedicated Clocks

Dedicated clocking scheme that is implemented on the Intel Stratix 10 TX transceiver signal integrity development board allows different protocols to run simultaneously by the Intel Stratix 10 TX FPGA.

Differential clock sources are provided from an I^2C programmable oscillator or PLL to the dedicated REFCLK input pins of transceiver blocks on both sides of the FPGA. The default frequencies for the oscillator and PLL at startup are:

- 156.25 MHz (Y1 and U3)
- 322.265625 MHz (U3)
- 176.5625 MHz (U3)
- 307.2 MHz (U3)

The default frequencies can be overridden and a different frequency can be programmed into the oscillators and PLLs for support of other protocols.

Note: Programmed frequencies are lost upon a board power down. Oscillator and PLL frequencies return to their default frequency upon power up.

The oscillator or PLL provides a differential LVDS trigger output to SMA connectors for scope or other laboratory equipment triggering purposes.

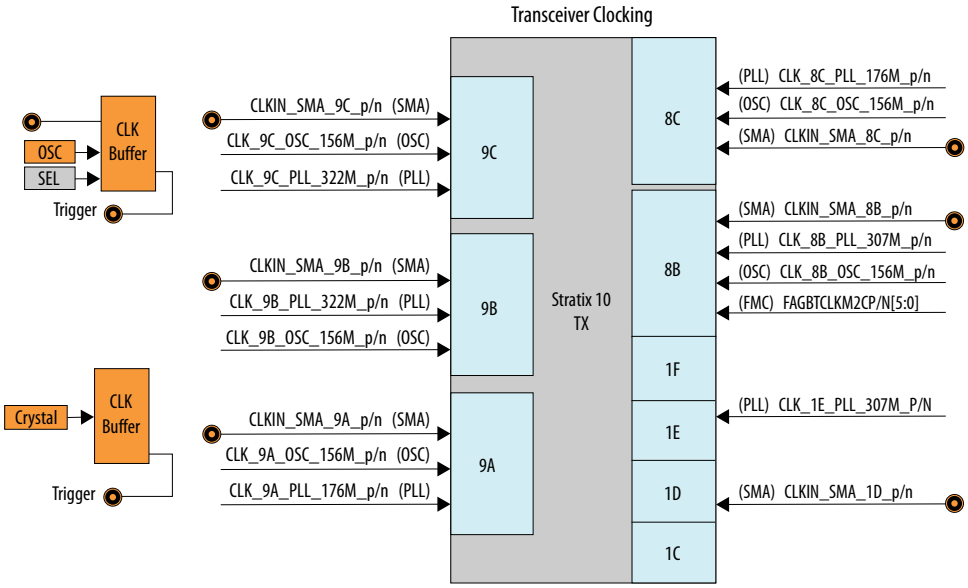
In addition to the two oscillators and PLLs, each transceiver tile have dedicated differential REFCLK input from a pair of SMA connectors to allow use of laboratory equipment clock generators as the transceiver clock source.

The six inputs below connect directly to the transceiver clock inputs:

- J34/J35 SMA connector direct connection to H-tile block
- J36/J37 SMA connector direct connection to E-tile 8B block
- J38/J39 SMA connector direct connection to E-tile 8C block
- J40/J41 SMA connector direct connection to E-tile 9A block
- J42/J43 SMA connector direct connection to E-tile 9B block
- J44/J45 SMA connector direct connection to E-tile 9C block

The figure below shows the dedicated transceiver clocks that are implemented on the Intel Stratix 10 TX FPGA development kit.

Figure 7. Transceiver Clocks



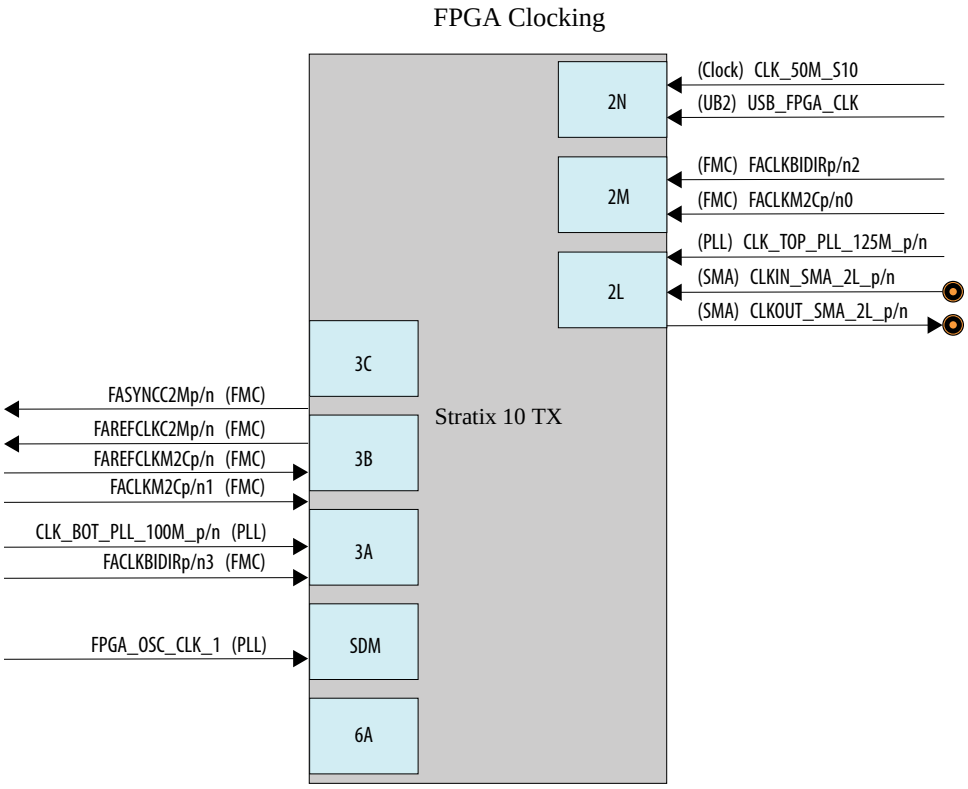
4.7.2. General-Purpose Clocks

In addition to transceiver dedicated clocks, five other clock sources are provided to the FPGA Global CLK inputs for general FPGA design as shown in the figure below.

The usage of these clocks is as follows:

- 50 MHz oscillator through an SL18860 buffer for Nios II applications. USB_FPGA_CLK drives from on-board Intel FPGA Download Cable II circuit.
- External differential clock source from SMA connectors. Dedicated differential output clock to SMA connectors.
- Three clock outputs are provided from two Si5341 PLLs:
  - CLK_BOT_PLL_100M_P/N: 100 MHz LVDS Standard
  - CLK_TOP_PLL_125M_P/N: 125 MHz LVDS Standard
  - FPGA_OSC_CLK_1: 125 MHz 1.8V CMOS Standard
- Clocks from FMC+ daughter card

Figure 8. FPGA Clocks



4.7.3. Embedded Intel FPGA Download Cable II Clock

A 24 MHz crystal is dedicated for the embedded Intel FPGA Download Cable II circuit. The crystal is used to clock the `Cypress CY7C68013A USB2 PHY` device.

4.8. Transceiver Channels

The Intel Stratix 10 TX transceiver signal integrity development kit dedicates 90 channels from both the left and right sides of the device. Transceiver channels are allocated as shown in the table below.

Figure 9. Transceiver Channels Block Diagram

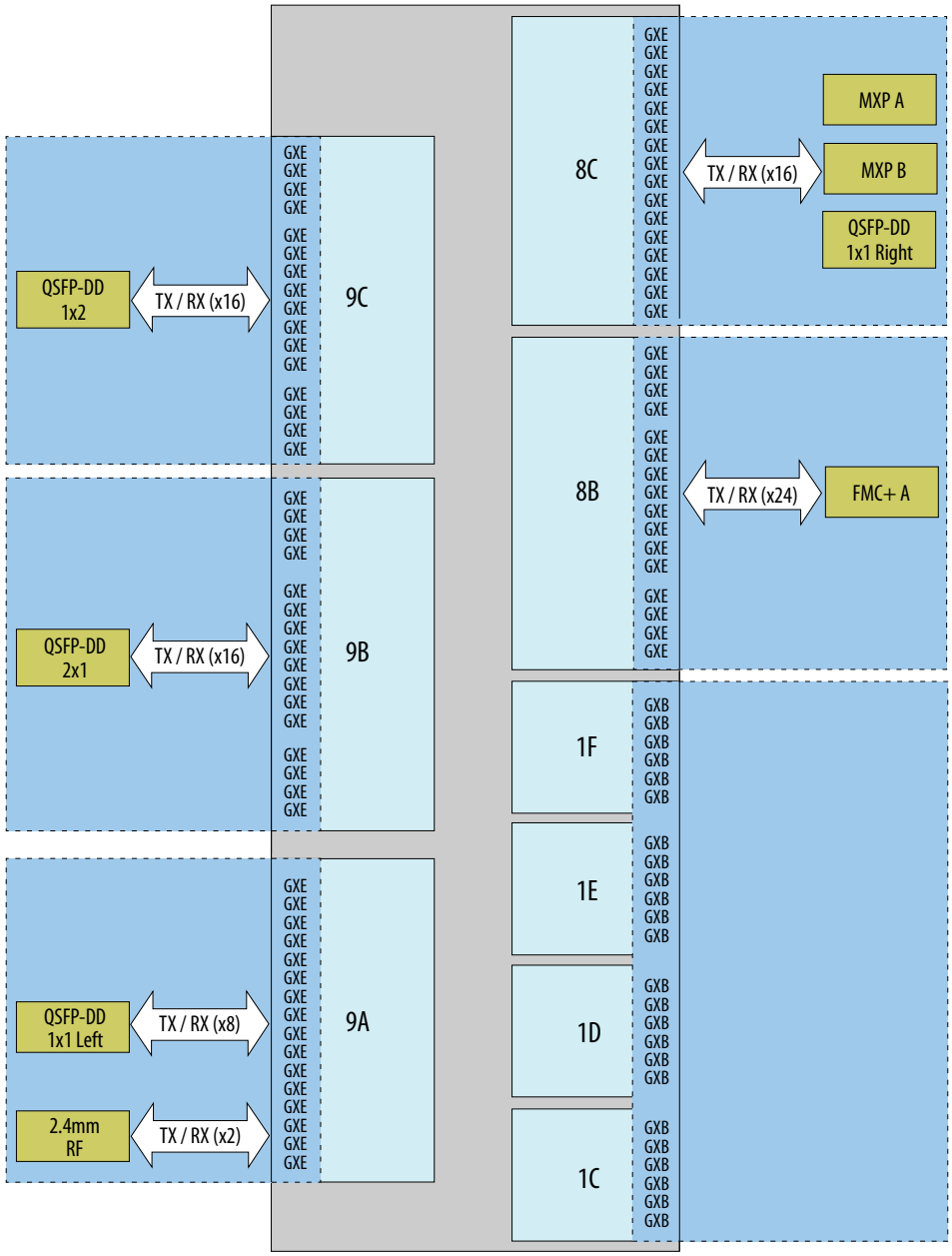


Table 11. Transceiver Channels

Transceiver Channel	Data Rate	Number of Channels
2.4mm RF channel	NRZ 28.9 Gbps or PAM4 58 Gbps	2
MXP connector A	NRZ 28.9 Gbps or PAM4 58 Gbps	4
MXP connector B	NRZ 28.9 Gbps or PAM4 58 Gbps	4
QSFPDD 1x1 Optical Interface (Left and Right)	NRZ 28.9 Gbps or PAM4 58 Gbps	16

continued...

Transceiver Channel	Data Rate	Number of Channels
QSFPDD 1x2 Optical Interface	NRZ 28.9 Gbps or PAM4 58 Gbps	16
QSFPDD 2x1 Optical Interface	NRZ 28.9 Gbps or PAM4 58 Gbps	16
FMC+ A Interface	17.4 Gbps or 28.3 Gbps	24

Table 12. 2.4 mm RF Interface

Signal Net Name	Description
SMAA_TXp/n, SMAB_TXp/n	2.4mm RF Transmitter
SMAA_RXp/n, SMAB_RXp/n	2.4mm RF Receiver

Table 13. MXP Interface

Signal Net Name	Description
MXPA_TXp/n[3:0]	MXP A Transmitter
MXPA_RXp/n[3:0]	MXP A Receiver
MXPB_TXp/n[3:0]	MXP B Transmitter
MXPB_RXp/n[3:0]	MXP B Receiver

Table 14. Optical Modules Interface

Signal Net Name	Description
QSFPDD2x1_TXp/n[15:0]	QSFPDD2x1 Transmitter
QSFPDD2x1_RXp/n[15:0]	QSFPDD2x1 Receiver
QSFPDD1x2_TXp/n[15:0]	QSFPDD1x2 Transmitter
QSFPDD1x2_RXp/n[15:0]	QSFPDD1x2 Receiver
QSFPDD1x1_TXp/n[7:0]	QSFPDD1x1 Transmitter
QSFPDD1x1_RXp/n[7:0]	QSFPDD1x1 Receiver
QSFPDD1x1_1_TXp/n [7:0]	QSFPDD1x1 Transmitter
QSFPDD1x1_1_RXp/n [7:0]	QSFPDD1x1 Receiver

Table 15. FMC+ Interface

Signal Net Name	Description
FAC2Mp/n[23:0]	FMC+ A GXB Transmitter
FAM2Cp/n[23:0]	FMC+ A GXB Receiver

4.9. Communication Ports

The Intel Stratix 10 TX transceiver signal integrity development kit supports a 10/100/1000 BASE-T Ethernet connection using a Marvell 88E1111 PHY device and the Intel Triple-Speed Ethernet Megacore MAC function. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA.

The Intel Stratix 10 GX FPGA device can communicate with the LVDS interfaces at up to 1.25 Gbps. The MAC function is provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5 V and 1.2 V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to an RJ-45 connector with internal magnetics that are used for driving copper lines with Ethernet traffic.

Table 16. Ethernet PHY Pin Assignments

Schematic Signal Name	Marvell 88E1111 (U23) PHY Pin Number	Description
ENET_LED_LINK1000	60/73	1000 Mb link LED
ENET_LED_LINK100	74	100 Mb link LED
ENET_LED_LINK10	59/76	10 Mb link LED
ENET_LED_TX	68	TX data active LED
ENET_LED_RX	69	RX data active LED
ENET_SGMII_TX_P	82	SGMII transmit
ENET_SGMII_TX_N	81	SGMII transmit
ENET_SGMII_RX_P	77	SGMII receive
ENET_SGMII_RX_N	75	SGMII receive
ENET_XTAL_25MHZ	55	25 MHz clock
ENET_T_INTn	23	Management bus interrrupt
ENET_RSET	30	Device reset
MDIO_T	24	Management bus data input/output
MDC_T	25	Management bus data clock
MDI_P0	29	Management bus data
MDI_N0	31	Management bus data
MDI_P1	33	Management bus data
MDI_N1	34	Management bus data
MDI_P2	39	Management bus data
MDI_N2	41	Management bus data
MDI_P3	42	Management bus data
MDI_N3	43	Management bus data

4.10. Flash Memory

4.10.1. Parallel NOR Flash Memory

The Intel Stratix 10 TX Transceiver Signal Integrity Development Kit has two 1-Gbit CFI compatible asynchronous flash device for non-volatile storage of the FPGA configuration data, board information, test application data and user code space.

Two flash devices are implemented to achieve a 16-bit wide data bus at 16 bits each per device. Both MAX V CPLD and Intel Stratix 10 TX FPGA can access this flash device.

MAX V CPLD accesses are for AvST configuration of the FPGA at power-on and board reset events. It uses the PFL Megafunction.

Table 17. Memory Map of the first 1G NOR Flash Memory (x16)

Block Description	Size (KB)	Address Range
Reserved	512	0x0750.0000 - 0x0757.FFFF
Reserved	14336	0x0670.0000 - 0x074F.FFFF
Reserved	8192	0x05F0.0000 - 0x06FF.FFFF
Reserved	8192	0x0570.0000 - 0x05EF.FFFF
User hardware1	44032	0x02C0.0000 - 0x056F.FFFF
User hardware0	44032	0x0010.0000 - 0x02BF.FFFF
PFL option bits	256	0x000C.0000 - 0x000F.FFFF
Reserved	256	0x0008.0000 - 0x000B.FFFF
Reserved	256	0x0004.0000 - 0x0007.FFFF
Reserved	256	0x0000.0000 - 0x0003.FFFF

Table 18. Memory Map of the second 1G NOR Flash Memory (x16)

Block Description	Size (KB)	Address Range
User hardware2	44032	0x0010.0000 - 0x02BF.FFFF
PFL option bits	256	0x000C.0000 - 0x000F.FFFF
Reserved	256	0x0008.0000 - 0x000B.FFFF
Reserved	256	0x0004.0000 - 0x0007.FFFF
Reserved	256	0x0000.0000 - 0x0003.FFFF

4.10.2. EPCQL Flash Memory

The Intel Stratix 10 TX Transceiver Signal Integrity Development Kit has an Intel 1024 Mb EPCQL flash for non-volatile storage of the FPGA configuration data, board information, test application data and user code space. The quad-serial flash provided has a x4 data width, the development board has a x4 data width which can supports an AS x4 configuration scheme.

The table below shows the memory map for this flash memory. This memory provides non-volatile storage for FPGA bit stream, Nios II factory software and other information.

Table 19. EPCQL Flash Memory Map

Block Description	Size (KB)	Address	Comments
Board Test System (BTS) Scratch	512	07F8.0000 - 07FF.FFFF	BTS System Testing
Board Information	64	07F7.0000 - 07F7.FFFF	Board Information
Ethernet Option Bits	64	07F6.0000 - 07F6.FFFF	MAC Address Information
Reserved	64	07F5.0000 - 07F5.FFFF	Reserved
Reserved	4096	0500.0000 - 053F.FFFF	Reserved
Factory Hardware (sof)	81920	0000.0000 - 04FF.FFFF	SOF File

4.11. System Power

4.11.1. Power Guidelines

Intel Stratix 10 TX transceiver signal integrity development kits can be powered by either Intel provided 240 W brick or a standard ATX power supply which provides more than 240 W power. Use Intel provided 24-pin to 6-pin adapter cable to hook up ATX power supply's 24-pin ATX output with Intel Stratix 10 TX transceiver signal integrity development kit's J46 connector. Do not plug an ATX power supply 6-pin connector into J46 connector directly.

You can supply power for VCC, VCCERAM, VCCRT, VCCR, VCCH_E and VCCERT rails with external equipment by following the two steps outlined below for such kind of application:

1. Turn OFF corresponding on-board regulators via SW2 or SW3 dipswitch before board power up.
2. Supply power with banana jacks (J48, J49) or power terminations (J51, J53, J55, J58, J56). Manage the power-up and power-down sequence for on-board regulators and external equipments with necessary tools. Contact Intel support for more details.

4.11.2. Power Supply

Power supply for this development kit is provided through an external laptop style DC power brick connected to a 6-pin ATX power connector. The input voltage is in the range of 12V +/- 5%. This DC voltage is then stepped down to the various power rails used by the components on the development kit.

Note: The power rails on the development board have the option to be supplied from an external source through a banana jack or power terminal connectors by first disabling corresponding power regulator using SW2/SW3 DIP Switch.

Table 20. Power Per Device

Device	Voltage Name	Voltage	Description
Intel Stratix 10 (1ST280EYF2912)	S10_VCC	0.85/VID	Core and periphery power
	S10_VCCH_E	1.1	E-tile XCVR power

continued...

Device	Voltage Name	Voltage	Description
	S10_VCCR	1.12/1.03	H-tile XCVR RX path
	S10_VCCT	1.12/1.03	H-tile XCVR TX path
	S10_VCCERAM	0.9	Memory and PLL digital power
	S10_VCCERT	0.9	E-tile XCVR power
	S10_1V8	1.8	IO voltage, I/O pre-drivers
	S10_2V4	2.4	VCCFUSEWR power
	S10_2V5	2.5	E-tile XCVR power
USB Intel MAX 10 (10M04SCU169)	3.3V_PRE 1.8V_PRE	3.3 1.8	Core, PLL and VCCIO VCCIO for Stratix 10 Interface
PWR Intel MAX 10 (10M16SAU169)	3.3V_STBY	3.3	Intel power management chip
MAX V (EPM2210F256)	S10_1V8 IO_3V3	1.8 3.3	System controller
Flash	S10_1V8	1.8	CFI Flash
USB PHY(CY7C68103)	3.3V_PRE	3.3	USB PHY
Ethernet PHY(88E1111)	IO_2V5	2.5	Ethernet PHY
Clock Buffer (SL18860DC)	1.8V_PRE	1.8	Core clock buffer
Clock Buffer (Si53311)	IO_2V5	2.5	Transceiver Reference Clock Buffers
Programmable PLL (Si5341)	S10_1V8 IO_2V5 IO_3V3	1.8 2.5 3.3	Transceiver Reference clock and core clock
Oscillator (Si549)	IO_3V3	3.3	Oscillator
Temperature monitor (MAX6581)	IO_3V3	3.3	Temperature monitor chip
QSFPDD Modules	IO_3V3	3.3	QSFP28 Modules
FMC	S10_1V8 IO_3V3 IO_12V	1.8 3.3 12	FMC+ interface

4.11.3. Power Management

Intel MAX 10 power logic power management solutions are provided in the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit.

Intel Intel MAX 10 power management solutions are capabale of measuring the voltage, measuring the current, trimming the voltage and sequencing the order at power on and power off. Voltages can be trimmed upto +/- 10%. Communication to these devices is through I^2C interface. Intel development kit's Power GUI is utilized to measure, trim and observe each voltage rail's condition.

4.11.4. Power Distribution System

Figure 10. Power Tree

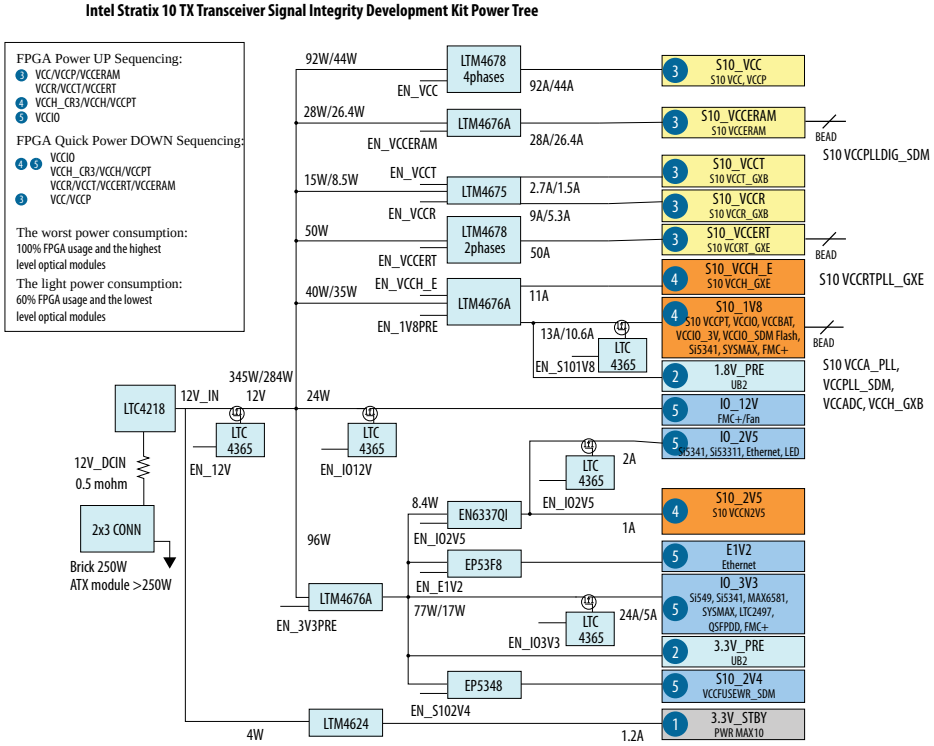
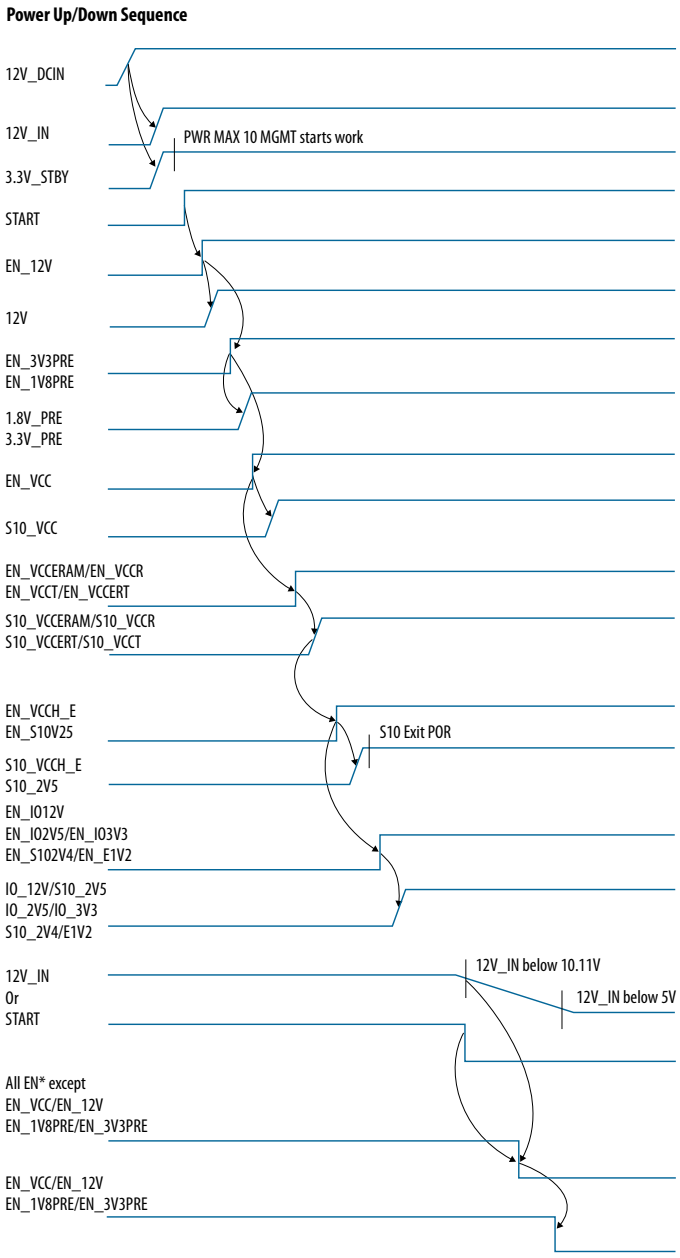


Figure 11. Power Sequence Waveforms



4.11.5. Thermal Limitations and Protection Guidelines

With 25 °C ambient temperature and 50 °C printed circuit board (PCB) temperature, you must ensure that your FPGA designs do not consume more than 200 W with the liquid cooling solution.

MAX6581 chip is connected to the Intel Stratix 10 TX FPGA internal temperature diode to continuously monitor FPGA die temperature. Meanwhile, a dedicated FPGA TSD real-time monitor solution under `~\ip\onchip_sensors\` is added to each transceiver example design to monitor the temperatures of both FPGA core and each transceiver tile.

Based on the data from both MAX6581 and FPGA, MAX V will run fan at its maximum speed whenever any temperature is over 60 °C or immediately power off the board whenever any temperature is over 100 °C. Remember to unplug the power supply when the board is powered off after the temperature crosses 100 °C. Plug the power supply back again to ensure that the board can be normally turned on/off again.

The cooling parts (air duct and fan) for QSFPDD modules are pre-installed, but not powered by default. Plug them into the J60 header if your designs require additional cooling on these interfaces. You can adjust fan speed for both FPGA and optical modules through Power GUI.

5. Board Test System

The Intel Stratix 10 TX Transceiver Signal Integrity Developement Kit includes a design example and an application called the Board Test System (BTS) to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance and measure power consumption.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Intel Stratix 10 TX FPGA device. The figure below shows the Graphical User Interface (GUI) for a board that is in factory configuration.

Figure 12. BTS GUI

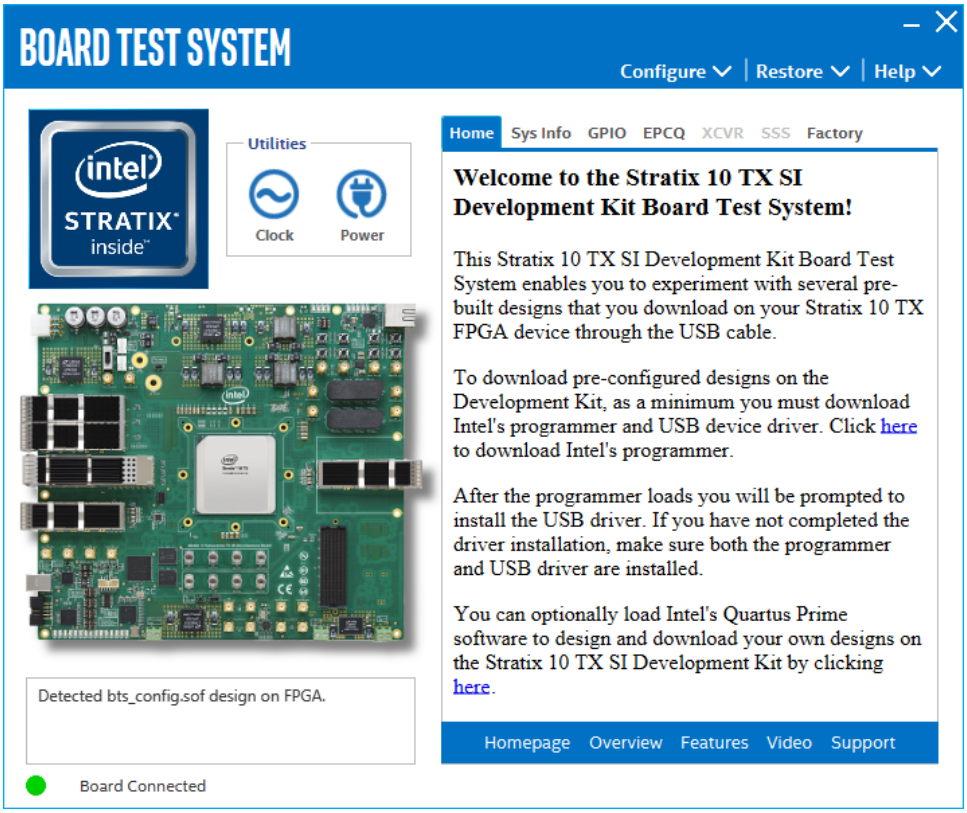
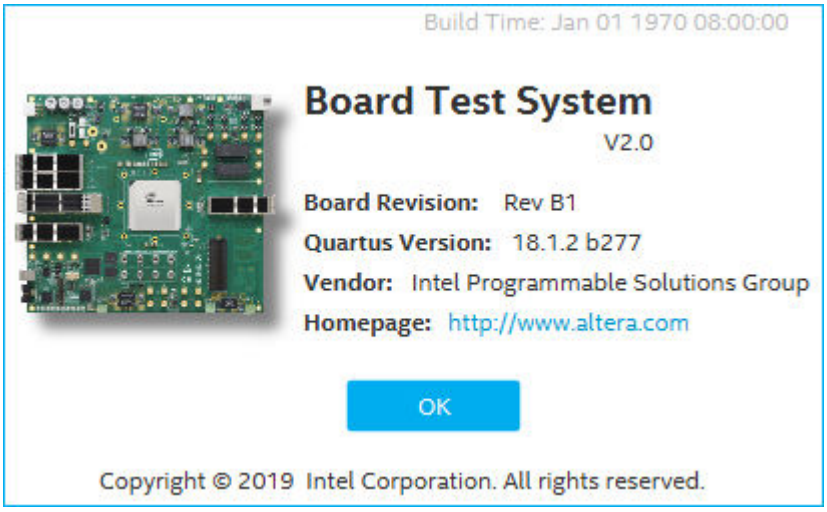


Figure 13. About BTS



5.1. Preparing the Development Kit

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the BTS. The Configure Menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS shares the JTAG bus with other applications like Nios II debugger and the Signal Tap II Embedded Logic Analyzer. As the Intel Quartus Prime Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Intel Quartus Prime Programmer.

5.2. Running the Board Test System

Before you begin

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, open the Intel Quartus Prime software to automatically set the enviromment variable `$QUARTUS_ROOTDIR`. The BTS uses this environment variable to locate the Intel Quartus Prime library. The version of Intel Quartus Prime software set in the `$QUARTUS_ROOTDIR` environment variable should be newer than version 18.1. For example, the Development Kit Installer version 18.1 requires that the Intel Quartus Prime software 18.1 or later version to be installed.

Also, to ensure that the FPGA is configured successfully, you should install the latest Intel Quartus Prime software that can support the silicon on the development kit. For this board, Intel recommends you install Intel Quartus Prime version 19.1.0 B240.

Please refer to the `README.txt` file under `examples\board_test_system` directory.

To run the BTS

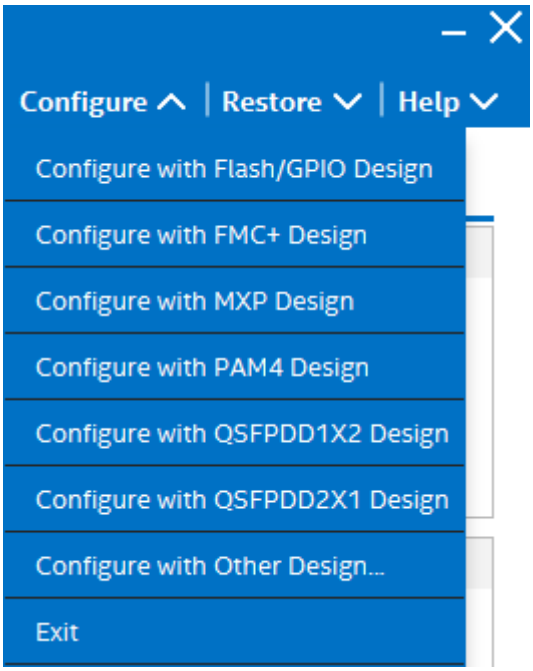
1. Navigate to the `<package dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.
2. A GUI appears, displaying the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, you will receive a message prompting you to configure your board with a valid BTS design. Refer to the **Configure** Menu for information on configuring your board.

5.3. Using the Board Test System

5.3.1. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 14. The Configure Menu



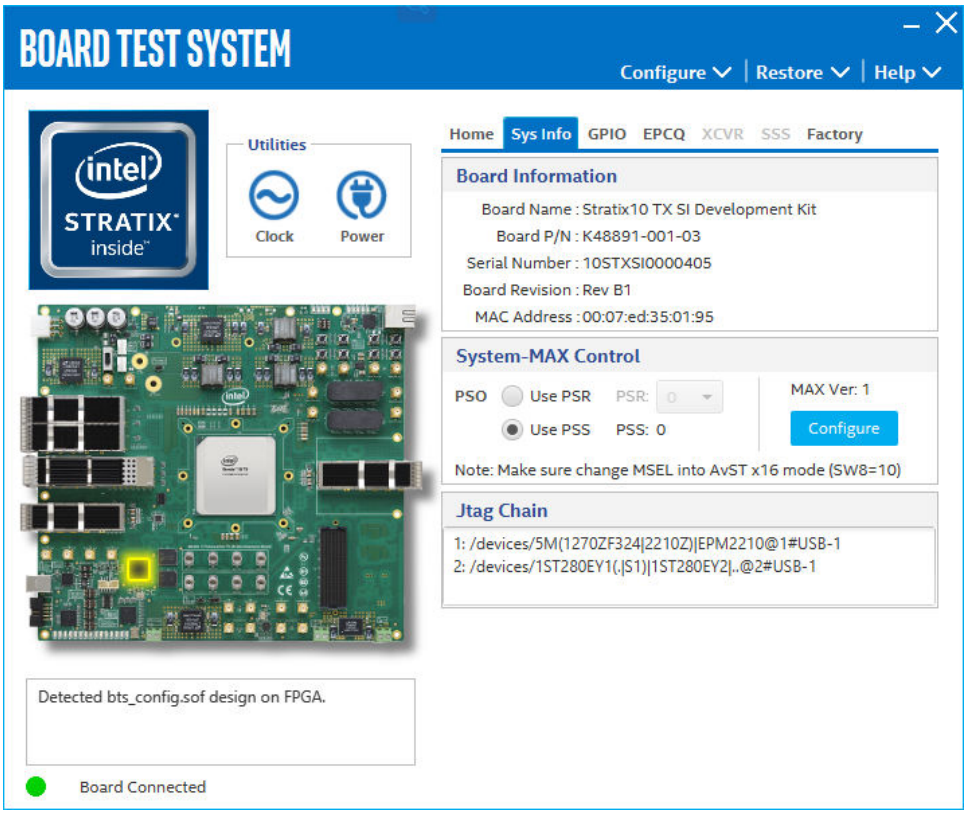
To configure the FPGA with a test system design, perform the following steps:

- On the Configure Menu, click the configure command that corresponds to the functionality you wish to test.
- In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
- When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

5.3.2. The System Info Tab

The System Info tab shows information about the board's current configuration. The tab displays system-MAX V control setting, the board's MAC address, and other details stored on the board.

Figure 15. The System Info Tab



The following sections describe the controls on the System Info tab.

Board Information

The Board Information control displays static information about your board. The information is displayed after configuring the FPGA with GPIO/FLASH design.

- Board Name: Indicates the official name of the board given by the BTS.
- Board P/N: Indicates the part number of the board.
- Serial Number: Indicates the serial number of the board.
- Board Revision: Indicates the revision of the board.
- MAC Address : Indicates the MAC Address of the board.

System-MAX Control

The MAX V register control allows you to view and change the current MAX V register values as described in the table below. Change to the register values with the GUI take effect immediately.

Table 21. MAX V Registers

MAX V Register Values	Description
Configure	Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values.
PSO	Sets the MAX V PSO register
PSR	Sets the MAX V PSR register. Allows PSR to determine the page of flash memory to use for FPGA reconfiguration. The numerical values in the list corrresponds to the page of flash memory to load during the FPGA reconfiguration.
PSS	Displays the MAX V PSS register value. Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
MAX Ver	Indicates the version of MAX V code currently running on the board.The MAX V code resides in the `<package dir>\examples\max5` directory. Newer revisions of this code may be available on the Stratix 10 Transceiver Signal Integrity Development Kit link on the Intel website.

JTAG Chain

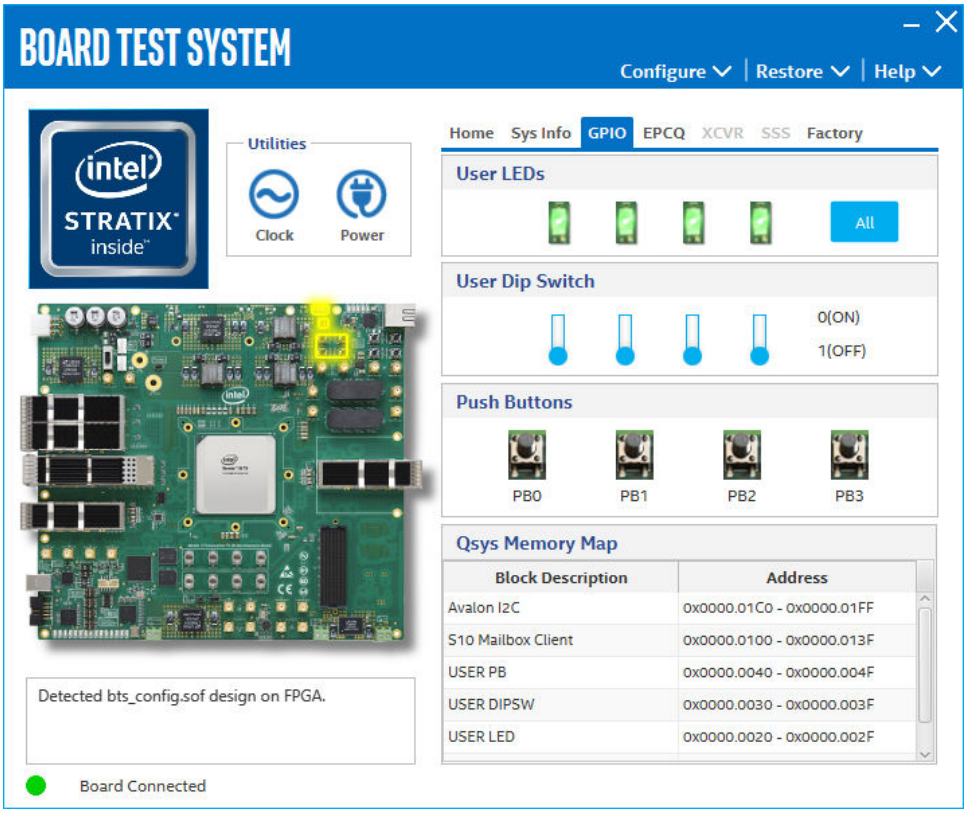
The JTAG chain control shows all the devices currently in the JTAG chain.

Note: When switch SW 1-2 (MAX BYPASS) is set to 1 (OFF), the JTAG chain includes the MAX V device. When set to 0 (ON), the MAX V device is removed from the JTAG chain. System MAX and FPGA must be in the JTAG chain when running the BTS GUI.

5.3.3. The GPIO Tab

The GPIO Tab allows you to interact with all the genral purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off and detect push button presses.

Figure 16. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User DIP Switches

The read-only User DIP switches control displays the current positions of the switches in the user DIP switch bank (SW4). Change the switches on the board to see the graphical display change.

User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

User Push Buttons

The read-only User Push Button control displays the current status of the push buttons. Press the push button on the board to see the graphical display change.

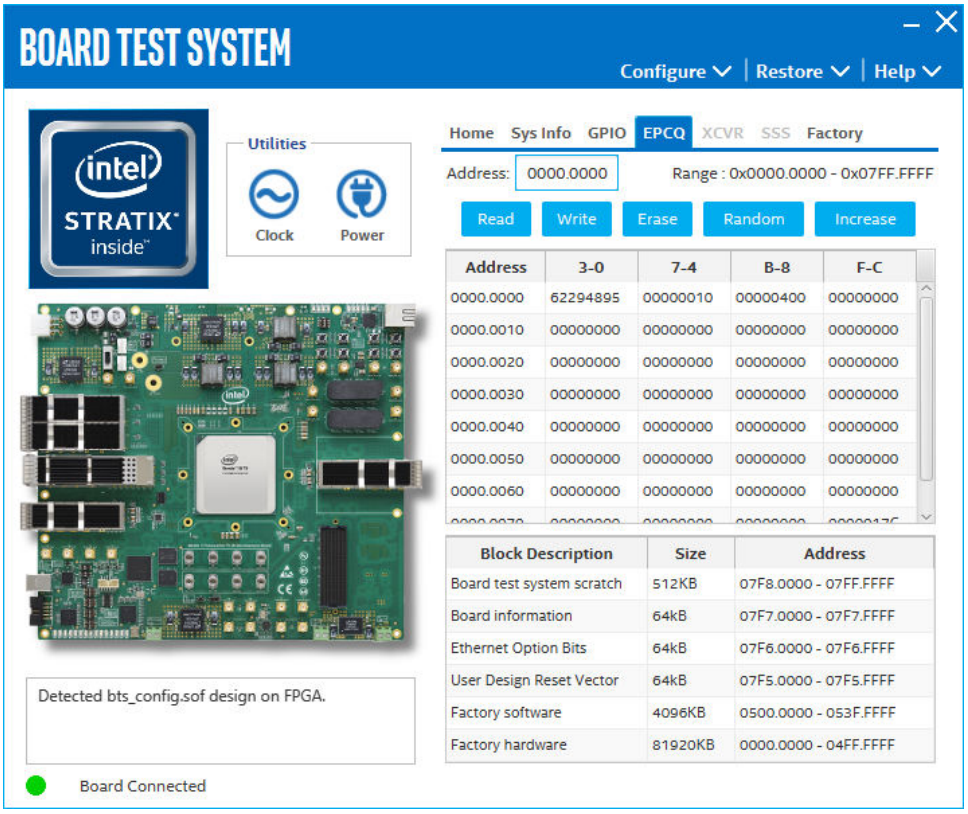
Qsys Memory Map

Shows the memory map of the GPIO/FLASH Qsys system on yor board.

5.3.4. The EPCQ Tab

The EPCQ tab allows you to read and write flash memory on your board.

Figure 17. The EPCQ Tab



The following sections describe the controls on the EPCQ tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory sits at the base address of `0x0000.0000`. To see flash memory contents, type the address above the base and values starting at this address are displayed. Valid entries are `0x0000.0000` through `0x07FF.FF80`.

Note: If you enter an address outside of `0x0000.0000` to `0x07FFF.FFFF` flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Note: To prevent overwriting the dedicated portions of the flash memory, the application limits the writable flash memory address range to `0x07F80000- 0x07FFFF80` .

Erase

When erasing flash memory contents should read FFFFFFFF, which is limited to a scratch page in the upper 512K block.

Increase

Start an increase data pattern to test flash memory.

Random

Starts a random data pattern to test flash memory.

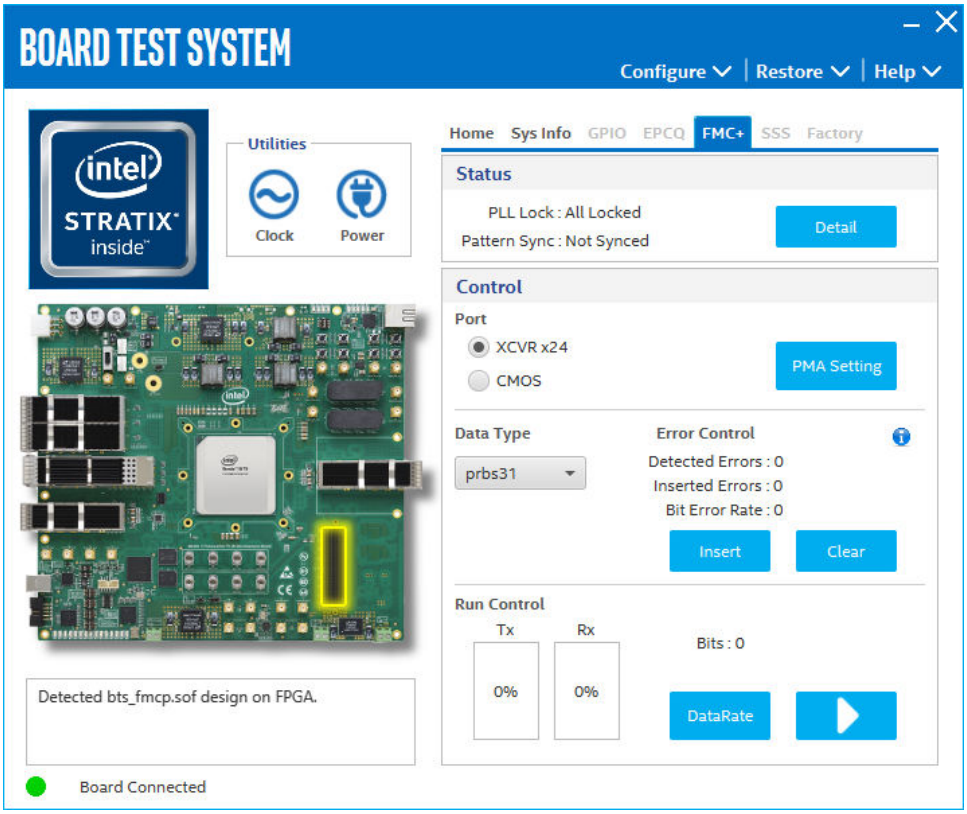
Flash Memory Map

Displays the flash memory map for the Intel Stratix 10 TX transceiver signal integrity development board.

5.3.5. The FMC+ Tab

This tab allows you to perform loopback tests on the FMC+ port, install FMC+ loopback daughter card and configure the FPGA with FMC+ image.

Figure 18. The FMC Tab



The following sections describe the controls on the FMC+ tab.

Status

Displays the following status information during a loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **Details:** Shows the details of PLL lock, pattern status and errors bits of each channel

PLL and Pattern Status

Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0
16	Locked	Synced	0
17	Locked	Synced	0
18	Locked	Synced	0
19	Locked	Synced	0
20	Locked	Synced	0
21	Locked	Synced	0
22	Locked	Synced	0
23	Locked	Synced	0

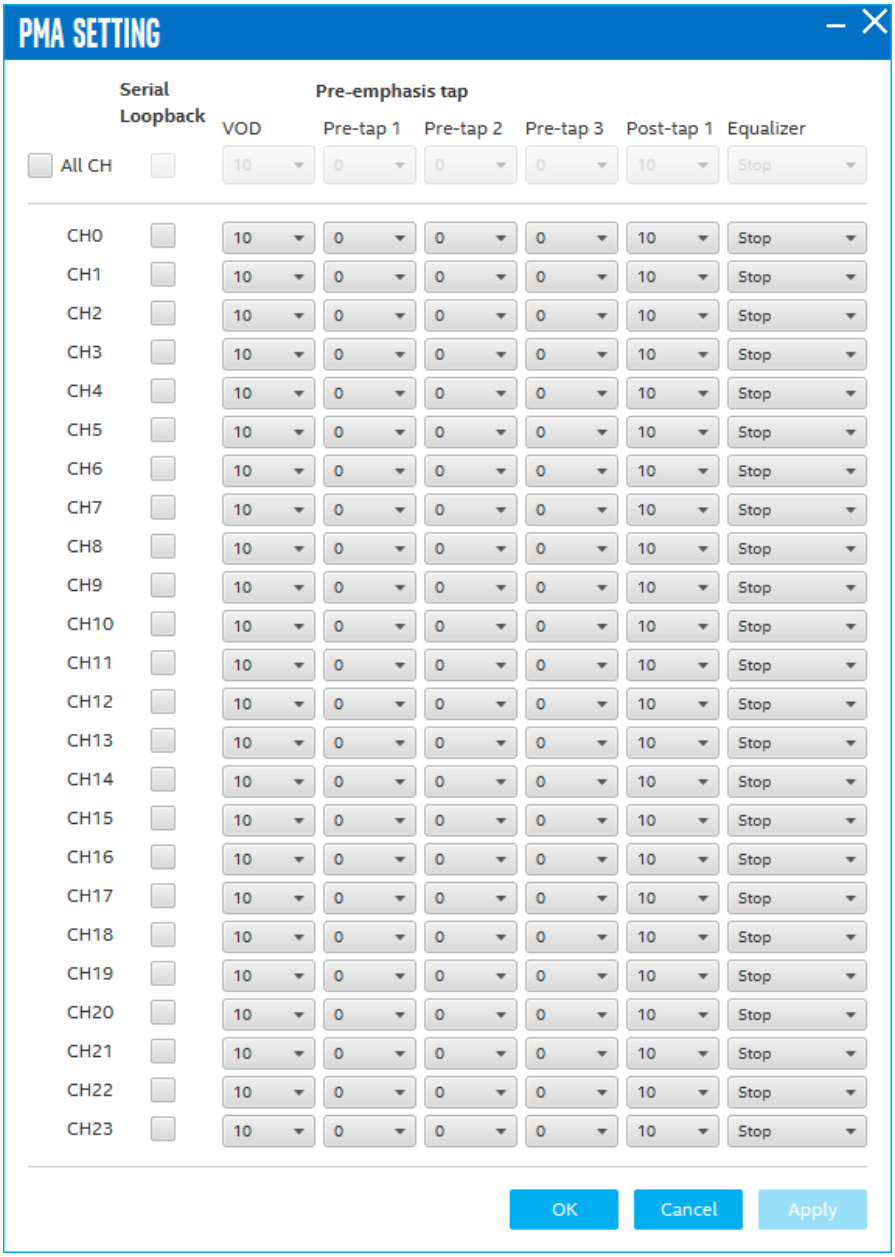
Port

Allows you to specify which interface to test. The following port tests are available: XCVR and CMOS

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- **Equalizer:** Specifies the AC gain setting for the receiver equalizer in four stage mode.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- **PRBS 7:** Selects pseudo-random 7-bit sequences.
- **PRBS 15:** Selects pseudo-random 15-bit sequences.
- **PRBS 23:** Selects pseudo-random 23-bit sequences.

- **PRBS 31:** Selects pseudo-random 31-bit sequences.
- **HF:** Selects highest frequency divide-by-2 data pattern `10101010`.
- **LF:** Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- Bit Error Rate: Displays the error rate of data transaction.
- **Insert:** Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- **Clear:** Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This toggle button control initiates and stops the tests.

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

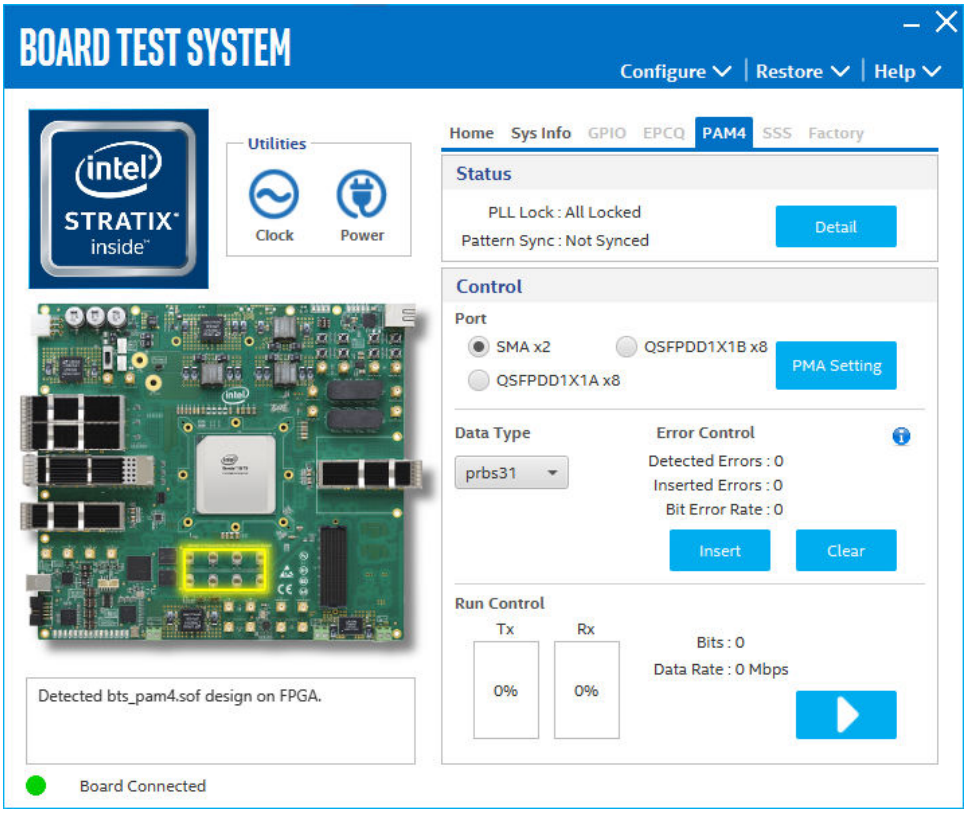
Data Rate

Channel	XCVR Type	Frequency
0	GXE	17499.84 Mbps
1	GXE	17499.84 Mbps
2	GXE	17499.84 Mbps
3	GXE	17499.84 Mbps
4	GXE	17499.52 Mbps
5	GXE	17499.84 Mbps
6	GXE	17499.84 Mbps
7	GXE	17499.84 Mbps
8	GXE	17499.84 Mbps
9	GXE	17499.84 Mbps
10	GXE	17499.84 Mbps
11	GXE	17499.84 Mbps
12	GXE	17499.84 Mbps
13	GXE	17499.84 Mbps
14	GXE	17499.84 Mbps
15	GXE	17499.84 Mbps
16	GXE	17499.84 Mbps
17	GXE	17499.84 Mbps
18	GXE	17499.84 Mbps
19	GXE	17499.84 Mbps
20	GXE	17499.84 Mbps
21	GXE	17499.84 Mbps
22	GXE	17499.84 Mbps
23	GXE	17499.84 Mbps

5.3.6. The PAM4 Tab

The PAM4 tab allows you to perform loopback tests on the SMAA, SMAB, QSFPDD1x1A and QSFPDD1x1B port. Install QSFPDD loopback module and cable for QSFPDD1x1 and 2.4 mm Rf connectors, configure FPGA with PAM4 image.

Figure 19. The PAM4 Tab



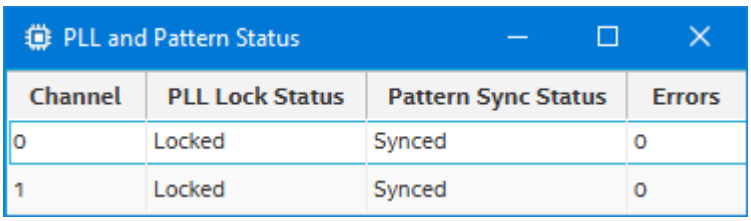
The following sections describe the controls on the PAM4 tab.

Status

Displays the following status information during a loopback test:

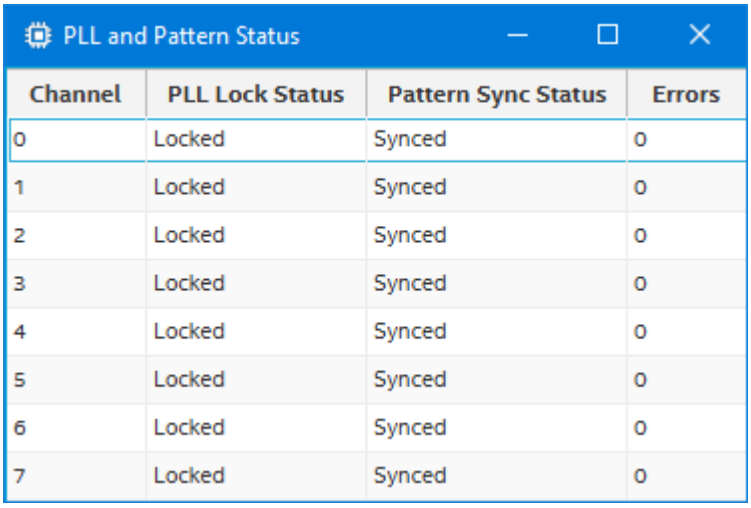
- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **Details:** Shows the details of PLL lock, pattern status and error bits of each channel.

Figure 20. SMA Status



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0

Figure 21. QSFPDD1X1 Status



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available: SMAx2, OSFPx8 and QSFPDDx8.

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the first post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer.

Figure 22. SMA PMA Setting

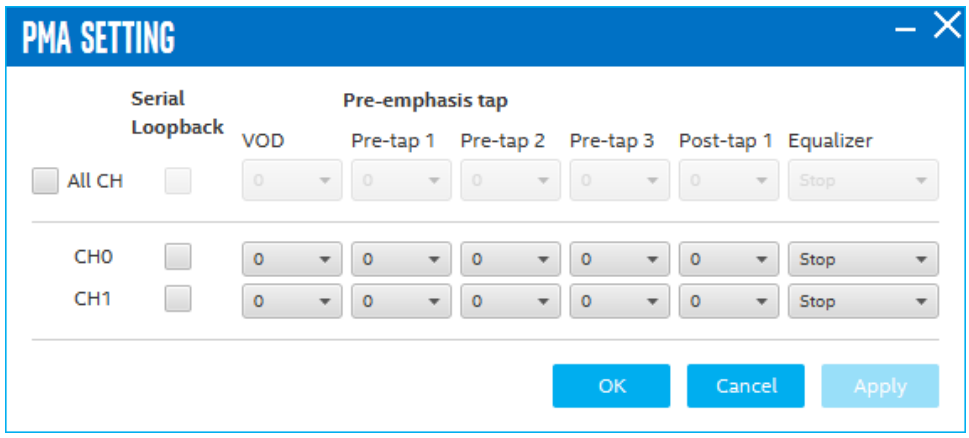
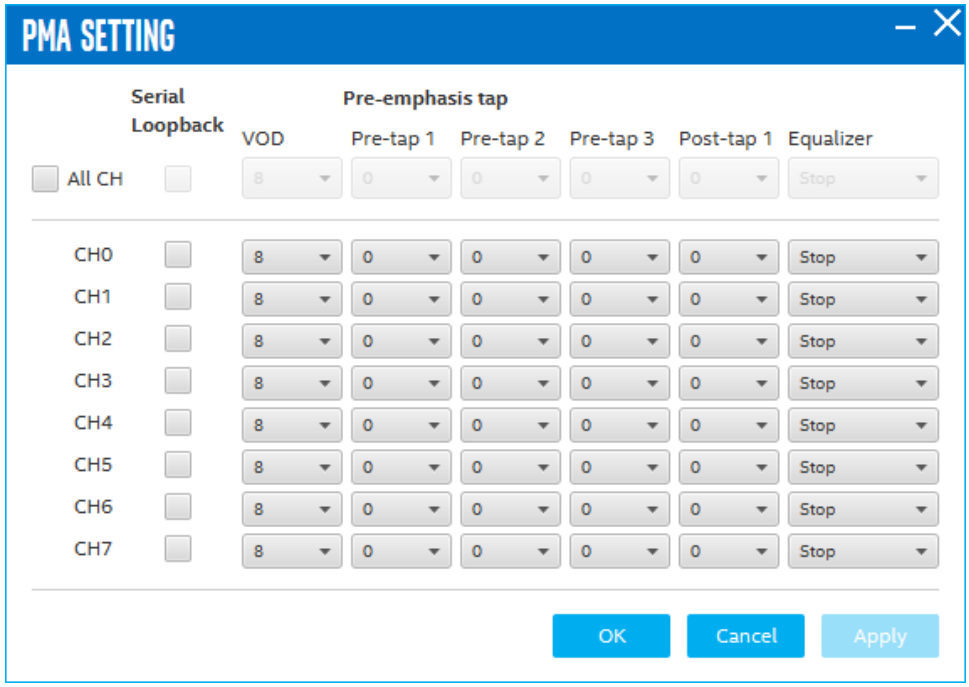


Figure 23. QSFPDD1X1 PMA Setting



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- **PRBS 7:** Selects pseudo-random 7-bit sequences.
- **PRBS 9:** Selects pseudo-random 9-bit sequences.
- **PRBS 11:** Selects pseudo-random 11-bit sequences.

- **PRBS 15:** Selects pseudo-random 15-bit sequences.
- **PRBS 23:** Selects pseudo-random 23-bit sequences.
- **PRBS 31:** Selects pseudo-random 31-bit sequences.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Displays the error rate of data transaction.
- **Insert:** Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- **Clear:** Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

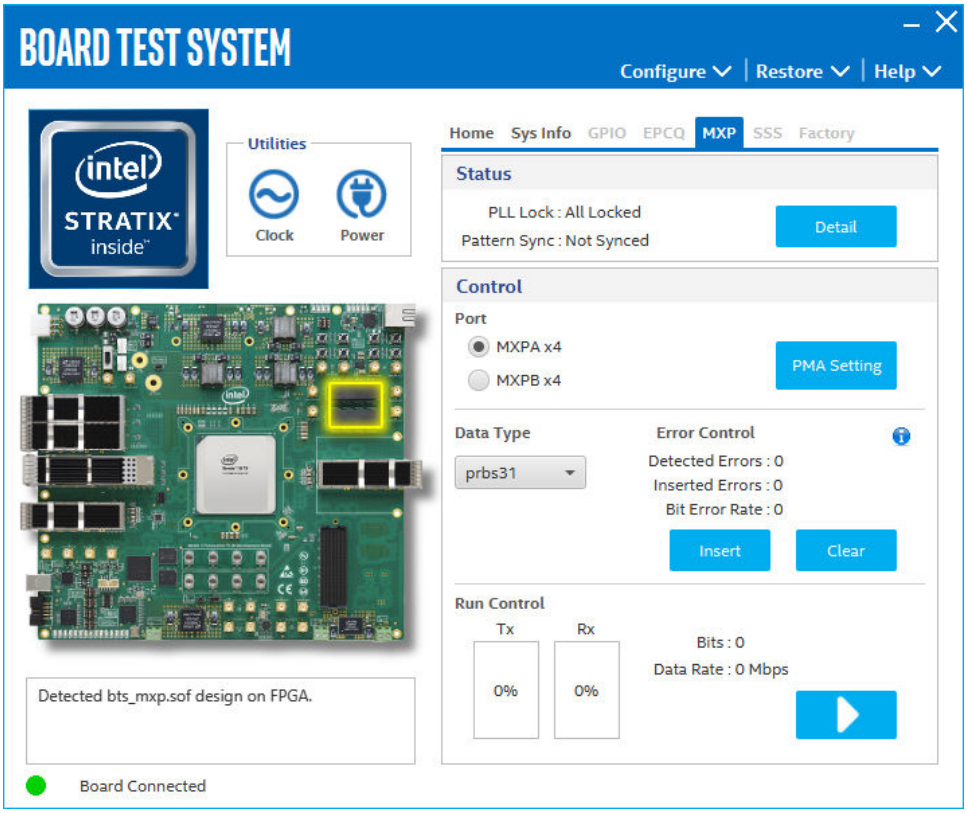
Start: This toggle button initiates and stops the tests.

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

5.3.7. The MXP Tab

The MXP tab allows you to perform loopback tests on the MXP port. Install MXP loopback modules for four MXP interfaces, configure FPGA with MXP image.

Figure 24. The MXP Tab

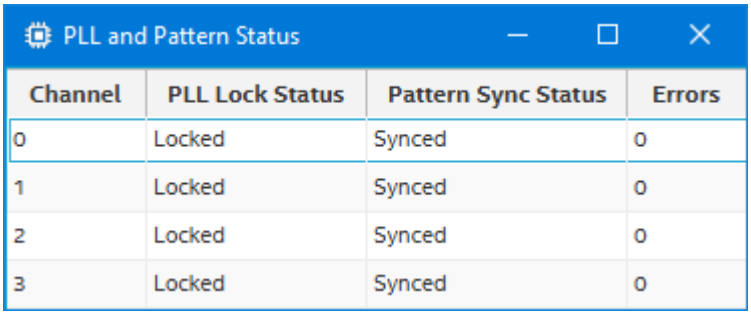


The following sections describe the controls on the MXP tab.

Status

Displays the following status information during a loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **Details:** Shows the details of PLL lock, pattern status and error bits of each channel.



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0

Port

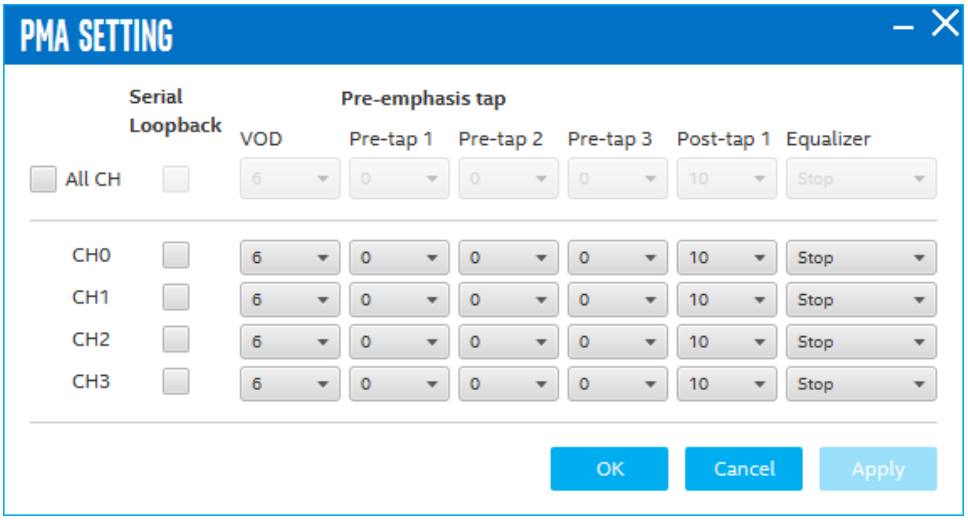
Allows you to specify which interface to test. The following port tests are available:

- MXPA
- MXPB

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- **PRBS 7:** Selects pseudo-random 7-bit sequences.
- **PRBS 15:** Selects pseudo-random 15-bit sequences.
- **PRBS 23:** Selects pseudo-random 23-bit sequences.

- **PRBS 31:** Selects pseudo-random 31-bit sequences.
- **HF:** Selects highest frequency divide-by-2 data pattern `10101010`.
- **LF:** Selects lowest frequency divide-by-33 data pattern

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- **Detected errors:** Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Displays the error rate of data transaction.
- **Insert:** Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- **Clear:** Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

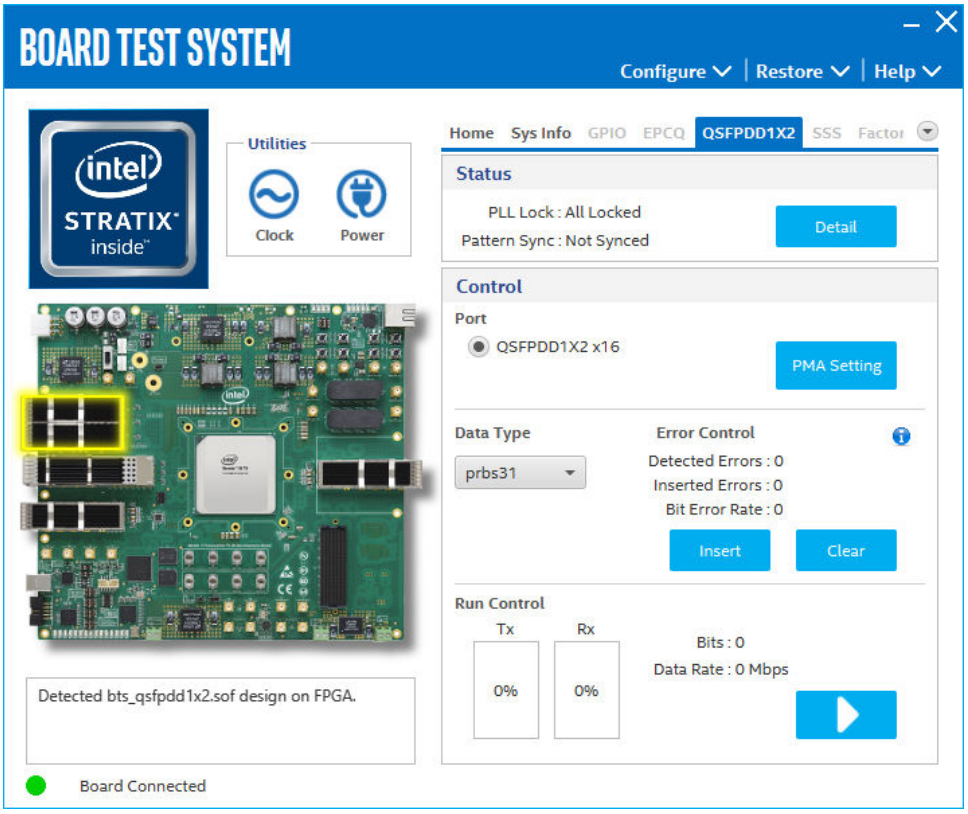
Start: This toggle button initiates and stops the tests.

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

5.3.8. The QSFPDD1x2 Tab

The QSFPDD1x2 tab allows you to perform loopback tests on the QSFPDD1x2 port. Install two QSFPDD loopback modules into QSFPDD1x2 interface, configure the FPGA with QSFPDD1x2 image.

Figure 25. The QSFPDD1x2 Tab



The following sections describe the controls on the QSFPDD1x2 tab.

Status

Displays the following status information during a loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **Details:** Shows the details of PLL lock, pattern status and error bits of each channel.

Figure 26. QSFPDD1X2 Status

PLL and Pattern Status

Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0

Port

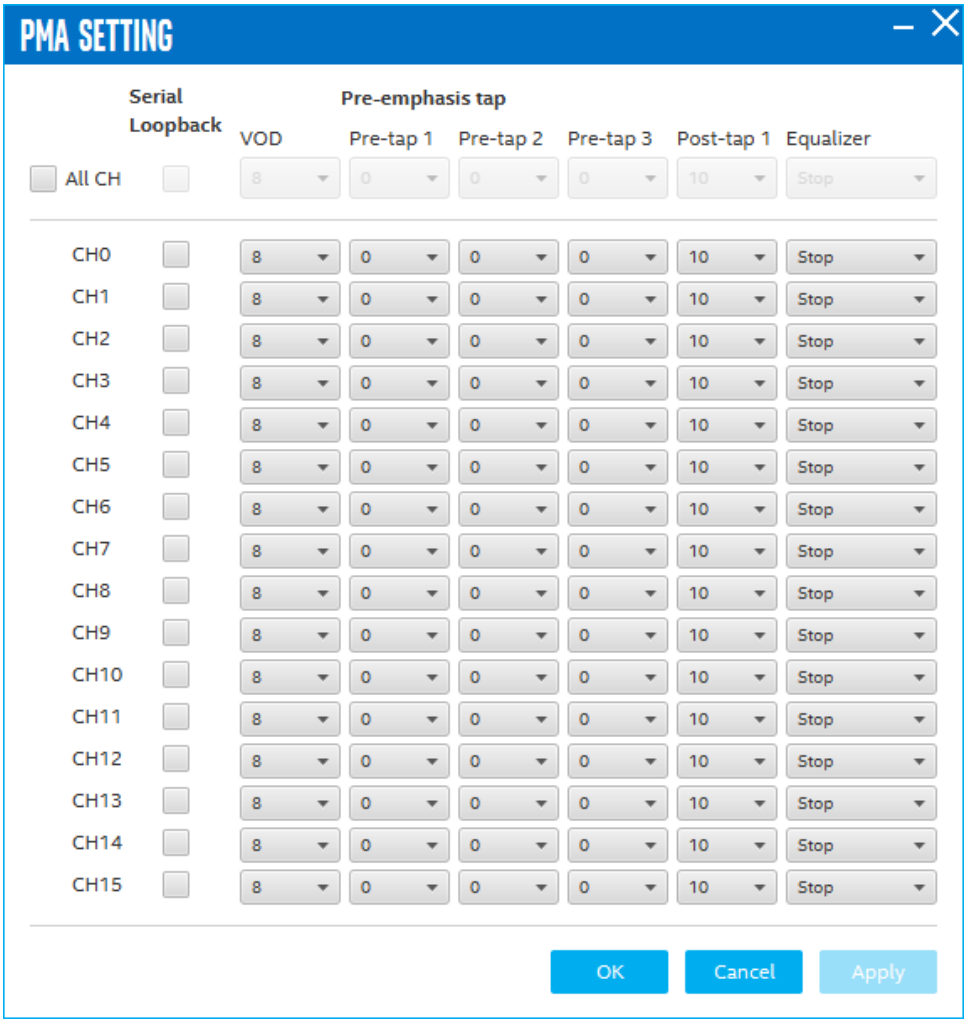
Allows you to specify which interface to test. The following port tests are available: QSFPDD1x2

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer.

Figure 27. QSFPDD1X2 PMA Setting



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- **PRBS 7:** Selects pseudo-random 7-bit sequences.
- **PRBS 15:** Selects pseudo-random 15-bit sequences.
- **PRBS 23:** Selects pseudo-random 23-bit sequences.
- **PRBS 31:** Selects pseudo-random 31-bit sequences.
- **HF:** Selects highest frequency divide-by-2 data pattern `10101010`.
- **LF:** Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- **Detected errors:** Displays the number of data errors detected in the hardware.
- **Inserted errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Displays the error rate of data transaction.
- **Insert:** Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- **Clear:** Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

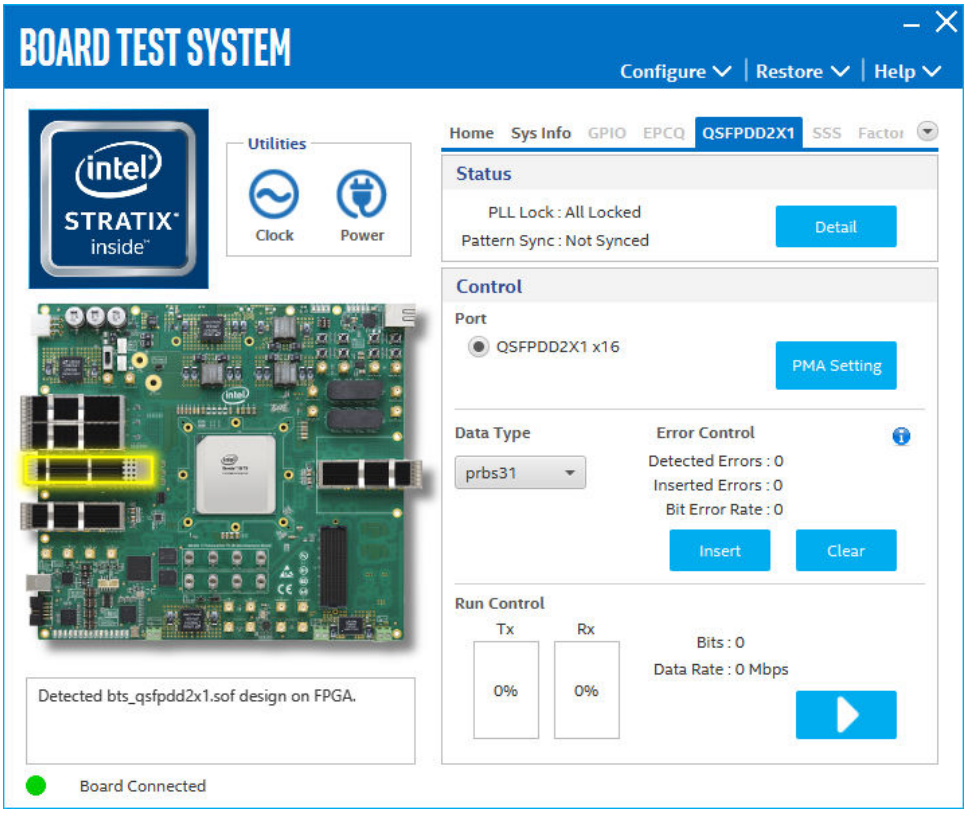
Start: This toggle button initiates and stops the tests.

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

5.3.9. The QSFPDD2x1 Tab

The QSFPDD2x1 Tab allows you to run transceivers QSFPDD2x1 loopback tests on your board. Install two QSFPDD loopback modules into QSFPDD2x1 interface, configure the FPGA with QSFPDD2x1 image.

Figure 28. The QSFPDD2x1 Tab



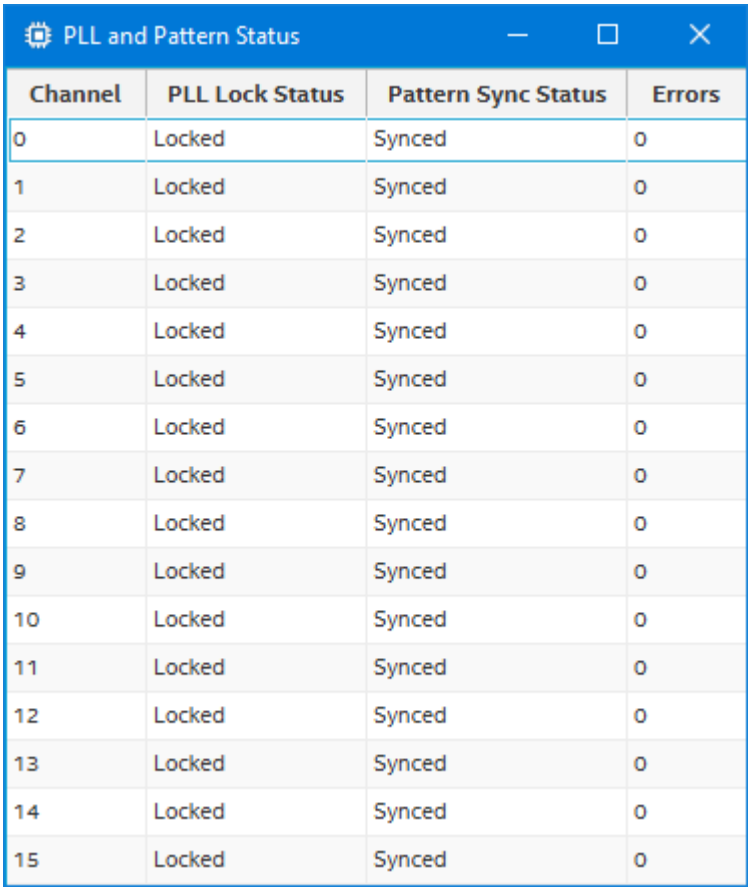
The following sections describe the controls on the QSFPDD2x1 tab.

Status

The Status control displays the following status information during the loopback test:

- **PLL lock:** Shows the PLL locked or unlocked state
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Details:** Shows the details of PLL lock, pattern status and error bits of each channel.

Figure 29. QSFPDD2X1 Status



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

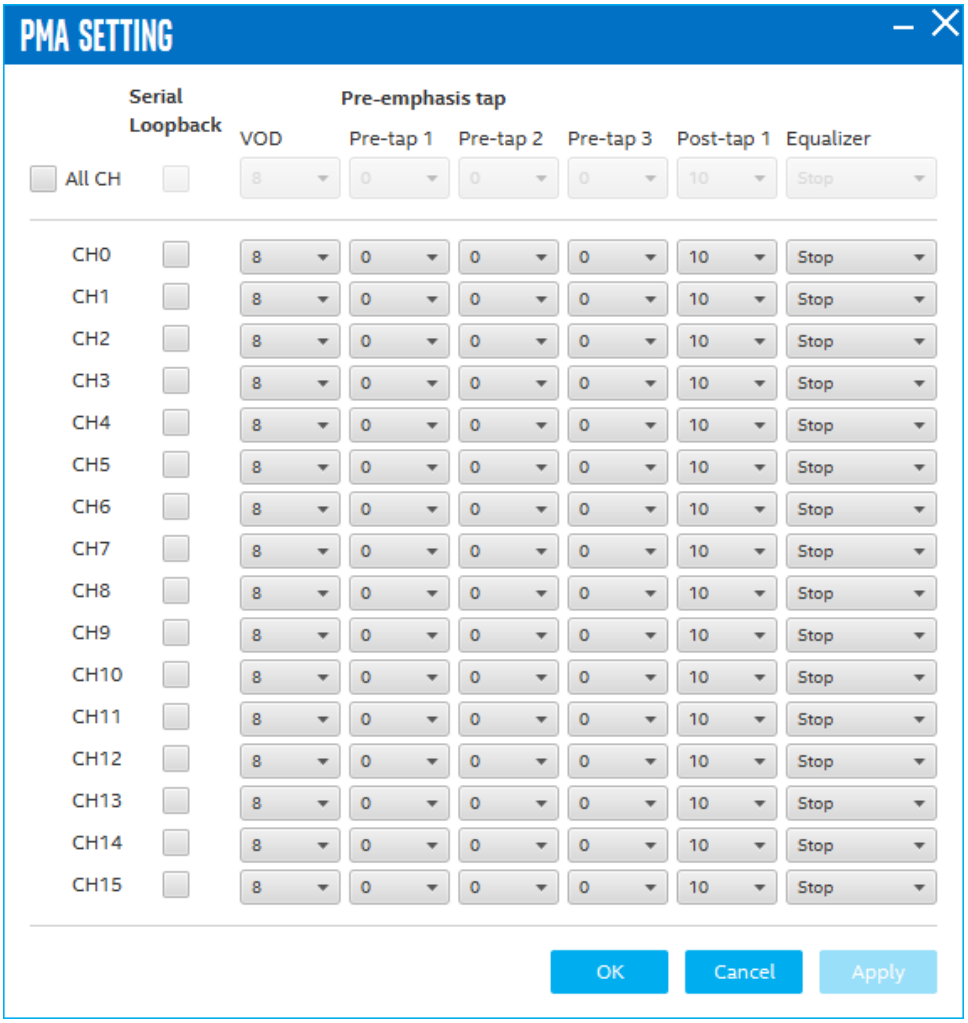
- QSFPDD2x1

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer.

Figure 30. QSFPDD2X1 PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7:** pseudo-random 7-bit sequences (default)
- **PRBS15:** pseudo-random 15-bit sequences
- **PRBS23:** pseudo-random 23-bit sequences
- **PRBS31:** pseudo-random 31-bit sequences
- **HF:** Selects highest frequency divide-by-2 data pattern `10101010`.
- **LF:** Selects lowest frequency divide-by-33 data pattern.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errrors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Displays the error rate of data transaction.
- **Insert Error:** Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This toggle button initiates and stops the tests.

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

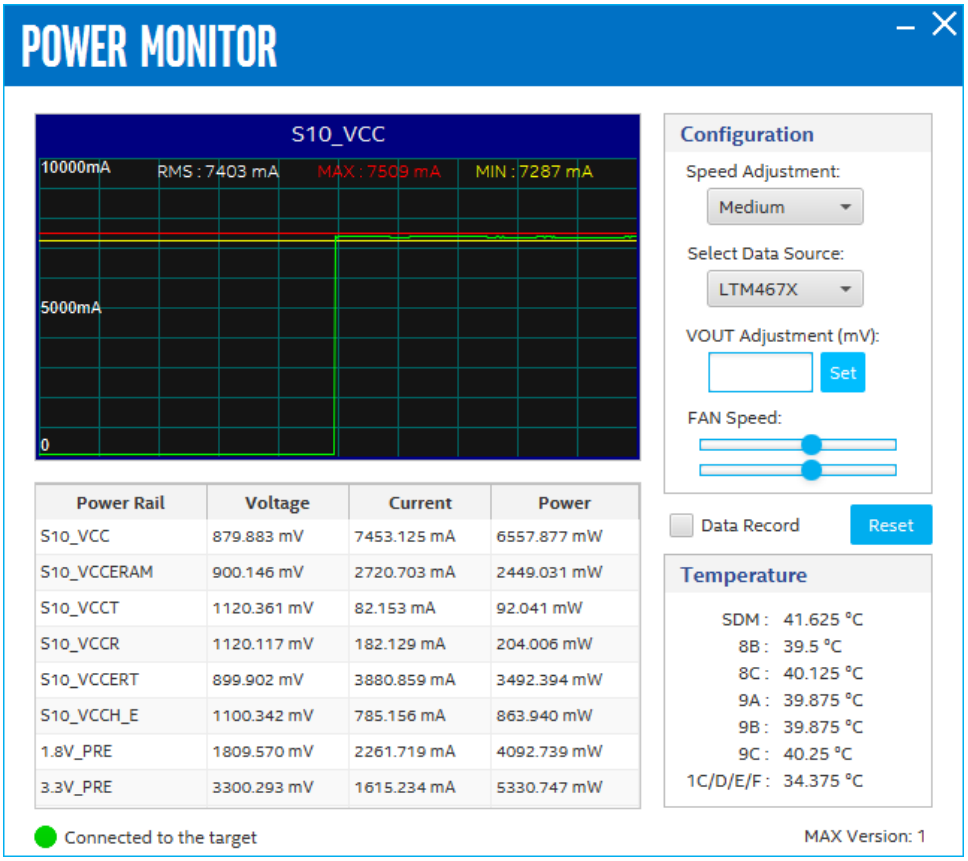
5.3.10. Power Monitor

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor cicruit attached to the device allows you to measure the power that the FPGA is consuming and trim voltage level.

To start the application, click the Power Monitor icon in the BTS. You can also run the Power Monitor as a stand-alone application. The `PowerMonitor.exe` resides in the `<package dir>\examples\board_test_system` directory.

Note: You cannot run the stand-alone power application and BTS at the same time. Also, you cannot run power and clock interface at the same time.

Figure 31. The Power Monitor



5.3.11. Clock Controller

The Clock Controller application sets the Si549 programmable oscillators to any frequency between 0.2 MHz and 800 MHz and sets the Si5341 PLL to any frequencies between 10 MHz and 750 MHz. The oscillator drives a 2-to-6 buffer that drives a copy of the clock to all transceiver blocks of the FPGA.

To start the application, click **Clock Controller** icon in the BTS. You can also run the Clock Controller as a stand-alone application.

The `ClockController.exe` resides in the `<package dir>\examples\board_test_system` directory.

The Clock Control communicates with the MAX V device on the board through the JTAG bus. The Si549 programmable oscillator and PLL are connected to the MAX V device through a 2-wire bus.

Figure 32. The Clock Controller - Si549

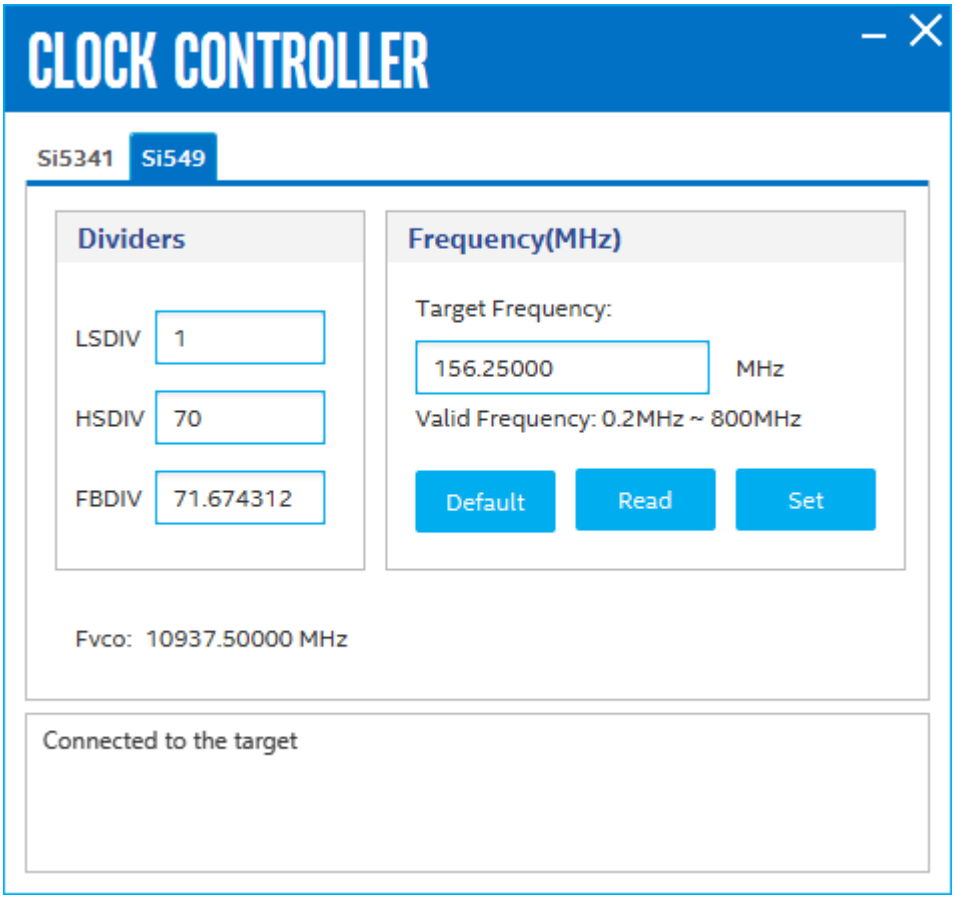
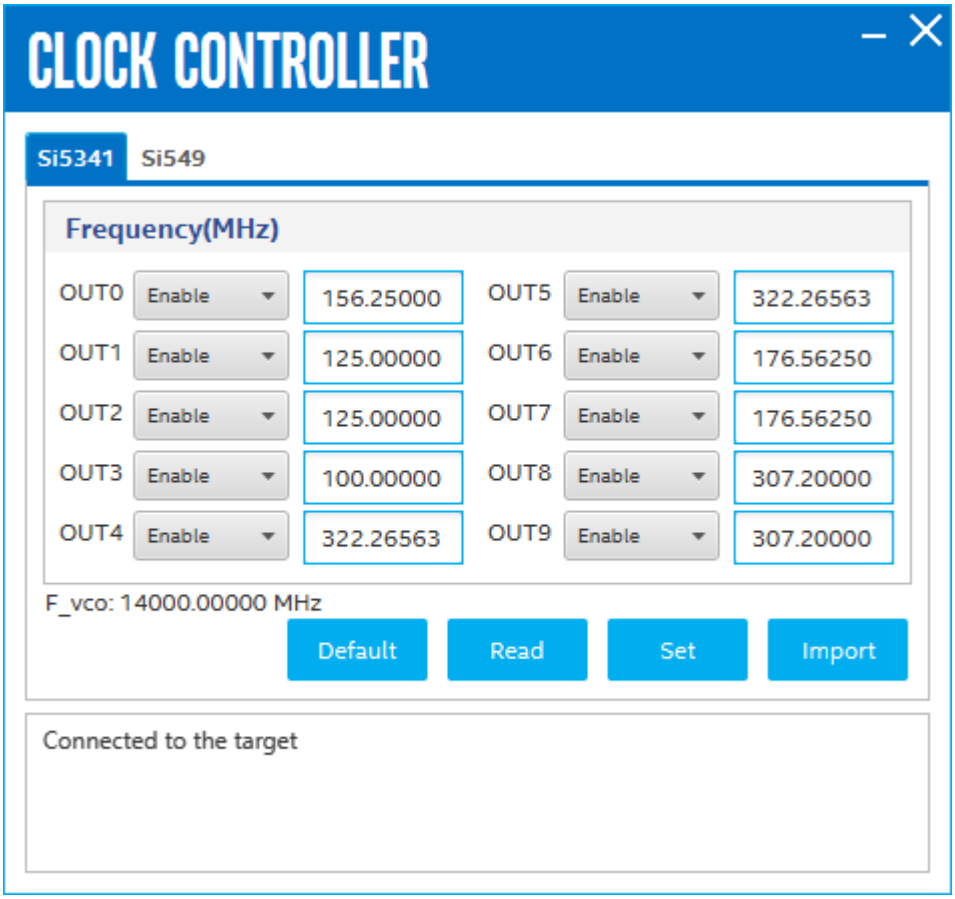


Figure 33. The Clock Controller - Si5341



The following sections describe the Clock Control controls.

Divider

The **Divider** control shows the current values from the Si549 registers.

Note: For more information about the Si549 registers, refer to the Si549 data sheet available on the Silicon Labs website (www.silabs.com).

F_{vco}

The **Fvco** control shows the calculated internal fixed-frequency crystal, based on the serial port register values.

Note: For more information about the F_{vco} value and how it is calculated, refer to the Si549 data sheet available on the Silicon Labs website (www.silabs.com)

Target Frequency

The **Target Frequency** control allows you to specify the frequency of the clock. Legal values are between 0.2 MHz and 800 MHz and select frequencies to 1400 MHz. For example, 421.31259873 is possible within 100 parts per million (ppm). The Target Frequency control works in conjunction with the **Set** Control.

Set

The **Set** control sets programmable oscillator or PLL frequency to the value in the Target frequency control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Note: Intel recommends resetting the FPGA logic after changing frequencies.

5.4. Simple Socket Server

The Intel Stratix 10 TX Transceiver Signal Integrity Development Kit ships with the Simple Socket Server design example stored in the factory portion of the EPCQL flash memory. The design consists of a Nios II embedded processor and an Ethernet MAC.

When you power up the board, the Intel Stratix 10 TX FPGA configures with the Simple Socket Server design example. The design can obtain an IP address from any DHCP server and serve a telnet server to any host computer on the same network. The telnet server allows you to control the LEDs on the board.

The source code for the Simple Socket Server design resides in the `<package dir>\examples\simple_socket_server` directory. If the Simple Socket Server is corrupted or deleted from the flash memory, you might need to restore the board's original contents, using the BTS application.

A. Additional Information

A.1. Add SmartVID settings in QSF file

Intel Stratix 10 FPGA silicon assembled on the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit enables SmartVID feature by default.

You may encounter the following error message when you switch from using the example design to your own design:

Error(19192): File <filename>.sof is incomplete - Power management settings are not set up appropriately on VID part"

To prevent Intel Quartus Prime from generating an error message due to incomplete SmartVID settings, you must put constraints listed below into the Intel Quartus Prime project QSF file.

Open your Intel Quartus Prime project QSF file, copy and paste the constraints listed below in the QSF file.

Before, you compile your project with correct SmartVID settings, ensure that there are no other similar settings with different values.

Constraints

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "400 KHZ"

set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 47

set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 48

set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00

set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS 00

set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS 00

set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS 00

set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS 00

set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS 00

set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON

set_global_assignment -name USE_PWRMGT_SCL SDM_IO14

set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
```

```
set_global_assignment -name USE_PWRMGT_ALERT SDM_IO12

set_global_assignment -name USE_CONF_DONE SDM_IO16

set_global_assignment -name USE_INIT_DONE SDM_IO0

set_global_assignment -name USE_CVP_CONFDONE SDM_IO15

set_global_assignment -name USE_SEU_ERROR SDM_IO13
```

The Intel Stratix 10 device family offers SmartVID standard power devices in all speed grades. Lower power fixed-voltage devices are also available in all speed grades except for the fastest speed grade. Please refer to *Intel Stratix 10 Power Management User Guide* for additional information.

Related Information

Intel Stratix 10 Power Management User Guide

A.2. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

A.2.1. Safety Warnings

Power Supply Hazardous Voltage

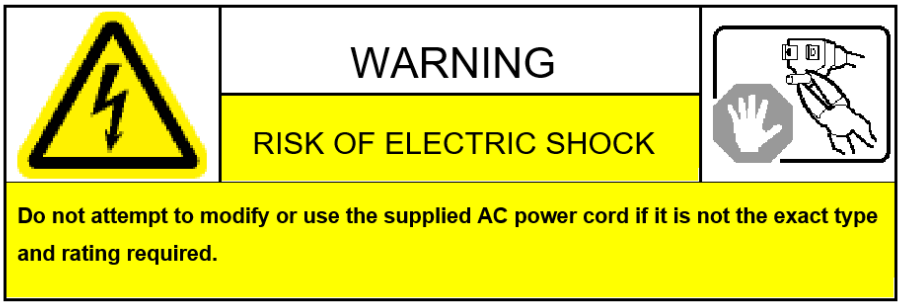
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

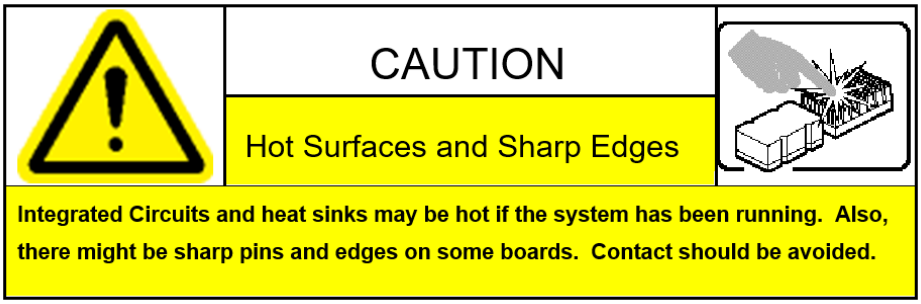
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

A.2.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the isde, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interfence to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obatined.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: **Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.**

Ecology Conformance Marking for WEEE and China RoHS

A.3. Compliance and Conformity Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

CE

B. Revision History

Table 22. Revision History of the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit User Guide

Document Version	Changes
2019.09.27	Added Add SmartVID settings in QSF file on page 72 OSFP no longer supported. Removed all references. Updated the following sections: • General Development Kit Description on page 4 • About the Intel Quartus® Prime Software on page 7 • Installing the Intel FPGA Download Cable II Driver on page 8 • Factory Default Switch and Jumper Settings on page 10 • Development Kit Overview on page 12 • Intel Stratix 10 TX FPGA on page 14 • MAX V CPLD on page 18 • Transceiver Dedicated Clocks on page 28 • Transceiver Channels on page 30 • Power Supply on page 35 • Power Distribution System on page 37 • Thermal Limitations and Protection Guidelines on page 38 • Board Test System on page 40 • The System Info Tab on page 43 • The GPIO Tab on page 44 • The EPCQ Tab on page 45 • The FMC+ Tab on page 47 • The PAM4 Tab on page 52 • The MXP Tab on page 56 • The QSFPDD1x2 Tab on page 59 • The QSFPDD2x1 Tab on page 63 • Power Monitor on page 67 • Clock Controller on page 68
2019.03.06	Updated supported NRZ data rate.
2018.10.08	Engineering Silicon (ES) Release.

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