



Cyclone IV GX FPGA Development Kit

User Guide



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The Altera® Cyclone® IV GX FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Cyclone IV GX FPGA designs. The PCI-SIG-compliant board, high-speed mezzanine card (HSMC), and the license-free Quartus® II Web Edition software provide everything you need to begin developing custom Cyclone IV GX FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (up to 3.125 Gbps)
- Develop embedded designs utilizing the Nios® II processor and the SSRAM memory
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 30 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO®, 10 Gigabit Ethernet, SONET, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI) and others
- Develop FPGAs design for cost-sensitive applications and volume production
- Measure the FPGA's low power consumption

Kit Features

This section briefly describes the Cyclone IV GX FPGA Development Kit contents.

Hardware

The Cyclone IV GX FPGA Development Kit includes the following hardware:


- Cyclone IV GX FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone IV GX EP4CGX150DF31 FPGA.
 - For detailed information about the board components and interfaces, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*.
- HSMC loopback board—A daughtercard that allows for loopback testing all signals on the HSMC interface using the Board Test System.
- HSMC debug breakout board—A daughtercard that routes 40 CMOS signals to a 0.1" header and adds 20 LEDs to the remaining 40 CMOS signals.
- Power supply and cables—The kit includes the following items:
 - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
 - USB cable
 - Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Web Edition Software

The Quartus II Web Edition Software is a license-free set of Altera tools with limited functionality.


-  Download the Quartus II Web Edition Software from the [Quartus II Web Edition Software](#) page of the Altera website. Alternatively, you can request a DVD from the [Altera IP and Software DVD Request Form](#) page of the Altera website.

The Quartus II Web Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.

-  To compare the Quartus II subscription and web editions, refer to [Altera Quartus II Software — Subscription Edition vs. Web Edition](#). The kit also works in conjunction with the subscription edition.

- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
 - Simulate behavior of a MegaCore function within your system.
 - Verify functionality of your design, and quickly and easily evaluate its size and speed.
 - Generate time-limited device programming files for designs that include MegaCore functions.
 - Program a device and verify your design in hardware.

-  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

-  For more information about OpenCore Plus, refer to [AN 320: OpenCore Plus Evaluation of Megafunctions](#).

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Cyclone IV GX FPGA Development Kit Installer

The license-free Cyclone IV GX FPGA Development Kit installer includes all the documentation and design examples for the kit.

Download the Cyclone IV GX FPGA Development Kit installer from the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website. Alternatively, you can request a development kit DVD from the [Altera Kit Installations DVD Request Form](#) page of the Altera website.

The remaining chapters in this user guide lead you through the following Cyclone IV GX FPGA development board with the HSMC daughtercard setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Cyclone IV GX FPGA
- Running the Board Test System designs



For complete information about the FPGA development board, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in “[Kit Features](#)” on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.



Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.



In typical applications with the Cyclone IV GX FPGA development board, a fan/heat sink is not necessary. However, under extreme conditions the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA temperature in real time, refer to “[The Power Monitor](#)” on page 6–15.



For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the [Cyclone IV GX FPGA Development Kit](#) page.
- For additional daughter cards available for purchase, refer to the [Development Board Daughtercards](#) page.
- For the Cyclone IV GX device documentation, refer to the [Literature: Cyclone IV Devices](#) page.
- To purchase devices from the eStore, refer to the [Devices](#) page.
- For Cyclone IV GX OrCAD symbols, refer to the [Capture CIS Symbols](#) page.
- For Nios II 32-bit embedded processor solutions, refer to the [Embedded Processing](#) page.

This chapter explains how to install the following software:

- Quartus II Web Edition Software
- Cyclone IV GX FPGA Development Kit
- USB-Blaster™ driver

Installing the Quartus II Web Edition Software

The Quartus II Web Edition Software provides the necessary tools used for developing hardware and software for Altera FPGAs. Included in the Quartus II Web Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Web Edition Software installer you acquired in “Software” on page 1–2.
2. Follow the on-screen instructions to complete the installation process.



If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing*.

Licensing Considerations

The Quartus II Web Edition Software is license-free and supports Cyclone IV GX devices without any additional licensing requirement. This kit also works in conjunction with the Quartus II Subscription Edition Software, once you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.

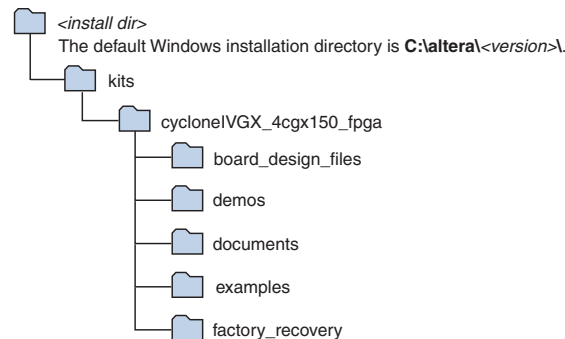
Installing the Cyclone IV GX FPGA Development Kit

To install the Cyclone IV GX FPGA Development Kit, perform the following steps:

1. Run the Cyclone IV GX FPGA Development Kit installer you acquired in “Software” on page 1–2.
2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to your Quartus II software as the default locations.

The installation program creates the Cyclone IV GX FPGA Development Kit directory structure shown in [Figure 3-1](#).

Figure 3-1. Cyclone IV GX FPGA Development Kit Installed Directory Structure



[Table 3-1](#) lists the file directory names and a description of their contents.

Table 3-1. Installed Directory Contents

| Directory Name | Description of Contents |
|---------------------------|--|
| board_design_files | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| demos | Contains demonstration applications. |
| documents | Contains the kit documentation. |
| examples | Contains the sample design files for the Cyclone IV GX FPGA Development Kit. |
| factory_recovery | Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents. |

Installing the USB-Blaster Driver

The Cyclone IV GX FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

- Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the [Altera Programming Cable Driver Information](#) page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

The instructions in this chapter explain how to set up the Cyclone IV GX FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Cyclone IV GX FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in [“Factory Default Switch Settings” on page 4-2](#) to return the board to its factory settings before proceeding.
2. The FPGA development board ships with design examples stored in the flash memory device. Verify the USER_FACTORY switch (SW1.1) is set to the off position to load the design stored in the factory portion of flash memory. [Table 4-1](#) shows the switch locations on the Cyclone IV GX FPGA development board.
3. Connect the DC adapter (16 V, 60 W) to the DC power jack (J5) on the FPGA board and plug the cord into a power outlet.



Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW3) to the on position. When power is supplied to the board, a blue LED (D11) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The USER_FACTORY switch (SW1.1) controls which design to load. When the switch is in the off position, the PFL loads the design from the factory portion of flash memory. When the switch is in the on position, the PFL loads the design from the user hardware portion of flash memory.



The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the
`<install_dir>\kits\cycloneIVGX_4cgx150_fpga\examples\max2` directory.

When configuration is complete, the CONF DN LED illuminates, signaling that the Cyclone IV GX device configured successfully.

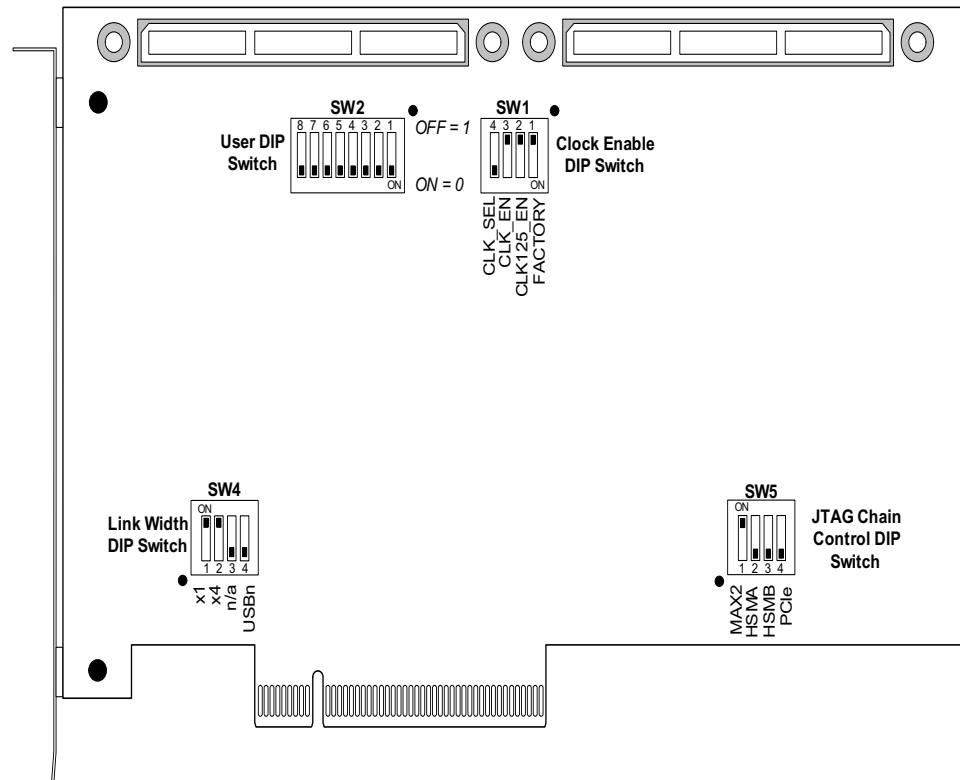


For more information about the PFL megafunction, refer to [AN 386: Using the Parallel Flash Loader with the Quartus II Software](#).

Factory Default Switch Settings

This section shows the factory switch settings for the Cyclone IV GX FPGA development board. [Figure 4-1](#) shows the switch locations and the default position of each switch on the top side of the board.

Figure 4-1. Switch Locations and Default Settings



To restore the switches to their factory default settings, perform these steps:

1. Set DIP switch bank (SW1) to match [Table 4-1](#) and [Figure 4-1](#).

Table 4-1. SW1 Dip Switch Settings (Part 1 of 2)

| Switch | Board Label | Function | Default Position |
|--------|--------------|--|------------------|
| 1 | USER_FACTORY | Switch 1 has the following options: <ul style="list-style-type: none"> ■ When on (0), the user file is loaded from flash at power-up ■ When off (1), the factory file is loaded from flash at power-up | Off |
| 2 | CLK125_EN | Switch 2 has the following options: <ul style="list-style-type: none"> ■ When on (0), the 125 MHz Oscillator is disabled ■ When off (1), the 125 MHz Oscillator is enabled | Off |

Table 4–1. SW1 Dip Switch Settings (Part 2 of 2)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 3 | CLKA_EN | Switch 3 has the following options: <ul style="list-style-type: none"> ■ When on (0), the 100 MHz Programmable Oscillator is disabled ■ When off (1), the 100 MHz Programmable Oscillator is enabled | Off |
| 4 | CLKA_SEL | Switch 4 has the following options: <ul style="list-style-type: none"> ■ When on (0), the OSC source is driven to the FPGA ■ When off (1), the SMA input source is driven to the FPGA | On |

- Set DIP switch bank (SW4) to match [Table 4–2](#) and [Figure 4–1](#).

Table 4–2. SW4 Dip Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|------------------|---|------------------|
| 1 | PCIE_PRSENT2n_x1 | Switch 1 has the following options: <ul style="list-style-type: none"> ■ When on, 0=x1 Presence Detect Enabled ■ When off, 1=x1 Presence Detect Disabled | On |
| 2 | PCIE_PRSENT2n_x4 | Switch 2 has the following options: <ul style="list-style-type: none"> ■ When on, 0=x4 Presence Detect Enabled ■ When off, 1=x4 Presence Detect Disabled | On |
| 3 | — | — | — |
| 4 | USB_DISABLEn | Switch 4 has the following options: <ul style="list-style-type: none"> ■ When on, 0=Embedded Blaster Disabled ■ When off, 1=Embedded Blaster Enabled | Off |

- Set DIP switch bank (SW5) to match [Table 4–3](#) and [Figure 4–1](#).

Table 4–3. SW5 Dip Switch Settings (JTAG)

| Switch | Board Label | Function | Default Position |
|--------|-----------------|--|------------------|
| 1 | EPM2210_JTAG_EN | Switch 1 has the following options: <ul style="list-style-type: none"> ■ When on (0), the MAX II device is included in the JTAG chain. ■ When off (1), the MAX II device is not included in the JTAG chain. | On |
| 2 | HSMA_JTAG_EN | Switch 2 has the following options: <ul style="list-style-type: none"> ■ When on (0), HSMA is included in the JTAG chain. ■ When off (1), HSMA is not included in the JTAG chain. | Off |
| 3 | HSMB_JTAG_EN | Switch 3 has the following options: <ul style="list-style-type: none"> ■ When on (0), HSMB is included in the JTAG chain. ■ When off (1), HSMB is not included in the JTAG chain. | Off |
| 4 | PCIE_JTAG_EN | Switch 4 has the following options: <ul style="list-style-type: none"> ■ When on (0), PCI Express is included in the JTAG chain. ■ When off (1), PCI Express is not included in the JTAG chain. | Off |



For more information about the FPGA board settings, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*.

The Cyclone IV GX FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the USER_FACTORY switch (SW1.1) in the off position, the Cyclone IV GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.



After successfully updating the user hardware flash memory, you can load the user design from flash memory into the FPGA. To do so, set the USER_FACTORY switch (SW1.1) to the on position and power cycle the board.

The source code for the Board Update Portal design resides in the `<install_dir>\kits\cycloneIVGX_4cgx150_fpga\examples` directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to [“Restoring the Flash Device to the Factory Settings” on page A-4](#) to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.



Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, set the USER_FACTORY switch (SW1.1) to the off position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

5. Click Cyclone IV GX FPGA Development Kit on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.



You can also navigate directly to the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware portion of flash memory. Designs must be in the Nios II Flash Programmer File (.flash) format.



Design files available from the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website include .flash files. You can also create .flash files from your own custom design. Refer to [“Preparing Design Files for Flash Programming” on page A-2](#) for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in [“Connecting to the Board Update Portal Web Page”](#) to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the .flash file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the USER_FACTORY switch (SW1.1) to the on position and power cycle the board, or press the PGM_SEL button (S2) until the user LED is on, and then press the PGM_LOAD button.
5. As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in [“Restoring the Flash Device to the Factory Settings” on page A-4](#).

The kit includes a design example and application called the Board Test System to test the functionality of the Cyclone IV GX FPGA development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in [“Installing the Cyclone IV GX FPGA Development Kit” on page 3–1](#).

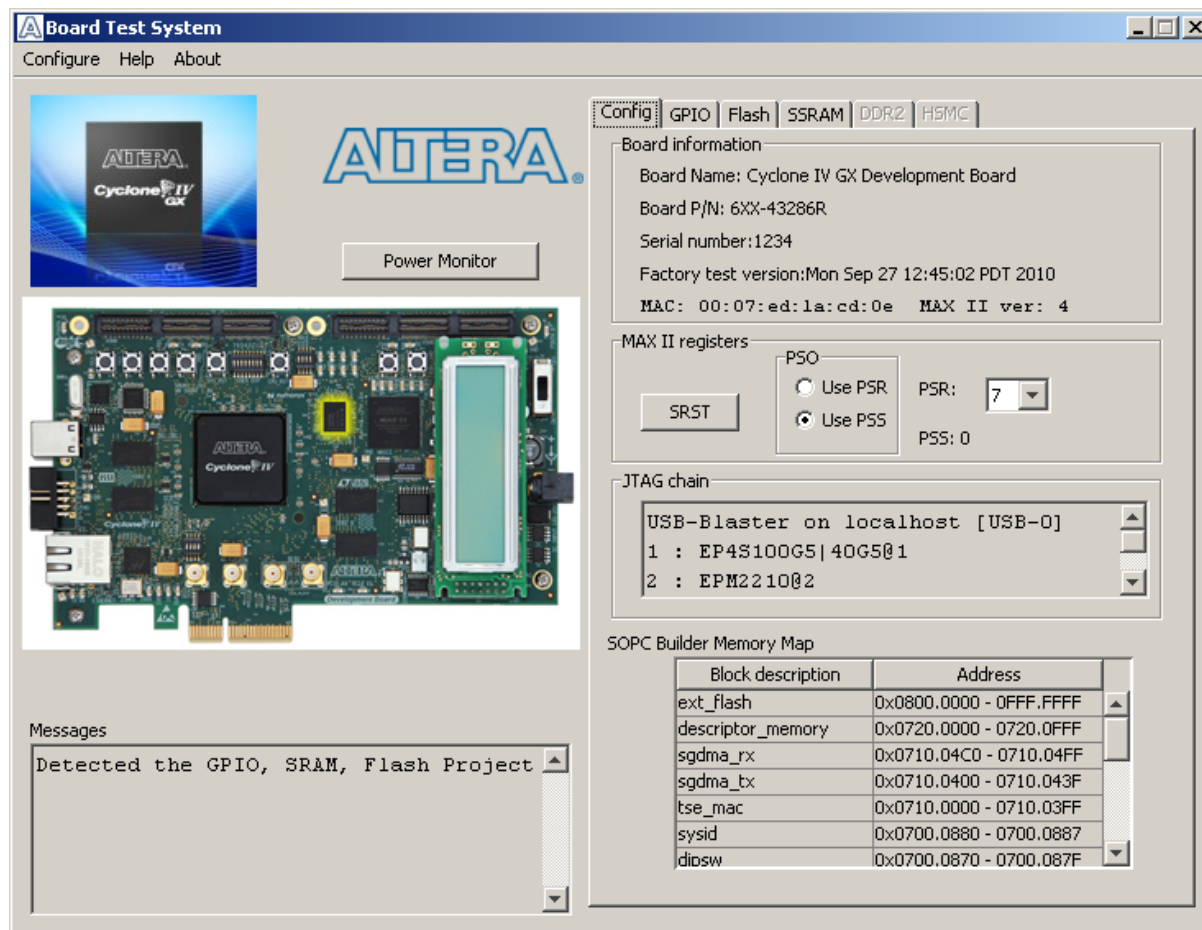
The application provides access to the following Cyclone IV GX FPGA development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- DDR2
- Two HSMC connectors
- Character LCD
- Ethernet
- Programmable oscillator
- Transceivers
- PCIe

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC that communicates over the JTAG bus to a test design running in the Cyclone IV GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.



The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switch banks match “[Factory Default Switch Settings](#)” on page 4–2.
3. Set the USER_FACTORY switch (SW1.1) to the on position.
4. Turn the power to the board on. The board loads the design stored in the user hardware portion of flash memory into the FPGA.



To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the `<install directs>\cycloneIVGX_4cgx150_fpga\examples\board_test_system` directory and run the **BoardTestSystem.exe** application.



On Windows, click **Start > All Programs > Altera > Cyclone IV GX FPGA Development Kit <version> > Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Cyclone IV GX FPGA development board’s flash memory ships preconfigured with the design that corresponds to the appropriate tabs.



If you power up your board with the USER_FACTORY switch (SW1.1) in the off position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to “[The Configure Menu](#)” for information about configuring your board.

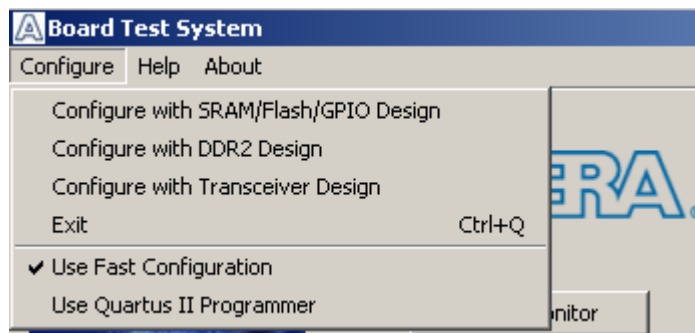
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. [Figure 6-2](#) shows the Configure menu.

Figure 6-2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design enable.

The Config Tab

The **Config** tab shows information about the board's current configuration. [Figure 6-1 on page 6-2](#) shows the **Config** tab. The tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **Config** tab.

Board Information

The **Board information** controls display static information about your board.

- **Name**—Indicates the official name of the board, given by the Board Test System.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System used to test this board originally.
- **Factory test date**—Indicates the date this board was test originally.

- **MAX II ver**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the `<install dir>\kits\cycloneIVGX_4cgx150_fpga\examples\max2` directory. Newer revisions of this code might be available on the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website.
- **MAC**—Indicates the MAC address of the board's Ethernet port.


MAX II Registers

This control allows you to view and change the current MAX II register values as described in [Table 6-1](#). Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6-1. MAX II Registers


| Register Name | Read/Write Capability | Description |
|----------------------------|-----------------------|---|
| System Reset (SRST) | Write only | Set to 0 to initiate an FPGA reconfiguration. |
| Page Select Register (PSR) | Read / Write | Determines which of the pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured. |
| Page Select Override (PSO) | Read / Write | When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration. |
| Page Select Switch (PSS) | Read only | Holds the current value of the flash page selected by pressing PGM_SEL pushbutton with status being displayed by the following LEDs: <ul style="list-style-type: none"> ■ EPCS LED = D19 illuminated. ■ USER LED = D20 illuminated. This is "User hardware 1" as shown on the flash memory map. ■ FACTORY LED = D21 illuminated (default). |

- **PSO**—Sets the MAX II PSO register. The following options are available:
 - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
 - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to [Table 6-1](#) for more information.
- **PSS**—Displays the MAX II PSS register value. Refer to [Table 6-1](#) for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to [Table 6-1](#) for more information.

 Because the **Config** tab requires that a specific design is running in the FPGA, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Cyclone IV GX device is always the first device in the chain.

 Setting DIP switch SW5.1 to the on position includes the MAX II device in the JTAG chain.

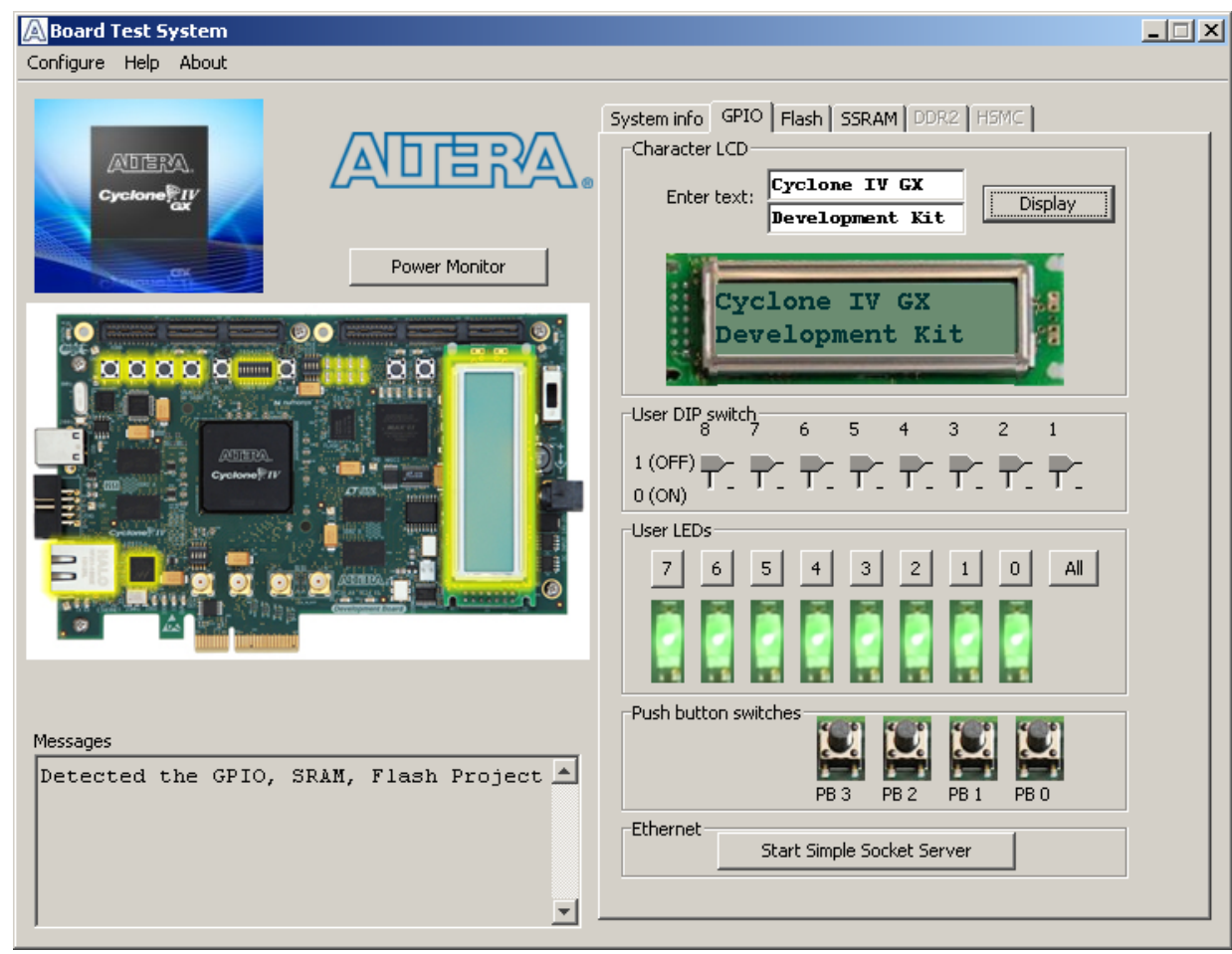
SOPC Builder Memory Map

This control shows the memory map of the FPGA design's SOPC Builder system.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the LCD, turn LEDs on or off, and detect push button presses. [Figure 6-3](#) shows the **GPIO** tab.

Figure 6-3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

Allows you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.



If you exceed the 16 character display limit on either line, a warning message appears.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Click the **LED** buttons to turn the board LEDs on and off.

Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

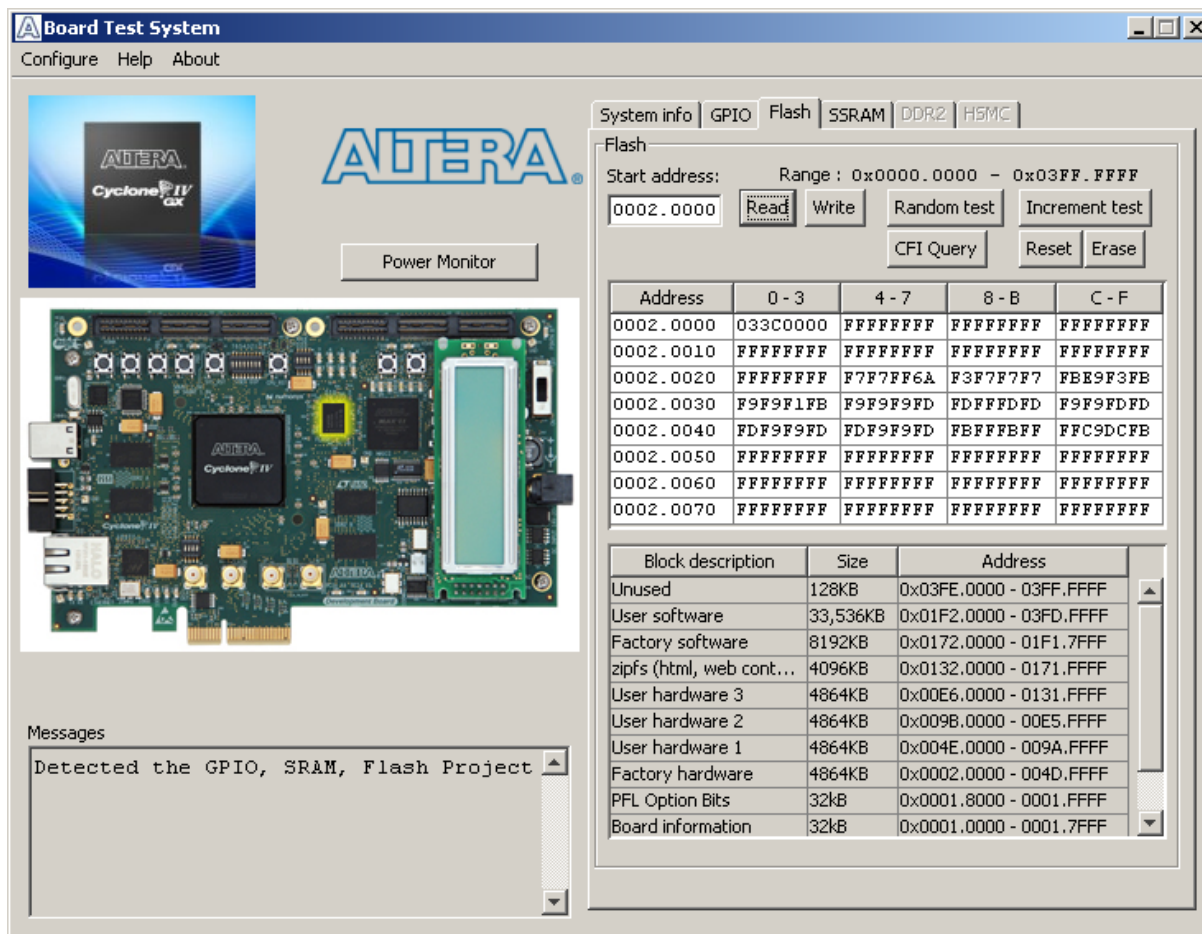
Ethernet

Click **Start Simple Socket Server** to run the `simple_socket_server.elf` program that was downloaded into FPGA during configuration.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6-4 shows the **Flash** tab.

Figure 6-4. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory addresses display in the format the Nios II processor within the FPGA uses, that is, each flash memory address is offset by 0x08000000. Thus, the first location in flash memory appears as 0x08000000 in the GUI.



If you enter an address outside of the 0x08000000 to 0x08FFFFFF flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.



To prevent overwriting the dedicated portions of flash memory, the application limits the writable flash memory address range to 0x08FE0000 to 0x08FFFFFF (which corresponds to address range 0x00FE0000 - 0x00FFFFFF in the uppermost portion of the user software memory block, as shown in [Figure 6-1 on page 6-2](#) and [Table A-1 on page A-1](#)).

Random Test

Starts a random data pattern test to flash memory. Limited to scratch page in the upper 128K block.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory. Limited to scratch page in the upper 128K block.

Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory. Limited to scratch page upper 128K blocks.

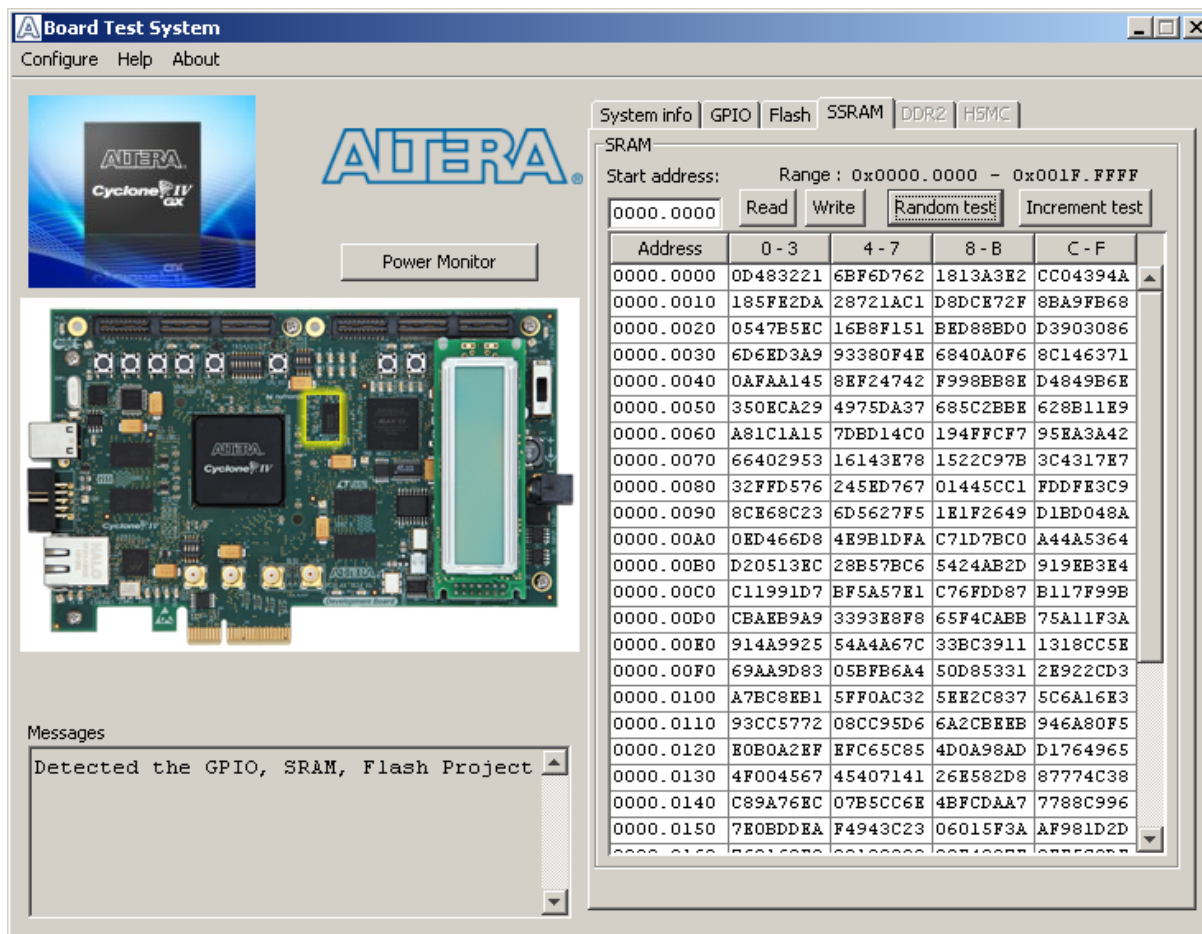
Flash Memory Map

Displays the flash memory map for the Cyclone IV GX FPGA Development Kit.

The SSRAM Tab

The **SSRAM** tab allows you to read and write SRAM and flash memory on your board. Figure 6-5 shows the **SSRAM** tab.

Figure 6-5. The SSRAM Tab



The following sections describe the controls on the **SSRAM** tab.

Read

The **Read** control reads the SSRAM on your board. To see the SSRAM contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The SSRAM addresses display in the format the Nios II processor within the FPGA uses, that is, each SSRAM address is offset by 0x00200000. Thus, the first location in SSRAM appears as 0x00200000 in the GUI.



If you enter an address outside of the 0x00200000 to 0x003FFFFFFF SSRAM address space, a warning message identifies the valid SSRAM address range.

Write

The **Write** control writes the SSRAM on your board. To update the SSRAM contents, change values in the table and click **Write**. The application writes the new values to SSRAM and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Random Test

Starts an random data pattern test to flash memory.

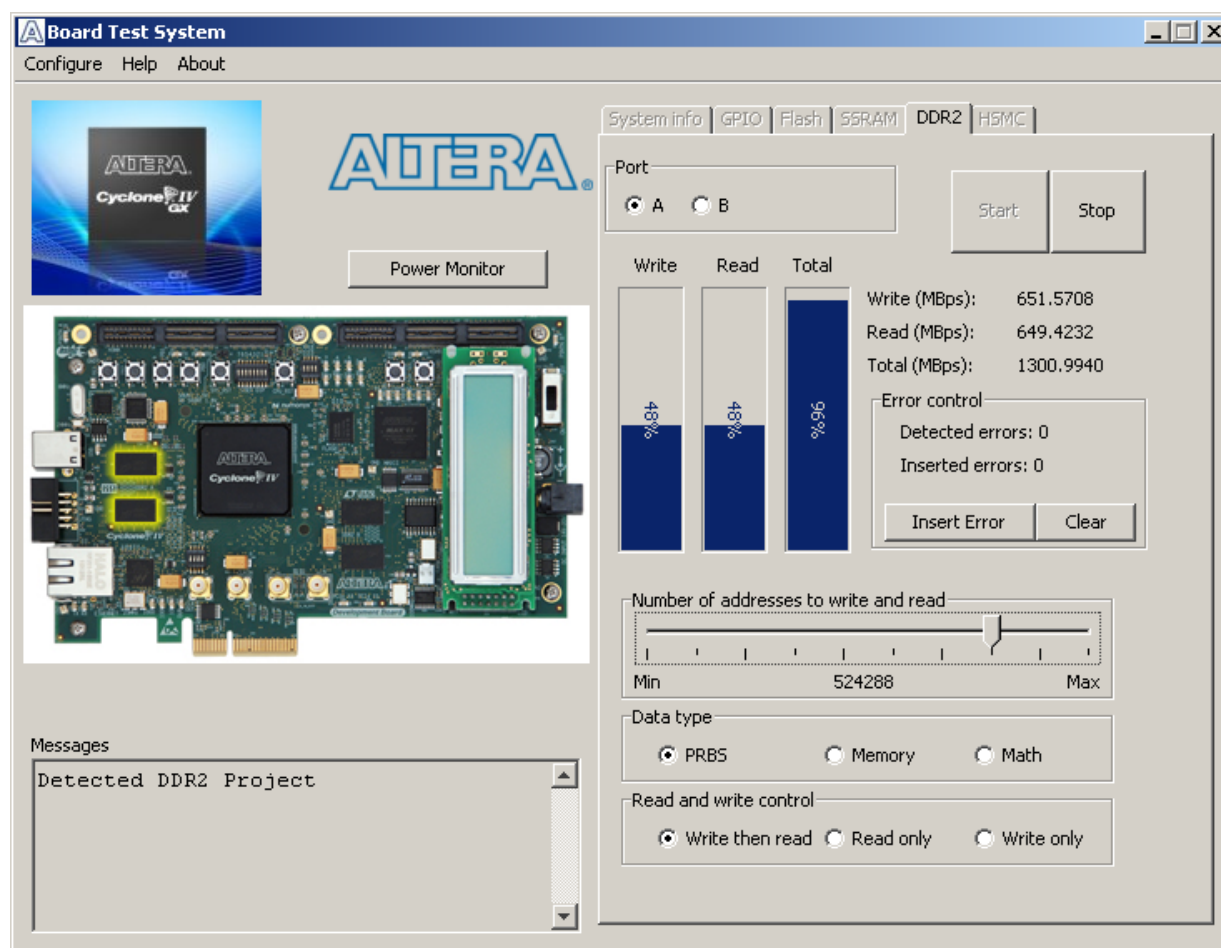
Incrementing Test

Starts an incrementing data pattern test to flash memory.

The DDR2 Tab

The **DDR2** tab allows you to read and write the DDR2 memory on your board. [Figure 6-6](#) shows the **DDR2** tab.

Figure 6-6. The DDR2 Tab



The following sections describe the controls on the **DDR2** tab.

Port

The **Port** control directs communication to one of two DDR2 memory ports on your board. Each interface is 32 bits wide. Since there are two DDR2 ports on the Cyclone IV GX FPGA development board, the DDR2 tab has 2 radio buttons to monitor each DDR2 interface.

Start

The **Start** control initiates DDR2 memory transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read, and Total** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps), and Total (MBps)**—Show the number of bytes of data analyzed per second. Each data bus is 32 bits wide and the frequency is 167 MHz double data rate (333 Mbps per pin), equating to a theoretical maximum bandwidth of 1332 MBps.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Number of Addresses to Write and Read

The **Number of addresses to write and read** control determines the number of addresses to use in each iteration of reads and writes. Valid values range from 8 to 16,777,216.

Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS**—Selects pseudo-random bit sequences.

- **Memory**—Selects a generic data pattern stored in the on chip memory of the Cyclone IV GX device.
- **Math**—Selects data generated from a simple math function within the FPGA fabric.

Read and Write Control

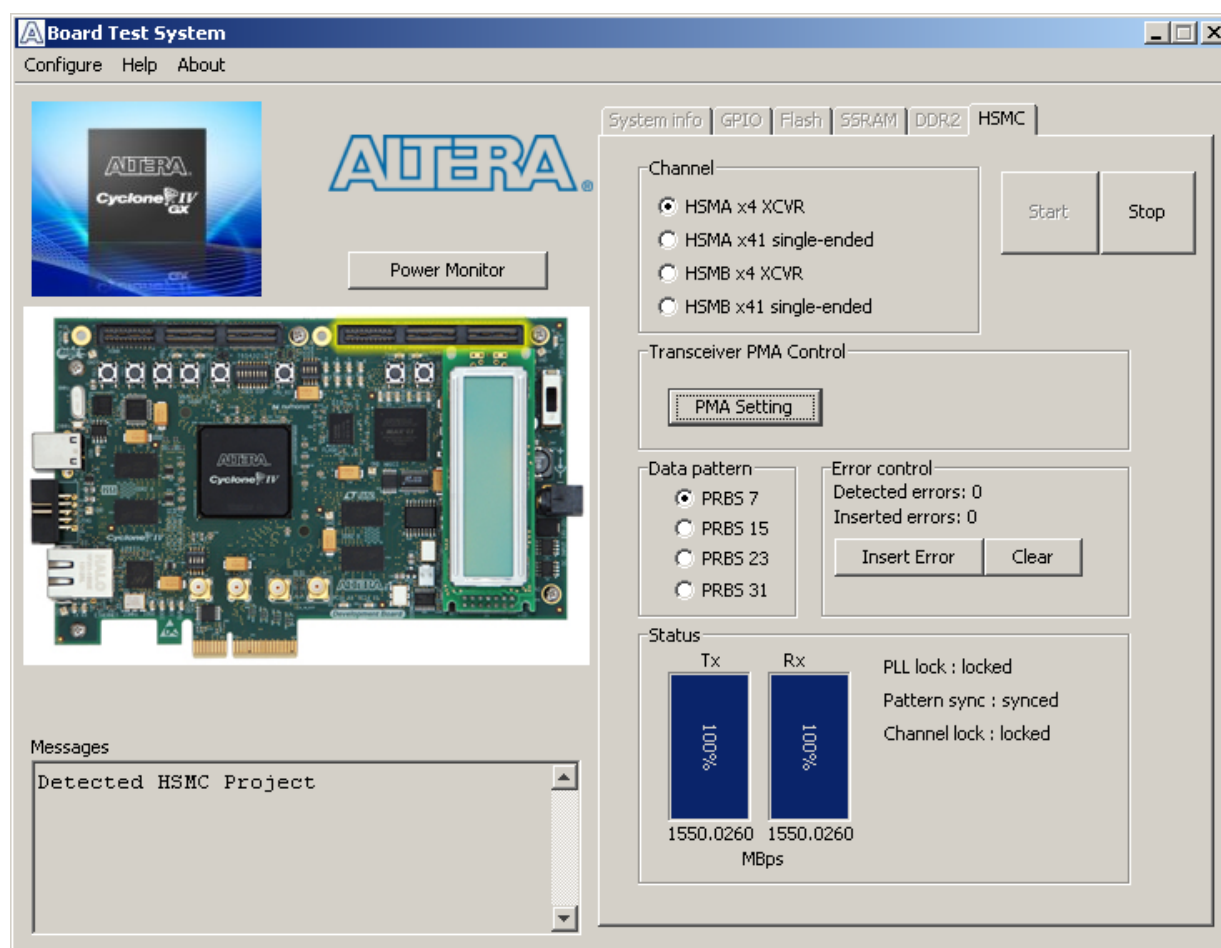
The **Read and write control** specifies the type of transactions to analyze. The following transaction types are available for analysis:

- **Write/Read**—Selects read and write transactions for analysis.
- **Read Only**—Selects read transactions for analysis.
- **Write Only**—Selects write transactions for analysis.

The HSMC Tab

The **HSMC** tab allows you to perform loopback tests on the HSMC A and HSMC B ports. [Figure 6-7](#) shows the **HSMC** tab.

Figure 6-7. The HSMC Tab





You must have the loopback HSMC installed on the HSMC connector that you are testing for this test to work correctly.

The following sections describe the controls on the **HSMC** tab.

Channel

- **HSMA x4 XCVR**—Selects the transceiver signals on HSMC Port A for test status reporting
- **HSMA x41 single-ended**—Selects the single-ended CMOS signals on HSMC Port A for test status reporting
- **HSMB x4 XCVR**—Selects the transceiver signals on HSMC Port B for test status reporting
- **HSMB x41 single-ended**—Selects the single-ended CMOS signals on HSMC Port B for test status reporting

Start

The **Start** control initiates HSMC transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
 - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
 - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
 - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.

- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX and RX performance bars**—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve. The maximum is 3.125 Gbps per transmitter x 4 transmitters = 12.5 Gbps = 1562.5 MBps, which requires a reference clock of approximately 100.8 MHz; the board powers up with a 100.0 MHz clock with a typical maximum performance of approximately 1550 MBps.
- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

The Power Monitor

The Power Monitor measures and reports current power information for the board. To start the application, click **Power Monitor** in the Board Test System application.



You can also run the Power Monitor as a stand-alone application. **PowerMonitor.exe** resides in the
<install dir>\kits\cycloneIVGX_4cgx150_fpga\examples\board_test_system
directory.

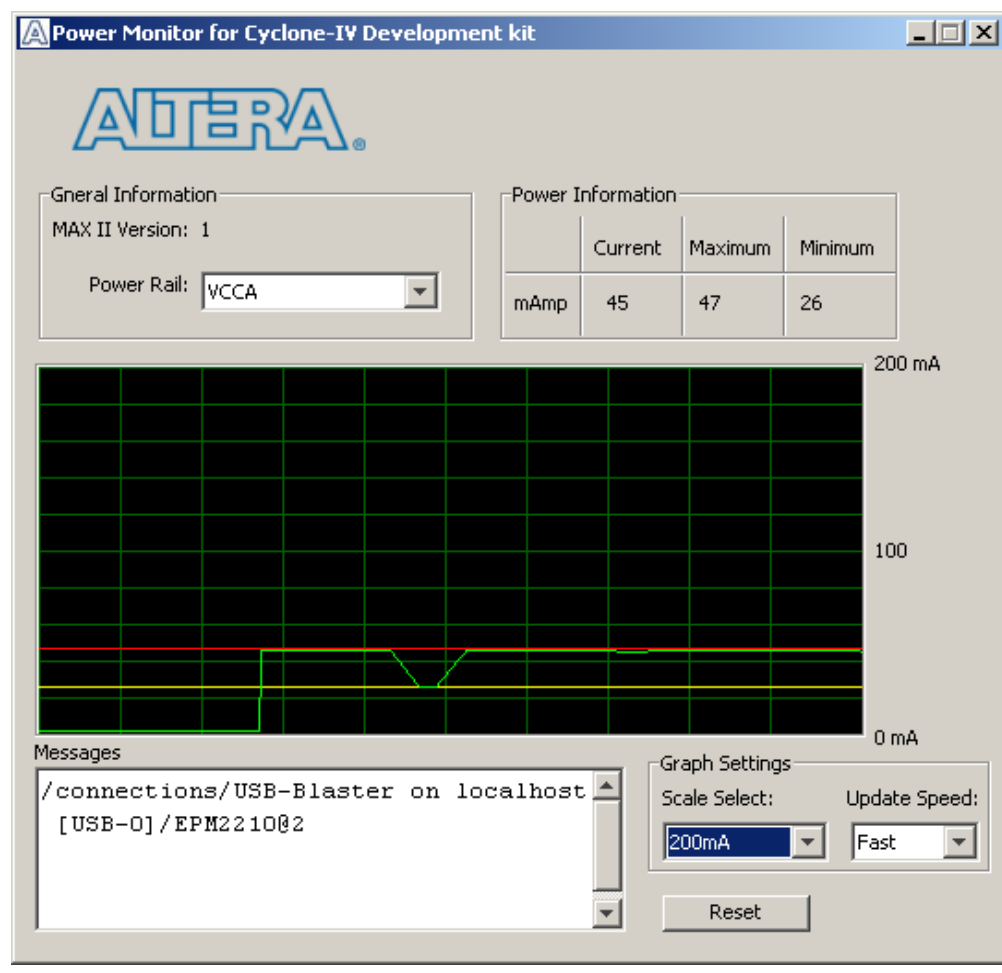
On Windows, click **Start > All Programs > Altera > Cyclone IV GX FPGA Development Kit <version> > Power Monitor** to start the application.

The Power Monitor communicates with the MAX II device on the board through the JTAG bus. A power monitor circuit attached to the MAX II device allows you to measure the power that the Cyclone IV GX FPGA device is consuming regardless of the design currently running. [Figure 6-8](#) shows the Power Monitor.



If the VCC rail consumes more than 3.25 A, Altera recommends that the fan be installed.

Figure 6–8. The Power Monitor



The following sections describe the Power Monitor controls.

General Information

The **General information** controls display the following information about the MAX II device:

- **MAX II version**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the *<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery* and *<install dir>\kits\cycloneIVGX_4cgx150_fpga\examples\max2* directories. Newer revisions of this code might be available on the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website.
- **Power rail**—Selects the power rail to measure. After selecting the desired rail, click **Reset** to refresh the screen with new board readings.



A table with the power rail is available in the *Cyclone IV GX FPGA Development Board Reference Manual*.

Power Information

The **Power information** control displays current, maximum, and minimum power readings for the following units:

- mVolt
- mAmp
- mWatt

Power Graph

The power graph displays the mWatt power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

Graph Settings

The following **Graph settings** controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

Reset

This **Reset** control clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

Calculating Power

The Power Monitor calculates power by measuring two different voltages with the LT2418 A/D and applying the equation $P = V \times I$ to determine the power consumption. The LT2418 measures the voltage after the appropriate sense resistor (V_{sense}) and the voltage drop across that sense resistor (V_{dif}). The current (I) is calculated by dividing the measured voltage drop across the resistor by the value of the sense resistor ($I = V_{dif}/R$). Through substitution, the equation for calculating power becomes $P = V \times I = V_{sense} \times (V_{dif}/R) = (V_{sense}) \times (V_{dif}) \times (1/.003)$.

You can verify the power numbers shown in the Power Monitor with a digital multimeter that is capable of measuring microvolts to ensure you have enough significant digits for an accurate calculation. Measure the voltage on one side of the resistor (the side opposite the power source) and then measure the voltage on the other side. The first measurement is V_{sense} and the difference between the two measurements is V_{dif} . Plug the values into the equation to determine the power consumption.

The Clock Control

The Clock Control application sets the Si570 programmable oscillator to any frequency between 10 MHz and 810 MHz with eight digits of precision to the right of the decimal point. The oscillator drives a 2-to-4 buffer that drives a copy of the clock to all four edges of the FPGA.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the

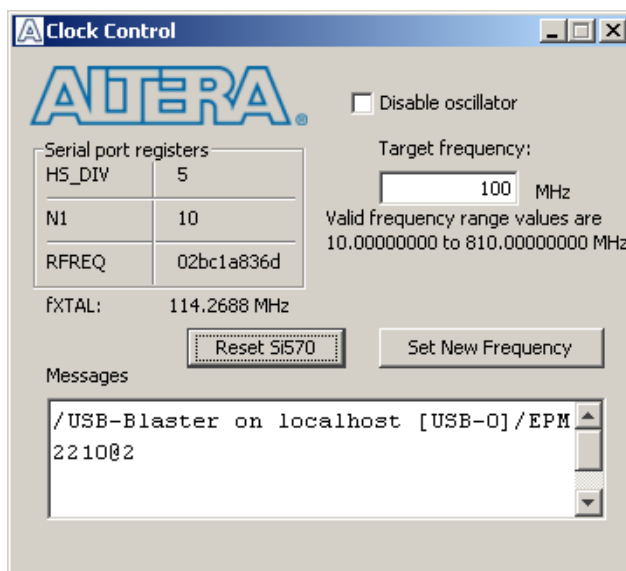
`<install dir>\kits\cycloneIVGX_4cgx150_fpga\examples\board_test_system` directory.

On Windows, click **Start > All Programs > Altera > Cyclone IV GX FPGA Development Kit <version> > Clock Control** to start the application.

For more information about the Si570 and the Cyclone IV GX FPGA development board's clocking circuitry and clock input pins, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*.

The Clock Control communicates with the MAX II device on the board through the JTAG bus. The Si570 programmable oscillator is connected to the MAX II device through a 2-wire serial bus. Figure 6-9 shows the Clock Control.

Figure 6-9. The Clock Control



The following sections describe the Clock Control application's control and status information.

Serial Port Registers

The **Serial port registers** control shows the current values from the Si570 registers.

For more information about the Si570 registers, refer to the *Si570/Si571* datasheet available on the Silicon Labs website (www.silabs.com).

fXTAL

The **fXTAL** control shows the calculated internal fixed-frequency crystal, based on the serial port register values.



For more information about the f_{XTAL} value and how it is calculated, refer to the Si570/Si571 datasheet available on the Silicon Labs website (www.silabs.com).

Target Frequency

The **Target frequency** control allows you to specify the frequency of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

Reset Si570

The **Reset Si570** control sets the Si570 programmable oscillator to the default frequency of 100 MHz.

Set New Frequency

The **Set New Frequency** control sets the Si570 programmable oscillator frequency to the value in the **Target frequency** control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific **.sof**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the FPGA development board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Cyclone IV GX FPGA, perform the following steps:

1. Start the Quartus II Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.



Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Cyclone IV GX FPGA development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Cyclone IV GX FPGA development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.



For more information about Altera development tools, refer to the [Design Software](#) page of the Altera website.

CFI Flash Memory Map

[Table A-1](#) shows the default memory contents of the 512-MB (64-MB) single-die CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A-1. Byte Address Flash Memory Map (Part 1 of 2)

| Block Description | Size | Address Range |
|---------------------------|----------|----------------------------|
| Unused | 128 KB | 0x03FF.FFFF 0x03FE.0000 |
| User software | 33536 KB | 0x03FD.FFFF 0x01F2.0000 |
| Factory software | 8192 KB | 0x01F1.FFFF 0x0172.0000 |
| zipfs (html, web content) | 4096 KB | 0x0171.FFFF 0x0132.0000 |
| User hardware 3 | 4864 KB | 0x0131.FFFF 0x00E6.0000 |
| User hardware 2 | 4864 KB | 0x00E5.FFFF 0x009A.0000 |
| User hardware 1 | 4864 KB | 0x0099.FFFF 0x004E.0000 |
| Factory hardware | 4864 KB | 0x004D.FFFF 0x0002.0000 |
| PFL option bits | 32 KB | 0x0001.FFFF 0x0001.8000 |

Table A-1. Byte Address Flash Memory Map (Part 2 of 2)

| Block Description | Size | Address Range |
|--------------------------|-------|----------------------------|
| Board information | 32 KB | 0x0001.7FFF 0x0001.0000 |
| Ethernet option bits | 32 KB | 0x0000.FFFF 0x0000.8000 |
| User design reset vector | 32 KB | 0x0000.7FFF 0x0000.0000 |



Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to “[Restoring the Flash Device to the Factory Settings](#)” on page A-4.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user hardware and user software locations of the flash memory.



For more information about Nios II EDS software tools and practices, refer to the [Embedded Software Development](#) page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:

- For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x4E0000
--pfl --optionbit=0x18000 --programmingmode=PS↵
```

- For Nios II **.elf** files:

```
elf2flash --base=0x08000000 --end=0x0BFFFFFF --reset=0x09F20000
--input=<yourfile>_sw.elf --output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec↵
```


The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.



The Board Update Portal standard **.flash** format conventionally uses either `<filename>_hw.flash` for hardware design files or `<filename>_sw.flash` for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to [“Using the Board Update Portal to Update User Designs” on page 5–2](#) for more information.



If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Set the USER_FACTORY switch (SW1.1) to the off position to load the Board Update Portal design from flash memory on power up.
2. Attach the USB-Blaster cable and power up the board.
3. If the board has powered up and the LCD displays either "Connecting..." or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the CONF DN LED does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to [“Configuring the FPGA Using the Quartus II Programmer” on page 6–19](#) for more information.
5. Click **Add File** and select
`<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery\c4gx150_fpga_bup.sof`.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The flash device is ready for programming.
8. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.

9. In the Nios II command shell, navigate to the `<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery` directory (or to the directory of the .flash files you created in “[Creating Flash Files Using the Nios II EDS](#)” on page A-2) and type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x08000000 <yourfile>_hw.flash ↵
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x08000000 <yourfile>_sw.flash ↵
```

11. Set the USER_FACTORY switch (SW1.1) to the on position and power cycle the board, or press the PGM_LOAD button to load and run the user hardware design.

Programming the board is now complete.



For more information about the `nios2-flash-programmer` utility, refer to the [Nios II Flash Programmer User Guide](#).

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following instructions:


1. Set the board switches to the factory default settings described in “[Factory Default Switch Settings](#)” on page 4-2.
2. Launch the Quartus II Programmer to configure the FPGA with a .sof capable of flash programming. Refer to “[Configuring the FPGA Using the Quartus II Programmer](#)” on page 6-19 for more information.
3. Click **Add File** and select `<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery\c4gx150_fpga_bup.sof`.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The flash device is ready for programming.
6. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
7. In the Nios II command shell, navigate to the `<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery` directory and type the following command to run the restore script:

```
./restore.sh ↵
```

Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.

8. After all flash programming completes, cycle the POWER switch (SW3) off then on.

9. Using the Quartus II Programmer, click **Add File** and select
`<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery\c4gx150_fpga_bup.sof`.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The flash memory device is now restored with the factory contents.
12. Cycle the POWER switch (SW3) off then on to load and run the restored factory design.
13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

`nios2-terminal` 

and follow the instructions in the terminal window to generate a unique MAC address.



To ensure that you have the most up-to-date factory restore files and information about this product, refer to the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website.

Restoring the MAX II CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX II CPLD on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in “[Factory Default Switch Settings](#)” on page 4-2.



Setting DIP switch SW5.1 to the on position includes the MAX II device in the JTAG chain.

2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select
`<install dir>\kits\cycloneIVGX_4cgx150_fpga\factory_recovery\max2.pof`.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX II CPLD. Configuration is complete when the progress bar reaches 100%.



To ensure that you have the most up-to-date factory restore files and information about this product, refer to the [Cyclone IV GX FPGA Development Kit](#) page of the Altera website.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

| Date | Version | Changes |
|---------------|---------|--|
| November 2014 | 1.1 | Corrected a document link to the reference manual. |
| November 2010 | 1.0 | Initial release. |

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

| Contact (1) | Contact Method | Address |
|---|----------------|--|
| Technical support | Website | www.altera.com/support |
| Technical training | Website | www.altera.com/training |
| | Email | custrain@altera.com |
| Product literature | Website | www.altera.com/literature |
| Non-technical support (General) (Software Licensing) | Email | nacomp@altera.com |
| | Email | authorization@altera.com |









Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

| Visual Cue | Meaning |
|---|---|
| Bold Type with Initial Capital Letters | Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI. |
| bold type | Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D: drive, and chiptrip.gdf file. |
| <i>Italic Type with Initial Capital Letters</i> | Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> . |
| <i>italic type</i> | Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pof file. |

| Visual Cue | Meaning |
|---|---|
| Initial Capital Letters | Indicate keyboard keys and menu names. For example, the Delete key and the Options menu. |
| “Subheading Title” | Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.” |
| Courier type | Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code> , <code>tdi</code> , and <code>input</code> . The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code> . Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code> . Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>). |
|  | An angled arrow instructs you to press the Enter key. |
| 1., 2., 3., and a., b., c., and so on | Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
|  | Bullets indicate a list of items when the sequence of the items is not important. |
|  | The hand points to information that requires special attention. |
|  | A question mark directs you to a software help system with related information. |
|  | The feet direct you to another document or website with related information. |
|  | A caution calls attention to a condition or possible situation that can damage or destroy the product or your work. |
|  | A warning calls attention to a condition or possible situation that can cause you injury. |
|  | The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents. |

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