Intel® Cyclone® 10 LP FPGA Evaluation Kit User Guide

Online Version
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Contents

1. Overview

The Intel® Cyclone® 10 LP Evaluation Kit provides an easy-to-use platform for evaluating the performance and features of the Intel Cyclone 10 LP FPGA device.

1.1. Evaluation Kit Description

The Intel Cyclone 10 LP FPGA Evaluation Kit includes the following components:

- The Intel Cyclone 10 LP FPGA evaluation board
- USB Y-cable (USB Type-A to mini Type-B) for both on-board Intel FPGA Download Cable II and 5 V power supply from USB port
- Intel Cyclone 10 LP FPGA Evaluation Kit collateral, available from the Intel Cyclone 10 LP FPGA page

The design tools for the Intel Cyclone 10 LP FPGA Evaluation Kit are contained in the Intel Quartus® Prime Standard Edition software. Intel Quartus Prime software can be downloaded from the Intel FPGA Download Center.

Related Information

- Intel Cyclone 10 LP FPGA page
- Intel FPGA Download Center

1.1.1. Evaluation Board Description

The evaluation kit includes a RoHS and CE compliant Intel Cyclone 10 LP FPGA Evaluation Board with the following components.

Featured Devices

- Intel Cyclone 10 LP FPGA (10CL025, U256 package)
- Intel Enpirion® EN5329QI/EN5339QI - 2A/3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
- Intel Enpirion EP5358xUI 600 mA PowerSoC DC-DC Step-Down Converters with Integrated Inductor
- Intel XWAY PHY11G Gigabit Ethernet PHY PEF7071
- Intel MAX® 10 FPGA 10M08SAU169C8G (Embedded Intel FPGA Download Cable II and System Management)

Programming and Configuration

- Embedded Intel FPGA Download Cable II (JTAG)
- Optional JTAG direct through 10-pin header
- Active Serial x1 configuration from EPCQ or EPCQ-A flash

Memory Devices

- 128 megabit (Mb) 8-bit HyperRAM with HBMC (Hyperbus Memory Controller) IP provided by Synaptic Labs
- Flash memory:
  - Rev A1 board: 64 Mb EPCQ
  - Rev A2 board: 128 Mb EPCQ-A

Communication Ports

- One Gigabit Ethernet (GbE) RJ-45 port
- One 2x20 GPIO Expansion Header
- One Arduino UNO R3 type connectors
- One 12-pin Digilent Pmod compatible connector

Clock Circuits

- Silicon Labs Si510 50 MHz crystal oscillator
- Silicon Labs Si5351 clock generator with programmable frequency GUI

Power Supply

- USB Y-cable (USB Type-A to mini Type-B) for both on-board Intel FPGA Download Cable II and 5 V power supply from USB port
- Supplemental 5 V DC power adapter option (5 V power adapter and cord are not included in the kit)

Related Information

EPCQ or EPCQ-A Flash Memory on page 34

1.1.2. Evaluation Kit Collateral

The Intel Cyclone 10 LP FPGA evaluation kit collateral includes example designs, board design files, documentation, and the Board Test System software.

Related Information

Installing the Evaluation Kit Collateral on page 8

1.1.3. Power Supply Description

There are two power supply options provided for the Intel Cyclone 10 LP FPGA Evaluation Board. The first is USB powered and the second is external AC/DC adapter powered. These two options can be used for different applications. There is an ORING circuit on-board to select suitable power source from USB power or DC jack.

USB-Power

A standard A to Mini-B USB Y-Cable is shipped with the evaluation board.

AC/DC Adapter Power

Caution: Use 5 V adapter for DC Jack J12 only. Components on the board can get damaged by power supplies with greater voltage.

1.2. Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum VCCINT current: 0.6 A
- Maximum board power consumption: 3 A @ 5 V when powered by AC/DC adapter

1.3. Handling the Board

When handling the board, it is important to observe static discharge precautions.

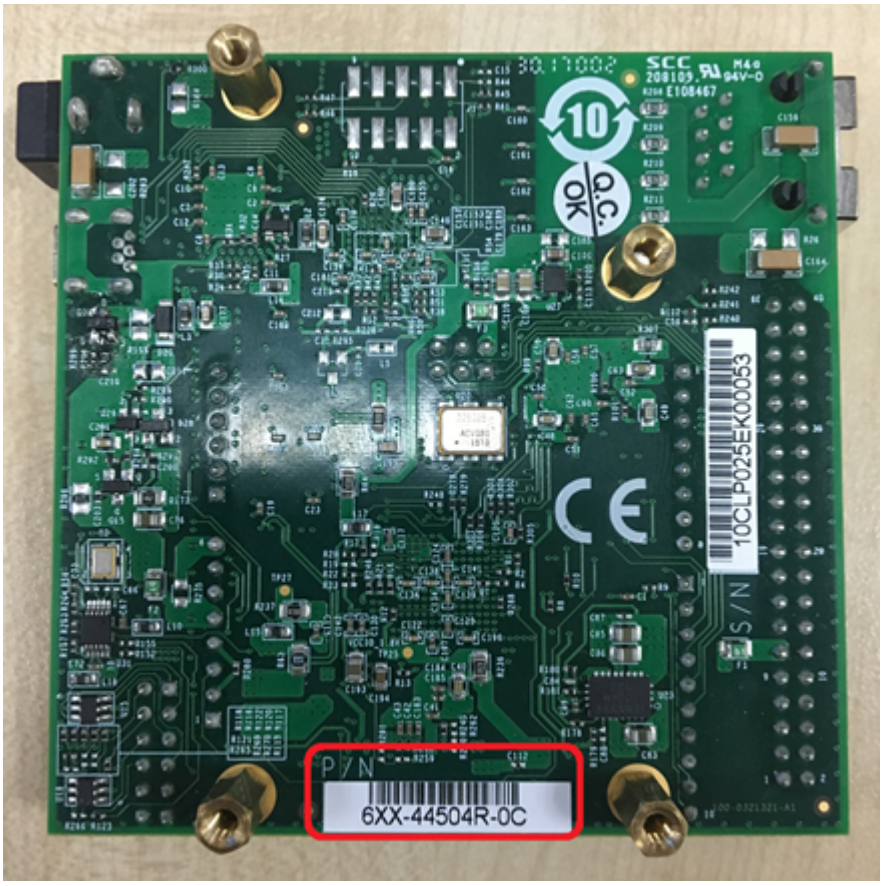
Caution: Without proper anti-static handling, the board could be damaged. Use anti-static handling precautions when touching the board.

Caution: This evaluation board should not be operated in a vibration environment.

1.4. Evaluation Board Revisions

Depending on its revision, your board has one of two flash memory devices: EPCQ64 or EPCQ128A. To determine which device you have, examine the part number label on the back side of the board, as shown in the following figure.

Figure 1. Intel Cyclone 10 LP Evaluation Board Part Number Label



The following table shows the board revision and flash memory type corresponding to the part number.

Table 1. Intel Cyclone 10 LP Evaluation Board Revision and Flash Type

Part Number	Board Revision	Flash Memory Type
6XX-44504R-0C or earlier	A1	EPCQ64
6XX-44504R-0D or later	A2	EPCQ128A

2. Getting Started

2.1. Installing Quartus Prime Software

To download the Intel Quartus Prime Standard Edition software, go to the **Quartus Prime Standard Edition** page in the Intel Download Center.

About Intel Quartus Prime Software

The Intel Quartus Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

The Intel Quartus Prime Design Suite design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation.

Intel Quartus Prime Standard Edition includes the most extensive support for Intel's latest device families and requires paid license.

Included in the Intel Quartus Prime Standard Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

Related Information

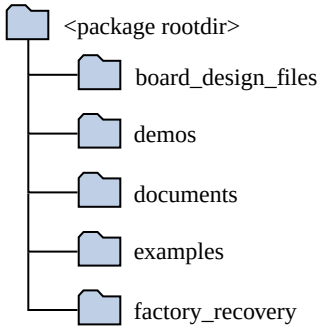
Intel FPGA Download Center

2.2. Installing the Evaluation Kit Collateral

To download the Intel Cyclone 10 LP FPGA Evaluation Kit collateral, perform the following steps:

1. Download the evaluation kit collateral from the Intel Cyclone 10 LP FPGA page.
2. Unzip the Intel Cyclone 10 LP FPGA Evaluation Kit collateral contents to your machine's local hard drive.
3. The collateral creates the directory structure shown in the figure below.

Figure 2. Evaluation Kit Directory Structure



The table below lists the file directory names and a description of their contents

Table 2. Directory Structure

File Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
`demos`	Contains demonstration applications when available
`documents`	Contains the evaluation kit documentation
`examples`	Contains the sample design files for the evaluation kit
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Related Information

Intel Cyclone 10 LP FPGA page

2.3. Installing Intel FPGA Download Cable Driver

The Intel Cyclone 10 LP FPGA Evaluation Board includes embedded Intel FPGA Download Cable circuits for FPGA programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

3. Evaluation Board Setup

The instructions in this chapter explain how to set up the Intel Cyclone 10 LP FPGA Evaluation Board.

3.1. Powering Up the Evaluation Board

There are two power supply options provided for the Intel Cyclone 10 LP FPGA Evaluation Board. The first is USB powered and the second is external AC/DC adapter powered. These two options can be used for different applications.

For most applications without Arduino, 2x20 GPIO, Pmod daughter cards, using an USB Cable offers sufficient current.

For some applications, daughter cards may draw high power consumption that USB port cannot offer sufficient current. A common 5 V AC/DC adapter can be plugged into the DC Jack J12 to offer higher current.

Caution: Use 5 V adapter for DC Jack J12 only. Components on the board can get damaged by power supplies with greater voltage.

To prepare and apply power to the board, perform the following steps:

1. The Intel Cyclone 10 LP evaluation board ships with its board switches pre-configured to support the design examples in the evaluation kit collateral. If you suspect your board might not be correctly configured with the default settings, follow the instructions in Default Switch Settings on page 10 to return the board to its factory settings before proceeding.
2. Connect either USB cable to J17 or 5 V DC adapter to J12 to power up the board.
3. After the board is powered up correctly, status LED illuminates. If you are using factory image stored in flash, the Blue LED will be ON to indicate power is good. Yellow LED D5 will be ON to indicate the FPGA is configured successfully. User LEDs D6, D7, D8, D9 will be blinking which is set in factory image.

3.2. Default Switch Settings

This section shows the factory DIP switch settings for the Intel Cyclone 10 LP FPGA evaluation board.

Table 3. DIP Switch Settings

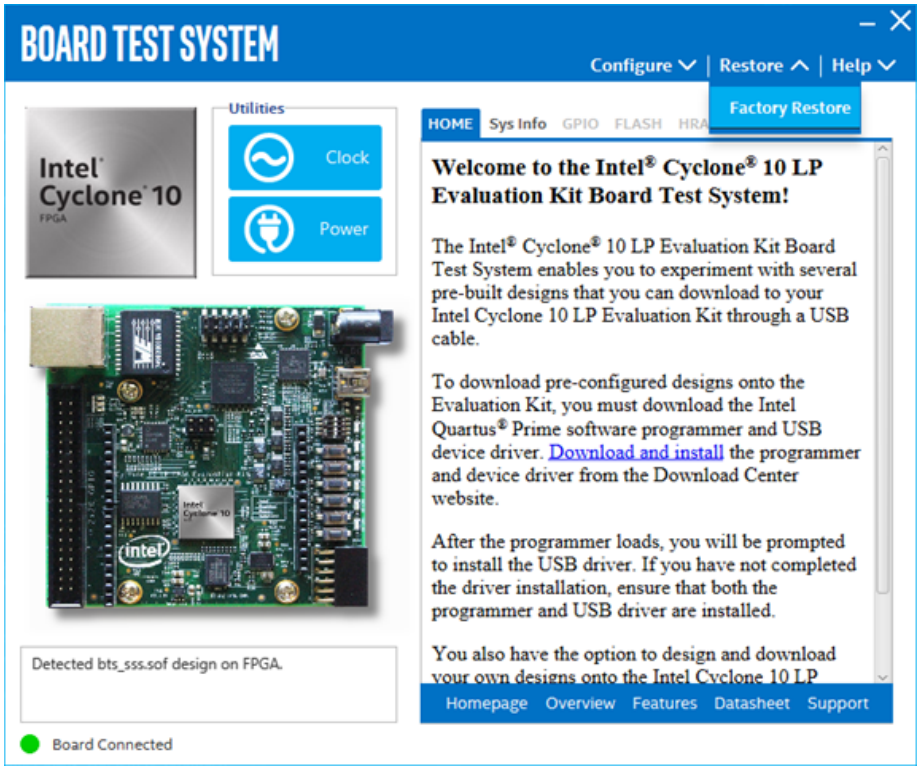
Switch	Board Label	Default Position	Function
SW1.4	BYPASS	OPEN/OFF/1	Virtual JTAG TAP Enable
SW1.3	DIP0	OPEN/OFF/1	Switch 0
SW1.2	DIP1	OPEN/OFF/1	Switch 1
SW1.1	DIP2	OPEN/OFF/1	Switch 2

3.3. Recovering Factory Default Settings

To restore the evaluation board to factory default settings, perform the following steps.

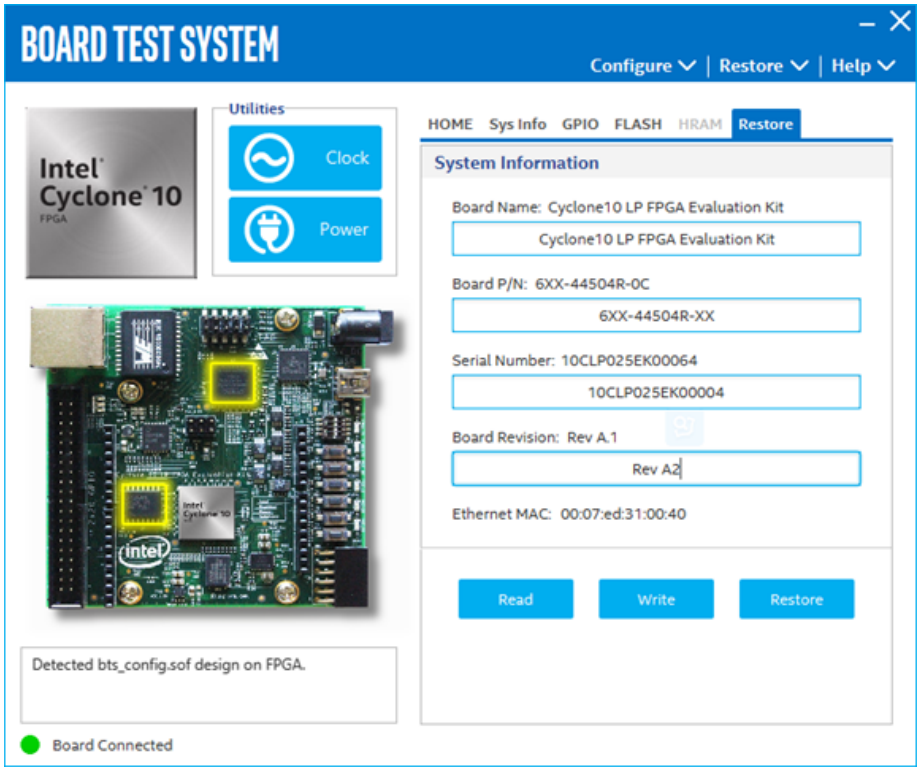
1. Make sure you have the latest Intel software tools, including the Intel Quartus Prime Standard Edition software, Nios II processor, and IP cores. If necessary, download the Intel Quartus Prime Standard Edition software from the Intel FPGA Download Center.
2. Launch the Board Test System (BTS) GUI application by one of the following methods:
   - Nios II command shell:
     a. Launch the Nios II command shell.
     b. Change directory to `<package dir>\examples\board_test_system\`.
     c. Type `./BoardTestSystem.exe` to launch the BTS GUI.
   - File manager:
     a. In a file manager GUI (such as File Explorer), change directory to `<package dir>\examples\board_test_system\`.
     b. Double-click `BoardTestSystem.exe` to launch the BTS GUI.
3. On the **Restore** menu, click **Factory Restore**.

Figure 3. Board Test System GUI with Restore Menu



4. Fill in the text boxes with your board details, as shown in the example below, and click **Restore**.
   The restore process takes several minutes.

Figure 4. Restoring Factory Defaults on the Intel Cyclone 10 LP LP FPGA Evaluation Board



Related Information

Intel FPGA Download Center

4. Evaluation Board Components

This chapter introduces all important components on the evaluation board.

4.1. Board Overview

This topic provides a high-level list of major components on the Intel Cyclone 10 LP FPGA evaluation board.

Figure 5. Intel Cyclone 10 LP FPGA Evaluation Board Block Diagram

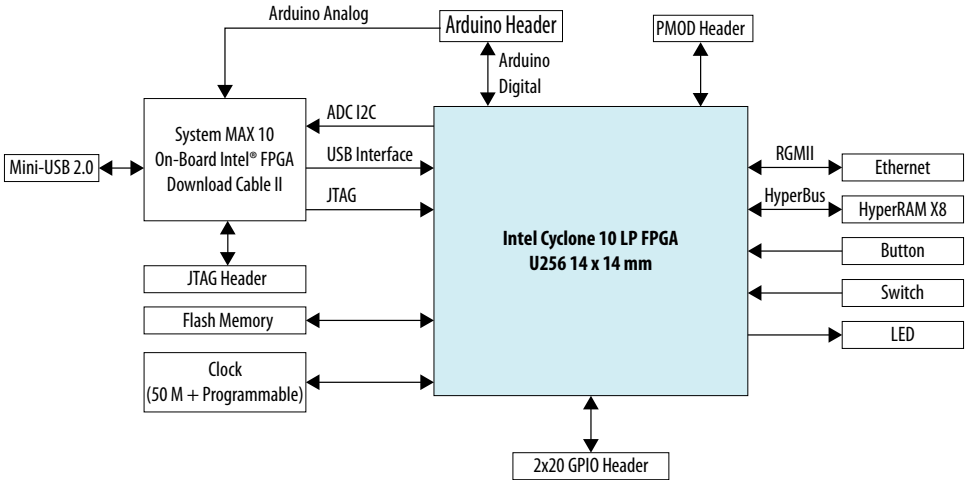


Table 4. Board Components

Board Reference	Type	Description
Featured Devices		
U1	FPGA	Intel Cyclone 10 LP FPGA 10CL025YU256I7G, 25k LEs, U256 package
U3	FPGA	Intel MAX 10 10M08SAU169C8G for On-board Intel FPGA Download Cable II and System Management
U25	Power Regulator	Intel Enpirion EN5329QI - 2A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
U23	Power Regulator	Intel Enpirion EN5339QI - 3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor

continued...

Board Reference	Type	Description
U26, U27	Power Regulator	Intel Enpirion EP5358HUI, 600 mA PowerSoC DC-DC step-down converters with integrated inductor.
U14	Gigabit Ethernet PHY	Intel XWAY PHY11G Single Port Gigabit Ethernet PHY (10/100/1000 Mbps) PEF7071
Configuration and Setup Elements		
J17	Embedded Intel FPGA Download Cable II	Type-B Mini USB Connector for programming and debugging the FPGA
J2	10-pin header	Optional JTAG direct through 10-pin header for external download cables
SW1.4	Virtual JTAG TAP Bypass Switch	ON/Closed/0: Bypass Virtual JTAG TAP OFF/Open/1: Enable Virtual JTAG TAP
S1	FPGA `nCONFIG` push button	Press this button to trigger reconfiguration
S2	FPGA reset push button	Press this button to reset all registers in the FPGA
Status Elements		
D4	Power LED (Blue)	Power Good LED (Detects `VCC_3.3V` and `VCC_1.2V`) ON: Detected Power is Good OFF: Detected Power is Bad
D5	Configuration LED (Yellow)	Config done status Indicator ON: FPGA configured successfully OFF: FPGA not configured
D10	Ethernet LED0 (Green)	Ethernet link status indicator ON: Link-up OFF: Link-down Blink: Link-up with traffic
D11	Ethernet LED1 (Green)	Ethernet link speed indicator ON: 100 Mbps OFF: 10/1000 Mbps or Link-down
D12	Ethernet LED2 (Green)	Ethernet link speed indicator ON: 1000 Mbps OFF: 10/1000 Mbps or Link-down
Clock Circuits		
U20	50 MHz Oscillator	50 MHz crystal oscillator for general purpose logic of Intel Cyclone 10 LP FPGA and Intel MAX 10 FPGA devices
U31	Programmable clock generator	Three channel Programmable clock generator. Default frequencies are 125 MHz, 100 MHz and 50 MHz
General User Input/Output		
S3, S4, S5, S6	General user push buttons	Four user push buttons. Driven low when pressed.
D6, D7, D8, D9	User LEDs	Four user LEDs. Illuminates when driven low.

continued...

Board Reference	Type	Description
SW1.1 - SW1.3	User DIP Switches	3-bit user DIP switches
Memory Devices		
U13	HyperRAM Memory	128 Mb x8 HyperRAM with 1.8 V I/O
U2	Flash	• Board Rev A1: 64 Mb EPCQ • Board Rev A2: 128 Mb EPCQ-A(1)
I/O and Expansion Ports		
J8	One Digilent Pmod Connector	12-pin interface with 8 I/O signal pins used to connect low frequency, low I/O peripheral modules
J4, J5, J6, J7, J18	Arduino UNO R3 type connector	Arduino UNO R3 type connectors with 3.3 V digital I/O and six analog input channels
J10	2x20 GPIO Expansion Header	2x20 GPIO Expansion Header with 36 I/O
J16	One Gigabit Ethernet Port	RJ-45 connector provides a 10/100/1000 Ethernet connection through a Intel PEF7071 PHY and the FPGA-based Intel Triple Speed Ethernet MegaCore function in RGMII mode
Power Supply		
J12	DC input jack	Supplemental 5 V DC power adapter connector
J17	USB Mini-B Connector	For 5 V power from USB port also used as Intel FPGA Download Cable communication port

Related Information

EPCQ or EPCQ-A Flash Memory on page 34

4.2. Intel Cyclone 10 LP FPGA Overview

The Intel Cyclone 10 LP FPGA Evaluation Board features the Intel Cyclone 10 LP 10CL025YU256I7G FPGA device in a 256 pin Ultra FineLine BGA package.

The Intel Cyclone 10 LP FPGAs are optimized for low cost and low static power, making them ideal for high-volume and cost-sensitive applications.

Table 5. Intel Cyclone 10 LP FPGA

Equivalent LEs	M9K Memory Blocks	M9K Memory Size (Kb)	18-bit x 18-bit multipliers	PLLs	Transceivers	Package Type
25K	66	594	66	4	---	256-pin UBGA (14 mm x 14 mm, 0.8 mm pitch)

(1) To identify your board revision, see "EPCQ or EPCQ-A Flash Memory".

Intel Cyclone 10 LP FPGA Feature Summary

Intel Cyclone 10 LP FPGA devices provide a high-density sea of programmable gates, on-board resources, and general purpose I/Os. These resources satisfy the requirements of I/O expansion and chip-to-chip interfacing. The Intel Cyclone 10 LP FPGA architecture suits smart and connected end applications across many market segments:

- Industrial and automotive
- Broadcast, wireline, and wireless
- Compute and storage
- Government, military, and aerospace
- Medical, consumer, and smart energy

Table 6. Summary of Features for Intel Cyclone 10 LP FPGA Devices

Feature	Description
Technology	• Low-cost, low-power FPGA fabric • 1.0 V and 1.2 V core voltage options • Available in commercial, industrial, and automotive temperature grades
Packaging	• Several package types and footprints: — FineLine BGA (FBGA) — Enhanced Thin Quad Flat Pack (EQFP) — Ultra FineLine BGA (UBGA) — Micro FineLine BGA (MBGA) • Multiple device densities with pin migration capability • RoHS6 compliance
Core architecture	• Logic elements (LEs)—four-input look-up table (LUT) and register • Abundant routing/metal interconnect between all LEs
Internal memory blocks	• M9K—9-kilobits (Kb) of embedded SRAM memory blocks, cascadable • Configurable as RAM (single-port, simple dual port, or true dual port), FIFO buffers, or ROM
Embedded multiplier blocks	• One 18 × 18 or two 9 × 9 multiplier modes, cascadable • Complete suite of DSP IPs for algorithmic acceleration
Clock networks	• Global clocks that drive throughout entire device, feeding all device quadrants • Up to 15 dedicated clock pins that can drive up to 20 global clocks
Phase-locked loops (PLLs)	• Up to four general purpose PLLs • Provides robust clock management and synthesis
General-purpose I/Os (GPIOs)	• Multiple I/O standards support • Programmable I/O features • True LVDS and emulated LVDS transmitters and receivers • On-chip termination (OCT)
SEU mitigation	SEU detection during configuration and operation
Configuration	• Active serial (AS), passive serial (PS), fast passive parallel (FPP) • JTAG configuration scheme • Configuration data decompression • Remote system upgrade

Related Information

Intel Cyclone 10 LP FPGA Device Overview

4.3. MAX 10 System Controller Overview

The highlights of the Intel MAX 10 devices include:

- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converter (ADC)
- Single-chip Nios II soft core processor support

Intel MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

Table 7. Summary of Features for Intel MAX 10 Devices

Feature	Description
Technology	55 nm TSMC Embedded Flash (Flash + SRAM) process technology
Packaging	• Low cost, small form factor packages—support multiple packaging technologies and pin pitches • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS6-compliant
Core architecture	• 4-input look-up table (LUT) and single register logic element (LE) • LEs arranged in logic array block (LAB) • Embedded RAM and user flash memory • Clocks and PLLs • Embedded multiplier blocks • General purpose I/Os
Internal memory blocks	• M9K—9 kilobits (Kb) memory blocks • Cascadable blocks to create RAM, dual port, and FIFO functions
User flash memory (UFM)	• User accessible non-volatile storage • High speed operating frequency • Large memory size • High data retention • Multiple interface option
Embedded multiplier blocks	• One 18 × 18 or two 9 × 9 multiplier modes • Cascadable blocks enabling creation of filters, arithmetic functions, and image processing pipelines
ADC	• 12-bit successive approximation register (SAR) type • Up to 16 analog inputs • Cumulative speed up to 1 million samples per second (MSPS) • Integrated temperature sensing capability
Clock networks	• Global clocks support • High speed frequency in clock network
Internal oscillator	Built-in internal ring oscillator
PLLs	• Analog-based • Low jitter • High precision clock synthesis

continued...

Feature	Description
	• Clock delay compensation • Zero delay buffering • Multiple output taps
General-purpose I/Os (GPIOs)	• Multiple I/O standards support • On-chip termination (OCT) • Up to 830 megabits per second (Mbps) LVDS receiver, 800 Mbps LVDS transmitter
External memory interface (EMIF)	Supports up to 600 Mbps external memory interfaces: • DDR3, DDR3L, DDR2, LPDDR2 • SRAM (Hardware support only) *Note:* For 600 Mbps performance, –6 device speed grade is required. Performance varies according to device grade (commercial, industrial, or automotive) and device speed grade (–6 or –7). Refer to the MAX 10 Device Data Sheet or External Memory Interface Spec Estimator for more details.
Configuration	• Internal configuration • JTAG • Advanced Encryption Standard (AES) 128-bit encryption and compression options • Flash memory data retention of 20 years at 85 °C
Flexible power supply schemes	• Single- and dual-supply device options • Dynamically controlled input buffer power down • Sleep mode for dynamic power reduction

Related Information

MAX 10 FPGA Device Overview

4.4. FPGA Configuration

The Intel Cyclone 10 LP FPGA Evaluation Board supports two configuration methods:

- Configuration by downloading a .sof file to the FPGA. Any power cycling of the FPGA or reconfiguration will power up the FPGA to a blank state.
- Programming of the board EPCQ or EPCQ-A flash with a .jic file. Any power cycling of the FPGA or reconfiguration will lead to reconfigure from flash with AS mode.

You can use two different Intel FPGA Download Cable hardware components to program the .sof or .jic files:

- Embedded Intel FPGA Download Cable II type-B mini-USB connector (J17)
- JTAG header (J2). Use an external Intel FPGA Download Cable, Intel FPGA Download Cable II or Ethernet Blaster download cable. The external download cable connects to the board through the JTAG header (J2).

4.4.1. Using the Quartus Prime Programmer

You can use the Intel Quartus Prime Programmer to configure the FPGA with a .sof.

Before configuring the FPGA

- Ensure that the Intel Quartus Prime Programmer and the Intel FPGA Download Cable driver are installed on the host computer.
- The USB cable is connected to the board.
- Power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Intel Cyclone 10 LP FPGA

1. Start the Intel Quartus Prime Programmer.
2. Click Add File and select the path to the desired .sof.
3. Turn on the Program/Configure option for the added file.
4. Click Start to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

4.4.2. Program On-Board EPCQ or EPCQ-A Flash Memory

The FPGA is set to Active Serial configuration mode by default. You can use the Intel Quartus Prime Programmer to program a .jic file to EPCQ or EPCQ-A flash.

Program the EPCQ or EPCQ-A Flash

1. Ensure the DIP switch SW1.4 is ON to bypass virtual JTAG TAP and then power on the board.
2. Open Intel Quartus Prime Programmer and ensure that JTAG is detected under Hardware Setup.
3. Select **Auto Detect** and choose the correct FPGA device.
4. Right-click on the FPGA device and select **Edit ➤ Attach Flash Device**.
5. Select **ASC Devices ➤ EPCQ64** (or **EPCQ128A**) in the pop-up window and then click **OK**.
6. Right-click on the EPCQ64 (or EPCQ128A) device and select **Edit ➤ Change File**. Next, choose the generated `.jic` file you want to program.
7. Select the **Program/Configure** checkboxes for FPGA and EPCQ or EPCQ-A devices. Click **Start** to begin programming the FPGA.
8. Flash is programmed successfully when the progress bar reaches 100% and displays **Successful**.

Attention: Please set SW1.4 to OFF if your following operations need to enable virtual JTAG TAP.

Note: Either EPCQ64 or EPCQA128 may be used on boards of different board revisions. Refer to "EPCQ or EPCQ-A Flash Memory" for details.

Related Information

EPCQ or EPCQ-A Flash Memory on page 34

4.4.3. Active Serial Configuration

1. After all steps in the previous section are completed, press push button S1 C10_NCONFIG or power cycle the board.
2. Yellow LED D5 will turn ON. This indicates that the FPGA is configured with the image in flash under Active Serial Mode.

4.5. Status Elements

Table 8. LEDs

Board Reference	Schematic Signal Name	Color	Description
D4	PWR_GD_LED	Blue	Power Good LED (Detects VCC_3.3V and VCC_1.2V) ON: Detected Power is good OFF: Detected Power is bad
D5	SYS_CONF_DONE	Yellow	Configuration Done Status Indicator ON: FPGA configured successfully OFF: FPGA not configured
D10	ENET_LED0	Green	Ethernet link status indicator ON: Link-up OFF: Link-down Blink: Link-up with traffic
D11	ENET_LED1	Green	Ethernet link speed indicator ON: 100 Mbps OFF: 10/1000 Mbps or Link-down
D12	ENET_LED2	Green	Ethernet link speed indicator ON: 1000 Mbps OFF: 10/100 Mbps or Link-down

4.6. Setup Elements

Table 9. DIP Switches

Board Reference	Schematic Signal Name	Description
SW1.4	VTAP_BYPASSn	Pull low to disable Virtual JTAG TAP in device chain

Table 10. Push Buttons

Board Reference	Schematic Signal Name	Description
S1	C10_nCONFIG	Press this push button to reconfigure Intel Cyclone 10 LP FPGA device
S2	C10_RESETn	Press to do device-wide reset, connect to Intel Cyclone 10 LP FPGA DEV_CLRn

4.7. General User Input/Output

Table 11. DIP Switches

Board Reference	Schematic Signal Name	FPGA Signal Name	Description
SW1.3	USER_DIP0	U1.M16	User-defined Switch0
SW1.2	USER_DIP1	U1.A8	User-defined Switch1
SW1.1	USER_DIP2	U1.A9	User-defined Switch2

Table 12. Push Buttons

Board Reference	Schematic Signal Name	FPGA Signal Name	Description
S3	USER_PB0	U1.E15	User-defined PB0
S4	USER_PB1	U1.F14	User-defined PB1
S5	USER_PB2	U1.C11	User-defined PB2
S6	USER_PB3	U1.D9	User-defined PB3

Table 13. LEDs

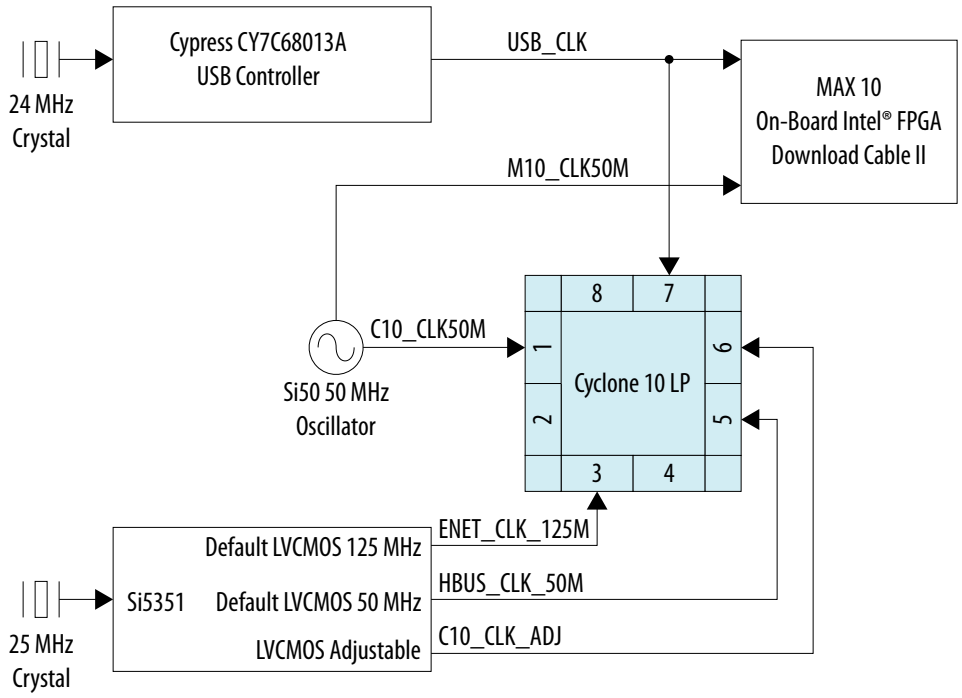
Board Reference	Schematic Signal Name	FPGA Signal Name	Color	Description
D6	USER_LED0	U1.L14	Green	User-defined LED0, active low
D7	USER_LED1	U1.K15	Green	User-defined LED1, active low
D8	USER_LED2	U1.J14	Green	User-defined LED2, active low
D9	USER_LED3	U1.J13	Green	User-defined LED3, active low

4.8. Clocks

Si5351 is a programmable clock generator that users can use Intel Clock GUI to program output frequency. It is controlled from Intel MAX 10 with I^2C bus.

The clock tree is shown in the figure below.

Figure 6. Intel Cyclone 10 LP FPGA Clock Tree



4.9. Connectors and Interfaces

This section describes the evaluation board's communication ports, and interface cards related to the Intel Cyclone 10 LP FPGA Evaluation Kit.

4.9.1. Gigabit Ethernet PHY

The evaluation board supports single port Ethernet through Intel XWAY PHY11G PEF7071 Ethernet PHY chips. This physical layer device has general applications using RJ-45 connector.

Figure 7. MAC-to-PHY connection by PEF7071 device

Specific to the Intel Cyclone 10 LP FPGA evaluation board, the MAC-to-PHY interface is configured to a RGMII interface connection with MDIO interface as management.

Table 14. Ethernet PHY Table

Schematic Signal Name	Schematic Shared Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
ENET_RG_TXCLK	C10_RG_TXCLK	D3	3.3 V	Out	RGMII TX clock
ENET_RG_TXD0	C10_RG_TXD0	E6	3.3 V	Out	RGMII TX data 0
ENET_RG_TXD1	C10_RG_TXD1	A3	3.3 V	Out	RGMII TX data 1
ENET_RG_TXD2	C10_RG_TXD2	B3	3.3 V	Out	RGMII TX data 2

continued...

Schematic Signal Name	Schematic Shared Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
ENET_RG_TXD3	C10_RG_TXD3	A2	3.3 V	Out	RGMII TX data 3
ENET_RG_TXCTL	C10_RG_TXCTL	D6	3.3 V	Out	RGMII TX control
ENET_RG_RXCLK	RG_RXCLK	B8	3.3 V	In	RGMII RX Clock
ENET_RG_RXD0	RG_RXD0	A7	3.3 V	In	RGMII RX data 0
ENET_RG_RXD1	RG_RXD1	B7	3.3 V	In	RGMII RX data 1
ENET_RG_RXD2	RG_RXD2	A6	3.3 V	In	RGMII RX data 2
ENET_EG_RXD3	RG_RXD3	B6	3.3 V	In	RGMII RX data 3
ENET_RG_RXCTL	RG_RXCTL	A5	3.3 V	In	RGMII RX Control
ENET_INT		B5	3.3 V	In	Management Interrupt
ENET_MDC		B4	3.3 V	Out	MDIO clock
ENET_MDIO		A4	3.3 V	I/O	MDIO data
ENET_RSTn		C6	3.3 V	Out	Device Reset
ENET_XTAL1					
ENET_XTAL2					
ENET_LED0			3.3 V	Out	Status LED0, Green
ENET_LED1			3.3 V	Out	Status LED1, Green
ENET_LED2			3.3 V	Out	Status LED2, Green
TPIAP					Twisted-Pair A, positive
TPIAN					Twisted-Pair A, negative
TPIBP					Twisted-Pair B, positive
TPIBN					Twisted-Pair B, negative
TPICP					Twisted-Pair C, positive
TPICN					Twisted-Pair C, negative
TPIDP					Twisted-Pair D, positive
TPIDN					Twisted-Pair D, negative

Note: 10/100/1000 Ethernet is supported beginning with the Intel Quartus Prime v17.1 software release.

4.9.2. 2x20 GPIO Expansion Header

The Intel Cyclone 10 LP FPGA evaluation board provides one 40-pin expansion GPIO header with up to 36 GPIO signals. This 2x20 GPIO Header is compatible with some Terasic 2x20 GPIO cards.

There are also +5 V (VCC_5V_GPIO) and +3.3 V (VCC_3.3V) and two GND pins on 2x20 GPIO expansion header. All GPIO signals GPIO[0:35] are 3.3 V single-ended LVCMOS/LVTTL signals who are connected to Intel Cyclone 10 LP FPGA directly.

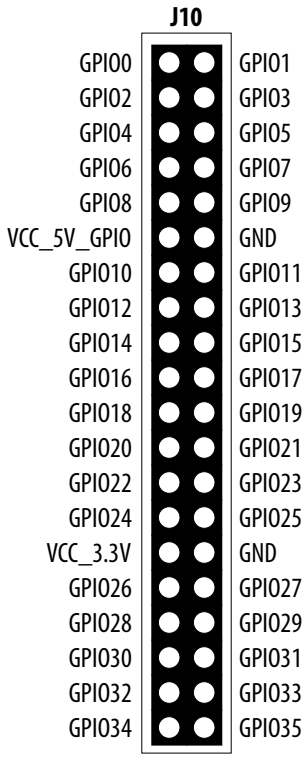
Table 15. 2X20 GPIO Header Signals

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J10.1	GPIO0	L13	3.3 V	IO	GPIO Signal 0
J10.2	GPIO1	L16	3.3 V	IO	GPIO Signal 1
J10.3	GPIO2	L15	3.3 V	IO	GPIO Signal 2
J10.4	GPIO3	K16	3.3 V	IO	GPIO Signal 3
J10.5	GPIO4	P16	3.3 V	IO	GPIO Signal 4
J10.6	GPIO5	R16	3.3 V	IO	GPIO Signal 5
J10.7	GPIO6	N16	3.3 V	IO	GPIO Signal 6
J10.8	GPIO7	N15	3.3 V	IO	GPIO Signal 7
J10.9	GPIO8	N14	3.3 V	IO	GPIO Signal 8
J10.10	GPIO9	P15	3.3 V	IO	GPIO Signal 9
J10.11	VCC_5V_GPIO	---	---	---	Short to VCC_5V
J10.12	GND	---	---	---	Ground
J10.13	GPIO10	N8	3.3 V	IO	GPIO Signal 10
J10.14	GPIO11	P8	3.3 V	IO	GPIO Signal 11
J10.15	GPIO12	M8	3.3 V	IO	GPIO Signal 12
J10.16	GPIO13	L8	3.3 V	IO	GPIO Signal 13
J10.17	GPIO14	R7	3.3 V	IO	GPIO Signal 14
J10.18	GPIO15	T7	3.3 V	IO	GPIO Signal 15
J10.19	GPIO16	L7	3.3 V	IO	GPIO Signal 16
J10.20	GPIO17	M7	3.3 V	IO	GPIO Signal 17
J10.21	GPIO18	R6	3.3 V	IO	GPIO Signal 18
J10.22	GPIO19	T6	3.3 V	IO	GPIO Signal 19
J10.23	GPIO20	T2	3.3 V	IO	GPIO Signal 20
J10.24	GPIO21	M6	3.3 V	IO	GPIO Signal 21
J10.25	GPIO22	R5	3.3 V	IO	GPIO Signal 22
J10.26	GPIO23	T5	3.3 V	IO	GPIO Signal 23

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J10.27	GPIO24	N5	3.3 V	IO	GPIO Signal 24
J10.28	GPIO25	N6	3.3 V	IO	GPIO Signal 25
J10.29	VCC_3.3V	---	---	---	VCC_3.3V
J10.30	GND	---	---	---	Ground
J10.31	GPIO26	R4	3.3 V	IO	GPIO Signal 26
J10.32	GPIO27	T4	3.3 V	IO	GPIO Signal 27
J10.33	GPIO28	N3	3.3 V	IO	GPIO Signal 28
J10.34	GPIO29	P3	3.3 V	IO	GPIO Signal 29
J10.35	GPIO30	R3	3.3 V	IO	GPIO Signal 30
J10.36	GPIO31	T3	3.3 V	IO	GPIO Signal 31
J10.37	GPIO32	P6	3.3 V	IO	GPIO Signal 32
J10.38	GPIO33	P2	3.3 V	IO	GPIO Signal 33
J10.39	GPIO34	P1	3.3 V	IO	GPIO Signal 34
J10.40	GPIO35	R1	3.3 V	IO	GPIO Signal 35

Figure 8. GPIO



The maximum power output capability is shown in the table below. When using 2x20 GPIO Header, USB may not provide sufficient power. Hence, use an external adapter connector (J12) to power up the board.

Table 16. 2X20 GPIO Header Power Output Capability

PowerRail	Output Pin Location	Max Current	Note
VCC_5V_GPIO	J10.11	0.5 A	VCC_5V output capability to card (depends on the power adapter capability)
VCC_3.3V	J10.29	0.5 A	VCC_3.3V output capability to daughter card

4.9.3. Arduino Connectors

The Intel Cyclone 10 LP FPGA Evaluation Board features an Arduino UNO R3 type interface which is comprised of headers J4, J5, J6, J7, J18.

The header's location is compatible with Arduino UNO R3. This interface contains 17 digital IOs (include one Reset) and six Analog inputs.

The header's location and definition are shown in the figure below.

Figure 9. Arduino Connector

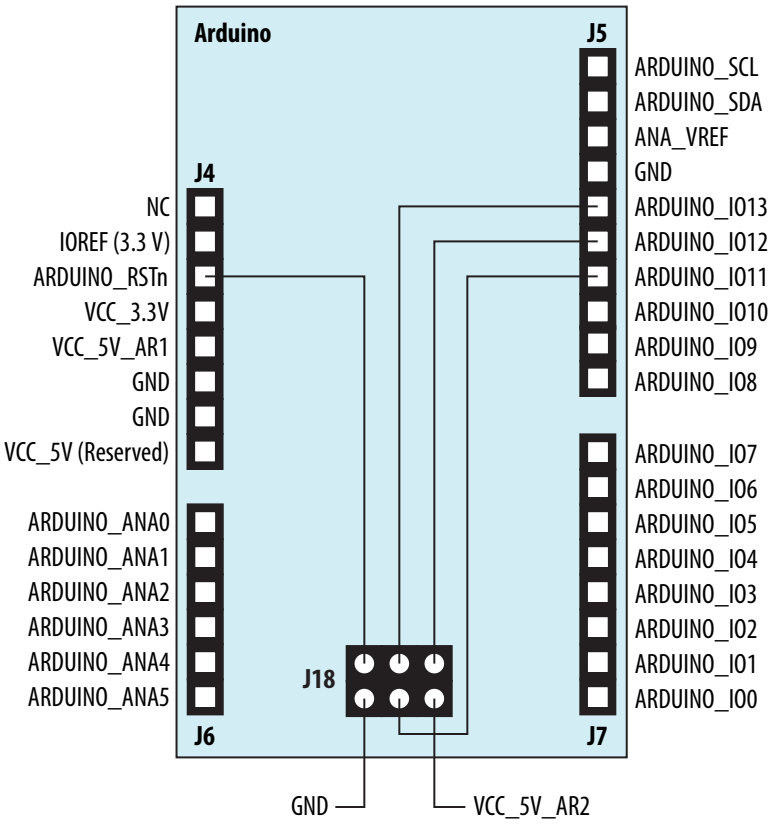


Table 17. Arduino Connector

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
Header 1 (PWR) J4.1	NC	---			
J4.2	IOREF	---	---	---	Connected to VCC_3.3V
J4.3	ARDUINO_RSTn	L3	3.3 V	In	Arduino Reset Input
J4.4	VCC_3.3V	---			3.3 V Power for Arduino shield
J4.5	VCC_5V_AR1				5 V Power for Arduino shield shared with VCC_5V
J4.6	GND				
J4.7	GND				
J4.8	NC				Reserve option to 5 V
Header 2 (Analog) J6.1	ARDUINO_ANA0	---	Analog	In	Arduino Analog Channel 0
J6.2	ARDUINO_ANA1	---	Analog	In	Arduino Analog Channel 1
J6.3	ARDUINO_ANA2	---	Analog	In	Arduino Analog Channel 2
J6.4	ARDUINO_ANA3	---	Analog	In	Arduino Analog Channel 3
J6.5	ARDUINO_ANA4	---	Analog	In	Arduino Analog Channel 4
J6.6	ARDUINO_ANA5	---	Analog	In	Arduino Analog Channel 5
Header 3 (Digital) J5.1	ARDUINO_IO8	K2	3.3 V	IO	Arduino Digital Bit 8
J5.2	ARDUINO_IO9	K5	3.3 V	IO	Arduino Digital Bit 9
J5.3	ARDUINO_IO10	L4	3.3 V	IO	Arduino Digital Bit 10
J5.4	ARDUINO_IO11	K1	3.3 V	IO	Arduino Digital 11
J5.5	ARDUINO_IO12	L2	3.3 V	IO	Arduino Digital 12
J5.6	ARDUINO_IO13	L1	3.3 V	IO	Arduino Digital 13
J5.7	GND	---	GND	---	---
J5.8	ANA_VREF	---	Analog	In	Arduino Analog Reference Voltage Reserved
J5.9	ARDUINO_SDA	N2	3.3 V	IO	Arduino I^2C Data
J5.10	ARDUINO_SCL	N1	3.3 V	IO	Arduino I^2C Clock

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
Header 4 (Digital) J7.1	ARDUINO_IO0	B1	3.3 V	IO	Arduino Digital Bit 0
J7.2	ARDUINO_IO1	C2	3.3 V	IO	Arduino Digital Bit 1
J7.3	ARDUINO_IO2	F3	3.3 V	IO	Arduino Digital Bit 2
J7.4	ARDUINO_IO3	D1	3.3 V	IO	Arduino Digital Bit 3
J7.5	ARDUINO_IO4	G2	3.3 V	IO	Arduino Digital Bit 4
J7.6	ARDUINO_IO5	G1	3.3 V	IO	Arduino Digital Bit 5
J7.7	ARDUINO_IO6	J2	3.3 V	IO	Arduino Digital Bit 6
J7.8	ARDUINO_IO7	J1	3.3 V	IO	Arduino Digital Bit 7
Header 5 (ICSP) J18.1	ARDUINO_IO12	L2	3.3 V	IO	Short to Arduino Digital Bit 12
J18.2	VCC_5V_AR2	---	---	---	5 V Power for Arduino shield, shared with VCC_5v
J18.3	ARDUINO_IO13	L1	3.3 V	IO	Short to Arduino Digital Bit 13
J18.4	ARDUINO_IO11	K1	3.3 V	IO	Short to Arduino Digital Bit 11
J18.5	ARDUINO_RSTn	L3	3.3 V	In	Short to Arduino Reset Input
J18.6	GND	---	---	---	---

4.9.3.1. Digital IOs

There are 17 one-bit Arduino digital IOs on Arduino connectors which are connected to the FPGA on the board. They are all 3.3 V single-ended IOs.

Caution: The Arduino interface only supports 3.3 V I/O. Care must be taken when you connect a shield into the connectors.

4.9.3.2. Analog Inputs

There are six analog inputs can be sourced through the Arduino header J6. These analog signals are first divided and filtered by operational amplifier MCP6242 and related components. This circuit scales the maximum allowable analog input to 5 V which meets standard Arduino UNO R3.

The Intel MAX 10 device (U3) features one ADC block with one dedicated analog input and 8 dual function pins. Six of the nine analog input pins are used for the Arduino analog input interface. The other three are used for current sense.

Table 18. Arduino Channel Connections

Arduino Connector	ADC Channel	MAX 10 ADC Name	MAX10 Pin
ARDUINO_ANA0 (J6.1)	ADC1 Channel5	ADC1IN5	U3.C1
ARDUINO_ANA1 (J6.2)	ADC1 Channel0 (Dedicated Channel)	ANAIN1	U3.D2
ARDUINO_ANA2 (J6.3)	ADC1 Channel1	ADC1IN1	U3.D1
ARDUINO_ANA3 (J6.4)	ADC1 Channel8	ADC1IN8	U3.E1
ARDUINO_ANA4 (J6.5)	ADC1 Channel7	ADC1IN7	U3.F1
ARDUINO_ANA5 (J6.6)	ADC1 Channel4	ADC1IN4	U3.E4

Intel Cyclone 10 LP FPGA device communicates with the ADC block in the Intel MAX 10 device on the board through the ADC I^2C interface, which supports both 100 KHz and 400 KHz I^2C clock frequency. The ADC output value is 12-bit data and I^2C data is 8-bit. Hence two register addresses are used to store 12-bit ADC output data. These registers are all read only. The ADC I^2C slave address of ADC block is 0x5E.

Table 19. Register Addresses for Arduino Channels

Arduino Connector	Register Address
ARDUINO_ANA0 (J6.1)	0x31, 0x30
ARDUINO_ANA1 (J6.2)	0x27, 0x26
ARDUINO_ANA2 (J6.3)	0x29, 0x28
ARDUINO_ANA3 (J6.4)	0x37, 0x36
ARDUINO_ANA4 (J6.5)	0x35, 0x34
ARDUINO_ANA5 (J6.6)	0x2F, 0x2E

Use the formula to covert ADC output value to voltage:

```
Voltage = (ADC_Output_Value/4096) * VREF * R_Divider
```

- ADC_Output_Value is the value in Decimal read from ADC I^2C bus as described above.
- VREF is the MAX 10 ADC reference voltage. Use 3.3 V when using MAX 10 internal reference source.
- R_Divider[(2)] is a resistors divider value along with operational amplifier MCP6242 in order to allow tolerance up to 5 V analog input. By default, it is 2.

For example, if you want to measure analog input value on ARDUINO_ANA0 (J6.1).

1. Read value of 0x30 register address is 0xB9 and read value of 0x31 register address is 0x3, then the ADC output value is 0x3B9, or in decimal, 953. Hence,

```
ADC_Output_Value=953
```

(2) Different analog outputs on Arduino shield have different output impedance, these divider resistor values may need to be adjusted based on your application.

2. MAX 10 internal reference voltage is used so

```
VREF = 3.3 V
```

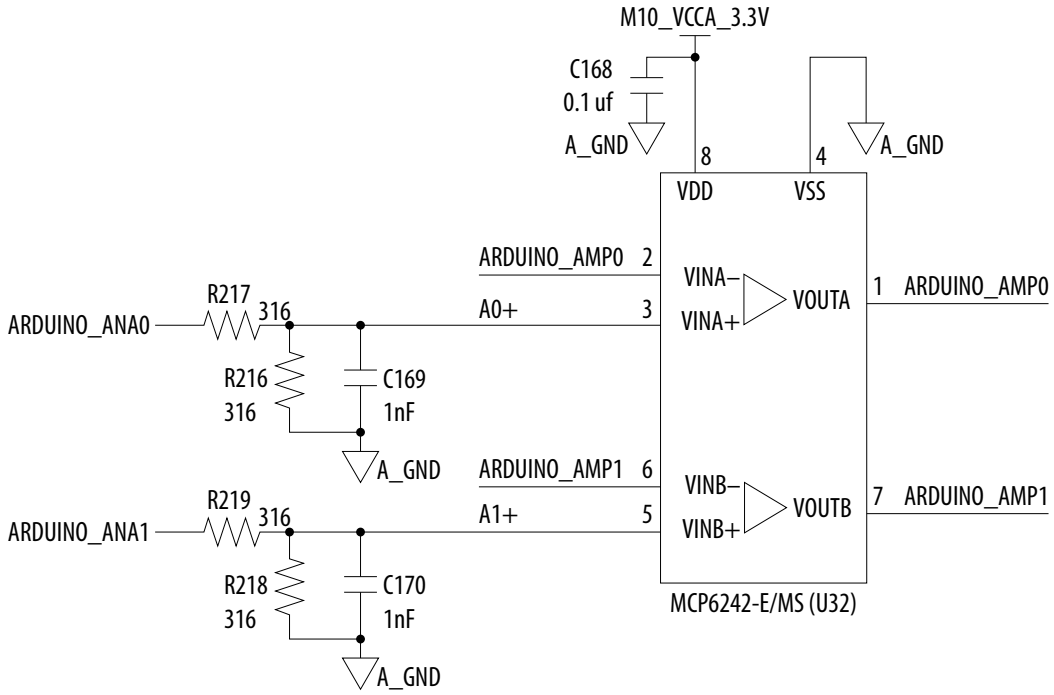
3. Divider resistor values are R217 = 316 ohm and R216 = 316 ohm, so

```
R_Divider = R217/R216 + 1 = 2
```

4. Calculated the analog signal voltage on ARDUINO_ANA0 (J6.1) is

```
Voltage @ ARDUINO_ANA0 = (953/4096) * 3.3 * 2 = 1.54 V
```

Figure 10. Arduino Analog Input Calculation Example



4.9.3.3. Arduino Power

There are several power rails on the Arduino connectors.

- **IOREF**: 3.3 V for digital IOs. It must be 3.3 V. 5 V is forbidden as it may damage devices on the board.
- **VCC_3.3V**: 3.3 V power generated by Intel Cyclone 10 LP FPGA Evaluation Board.
- **VCC_5V_AR1/2**: 5 V power from Intel Cyclone 10 LP FPGA Evaluation Board.
- **ARDUINO_AREF**: Reserved analog reference voltage. Care must be taken that the range can be 0 ~3.3 V. 5 V is forbidden.

When using Arduino connector, USB may not provide sufficient power so we suggest you use external adapter connector (J12) to power up the board.

Arduino UNO R3 did not specify limitation of output current capability. The following table shows the maximum output current for the Intel Cyclone 10 LP FPGA Evaluation Board.

Table 20. Arduino Power Output Capability

Power Rail	Output Pin Location	Maximum Current	Note
VCC_5V_AR1 VCC_5V_AR2	J4.5 J18.2	0.5 A	5 V output capability to Arduino Shield, shared with VCC_5V (depends on the power adapter specification)
VCC_3.3V	J4.4	0.05 A	VCC_3.3V output capability to Arduino Shield
IOREF	J4.2	0.05 A	Connected to VCC_3.3V

4.9.4. Pmod Connectors

The Intel Cyclone 10 LP FPGA Evaluation Board features one Digilent Pmod™ Compatible header which is used to connect low frequency, low I/O pin count peripheral module.

The 12-pin version Pmod connector is chosen and this provides 8 I/O signal pins. The peripheral module interface also encompasses a variant using I2C interface and two or four wire MTE cables. The Pmod signals are connected to FPGA Bank 6.

Table 21. Pmod Signals

Board Reference	Schematic Signal Name	Schematic Share Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
Pmod (J8)	PMOD_D0	PMOD_IO0	D16	3.3 V	IO	Pmod IO 0
	PMOD_D1	PMOD_IO1	F13	3.3 V	IO	Pmod IO 1
	PMOD_D2	PMOD_IO2	D15	3.3 V	IO	Pmod IO 2
	PMOD_D3	PMOD_IO3	F16	3.3 V	IO	Pmod IO 3
	PMOD_D4	PMOD_IO4	C16	3.3 V	IO	Pmod IO 4
	PMOD_D5	PMOD_IO5	F15	3.3 V	IO	Pmod IO 5
	PMOD_D6	PMOD_IO6	C15	3.3 V	IO	Pmod IO 6
	PMOD_D7	PMOD_IO7	B16	3.3 V	IO	Pmod IO 7

The Pmod specification does not specify module power consumption, but assumes no more than approximately 100 mA. On this board, the Pmod connector can offer up to 250 mA @ 3.3 V when the board is powered from external adapter connector (J12).

When using the Pmod module, the USB may not provide sufficient power. Intel recommends that you use an external adapter connector (J12) to power up the board.

Table 22. Pmod Header Power Output Capability

Power Rail	Output Pin Location	Maximum Current	Note
VCC_3.3 V	J8.6, J8.12	0.25A	VCC_3.3 V output capability to Pmod module

4.10. Memory

4.10.1. HyperRAM

HyperRAM is a portfolio of high-speed, low-pin-count memory product that uses the HyperBus interface technology. The Intel Cyclone 10 LP FPGA Evaluation Board supports HyperRAM with HyperBus Controller (HBMC) IP provided by Synaptic Labs.

One of the following HyperRAM parts is used:

- ISSI IS66WVH16M8ALL-166B1LI
- Cypress S70KS1281DPBHI020

HyperRAM is organized by 16M words x 8 bits with 1.8 V interface.

Table 23. HyperRAM Signals List

Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
HBUS_DQ7	R13	1.8 V	IO	Data Input/Output Bit 7
HBUS_DQ6	R12	1.8 V	IO	Data Input/Output Bit 6
HBUS_DQ5	R11	1.8 V	IO	Data Input/Output Bit 5
HBUS_DQ4	T10	1.8 V	IO	Data Input/Output Bit 4
HBUS_DQ3	R10	1.8 V	IO	Data Input/Output Bit 3
HBUS_DQ2	T11	1.8 V	IO	Data Input/Output Bit 2
HBUS_DQ1	T13	1.8 V	IO	Data Input/Output Bit 1
HBUS_DQ0	T12	1.8 V	IO	Data Input/Output Bit 0
HBUS_CKp	P14	1.8 V	OUT	Differential Clock, Positive Node
HBUS_CKn	R14	1.8 V	OUT	Differential Clock, Negative Node
HBUS_CS2n	P9	1.8 V	OUT	Chip Select for HyperRAM
HBUS_RWDS	T14	1.8 V	IO	Read Write Data Strobe
HBUS_RSTn	N9	1.8 V	OUT	Hardware Reset
HBUS_CS1n	N12	1.8 V	OUT	Chip Select for Hyper FLASH (Reserved Only)
HBUS_RSTOn	T15	1.8 V	IN	Reset Output from slave to master (Reserved Only)
HBUS_INTn	P11	1.8 V	IN	Interrupt Output from slave to master (Reserved Only)

Note: The Synaptic Labs HyperBus® Memory Controller IP (HBMC) for Intel FPGA is available in a Basic Edition (OpenCore) and a Full Edition. The differences are listed in the following table.

Table 24. HBMC Features by Edition

	Basic Edition	Full Edition
License required	Trial license	Node-locked license
.sof file supports conversion to other formats	No	Yes
.sof file runs on the BTS	No	Yes
Burst lengths supported	1 or 8	1, 2, 4, 8, 16, 32, 64 or 128

Note: Contact Synaptic Labs to download the HBMC license and the latest version of the HBMC IP.

Related Information

Synaptic Labs Website

4.10.2. EPCQ or EPCQ-A Flash Memory

The Intel Cyclone 10 LP FPGA Evaluation board has an Intel 64 Mb EPCQ64 or 128 Mb EPCQ128A in-system programmable NOR flash for non-volatile storage of the FPGA configuration data, board information, test application data and user code space.

Depending on its revision, your board has one of two flash memory devices: EPCQ64 or EPCQ128A. To determine which device you have, refer to "Evaluation Board Revisions".

Although the quad-serial flash provided has a ×4 data width, the evaluation board has a ×1 data width because the Intel Cyclone 10 LP FPGA only supports an AS ×1 configuration scheme. Other data signals are tied to 3.3 V power required by the device datasheet.

The table below shows the memory map for this flash memory. This memory provides non-volatile storage for FPGA bit stream, Nios II factory software and other information.

Table 25. Flash Memory Map

Block Description	Size (KB)	Address	Comments
Board Test System Scratch	512	0x0073.0000 - 0x007A.FFFF	BTS System Testing
Board Information	64	0x0072.0000 - 0x0072.FFFF	Board Information
Ethernet Option Bits	64	0x0071.0000 - 0x0071.FFFF	MAC Address Information
User Design Reset Vector	64	0x0070.0000 - 0x0070.FFFF	Nios II Reset Vector Information
Factory Software (ELF)	4096	0x0030.0000 - 0x006F.FFFF	Software File
Factory Hardware (sof)	3072	0x0000.0000 - 0x002F.FFFF	SOF File
Total	7872		

The signal connections between the Intel Cyclone 10 LP FPGA and flash comply with the AS ×1 configuration requirements.

Table 26. Signal Connections

Flash Pin Number	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
U2.16	C10_AS_DCLK	U1.H1	3.3 V	FPGA Clock Output
U2.7	C10_AS_CSn	U1.D2	3.3 V	FPGA Chip Select Output
U2.8	C10_AS_DATA0	U1.H2	3.3 V	FPGA Data Input
U2.15	C10_AS_ASDO	U1.C1	3.3 V	FPGA Data and Control Signals Output

Note: When using a serial flash loader (SFL) core and the Intel Quartus Prime Programmer to erase and program the flash, virtual JTAG must be bypassed by setting the SW1.4 switch to ON. Signal Net VTAP_BYPASSn is logic 0.

Related Information

Evaluation Board Revisions on page 6

4.11. System Power

4.11.1. Power Supply Options

There are two power supply options provided for the Intel Cyclone 10 LP FPGA Evaluation Board. The first is USB powered and the second is external AC/DC adapter powered. These two options can be used for different applications. There is an ORING circuit on-board to select suitable power source from USB power or DC jack.

USB-Power

A standard A to Mini-B USB Y-Cable is shipped with the evaluation board. There are three USB ports as listed in the following table.

Table 27. USB Ports

Port	Description
P1	• USB Standard A Plug. • Connects to USB host • Used for both USB signals and USB VBUS 5 V
P2	• Complementary USB Standard A plug for additional USB VBUS 5 V power. • No signal connection.
P3	• USB Mini-B Plug • Connected to USB Port J17

When P1 and P2 are plugged into USB Host ports at the same time, it can supply up to 1A current to the Intel Cyclone 10 LP FPGA Evaluation Board.

Figure 11. USB Y-Cable

AC/DC Adapter Power

The DC Jack uses Wurth Elektronik P/N 694106301002 as power input connector.

The required DC mate plug is required to meet the parameters below

- Inner Diameter (ID): 2.1 mm
- Outer Diameter (OD): 5.5 mm
- Voltage: 5 V
- Center Polarity: Positive (5 V)

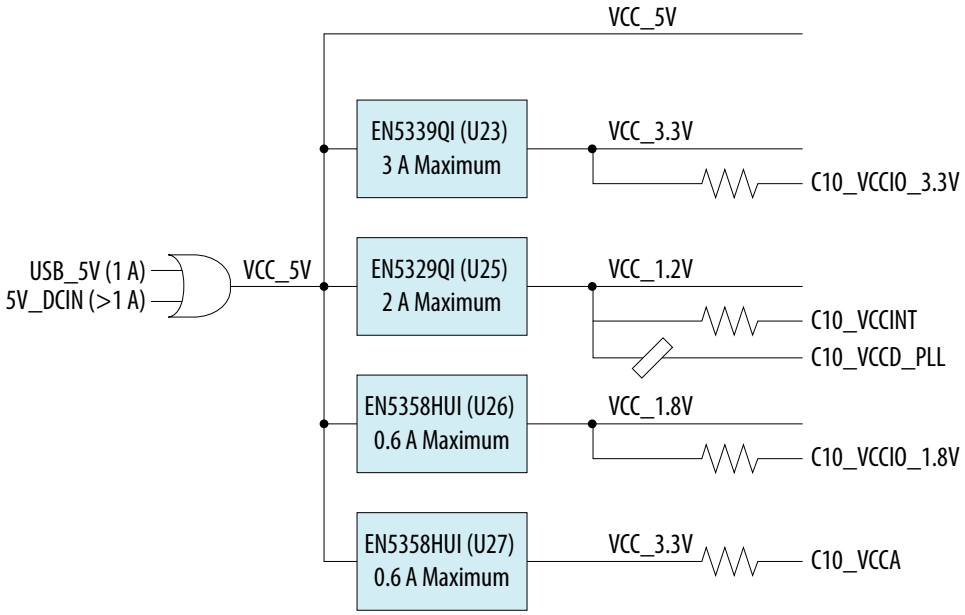
Caution: Use 5 V adapter for DC Jack J12 only. Components on the board can get damaged by power supplies with greater voltage.

Related Information

- Powering Up the Evaluation Board on page 10
- Evaluation Kit Description on page 4

4.11.2. Power Tree

Figure 12. Intel Cyclone 10 LP FPGA Evaluation Board Power Tree



No special power up or down sequence control is required, because the Intel Cyclone 10 LP FPGA can be powered up and down in any sequence.

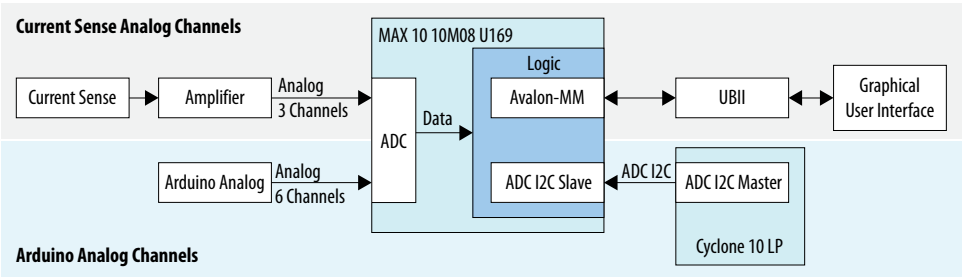
4.11.3. Current Measurement

To demonstrate low power feature, Intel Cyclone 10 LP FPGA power rails are isolated with resistors for voltage drop measurement either manually or automatically.

VCCINT, VCCA and VCCIO_3.3V supports automatic current measurement. The voltage drop across sense resistors are connected to Intel MAX 10 integrated ADC with current sense amplifiers. Refer to the figure below.

The selected Intel MAX 10 10M08SA-U169 contains one ADC with 9 analog input channels. Three channels are used for Intel Cyclone 10 LP FPGA current measurement and six channels are used for Arduino analog.

Figure 13. Current Measurement



Other Intel Cyclone 10 LP FPGA power rails support manual measurement by measure voltage drop across sensing resistors with a multi-meter.

5. Simple Socket Server

The Intel Cyclone 10 LP FPGA Evaluation Board ships with the Simple Socket Server design example stored in the factory portion of the flash memory. The design consists of a Nios II embedded processor and an Ethernet MAC.

Note: The Intel Cyclone 10 LP Evaluation Board Rev A1 hardware design does not include Ethernet MAC support. If you have a Rev A1 board, download and install the Rev A2 design. Refer to "Installing the Evaluation Kit Collateral" for instructions to download the Rev A2 design.

When you power up the board, the Intel Cyclone 10 LP FPGA configures with the Simple Socket Server design example. The design can obtain an IP address from any DHCP server and serve a telnet server to any host computer on the same network. The telnet server allows you to control the LEDs on the board.

The source code for the Simple Socket Server design resides in the `<package dir>\examples\golden_system_ref_design` directory. If the Simple Socket Server is corrupted or deleted from the flash memory, you might need to restore the board's original contents, using the BTS application.

Related Information

- Recovering Factory Default Settings on page 11
  How to restore the board's original factory contents using the BTS application
- Evaluation Board Revisions on page 6
- Installing the Evaluation Kit Collateral on page 8

5.1. Connecting to the Simple Socket Server

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP-enabled network.
- A separate working Ethernet port for the board, connected to the same network.
- The Ethernet cable, USB power cables, and evaluation board that are included in the kit.

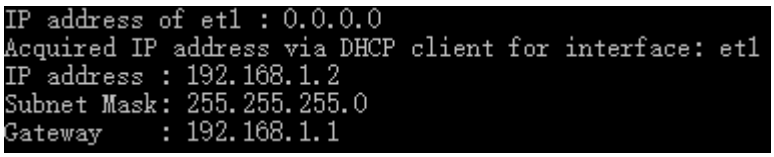
Follow these instructions to connect to the Simple Socket Server.

1. Install the latest Intel software tools, including the Intel Quartus Prime software, Nios II processor and IP functions. If necessary, download the Intel Quartus Prime Standard Edition software.
2. Attach the Ethernet cable from the board to the LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address.
4. Launch the Nios II command shell and type the following command:

nios2-terminal.exe

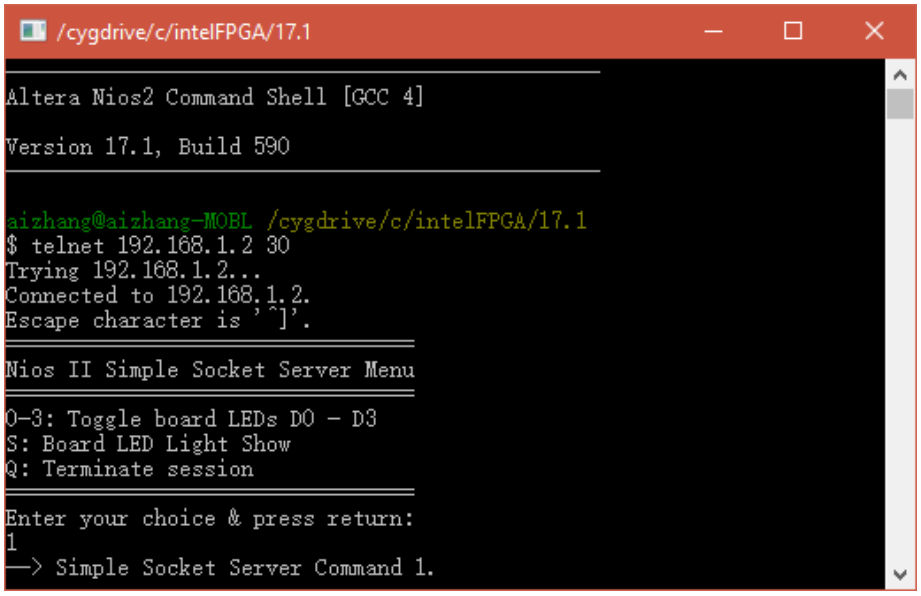
When the IP address is assigned, it is displayed as shown in the following figure.

Figure 14. IP Address in Nios II Command Shell



After configuring with the Simple Socket Server design example, you can see the four LEDs lighting at the same time. You can access the telnet server from the Nios II command shell as shown in the following figure.

Figure 15. Accessing telnet from the Nios II Command Shell

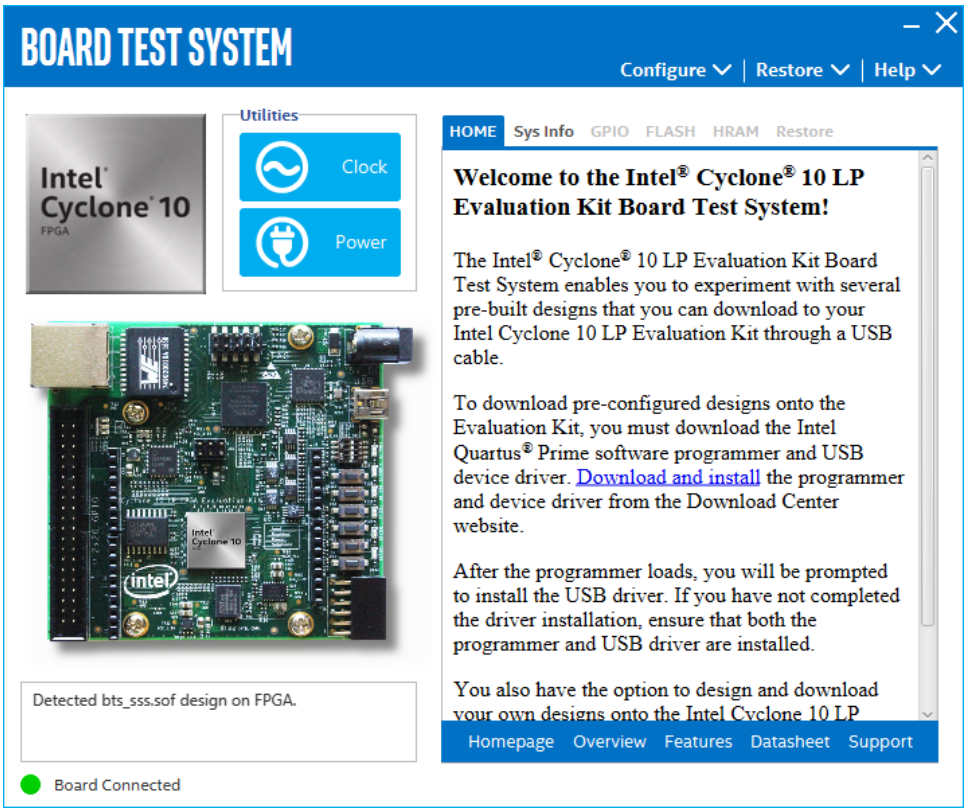


In this example, the IP address of the board is 192.168.1.2, and the server port is 30.

6. Board Test System

The evaluation kit collateral includes an application called the Board Test System (BTS). The BTS provides an easy-to-use interface to alter the functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance and measure power usage. While using the BTS, you can reconfigure the FPGA several times with test designs specific to the functionality you are testing.

Figure 16. Board Test System (BTS) Graphical User Interface (GUI)



Several designs are provided to test major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

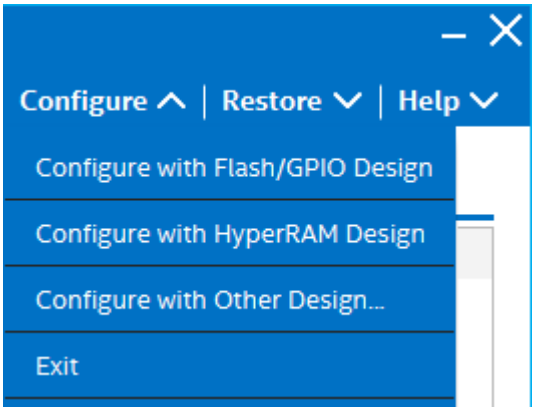
The BTS communicates over the JTAG bus to a test design running in the FPGA. The BTS and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the Signal Tap Embedded Logic Analyzer. As the Intel Quartus Prime uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time-out.

Note: Close other applications before attempting to reconfigure the FPGA using the Intel Quartus Prime Programmer.

6.1. The Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

Figure 17. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click Configure to download the corresponding design to the FPGA.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

6.2. The System Info Tab

The **System Info** tab shows the board's current configuration. The tab displays the JTAG chain, the board's MAC address and other details stored on the board.

Figure 18. The System Info Tab

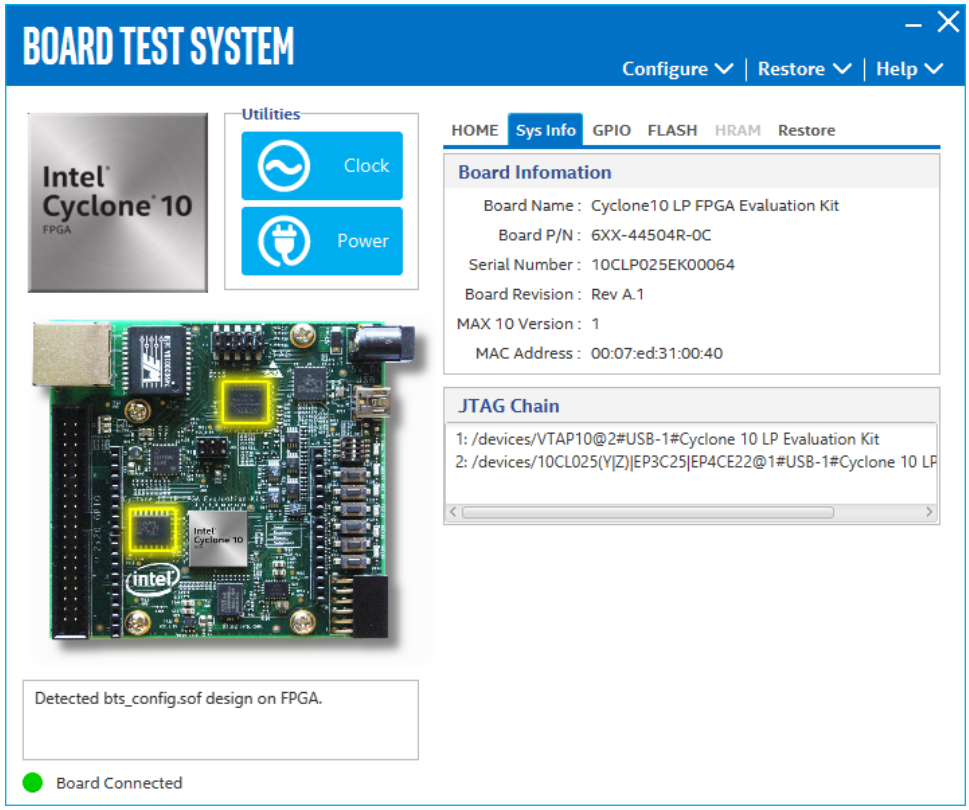


Table 28. The System Info Tab Controls

Controls	Description
Board Information	The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board.
Board Name	Indicates the official name of the board, given by the Board Test System.
Board P/N	Indicates the part number of the board.
Serial Number	Indicates the serial number of the board.
Board Revision	Indicates the version of the Board.
MAX 10 Version	Indicates the version of MAX code currently running on the board.
MAC Address	Indicates the Ethernet MAC address of the board.
JTAG Chain	Shows all the devices currently in the JTAG chain.

6.3. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off, detect push button presses and Platform Designer (Standard) Memory Map of GPIO design is displayed here.

Figure 19. The GPIO Tab

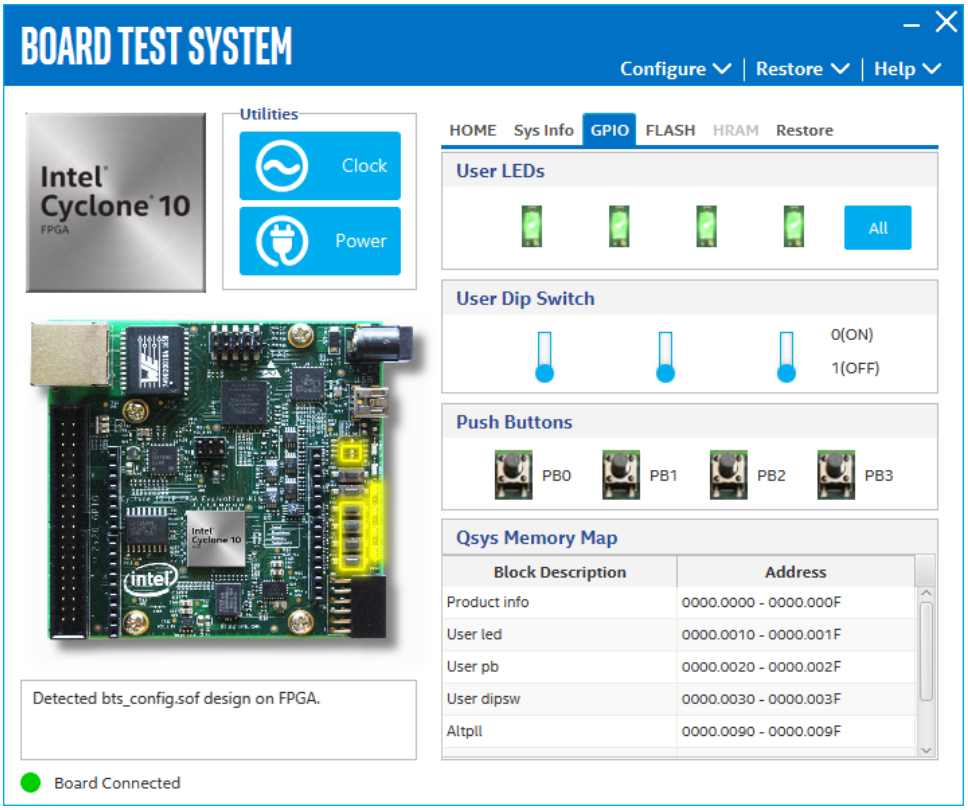


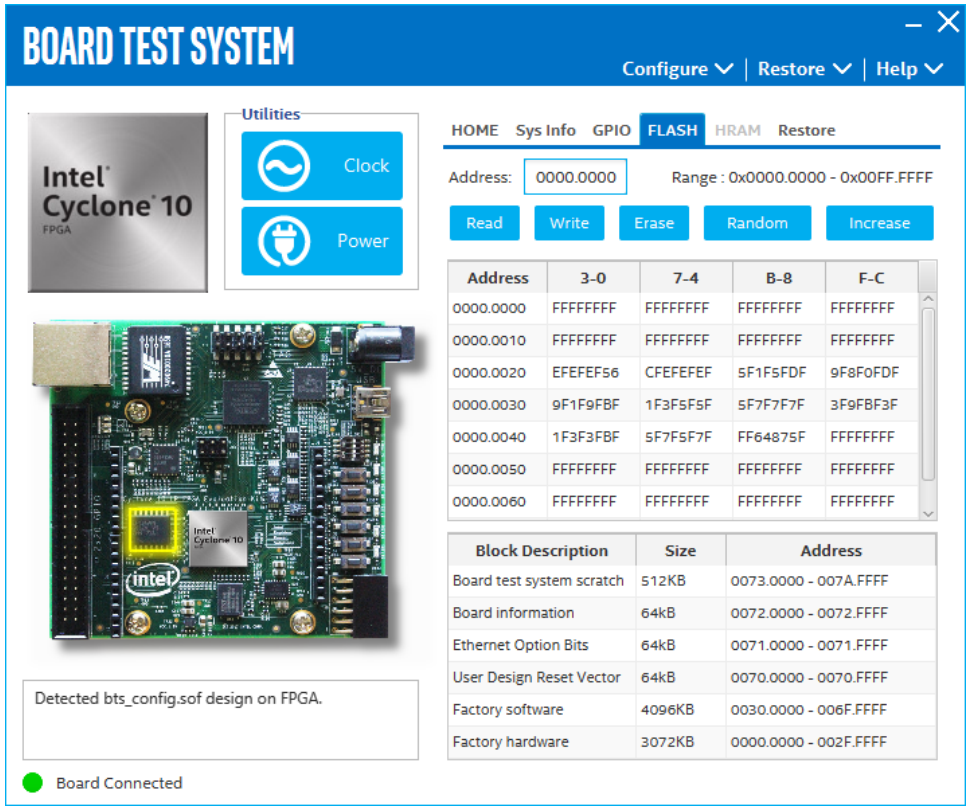
Table 29. The GPIO Tab Controls

Control	Description
User LEDs	Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click the **0** to **3** buttons to toggle red or green LEDs, or click the **All** button.
User DIP Switch	Displays the current positions of the switches in the user DIP switch banks. Change the switches on the board to see the graphical display change accordingly.
Push Buttons	Read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.
Qsys Memory Map	Shows the memory map of the current bts_config design on your board, as determined by Platform Designer (Standard) (formerly known as Qsys).

6.4. The Flash Tab

The **Flash** Tab allows you to read and write flash memory on your board.

Figure 20. The Flash Tab



Control	Description
Read	Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table.
Write	Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.
Erase	Erases flash memory.
Increase	Starts an incrementing data pattern test to flash memory, limited to the 512 K test system scratch page.
Random	Starts a random data pattern test to flash memory, limited to the 512 K test system scratch page.
Flash Memory Map	Displays the flash memory map for the development board.

6.5. The HyperRAM Tab

The **HyperRAM** tab allows you to test the HyperRAM by reading and writing to a selected number of addresses with selectable burst length. The supported burst lengths are 2, 4, 8, 16, 32, 64, and 128.

Figure 21. The HyperRAM Tab

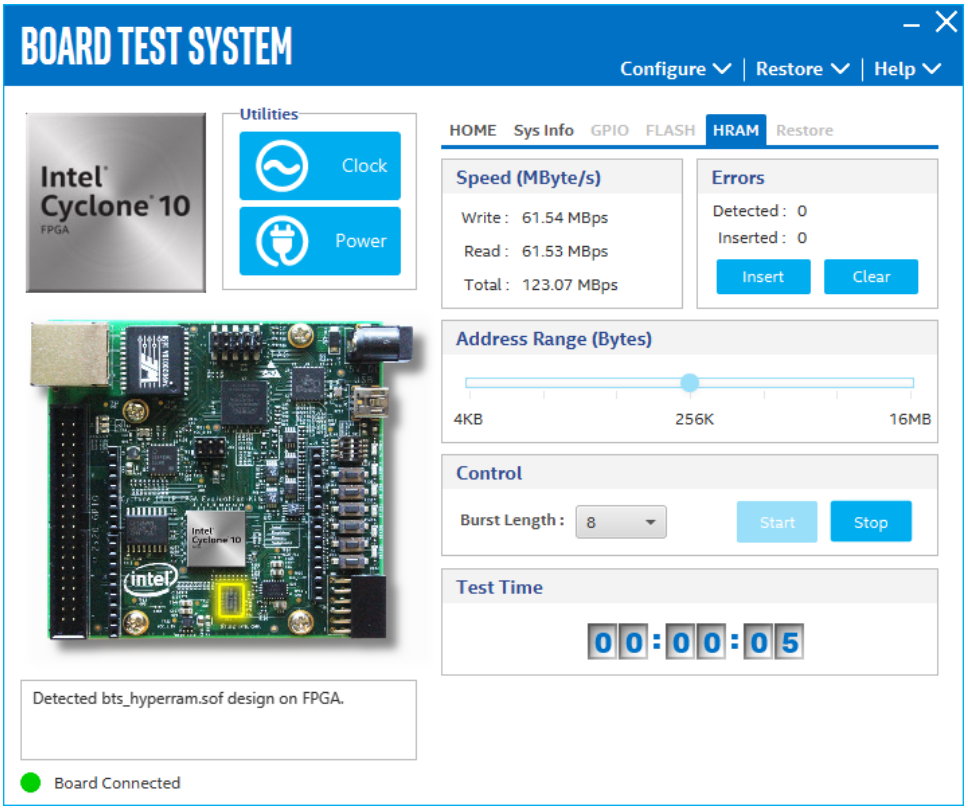


Table 30. The HyperRAM Tab Controls

Control	Description
Speed (MByte/s)	• **Write**, **Read**, and **Total**—Show the number of bytes of data analyzed per second. The data bus is 8 bits wide and the frequency is 150 MHz double data rate. With 300 megabits per second (Mbps) per pin, the theoretical maximum bandwidth is 2400 Mbps or 300 MByte/s.
Errors	These controls display data errors detected during analysis and allow you to insert errors. • **Detected**—Displays the number of data errors detected in the hardware. • **Inserted**—Displays the number of errors inserted into the transaction stream. • **Insert**—Inserts a one-word error into the transaction stream each time you click the button. **Insert** is only enabled during transaction performance analysis. *Note:* For Address Range of 16 MB, ensure the interval between two clicks on **Insert** button is larger than the one during testing. • **Clear**—Resets the Detected errors and Inserted errors counters to zeroes.

continued...

Control	Description
Address Range (Bytes)	Determines the number of addresses to use in each iteration of reads and writes.
Test Times	This item displays test times since you last clicked **Start**.
Control	• **Burst Length**—Allows you to change the burst length of the design. Supported burst lengths are 2, 4, 8, 16, 32, 64, and 128. • **Start**—Start HyperRAM testing • **Stop**—Stop HyperRAM testing

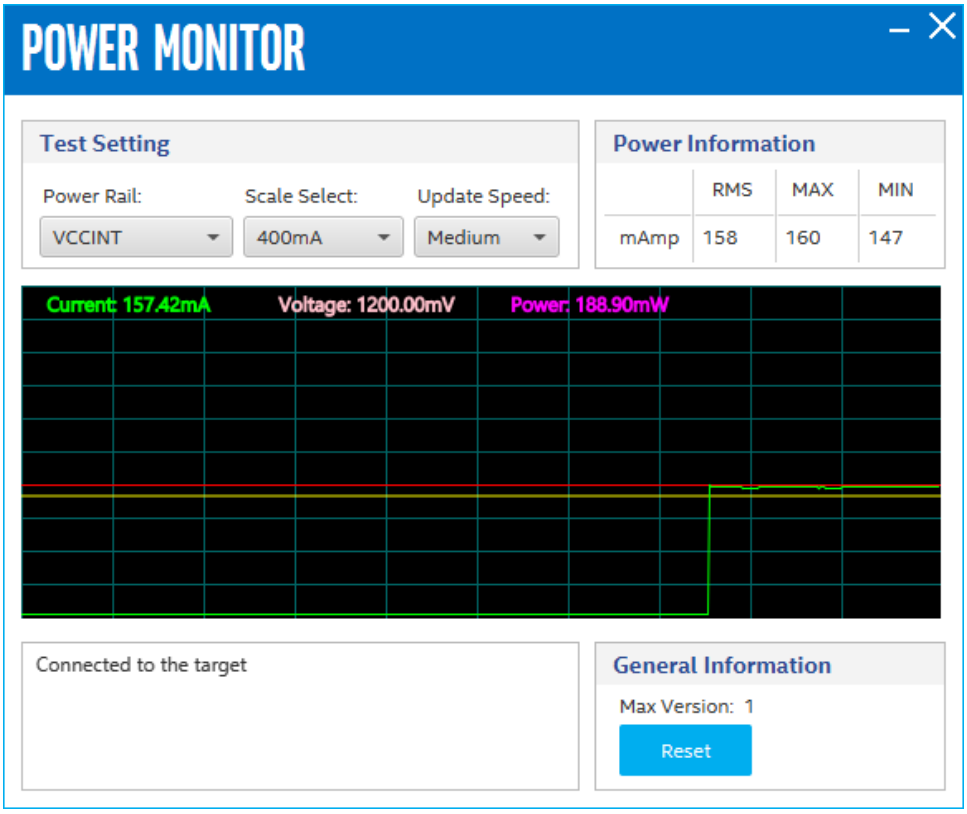
6.6. The Power Monitor

The Power Monitor measures and reports current power information and communicates with the Intel MAX 10 device on the board through the JTAG bus. A power monitor circuit attached to the Intel MAX 10 device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the Board Test System application. You can also run the Power Monitor as a stand-alone application. The `PowerMonitor.exe` resides in the `<package dir>\examples\board_test_system` directory.

Caution: You cannot run the stand-alone power application and the BTS application at the same time.

Figure 22. The Power Monitor



This window displays Intel Cyclone 10 LP current monitors.

Current shows the current value of each power rail:

- 3.3 V VCCIO
- 2.5 V VCCA
- 1.2 V VCCINT

Voltage shows the typical voltage value of each power rail. It is not read from ADC.

Update Speed allows you to select how often the display updates the values:

- **Slow**—every 2 seconds
- **Medium**—every 500 ms
- **Fast** (default)—every 100 ms

6.7. The Clock Control

The Intel Cyclone 10 LP FPGA Evaluation Kit Clock Control application sets the programmable oscillator to any frequency between 3 KHz and 200 MHz.

The Clock Control communicates with the Intel MAX 10 device on the board through the JTAG bus. The programmable oscillator is connected to the Intel MAX 10 device through a 2-wire serial bus.

Figure 23. The Si5351 Tab

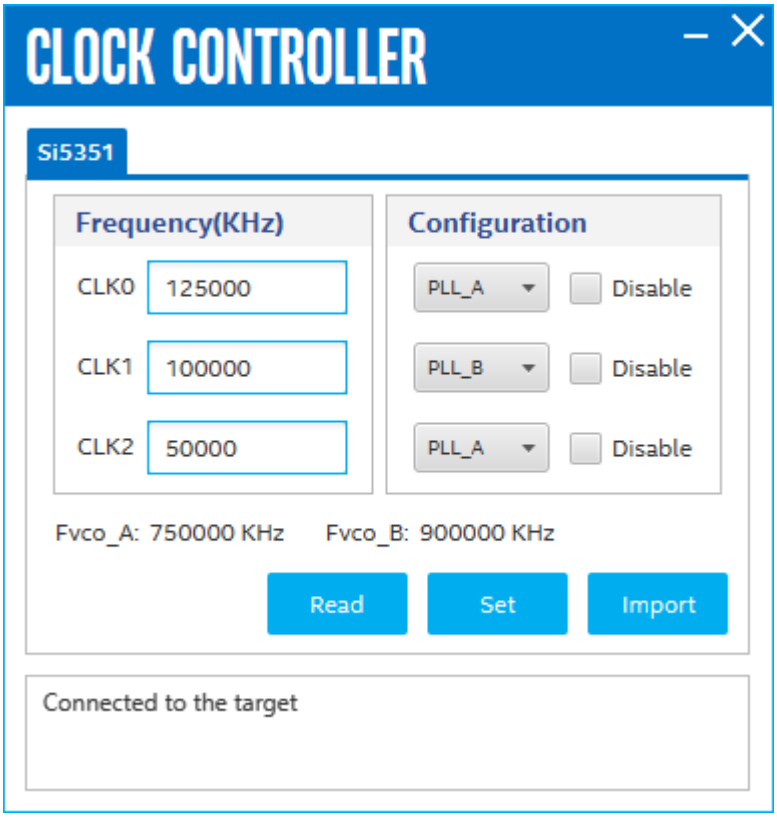


Table 31. The Si5351 Tab Controls

Control	Description
Fvco_A/Fvco_B	Displays the generating signal value of the voltage-controlled oscillator.
Frequency (KHz)	Allows you to specify the frequency of the clock.
PLL Choose	Allows you to specify the PLL used by the clock.
Disable	Disable each clock output as required.
Read	Reads the current frequency setting for the oscillator associated with the active tab.
Set	Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK2 controls. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.
Import	Allows you to import a register table file generated by Clock Builder. You can reset the clock to default by importing the default register file "Si5351A-Registers.txt" in the application folder.

A. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

A.1. Safety Warnings

Power Supply Hazardous Voltage

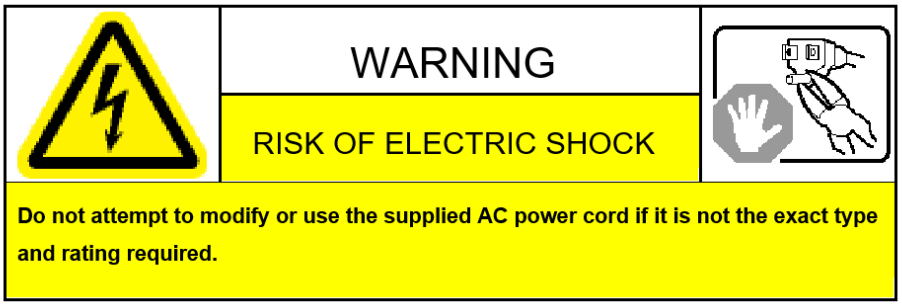
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

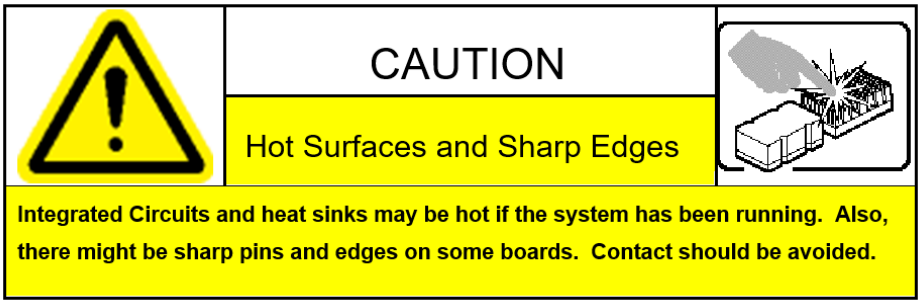
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

A.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

B. Additional Information

B.1. Revision History

Table 32. Document Revision History for Intel Cyclone 10 LP FPGA Evaluation Kit User Guide

Version	Description
2019.12.19	Note added to inform users to contact Synaptic Labs to download HBMC license and latest version of HMBC IP. Updated HyperRAM on page 33.
2018.02.05	• This user guide supports Rev A1 and Rev A2 evaluation boards: — Rev A1: 64 Mb EPCQ flash, ISSI IS66WVH16M8ALL-166B1LI HyperRAM — Rev A2: 128 Mb EPCQ-A flash, Cypress S70KS1281DPBHI020 HyperRAM • Correction to Intel Quartus Prime support: the Intel Cyclone 10 LP device is supported only by Intel Quartus Prime Standard Edition software • New chapter: "Simple Socket Server" • New section in "Evaluation Board Setup" chapter: "Factory Reset" • Changes and additions to BTS GUI • Added the following illustrations: — "Intel Cyclone 10 LP Evaluation Board Part Number Label" — "Board Test System GUI with Restore Menu" — "Restoring Factory Defaults on the Intel Cyclone 10 LP LP FPGA Evaluation Board" • Updated the following illustrations: — "Intel Cyclone 10 LP FPGA Evaluation Board Block Diagram" — "Arduino Connector" — "Accessing telnet from the Nios II Command Shell" — "Board Test System (BTS) Graphical User Interface (GUI)" — "The Configure Menu" — "The System Info Tab" — "The GPIO Tab" — "The Flash Tab" — "The HyperRAM Tab" — "The Power Monitor" — "The Si5351 Tab"
2017.08.23	Preliminary Release

B.2. Compliance and Conformity Statements

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the development board in such a way as to generate

electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development board.

CE

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