Arria 10 GX Transceiver Signal Integrity Development Kit User Guide

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About This Development Kit 1

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The Altera® Arria® 10 GX Transceiver Signal Integrity Development Kit is a complete design environment that includes both the hardware and software you need to develop Arria 10 GX FPGA designs. The one year license for the Quartus Prime Design Suite® software provides everything you need to begin developing custom Arria 10 GX FPGA designs.

The following list describes what you can accomplish with the kit:

- Evaluate transceiver performance from 611 Mbps up to 17.4 Gbps.
- Generate and check pseudo-random binary sequence (PRBS) patterns.
- Dynamically change differential output voltage (VOD) pre-emphasis, and equalization settings to optimize transceiver performance for your channel.
- Perform jitter analysis.
- Verify physical medium attachment (PMA) compliance to PCI Express® (PCIe®), Gbps Ethernet (GbE), XAUI, CEI-6G, Serial RapidIO® , high-definition serial digital interface (HD-SDI) and other major standards.

Development Kit Features

This section lists and describes the contents of the Arria 10 GX Transceiver Signal Integrity Development Kit.

Hardware

The Arria 10 GX Transceiver Signal Integrity Development Kit includes the following hardware:

- Arria 10 GX transceiver signal integrity development board—A development platform that allows you to develop and prototype hardware designs running on the Arria 10 GX FPGA device.
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America, Japan, Europe and the United Kingdom
  - USB type A to B cable
  - Ethernet cable

Software

The new Quartus® Prime design software includes everything needed to design for Altera FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Quartus Prime software includes an additional Spectra-Q® engine that is optimized for future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of

faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

The Quartus Prime software is available in three editions based on specific design requirements: Quartus Prime Pro Edition, Quartus Prime Standard Edition, and Quartus Prime Design Suite Lite Edition.

- Quartus Prime Pro Edition is optimized to support the advanced features in Altera's next generation FPGAs and SoCs, starting with the Arria 10 device family and requires a paid license.
- Quartus Prime Standard Edition includes the most extensive support for Altera's latest device families and requires paid license.
- Quartus Prime Lite Edition provides an ideal entry point to Altera's high-volume device families and is available as a free download with no license file required.

Included in the Quartus Prime Pro Edition are the Quartus Prime software, Nios® II EDS and the MegaCore® IP Library. To install Altera's development tools, download the Quartus Prime Pro Edition software from this web page in the **Download Center** of Altera's website.

Development Kit Package

The license-free Arria 10 GX Transceiver Signal Integrity Development Kit package contains Design Examples, Board Test System (BTS), Development Kit schematics, Development Kit Board files, User Guide, Quick Start Guide and Bill of Materials (BoM).

Getting Started 2

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The remaining chapters in this user guide lead you through the following development kit setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the Arria 10 GX transceiver signal integrity development board
- Configuring the Arria 10 GX FPGA device
- Running the Board Test System designs

Before You Begin

Before using the kit or installing the software, check the development kit contents and inspect the board to verify that you received all of the items listed in "*Development Kit Features*". If any of the items are missing, **contact Altera** before you proceed.

Related Information

Development Kit Features on page 1-1

Activating your Software License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus Prime software. After one year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus Prime software. To continue using the Quartus Prime software, you should download the free Quartus Prime Lite Edition or purchase a paid license for the Quartus Prime Pro Edition.

Before using the Quartus Prime software, you must activate your license, identify specific users and computers and obtain and install license file. If you already have a licensed version of the Standard Edition or Pro Edition, you can use that license file with this kit. If not follow these steps:

1. Log on at the **myAltera Account Sign In** web page and click **Sign In.**
2. On the myAltera Home web page, click the **Self-Service Licensing Center** link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search.**

6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products** and click Close.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the License Setup page of the **Options** dialog box in the Quartus Prime software to enable the software.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Without proper anti-static handling, you can damage the board.
2. Verify that all components are on the board and appear intact.
3. The Arria 10 GX transceiver signal integrity development kit shall have a Fan/Heatsink assembly installed on the top of the FPGA device. If this assembly needs to be installed, refer to the instructions on the documentation package and reference assembly drawing.

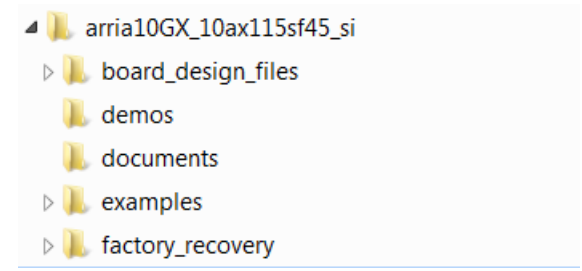
   For more information about power consumption and thermal modeling, refer to **AN 358: Thermal Management for FPGAs**.

Installing the Development Kit

To install the Arria 10 GX Transceiver Signal Integrity Development Kit, perform the following steps:

1. Download the kit installer from the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Unzip the Arria 10 GX Transceiver Signal Integrity Development Kit installer package.
3. The installer package creates the development kit directory structure shown in the figure below.

Figure 2-1: Installed Development Kit Directory Structure



Note: Early-release versions might have slightly different directory names.

The table below lists the file directory names and a description of their contents

Table 2-1: Installed Development Kit Directory Structure

File directory Name	Description of Contents
board_design_files	Contains schematics, layout, assembly, and bill of material board design files. Use these files as a starting point for a new protoytpe board design
demos	Contains demonstration applications when available
documents	Contains the development kit documentation
examples	Contains the sample design files for the development kit
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents

Installing the USB-Blaster Driver

The Arria 10 GX Transceiver Signal Integrity Development Kit includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the **Altera Cable and Adapter Drivers Information** web page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Development Board Setup 3

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The instructions in this chapter explain how to set up the Arria 10 GX Transceiver Signal Integrity Development Board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Arria 10 GX transceiver signal integrity development kit ships with its board switches pre-configured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in **Factory Default Switch Settings** on page 3-2 to return the board to its factory settings before proceeding.
2. The development kit ships with design examples stored in the flash memory device. A slide switch is provided to turn the board power **ON** or **OFF**. When the switch **SW1** is powered on, two green LEDs will illuminate to indicate that all power is applied to the board. These two LEDs are driven by the power circuitry when the power switch is turned **ON**. **RESET** button is connected to the MAX® V CPLD (**MAX_RESETn** pin) that is used for FPP configuration.

   Caution: When the power cord is plugged into connector **J1** of the Arria 10 GX Transceiver Signal Integrity Development Kit, 12V and 5V are present on the board with switch **SW1** in the '**OFF**' position. These voltages are restricted to a small area of the board. When switch **SW1** is placed to '**ON**' position, all voltage planes have power at this point.
3. When this button is pressed, the MAX V CPLD will initiate a reloading of the stored image from flash memory using FPP configuration mode. The image loaded right after power cycle or MAX V reset depends on **FACTORY_LOAD** settings: **(1)** OFF (1) - factory load **(2)** ON (0) user defined load #1. Page selection can be changed by **PGMSEL** button when the board is powered on, and **PGM_CONFIG** is used to reconfigure FPGA with corresponding page which is indicated by **PGM_LED0**, **PGM_LED1** or **PGM_LED2**

   Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.
4. Set the **POWER-ON** switch **SW1** to the on position. When power is supplied to the board, two green LEDs (**D32** and **D34**) illuminates indicating that the board has power.

The MAX V CPLD device on the board contains a parallel flash loader (PFL) megafunction. After a **POWER-ON** or **RESET** (reconfiguration) event, the MAX V CPLD will configure the Arria 10 GX FPGA in FPP mode with either the FACTORY POF or a USER defined POF depending on the setting of **FACTORY_LOAD**. The setting of the PGMSEL bit is selected by the **PGMSEL** pushbutton. Pressing this

button and observing the program LEDs dictates which program will be selected. Then the **PGM_CONFIG** pushbutton needs to be pressed to load the program.

The kit includes a MAX V CPLD design which contains the PFL megafunction. The design resides in the **<package dir>\examples\max5** directory.

1. When configuration is complete, **LED D26 (CFGDN)** illuminates signaling that the Arria 10 GX FPGA device configured successfully.
2. If the configuration fails, the **LED 24** (ERROR) illuminates.

Factory Default Switch Settings

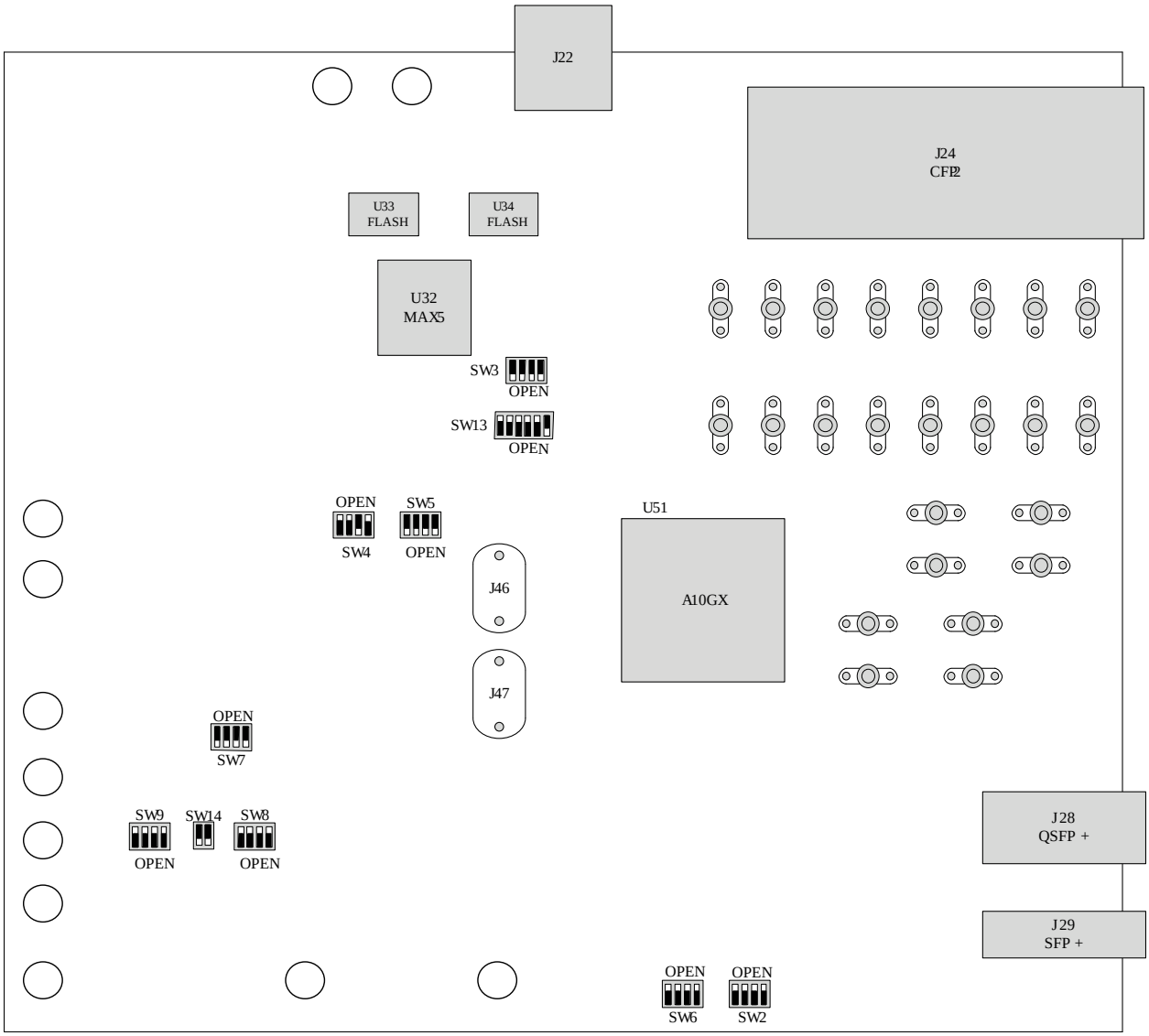
This section shows the factory switch settings for the Arria 10 GX Transceiver Signal Integrity development kit.

Table 3-1: Factory Default Switch Settings

Switch	Board Label	Function	Default Position
SW2-1	A10_Unlock	A10_Unlock	OPEN
SW2-2	USER DIP6	User DIP Switches	OPEN
SW2-3	USER DIP5	User DIP Switches	OPEN
SW2-4	USER DIP4	User DIP Switches	OPEN
SW6-1	USER DIP3	User DIP Switches	OPEN
SW6-2	USER DIP2	User DIP Switches	OPEN
SW6-3	USER DIP1	User DIP Switches	OPEN
SW6-4	USER DIP0	User DIP Switches	OPEN
SW3-1	MAX V Switch	MAX V Switch	OPEN
SW3-2	FACTORY LOAD	Factory Load Control	OPEN
SW3-3	CLK ENABLE	Clock Enable	OPEN
SW3-4	CLK SEL	Clock Selection	OPEN
SW4-1	S0	Frequency Select	OPEN
SW4-2	S1	Frequency Select	OPEN
SW4-3	SS0	Spread Spectrum Select	OPEN
SW4-4	SS1	Spread Spectrum Select	OPEN
SW5-1	CLKSEL Left Top		OPEN
SW5-2	CLKSEL Left Bottom	Open = OSC	OPEN
SW5-3	CLKSEL Right Top	Close = SMA	OPEN
SW5-4	CLKSEL Right Top		OPEN
SW7-1	ENPWR_SEQ	N/A	CLOSE
SW7-2	EN12V	N/A	CLOSE

Switch	Board Label	Function	Default Position
SW8-1	ENVCCTL_GXB	N/A	CLOSE
SW8-2	ENVCCRR_GXB	N/A	CLOSE
SW8-3	ENVCCRL_GXB	N/A	CLOSE
SW8-4	ENA10GX_VCC	N/A	CLOSE
SW9-1	ENVCCTIO	N/A	CLOSE
SW9-2	ENVCCRAM	N/A	CLOSE
SW9-3	ENVCCH_GXB	N/A	CLOSE
SW9-4	ENVCCTR_GXB	N/A	CLOSE
SW13-1	MSEL0	MSEL Setting	
SW13-2	MSEL1	MSEL Setting	
SW13-3	MSEL2	MSEL Setting	
SW13-4	VID_EN	VID Enable	
SW13-5	FAN_ON	Fan always ON	OPEN
SW13-6	MAX_BYPASS	Bypass MAX V (Active Low)	OPEN
SW14-1	I2C_33V_SCL / LT_SCL	I2C-Clock	CLOSE
SW14-2	I2C_33V_SDA / LT_SDA	I2C-Data	CLOSE

Figure 3-1: Factory Default Switch Settings



Board Update Portal 4

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The Arria 10 GX Transceiver Signal Integrity Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC and an HTML web server.

When you power up the board with the **SW3.2 FACTORY_LOAD** to **OFF(1)** position, the Arria 10 GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user portion of flash memory and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user flash memory, you can load the user design from flash memory into the FPGA. To do so, set **SW3.2** to **ON (0)** position and power cycle the board.

The source code for the Board Update Portal design resides in the **<package dir>\examples\board_update_portal** directory.

If the Board Update Portal is corrupted or deleted from the flash memory, refer to "*Restoring the Flash Device to the Factory Settings*" to restore the board with its original factory contents.

Related Information

Restoring the Flash Device to the Factory Settings on page 8-4

Connecting to the Board Update Portal Web Page

Before you begin

This section provides instructions to connect to the Board Update Portal web page. Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet, power cables and development board that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Install the latest Altera software tools, including Quartus Prime software, Nios II processor and IP functions.
2. With the board powered down, set **SW3.2** to **OFF (1)** position.
3. Attach the Ethernet cable from the board to your LAN.
4. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
5. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

You can click **Arria 10 GX Transceiver Signal Integrity Development Kit** on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the **Arria 10 GX Transceiver Signal Integrity Development Kit page** of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page include **.flash** files. You can also create .flash files from your own custom design. Refer to "**Preparing Design Files for Flash Programming** *on page 8-2*" in the Appendix of this user guide for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "**Connecting to the Board Update Portal Web Page** *on page 4-1*" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set **SW3.2** to **ON (0)** position.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "**Restoring the Flash Device to the Factory Settings** *on page 8-4*" in the Appendix of this user guide.

Board Components

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Board Overview

This section provides an overview of the Arria 10 GX transceiver signal integrity development board, including an annotated board image and component descriptions.

Figure 5-1: Overview of the Arria 10 GX Transceiver Signal Integrity Development Board Features

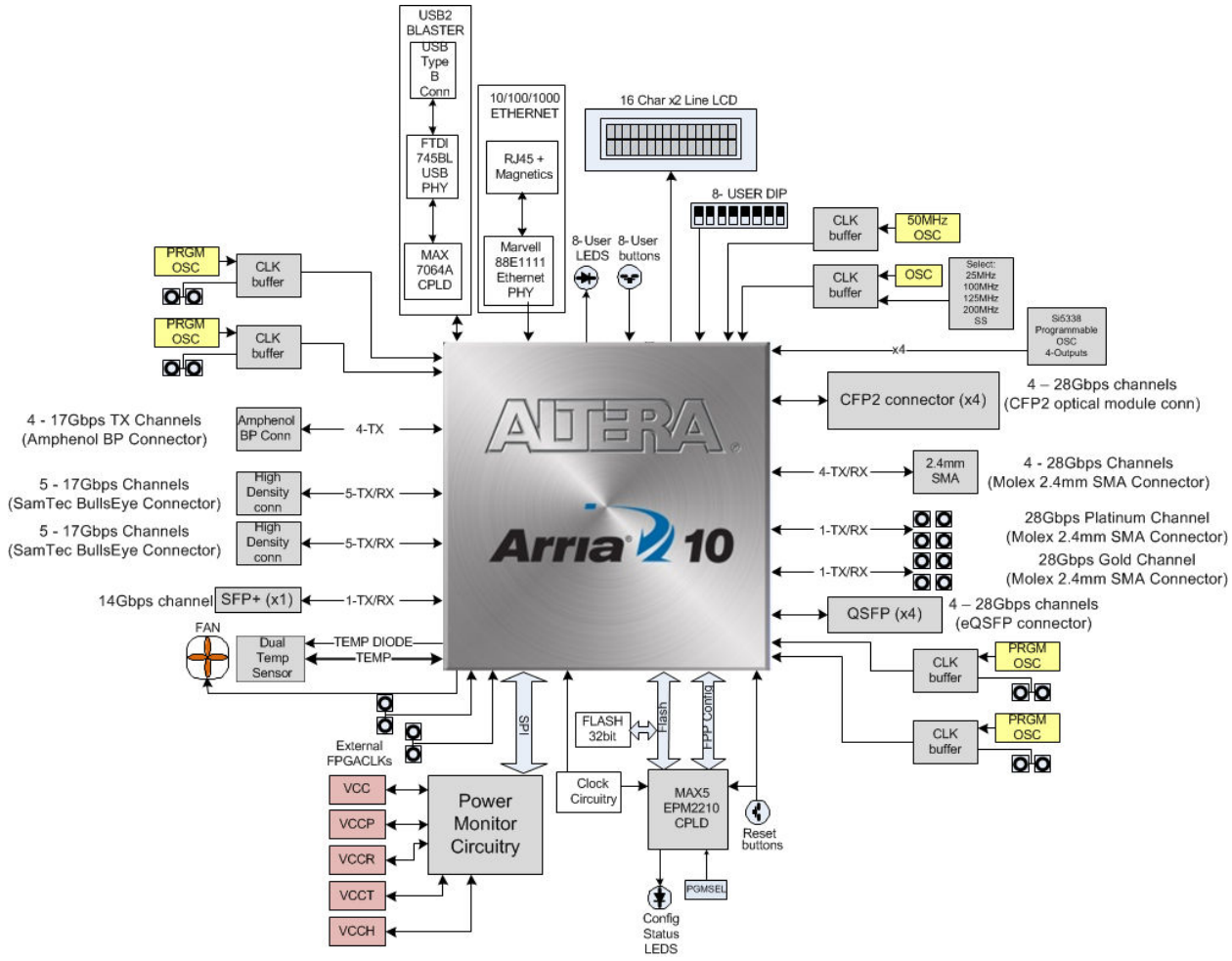


Table 5-1: Transceiver Signal Integrity Development Kit Components

Board Reference	Type	Description
Featured Devices		
U51	FPGA	Arria 10 GX1150 FPGA (10AX115F1932C)
U32	CPLD	MAX V CPLD (5M2210ZF256), 256-pin BGA
General User Input and Output		
D13 - D20	User LEDs (Green)	User LEDs (Green)
D21 - D26	MAX V LEDs (Green)	MAX V LEDs (Green)
S1 - S12	User Push Buttons	User Push Buttons
SW2, SW6	User DIP Switches	User DIP Switches
SW3	MAX V DIP Switch	MAX V DIP Switch

Board Reference	Type	Description
J20	LCD Display Header	Connector for 16 Character x 2 Line LCD I2C
Configuration, Status and Setup Elements		
J66	USB Blaster Programming Header (uses JTAG mode only)	Header to interface external USB Blaster direct to FPGA (through USB2 MAX2)
D4	Green LED	USB2 Transmit-Receive Activity
D8-D12	Ethernet LEDs	Ethernet LEDs (TX / RX / LINK)
Clock Circuitry		
X3	25-MHz Oscillator	This 25-MHz oscillator is the clock source to clock buffer ICS557-03 that provides selectable frequencies and spread percentages of its differential outputs.
X4	50-MHz oscillator	This 50-MHz oscillator is the clock source to clock buffer SL18860DC that provides three 50 MHz outputs to the FPGA (x2) and the MAX V (x1)
SW4	Spread spectrum / Frequency selection switch	SW4 selects frequency and spread spectrum percentages of clock buffer outputs ICS557-03. Refer to **Table 5-2** for additional details.
J49 - J50	External core clock input	SMA External input at CLKIN_3B0 p/n
J51 - J52	External core clock output	SMA external output at PLL_3B_CLKOUT0 p/n
Y3	Transceiver Dedicated Reference Clock / Programmable Oscillator	Feeds REFCLKs on left side of the Arria 10 GX device and an LVDS trigger output at board reference J100/J101. The external input is available at board reference J53 and J54. The default frequency is 644.53125 MHz.
Y4	Transceiver Dedicated Reference Clock / Programmable Oscillator	Feeds REFCLKs on left side of the Arria 10 GX device and an LVDS trigger output at board reference J102/J103. The external input is available at board reference J56 and J57. The default frequency is 706.25 MHz.
Y5	Transceiver Dedicated Reference Clock / Programmable Oscillator	Feeds REFCLKs on right side of the Arria 10 GX device and an LVDS trigger output at board reference J104/J105. The external input is available at board reference J59 and J60. The default frequency is 625 MHz.

Board Reference	Type	Description
Y6	Transceiver Dedicated Reference Clock / Programmable Oscillator	Feeds REFCLKs on right side of the Arria 10 GX device and an LVDS trigger an output at board reference J106 / J107. The external input is available at board reference J62 and J63. The default frequency is 875 MHz.
Y2	Global Clock / 25 MHz Oscillator	25-MHz crystal oscillator input to Si5338A clock buffer that feeds core fabric
X5	Global Clock / 125 MHz Oscillator	Feeds core fabric at CLKIN_2L0 p/n
Transceiver Interfaces		
J46	High Density Connector	15Gbps, 5 channels High Density Connector
J47	High Density Connector	15Gbps, 5 channels High Density Connector
J30 - J45 J67- J74	2.4 mm SMA Connector	25.78 Gbps, 4 channels 2.4 mm SMA Connector
J24	CFP2 Optical Transceiver Interface	25.78 Gbps, 4 Transceiver channels connected to the CFP2 module
J23, J25, J26, J27	CFP2 optional MCLK input / output	CFP2 TX MCLK SMA Connectors CFP2 RX MCLK SMA Connectors
J28	QSFP+ optical transceiver interface	25.78 Gbps, 4 Transceiver channels connected to the QSFP+ module.
J29	SFP+ optical transceiver interface	14 Gbps, single Transceiver channel connected to the SFP+ module.
J22	Backplane Connector	17 Gbps, 4 transceiver channels connected to the Amphenol backplane connector.
Memory Devices		
U33, U34	Flash Memory	Two 1-Gbit Micron PC28F00AP30BF CFI Flash device
Communication Ports		
J19	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection through a Marvell 88E1111 PHY
CN1	USB Type-B connector	Connects a type-B USB cable
Power Supply		
U209	LTM 2987	Linear Technology Power monitor device
U225	LTC2974	Linear Technology Power monitor device

Table 5-2: SW-4 Board Reference

<table>
<tr><th>Board Reference Spread Spectrum/ Frequency Selection Switch</th><th>Spread Spectrum Buffer Inputs</th><th></th></tr>
<tr><td>SW4-1</td><td>S0</td><td rowspan="2"><table><tr><th>S1</th><th>S0</th><th>CLK Freq</th></tr><tr><td>0</td><td>0</td><td>25 MHz</td></tr><tr><td>0</td><td>1</td><td>100 MHz</td></tr><tr><td>1</td><td>0</td><td>125 MHz</td></tr><tr><td>1</td><td>1</td><td>200 MHz</td></tr></table></td></tr>
<tr><td>SW4-2</td><td>S1</td></tr>
<tr><td>SW4-3</td><td>SS0</td><td rowspan="2"><table><tr><th>SS1</th><th>SS0</th><th>Spread %</th></tr><tr><td>0</td><td>0</td><td>+/-25</td></tr><tr><td>0</td><td>1</td><td>-0.5</td></tr><tr><td>1</td><td>0</td><td>-0.75</td></tr><tr><td>1</td><td>1</td><td>no spread</td></tr></table></td></tr>
<tr><td>SW4-4</td><td>SS1</td></tr>
</table>

Arria 10 FPGA

The development board features the Arria 10 GX115 FPGA (10AX115F1932C).

Arria 10 GX FPGA Device Features :

- 1.15M Logic Elements (LEs)
- 427,200 Adaptive Logic Modules (ALMs)
- 1,708,800 Registers
- 54,260 Kb of M20K Memory
- 12,984 Kb of MLAB Memory
- 1518 Variable Precision Digital Signal Processing (DSP) Blocks
- 3036 18-bit x 19-bit Multipliers
- 32 Fractional Synthesis Phase-Locked Loops (PLLs)
- 72 15Gbps Transceivers

I/O Resources

The table below summarizes the FPGA I/O usage by function on the Arria 10 GX transceiver signal integrity development board.

Table 5-3: Arria 10 GX I/O Usage Summary

Function	I/O Count	Description
Configuration		

Function	I/O Count	Description
JTAG USB Blaster or JTAG Header	4	Built-in USB-Blaster or JTAG 0.1-mm header for debugging
MSEL [2:0]	3	Configuration input pins to set configuration scheme
FPGA_CONF_DONE	1	Configuration done pin
FPGA_nSTATUS	1	Configuration status pin
FPGA_INIT_DONE	1	Configuration pin to signify user mode
FPGA_nCSO	1	Chip select pin to EPCQ device
FPGA_nCONFIG	1	Configuration input pin to reset FPGA
CLKUSR-100MHz	1	100 MHz Clock
FPGA_DCLK	1	Configuration Clock for PS and FPP configuration schemes
CPU_RESETn	1	Configuration input pin that clears all device registers
DEV_OE	1	Configuration input pin that enables all IOs
FPGA_CONFIG_D[31:0]	32	Configuration data input pins
FPGA_AS_DATA[3:0]	4	EPCQ data bus
PCIE_RESET	1	Reset pin for PCIe HIP
FPGA_PR_DONE	1	Partial reconfiguration done pin
FPGA_PR_REQUEST	1	Partial reconfiguration request pin
FPGA_PR_READY	1	Partial reconfiguration ready pin
FPGA_PR_ERROR	1	Partial reconfiguration error pin
USB		
USB_FULL	1	USB FIFO is full
USB_EMPTY	1	USB FIFO is empty
USB_RESETn	1	USB Reset
USB_OEn	1	USB Output Enable
USB_RDn	1	USB Read
USB_WRn	1	USB Write
USB_DATA[7:0]	8	USB Data Bus
USB_ADDR[1:0]	2	USB Address Bus
USB_SCL	1	USB Serial Clock
USB_SDA	1	USB Serial Data

Flash Memory

Function	I/O Count	Description
F M_D[31:0]	32	Flash data bus
FM_A[26:1]	26	Flash address bus
FLASH_WEn	1	Flash write enable strobe
FLASH_CEn0	1	Flash chip enable
FLASH_CEn1	1	Flash chip enable
FLASH_OEn	1	Flash output enable
FLASH_RDYBSYn0	1	Flash ready or busy
FLASH_RDYBSYn1	1	Flash ready or busy
FLASH_RESETn	1	Flash reset
FLASH_CLK	1	Flash clock
FLASH_ADVn	1	Flash address valid
MAX V CPLD		
MAX5_OEn	1	Output Enable
MAX5_CSn	1	Chip Select
MAX5_WEn	1	Write Enable
MAX5_CLK	1	Clock
MAX5_BEn[3:0]	4	Byte Enable
Switches, Buttons, LED		
USER_LED [7:0]	8	Light Emitting Diode
USER_PB [7:0]	8	Push Buttons
USER_DIP [6:0]	7	DIP Switches
USER_IO [9:0]	10	Input/Output
A10_UNLOCK	1	FPGA Unlock Switch
Ethernet		
ENET_SGMII_TX_P/N	2	Ethernet SGMII transmit data
ENET_SGMII_RX_P/N	2	Ethernet SGMII receive data
ENET_RSTn	1	Reset
ENET_INTn	1	Interrupt
MDIO	1	Ethernet Management Data IO
MDC	1	Ethernet Management Data Clock
Temperature Sense		
Temperature Sense Diodes	2	Arria 10 internal sense diode
Transceivers		
SFP_TX_DIS	1	SFP + TX disable control pin

Function	I/O Count	Description
SFP_RS0	1	SFP + Rate Select - Receiver Control Pin
SFP_RS1	1	SFP + Rate Select - Transmit Control Pin
SFP_MOD_ABS	1	SFP + Module Absent Status Pin
SFP_RX_LOS	1	SFP + Loss of Signal Status Pin
SFP_TX_FLT	1	SFP + Transmitter Fault Status Pin
CFP2_MOD_LOPWR	1	CFP2 Module Low Power Mode
CFP2_MOD_RSTn	1	CFP2 Module Reset
CFP2_PRG_CNTL[3:1]	3	CFP2 Program Control bits
CFP2_PRG_ALRM[3:1]	3	CFP2 Program Alarm bits
CFP2_PRG_PRTADR[2:0]	3	CFP2 MDIO Physical Port Address
CFP2_TX_DIS	1	CFP2 Transmitter Disable
CFP2_RX_LOS	1	CFP2 Receiver loss of signal
CFP2_MOD_ABS	1	CFP2 Module Absent
CFP2_MDC	1	CFP2 Management Data Clock
CFP2_MDIO	1	CFP2 Management Data I/O Bi-Directional Data
CFP2_GLB_ALRMn	1	CFP2 Global Alarm
Global Clocks		
USB_FPGA_CLK	1	USB FPGA Clock
50MHz_A10GX_CLK	1	50 MHz Global clock input
50MHz_CLK3D	1	50 MHz Global clock input
A10GX_CLK2Jp	1	Global Clock input (selectable freq/ spread %)
A10GX_CLK2Jn	1	Global Clock input (selectable freq/ spread %)
A10GX_CLK3Bp	1	Global Clock input from SMA
A10GX_CLK3Bn	1	Global Clock input from SMA
100MHZ_LVDS_CLK3p	1	Differential global clock
100MHZ_LVDS_CLK3n	1	Differential global clock
100MHZ_LVDS_CLK2p	1	Differential global clock
100MHZ_LVDS_CLK2n	1	Differential global clock
100MHZ_LVDS_CLK1p	1	Differential global clock
100MHZ_LVDS_CLK1n	1	Differential global clock
CLK_125MHz_P/N	2	125 MHz differential core clock

Function	I/O Count	Description
Transceiver Clocks		
REFCLK_GXBL_1E_T	2	Differential REFCLK input to the left side of xcvr block 1E
REFCLK_GXBL_1F_T	2	Differential REFCLK input to the left side of xcvr block 1F
REFCLK_GXBL_1G_T	2	Differential REFCLK input on the left side of xcvr block 1G
REFCLK_GXBL_1H_T	2	Differential REFCLK input to the left side of xcvr block 1H
REFCLK_GXBL_1D_T	2	Differential REFCLK input to the left side of xcvr block 1D
REFCLK_GXBL_1C_T	2	Differential REFCLK input to the left side of xcvr block 1C
REFCLK_GXBL_1E_T	2	Differential REFCLK input to the left side of xcvr block 1E
REFCLK_GXBL_1G_T	2	Differential REFCLK input to the left side of xcvr block 1G
REFCLK_GXBR_4E_T	2	Differential REFCLK input to the left side of xcvr block 4E
REFCLK_GXBR_4F_T	2	Differential REFCLK input to the left side of xcvr block 4F
REFCLK_GXBR_4G_T	2	Differential REFCLK input to the left side of xcvr block 4G
REFCLK_GXBR_4H_T	2	Differential REFCLK input to the left side of xcvr block 4H
REFCLK_GXBR_4C_T	2	Differential REFCLK input to the left side of xcvr block 4C
REFCLK_GXBR_4C_B	2	Differential REFCLK input to feed the channels on the right side of the Arria 10 GX device 4C
REFCLK_GXBR_4D_B	2	Differential REFCLK input to the left side of xcvr block 4D
REFCLK_GXBR_4E_B	2	Differential REFCLK input to the left side of xcvr block 4E
REFCLK_GXBR_4H_B	2	Differential REFCLK input to the left side of xcvr block 4H

MAX V CPLD

The Arria 10 transceiver development kit consists of a MAX V CPLD (5M2210Z-F256), 256-pin FineLine BGA package. MAX V CPLD devices provide programmable solutions for applications such as I/O

expansion, bus and protocol bridging, power monitoring, FPGA configuration, and analog IC interface. MAX V devices feature on-chip flash storage, internal oscillator, and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirement.

The following list summarizes the MAX V device features:

- 2210 Logic Elements (LEs)
- 8192 bits of User Flash Memory
- 4 global clocks
- 1 internal oscillator
- 271 maximum user I/O pins
- Low-cost, low power and non-volatile CPLD architecture
- Fast propagation delays and clock-to-output times
- Single 1.8V external supply for device core
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors

The table below lists the MAX V CPLD Pin-out, the I/O signals present on the MAX V CPLD.

Table 5-4: MAX V CPLD Device Pin-Out

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
FPGA_CONFIG_D0	D3	AU27	FPP Configuration Data Bus
FPGA_CONFIG_D1	C2	AU28	FPP Configuration Data Bus
FPGA_CONFIG_D2	C3	AP28	FPP Configuration Data Bus
FPGA_CONFIG_D3	E3	AR29	FPP Configuration Data Bus
FPGA_CONFIG_D4	D2	AT28	FPP Configuration Data Bus
FPGA_CONFIG_D5	E4	AT29	FPP Configuration Data Bus
FPGA_CONFIG_D6	D1	AW27	FPP Configuration Data Bus
FPGA_CONFIG_D7	E5	AY27	FPP Configuration Data Bus
FPGA_CONFIG_D8	F3	AY26	FPP Configuration Data Bus
FPGA_CONFIG_D9	E1	AW26	FPP Configuration Data Bus
FPGA_CONFIG_D10	F4	AV26	FPP Configuration Data Bus
FPGA_CONFIG_D11	F2	AU26	FPP Configuration Data Bus
FPGA_CONFIG_D12	F1	AV29	FPP Configuration Data Bus
FPGA_CONFIG_D13	F6	AV30	FPP Configuration Data Bus
FPGA_CONFIG_D14	G2	AV31	FPP Configuration Data Bus
FPGA_CONFIG_D15	G3	AW31	FPP Configuration Data Bus
FPGA_CONFIG_D16	G1	AW28	FPP Configuration Data Bus
FPGA_CONFIG_D17	G4	AV28	FPP Configuration Data Bus
FPGA_CONFIG_D18	H2	AY31	FPP Configuration Data Bus

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
FPGA_CONFIG_D19	G5	AY30	FPP Configuration Data Bus
FPGA_CONFIG_D20	H3	BA29	FPP Configuration Data Bus
FPGA_CONFIG_D21	J1	BA30	FPP Configuration Data Bus
FPGA_CONFIG_D22	J2	BA32	FPP Configuration Data Bus
FPGA_CONFIG_D23	H4	BB32	FPP Configuration Data Bus
FPGA_CONFIG_D24	K2	BA33	FPP Configuration Data Bus
FPGA_CONFIG_D25	K5	BB33	FPP Configuration Data Bus
FPGA_CONFIG_D26	L1	BB31	FPP Configuration Data Bus
FPGA_CONFIG_D27	L2	BC31	FPP Configuration Data Bus
FPGA_CONFIG_D28	K3	BC33	FPP Configuration Data Bus
FPGA_CONFIG_D29	M2	BD33	FPP Configuration Data Bus
FPGA_CONFIG_D30	L4	BA34	FPP Configuration Data Bus
FPGA_CONFIG_D31	L3	BB35	FPP Configuration Data Bus
FM_A1	C14	F28	Flash address bus
FM_A2	C15	F27	Flash address bus
FM_A3	E13	G28	Flash address bus
FM_A4	E12	G27	Flash address bus
FM_A5	D15	H25	Flash address bus
FM_A6	F14	G25	Flash address bus
FM_A7	D16	K27	Flash address bus
FM_A8	F13	D31	Flash address bus
FM_A9	E15	C31	Flash address bus
FM_A10	E16	C30	Flash address bus
FM_A11	F15	C29	Flash address bus
FM_A12	G14	E30	Flash address bus
FM_A13	F16	E31	Flash address bus
FM_A14	G13	E29	Flash address bus
FM_A15	G15	D29	Flash address bus
FM_A16	G12	F30	Flash address bus
FM_A17	G16	F29	Flash address bus
FM_A18	H14	J29	Flash address bus
FM_A19	H15	K31	Flash address bus
FM_A20	H13	K30	Flash address bus

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
FM_A21	H16	L30	Flash address bus
FM_A22	J13	L29	Flash address bus
FM_A23	R3	G30	Flash address bus
FM_A24	P5	G31	Flash address bus
FM_A25	T2	H29	Flash address bus
FM_A26	P9	H30	Flash address bus
FM_D0	J14	H34	Flash data bus
FM_D1	J15	J33	Flash data bus
FM_D2	K16	J32	Flash data bus
FM_D3	K13	L34	Flash data bus
FM_D4	K15	K34	Flash data bus
FM_D5	K14	N34	Flash data bus
FM_D6	L16	M35	Flash data bus
FM_D7	L11	M32	Flash data bus
FM_D8	L15	L32	Flash data bus
FM_D9	L12	U32	Flash data bus
FM_D10	M16	T32	Flash data bus
FM_D11	L13	R30	Flash data bus
FM_D12	M15	R31	Flash data bus
FM_D13	L14	U33	Flash data bus
FM_D14	N16	T33	Flash data bus
FM_D15	M13	N33	Flash data bus
FM_D16	N15	P33	Flash data bus
FM_D17	N14	R34	Flash data bus
FM_D18	P15	P34	Flash data bus
FM_D19	P14	T34	Flash data bus
FM_D20	D13	T35	Flash data bus
FM_D21	D14	D26	Flash data bus
FM_D22	F11	E26	Flash data bus
FM_D23	J16	A28	Flash data bus
FM_D24	F12	A27	Flash data bus
FM_D25	K12	B28	Flash data bus
FM_D26	M14	B27	Flash data bus

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
FM_D27	N13	B26	Flash data bus
FM_D28	R1	C26	Flash data bus
FM_D29	P4	D27	Flash data bus
FM_D30	N5	E27	Flash data bus
FM_D31	P6	C28	Flash data bus
USB_MAX5_CLK	H5	----	USB Clock
CLK_CONFIG	J5	----	100 MHz Clock
50MHz_MAX5_CLK	J12	----	Dedicated 50 MHz MAX V clock input
FPGA_nSTATUS	J4	AN29	FPGA status
FPGA_CONF_DONE	K1	AP27	FPGA Configuration complete
FPGA_DCLK	J3	AM26	FPGA configuration clock
FPGA_PR_ERROR	P2	BA28	FPGA configuration error
FPGA_PR_READY	E2	BB30	FPGA configuration ready
FPGA_PR_REQUEST	F5	BD31	FPGA configuration request
FPGA_PR_DONE	H1	BB28	FPGA configuration complete
FPGA_INIT_DONE	K4	BC29	FPGA initialization complete
M5_JTAG_TCK	P3	----	JTAG chain Test clock input
M5_JTAG_TDI	L6	----	JTAG chain test data input
M5_JTAG_TDO	M5	----	JTAG chain test data output
M5_JTAG_TMS	N4	----	JTAG chain test mode select
TEMP_ALERTn	D4	----	Temperature Alert
OVERTEMPn	B1	----	Over-temperature indicator LED
OVERTEMP	C5	----	Over-temperature status bit
MAX_CONF_DONE	E11	----	MAX V Configuration Done
PGM_SEL	B13	----	Flash memory PGM select
PGM_CONFIG	D12	----	Flash memory PGM Configuration
PGM_LED0	B14	----	Flash memory PGM select indicator 0
PGM_LED1	C13	----	Flash memory PGM select indicator 1
PGM_LED2	B16	----	Flash memory PGM select indicator 2

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
CLK_SEL	A13	----	Clock Select (dipswitch set)
CLK_ENABLE	A15	----	Clock Enable (dipswitch set)
FACTORY_LOAD	A2	----	Factory Image for Configuration
MAX_ERROR	A4	----	MAX V Error Indicator LED
MAX_LOAD	A6	----	MAX V Load Indicator LED
MSEL0	B10	AN26	DIP - FPGA mode select 0
MSEL1	B3	AL28	DIP - FPGA mode select 1
MSEL2	C10	AK25	DIP - FPGA mode select 2
CPU_RESETn	C12		CPU Reset (via pushbutton)
I2C_18V_SCL	C7	AM35	I2C Clock, 1.8V leg of I2C Chain
I2C_18V_SDA	D10	AK32	I2C Data, 1.8V leg of I2C Chain
CLK_125MHz_EN	D5	----	125 MHz Clock enable
CLK_50MHz_EN	E8	----	50 MHz Clock Enable
FLASH_WEn	N6	AR35	Flash write enable
FLASH_CEn0	R5	AT30	Flash chip enable
FLASH_CEn1	M7	AR31	Flash chip enable
FLASH_OEn	M6	AT34	Flash output enable
FLASH_RDYBSYn0	T5	AT35	Flash chip ready/busy
FLASH_RDYBSYn1	R7	AN31	Flash chip ready/busy
FLASH_RESETn	P7	AP31	Flash Reset
FLASH_CLK	R6	AU31	Flash clock
FLASH_ADVn	N7	AU30	Flash address valid
MAX_RESETn	M9	----	MAX V Reset
MAX5_SWITCH	R12	----	MAX V switch (via dipswitch)
MAX5_OEn	M10	AG32	MAX V output enable
MAX5_CSn	R10	W32	MAX V chip select
MAX5_WEn	N10	W33	MAX V write enable
MAX5_CLK	T11	AA34	MAX V clock
MAX5_BEn0	P10	W35	MAX V byte enable 0
MAX5_BEn1	R11	Y35	MAX V byte enable 1
MAX5_BEn2	T12	V33	MAX V byte enable 2
MAX5_BEn3	N11	V34	MAX V byte enable 3

Schematic Signal Name	MAX V CPLD Pin Number	Arria 10 GX Pin Number	Description
ENET_INTn	R16	AW12	Ethernet Interrupt
ENET_RSTn	P13	AV13	Ethernet Reset
FAN_RPM	N9	----	Fan RPM Control
USB_CFG0	R4	----	USB configuration bits
USB_CFG1	T4	----	USB configuration bits
USB_CFG2	P8	----	USB configuration bits
USB_CFG3	T7	----	USB configuration bits
USB_CFG4	N8	----	USB configuration bits
USB_CFG5	R8	----	USB configuration bits
USB_CFG6	T8	----	USB configuration bits
USB_CFG7	T9	----	USB configuration bits
USB_CFG8	R9	----	USB configuration bits

Configuration Elements

This section describes the FPGA, flash memory, and MAX V CPLD System Controller device programming methods supported by the Arria 10 GX transceiver signal integrity development board.

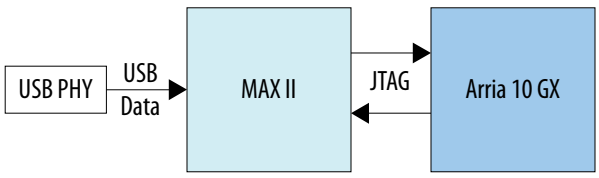
The Arria 10 GX transceiver signal integrity development board supports three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus Prime Programmer in JTAG mode with the supplied USB cable.
- MAX V configures the FPGA device via FPP mode using stored images from CFI flash devices either at power-up or pressing the MAX_RESETn/PGM_CONFIG push button.
- JTAG external header for initial debugging.

FPGA Programming over Embedded USB-Blaster

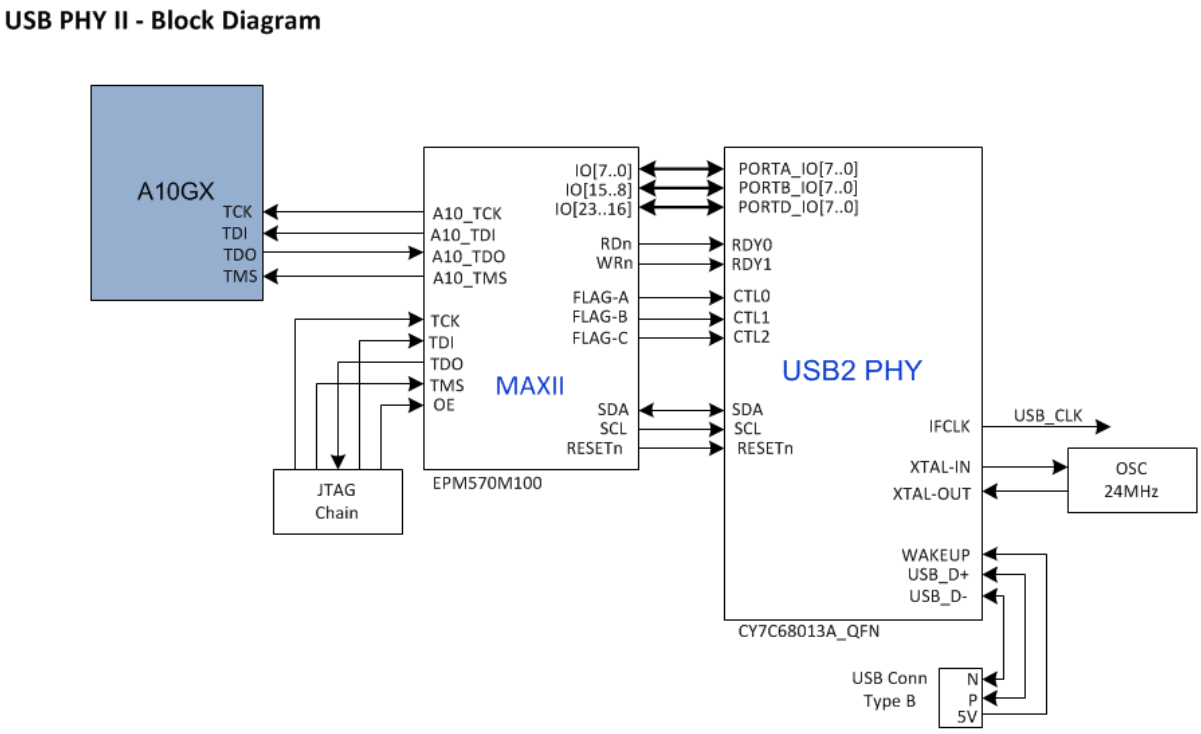
The figure below shows the high-level conceptual block diagram for the embedded USB-Blaster.

Figure 5-2: USB-Blaster Conceptual Block Diagram



The figure below shows a more detailed schematic block diagram for the embedded USB-Blaster interfacing to the Arria 10 GX FPGA device.

Figure 5-3: Detailed USB-Blaster to FPGA Schematic

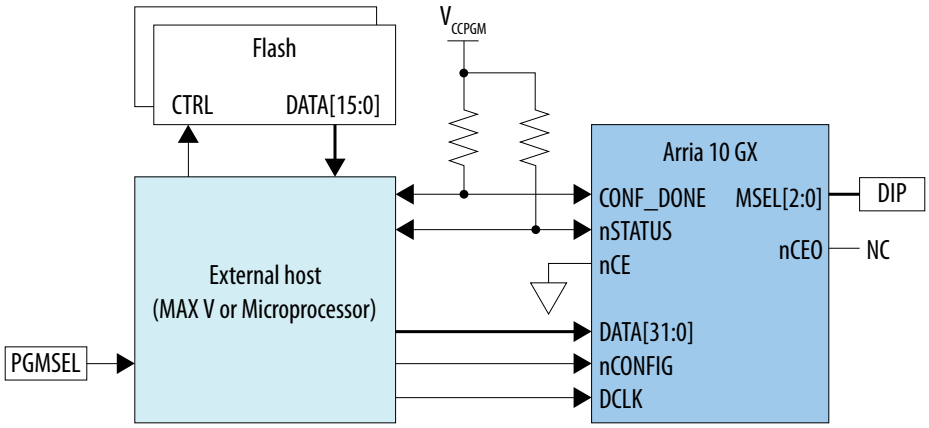


The embedded USB Blaster core for USB-based configuration of the Arria 10 GX FPGA device is implemented using a TYPE B USB connector, a CY7C68013A USB2 PHY device, and an Altera MAX II EPM570M100 CPLD. This will allow configuration of the Arria 10 GX FPGA device using a USB cable directly connected to a PC running Quartus Prime software without requiring the external USB Blaster dongle. This design will convert USB data to interface with the Arria 10 GX FPGA's dedicated JTAG port. An LED **(D4)** is provided to indicate USB Blaster activity. The embedded USB blaster is automatically disabled when an external USB Blaster dongle is connected to the JTAG chain.

FPGA Programming from Flash Memory

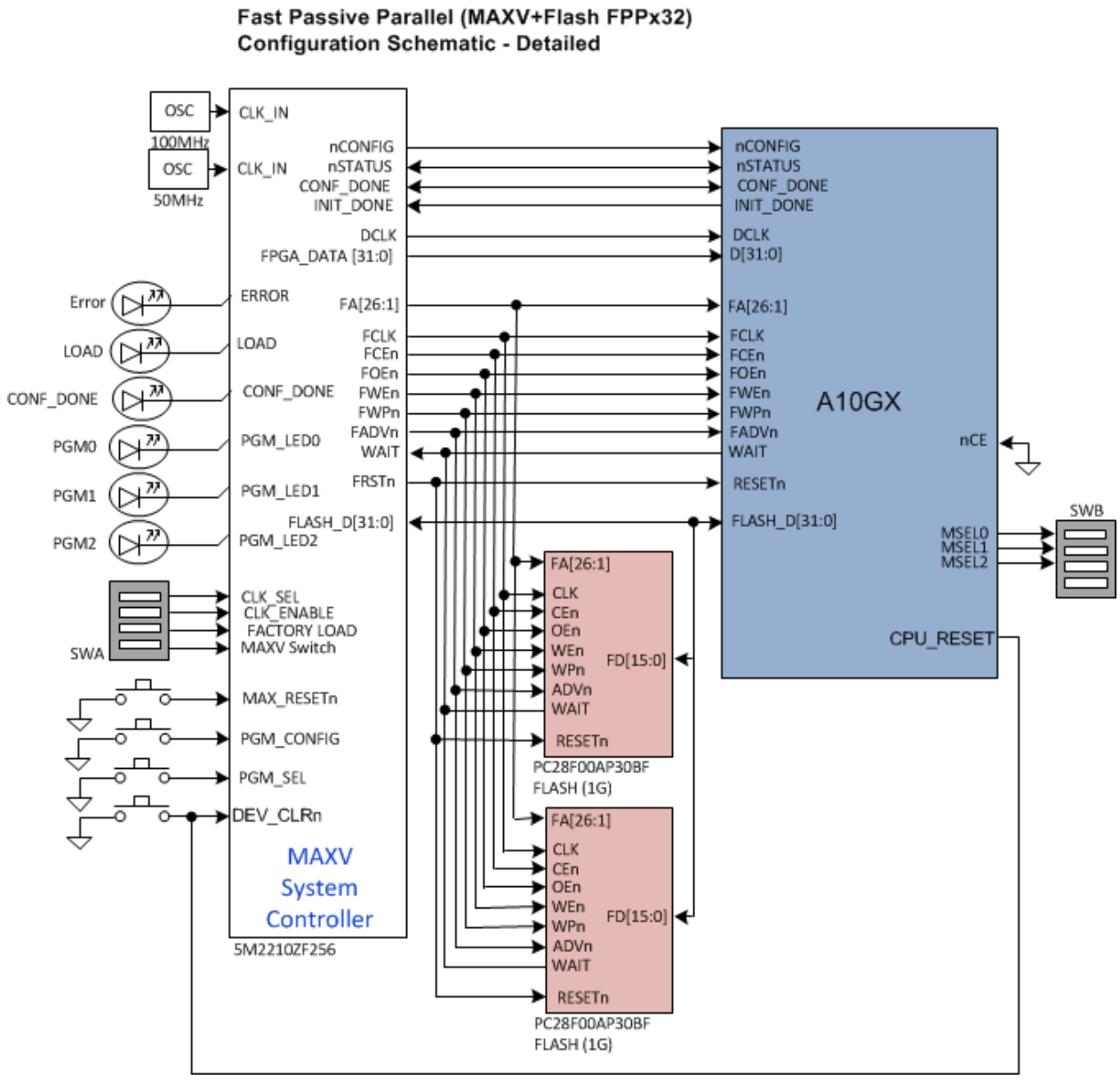
The figure below shows the high-level conceptual block diagram for the MAX V + Flash Fast Passive Parallel (FPP) configuration.

Figure 5-4: MAX V + Flash FPP x32 Configuration Conceptual Diagram



The figure below shows a more detailed schematic block diagram for the MAX V + Flash FPP mode implementation.

Figure 5-5: Detailed MAX V + Flash FPP x32 Configuration Schematic



Once the FPGA is successfully initialized and in user mode, the CPLD will tri-state its Flash interface signals to avoid contention with the FPGA. A **PGMSEL** dipswitch (SW3) is provided to select between two **POF** files (**FACTORY** or **USER**) stored on the Flash. The Parallel Flash Loader (PFL) Megafunction will be used to implement FPP x32 configuration in the MAX V CPLD. The PFL Megafunction reads data from the flash and converts it to Fast Passive Parallel format. This data is written to the Arria 10 FPGA device dedicated DCLK and D[31:0] configuration pins at 50 MHz. The actual configuration data rate is limited by the flash read speed.

Implementation will be done using an Altera MAX V 5M2210ZF256FBGA CPLD acting as the FPP download controller and two 1G Flash devices. The flash will be a Numonyx 1.8V core, 1.8V I/O 1Gigabit CFI NOR-type device (P/N: PC28F00AP30BF). The MAX V CPLD will share the CFI Flash interface with

the Arria 10 GX FPGA. No arbitration is needed between the MAX V CPLD and Arria 10 GX FPGA to access the Flash as the CPLD only has access prior to FPGA initialization.

After a **POWER-ON** or **RESET** (re-configuration) event, the MAX V device will configure the Arria 10 GX FPGA in FPP x32 mode with either the FACTORY POF or a USER defined POF depending on the FACTORY_LOAD setting. The **PGMSEL** bit is set via a pushbutton and observing the appropriate LED indicating a Factory or User file to be loaded. After selection of the program file; another pushbutton is press to load the program; that button is the **PGM_CONFIG** button.

The **MSEL [2:0]** pins indicate which passive mode is being used and whether the Fast or Slow POR delay is chosen. The data bus width information is contained in the Mode Select Decode Frame that is part of the configuration data. PORSEL is an internal signal decoded from **MSEL[2:0]** pins. PORSEL = 1 selects a Fast POR delay between 4-12ms. PORSEL = 0 selects a Slow POR delay between 100-300ms.The manufacturing default condition should be [000] for a Fast POR Delay mode without decompression or security enabled.

The 4 modes of Passive Programming are passive serial, passive parallel x8, passive parallel x16, and passive parallel x32.

For FPPx32 modes, **MSEL [2:0]** signals need to be set according to the table below

Table 5-5: Supported FPPx32 Modes

MSEL[2:0]	Mode of Operation	Voltages Supported (v)	POR Delay (ms)
000	Passive Fast	1.8	4-12
001	Passive Slow	1.8	100-300
010	Active Fast	1.8	4-12
011	Active Slow	1.8	100-300
100	ATPG	1.8	4-12
101	Test	1.8	4-12
110	Test Verify	1.8	4-12
111	Regscan	1.8	4-12

The LEDs associated with program load of FPPx32 mode configuration status as follows:

- PGM_LED0 : ON when FACTORY image is selected
- PGM_LED1 : ON when USER #1 image is selected
- PGM_LED2 : ON when USER #2 image is selected
- MAX_ERROR : ON when a Configuration Error has occurred
- MAX_LOAD : ON when image is being loaded
- MAX_CONF_DONE : ON when FPGA is successfully configured

Note: All the LEDs listed above are green.

FPGA Programming over External USB-Blaster

The JTAG chain allows programming of both the Arria 10 GX FPGA and MAX V CPLD devices using an external Altera USB blaster dongle or the on-board USB2 blaster via the USB interface connector.

During board bring-up and as a back-up in case the on-board USB2 blaster has a problem, the external Altera USB Blaster dongle can be used to program both Arria 10 GX FPGA and MAX V CPLD via the external blaster 2 x 5 pin 0.1” programming header (J66).

Another 2 x 5 pin 0.1" vertical non-shrouded header (J18) is provided on the board for programming the MAXII_Blaster CPLD for configuring the on-board USB Blaster circuitry. Once the on-board blaster is configured and operational, the on-board blaster can be used for subsequent programming of the Arria 10 GX FPGA and MAX V CPLD.

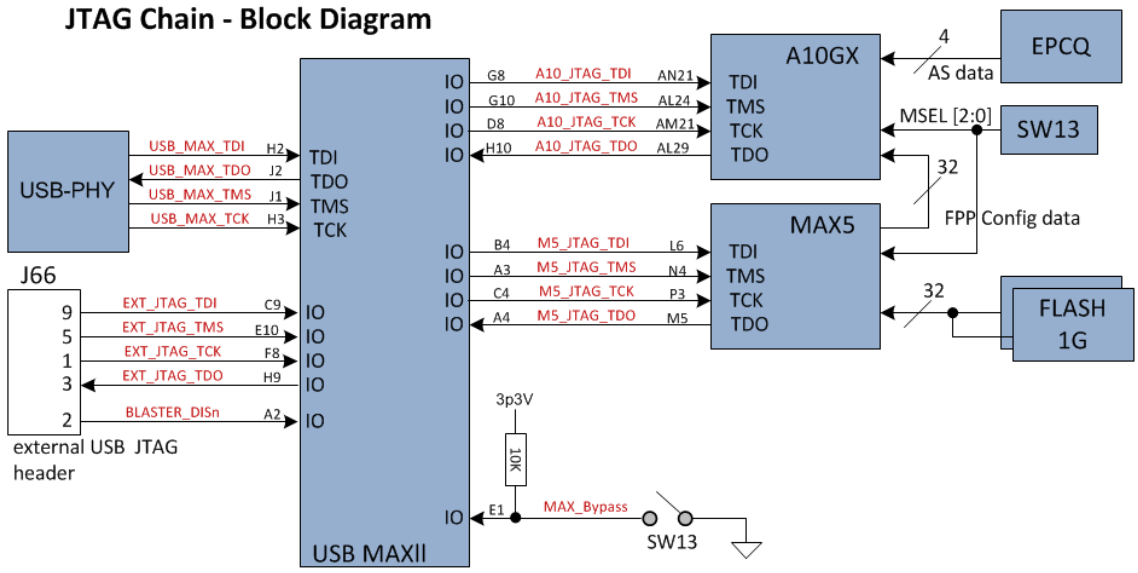
The on-board blaster JTAG chain will connect the Arria 10 GX FPGA and the MAX V CPLD devices in the following order, with the option to bypass the MAX V CPLD by a dip switch setting as follows:

- Switch closed : MAX V is bypassed, only Arria 10 GX FPGA is in the JTAG chain
- Switch open (Default) : Both MAX V and Arria 10 GX FPGA are in the JTAG chain

Note: The Arria 10 GX FPGA device is always available in the JTAG chain and cannot be bypassed.

Pin 2 of the Arria 10 GX FPGA and MAX V JTAG Header will be used to disable the embedded USB Blaster by connecting it to the embedded Blaster's DEVOEn pin with a pull-up resistor. Since Pin 2 from the mating Blaster dongle is GND, when the dongle is connected into the JTAG header, the embedded Blaster is disabled to avoid contention with the external USB blaster dongle.

Figure 5-6: JTAG Chain



Status Elements

The development board includes board-specific status LEDs and switches for enabling and configuring various features on the board, as well as a 16 character x 2 line LCD for displaying board power and temperature measurements. This section describes these status elements.

Table 5-6: Board-Specific LEDs

Board Reference	Schematic Signal Name	Description
D32	------	Green LED. Power LED-5V present.

Board Reference	Schematic Signal Name	Description
D34	------	Green LED. Power LED-12V present.
D3	T_OVERTEMPn	Amber LED. Over Temperature LED.
D4	RX-TX_ACTIVITY	Green LED. On-Board USB Blaster LED.
D8	ENET_LED_TX	Green LED. Blinks to indicate Ethernet PHY transmit activity.
D9	ENET_LED_RX	Green LED. Blinks to indicate Ethernet PHY receive activity.
D10	ENET_LED_LINK1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed.
D11	ENET_LED_LINK100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed.
D12	ENET_LED_LINK10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- JTAG Chain Device Removal Switch
- Program Select Push Button
- MAX V Reset Push Button
- CPU Reset Push Button

JTAG Chain Device Removal Switch: The JTAG chain will connect the Arria 10 GX FPGA and the MAX V CPLD devices in a chain, with the option to selectively bypass the MAX V CPLD by a dip switch setting. This switch will be one position of a 6-position switch. The other positions will consist of the MSEL bits for configuration modes, Fan Control and VID enable.

Program Select Push Button: After a **POWER-ON** or **RESET** (reconfiguration) event, the MAX V will configure the Arria 10 GX FPGA in FPP mode with either the FACTORY POF or a USER defined POF depending on FACTORY_LOAD setting. The setting of the **PGMSEL** bit is selected by the **PGMSEL** pushbutton. Pressing this button and observing the program LEDs (FACTORY or USER) dictates which program will be selected. Then the **PGM_CONFIG** pushbutton needs to be pressed to load the program.

MAX V RESET Push Button: This pushbutton is the board Master Reset. This button is connected to the MAX V CPLD (MAX_RESETn pin) that is used for FPP configuration. When this button is pressed, the MAX V CPLD will initiate a reloading of the stored image from flash memory using FPP configuration mode. The image that is reloaded depends on the **PGMSEL** setting.

CPU RESET Push Button: This pushbutton is the Nios II CPU Reset. This button is connected to an Arria 10 GX FPGA **DEV_CLRn** and can be used by Nios II implementations as a dedicated CPU Reset button. This button is also connected to the MAX V CPLD so that the FPGA device can be reset right after its configuration with FPP mode.

Clock Circuits

Transceiver Dedicated Clocks

The figure below shows the dedicated transceiver clocking that will be implemented for the FPGA. This clocking scheme will allow 4 different protocols to be running simultaneously by the Arria 10 GX FPGA.

Four differential clock sources are provided from an I2C programmable VCO oscillator to the dedicated REFCLK input pins of transceiver blocks on both sides of the FPGA. The default frequencies for these four oscillators at startup are:-

- 644.53125 MHz (Y3 left side xcvrs)
- 706.25 MHz (Y4 left side xcvrs)
- 625 MHz (Y5 right side xcvrs)
- 875 MHz (Y6 right side xcvrs)

The default frequencies can be overridden and a different frequency can be programmed into the oscillators for support of other protocols.

Caution: Programmed frequencies will be lost upon a board power down condition. Oscillator frequencies return to their default frequency upon power up.

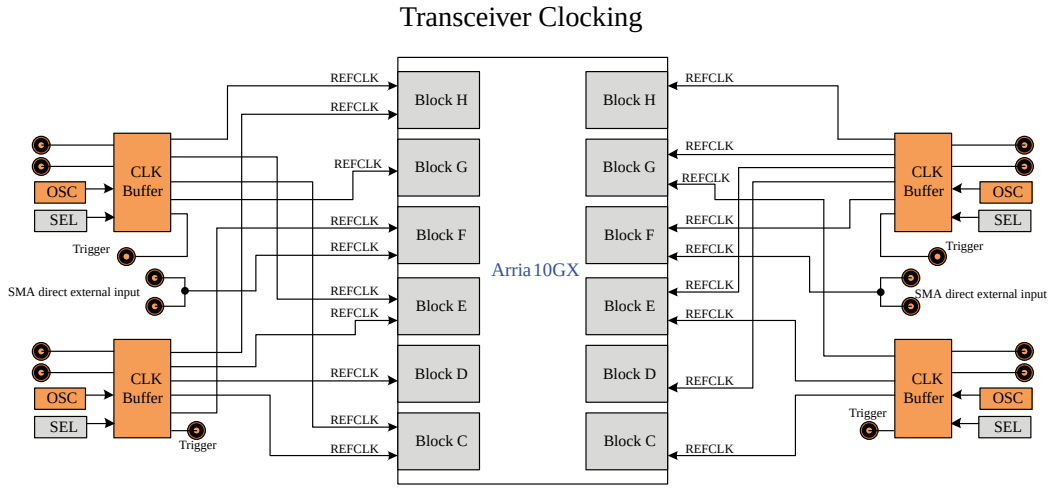
Each oscillator will support a programmable frequency range of 10 MHz - 1.4 GHz and provide a differential LVDS trigger output to SMA connectors for scope or other lab equipment triggering purposes.

In addition to the four oscillators, each side will have a dedicated differential REFCLK input from a pair of SMA connectors to allow use of lab equipment clock generators as the transceiver clock source.

The clock inputs described above all pass through a clock buffer first, the two inputs below connect directly to the transceiver clock inputs:-

- J122/J123 SMA connectors direct connection to REFCLK_GXBL1F block.
- J124/J125 SMA connectors direct connection to REFCLK_GXBR4F block.

Figure 5-7: Transceiver Dedicated Clocking



General Purpose Clocks

In addition to the transceiver dedicated clocks, five other clock sources will be provided to the FPGA Global CLK inputs for general FPGA design as shown in the figure below

The usage of these clocks is as follows:

1. 50 MHz oscillator through an ICS8304 buffer for Nios II applications. This clock is also routed to the MAX V device for configuration.
2. 25 MHz crystal supplied to an ICS557-03 Spread Spectrum differential clock buffer. The available frequencies and down spread percentages available from the spread spectrum buffer as shown in the table below
3. External differential clock source from SMA connectors.
4. Four 100 MHz clock outputs are provided from an SiLabs Si5338A-Custom clock buffer.
   - CLK0: 100MHz- LVDS standard
   - CLK1: 100MHz- LVDS standard
   - CLK2: 100MHz- 1.8V CMOS standard
   - CLK3: 100MHz- LVDS standard
5. One 125 MHz LVDS standard Oscillator output.

Figure 5-8: General Purpose FPGA Clocks

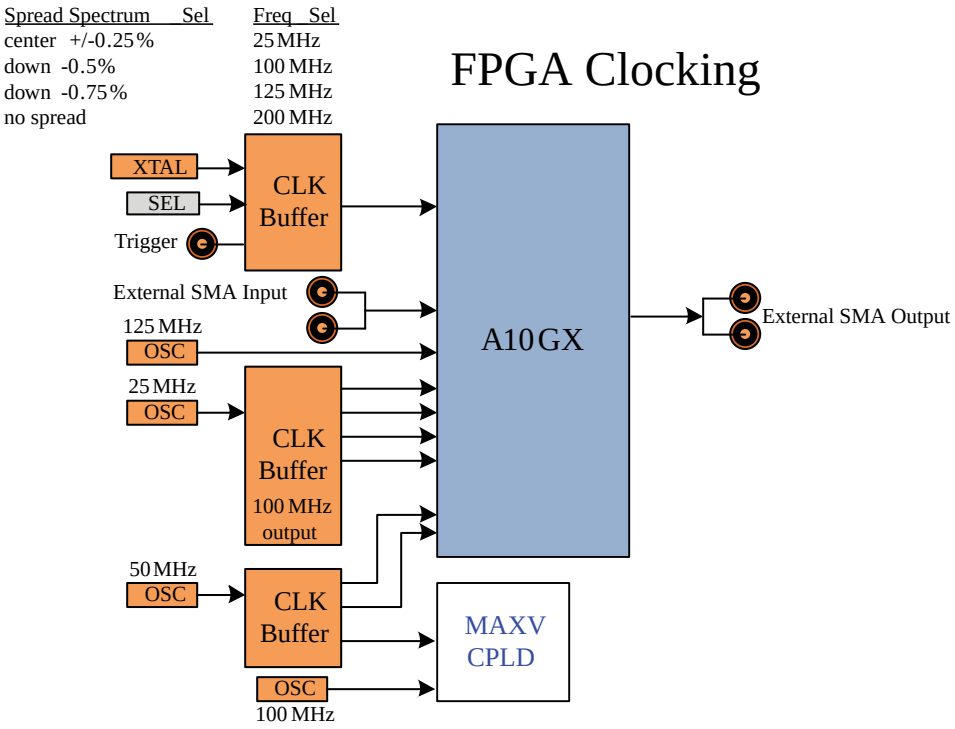


Table 5-7: Spread Spectrum Clock Settings and frequencies

Spread Spectrum Buffer (inputs)		Output Clock Select	Spread (%)
SS1/S1	**SS0/S0**		
0	0	25 MHz (Default)	Center +/- 0.25
0	1	100 MHz	Down -0.5
1	0	125 MHz	Down -0.75
1	1	200 MHz	No Spread

Embedded USB Blaster Clock

A 24 MHz oscillator is dedicated for the embedded USB2 Blaster circuitry. The oscillator is used to clock the Cypress CY7C68013A USB2 PHY device.

General User Input/Output

This section describes the user I/O interface to the FPGA. This section describes the following elements:

- User-defined push buttons
- User-defined DIP switches
- User-defined LEDs
- Character LCD

User-Defined Push Buttons

The development board includes 8 user-defined push buttons and 4 system push buttons that allow you to interact with the Arria 10 GX FPGA device. When you press and hold down the push button, the device pin is set to logic 0; when you release the push button, the device pin is set to logic 1. There is no board-specific function for these general user push buttons.

The table below lists the push buttons, schematic signal names and their corresponding Arria 10 GX FPGA device pin numbers.

Table 5-8: User-Defined Push Buttons

Board Reference	Schematic Signal Name	Description	Arria 10 Device Pin Number
S1	USER_PB0	User push button	AU22 (Arria 10 GX)
S2	USER_PB1	User push button	BA25 (Arria 10 GX)
S3	USER_PB2	User push button	AY25 (Arria 10 GX)
S4	USER_PB3	User push button	AY24 (Arria 10 GX)
S5	USER_PB4	User push button	BA24 (Arria 10 GX)
S6	USER_PB5	User push button	AU25 (Arria 10 GX)
S7	USER_PB6	User push button	AV25 (Arria 10 GX)
S8	USER_PB7	User push button	AY22 (Arria 10 GX)
S9	PGM_SEL	System push button	B13 (MAX V)

Board Reference	Schematic Signal Name	Description	Arria 10 Device Pin Number
S10	PGM_CONFIG	System push button	D12 (MAX V)
S11	MAX_RESETn	System push button	M9 (MAX V)
S12	CPU_RESETn	System push button	C12 (MAX V), BD27 (A10)

User-Defined DIP Switch

Board reference **SW2** and **SW6** are two 4-pin DIP switches. The switches are user-defined, and are provides additional FPGA input control. When the switch is in the **OPEN** position, a logic 1 is selected. When the switch is in the CLOSED or **ON** position, a logic 0 is selected. There is no board-specific function for these switches.

The table below lists the schematic signal names of each DIP switch and their corresponding Arria 10 GX FPGA pin numbers.

Table 5-9: User-Defined DIP Switches

Board Reference	Schematic Signal Name	Arria 10 GX Device Pin Number
SW6-1-8	USER_DIP3	BA18
SW6-2-7	USER_DIP2	BA17
SW6-3-6	USER_DIP1	BA20
SW6-4-5	USER_DIP0	BA19
SW2-4-5	USER_DIP4	BC21
SW2-3-6	USER_DIP5	BB21
SW2-2-7	USER_DIP6	BC20
SW2-1-8	A10_UNLOCK	BB20

User-Defined LEDs

The development board includes eight user-defined LEDs. Board references D13 through D20 are user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Arria 10 GX FPGA device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

The table below lists the user-defined schematic signal names and their corresponding Arria 10 device pin numbers

Table 5-10: User-Defined LEDs

Board Reference	Schematic Signal Name	Arria 10 Device Pin Number
D13	USER_LED0	AP22
D14	USER_LED1	AP23
D15	USER_LED2	AT25
D16	USER_LED3	AR25
D17	USER_LED4	AT23

Board Reference	Schematic Signal Name	Arria 10 Device Pin Number
D18	USER_LED5	AT24
D19	USER_LED6	AR24
D20	USER_LED7	AP24

Character LCD

A 16 character x 2 line LCD display will be connected to the Arria 10 GX FPGA device to display board information and IP address. The LCD module used is New Haven - NHD-0216K3Z-NSW-BBW-V3. This LCD module will be mounted to the Arria 10 GX transceiver signal integrity development board using a 1 x 10 vertical male 0.1" header on the left side of the module and 3 plastic standoffs. This mounting scheme will allow low profile (less than 0.5 inches in height) components to be placed underneath the LCD module, preserving board real-estate.

The table below summarizes the LCD pin assignments. The signals name and directions are relative to the Arria 10 GX FPGA device

Table 5-11: LCD Pin Assignments and Schematic Signal Names

Board Reference (J20)	Schematic Signal Name	Description
4	SPI_SS_DISP	SPI Slave Select option - voltage level translated from 5V to 1.8V
5	SPI_T_SS_DISP	SPI Slave Select option
7	I2C_5V_SCL	I2C serial clock
8	I2C_5V_SDA	I2C serial data

Transceiver Channels

The Arria 10 GX transceiver signal integrity development board dedicates 29 transceiver channels from both the left and right sides of the device. Transceiver channels are allocated as shown in the table below

Table 5-12: Arria 10 Transceiver Channels

Transceiver Channel	Data Rate	Number of channels
High Density Connector - J46 (Samtec Bullseye connector)	15 Gbps	5
High Density Connector - J47 (Samtec Bullseye connector)	15 Gbps	5
Amphenol (Excede+) Backplane Connector	15 Gbps	4
CFP2 Optical Interface	25.78 Gbps (applies to GT device only)	4

Transceiver Channel	Data Rate	Number of channels
SFP+ Optical Interface	14 Gbps	1
QSFP+ Optical Interface	25.78 Gbps (applies to GT device only)	4
2.4 mm SMA 'Gold' channel	15 Gbps	1
2.4 mm SMA 'Platinum' channel	15 Gbps	1
2.4 mm SMA channels	15 Gbps	4

Figure 5-9: Arria 10 GX Transceiver Usage Block Diagram

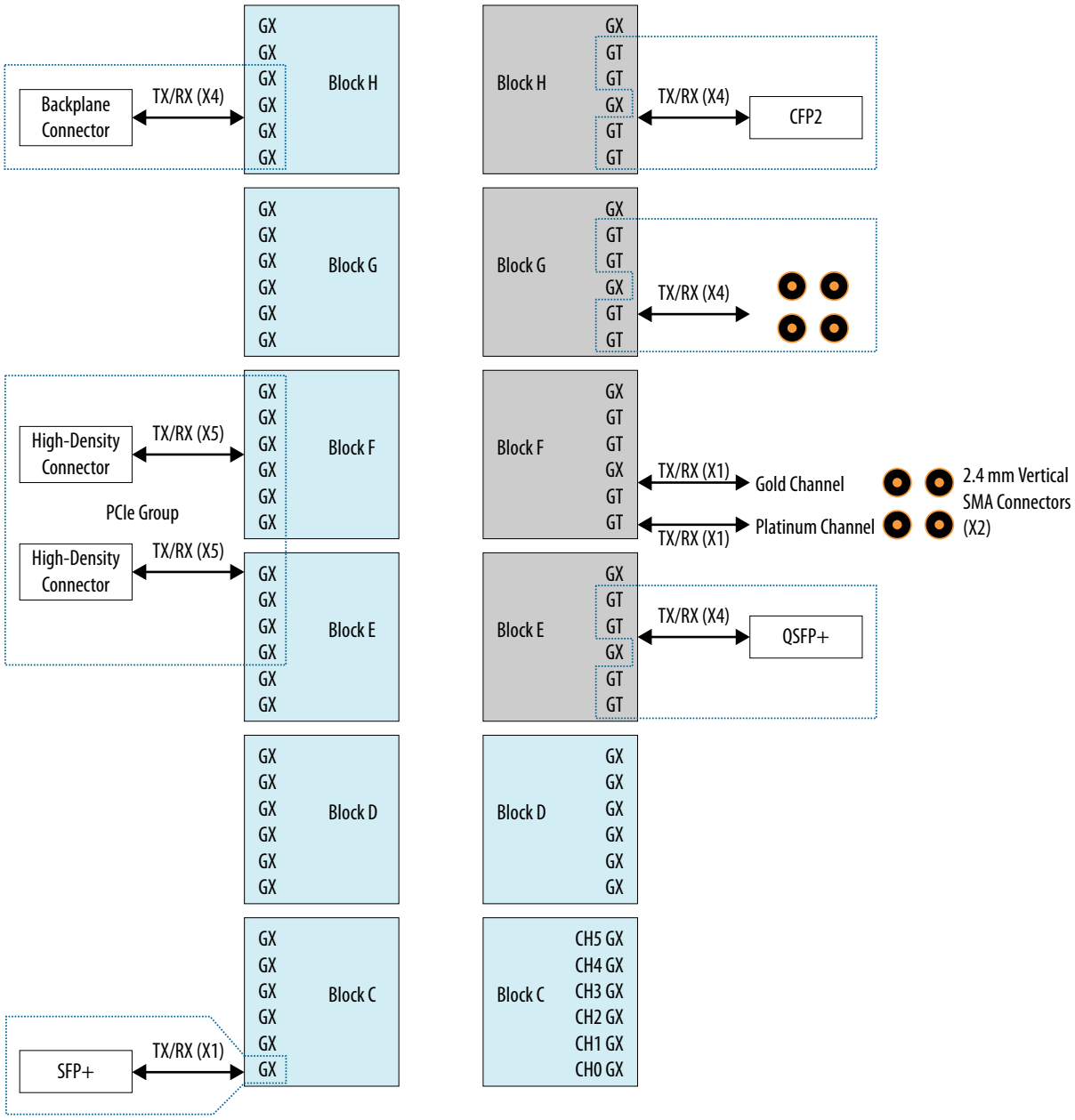


Table 5-13: Amphenol Backplane Connector (J22)

Signal Net Name	FPGA Pin Number	Description
GXBR_4H_TX0p	D1	GXB transmit
GXBR_4H_TX0n	D2	GXB transmit
GXBR_4H_TX1p	C3	GXB transmit
GXBR_4H_TX1n	C4	GXB transmit

Signal Net Name	FPGA Pin Number	Description
GXBR_4H_TX2p	B1	GXB transmit
GXBR_4H_TX2n	B2	GXB transmit
GXBR_4H_TX3p	A3	GXB transmit
GXBR_4H_TX3n	A4	GXB transmit
GXBR_4H_RX0p	H5	GXB receive
GXBR_4H_RX0n	H6	GXB receive
GXBR_4H_RX1p	G7	GXB receive
GXBR_4H_RX1n	G8	GXB receive
GXBR_4H_RX2p	F5	GXB receive
GXBR_4H_RX2n	F6	GXB receive
GXBR_4H_RX3p	E7	GXB receive
GXBR_4H_RX3n	E8	GXB receive

Table 5-14: QSFP+ Connector Interface (J28)

Signal Net Name	FPGA Pin Number	Description
GXBL_1E_TX0p	AP44	GXB transmit
GXBL_1E_TX0n	AP43	GXB transmit
GXBL_1E_TX1p	AM44	GXB transmit
GXBL_1E_TX1n	AM43	GXB transmit
GXBL_1E_TX3p	AH44	GXB transmit
GXBL_1E_TX3n	AH43	GXB transmit
GXBL_1E_TX4p	AF44	GXB transmit
GXBL_1E_TX4n	AF43	GXB transmit
GXBL_1E_RX0p	AG42	GXB receive
GXBL_1E_RX0n	AG41	GXB receive
GXBL_1E_RX1p	AF40	GXB receive
GXBL_1E_RX1n	AF39	GXB receive
GXBL_1E_RX3p	AD40	GXB receive
GXBL_1E_RX3n	AD39	GXB receive
GXBL_1E_RX4p	AC42	GXB receive
GXBL_1E_RX4n	AC41	GXB receive

Table 5-15: SFP+ Interface Connector (J29)

Signal Net Name	FPGA Pin Number	Description
GXBR_4C_TX0p	BC7	GXB transmit
GXBR_4C_TX0n	BC8	GXB transmit
GXBR_4C_RX0p	AW7	GXB receive
GXBR_4C_RX0n	AW8	GXB receive

Table 5-16: CFP2 Interface Connector (J24A / J24B)

Signal Net Name	FPGA Pin Number	Description
GXBL_1H_TX0p	D44	GXB transmit
GXBL_1H_TX0n	D43	GXB transmit
GXBL_1H_TX1p	C42	GXB transmit **Note:** TX1 p/n pins swapped at CFP2 connector J24B
GXBL_1H_TX1n	C41	GXB transmit **Note:** TX1 p/n pins swapped at CFP2 connector J24B
GXBL_1H_TX3p	A42	GXB transmit
GXBL_1H_TX3n	A41	GXB transmit
GXBL_1H_TX4p	B40	GXB transmit **Note:** TX4 p/n pins swapped at CFP2 connector J24B
GXBL_1H_TX4n	B39	GXB transmit **Note:** TX4 p/n pins swapped at CFP2 connector J24B
GXBL_1H_RX0p	H40	GXB receive **Note:** RX0 p/n pins swapped at CFP2 connector J24B
GXBL_1H_RX0n	H39	GXB receive **Note:** RX0 p/n pins swapped at CFP2 connector J24B
GXBL_1H_RX1p	G38	GXB receive
GXBL_1H_RX1n	G37	GXB receive

Signal Net Name	FPGA Pin Number	Description
GXBL_1H_RX3p	E37	GXB receive **Note:** RX3 p/n pins swapped at FPGA
GXBL_1H_RX3n	E38	GXB receive **Note:** RX3 p/n pins swapped at FPGA
GXBL_1H_RX4p	D40	GXB receive
GXBL_1H_RX4n	D39	GXB receive

Table 5-17: High Density Connectors - 2.4mm SMA Connectors (J46 / J47)

Signal Net Name	FPGA Pin Number	Description
GXBR_4E_TX_2p	AK1	GXB transmit
GXBR_4E_TX_2n	AK2	GXB transmit
GXBR_4E_TX_3p	AH1	GXB transmit
GXBR_4E_TX_3n	AH2	GXB transmit
GXBR_4E_TX_4p	AF1	GXB transmit
GXBR_4E_TX_4n	AF2	GXB transmit
GXBR_4E_TX_5p	AD1	GXB transmit
GXBR_4E_TX_5n	AD2	GXB transmit
GXBR_4E_RX_2p	AE3	GXB receive
GXBR_4E_RX_2n	AE4	GXB receive
GXBR_4E_RX_3p	AD5	GXB receive
GXBR_4E_RX_3n	AD6	GXB receive
GXBR_4E_RX_4p	AC3	GXB receive
GXBR_4E_RX_4n	AC4	GXB receive
GXBR_4E_RX_5p	AB5	GXB receive
GXBR_4E_RX_5n	AB6	GXB receive
GXBR_4F_TX_0p	AB1	GXB transmit
GXBR_4F_TX_0n	AB2	GXB transmit
GXBR_4F_TX_1p	Y1	GXB transmit
GXBR_4F_TX_1n	Y2	GXB transmit
GXBR_4F_TX_2p	V1	GXB transmit
GXBR_4F_TX_2n	V2	GXB transmit
GXBR_4F_TX_3p	T1	GXB transmit
GXBR_4F_TX_3n	T2	GXB transmit

Signal Net Name	FPGA Pin Number	Description
GXBR_4F_TX_4p	P1	GXB transmit
GXBR_4F_TX_4n	P2	GXB transmit
GXBR_4F_TX_5p	M1	GXB transmit
GXBR_4F_TX_5n	M2	GXB transmit
GXBR_4F_RX_0p	AA3	GXB receive
GXBR_4F_RX_0n	AA4	GXB receive
GXBR_4F_RX_1p	W3	GXB receive
GXBR_4F_RX_1n	W4	GXB receive
GXBR_4F_RX_2p	Y5	GXB receive
GXBR_4F_RX_2n	Y6	GXB receive
GXBR_4F_RX_3p	V5	GXB receive
GXBR_4F_RX_3n	V6	GXB receive
GXBR_4F_RX_4p	U3	GXB receive
GXBR_4F_RX_4n	U4	GXB receive
GXBR_4F_RX_5p	T5	GXB receive
GXBR_4F_RX_5n	T6	GXB receive

Communication Ports

The development board supports a 10/100/1000 BASE-T Ethernet connection using a Marvell 88E1111 PHY device and the Altera Triple-Speed Ethernet Megacore MAC function. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA. The Arria 10 GX FPGA device can communicate with the LVDS interfaces at up to 1.25 Gbps. The MAC function must be provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5-V and 1.2-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to an RJ-45 connector with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Table 5-18: Ethernet PHY Pin Assignments

Schematic Signal Name	88E1111 PHY (U35) Pin Number	Description
ENET_LED_LINK1000	60/73	1000-Mb link LED
ENET_LED_LINK100	74	100-Mb link LED
ENET_LED_LINK_10	59/76	10-Mb link LED
ENET_LED_TX	68	TX data active LED
ENET_LED_RX	69	RX data active LED
ENET_SGMII_TX_P	82	SGMII transmit
ENET_SGMII_TX_N	81	SGMII transmit
ENET_SGMII_RX_P	77	SGMII receive

Schematic Signal Name	88E1111 PHY (U35) Pin Number	Description
ENET_SGMII_RX_N	75	SGMII receive
ENET_XTAL_25MHZ	55	25 MHz clock
ENET_T_INTn	23	Management bus Interrupt
ENET_RSET	30	Device reset
MDIO_T	24	Management bus data input/output
MDC_T	25	Management bus data clock
MDI_P0	29	Management bus data
MDI_N0	31	Management bus data
MDI_P1	33	Management bus data
MDI_N1	34	Management bus data
MDI_P2	39	Management bus data
MDI_N2	41	Management bus data
MDI_P3	42	Management bus data
MDI_N3	43	Management bus data

Flash Memory

The development board has two 1-Gbit CFI compatible synchronous flash device for non-volatile storage of the FPGA configuration data, board information, test application data and user code space.

Two Flash devices are implemented to achieve a 32-bit wide data bus at 16 bits each per device. The target device is a Micron PC28F00AP30BF CFI Flash device. Both MAX V CPLD and Arria 10 GX FPGA can access this Flash device. MAX V CPLD accesses will be for FPP configuration of the FPGA at power-on and board reset events. This will use the Altera PFL Megafunction. Arria 10 GX FPGA access to the FLASH's user space will be done by Nios II for the BUP application. The flash will be wired for WORD mode operation to support FPPx32 download directly.

The table below shows the memory map for the on-board flash. This memory will provide non-volatile storage for two FPGA bit-streams as well as various settings for data used for the BUP image and on-board devices such as PFL configuration bits.

Table 5-19: Flash Memory Map

Block Description	Size	Address
Board Test System	512 KB	0x09F4.0000 - 09FB.FFFF
User Software	14,336 KB	0x0914.0000 - 09F3.FFFF
Factory Software	8,192 KB	0x0894.0000 - 0913.FFFF
zipfs	8,192 KB	0x0814.0000 - 0893.FFFF
User Hardware 2	44,032 KB	0x0564.0000 - 0813.FFFF
User Hardware 1	44,032 KB	0x02B4.0000 - 0563.FFFF

Block Description	Size	Address
Factory Hardware	44,032 KB	0x0004.0000 - 02B3.FFFF
PFL Option Bits	64 KB	0x0003.0000 - 0003.FFFF
Board Information	64 KB	0x0002.0000 - 0002.FFFF
Ethernet Option Bits	64 KB	0x0001.0000 - 0001.FFFF
User Design Reset	64 KB	0x0000.0000 - 0000.FFFF

Each FPGA bit stream can be a maximum of 254.25 Mbits (or less than 32 MBytes) for the Arria 10 GX FPGA device. The remaining area will be designated as RESERVED flash area for storage of the BUP image and PFL configuration settings, software binaries and other data relevant to the FPGA design.

The table below lists the flash pin assignments, signal names and functions

Table 5-20: Flash Memory Pin Assignments, Signal Names and Functions

FLASH Memory Device Pin Number (U33/ U34)	Schematic Signal Name	Description	Arria 10 Device Pin Number
A1 (U33/U34)	FM_A1	Address Bus	F28
B1 (U33/U34)	FM_A2	Address Bus	F27
C1 (U33/U34)	FM_A3	Address Bus	G28
D1 (U33/U34)	FM_A4	Address Bus	G27
D2 (U33/U34)	FM_A5	Address Bus	H25
A2 (U33/U34)	FM_A6	Address Bus	G25
C2 (U33/U34)	FM_A7	Address Bus	K27
A3 (U33/U34)	FM_A8	Address Bus	D31
B3 (U33/U34)	FM_A9	Address Bus	C31
C3 (U33/U34)	FM_A10	Address Bus	C30
D3 (U33/U34)	FM_A11	Address Bus	C29
C4 (U33/U34)	FM_A12	Address Bus	E30
A5 (U33/U34)	FM_A13	Address Bus	E31
B5 (U33/U34)	FM_A14	Address Bus	E29
C5 (U33/U34)	FM_A15	Address Bus	D29
D7 (U33/U34)	FM_A16	Address Bus	F30
D8 (U33/U34)	FM_A17	Address Bus	F29
A7 (U33/U34)	FM_A18	Address Bus	J29
B7 (U33/U34)	FM_A19	Address Bus	K31
C7 (U33/U34)	FM_A20	Address Bus	K30
C8 (U33/U34)	FM_A21	Address Bus	L30
A8 (U33/U34)	FM_A22	Address Bus	L29

FLASH Memory Device Pin Number (U33/ U34)	Schematic Signal Name	Description	Arria 10 Device Pin Number
G1 (U33/U34)	FM_A23	Address Bus	G30
H8 (U33/U34)	FM_A24	Address Bus	G31
B6 (U33/U34)	FM_A25	Address Bus	H29
B8 (U33/U34)	FM_A26	Address Bus	H30
F2 (U33)	FM_D0	Data Bus	H34
E2 (U33)	FM_D1	Data Bus	J33
G3 (U33)	FM_D2	Data Bus	J32
E4 (U33)	FM_D3	Data Bus	L34
E5 (U33)	FM_D4	Data Bus	K34
G5 (U33)	FM_D5	Data Bus	N34
G6 (U33)	FM_D6	Data Bus	M35
H7 (U33)	FM_D7	Data Bus	M32
E1 (U33)	FM_D8	Data Bus	L32
E3 (U33)	FM_D9	Data Bus	U32
F3 (U33)	FM_D10	Data Bus	T32
F4 (U33)	FM_D11	Data Bus	R30
F5 (U33)	FM_D12	Data Bus	R31
H5 (U33)	FM_D13	Data Bus	U33
G7 (U33)	FM_D14	Data Bus	T33
E7 (U33)	FM_D15	Data Bus	N33
F2 (U34)	FM_D16	Data Bus	P33
E2 (U34)	FM_D17	Data Bus	R34
G3 (U34)	FM_D18	Data Bus	P34
E4 (U34)	FM_D19	Data Bus	T34
E5 (U34)	FM_D20	Data Bus	T35
G5 (U34)	FM_D21	Data Bus	D26
G6 (U34)	FM_D22	Data Bus	E26
H7 (U34)	FM_D23	Data Bus	A28
E1 (U34)	FM_D24	Data Bus	A27
E3 (U34)	FM_D25	Data Bus	B28
F3 (U34)	FM_D26	Data Bus	B27
F4 (U34)	FM_D27	Data Bus	B26
F5 (U34)	FM_D28	Data Bus	C26

FLASH Memory Device Pin Number (U33/ U34)	Schematic Signal Name	Description	Arria 10 Device Pin Number
H5 (U34)	FM_D29	Data Bus	D27
G7 (U34)	FM_D30	Data Bus	E27
E7 (U34)	FM_D31	Data Bus	C28
E6 (U33/U34)	FLASH_CLK	Clock	AU31
D4 (U33/U34)	FLASH_RESETn	Reset	AP31
B4 (U33)	FLASH_CEn0	Chip Enable 0	AT30
B4 (U34)	FLASH_CEn1	Chip Enable 1	AR31
F8 (U33/U34)	FLASH_OEn	Output Enable	AT34
G8 (U33/U34)	FLASH_WEn	Write Enable	AR35
F6 (U33/U34)	FLASH_ADVn	Address Valid	AU30
C6 (U33/U34)	FLASH_WPn	Write Protect	----
F7 (U33)	FLASH_RDYBSYn0	Ready / Busy	AT35
F7 (U34)	FLASH_RDYBSYn1	Ready / Busy	AN31

- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software. When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FM_A1 mapped to address bit 2 in software.

Power Supply

Power for this board will be provided through an external Laptop style DC power brick connected to a 4-pin power DIN jack (CUI Inc. PD-40S). The input voltage must be in the range of 12V +/- 5%. This DC voltage is then stepped down to the various power rails used by the components on the board.

Some power rails on the board will have the option to be supplied from an external source via banana jack connectors by first removing a jumper for that power rail.

Table 5-21: Power per Device

Device	Voltage Name	Voltage	Note
FPGA (10AX115)	VCC	0.8/0.85/0.9	Core voltage
	VCCERAM	0.9/0.95	Memory Power Pins
	VCCP	0.8/0.85/0.9	Periphery Power
	VCCPGM	1.2/1.5/1.8	Configuration Power
	VCCBAT	1.2/1.8	Battery Backup supply for Design Security Volatile Key Register
	VCCIO	1.2/1.25/1.35/1.5/1.8	IO Voltage
	VCCPT	1.5/1.8/2.5/3.0	Programmable Power Technology and I/O Pre-drivers
	VCCA_PLL	1.8	PLL Analog Power
	VCCT VCCR	0.9/1.1	XCVR voltage TX/RX Paths
	VCCH	1.8	XCVR voltage TX Buffer
MAX V_FPP (EPM2210_ 256FBGA)	1.8V	1.8	Core, configuration, VCCIO
FLASH (PC28F00BP30BF)	1p8V	1.8	Configuration
MAXII_USB (EPM570M100)	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V	Core, configuration, VCCIO for USB2 Interface
USB PHY (CY7C68013A_ QFN)	VCC	3.3V	USB PHY
Ethernet PHY (88E1111)	2.5V/1.2V	2.5 1.2	Ethernet PHY
Power Monitor (LTM2987CY / LTC2974)	12V	12.0	Power Monitor Devices
Temp Sense ADC (MAX 1619)	3.3V	3.3	Temperature Measure
Clock Buffer (SL18860DC)	1.8V	1.8	50 MHz clock source to FPGA / MAX V
Clock Buffer(x4) (Si53311)	2.5V	2.5	Transceiver Reference Clock Buffers
SS Clock Generator (ICS557)	3.3V	3.3	Spread Spectrum/ Clock Select capability to core clock
Programmable Clock Buffer Si5338A	1.8V/2.5V	1.8V/2.5V	100 MHz clock source to FPGA/ MAX V core clock inputs

Device	Voltage Name	Voltage	Note
SFP+ Module	SFP_VCCT / SFP_ VCCR (3.3V)	3.3	SFP+ module
CFP2 Module	CFP2_3.3V_FLT CFP2_1.2V	3.3 / 1.2	CFP2 module
eQSFP+ Module	QSFP_VCC1/QSFP_ VCCTX/QSFP_ VCCRX (3.3V)	3.3	QSFP module

Power Measurement

There are ten voltage rails that are monitored by an LTM2987 and LTC2974 Power Monitor devices. The voltage rails monitored are listed in the table below. These power monitor devices are capable of measuring the voltage, measuring the current, trimming the voltage, and sequencing the order at power on and power off. Voltages can be trimmed up to +/-10%. Communication to these devices is through I2C interface. A Linear Technology power monitor application know as LTPowerPlay can be utilized to measure, trim, and observe each voltage rail's condition.

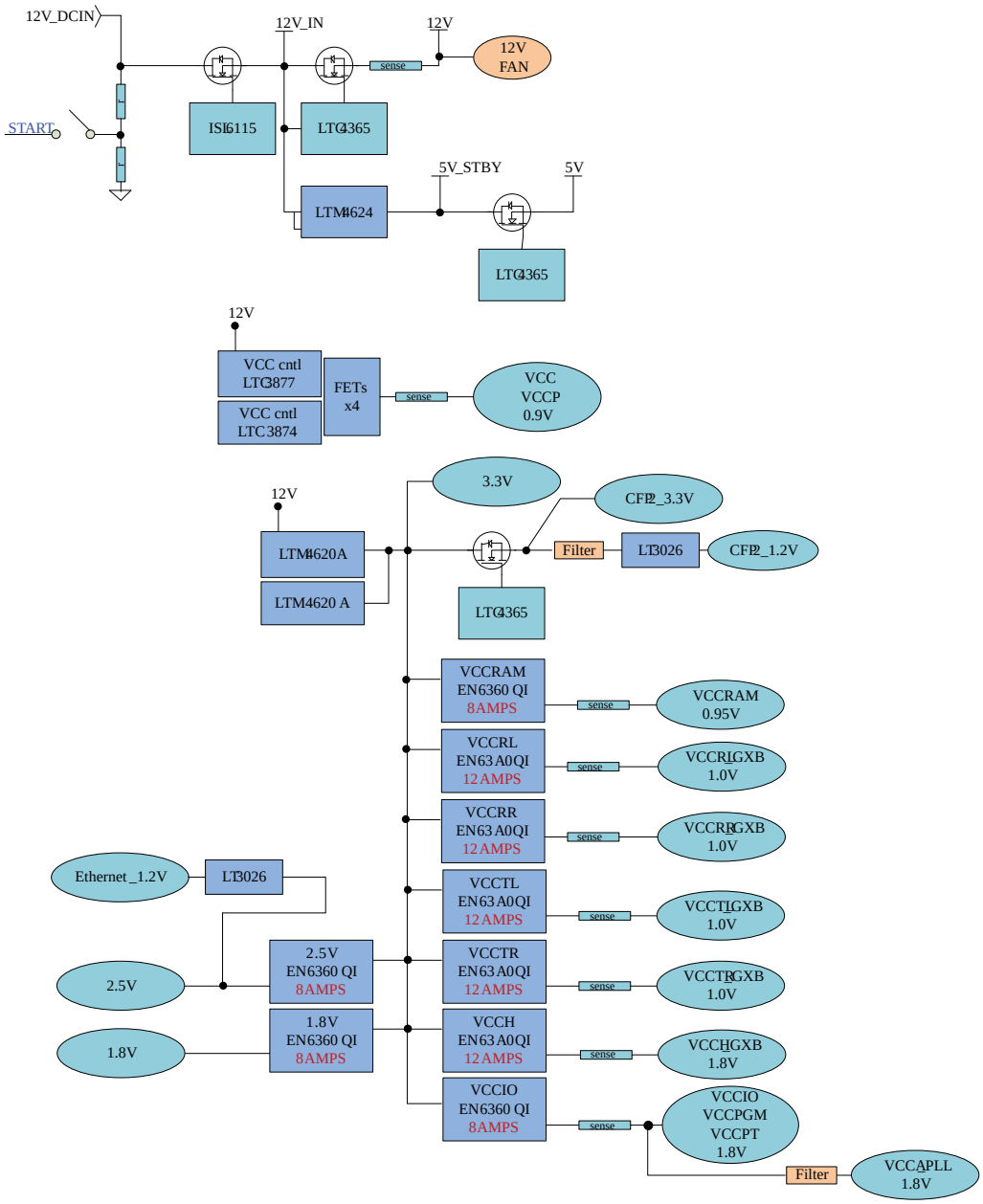
Table 5-22: Measured Voltage Rails

Rail No.	Measured Net Name	Voltage	Description
1	VCC	0.8V/0.85V/0.9V	FPGA Core voltage
2	VCCRL	0.9V/1.1V	XCVR RX path - left side
3	VCCRR	0.9V/1.1V	XCVR RX path - right side
4	VCCTL	0.9V/1.1V	XCVR TX path - left side
5	VCCTR	0.9V/1.1V	XCVR TX path - right side
6	VCCH	1.8V	XCVR TX Buffer
7	VCCRAM	0.95V	FPGA Memory Power pins
8	A10GX_1.8V power	1.8V	FPGA I/O
9	12V	12V	12V Input Power
10	3.3V	3.3V	3.3V Input Power

Power Distribution System

The figure shows the power distribution system on the Arria 10 GX transceiver signal integrity development board.

Figure 5-10: Power Distribution System



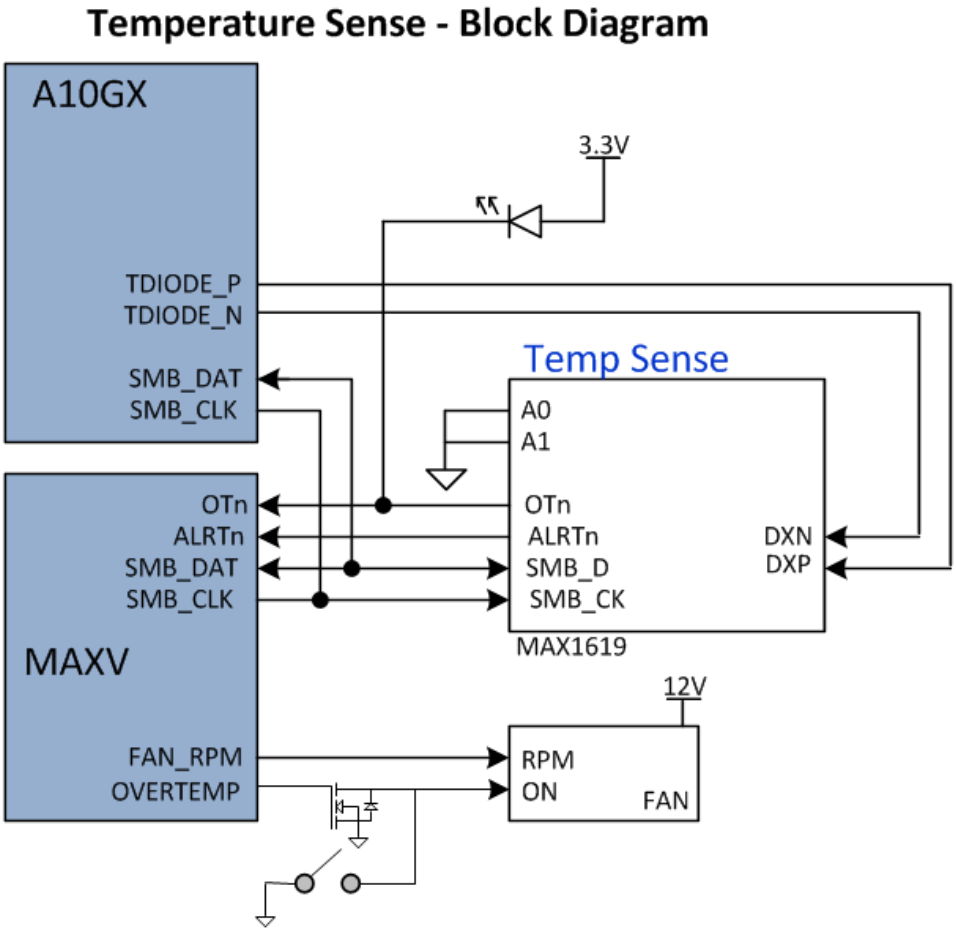
Temperature Sense

Temperature monitoring will be done by a MAX1619 dual temperature sense device. This device will allow temperature sensing of both the Arria 10 GX FPGA die and board ambient. The MAX1619 is connected to the Arria 10 GX FPGA by a 2-wire SMBus interface. Additionally, the OverTemp (OTn) and ALERTn signals from the MAX1619 is brought to the MAX V device to allow it to immediately sense a temperature fault condition and turn on the Arria 10 GX FPGA's attached FAN.

An over temperature warning LED (amber-colored) is provided for the Arria 10 GX FPGA device. This LED will indicate the temperature fault condition and that the FAN should be connected and running. The fan will be controlled by the OverTemp signal from the MAX1619 and can be set to turn on when the

Arria 10 GX FPGA die temperature exceeds a specified set point. Temperature fault set points can be programmed into the MAX1619. The HDL design code along with **.sof/.pof** files are provided to the user.

Figure 5-11: Temperature Measurement Circuit



Board Test System 6

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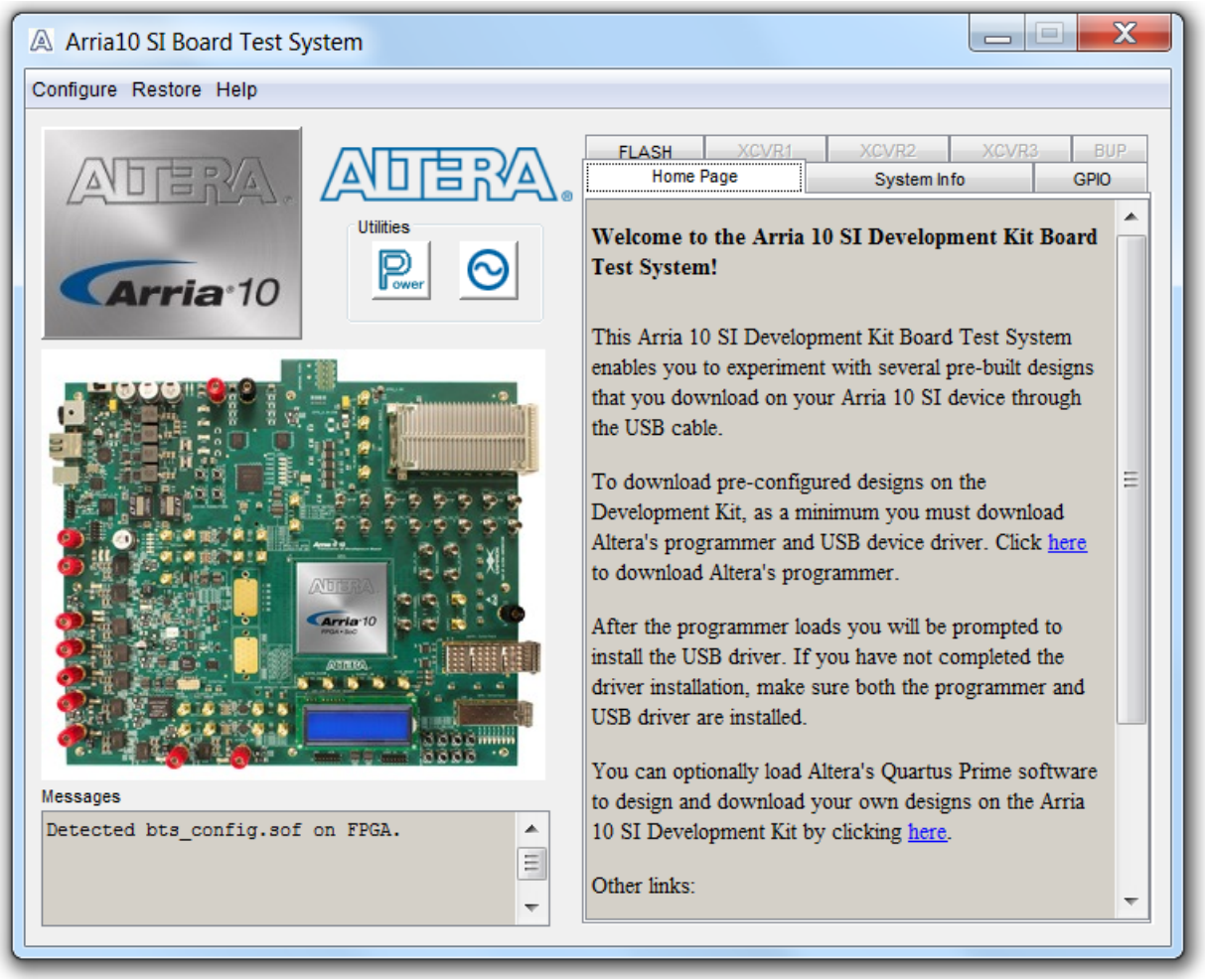
This development kit includes a design example and an application called the Board Test System (BTS) to test the functionality of the Arria 10 GX Transceiver Signal Integrity Development Board.

The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. The application is also useful as a reference for designing systems.

The Board Test System communicates over the JTAG bus to a test design running in the Arria 10 GX FPGA device. The figure below shows the initial Graphic User Interface (GUI) for a board that is in the factory configuration.

Figure 6-1: Board Test System Graphical User Interface



Preparing the Board

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The **Configure** menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The Board Test System shares the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus Prime Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus Prime Programmer.

With the power to the board OFF, following these steps:

1. Connect the USB cable to the board.

If you connect an external USB-Blaster download cable and power cycle the board, the on-board Blaster is disabled. To successfully use the USB-Blaster cable, disconnect it before power cycling the board. After you power cycled the board, then reconnect the USB-Blaster cable.

2. Ensure that the development board DIP switches are set to the default positions as shown in the "**Factory Default Switch Settings** on page 3-2".

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached.

Running the Board Test System

Before you begin

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `$QUARTUS_ROOTDIR`. The Board Test System uses this environment variable to locate the Quartus Prime library. The version of Quartus Prime software set in the `$QUARTUS_ROOTDIR` environment variable should be newer than version 14.1. For example, the Development Kit Installer version 15.1 requires that the Quartus Prime software 14.1 or later version to be installed.

Also, to ensure that the FPGA can be configured successfully, you should install the latest Quartus Prime software which can support the silicon on the development kit.

Please refer to the **README.txt** file under **examples\board_test_system** directory.

To run the application:

1. Navigate to the **<package dir>\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.
2. A GUI appears, displaying the application tab corresponds to the design running in the FPGA. If the design loaded in FPGA is not supported by BTS GUI, you will receive a message prompting you to configure your board with a valid Board Test System design. Refer to **The Configure Menu** on page 6-4 for information on configuring your board.

Version Selector

The Board Test System (BTS) will prompt you with a Version Selector window once opened. You can also open the Version Selector window through the **Configure** tab by clicking **Select Silicon Version**. Select the silicon version of the Arria 10 GX FPGA device that is installed on your board.

Figure 6-2: Version Selector

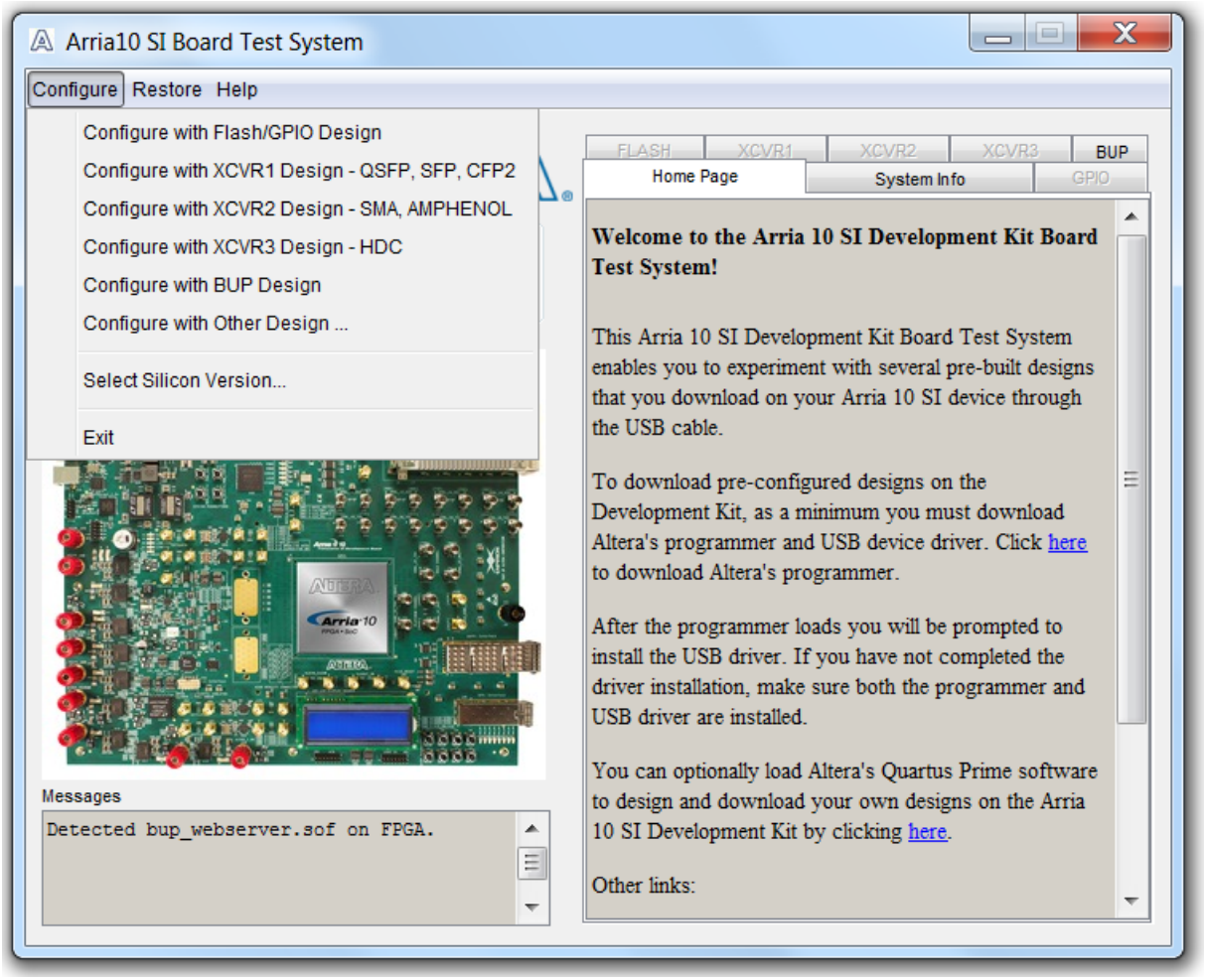
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 6-3: The Configure Menu



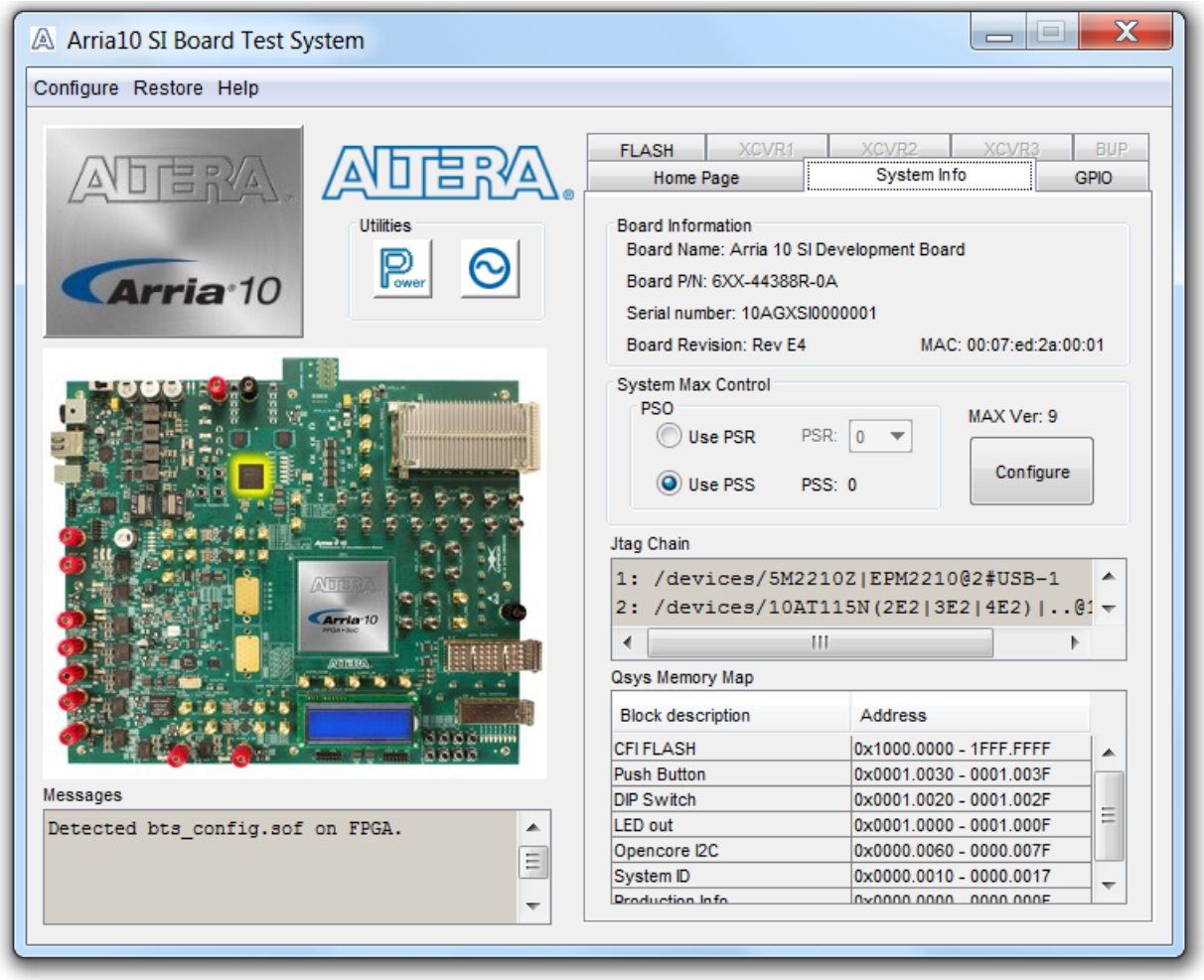
To configure the FPGA with a test system design, perform the following steps:

- On the **Configure** menu, click the **configure** command that corresponds to the functionality you wish to test.
- In the dialog box that appears, click **Configure** to download the corresponding design's **SRAM Object File (.sof)** to the FPGA. The download process usually takes less than a minute.
- When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, rather than the Board Test System GUI, you may need to restart the GUI.

The System Info Tab

The **System Info** tab shows information about the board's current configuration. The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

Figure 6-4: The System Info Tab



The following sections describe the controls on the **System Info** tab.

Board Information

The Board information control displays static information about your board.

- Board Name—Indicates the official name of the board, given by the Board Test System.
- Board P/N—Indicates the part number of the board.
- Serial number—Indicates the serial number of the board.
- Factory test version—Indicates the version of the Board Test System used to production test the board.
- MAX V ver—Indicates the version of MAX V code currently running on the board.

The MAX V code resides in the **<package dir>\examples\max5** directory. Newer revisions of this code might be available on the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page of the Altera website.

- MAC—Indicates the MAC address of the board.

MAX V Registers

The MAX V registers control allows you to view and change the current MAX V register values as described in the table below. Changes to the register values with the GUI take effect immediately.

Table 6-1: MAX V Registers

MAX V Register Values	Description
SRST	Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values.
PSO	Sets the MAX V PSO register.
PSR	Sets the MAX V PSR register. Allows PSR to determine the page of flash memory to use for FPGA reconfiguration. The numerical values in the list corresponds to the page of flash memory to load during the FPGA reconfiguration.
PSS	Displays the MAX V PSS register value. Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.

Because the System Info tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The JTAG chain control shows all the devices currently in the JTAG chain. The Arria 10 GX FPGA device is always the first device in the chain.

Note: When set to 1, switch SW13.6 (MAX BYPASS) includes the MAX V device in the JTAG chain; when set to 0, the MAX V device is removed from the JTAG chain.

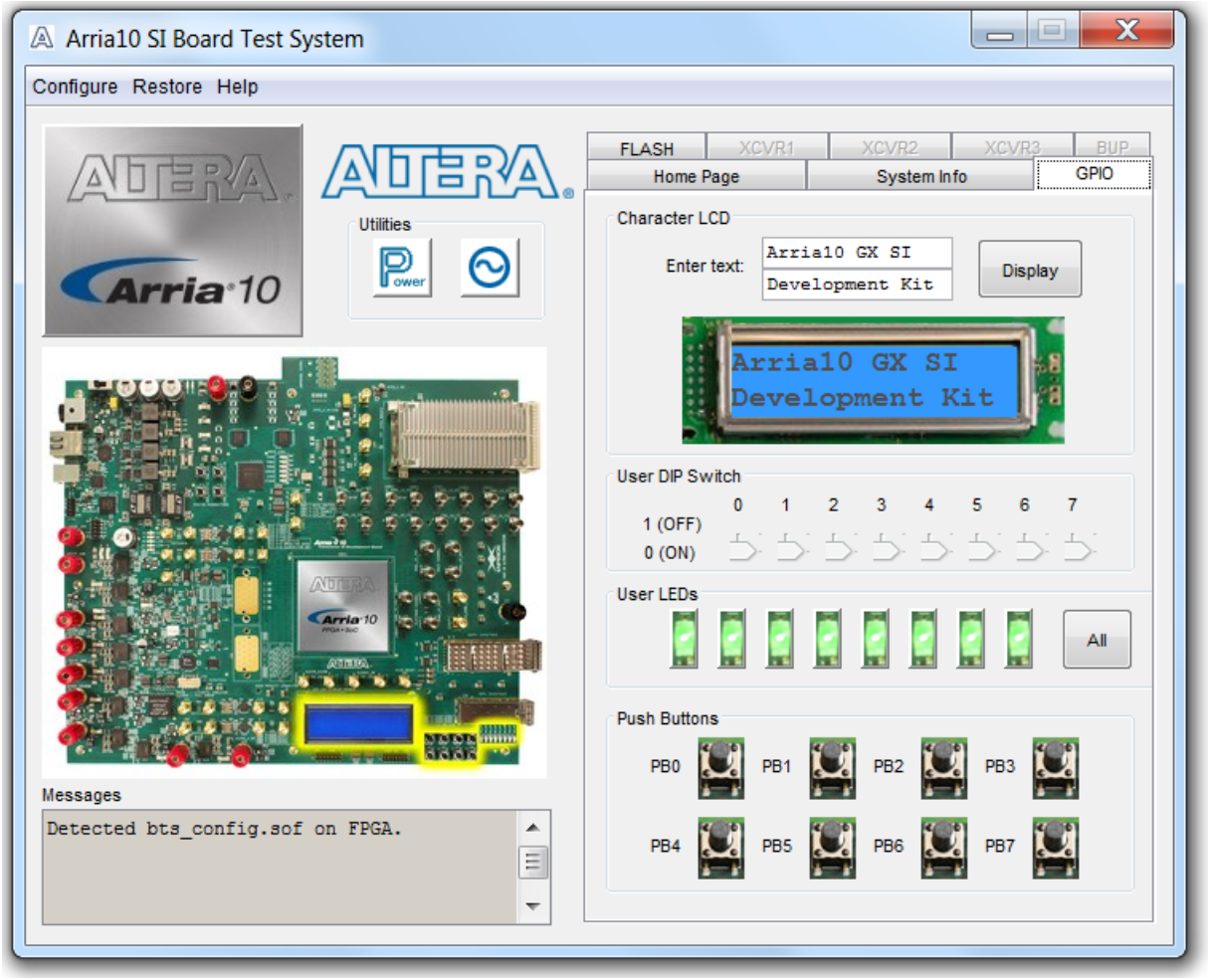
Qsys Memory Map

The Qsys memory map control shows the memory map of **bts_config.sof** design running on your board.

The GPIO Tab

The **GPIO tab** allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 6-5: The GPIO Tab



The following sections describe the controls on the GPIO tab.

Character LCD

The Character LCD controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click Display. If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only User DIP switches control displays the current positions of the switches in the user DIP switch bank (**SW2** and **SW6**). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

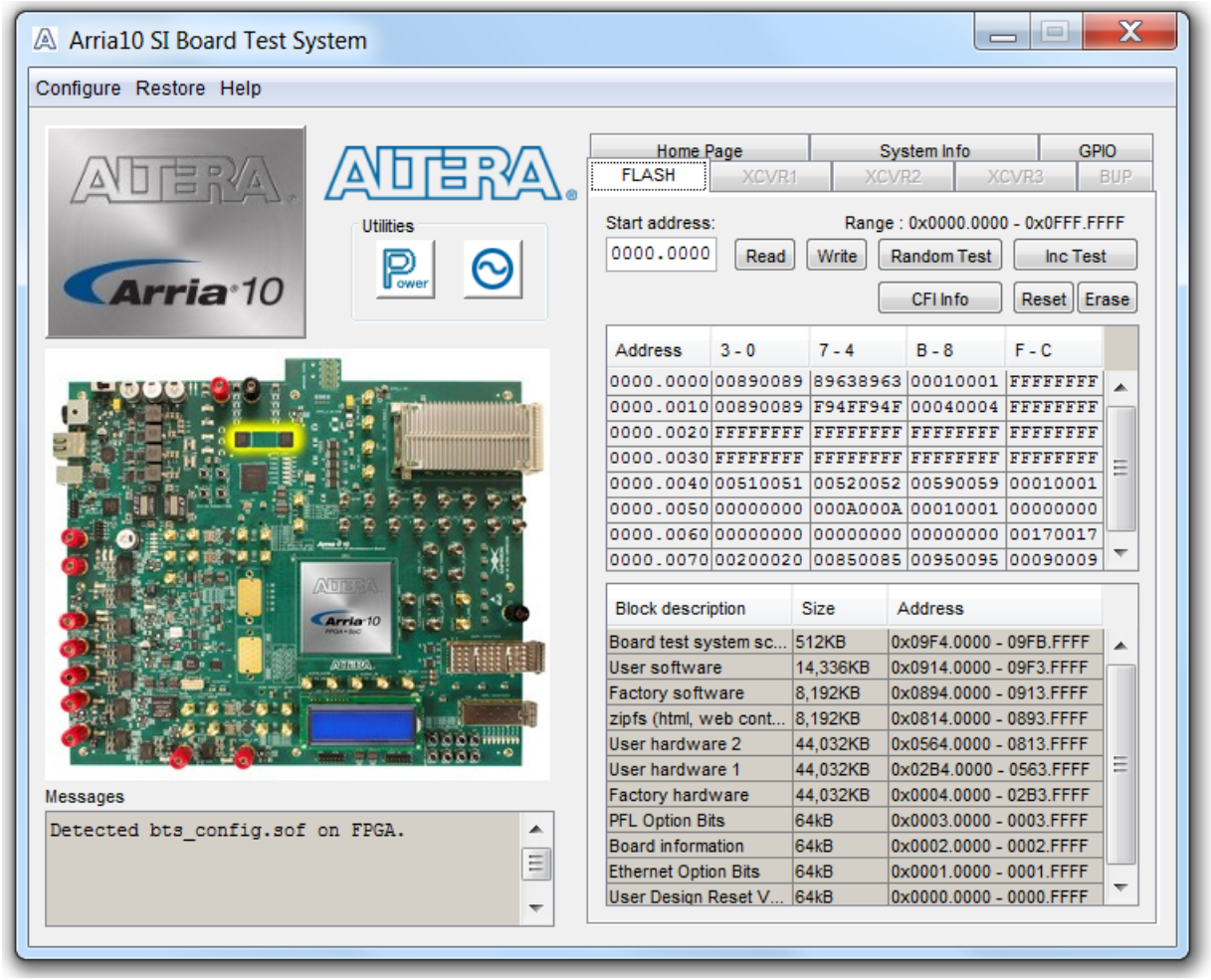
Push Button Switches

The read-only Push button switches control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash tab** allows you to read and write flash memory on your board.

Figure 6-6: The Flash Tab



The following sections describe the controls on the Flash tab.

Read

The Read control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table. The flash memory sits at a base address of 0x1000.0000. To see flash memory contents type the address above the base and values starting at this address are displayed. Valid entries are 0x0000.0000 through 0x0FFF.FF80.

Caution: If you enter an address outside of 0x0000.0000 to 0x07FF.FFFF flash memory address space, a warning message identifies the valid flash memory address range.

Write

The Write control writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Caution: To prevent overwriting the dedicated portions of flash memory, the application limits the writable flash memory address range to 0x0FF80000 - 0x0FFFFF80 (which corresponds to address range 0x0000.0000 - 0x00080000 in the uppermost portion of the user software memory block).

Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 512K block.

CFI Info

The CFI Query control updates the memory table, displaying the CFI ROM table contents from the flash device.

Inc Test

Starts an incrementing data pattern test to flash memory, which is limited to scratch page in the upper 512K block.

Reset

The Reset control executes the flash device's reset command and updates the memory table displayed on the Flash tab.

Erase

When erasing flash memory contents should read FFFF FFFF, which is limited to a scratch page in the upper 512K block.

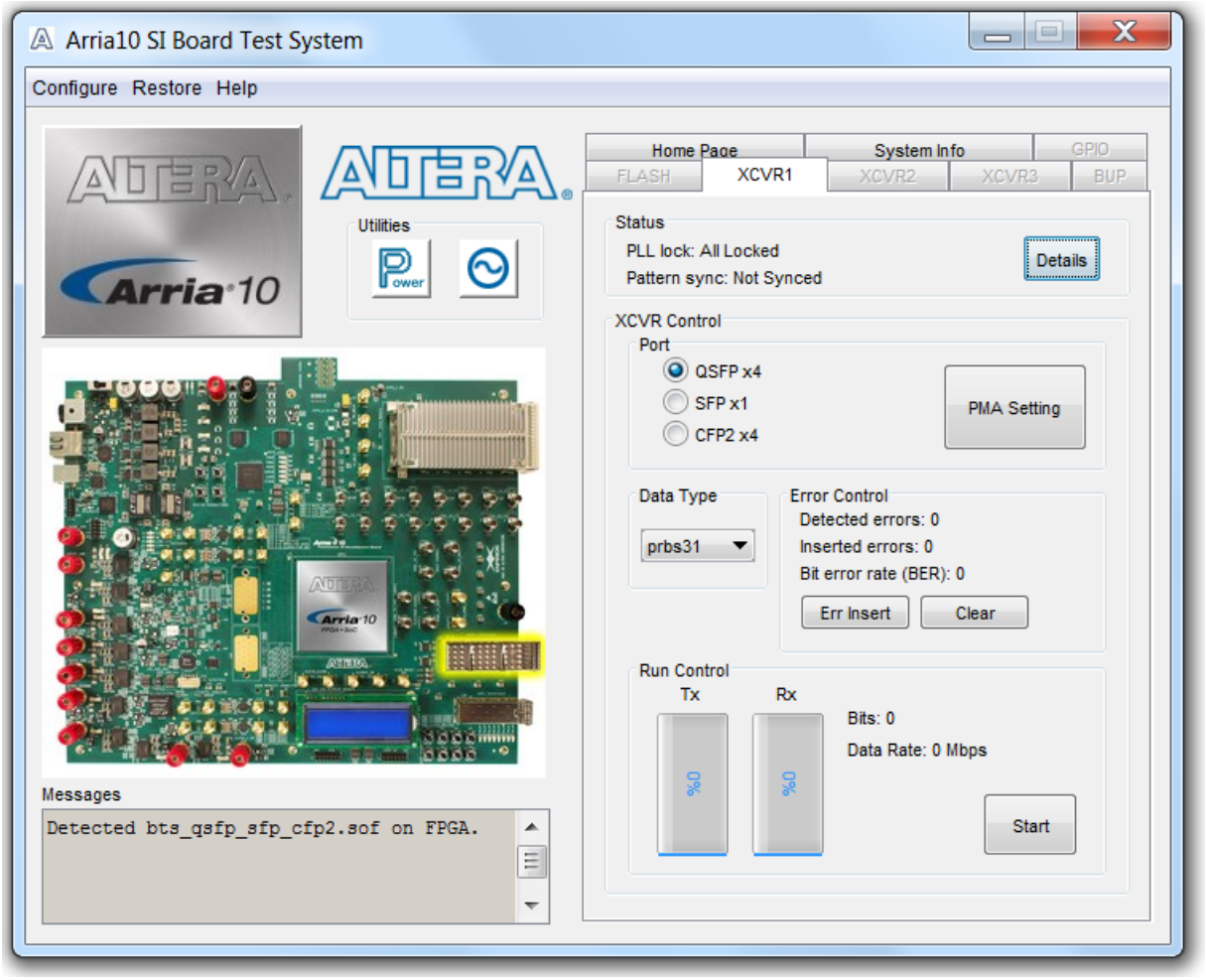
Flash Memory Map

Displays the flash memory map for the Arria 10 GX transceiver signal integrity development kit.

The XCVR #1 Tab

The **XCVR #1** tab allows you to run transceivers QSFP, SFP+ and CFP2 loopback tests on your board. You can run the test using either electrical loopback modules or optical fibre modules.

Figure 6-7: The XCVR #1 Tab



The following sections describe the controls on the XCVR #1 tab.

Status

The Status control displays the following status information during the loopback test:

- PLL lock—Shows the PLL locked or unlocked state.
- Pattern sync—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details - Shows the PLL lock and pattern sync status.

Related Information

- **Status** on page 6-14
- **Status** on page 6-16

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

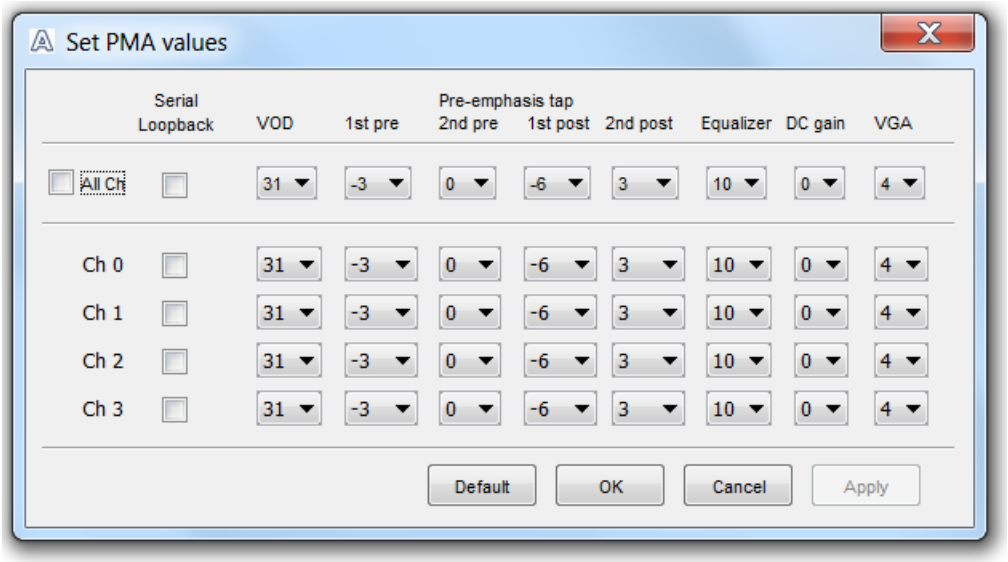
- QSFP
- SFP +
- CFP2

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

1. Serial Loopback - Routes signals between the transmitter and the receiver.
2. VOD - Specifies the voltage output differential of the transmitter buffer.
3. Pre-emphasis tap :
   - 1st pre - Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
   - 2nd pre - Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
   - 1st post - Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
   - 2nd post - Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
4. Equalizer - Specifies the AC gain setting for the receiver equalizer in four stage mode.
5. DC Gain - Specifies the DC gain setting for the receiver equalizer in four stage mode.
6. VGA - Specifies the VGA gain value.

Figure 6-8: PMA Settings



Related Information

- **PMA Setting** on page 6-15
- **PMA Setting** on page 6-16

Data Type

The Data type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- PRBS7 —pseudo-random 7-bit sequences (default)
- PRBS15—pseudo-random 15-bit sequences
- PRBS23—pseudo-random 23-bit sequences
- PRBS31—pseudo-random 31-bit sequences
- HF—highest frequency divide-by-2 data pattern "10101010"
- LF —lowest frequency divide by 33 data pattern

Settings HF and LF are for transmit observation only and are not intended for use in the receiver data detection circuitry.

Related Information

- **Data Type** on page 6-15
- **Data Type** on page 6-17

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- Detected errors—Displays the number of data errors detected in the received bit stream.
- Inserted errors—Displays the number of errors inserted into the transmit data stream.
- Insert Error—Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear—Resets the Detected errors and Inserted errors counters to zeros.

Related Information

- **Error Control** on page 6-15
- **Error Control** on page 6-17

Run Control

- TX and RX performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Start—This control initiates the loopback tests.
- Stop—This control terminates the loopback tests.
- Tx (MBps) and Rx (MBps)—Show the number of bytes of data analyzed per second.

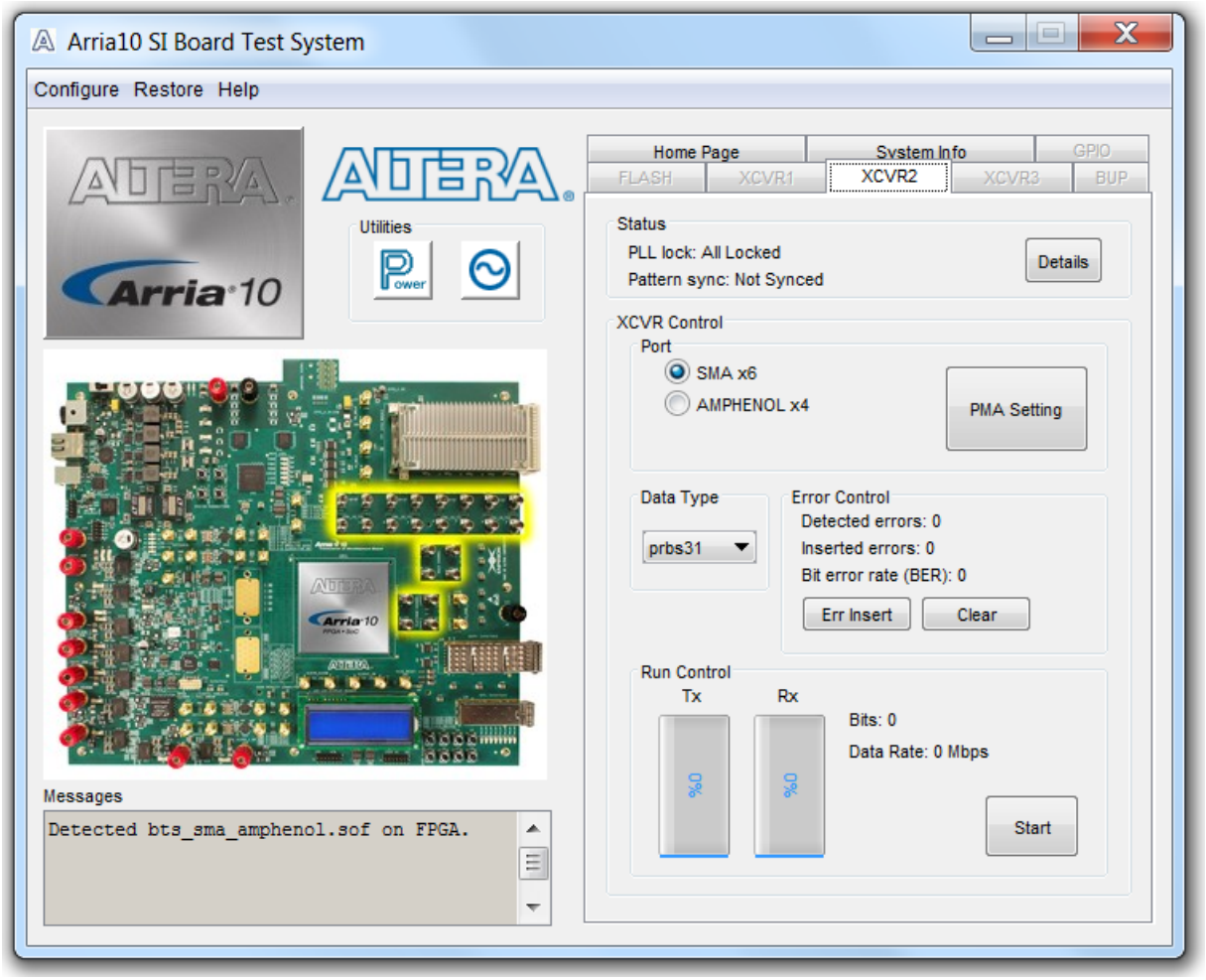
Related Information

- **Run Control** on page 6-15
- **Run Control** on page 6-17

The XCVR #2 Tab

The **XCVR #2** tab allows you to run a x4 backplane and x6 SMA (2.4 mm) loopback tests.

Figure 6-9: The XCVR #2 Tab



The following sections describe the controls on the XCVR #2 tab.

Status

The Status control displays the following status information during the loopback test.

Refer to the Status section of the XCVR #1 Tab for related information.

Related Information

Status on page 6-11

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

- Amphenol
- SMA

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface.

Refer to the PMA setting section of the XCVR #1 Tab for related information.

Related Information

PMA Setting on page 6-12

Data Type

The Data type control specifies the type of data contained in the transactions.

Refer to the Data Type section of the XCVR #1 Tab for related information.

Related Information

Data Type on page 6-13

Error Control

This control displays data errors detected during analysis and allows you to insert errors.

Refer to the Error Control section of the XCVR #1 Tab for related information.

Related Information

Error Control on page 6-13

Run Control

Refer to the Run Control section of the XCVR #1 Tab for related information.

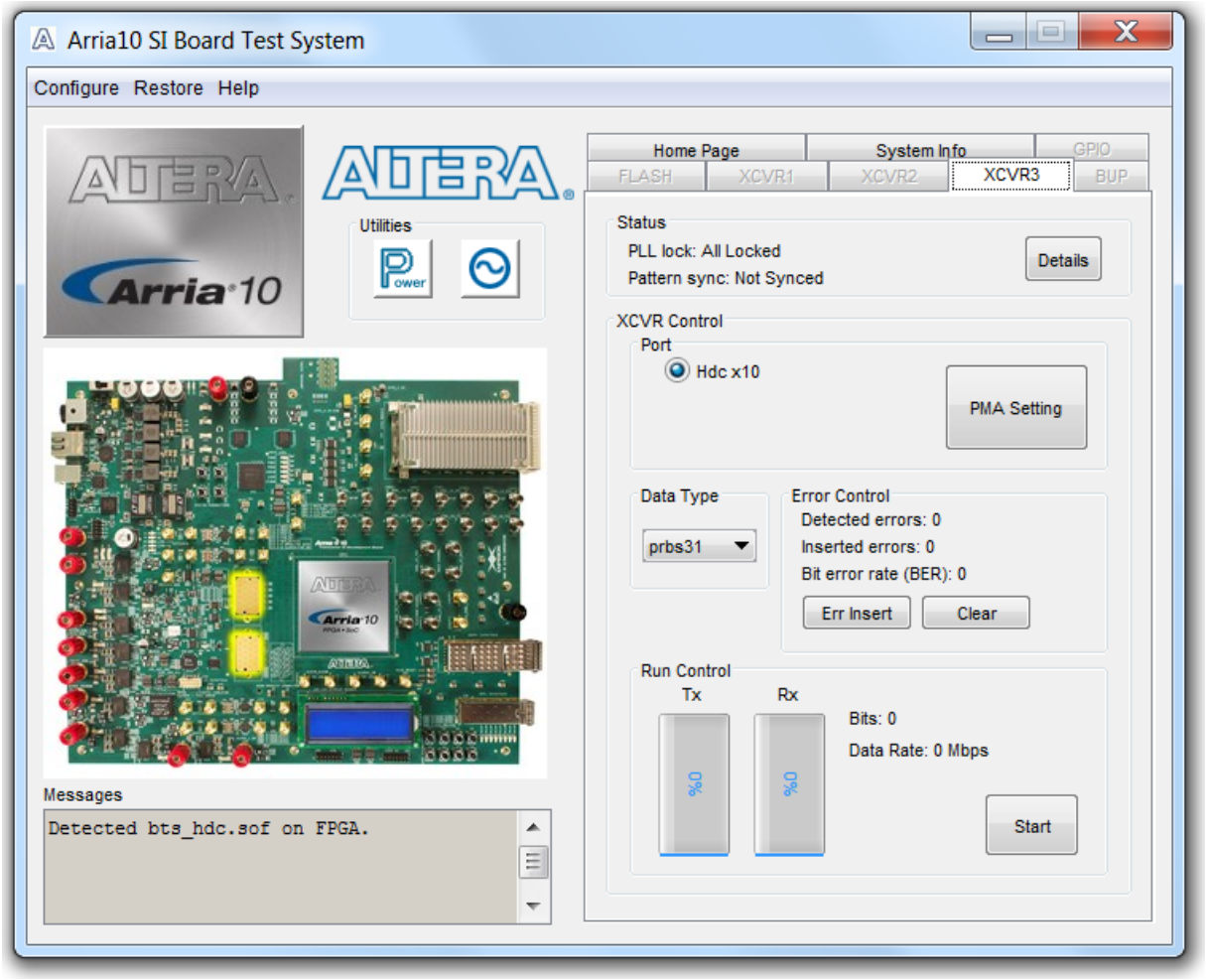
Related Information

Run Control on page 6-13

The XCVR #3 Tab

The **XCVR #3** tab allows you to run x10 high density loopback test through BullsEye connector.

Figure 6-10: The XCVR #3 Tab



The following sections describe the controls on the XCVR #3 tab.

Status

The Status control displays the following status information during the loopback test.

Refer to the Status section of the XCVR #1 Tab for related information.

Related Information

Status on page 6-11

Port

Use the following control to select the high density interface to apply PMA settings, data type and error control: High Density (BullsEye)

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface.

Refer to the PMA setting section of the XCVR #1 Tab for related information.

Related Information

PMA Setting on page 6-12

Data Type

The Data type control specifies the type of data contained in the transactions.

Refer to the Data Type section of the XCVR #1 Tab for related information.

Related Information

Data Type on page 6-13

Error Control

This control displays data errors detected during analysis and allows you to insert errors.

Refer to the Error Control section of the XCVR #1 Tab for related information.

Related Information

Error Control on page 6-13

Run Control

Refer to the Run Control section of the XCVR #1 Tab for related information.

Related Information

Run Control on page 6-13

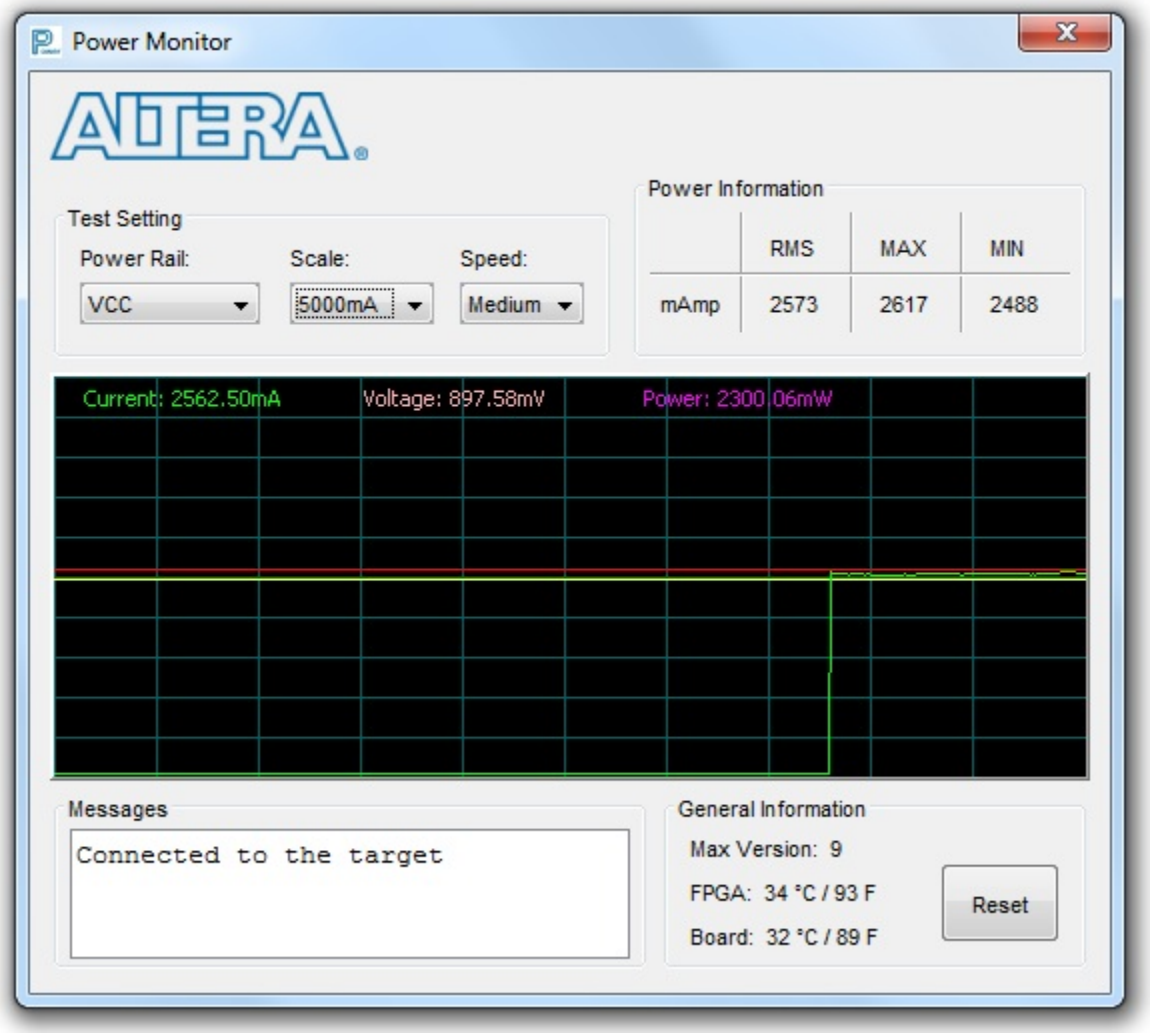
Power Monitoring

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the Board Test System application. You can also run the Power Monitor as a stand-alone application. The **PowerMonitor.exe** reside in the **<package dir>\examples\board_test_system** directory

Note: You cannot run the stand-alone power application and the BTS application at the same time. Also, you cannot run power and clock interface at the same time.

Figure 6-11: Power Monitor



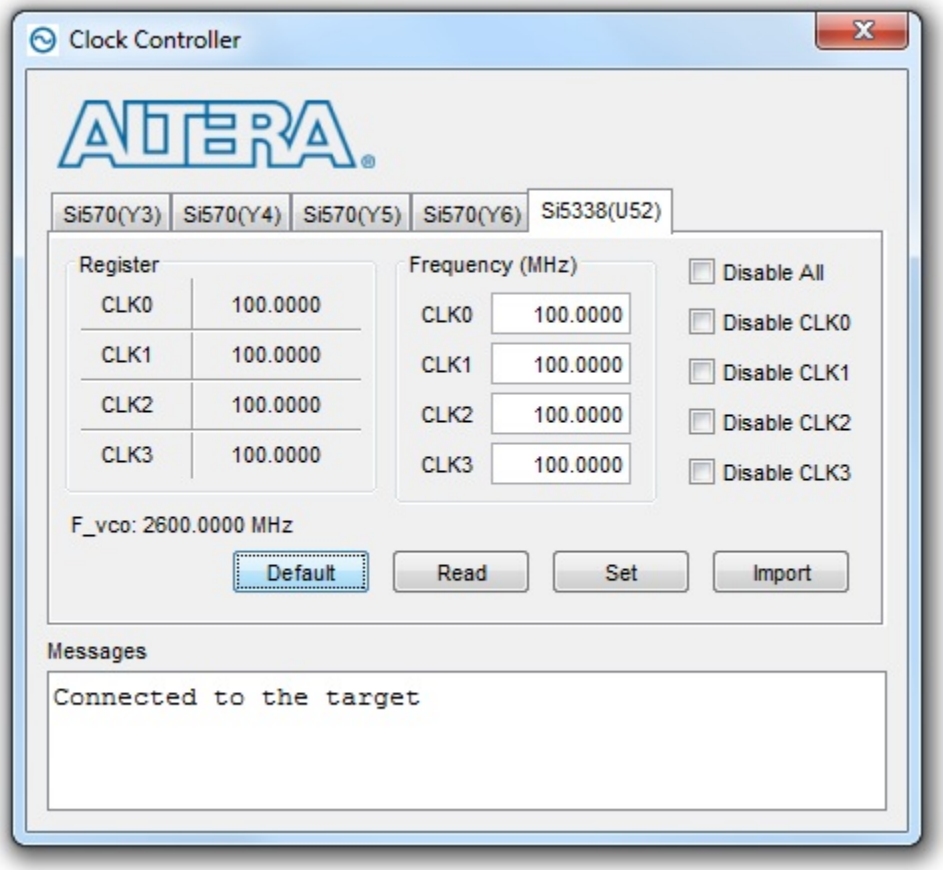
The Clock Control

The Clock Control application sets the Si570 programmable oscillators to any frequency between 10 MHz and 945 MHz and select frequencies to 1400 MHz. The oscillator drives a 2-to-6 buffer that drives a copy of the clock to all transceiver blocks of the FPGA.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the **<package dir>\examples\board_test_system** directory.

The Clock Control communicates with the MAX V device on the board through the JTAG bus. The Si570 programmable oscillator is connected to the MAX V device through a 2-wire serial bus.

Figure 6-12: The Clock Control



The following sections describe the Clock Control controls.

Serial Port Registers

The Serial port registers control shows the current values from the Si570 registers.

Note: For more information about the Si570 registers, refer to the Si570/Si571 data sheet available on the Silicon Labs website (**www.silabs.com**).

fXTAL

The fXTAL control shows the calculated internal fixed-frequency crystal, based on the serial port register values.

Note: For more information about the fXTAL value and how it is calculated, refer to the Si570/Si571 data sheet available on the Silicon Labs website (**www.silabs.com**).

Target Frequency

The Target frequency control allows you to specify the frequency of the clock. Legal values are between 10 and 945 MHz and select frequencies to 1400 MHz. For example, 421.31259873 is possible within 100 parts per million (ppm). The Target frequency control works in conjunction with the Set New Frequency control.

Reset Si570

The clear control sets the Si570 programmable oscillator to the default frequency as follows:

Y3 = 644.53125 MHz

Y4 = 706.25 MHz

Y5 = 625 MHz

Y6 = 875 MHz

Set New Frequency

The Set New Frequency control sets the Si570 programmable oscillator frequency to the value in the Target frequency control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time.

Note: Altera recommends resetting the FPGA logic after changing frequencies.

Additional Information 7

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This chapter provides the revision history about the document

Document Revision History

Table 7-1: Arria 10 GX Transceiver Signal Integrity Development Kit History

Version	Release Date	Description
Production Silicon	July 2016	Initial Release

Programming the Flash Memory Device

A

2016.07.14

UG-20005

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the pre-programmed contents of the common flash interface (CFI) flash memory device on the Arria 10 GX transceiver signal integrity development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Arria 10 GX transceiver signal integrity development board ships with the CFI flash device pre-programmed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus Prime software.

CFI Flash Memory Map

The table below shows the default memory contents of the two 1-Gb CFI flash devices. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A-1: Byte Address Flash Memory Map

Block Description	Size	Address
Board Test System	512 KB	0x09F4.0000 - 09FB.FFFF
User Software	14,336 KB	0x0914.0000 - 09F3.FFFF
Factory Software	8,192 KB	0x0894.0000 - 0913.FFFF
zipfs	8,192 KB	0x0814.0000 - 0893.FFFF
User Hardware 2	44,032 KB	0x0564.0000 - 0813.FFFF
User Hardware 1	44,032 KB	0x02B4.0000 - 0563.FFFF
Factory Hardware	44,032 KB	0x0004.0000 - 02B3.FFFF
PFL Option Bits	64 KB	0x0003.0000 - 0003.FFFF
Board Information	64 KB	0x0002.0000 - 0002.FFFF
Ethernet Option Bits	64 KB	0x0001.0000 - 0001.FFFF

Block Description	Size	Address
User Design Reset	64 KB	0x0000.0000 - 0000.FFFF

Attention: Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS *elf2flash* command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS nios2-flash-programmer utility to write the **.flash** files to the user software locations of the flash memory.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus Prime software, and software developed using the Nios II EDS, follow these instructions:

1. On the **Windows Start** menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:

   For Quartus II .sof files:

   ```
   sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x02b40000
   --pfl --optionbit=0x00030000 --programmingmode=PSr
   ```

   For Nios II .elf files:

   ```
   elf2flash --base=0x0 --end=0x0FFFFFFF --reset=0x09140000 --input=<yourfile>_sw.elf
   --output=<yourfile>_sw.flash
   --boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srecr
   ```

   The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to .flash format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.

   The Board Update Portal standard .flash format conventionally uses either one of these listed below:-

   - `<filename>_hw.flash` for hardware design files
   - `<filename>_sw.flash` for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "*Using the Board Update Portal to Update User Designs*" for more information.

Related Information

Using the Board Update Portal to Update User Designs on page 4-2
The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Programming Flash Memory Using the Nios II EDS

If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly.

To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Set the **SW3.2** to **OFF (1)** position to load the Board Update Portal design from flash memory on power up.
2. Attach the USB-Blaster cable and power up the board.
3. If the board has powered up and the LCD displays either "*Connecting...*" or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD, or if the **D24 (MAX_ERROR)** is **ON**, continue to step 4 to load the FPGA with a BUP design.
4. Launch the Quartus Prime Programmer to configure the FPGA with a **.sof** capable of flash programming.
5. Click **Add File** and select **<package dir>\factory_recovery\build_factory_source*\a10_si_bup.sof**
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%
8. On the **Windows Start** menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell.**
9. In the Nios II command shell, navigate to the **<package dir>\factory_recovery** directory (or to the directory of the **.flash** files you created in "**Creating Flash Files Using the Nios II EDS** on page 8-2" section and type the following Nios II EDS command:

   ```
   nios2-flash-programmer --base=0x0 <yourfile>_hw.flash r
   ```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

    ```
    nios2-flash-programmer --base=0x0 <yourfile>_sw.flash r
    ```

11. Set the **SW3.2** to **ON(0)** position and power cycle the board

    Programming the board is now complete. For more information about the *nios2-flash-programmer* utility, refer to the **Nios II Flash Programmer User Guide**.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the transceiver signal integrity development board. Make sure you have the Nios II EDS installed and perform the following instructions:

1. Set the board switches to the factory default settings described in "**Factory Default Switch Settings** on page 3-2".
2. Open GUI application **BoardTestSystem.exe**
   a. Launch Nios II command shell, change to directory ***\examples\board_test_system**and then type in **./BoardTestSystem.exe** to open the GUI.
   b. Change to directory ***\examples\board_test_system**, and then double click **BoardTestSystem(Pro).exe** to open the GUI.
3. Select **Restore > Factory Restore**.
4. Set the correct board information and then click **Restore**. Please note the restore process takes about 10 minutes.

   Attention: To ensure that you have the most up-to-date factory restore files and information about this product, refer to the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page on the Altera website.

Related Information

Factory Default Switch Settings on page 3-2

Restoring the MAX V CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX VCPLD on the Arria 10 GX transceiver signal integrity development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "**Factory Default Switch Settings** on page 3-2".
2. Launch the **Quartus Programmer**.
3. Click **Auto Detect**.
4. Click **Add File** and select

   <package dir>\factory_recovery\max5.pof.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

   Attention: To ensure that you have the most up-to-date factory restore files and information about this product, refer to the **Arria 10 GX Transceiver Signal Integrity Development Kit** web page on the Altera website.

Related Information

Factory Default Switch Settings on page 3-2

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