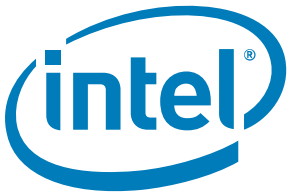
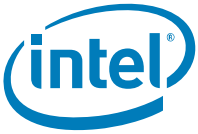


Intel® I/O Controller Hub 10 (ICH10) Family

Datasheet

October 2008

Document Number: 319973-003



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The Intel® I/O Controller Hub 10 (ICH10) Family chipset component may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

I^2C is a two-wire communications bus/protocol developed by Philips. SMBus is a subset of the I^2C bus/protocol and was developed by Intel. Implementations of the I^2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel® Active Management Technology requires the computer system to have an Intel® AMT-enabled chipset, network hardware and software, as well as connection with a power source and a corporate network connection. Setup requires configuration by the purchaser and may require scripting with the management console or further integration into existing security frameworks to enable certain functionality. It may also require modifications of implementation of new business processes. With regard to notebooks, Intel AMT may not be available or certain capabilities may be limited over a host OS-based VPN or when connecting wirelessly, on battery power, sleeping, hibernating or powered off. For more information, see www.intel.com/technology/platform-technology/intel-amt/

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain computer system software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

No computer system can provide absolute security under all conditions. Intel® Trusted Execution Technology (Intel® TXT) requires a computer system with Intel® Virtualization Technology, an Intel TXT-enabled processor, chipset, BIOS, Authenticated Code Modules and an Intel TXT-compatible measured launched environment (MLE). The MLE could consist of a virtual machine monitor, an OS or an application. In addition, Intel TXT requires the system to contain a TPM v1.2, as defined by the Trusted Computing Group and specific software for some uses. For more information, see http://www.intel.com/technology/security

Home networking capability and many Intel® Viiv™ technology-based usage models will require additional hardware devices, software or services. Functionality of Intel® Viiv™ technology verified devices will vary; check product details for desired features. System and component performance and functionality will vary depending on your specific hardware and software configurations. See www.intel.com/go/viiv_info for more information.

Intel® High Definition Audio requires a system with an appropriate Intel chipset and a motherboard with an appropriate codec and the necessary drivers installed. System sound quality will vary depending on actual implementation, controller, codec, drivers and speakers. For more information about Intel® HD audio, refer to http://www.intel.com/

Intel, Intel logo, Intel SpeedStep, Intel Viiv, and Intel vPro are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2008, Intel Corporation

Contents

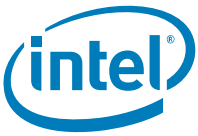
1 Introduction 33
1.1 About This Manual 33
1.2 Overview 37
1.2.1 Capability Overview 39
1.3 Intel® ICH10 Family High-Level Component Differences 44

2 Signal Description 45
2.1 Direct Media Interface (DMI) to Host Controller 47
2.2 PCI Express* Interface 48
2.3 LAN Connect Interface 48
2.4 Gigabit LAN Connect Interface 49
2.5 Firmware Hub Interface 50
2.6 PCI Interface 50
2.7 Serial ATA Interface 52
2.8 LPC Interface 55
2.9 Interrupt Interface 55
2.10 USB Interface 56
2.11 Power Management Interface 58
2.12 Processor Interface 61
2.13 SMBus Interface 62
2.14 System Management Interface 63
2.15 Real Time Clock Interface 64
2.16 Other Clocks 65
2.17 Miscellaneous Signals 65
2.18 Intel® High Definition Audio Link 66
2.19 Serial Peripheral Interface (SPI) 67
2.20 Controller Link 68
2.21 Intel® Quiet System Technology 68
2.22 JTAG Signals (Intel® ICH10 Corporate Family Only) 69
2.23 General Purpose I/O Signals 70
2.24 Power and Ground Signals 73
2.25 Pin Straps 75
2.25.1 Functional Straps 75
2.25.2 External RTC Circuitry 79

3 Intel® ICH10 Pin States 81
3.1 Integrated Pull-Ups and Pull-Downs 81
3.2 Output and I/O Signals Planes and States 83
3.3 Power Planes for Input Signals 88

4 Intel® ICH10 and System Clock Domains 91

5 Functional Description 93
5.1 DMI-to-PCI Bridge (D30:F0) 93
5.1.1 PCI Bus Interface 93
5.1.2 PCI Bridge As an Initiator 93
5.1.3 Parity Error Detection and Generation 95
5.1.4 PCIRST# 96
5.1.5 Peer Cycles 96
5.1.6 PCI-to-PCI Bridge Model 96
5.1.7 IDSEL to Device Number Mapping 97
5.1.8 Standard PCI Bus Configuration Mechanism 97
5.2 PCI Express* Root Ports (D28:F0,F1,F2,F3,F4,F5) 97
5.2.1 Interrupt Generation 97
5.2.2 Power Management 98
5.2.3 SERR# Generation 99
5.2.4 Hot-Plug 100
5.3 Gigabit Ethernet Controller (B0:D25:F0) 101
5.3.1 Gigabit Ethernet PCI Bus Interface 102
5.3.2 Error Events and Error Reporting 103
5.3.3 Ethernet Interface 103
5.3.4 PCI Power Management 104
5.3.5 Configurable LEDs 105



5.3.6 Function Level Reset Support (FLR) 106
5.4 LPC Bridge (w/ System and Management Functions) (D31:F0) 107
5.4.1 LPC Interface 107
5.5 DMA Operation (D31:F0) 112
5.5.1 Channel Priority 113
5.5.2 Address Compatibility Mode 113
5.5.3 Summary of DMA Transfer Sizes 114
5.5.4 Autoinitialize 114
5.5.5 Software Commands 115
5.6 LPC DMA 115
5.6.1 Asserting DMA Requests 115
5.6.2 Abandoning DMA Requests 116
5.6.3 General Flow of DMA Transfers 116
5.6.4 Terminal Count 116
5.6.5 Verify Mode 117
5.6.6 DMA Request Deassertion 117
5.6.7 SYNC Field / LDRQ# Rules 118
5.7 8254 Timers (D31:F0) 118
5.7.1 Timer Programming 119
5.7.2 Reading from the Interval Timer 120
5.8 8259 Interrupt Controllers (PIC) (D31:F0) 121
5.8.1 Interrupt Handling 122
5.8.2 Initialization Command Words (ICWx) 123
5.8.3 Operation Command Words (OCW) 124
5.8.4 Modes of Operation 124
5.8.5 Masking Interrupts 127
5.8.6 Steering PCI Interrupts 127
5.9 Advanced Programmable Interrupt Controller (APIC) (D31:F0) 128
5.9.1 Interrupt Handling 128
5.9.2 Interrupt Mapping 128
5.9.3 PCI / PCI Express* Message-Based Interrupts 129
5.9.4 Front Side Bus Interrupt Delivery 129
5.9.5 IOxAPIC Address Remapping 131
5.9.6 External Interrupt Controller Support 131
5.10 Serial Interrupt (D31:F0) 132
5.10.1 Start Frame 132
5.10.2 Data Frames 133
5.10.3 Stop Frame 133
5.10.4 Specific Interrupts Not Supported via SERIRQ 133
5.10.5 Data Frame Format 134
5.11 Real Time Clock (D31:F0) 135
5.11.1 Update Cycles 135
5.11.2 Interrupts 136
5.11.3 Lockable RAM Ranges 136
5.11.4 Century Rollover 136
5.11.5 Clearing Battery-Backed RTC RAM 136
5.12 Processor Interface (D31:F0) 138
5.12.1 Processor Interface Signals 138
5.12.2 Dual-Processor Issues 141
5.13 Power Management (D31:F0) 142
5.13.1 Features 142
5.13.2 Intel® ICH10 and System Power States 142
5.13.3 System Power Planes 145
5.13.4 SMI#/SCI Generation 145
5.13.5 Dynamic Processor Clock Control 148
5.13.6 Sleep States 151
5.13.7 Thermal Management 154
5.13.8 Event Input Signals and Their Usage 155
5.13.9 ALT Access Mode 158
5.13.10 System Power Supplies, Planes, and Signals 162
5.13.11 Clock Generators 164
5.13.12 Legacy Power Management Theory of Operation 165
5.13.13 Reset Behavior 165
5.14 System Management (D31:F0) 167
5.14.1 Theory of Operation 167
5.14.2 TCO Modes 169
5.15 General Purpose I/O (D31:F0) 173

5.15.1 Power Wells 173
5.15.2 SMI# and SCI Routing 173
5.15.3 Triggering 173
5.15.4 GPIO Registers Lockdown 173
5.15.5 Serial POST Codes Over GPIO 174
5.15.6 Intel Management Engine GPIOs 176
5.16 SATA Host Controller (D31:F2, F5) 176
5.16.1 SATA Feature Support 177
5.16.2 Theory of Operation 178
5.16.3 SATA Swap Bay Support 178
5.16.4 Hot Plug Operation 178
5.16.5 Function Level Reset Support (FLR) 179
5.16.6 Intel® Matrix Storage Technology Configuration 180
5.16.7 Power Management Operation 181
5.16.8 SATA Device Presence 183
5.16.9 SATA LED 184
5.16.10 AHCI Operation 184
5.16.11 Serial ATA Reference Clock Low Power Request (SATACLKREQ#) 184
5.16.12 SGPIO Signals 185
5.16.13 External SATA 189
5.17 High Precision Event Timers 189
5.17.1 Timer Accuracy 189
5.17.2 Interrupt Mapping 190
5.17.3 Periodic vs. Non-Periodic Modes 190
5.17.4 Enabling the Timers 191
5.17.5 Interrupt Levels 191
5.17.6 Handling Interrupts 192
5.17.7 Issues Related to 64-Bit Timers with 32-Bit Processors 192
5.18 USB UHCI Host Controllers (D29:F0, F1, F2, F3 and D26:F0, F1 and F2) 192
5.18.1 Data Structures in Main Memory 193
5.18.2 Data Transfers to/from Main Memory 193
5.18.3 Data Encoding and Bit Stuffing 193
5.18.4 Bus Protocol 193
5.18.5 Packet Formats 194
5.18.6 USB Interrupts 194
5.18.7 USB Power Management 197
5.18.8 USB Legacy Keyboard Operation 197
5.18.9 Function Level Reset Support (FLR) 200
5.19 USB EHCI Host Controllers (D29:F7 and D26:F7) 201
5.19.1 EHC Initialization 201
5.19.2 Data Structures in Main Memory 202
5.19.3 USB 2.0 Enhanced Host Controller DMA 202
5.19.4 Data Encoding and Bit Stuffing 202
5.19.5 Packet Formats 203
5.19.6 USB 2.0 Interrupts and Error Conditions 203
5.19.7 USB 2.0 Power Management 204
5.19.8 Interaction with UHCI Host Controllers 205
5.19.9 USB 2.0 Legacy Keyboard Operation 208
5.19.10 USB 2.0 Based Debug Port 209
5.19.11 USB Pre-Fetch Based Pause 213
5.19.12 Function Level Reset Support (FLR) 214
5.20 SMBus Controller (D31:F3) 214
5.20.1 Host Controller 215
5.20.2 Bus Arbitration 219
5.20.3 Bus Timing 220
5.20.4 Interrupts / SMI# 221
5.20.5 SMBALERT# 222
5.20.6 SMBus CRC Generation and Checking 222
5.20.7 SMBus Slave Interface 222
5.21 Intel® High Definition Audio Overview 228
5.22 Intel® Active Management Technology (Intel® AMT) (Corporate Only) 228
5.22.1 Intel® AMT Features 229
5.22.2 Intel® AMT Requirements 229
5.23 Serial Peripheral Interface (SPI) 229
5.23.1 SPI Supported Feature Overview 230
5.23.2 Flash Descriptor 232
5.23.3 Flash Access 234

5.23.4 Serial Flash Device Compatibility Requirements 235
5.23.5 Multiple Page Write Usage Model 237
5.23.6 Flash Device Configurations 238
5.23.7 SPI Flash Device Recommended Pinout 238
5.23.8 Serial Flash Device Package 239
5.24 Intel® Quiet System Technology (Intel® QST) 240
5.24.1 PWM Outputs 240
5.24.2 TACH Inputs 240
5.25 Thermal Sensors 240
5.26 Feature Capability Mechanism 241
5.27 Integrated Trusted Platform Module (Corporate Only) 241
5.27.1 Integrated TPM Hardware Requirements 241
5.27.2 Enabling integrated TPM 242

6 Ballout Definition 243
6.1 Intel® ICH10 Ballout 243

7 Package Information 253
7.1 Intel® ICH10 Package 253

8 Electrical Characteristics 255
8.1 Thermal Specifications 255
8.2 Absolute Maximum Ratings 255
8.3 DC Characteristics 255
8.4 AC Characteristics 268
8.5 Timing Diagrams 280

9 Register and Memory Mapping 293
9.1 PCI Devices and Functions 294
9.2 PCI Configuration Map 295
9.3 I/O Map 295
9.3.1 Fixed I/O Address Ranges 295
9.3.2 Variable I/O Decode Ranges 298
9.4 Memory Map 299
9.4.1 Boot-Block Update Scheme 300

10 Chipset Configuration Registers 303
10.1 Chipset Configuration Registers (Memory Space) 303
10.1.1 VCH—Virtual Channel Capability Header Register 306
10.1.2 VCAP1—Virtual Channel Capability #1 Register 306
10.1.3 VCAP2—Virtual Channel Capability #2 Register 307
10.1.4 PVC—Port Virtual Channel Control Register 307
10.1.5 PVS—Port Virtual Channel Status Register 307
10.1.6 V0CAP—Virtual Channel 0 Resource Capability Register 308
10.1.7 V0CTL—Virtual Channel 0 Resource Control Register 308
10.1.8 V0STS—Virtual Channel 0 Resource Status Register 309
10.1.9 V1CAP—Virtual Channel 1 Resource Capability Register 309
10.1.10 V1CTL—Virtual Channel 1 Resource Control Register 310
10.1.11 V1STS—Virtual Channel 1 Resource Status Register 310
10.1.12 PAT—Port Arbitration Table (Consumer Only) 311
10.1.13 CIR1—Chipset Initialization Register 1 311
10.1.14 REC—Root Error Command Register 311
10.1.15 RCTCL—Root Complex Topology Capabilities List Register 312
10.1.16 ESD—Element Self Description Register 312
10.1.17 ULD—Upstream Link Descriptor Register 312
10.1.18 ULBA—Upstream Link Base Address Register 313
10.1.19 RP1D—Root Port 1 Descriptor Register 313
10.1.20 RP1BA—Root Port 1 Base Address Register 313
10.1.21 RP2D—Root Port 2 Descriptor Register 314
10.1.22 RP2BA—Root Port 2 Base Address Register 314
10.1.23 RP3D—Root Port 3 Descriptor Register 314
10.1.24 RP3BA—Root Port 3 Base Address Register 315
10.1.25 RP4D—Root Port 4 Descriptor Register 315
10.1.26 RP4BA—Root Port 4 Base Address Register 315
10.1.27 HDD—Intel® High Definition Audio Descriptor Register 316
10.1.28 HDBA—Intel® High Definition Audio Base Address Register 316
10.1.29 RP5D—Root Port 5 Descriptor Register 316
10.1.30 RP5BA—Root Port 5 Base Address Register 317

10.1.31 RP6D—Root Port 6 Descriptor Register 317
10.1.32 RP6BA—Root Port 6 Base Address Register 317
10.1.33 ILCL—Internal Link Capabilities List Register 318
10.1.34 LCAP—Link Capabilities Register 318
10.1.35 LCTL—Link Control Register 318
10.1.36 LSTS—Link Status Register 319
10.1.37 CIR2 — Chipset Initialization Register 2 319
10.1.38 CIR3 — Chipset Initialization Register 3 319
10.1.39 BCR — Backbone Configuration Register 319
10.1.40 RPC—Root Port Configuration Register 320
10.1.41 DMIC—DMI Control Register 321
10.1.42 RPFN—Root Port Function Number and Hide for PCI Express* Root Ports 321
10.1.43 FLRSTAT—FLR Pending Status Register 323
10.1.44 CIR13—Chipset Initialization Register 13 324
10.1.45 CIR5—Chipset Initialization Register 5 324
10.1.46 TRSR—Trap Status Register 324
10.1.47 TRCR—Trapped Cycle Register 325
10.1.48 TWDR—Trapped Write Data Register 325
10.1.49 IOTRn — I/O Trap Register (0-3) 326
10.1.50 DMC—DMI Miscellaneous Control Register 327
10.1.51 CIR6—Chipset Initialization Register 6 327
10.1.52 CIR7—Chipset Initialization Register 7 327
10.1.53 TCTL—TCO Configuration Register 328
10.1.54 D31IP—Device 31 Interrupt Pin Register 329
10.1.55 D30IP—Device 30 Interrupt Pin Register 330
10.1.56 D29IP—Device 29 Interrupt Pin Register 330
10.1.57 D28IP—Device 28 Interrupt Pin Register 331
10.1.58 D27IP—Device 27 Interrupt Pin Register 332
10.1.59 D26IP—Device 26 Interrupt Pin Register 333
10.1.60 D25IP—Device 25 Interrupt Pin Register 334
10.1.61 D31IR—Device 31 Interrupt Route Register 334
10.1.62 D30IR—Device 30 Interrupt Route Register 335
10.1.63 D29IR—Device 29 Interrupt Route Register 336
10.1.64 D28IR—Device 28 Interrupt Route Register 337
10.1.65 D27IR—Device 27 Interrupt Route Register 338
10.1.66 D26IR—Device 26 Interrupt Route Register 339
10.1.67 D25IR—Device 25 Interrupt Route Register 340
10.1.68 OIC—Other Interrupt Control Register (Corporate Only) 341
10.1.69 OIC—Other Interrupt Control Register (Consumer Only) 341
10.1.70 SBEMC3—Scheduled Break Event C3 Exit Latency 342
10.1.71 SBEMC4—Scheduled Break Event C4 Exit Latency 342
10.1.72 PRSTS—Power and Reset Status (Corporate Only) 343
10.1.73 RC—RTC Configuration Register 344
10.1.74 HPTC—High Precision Timer Configuration Register 344
10.1.75 GCS—General Control and Status Register 345
10.1.76 BUC—Backed Up Control Register 347
10.1.77 FD—Function Disable Register 348
10.1.78 CG—Clock Gating 350
10.1.79 FDSW—Function Disable SUS Well 352
10.1.80 CIR8—Chipset Initialization Register 8 352
10.1.81 CIR9—Chipset Initialization Register 9 352
10.1.82 PPO—Port Power Off 352
10.1.83 CIR10—Chipset Initialization Register 10 353
10.1.84 MAP—Remap Control Register 353

11 PCI-to-PCI Bridge Registers (D30:F0) 355

11.1 PCI Configuration Registers (D30:F0) 355
11.1.1 VID— Vendor Identification Register (PCI-PCI—D30:F0) 356
11.1.2 DID— Device Identification Register (PCI-PCI—D30:F0) 356
11.1.3 PCICMD—PCI Command (PCI-PCI—D30:F0) 357
11.1.4 PSTS—PCI Status Register (PCI-PCI—D30:F0) 357
11.1.5 RID—Revision Identification Register (PCI-PCI—D30:F0) 359
11.1.6 CC—Class Code Register (PCI-PCI—D30:F0) 359
11.1.7 PMLT—Primary Master Latency Timer Register (PCI-PCI—D30:F0) 360
11.1.8 HEADTYP—Header Type Register (PCI-PCI—D30:F0) 360
11.1.9 BNUM—Bus Number Register (PCI-PCI—D30:F0) 360

11.1.10 SMLT—Secondary Master Latency Timer Register (PCI-PCI—D30:F0) 361
11.1.11 IOBASE_LIMIT—I/O Base and Limit Register (PCI-PCI—D30:F0) 361
11.1.12 SECSTS—Secondary Status Register (PCI-PCI—D30:F0) 362
11.1.13 MEMBASE_LIMIT—Memory Base and Limit Register (PCI-PCI—D30:F0) 363
11.1.14 PREF_MEM_BASE_LIMIT—Prefetchable Memory Base and Limit Register (PCI-PCI—D30:F0) 363
11.1.15 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI-PCI—D30:F0) 364
11.1.16 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI-PCI—D30:F0) 364
11.1.17 CAPP—Capability List Pointer Register (PCI-PCI—D30:F0) 364
11.1.18 INTR—Interrupt Information Register (PCI-PCI—D30:F0) 364
11.1.19 BCTRL—Bridge Control Register (PCI-PCI—D30:F0) 365
11.1.20 SPDH—Secondary PCI Device Hiding Register (PCI-PCI—D30:F0) 366
11.1.21 DTC—Delayed Transaction Control Register (PCI-PCI—D30:F0) 367
11.1.22 BPS—Bridge Proprietary Status Register (PCI-PCI—D30:F0) 368
11.1.23 BPC—Bridge Policy Configuration Register (PCI-PCI—D30:F0) 369
11.1.24 SVCAP—Subsystem Vendor Capability Register (PCI-PCI—D30:F0) 370
11.1.25 SVID—Subsystem Vendor IDs Register (PCI-PCI—D30:F0) 370

12 Gigabit LAN Configuration Registers 371
12.1 Gigabit LAN Configuration Registers (Gigabit LAN — D25:F0) 371
12.1.1 VID—Vendor Identification Register (Gigabit LAN—D25:F0) 372
12.1.2 DID—Device Identification Register (Gigabit LAN—D25:F0) 372
12.1.3 PCICMD—PCI Command Register (Gigabit LAN—D25:F0) 373
12.1.4 PCISTS—PCI Status Register (Gigabit LAN—D25:F0) 374
12.1.5 RID—Revision Identification Register (Gigabit LAN—D25:F0) 375
12.1.6 CC—Class Code Register (Gigabit LAN—D25:F0) 375
12.1.7 CLS—Cache Line Size Register (Gigabit LAN—D25:F0) 375
12.1.8 PLT—Primary Latency Timer Register (Gigabit LAN—D25:F0) 375
12.1.9 HT—Header Type Register (Gigabit LAN—D25:F0) 375
12.1.10 MBARA—Memory Base Address Register A (Gigabit LAN—D25:F0) 376
12.1.11 MBARB—Memory Base Address Register B (Gigabit LAN—D25:F0) 376
12.1.12 MBARC—Memory Base Address Register C (Gigabit LAN—D25:F0) 377
12.1.13 SVID—Subsystem Vendor ID Register (Gigabit LAN—D25:F0) 377
12.1.14 SID—Subsystem ID Register (Gigabit LAN—D25:F0) 377
12.1.15 ERBA—Expansion ROM Base Address Register (Gigabit LAN—D25:F0) 377
12.1.16 CAPP—Capabilities List Pointer Register (Gigabit LAN—D25:F0) 378
12.1.17 INTR—Interrupt Information Register (Gigabit LAN—D25:F0) 378
12.1.18 MLMG—Maximum Latency/Minimum Grant Register (Gigabit LAN—D25:F0) 378

12.1.19 CLIST 1—Capabilities List Register 1 (Gigabit LAN—D25:F0) 378
12.1.20 PMC—PCI Power Management Capabilities Register (Gigabit LAN—D25:F0) 379
12.1.21 PMCS—PCI Power Management Control and Status Register (Gigabit LAN—D25:F0) 380
12.1.22 DR—Data Register (Gigabit LAN—D25:F0) 381
12.1.23 CLIST 2—Capabilities List Register 2 (Gigabit LAN—D25:F0) 381
12.1.24 MCTL—Message Control Register (Gigabit LAN—D25:F0) 381
12.1.25 MADDL—Message Address Low Register (Gigabit LAN—D25:F0) 382
12.1.26 MADDH—Message Address High Register (Gigabit LAN—D25:F0) 382
12.1.27 MDAT—Message Data Register (Gigabit LAN—D25:F0) 382
12.1.28 FLRCAP—Function Level Reset Capability (Gigabit LAN—D25:F0) 382
12.1.29 FLRCLV—Function Level Reset Capability Length and Version (Gigabit LAN—D25:F0) 383
12.1.30 DEVCTRL—Device Control (Gigabit LAN—D25:F0) 383
12.2 MBARA—Gigabit LAN Base Address A Registers 384
12.2.1 LDR4—LAN Device Initialization Register 4 (Gigabit LAN Memory Mapped Base Address Register) 384
12.2.2 LDR3—LAN Device Initialization Register 3 (Gigabit LAN Memory Mapped Base Address Register) 384
12.2.3 LDCR2—LAN Device Control Register 2 (Gigabit LAN Memory Mapped Base Address Register) 385
12.2.4 LDCR4—LAN Device Control Register 4 (Gigabit LAN Memory Mapped Base Address Register) 385
12.2.5 LDR5—LAN Device Control Register 5 (Gigabit LAN Memory Mapped Base Address Register) 385
12.2.6 LDR1—LAN Device Initialization Register 1 (Gigabit LAN Memory Mapped Base Address Register) 385

13 LPC Interface Bridge Registers (D31:F0) 387
13.1 PCI Configuration Registers (LPC I/F—D31:F0) 387
13.1.1 VID—Vendor Identification Register (LPC I/F—D31:F0) 389
13.1.2 DID—Device Identification Register (LPC I/F—D31:F0) 389
13.1.3 PCICMD—PCI COMMAND Register (LPC I/F—D31:F0) 389
13.1.4 PCISTS—PCI Status Register (LPC I/F—D31:F0) 390
13.1.5 RID—Revision Identification Register (LPC I/F—D31:F0) 391
13.1.6 PI—Programming Interface Register (LPC I/F—D31:F0) 391
13.1.7 SCC—Sub Class Code Register (LPC I/F—D31:F0) 391
13.1.8 BCC—Base Class Code Register (LPC I/F—D31:F0) 391
13.1.9 PLT—Primary Latency Timer Register (LPC I/F—D31:F0) 391
13.1.10 HEADTYP—Header Type Register (LPC I/F—D31:F0) 392
13.1.11 SS—Sub System Identifiers Register (LPC I/F—D31:F0) 392
13.1.12 PMBASE—ACPI Base Address Register (LPC I/F—D31:F0) 392
13.1.13 ACPI_CNTL—ACPI Control Register (LPC I/F — D31:F0) 393
13.1.14 GPIOBASE—GPIO Base Address Register (LPC I/F — D31:F0) 393
13.1.15 GC—GPIO Control Register (LPC I/F — D31:F0) 394
13.1.16 PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0) 395
13.1.17 SIRQ_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0) 396
13.1.18 PIRQ[n]_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0) 397
13.1.19 LPC_IBDF—IOxAPIC Bus:Device:Function (LPC I/F—D31:F0) 398
13.1.20 LPC_HnBDF – HPET n Bus:Device:Function (LPC I/F—D31:F0) 398
13.1.21 LPC_I/O_DEC—I/O Decode Ranges Register (LPC I/F—D31:F0) 399
13.1.22 LPC_EN—LPC I/F Enables Register (LPC I/F—D31:F0) 400
13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0) 401
13.1.24 GEN2_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0) 401

13.1.25 GEN3_DEC—LPC I/F Generic Decode Range 3 Register (LPC I/F—D31:F0) 402
13.1.26 GEN4_DEC—LPC I/F Generic Decode Range 4 Register (LPC I/F—D31:F0) 403
13.1.27 LGMR — LPC I/F Generic Memory Range (LPC I/F—D31:F0) (Corporate Only) 403
13.1.28 FWH_SEL1—Firmware Hub Select 1 Register (LPC I/F—D31:F0) 404
13.1.29 FWH_SEL2—Firmware Hub Select 2 Register (LPC I/F—D31:F0) 405
13.1.30 FWH_DEC_EN1—Firmware Hub Decode Enable Register (LPC I/F—D31:F0) 406
13.1.31 BIOS_CNTL—BIOS Control Register (LPC I/F—D31:F0) 408
13.1.32 FDCAP—Feature Detection Capability ID (LPC I/F—D31:F0) 409
13.1.33 FDLEN—Feature Detection Capability Length (LPC I/F—D31:F0) 409
13.1.34 FDVER—Feature Detection Version (LPC I/F—D31:F0) 409
13.1.35 FDVCT—Feature Vector (LPC I/F—D31:F0) 410
13.1.36 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0) 410
13.2 DMA I/O Registers (LPC I/F—D31:F0) 411
13.2.1 DMABASE_CA—DMA Base and Current Address Registers (LPC I/F—D31:F0) 412
13.2.2 DMABASE_CC—DMA Base and Current Count Registers (LPC I/F—D31:F0) 413
13.2.3 DMAMEM_LP—DMA Memory Low Page Registers (LPC I/F—D31:F0) 413
13.2.4 DMACMD—DMA Command Register (LPC I/F—D31:F0) 414
13.2.5 DMASTA—DMA Status Register (LPC I/F—D31:F0) 414
13.2.6 DMA_WRSMSK—DMA Write Single Mask Register (LPC I/F—D31:F0) 415
13.2.7 DMACH_MODE—DMA Channel Mode Register (LPC I/F—D31:F0) 416
13.2.8 DMA Clear Byte Pointer Register (LPC I/F—D31:F0) 417
13.2.9 DMA Master Clear Register (LPC I/F—D31:F0) 417
13.2.10 DMA_CLMSK—DMA Clear Mask Register (LPC I/F—D31:F0) 417
13.2.11 DMA_WRMSK—DMA Write All Mask Register (LPC I/F—D31:F0) 418
13.3 Timer I/O Registers (LPC I/F—D31:F0) 419
13.3.1 TCW—Timer Control Word Register (LPC I/F—D31:F0) 420
13.3.2 SBYTE_FMT—Interval Timer Status Byte Format Register (LPC I/F—D31:F0) 422
13.3.3 Counter Access Ports Register (LPC I/F—D31:F0) 423
13.4 8259 Interrupt Controller (PIC) Registers (LPC I/F—D31:F0) 424
13.4.1 Interrupt Controller I/O MAP (LPC I/F—D31:F0) 424
13.4.2 ICW1—Initialization Command Word 1 Register (LPC I/F—D31:F0) 425
13.4.3 ICW2—Initialization Command Word 2 Register (LPC I/F—D31:F0) 426
13.4.4 ICW3—Master Controller Initialization Command Word 3 Register (LPC I/F—D31:F0) 427
13.4.5 ICW3—Slave Controller Initialization Command Word 3 Register (LPC I/F—D31:F0) 427
13.4.6 ICW4—Initialization Command Word 4 Register (LPC I/F—D31:F0) 428
13.4.7 OCW1—Operational Control Word 1 (Interrupt Mask) Register (LPC I/F—D31:F0) 428
13.4.8 OCW2—Operational Control Word 2 Register (LPC I/F—D31:F0) 429
13.4.9 OCW3—Operational Control Word 3 Register (LPC I/F—D31:F0) 430
13.4.10 ELCR1—Master Controller Edge/Level Triggered Register (LPC I/F—D31:F0) 431
13.4.11 ELCR2—Slave Controller Edge/Level Triggered Register (LPC I/F—D31:F0) 432
13.5 Advanced Programmable Interrupt Controller (APIC)(D31:F0) 433
13.5.1 APIC Register Map (LPC I/F—D31:F0) 433
13.5.2 IND—Index Register (LPC I/F—D31:F0) 434
13.5.3 DAT—Data Register (LPC I/F—D31:F0) 434
13.5.4 EOIR—EOI Register (LPC I/F—D31:F0) 435

13.5.5 ID—Identification Register (LPC I/F—D31:F0) 436
13.5.6 VER—Version Register (LPC I/F—D31:F0) 436
13.5.7 REDIR_TBL—Redirection Table (LPC I/F—D31:F0) 437
13.6 Real Time Clock Registers 439
13.6.1 I/O Register Address Map 439
13.6.2 Indexed Registers 440
13.7 Processor Interface Registers (LPC I/F—D31:F0) 444
13.7.1 NMI_SC—NMI Status and Control Register (LPC I/F—D31:F0) 444
13.7.2 NMI_EN—NMI Enable (and Real Time Clock Index) Register (LPC I/F—D31:F0) 445
13.7.3 PORT92—Fast A20 and Init Register (LPC I/F—D31:F0) 445
13.7.4 COPROC_ERR—Coprocessor Error Register (LPC I/F—D31:F0) 446
13.7.5 RST_CNT—Reset Control Register (LPC I/F—D31:F0) 446
13.8 Power Management Registers (PM—D31:F0) 447
13.8.1 Power Management PCI Configuration Registers (PM—D31:F0) 447
13.8.2 APM I/O Decode 460
13.8.3 Power Management I/O Registers 461
13.9 System Management TCO Registers (D31:F0) 483
13.9.1 TCO_RLD—TCO Timer Reload and Current Value Register 483
13.9.2 TCO_DAT_IN—TCO Data In Register 484
13.9.3 TCO_DAT_OUT—TCO Data Out Register 484
13.9.4 TCO1_STS—TCO1 Status Register 484
13.9.5 TCO2_STS—TCO2 Status Register 486
13.9.6 TCO1_CNT—TCO1 Control Register 488
13.9.7 TCO2_CNT—TCO2 Control Register 489
13.9.8 TCO_MESSAGE1 and TCO_MESSAGE2 Registers 489
13.9.9 TCO_WDCNT—TCO Watchdog Control Register 490
13.9.10 SW_IRQ_GEN—Software IRQ Generation Register 490
13.9.11 TCO_TMR—TCO Timer Initial Value Register 490
13.10 General Purpose I/O Registers (D31:F0) 491
13.10.1 GPIO_USE_SEL—GPIO Use Select Register 492
13.10.2 GP_IO_SEL—GPIO Input/Output Select Register 492
13.10.3 GP_LVL—GPIO Level for Input or Output Register 493
13.10.4 GPO_BLINK—GPO Blink Enable Register 493
13.10.5 GP_SER_BLINK—GP Serial Blink 494
13.10.6 GP_SB_CMDSTS—GP Serial Blink Command Status 495
13.10.7 GP_SB_DATA—GP Serial Blink Data 495
13.10.8 GPI_INV—GPIO Signal Invert Register 496
13.10.9 GPIO_USE_SEL2—GPIO Use Select 2 Register 497
13.10.10 GP_IO_SEL2—GPIO Input/Output Select 2 Register 498
13.10.11 GP_LVL2—GPIO Level for Input or Output 2 Register 498
13.10.12 GPIO_USE_SEL3—GPIO Use Select 3 Register (Corporate Only) 499
13.10.13 GP_IO_SEL3—GPIO Input/Output Select 3 Register (Corporate Only) 499
13.10.14 GP_LVL3—GPIO Level for Input or Output 3 Register (Corporate Only) 500
13.10.15 GP_RST_SEL — GPIO Reset Select 500

14 SATA Controller Registers (D31:F2) 501
14.1 PCI Configuration Registers (SATA–D31:F2) 501
14.1.1 VID—Vendor Identification Register (SATA—D31:F2) 503
14.1.2 DID—Device Identification Register (SATA—D31:F2) 503
14.1.3 PCICMD—PCI Command Register (SATA–D31:F2) 503
14.1.4 PCISTS — PCI Status Register (SATA–D31:F2) 504
14.1.5 RID—Revision Identification Register (SATA—D31:F2) 505
14.1.6 PI—Programming Interface Register (SATA–D31:F2) 505
14.1.7 SCC—Sub Class Code Register (SATA–D31:F2) 506
14.1.8 BCC—Base Class Code Register (SATA–D31:F2) 506
14.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F2) 507
14.1.10 HTYPE—Header Type (SATA–D31:F2) 507
14.1.11 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F2) 507
14.1.12 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F2) 508
14.1.13 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1) 508

14.1.14 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1) 508
14.1.15 BAR — Legacy Bus Master Base Address Register (SATA–D31:F2) 509
14.1.16 ABAR/SIDPBA1 — AHCI Base Address Register/Serial ATA Index Data Pair Base Address (SATA–D31:F2) 509
14.1.17 SVID—Subsystem Vendor Identification Register (SATA–D31:F2) 510
14.1.18 SID—Subsystem Identification Register (SATA–D31:F2) 510
14.1.19 CAP—Capabilities Pointer Register (SATA–D31:F2) 510
14.1.20 INT_LN—Interrupt Line Register (SATA–D31:F2) 511
14.1.21 INT_PN—Interrupt Pin Register (SATA–D31:F2) 511
14.1.22 IDE_TIM — IDE Timing Register (SATA–D31:F2) 511
14.1.23 PID—PCI Power Management Capability Identification Register (SATA–D31:F2) 511
14.1.24 PC—PCI Power Management Capabilities Register (SATA–D31:F2) 512
14.1.25 PMCS—PCI Power Management Control and Status Register (SATA–D31:F2) 512
14.1.26 MSICI—Message Signaled Interrupt Capability Identification (SATA–D31:F2) 513
14.1.27 MSIMC—Message Signaled Interrupt Message Control (SATA–D31:F2) 514
14.1.28 MSIMA— Message Signaled Interrupt Message Address (SATA–D31:F2) 515
14.1.29 MSIMD—Message Signaled Interrupt Message Data (SATA–D31:F2) 515
14.1.30 MAP—Address Map Register (SATA–D31:F2) 516
14.1.31 PCS—Port Control and Status Register (SATA–D31:F2) 516
14.1.32 SCLKCG—SATA Clock Gating Control Register 519
14.1.33 SCLKGC—SATA Clock General Configuration Register 520
14.1.34 FLRCID—FLR Capability ID (SATA–D31:F2) 522
14.1.35 FLRCLV—FLR Capability Length and Version (SATA–D31:F2) 522
14.1.36 FLRC—FLR Control (SATA–D31:F2) 523
14.1.37 ATC—APM Trapping Control Register (SATA–D31:F2) 523
14.1.38 ATS—APM Trapping Status Register (SATA–D31:F2) 524
14.1.39 SP Scratch Pad Register (SATA–D31:F2) 524
14.1.40 BFCS—BIST FIS Control/Status Register (SATA–D31:F2) 525
14.1.41 BFTD1—BIST FIS Transmit Data1 Register (SATA–D31:F2) 527
14.1.42 BFTD2—BIST FIS Transmit Data2 Register (SATA–D31:F2) 527
14.2 Bus Master IDE I/O Registers (D31:F2) 528
14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2) 529
14.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F2) 530
14.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F2) 531
14.2.4 AIR—AHCI Index Register (D31:F2) 531
14.2.5 AIDR—AHCI Index Data Register (D31:F2) 531
14.3 Serial ATA Index/Data Pair Superset Registers 532
14.3.1 SINDX – Serial ATA Index (D31:F2) 532
14.3.2 SDATA – Serial ATA Data (D31:F2) 532
14.4 AHCI Registers (D31:F2) 536
14.4.1 AHCI Generic Host Control Registers (D31:F2) 537
14.4.2 Vendor Specific Registers (D31:F2) 545
14.4.3 Port Registers (D31:F2) 545

15 SATA Controller Registers (D31:F5) 563
15.1 PCI Configuration Registers (SATA–D31:F5) 563
15.1.1 VID—Vendor Identification Register (SATA—D31:F5) 564
15.1.2 DID—Device Identification Register (SATA—D31:F5) 565
15.1.3 PCICMD—PCI Command Register (SATA–D31:F5) 565
15.1.4 PCISTS — PCI Status Register (SATA–D31:F5) 566
15.1.5 RID—Revision Identification Register (SATA—D31:F5) 566
15.1.6 PI—Programming Interface Register (SATA–D31:F5) 567
15.1.7 SCC—Sub Class Code Register (SATA–D31:F5) 567
15.1.8 BCC—Base Class Code Register (SATA–D31:F5) 567
15.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F5) 568
15.1.10 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F5) 568

15.1.11 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F5) 568
15.1.12 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1) 569
15.1.13 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1) 569
15.1.14 BAR — Legacy Bus Master Base Address Register (SATA–D31:F5) 570
15.1.15 SIDPBA — SATA Index/Data Pair Base Address Register (SATA–D31:F5) 570
15.1.16 SVID—Subsystem Vendor Identification Register (SATA–D31:F5) 571
15.1.17 SID—Subsystem Identification Register (SATA–D31:F5) 571
15.1.18 CAP—Capabilities Pointer Register (SATA–D31:F5) 571
15.1.19 INT_LN—Interrupt Line Register (SATA–D31:F5) 571
15.1.20 INT_PN—Interrupt Pin Register (SATA–D31:F5) 571
15.1.21 IDE_TIM — IDE Timing Register (SATA–D31:F5) 572
15.1.22 PID—PCI Power Management Capability Identification Register (SATA–D31:F5) 572
15.1.23 PC—PCI Power Management Capabilities Register (SATA–D31:F5) 572
15.1.24 PMCS—PCI Power Management Control and Status Register (SATA–D31:F5) 573
15.1.25 MID—Message Signal Interrupt Identifier (SATA–D31:F5) (Consumer Only) 573
15.1.26 MC—Message Signal Interrupt Message Control (SATA–D31:F5) (Consumer Only) 574
15.1.27 MA—Message Signal Interrupt Message Address (SATA–D31:F5) (Consumer Only) 574
15.1.28 MD—Message Signal Interrupt Message Data (SATA–D31:F5) (Consumer Only) 574
15.1.29 MAP—Address Map Register (SATA–D31:F5)16 575
15.1.30 PCS—Port Control and Status Register (SATA–D31:F5) 576
15.1.31 SATACR0— SATA Capability Register 0 (SATA–D31:F5) 577
15.1.32 SATACR1— SATA Capability Register 1 (SATA–D31:F5) 577
15.1.33 FLRCID— FLR Capability ID (SATA–D31:F5) 577
15.1.34 FLRCLV— FLR Capability Length and Value (SATA–D31:F5) 578
15.1.35 FLRCTRL— FLR Control (SATA–D31:F5) 578
15.1.36 ATC—APM Trapping Control Register (SATA–D31:F5) 579
15.1.37 ATC—APM Trapping Control (SATA–D31:F5) 579
15.2 Bus Master IDE I/O Registers (D31:F5) 580
15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5) 581
15.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F5) 582
15.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F5) 582
15.3 Serial ATA Index/Data Pair Superset Registers 583
15.3.1 SINDX—SATA Index Register (D31:F5) 583
15.3.2 SDATA—SATA Index Data Register (D31:F5) 583

16 UHCI Controllers Registers 589
16.1 PCI Configuration Registers (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 589
16.1.1 VID—Vendor Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 590
16.1.2 DID—Device Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 590
16.1.3 PCICMD—PCI Command Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 591
16.1.4 PCISTS—PCI Status Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 592
16.1.5 RID—Revision Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 592
16.1.6 PI—Programming Interface Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 593
16.1.7 SCC—Sub Class Code Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 593
16.1.8 BCC—Base Class Code Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 593

16.1.9 MLT—Master Latency Timer Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 593
16.1.10 HEADTYP—Header Type Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 594
16.1.11 BASE—Base Address Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 594
16.1.12 SVID — Subsystem Vendor Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 594
16.1.13 SID — Subsystem Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 595
16.1.14 CAP_PTR—Capabilities Pointer (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 595
16.1.15 INT_LN—Interrupt Line Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 595
16.1.16 INT_PN—Interrupt Pin Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 596
16.1.17 FLRCID—Function Level Reset Capability ID (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 596
16.1.18 FLRNCP—Function Level Reset Next Capability Pointer (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 596
16.1.19 FLRCLV—Function Level Reset Capability Length and Version (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 597
16.1.20 USB_FLRCTRL—FLR Control Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 597
16.1.21 USB_FLRSTAT—FLR Status Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 598
16.1.22 USB_RELNUM—Serial Bus Release Number Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 598
16.1.23 USB_LEGKEY—USB Legacy Keyboard/Mouse Control Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 598
16.1.24 USB_RES—USB Resume Enable Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 600
16.1.25 CWP—Core Well Policy Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 601
16.1.26 UCR1—UCHI Configuration Register 1 (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 601
16.2 USB I/O Registers 602
16.2.1 USBCMD—USB Command Register 603
16.2.2 USBSTS—USB Status Register 606
16.2.3 USBINTR—USB Interrupt Enable Register 607
16.2.4 FRNUM—Frame Number Register 607
16.2.5 FRBASEADD—Frame List Base Address Register 608
16.2.6 SOFMOD—Start of Frame Modify Register 608
16.2.7 PORTSC[0,1]—Port Status and Control Register 609

17 EHCI Controller Registers (D29:F7, D26:F7) 611

17.1 USB EHCI Configuration Registers (USB EHCI—D29:F7, D26:F7) 611
17.1.1 VID—Vendor Identification Register (USB EHCI—D29:F7, D26:F7) 612
17.1.2 DID—Device Identification Register (USB EHCI—D29:F7, D26:F7) 612
17.1.3 PCICMD—PCI Command Register (USB EHCI—D29:F7, D26:F7) 613
17.1.4 PCISTS—PCI Status Register (USB EHCI—D29:F7, D26:F7) 614
17.1.5 RID—Revision Identification Register (USB EHCI—D29:F7, D26:F7) 615
17.1.6 PI—Programming Interface Register (USB EHCI—D29:F7, D26:F7) 615
17.1.7 SCC—Sub Class Code Register (USB EHCI—D29:F7, D26:F7) 615
17.1.8 BCC—Base Class Code Register (USB EHCI—D29:F7, D26:F7) 615
17.1.9 PMLT—Primary Master Latency Timer Register (USB EHCI—D29:F7, D26:F7) 616
17.1.10 MEM_BASE—Memory Base Address Register (USB EHCI—D29:F7, D26:F7) 616

17.1.11 SVID—USB EHCI Subsystem Vendor ID Register (USB EHCI—D29:F7, D26:F7) 616
17.1.12 SID—USB EHCI Subsystem ID Register (USB EHCI—D29:F7, D26:F7) 617
17.1.13 CAP_PTR—Capabilities Pointer Register (USB EHCI—D29:F7, D26:F7) 617
17.1.14 INT_LN—Interrupt Line Register (USB EHCI—D29:F7, D26:F7) 617
17.1.15 INT_PN—Interrupt Pin Register (USB EHCI—D29:F7, D26:F7) 617
17.1.16 PWR_CAPID—PCI Power Management Capability ID Register (USB EHCI—D29:F7, D26:F7) 618
17.1.17 NXT_PTR1—Next Item Pointer #1 Register (USB EHCI—D29:F7, D26:F7) 618
17.1.18 PWR_CAP—Power Management Capabilities Register (USB EHCI—D29:F7, D26:F7) 619
17.1.19 PWR_CNTL_STS—Power Management Control/ Status Register (USB EHCI—D29:F7, D26:F7) 620
17.1.20 DEBUG_CAPID—Debug Port Capability ID Register (USB EHCI—D29:F7, D26:F7) 621
17.1.21 NXT_PTR2—Next Item Pointer #2 Register (USB EHCI—D29:F7, D26:F7) 621
17.1.22 DEBUG_BASE—Debug Port Base Offset Register (USB EHCI—D29:F7, D26:F7) 621
17.1.23 USB_RELNUM—USB Release Number Register (USB EHCI—D29:F7, D26:F7) 621
17.1.24 FL_ADJ—Frame Length Adjustment Register (USB EHCI—D29:F7, D26:F7) 622
17.1.25 PWAKE_CAP—Port Wake Capability Register (USB EHCI—D29:F7, D26:F7) 623
17.1.26 LEG_EXT_CAP—USB EHCI Legacy Support Extended Capability Register (USB EHCI—D29:F7, D26:F7) 624
17.1.27 LEG_EXT_CS—USB EHCI Legacy Support Extended Control / Status Register (USB EHCI—D29:F7, D26:F7) 624
17.1.28 SPECIAL_SMI—Intel Specific USB 2.0 SMI Register (USB EHCI—D29:F7, D26:F7) 626
17.1.29 ACCESS_CNTL—Access Control Register (USB EHCI—D29:F7, D26:F7) 628
17.1.30 EHCIIR1—EHCI Initialization Register 1 (USB EHCI—D29:F7, D26:F7) 628
17.1.31 FLR_CID—Function Level Reset Capability ID (USB EHCI—D29:F7, D26:F7) 628
17.1.32 FLR_NEXT—Function Level Reset Next Capability Pointer (USB EHCI—D29:F7, D26:F7) 629
17.1.33 FLR_CLV—Function Level Reset Capability Length and Version (USB EHCI—D29:F7, D26:F7) 629
17.1.34 FLR_CTRL—Function Level Reset Control Register (USB EHCI—D29:F7, D26:F7) 630
17.1.35 FLR_STS—Function Level Reset Status Register (USB EHCI—D29:F7, D26:F7) 630
17.1.36 EHCIIR2—EHCI Initialization Register 2 (USB EHCI—D29:F7, D26:F7) 630
17.2 Memory-Mapped I/O Registers 631
17.2.1 Host Controller Capability Registers 631
17.2.2 Host Controller Operational Registers 635
17.2.3 USB 2.0-Based Debug Port Register 649

18 Intel® High Definition Audio Controller Registers (D27:F0) 653
18.1 Intel® High Definition Audio PCI Configuration Space (Intel® High Definition Audio— D27:F0) 653
18.1.1 VID—Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0) 655
18.1.2 DID—Device Identification Register (Intel® High Definition Audio Controller—D27:F0) 655
18.1.3 PCICMD—PCI Command Register (Intel® High Definition Audio Controller—D27:F0) 655

18.1.4 PCISTS—PCI Status Register (Intel® High Definition Audio Controller—D27:F0) 656
18.1.5 RID—Revision Identification Register (Intel® High Definition Audio Controller—D27:F0) 657
18.1.6 PI—Programming Interface Register (Intel® High Definition Audio Controller—D27:F0) 657
18.1.7 SCC—Sub Class Code Register (Intel® High Definition Audio Controller—D27:F0) 657
18.1.8 BCC—Base Class Code Register (Intel® High Definition Audio Controller—D27:F0) 657
18.1.9 CLS—Cache Line Size Register (Intel® High Definition Audio Controller—D27:F0) 657
18.1.10 LT—Latency Timer Register (Intel® High Definition Audio Controller—D27:F0) 658
18.1.11 HEADTYP—Header Type Register (Intel® High Definition Audio Controller—D27:F0) 658
18.1.12 HDBARL—Intel® High Definition Audio Lower Base Address Register (Intel® High Definition Audio—D27:F0) 658
18.1.13 HDBARU—Intel® High Definition Audio Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0) 658
18.1.14 SVID—Subsystem Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0) 659
18.1.15 SID—Subsystem Identification Register (Intel® High Definition Audio Controller—D27:F0) 659
18.1.16 CAPPTR—Capabilities Pointer Register (Intel® High Definition Audio Controller—D27:F0) 659
18.1.17 INTLN—Interrupt Line Register (Intel® High Definition Audio Controller—D27:F0) 660
18.1.18 INTPN—Interrupt Pin Register (Intel® High Definition Audio Controller—D27:F0) 660
18.1.19 HDCTL—Intel® High Definition Audio Control Register (Intel® High Definition Audio Controller—D27:F0) 660
18.1.20 TCSEL—Traffic Class Select Register (Intel® High Definition Audio Controller—D27:F0) 661
18.1.21 PID—PCI Power Management Capability ID Register (Intel® High Definition Audio Controller—D27:F0) 661
18.1.22 PC—Power Management Capabilities Register (Intel® High Definition Audio Controller—D27:F0) 662
18.1.23 PCS—Power Management Control and Status Register (Intel® High Definition Audio Controller—D27:F0) 663
18.1.24 MID—MSI Capability ID Register (Intel® High Definition Audio Controller—D27:F0) 664
18.1.25 MMC—MSI Message Control Register (Intel® High Definition Audio Controller—D27:F0) 664
18.1.26 MMLA—MSI Message Lower Address Register (Intel® High Definition Audio Controller—D27:F0) 664
18.1.27 MMUA—MSI Message Upper Address Register (Intel® High Definition Audio Controller—D27:F0) 664
18.1.28 MMD—MSI Message Data Register (Intel® High Definition Audio Controller—D27:F0) 665
18.1.29 PXID—PCI Express* Capability ID Register (Intel® High Definition Audio Controller—D27:F0) 665
18.1.30 PXC—PCI Express* Capabilities Register (Intel® High Definition Audio Controller—D27:F0) 665
18.1.31 DEVCAP—Device Capabilities Register (Intel® High Definition Audio Controller—D27:F0) 666
18.1.32 DEVC—Device Control Register (Intel® High Definition Audio Controller—D27:F0) 667
18.1.33 DEVS—Device Status Register (Intel® High Definition Audio Controller—D27:F0) 668
18.1.34 VCCAP—Virtual Channel Enhanced Capability Header (Intel® High Definition Audio Controller—D27:F0) 668
18.1.35 PVCCAP1—Port VC Capability Register 1 (Intel® High Definition Audio Controller—D27:F0) 669
18.1.36 PVCCAP2 — Port VC Capability Register 2 (Intel® High Definition Audio Controller—D27:F0) 669

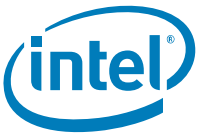
18.1.37 PVCCTL — Port VC Control Register (Intel® High Definition Audio Controller—D27:F0) 669
18.1.38 PVCSTS—Port VC Status Register (Intel® High Definition Audio Controller—D27:F0) 670
18.1.39 VC0CAP—VC0 Resource Capability Register (Intel® High Definition Audio Controller—D27:F0) 670
18.1.40 VC0CTL—VC0 Resource Control Register (Intel® High Definition Audio Controller—D27:F0) 671
18.1.41 VC0STS—VC0 Resource Status Register (Intel® High Definition Audio Controller—D27:F0) 671
18.1.42 VCiCAP—VCi Resource Capability Register (Intel® High Definition Audio Controller—D27:F0) 672
18.1.43 VCiCTL—VCi Resource Control Register (Intel® High Definition Audio Controller—D27:F0) 672
18.1.44 VCiSTS—VCi Resource Status Register (Intel® High Definition Audio Controller—D27:F0) 673
18.1.45 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (Intel® High Definition Audio Controller—D27:F0) 673
18.1.46 ESD—Element Self Description Register (Intel® High Definition Audio Controller—D27:F0) 673
18.1.47 L1DESC—Link 1 Description Register (Intel® High Definition Audio Controller—D27:F0) 674
18.1.48 L1ADDL—Link 1 Lower Address Register (Intel® High Definition Audio Controller—D27:F0) 674
18.1.49 L1ADDU—Link 1 Upper Address Register (Intel® High Definition Audio Controller—D27:F0) 674
18.2 Intel® High Definition Audio Memory Mapped Configuration Registers (Intel® High Definition Audio— D27:F0) 675
18.2.1 GCAP—Global Capabilities Register (Intel® High Definition Audio Controller—D27:F0) 679
18.2.2 VMIN—Minor Version Register (Intel® High Definition Audio Controller—D27:F0) 679
18.2.3 VMAJ—Major Version Register (Intel® High Definition Audio Controller—D27:F0) 679
18.2.4 OUTPAY—Output Payload Capability Register (Intel® High Definition Audio Controller—D27:F0) 680
18.2.5 INPAY—Input Payload Capability Register (Intel® High Definition Audio Controller—D27:F0) 680
18.2.6 GCTL—Global Control Register (Intel® High Definition Audio Controller—D27:F0) 681
18.2.7 WAKEEN—Wake Enable Register (Intel® High Definition Audio Controller—D27:F0) 682
18.2.8 STATESTS—State Change Status Register (Intel® High Definition Audio Controller—D27:F0) 682
18.2.9 GSTS—Global Status Register (Intel® High Definition Audio Controller—D27:F0) 683
18.2.10 OUTSTRMPAY—Output Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0) 683
18.2.11 INSTRMPAY—Input Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0) 684
18.2.12 INTCTL—Interrupt Control Register (Intel® High Definition Audio Controller—D27:F0) 685
18.2.13 INTSTS—Interrupt Status Register (Intel® High Definition Audio Controller—D27:F0) 686
18.2.14 WALCLK—Wall Clock Counter Register (Intel® High Definition Audio Controller—D27:F0) 686
18.2.15 SSYNC—Stream Synchronization Register (Intel® High Definition Audio Controller—D27:F0) 687
18.2.16 CORBLBASE—CORB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0) 687
18.2.17 CORBUBASE—CORB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0) 688
18.2.18 CORBWP—CORB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0) 688
18.2.19 CORBRP—CORB Read Pointer Register (Intel® High Definition Audio Controller—D27:F0) 688

18.2.20 CORBCTL—CORB Control Register (Intel® High Definition Audio Controller—D27:F0) 689
18.2.21 CORBST—CORB Status Register (Intel® High Definition Audio Controller—D27:F0) 689
18.2.22 CORBSIZE—CORB Size Register Intel® High Definition Audio Controller—D27:F0) 689
18.2.23 RIRBLBASE—RIRB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0) 690
18.2.24 RIRBUBASE—RIRB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0) 690
18.2.25 RIRBWP—RIRB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0) 690
18.2.26 RINTCNT—Response Interrupt Count Register (Intel® High Definition Audio Controller—D27:F0) 691
18.2.27 RIRBCTL—RIRB Control Register (Intel® High Definition Audio Controller—D27:F0) 691
18.2.28 RIRBSTS—RIRB Status Register (Intel® High Definition Audio Controller—D27:F0) 692
18.2.29 RIRBSIZE—RIRB Size Register (Intel® High Definition Audio Controller—D27:F0) 692
18.2.30 IC—Immediate Command Register (Intel® High Definition Audio Controller—D27:F0) 692
18.2.31 IR—Immediate Response Register (Intel® High Definition Audio Controller—D27:F0) 693
18.2.32 IRS—Immediate Command Status Register (Intel® High Definition Audio Controller—D27:F0) 693
18.2.33 DPLBASE—DMA Position Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0) 694
18.2.34 DPUBASE—DMA Position Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0) 694
18.2.35 SDCTL—Stream Descriptor Control Register (Intel® High Definition Audio Controller—D27:F0) 695
18.2.36 SDSTS—Stream Descriptor Status Register (Intel® High Definition Audio Controller—D27:F0) 697
18.2.37 SDLPIB—Stream Descriptor Link Position in Buffer Register (Intel® High Definition Audio Controller—D27:F0) 698
18.2.38 SDCBL—Stream Descriptor Cyclic Buffer Length Register (Intel® High Definition Audio Controller—D27:F0) 698
18.2.39 SDLVI—Stream Descriptor Last Valid Index Register (Intel® High Definition Audio Controller—D27:F0) 699
18.2.40 SDFIFOW—Stream Descriptor FIFO Watermark Register (Intel® High Definition Audio Controller—D27:F0) 699
18.2.41 SDFIFOS—Stream Descriptor FIFO Size Register (Intel® High Definition Audio Controller—D27:F0) 700
18.2.42 SDFMT—Stream Descriptor Format Register (Intel® High Definition Audio Controller—D27:F0) 701
18.2.43 SDBDPL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0) 702
18.2.44 SDBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0) 702

19 SMBus Controller Registers (D31:F3) 703
19.1 PCI Configuration Registers (SMBus—D31:F3) 703
19.1.1 VID—Vendor Identification Register (SMBus—D31:F3) 703
19.1.2 DID—Device Identification Register (SMBus—D31:F3) 704
19.1.3 PCICMD—PCI Command Register (SMBus—D31:F3) 704
19.1.4 PCISTS—PCI Status Register (SMBus—D31:F3) 705
19.1.5 RID—Revision Identification Register (SMBus—D31:F3) 705
19.1.6 PI—Programming Interface Register (SMBus—D31:F3) 706
19.1.7 SCC—Sub Class Code Register (SMBus—D31:F3) 706
19.1.8 BCC—Base Class Code Register (SMBus—D31:F3) 706
19.1.9 SMBMBAR0—D31_F3_SMBus Memory Base Address 0 (SMBus—D31:F3) 706
19.1.10 SMBMBAR1—D31_F3_SMBus Memory Base Address 1 (SMBus—D31:F3) 707
19.1.11 SMB_BASE—SMBus Base Address Register (SMBus—D31:F3) 707

19.1.12 SVID—Subsystem Vendor Identification Register (SMBus—D31:F2/F4) 707
19.1.13 SID—Subsystem Identification Register (SMBus—D31:F2/F4) 708
19.1.14 INT_LN—Interrupt Line Register (SMBus—D31:F3) 708
19.1.15 INT_PN—Interrupt Pin Register (SMBus—D31:F3) 708
19.1.16 HOSTC—Host Configuration Register (SMBus—D31:F3) 709
19.2 SMBus I/O and Memory Mapped I/O Registers 710
19.2.1 HST_STS—Host Status Register (SMBus—D31:F3) 711
19.2.2 HST_CNT—Host Control Register (SMBus—D31:F3) 712
19.2.3 HST_CMD—Host Command Register (SMBus—D31:F3) 714
19.2.4 XMIT_SLVA—Transmit Slave Address Register (SMBus—D31:F3) 714
19.2.5 HST_D0—Host Data 0 Register (SMBus—D31:F3) 714
19.2.6 HST_D1—Host Data 1 Register (SMBus—D31:F3) 714
19.2.7 Host_BLOCK_DB—Host Block Data Byte Register (SMBus—D31:F3) 715
19.2.8 PEC—Packet Error Check (PEC) Register (SMBus—D31:F3) 715
19.2.9 RCV_SLVA—Receive Slave Address Register (SMBus—D31:F3) 716
19.2.10 SLV_DATA—Receive Slave Data Register (SMBus—D31:F3) 716
19.2.11 AUX_STS—Auxiliary Status Register (SMBus—D31:F3) 716
19.2.12 AUX_CTL—Auxiliary Control Register (SMBus—D31:F3) 717
19.2.13 SMLINK_PIN_CTL—SMLink Pin Control Register (SMBus—D31:F3) 717
19.2.14 SMBus_PIN_CTL—SMBus Pin Control Register (SMBus—D31:F3) 718
19.2.15 SLV_STS—Slave Status Register (SMBus—D31:F3) 718
19.2.16 SLV_CMD—Slave Command Register (SMBus—D31:F3) 719
19.2.17 NOTIFY_DADDR—Notify Device Address Register (SMBus—D31:F3) 719
19.2.18 NOTIFY_DLOW—Notify Data Low Byte Register (SMBus—D31:F3) 720
19.2.19 NOTIFY_DHIGH—Notify Data High Byte Register (SMBus—D31:F3) 720

20 PCI Express* Configuration Registers 721
20.1 PCI Express* Configuration Registers (PCI Express—D28:F0/F1/F2/F3/F4/F5) 721
20.1.1 VID—Vendor Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 724
20.1.2 DID—Device Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 724
20.1.3 PCICMD—PCI Command Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 725
20.1.4 PCISTS—PCI Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 726
20.1.5 RID—Revision Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 727
20.1.6 PI—Programming Interface Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 727
20.1.7 SCC—Sub Class Code Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 727
20.1.8 BCC—Base Class Code Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 727
20.1.9 CLS—Cache Line Size Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 728
20.1.10 PLT—Primary Latency Timer Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 728
20.1.11 HEADTYP—Header Type Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 728
20.1.12 BNUM—Bus Number Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 728
20.1.13 SLT—Secondary Latency Timer (PCI Express—D28:F0/F1/F2/F3/F4/F5) 729
20.1.14 IOBL—I/O Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 729
20.1.15 SSTS—Secondary Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 730
20.1.16 MBL—Memory Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 731
20.1.17 PMBL—Prefetchable Memory Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 731
20.1.18 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 731
20.1.19 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 732



20.1.20 CAPP—Capabilities List Pointer Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 732
20.1.21 INTR—Interrupt Information Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 732
20.1.22 BCTRL—Bridge Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 733
20.1.23 CLIST—Capabilities List Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 734
20.1.24 XCAP—PCI Express* Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 734
20.1.25 DCAP—Device Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 735
20.1.26 DCTL—Device Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 736
20.1.27 DSTS—Device Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 737
20.1.28 LCAP—Link Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 738
20.1.29 LCTL—Link Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 740
20.1.30 LSTS—Link Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 741
20.1.31 SLCAP—Slot Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 742
20.1.32 SLCTL—Slot Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 743
20.1.33 SLSTS—Slot Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 744
20.1.34 RCTL—Root Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 745
20.1.35 RSTS—Root Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 745
20.1.36 DCAP2—Device Capabilities 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5) 746
20.1.37 DCTL2—Device Control 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5) 746
20.1.38 LCTL2—Link Control 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5) 747
20.1.39 MID—Message Signaled Interrupt Identifiers Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 747
20.1.40 MC—Message Signaled Interrupt Message Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 747
20.1.41 MA—Message Signaled Interrupt Message Address Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 748
20.1.42 MD—Message Signaled Interrupt Message Data Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 748
20.1.43 SVCAP—Subsystem Vendor Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 748
20.1.44 SVID—Subsystem Vendor Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 748
20.1.45 PMCAP—Power Management Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 749
20.1.46 PMC—PCI Power Management Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 749
20.1.47 PMCS—PCI Power Management Control and Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 750
20.1.48 MPC2—Miscellaneous Port Configuration Register 2 (PCI Express—D28:F0/F1/F2/F3/F4/F5) 751
20.1.49 MPC—Miscellaneous Port Configuration Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 752
20.1.50 SMSCS—SMI/SCI Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 754
20.1.51 RPDCGEN—Root Port Dynamic Clock Gating Enable (PCI Express-D28:F0/F1/F2/F3/F4/F5) 755
20.1.52 PECR1—PCI Express* Configuration Register 1 (PCI Express—D28:F0/F1/F2/F3/F4/F5) 755

20.1.53 VCH—Virtual Channel Capability Header Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 756
20.1.54 VCAP2—Virtual Channel Capability 2 Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 756
20.1.55 PVC—Port Virtual Channel Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 756
20.1.56 PVS—Port Virtual Channel Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 757
20.1.57 V0CAP—Virtual Channel 0 Resource Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 757
20.1.58 V0CTL—Virtual Channel 0 Resource Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 758
20.1.59 V0STS—Virtual Channel 0 Resource Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 758
20.1.60 UES—Uncorrectable Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 759
20.1.61 UEM—Uncorrectable Error Mask (PCI Express—D28:F0/F1/F2/F3/F4/F5) 760
20.1.62 UEV — Uncorrectable Error Severity (PCI Express—D28:F0/F1/F2/F3/F4/F5) 761
20.1.63 CES — Correctable Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 762
20.1.64 CEM — Correctable Error Mask Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 762
20.1.65 AECC — Advanced Error Capabilities and Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 763
20.1.66 RES — Root Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 763
20.1.67 RCTCL — Root Complex Topology Capability List Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 763
20.1.68 ESD—Element Self Description Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 764
20.1.69 ULD — Upstream Link Description Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 764
20.1.70 ULBA — Upstream Link Base Address Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 765
20.1.71 PECR2 — PCI Express* Configuration Register 2 (PCI Express—D28:F0/F1/F2/F3/F4/F5) 765
20.1.72 PEETM — PCI Express* Extended Test Mode Register (PCI Express—D28:F0/F1/F2/F3/F4/F5) 765
20.1.73 PEC1 — PCI Express* Configuration Register 1 (PCI Express—D28:F0/F1/F2/F3/F4/F5) 766

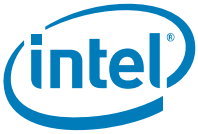
21 High Precision Event Timer Registers 767
21.1 Memory Mapped Registers 767
21.1.1 GCAP_ID—General Capabilities and Identification Register 769
21.1.2 GEN_CONF—General Configuration Register 770
21.1.3 GINTR_STA—General Interrupt Status Register 770
21.1.4 MAIN_CNT—Main Counter Value Register 771
21.1.5 TIMn_CONF—Timer n Configuration and Capabilities Register 772
21.1.6 TIMn_COMP—Timer n Comparator Value Register 775

22 Serial Peripheral Interface (SPI) 777
22.1 Serial Peripheral Interface Memory Mapped Configuration Registers 777
22.1.1 BFPR –BIOS Flash Primary Region Register (SPI Memory Mapped Configuration Registers) 779
22.1.2 HSFS—Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers) 779
22.1.3 HSFC—Hardware Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers) 781
22.1.4 FADDR—Flash Address Register (SPI Memory Mapped Configuration Registers) 781
22.1.5 FDATA0—Flash Data 0 Register (SPI Memory Mapped Configuration Registers) 782
22.1.6 FDATAN—Flash Data [N] Register (SPI Memory Mapped Configuration Registers) 782

22.1.7 FRAP—Flash Regions Access Permissions Register (SPI Memory Mapped Configuration Registers) 783
22.1.8 FREG0—Flash Region 0 (Flash Descriptor) Register (SPI Memory Mapped Configuration Registers) 784
22.1.9 FREG1—Flash Region 1 (BIOS Descriptor) Register (SPI Memory Mapped Configuration Registers) 784
22.1.10 FREG2—Flash Region 2 (ME) Register (SPI Memory Mapped Configuration Registers) 785
22.1.11 FREG3—Flash Region 3 (GbE) Register (SPI Memory Mapped Configuration Registers) 785
22.1.12 FREG4—Flash Region 4 (Platform Data) Register (SPI Memory Mapped Configuration Registers) 786
22.1.13 PR0—Protected Range 0 Register (SPI Memory Mapped Configuration Registers) 786
22.1.14 PR1—Protected Range 1 Register (SPI Memory Mapped Configuration Registers) 787
22.1.15 PR2—Protected Range 2 Register (SPI Memory Mapped Configuration Registers) 788
22.1.16 PR3—Protected Range 3 Register (SPI Memory Mapped Configuration Registers) 788
22.1.17 PR4—Protected Range 4 Register (SPI Memory Mapped Configuration Registers) 789
22.1.18 SSFS—Software Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers) 790
22.1.19 SSFC—Software Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers) 791
22.1.20 PREOP—Prefix Opcode Configuration Register (SPI Memory Mapped Configuration Registers) 792
22.1.21 OPTYPE—Opcode Type Configuration Register (SPI Memory Mapped Configuration Registers) 792
22.1.22 OPMENU—Opcode Menu Configuration Register (SPI Memory Mapped Configuration Registers) 793
22.1.23 BBAR—BIOS Base Address Configuration Register (SPI Memory Mapped Configuration Registers) 794
22.1.24 FDOC—Flash Descriptor Observability Control Register (SPI Memory Mapped Configuration Registers) 794
22.1.25 FDOD—Flash Descriptor Observability Data Register (SPI Memory Mapped Configuration Registers) 795
22.1.26 AFC—Additional Flash Control Register (SPI Memory Mapped Configuration Registers) 795
22.1.27 LVSCC— Host Lower Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers) 796
22.1.28 UVSCC— Host Upper Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers) 797
22.1.29 FPB — Flash Partition Boundary (SPI Memory Mapped Configuration Registers) 799
22.2 Flash Descriptor Registers 800
22.2.1 Flash Descriptor Content 800
22.2.2 Flash Descriptor Component Section 802
22.2.3 Flash Descriptor Region Section 805
22.2.4 Flash Descriptor Master Section 807
22.2.5 Descriptor Upper Map Section 810
22.2.6 Intel ME Vendor Specific Component Capabilities Table 810
22.3 OEM Section 815
22.4 GbE SPI Flash Program Registers 815
22.4.1 GLFPR –Gigabit LAN Flash Primary Region Register (GbE LAN Memory Mapped Configuration Registers) 816
22.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers) 817
22.4.3 HSFC—Hardware Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers) 818
22.4.4 FADDR—Flash Address Register (GbE LAN Memory Mapped Configuration Registers) 818
22.4.5 FDATA0—Flash Data 0 Register (GbE LAN Memory Mapped Configuration Registers) 819
22.4.6 FRAP—Flash Regions Access Permissions Register (GbE LAN Memory Mapped Configuration Registers) 820

22.4.7 FREG0—Flash Region 0 (Flash Descriptor) Register (GbE LAN Memory Mapped Configuration Registers) 821
22.4.8 FREG1—Flash Region 1 (BIOS Descriptor) Register (GbE LAN Memory Mapped Configuration Registers) 821
22.4.9 FREG2—Flash Region 2 (ME) Register (GbE LAN Memory Mapped Configuration Registers) 821
22.4.10 FREG3—Flash Region 3 (GbE) Register (GbE LAN Memory Mapped Configuration Registers) 822
22.4.11 FPR0—Flash Protected Range 0 Register (GbE LAN Memory Mapped Configuration Registers) 822
22.4.12 FPR1—Flash Protected Range 1 Register (GbE LAN Memory Mapped Configuration Registers) 823
22.4.13 SSFS—Software Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers) 824
22.4.14 SSFC—Software Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers) 825
22.4.15 PREOP—Prefix Opcode Configuration Register (GbE LAN Memory Mapped Configuration Registers) 826
22.4.16 OPTYPE—Opcode Type Configuration Register (GbE LAN Memory Mapped Configuration Registers) 826
22.4.17 OPMENU—Opcode Menu Configuration Register (GbE LAN Memory Mapped Configuration Registers) 827

23 Thermal Sensor Registers (D31:F6) 829
23.1 PCI Bus Configuration Registers 829
23.1.1 VID—Vendor Identification 830
23.1.2 DID—Device Identification 830
23.1.3 CMD—Command 830
23.1.4 STS—Status 831
23.1.5 RID—Revision Identification 831
23.1.6 PI— Programming Interface 831
23.1.7 SCC—Sub Class Code 832
23.1.8 BCC—Base Class Code 832
23.1.9 CLS—Cache Line Size 832
23.1.10 LT—Latency Timer 832
23.1.11 BIST—Built-in Self Test 833
23.1.12 TBAR—Thermal Base 833
23.1.13 TBARH—Thermal Base High DWord 833
23.1.14 SVID—Subsystem Vendor ID 834
23.1.15 SID—Subsystem ID 834
23.1.16 CAP_PTR —Capabilities Pointer 834
23.1.17 Offset 3Ch – INTLN—Interrupt Line 834
23.1.18 INTPN—Interrupt Pin 835
23.1.19 TBARB—BIOS Assigned Thermal Base Address 835
23.1.20 TBARBH—BIOS Assigned Thermal Base High DWord 835
23.1.21 PID—PCI Power Management Capability ID 836
23.1.22 PC—Power Management Capabilities 836
23.1.23 PCS—Power Management Control And Status 837
23.2 Thermal Memory Mapped Configuration Registers (Thermal Sensor - D31:F26) 838
23.2.1 TSxE—Thermal Sensor [1:0] Enable 838
23.2.2 TSxS—Thermal Sensor[1:0] Status 839
23.2.3 TSxTTP—Thermal Sensor [1:0] Catastrophic Trip Point 839
23.2.4 TSxCO—Thermal Sensor [1:0] Catastrophic Lock-Down 839
23.2.5 TSxPC—Thermal Sensor [1:0] Policy Control 840
23.2.6 TSxLOCK—Thermal Sensor [1:0] Register Lock Control 840



Figures

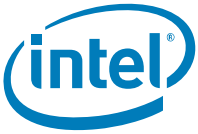
2-1 Intel® ICH10 Interface Signals Block Diagram 46
2-1 Example External RTC Circuit 79
4-1 ICH10 Conceptual System Clock Diagram 92
5-1 Generation of SERR# to Platform 99
5-2 LPC Interface Diagram 107
5-3 Intel® ICH10 DMA Controller 112
5-4 DMA Request Assertion through LDRQ# 115
5-5 Coprocessor Error Timing Diagram 140
5-6 TCO Legacy/Compatible Mode SMBus Configuration 169
5-7 Advanced TCO Intel® ME SMBus/SMLink Configuration 171
5-8 Advanced TCO BMC Mode SMBus/SMLink Configuration 172
5-9 Serial Post over GPIO Reference Circuit 174
5-10 SATA Power States 181
5-11 Flow for Port Enable / Device Present Bits 183
5-12 Serial Data transmitted over the SGPIO Interface 188
5-13 USB Legacy Keyboard Flow Diagram 198
5-14 Intel® ICH10-USB Port Connections Default Six and Six Configuration 206
5-15 Intel® ICH10-USB Port Connections Eight and Four Configuration 206
5-16 Flash Partition Boundary 231
5-17 Flash Descriptor Sections 232
6-1 Intel® ICH10 Ballout (Top view–Left Side) 244
6-2 Intel® ICH10 Ballout (Top view–Right Side) 245
7-1 Intel® ICH10 Package (Top View) 253
7-2 Intel® ICH10 Package (Bottom View) 254
7-3 Intel® ICH10 Package (Side View) 254
8-1 Clock Timing 280
8-2 Valid Delay from Rising Clock Edge 280
8-3 Setup and Hold Times 281
8-4 Float Delay 281
8-5 Pulse Width 281
8-6 Output Enable Delay 281
8-7 USB Rise and Fall Times 282
8-8 USB Jitter 282
8-9 USB EOP Width 282
8-10 SMBus Transaction 283
8-11 SMBus Timeout 283
8-12 SPI Timings 284
8-13 Intel® High Definition Audio Input and Output Timings 284
8-14 Power Sequencing and Reset Signal Timings 285
8-15 G3 (Mechanical Off) to S0 Timings 286
8-16 S0 to S1 to S0 Timings 287
8-17 S0 to S5 to S0 Timings 287
8-18 C0 to C2 to C0 Timings 288
8-19 C0 to C3 to C0 Timings 288
8-20 C0 to C4 to C0 Timings 289
8-21 Sleep control signal relationship - Host boots and Intel Management Engine off 290
8-22 Sleep control signal relationship - Host and Intel Management Engine boot after G3 290
8-23 Sleep control signal relationship - Host stays in S5 and Intel Management Engine boots after G3 291
8-24 S4, S5/M1 to S0/M0 291
8-25 S0 to S3/S4/S5 and G3 Timings 291

Tables

1-1 Industry Specifications 33
1-2 PCI Devices and Functions 37
1-3 Intel® ICH10 Components 44
2-1 Direct Media Interface Signals 47
2-2 PCI Express* Signals 48
2-3 LAN Connect Interface Signals 48
2-4 Gigabit LAN Connect Interface Signals 49
2-5 Firmware Hub Interface Signals 50
2-6 PCI Interface Signals 50
2-7 Serial ATA Interface Signals 52
2-8 LPC Interface Signals 55
2-9 Interrupt Signals 55
2-10 USB Interface Signals 56
2-11 Power Management Interface Signals 58
2-12 Processor Interface Signals 61
2-13 SMBus Interface Signals 62
2-14 System Management Interface Signals 63
2-15 Real Time Clock Interface 64
2-16 Other Clocks 65
2-17 Miscellaneous Signals 65
2-18 Intel® High Definition Audio Link Signals 66
2-19 Serial Peripheral Interface (SPI) Signals 67
2-20 Controller Link Signals 68
2-21 Intel® Quiet System Technology Signals 68
2-22 JTAG Signals 69
2-23 General Purpose I/O Signals 70
2-24 Power and Ground Signals 73
2-25 Functional Strap Definitions 75
3-1 Integrated Pull-Up and Pull-Down Resistors 81
3-2 Power Plane and States for Output and I/O Signals for Configurations 83
3-3 Power Plane for Input Signals for Configurations 88
4-1 Intel® ICH10 and System Clock Domains 91
5-1 PCI Bridge Initiator Cycle Types 93
5-2 Type 1 Address Format 96
5-3 MSI versus PCI IRQ Actions 98
5-4 LAN Mode Support 103
5-5 LPC Cycle Types Supported 108
5-6 Start Field Bit Definitions 108
5-7 Cycle Type Bit Definitions 109
5-8 Transfer Size Bit Definition 109
5-9 SYNC Bit Definition 110
5-10 DMA Transfer Size 114
5-11 Address Shifting in 16-Bit I/O DMA Transfers 114
5-12 Counter Operating Modes 119
5-13 Interrupt Controller Core Connections 121
5-14 Interrupt Status Registers 122
5-15 Content of Interrupt Vector Byte 122
5-16 APIC Interrupt Mapping1 128
5-17 Interrupt Message Address Format 130
5-18 Interrupt Message Data Format 131
5-19 Stop Frame Explanation 133
5-20 Data Frame Format 134
5-21 Configuration Bits Reset by RTCRST# Assertion 137
5-22 INIT# Going Active 139
5-23 NMI Sources 140
5-24 DP Signal Differences 141
5-25 General Power States for Systems Using Intel® ICH10 143
5-26 State Transition Rules for Intel® ICH10 144
5-27 System Power Plane 145
5-28 Causes of SMI# and SCI 146
5-29 Break Events 149
5-30 Sleep Types 151
5-31 Causes of Wake Events 152
5-32 GPI Wake Events 153
5-33 Transitions Due to Power Failure 154

5-34 Transitions Due to Power Button 155
5-35 Transitions Due to RI# Signal 157
5-36 Write Only Registers with Read Paths in ALT Access Mode 159
5-37 PIC Reserved Bits Return Values 161
5-38 Register Write Accesses in ALT Access Mode 161
5-39 Intel® ICH10 Clock Inputs 164
5-40 Causes of Host and Global Resets 166
5-41 Event Transitions that Cause Messages 170
5-42 Multi-activity LED message type 187
5-43 Legacy Replacement Routing 190
5-44 Bits Maintained in Low Power States 197
5-45 USB Legacy Keyboard State Transitions 198
5-46 UHCI vs. EHCI 201
5-47 Debug Port Behavior 210
5-48 I2C Block Read 218
5-49 Enable for SMBALERT# 221
5-50 Enables for SMBus Slave Write and SMBus Host Events 221
5-51 Enables for the Host Notify Command 221
5-52 Slave Write Registers 223
5-53 Command Types 223
5-54 Slave Read Cycle Format 224
5-55 Data Values for Slave Read Registers 225
5-56 Host Notify Format 227
5-57 Region Size versus Erase Granularity of Flash Components 231
5-58 Region Access Control Table 233
5-59 Hardware Sequencing Commands and Opcode Requirements 236
5-60 Flash Protection Mechanism Summary 237
5-61 Recommended Pinout for 8-Pin Serial Flash Device 238
5-62 Recommended Pinout for 16-Pin Serial Flash Device 239
6-1 Intel® ICH10 Ballout by Signal Name 246
8-1 Intel® ICH10 Absolute Maximum Ratings 255
8-2 DC Current Characteristics (Consumer Only)1 255
8-3 DC Current Characteristics (Corporate Only) 257
8-4 DC Characteristic Input Signal Association 258
8-5 DC Input Characteristics 260
8-6 DC Characteristic Output Signal Association 262
8-7 DC Output Characteristics 264
8-8 Other DC Characteristics 266
8-9 Clock Timings 268
8-10 PCI Interface Timing 269
8-11 Universal Serial Bus Timing 270
8-12 SATA Interface Timings 271
8-13 SMBus Timing 272
8-14 Intel® High Definition Audio Timing 272
8-15 LPC Timing 273
8-16 Miscellaneous Timings 273
8-17 SPI Timings (20 MHz) 273
8-18 SPI Timings (33 MHz) 274
8-19 SST Timings 274
8-20 PECI Timings 275
8-21 Power Sequencing and Reset Signal Timings 275
8-22 Power Management Timings 277
9-1 PCI Devices and Functions 294
9-2 Fixed I/O Ranges Decoded by Intel® ICH10 296
9-3 Variable I/O Decode Ranges 298
9-4 Memory Decode Ranges from Processor Perspective 299
10-1 Chipset Configuration Register Memory Map (Memory Space) 303
11-1 PCI Bridge Register Address Map (PCI-PCI—D30:F0) 355
12-1 Gigabit LAN Configuration Registers Address Map (Gigabit LAN —D25:F0) 371
12-2 Gigabit LAN Base Address A Registers Address Map (Gigabit LAN— D25:F0) 384
13-1 LPC Interface PCI Register Address Map (LPC I/F—D31:F0) 387
13-2 DMA Registers 411
13-3 PIC Registers (LPC I/F—D31:F0) 424
13-4 APIC Direct Registers (LPC I/F—D31:F0) 433
13-5 APIC Indirect Registers (LPC I/F—D31:F0) 433

13-6 RTC I/O Registers 439
13-7 RTC (Standard) RAM Bank 440
13-8 Processor Interface PCI Register Address Map (LPC I/F—D31:F0) 444
13-9 Power Management PCI Register Address Map (PM—D31:F0) 447
13-10 APM Register Map 460
13-11 ACPI and Legacy I/O Register Map 461
13-12 TCO I/O Register Address Map 483
13-13 Registers to Control GPIO Address Map 491
14-1 SATA Controller PCI Register Address Map (SATA–D31:F2) 501
14-2 Bus Master IDE I/O Register Address Map 528
14-3 AHCI Register Address Map 536
14-4 Generic Host Controller Register Address Map 537
14-5 Port [5:0] DMA Register Address Map 545
15-1 SATA Controller PCI Register Address Map (SATA–D31:F5) 563
15-2 Bus Master IDE I/O Register Address Map 580
16-1 UHCI Controller PCI Configuration Map 589
16-2 UHCI Controller PCI Register Address Map (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2) 589
16-3 USB I/O Registers 602
16-4 Run/Stop, Debug Bit Interaction SWDBG (Bit 5), Run/Stop (Bit 0) Operation 605
17-1 USB EHCI PCI Register Address Map (USB EHCI—D29:F7, D26:F7) 611
17-2 Enhanced Host Controller Capability Registers 631
17-3 Enhanced Host Controller Operational Register Address Map 635
17-4 Debug Port Register Address Map 649
18-1 Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) 653
18-2 Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) 675
19-1 SMBus Controller PCI Register Address Map (SMBus—D31:F3) 703
19-2 SMBus I/O and Memory Mapped I/O Register Address Map 710
20-1 PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5) 721
21-1 Memory-Mapped Registers 767
22-1 Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) 777
22-2 Gigabit LAN SPI Flash Program Register Address Map (GbE LAN Memory Mapped Configuration Registers) 815
23-1 Thermal Sensor Register Address Map 829
23-2 Thermal Memory Mapped Configuration Register Address Map 838

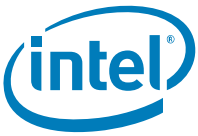


Revision History

Revision Number	Description	Revision Date
-001	• Initial release.	June 2008
-002	• Added Intel ICH10 corporate components • Added Notes 12 and 13 to Table 2-23, updated signal description for VccGLAN1_5 and VccGLAN3_3 in Table 2-24, and updated GPIO33 and GPIO49 strap definitions in Table 2-25. • Updated register descriptions for USBIR1 (Section 10.1.82), USBIR2 (Section 10.1.83), and EHCIIR1 (Section 17.1.30)	September 2008
-003	• Updated Intel ICH10 corporate components table	October 2008

Intel® ICH10 Features

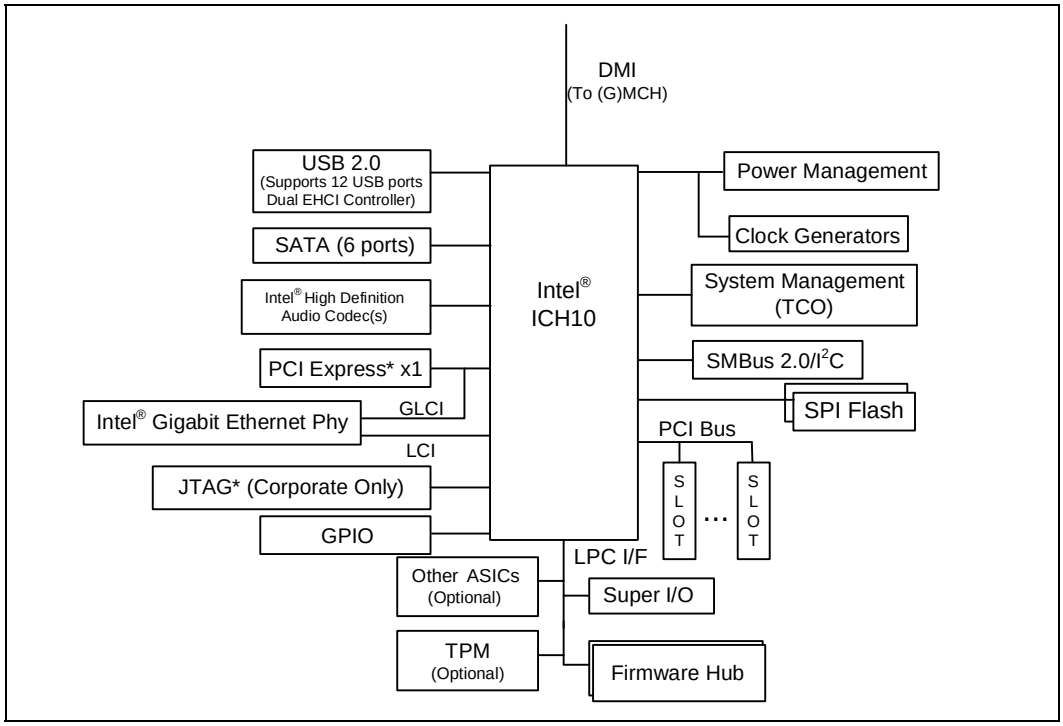
- Direct Media Interface
  - 10 Gb/s each direction, full duplex
  - Transparent to software
- PCI Express*
  - 6 PCI Express root ports
  - Supports PCI Express 1.1
  - Ports 1-4 can be statically configured as 4x1, or 1x4
  - Support for full 2.5 Gb/s bandwidth in each direction per x1 lane
  - Module based Hot-Plug supported (e.g., ExpressCard*)
- PCI Bus Interface
  - Supports PCI Rev 2.3 Specification at 33 MHz
  - Four available PCI REQ/GNT pairs
  - Support for 64-bit addressing on PCI using DAC protocol
- Integrated Serial ATA Host Controller
  - Up to six SATA ports
  - Data transfer rates up to 3.0 Gb/s (300 MB/s).
  - Integrated AHCI controller
- External SATA support
  - Port Disable Capability
- Intel® Matrix Storage Technology
  - Configures the ICH10 SATA controller as a RAID controller supporting RAID 0/1/5/10
- Intel® High Definition Audio Interface
  - PCI Express endpoint
  - Independent Bus Master logic for eight general purpose streams: four input and four output
  - Support four external Codecs
  - Supports variable length stream slots
  - Supports multichannel, 32-bit sample depth, 192 kHz sample rate output
  - Provides mic array support
  - Allows for non-48 kHz sampling output
  - Support for ACPI Device States
  - Low Voltage Mode
- Intel® Quiet System Technology
  - Four TACH signals and three PWM signals
  - Improved algorithms for better performance
- Simple Serial Transport (SST) 1.0 Bus and Platform Environment Control Interface (PECI)
- USB 2.0
  - Six UHCI Host Controllers, supporting up to twelve external ports
  - Two EHCI Host Controllers, supporting up to twelve external ports
  - Two Configuration Options for EHCI Controllers 6+6 and 8+4
  - Per-Port-Disable Capability
  - Includes up to two USB 2.0 High-speed Debug Ports
  - Supports wake-up from sleeping states S1-S4 Supports legacy Keyboard/Mouse software
- Integrated Gigabit LAN Controller
  - Integrated ASF Management Controller
  - Network security with System Defense
  - Supports IEEE 802.3
  - LAN Connect Interface (LCI) and Gigabit LAN Connect Interface (GLCI)
  - 10/100/1000 Mbps Ethernet Support
  - Jumbo Frame Support
- Intel® Active Management Technology with System Defense (Corporate Only)
  - Network Outbreak Containment Heuristics
- Intel® I/O Virtualization (VT-d) Support
- Intel® Trusted Execution Technology (Intel TXT) Support (Corporate Only)
- Power Management Logic
  - Supports ACPI 3.0b
  - ACPI-defined power states (C1, C2, C3, C4, S1, S3-S5)
  - ACPI Power Management Timer
  - SMI# generation
  - All registers readable/restorable for proper resume from 0 V suspend states
  - Support for APM-based legacy power management for non-ACPI implementations
- External Glue Integration
  - Integrated Pull-up, Pull-down and Series Termination resistors on processor I/F
  - Integrated Pull-down and Series resistors on USB
- Enhanced DMA Controller
  - Two cascaded 8237 DMA controllers
  - Supports LPC DMA



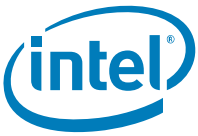
- SMBus
  - — Faster speed, up to 100 kbps
  - — Flexible SMBus/SMLink architecture to optimize for ASF
  - — Provides independent manageability bus through SMLink interface
  - — Supports SMBus 2.0 Specification
  - — Host interface allows processor to communicate via SMBus
  - — Slave interface allows an internal or external Microcontroller to access system resources
  - — Compatible with most two-wire components that are also I^2C compatible
- High Precision Event Timers
  - — Advanced operating system interrupt scheduling
- Timers Based on 82C54
  - — System timer, Refresh request, Speaker tone output
- Real-Time Clock
  - — 256 Byte battery-backed CMOS RAM
  - — Integrated oscillator components
  - — Lower Power DC/DC Converter implementation
- System TCO Reduction Circuits
  - — Timers to generate SMI# and Reset upon detection of system hang
  - — Timers to detect improper processor reset
  - — Integrated processor frequency strap logic
  - — Supports ability to disable external devices
- Interrupt Controller
  - — Supports up to eight PCI interrupt pins
  - — Supports PCI 2.3 Message Signaled Interrupts
  - — Two cascaded 82C59 with 15 interrupts
  - — Integrated I/O APIC capability with 24 interrupts
  - — Supports Processor System Bus interrupt delivery
- 1.1 V operation with 1.5 and 3.3 V I/O
  - — 5 V tolerant buffers on PCI, USB and selected Legacy signals
- 1.1 V Core Voltage
- Five Integrated Voltage Regulators for different power rails
- Firmware Hub I/F supports BIOS Memory size up to 8 MBytes
- Serial Peripheral Interface (SPI)
  - — Supports up to two SPI devices
  - — Supports 20 MHz and 33 MHz SPI devices
  - — NEW: Dual erase support
- Low Pin Count (LPC) I/F
  - — Supports two Master/DMA devices.
  - — Support for Security Device (Trusted Platform Module) connected to LPC.
- GPIO
  - — TTL, Open-Drain, Inversion
  - — GPIO lock down
- NEW: JTAG (Corporate Only)
  - — Boundary Scan for testing during board manufacturing
- Package 31x31 mm 676 mBGA

Note: Not all features are available on all ICH10 components. See Section 1.3 for more details.

Intel® ICH10 Configuration



§ §



1 Introduction

This document is intended for Original Equipment Manufacturers and BIOS vendors creating Intel® I/O Controller Hub 10 (ICH10) Family based products. This document is for the following components:

Consumer Family

- Intel® 82801JIB ICH10 Consumer Base (ICH10)
- Intel® 82801JIR ICH10 RAID (ICH10R)

Corporate Family

- Intel® 82801JD ICH10 Corporate Base (ICH10D)
- Intel® 82801JDO ICH10 Digital Office (ICH10DO)

Section 1.3 provides high-level feature differences for the ICH10 Family components.

Note: Throughout this document, ICH10 is used as a general ICH10 term and refers to the Intel 82801JIB ICH10, Intel 82801JIR ICH10R, Intel 82801JD ICH10D, Intel 82801JDO ICH10DO components, unless specifically noted otherwise.

Note: Throughout this document, the term “Consumer Only” refers to information that is for the Intel 82801JIB ICH10 and Intel 82801JIR ICH10R, unless specifically noted otherwise. The term “Corporate Only” refers to information that is for the Intel 82801JD ICH10D and 82801JDO ICH10DO, unless specifically noted otherwise.

1.1 About This Manual

This manual assumes a working knowledge of the vocabulary and principles of PCI Express*, USB, AHCI, SATA, Intel® High Definition Audio (Intel® HD Audio), SMBus, PCI, ACPI, and LPC. Although some details of these features are described within this manual, refer to the individual industry specifications listed in Table 1-1 for the complete details.

Table 1-1. Industry Specifications

Specification	Location
PCI Express* Base Specification, Revision 1.1	http://www.pcisig.com/specifications
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Power Management Specification, Revision 1.1	http://www.pcisig.com/specifications
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs
Advanced Configuration and Power Interface, Version 3.0b (ACPI)	http://www.acpi.info/spec.htm
Universal Host Controller Interface, Revision 1.1 (UHCI)	http://developer.intel.com/design/USB/UHCI11D.htm

Table 1-1. Industry Specifications

Specification	Location
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Serial ATA Specification, Revision 2.5	http://www.serialata.org/specifications.asp
Serial ATA II: Extensions to Serial ATA 1.0, Revision 1.0	http://www.serialata.org/specifications.asp
Serial ATA II Cables and Connectors Volume 2 Gold	http://www.serialata.org/specifications.asp
Alert Standard Format Specification, Version 1.03	http://www.dmtf.org/standards/asf
IEEE 802.3 Fast Ethernet	http://standards.ieee.org/getieee802/
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
IA-PC HPET (High Precision Event Timers) Specification, Revision 0.98a	http://www.intel.com/hardwaredesign/hpetspec.htm
TPM Specification 1.02, Level 2 Revision 103	http://www.trustedcomputinggroup.org/specs/TPM
Intel® I/O Controller Hub 10 (ICH10) Family Specification Update	http://www.intel.com/design/chipsets/specupdt/319974.pdf
Intel® I/O Controller Hub 10 (ICH10) Family Thermal and Mechanical Design Guidelines	http://www.intel.com/design/chipsets/designex/319975.pdf
Intel® ICH10 EDS Spec. Update, Latest Revision	**Intel Users:** http://esales.intel.com Search for “ICH10” **External Users**: http://www.intel.com/ibl Chipsets > South Bridges/IO Controller Hub > ICH Family > ICH10 > Technical
Intel® ICH10 Chipset Mechanical Ballout File, Latest Revision *Intel® ICH10 Family XOR Chains In-Circuit Tester Package,* Revision *TBD* *Intel® ICH10 IBIS Model*, Revision Latest Revision	**Intel Users:** http://esales.intel.com Search for “ICH10” **External Users**: http://www.intel.com/ibl Chipsets > South Bridges/IO Controller Hub > ICH Family > ICH10 > Technical

Chapter 1. Introduction
Chapter 1 introduces the ICH10 and provides information on manual organization and gives a general overview of the ICH10.

Chapter 2. Signal Description
Chapter 2 provides a block diagram of the ICH10 and a detailed description of each signal. Signals are arranged according to interface and details are provided as to the drive characteristics (Input/Output, Open-drain, etc.) of all signals.

Chapter 3. Intel® ICH10 Pin States
Chapter 3 provides a complete list of signals, their associated power well, their logic level in each suspend state, and their logic level before and after reset.

Chapter 4. Intel® ICH10 and System Clock Domains
Chapter 4 provides a list of each clock domain associated with the ICH10 in an ICH10 based system.

Chapter 5. Functional Description
Chapter 5 provides a detailed description of the functions in the ICH10. All PCI buses, devices and functions in this manual are abbreviated using the following nomenclature; Bus:Device:Function. This manual abbreviates buses as B0 and B1, devices as D8, D27, D28, D29, D30 and D31 and functions as F0, F1, F2, F3, F4, F5, F6 and F7. For example Device 31 Function 0 is abbreviated as D31:F0, Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. Note that the ICH10's external PCI bus is typically Bus 1, but may be assigned a different number depending upon system configuration.

Chapter 6. Ballout Definition
Chapter 6 provides a table of each signal and its ball assignment in the 676-mBGA package.

Chapter 7. Package Information
Chapter 7 provides drawings of the physical dimensions and characteristics of the 676-mBGA package.

Chapter 8. Electrical Characteristics
Chapter 8 provides all AC and DC characteristics including detailed timing diagrams.

Chapter 9. Register and Memory Mappings
Chapter 9 provides an overview of the registers, fixed I/O ranges, variable I/O ranges and memory ranges decoded by the ICH10.

Chapter 10. Chipset Configuration Registers
Chapter 10 provides a detailed description of all registers and base functionality that is related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express*). It contains the root complex register block, which describes the behavior of the upstream internal link.

Chapter 11. PCI-to-PCI Bridge Registers
Chapter 11 provides a detailed description of all registers that reside in the PCI-to-PCI bridge. This bridge resides at Device 30, Function 0 (D30:F0).

Chapter 12. Integrated LAN Controller Registers
Chapter 12 provides a detailed description of all registers that reside in the ICH10's integrated LAN controller. The integrated LAN Controller resides at Device 25, Function 0 (D25:F0).

Chapter 13. LPC Bridge Registers
Chapter 13 provides a detailed description of all registers that reside in the LPC bridge. This bridge resides at Device 31, Function 0 (D31:F0). This function contains registers for many different units within the ICH10 including DMA, Timers, Interrupts, Processor Interface, GPIO, Power Management, System Management and RTC.

Chapter 14. SATA Controller Registers
Chapter 14 provides a detailed description of all registers that reside in the SATA controller #1. This controller resides at Device 31, Function 2 (D31:F2).

Chapter 15. SATA Controller Registers
Chapter 15 provides a detailed description of all registers that reside in the SATA controller #2. This controller resides at Device 31, Function 5 (D31:F5).

Chapter 16. UHCI Controller Registers
Chapter 16 provides a detailed description of all registers that reside in the six UHCI host controllers. These controllers reside at Device 29, Functions 0, 1, 2, and 3 (D29:F0/F1/F2/F3) and Device 26, Function 0, 1 and 2 (D26:F0/F1/F2).

Chapter 17. EHCI Controller Registers
Chapter 17 provides a detailed description of all registers that reside in the two EHCI host controllers. These controllers reside at Device 29, Function 7 (D29:F7) and Device 26, Function 7 (D26:F7).

Chapter 18. SMBus Controller Registers
Chapter 19 provides a detailed description of all registers that reside in the SMBus controller. This controller resides at Device 31, Function 3 (D31:F3).

Chapter 19. Intel® High Definition Audio Controller Registers
Chapter 18 provides a detailed description of all registers that reside in the Intel High Definition Audio controller. This controller resides at Device 27, Function 0 (D27:F0).

Chapter 20. PCI Express* Port Controller Registers
Chapter 20 provides a detailed description of all registers that reside in the PCI Express controller. This controller resides at Device 28, Functions 0 to 5 (D30:F0-F5).

Chapter 21. High Precision Event Timers Registers
Chapter 21 provides a detailed description of all registers that reside in the multimedia timer memory mapped register space.

Chapter 22. Serial Peripheral Interface Registers
Chapter 22 provides a detailed description of all registers that reside in the SPI memory mapped register space.

Chapter 23. Thermal Sensors
Chapter 23 provides a detailed description of all registers that reside in the thermal sensors PCI configuration space. The registers reside at Device 31, Function 6 (D31:F6).

1.2 Overview

The ICH10 provides extensive I/O support. Functions and capabilities include:

- *PCI Express* Base Specification,* Revision 1.1 support
- *PCI Local Bus Specification*, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 3.0b
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
- USB host interface with support for up to twelve USB ports; six UHCI host controllers; two EHCI high-speed USB 2.0 Host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- *System Management Bus (SMBus) Specification*, Version 2.0 with additional support for I^2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Matrix Storage Technology
- Supports Intel® Active Management Technology (Corporate Only)
- Supports Intel® Virtualization Technology for Directed I/O
- Supports Intel® Trusted Execution Technology (Corporate Only)
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- Intel® Quiet System Technology
- Integrated TPM 1.2 (Corporate Only)
- JTAG Boundary Scan support (Corporate Only)

The Intel ICH10 incorporates a variety of PCI devices and functions, as shown in Table 1-2. They are divided into seven logical devices. The first is the DMI-To-PCI bridge (Device 30). The second device (Device 31) contains most of the standard PCI functions that always existed in the PCI-to-ISA bridges (South Bridges), such as the Intel PIIX4. The third and fourth (Device 29 and Device 26) are the USB host controller devices. The fifth (Device 28) is PCI Express device. The sixth (Device 27) is the HD Audio controller device, and the seventh (Device 25) is the Gigabit Ethernet controller device.

Table 1-2. PCI Devices and Functions (Sheet 1 of 2)

Bus:Device:Function	Function Description
Bus 0:Device 30:Function 0	DMI-to-PCI Bridge
Bus 0:Device 31:Function 0	LPC Controller[1]
Bus 0:Device 31:Function 2	SATA Controller #1
Bus 0:Device 31:Function 5	SATA Controller #2[3]
Bus 0:Device 31:Function 6	Thermal Subsystem
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 29:Function 0	USB FS/LS UHCI Controller #1

Table 1-2. PCI Devices and Functions (Sheet 2 of 2)

Bus:Device:Function	Function Description
Bus 0:Device 29:Function 1	USB FS/LS UHCI Controller #2
Bus 0:Device 29:Function 2	USB FS/LS UHCI Controller #3
Bus 0:Device 29:Function 3	USB FS/LS UHCI Controller #6[2]
Bus 0:Device 29:Function 7	USB HS EHCI Controller #1
Bus 0:Device 26:Function 0	USB FS/LS UHCI Controller #4
Bus 0:Device 26:Function 1	USB FS/LS UHCI Controller #5
Bus 0:Device 26:Function 2	USB FS/LS UHCI Controller #6[2]
Bus 0:Device 26:Fucntion 7	USB HS EHCI Controller #2
Bus 0:Device 28:Function 0	PCI Express* Port 1
Bus 0:Device 28:Function 1	PCI Express Port 2
Bus 0:Device 28:Function 2	PCI Express Port 3
Bus 0:Device 28:Function 3	PCI Express Port 4
Bus 0:Device 28:Function 4	PCI Express Port 5
Bus 0:Device 28:Function 5	PCI Express Port 6
Bus 0:Device 27:Function 0	Intel® High Definition Audio Controller
Bus 0:Device 25:Function 0	Gigabit Ethernet Controller

NOTES:
1. The PCI-to-LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, and DMA
2. Device 26:Function 2 maybe configured as Device 29:Function 3 during BIOS Post.
3. SATA Controller 2 is only visible when D31:F2 CC.SCC=01h.

1.2.1 Capability Overview

The following sub-sections provide an overview of the ICH10 capabilities.

Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the Memory Controller Hub / Graphics Memory Controller Hub ((G)MCH) and I/O Controller Hub 10 (ICH10). This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

PCI Express* Interface

The ICH10 provides up to 6 PCI Express Root Ports, supporting the *PCI Express Base Specification,* Revision 1.1. Each Root Port supports 2.5 GB/s bandwidth in each direction (5 GB/s concurrent). PCI Express Root Ports 1–4 can be statically configured as four x1 Ports or ganged together to form one x4 port. Ports 5 and 6 can only be used as two x1 ports.

Note: The integrated Gigabit Ethernet controllers data lines for 1000 MB/s speed are multiplexed with PCI Express* Root Port 6 and therefore unavailable if a Gigabit Ethernet PHY is connected. The use of a 10/100 MB/s PHY does not consume PCI Express Root Port 6 and therefore the port is available to be utilized as a x1 Port.

Serial ATA (SATA) Controller

The ICH10 has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 3.0 GB/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The ICH10 supports the *Serial ATA Specification*, Revision 1.0a. The ICH10 also supports several optional sections of the Serial ATA II: Extensions to *Serial ATA 1.0 Specification*, Revision 1.0 (AHCI support is required for some elements).

AHCI

The ICH10 provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (e.g., an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware. See Section 1.3 for details on component feature availability.

Intel® Matrix Storage Technology

The ICH10 provides support for Intel® Matrix Storage Technology, providing both AHCI (see above for details on AHCI) and integrated RAID functionality. The industry-leading RAID capability provides high-performance RAID 0, 1, 5, and 10 functionality on up to 6 SATA ports of ICH10. Matrix RAID support is provided to allow multiple RAID levels to be combined on a single set of hard drives, such as RAID 0 and RAID 1 on two disks. Other RAID features include hot spare support, SMART alerting, and RAID 0 auto replace. Software components include an Option ROM for pre-boot configuration and

boot functionality, a Microsoft Windows* compatible driver, and a user interface for configuration and management of the RAID capability of ICH10. See Section 1.3 for details on component feature availability.

PCI Interface

The ICH10 PCI interface provides a 33 MHz, Revision 2.3 implementation. The ICH10 integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal ICH10 requests. This allows for combinations of up to four PCI down devices and PCI slots.

Low Pin Count (LPC) Interface

The ICH10 implements an LPC Interface as described in the *LPC 1.1 Specification*. The Low Pin Count (LPC) bridge function of the ICH10 resides in PCI Device 31:Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

Serial Peripheral Interface (SPI)

The ICH10 implements an SPI Interface as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for the FWH, and is required to support Gigabit Ethernet, Intel® Active Management Technology, and integrated Intel® Quiet System Technology. The ICH10 supports up to two SPI flash devices with speed up to 33 MHz using two chip select pins.

Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers. Channel 4 is reserved as a generic bus master request.

The ICH10 supports LPC DMA, which is similar to ISA DMA, through the ICH10's DMA controller. LPC DMA is handled through the use of the LDRQ# lines from peripherals and special encoding on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

The ICH10 provides an ISA-Compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two, 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the ICH10 supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA compatible Programmable Interrupt controller (PIC) described in the previous section, the ICH10 incorporates the Advanced Programmable Interrupt Controller (APIC).

Universal Serial Bus (USB) Controllers

The ICH10 contains up to two Enhanced Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The ICH10 also contains up to six Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The ICH10 supports up to twelve USB 2.0 ports. All twelve ports are high-speed, full-speed, and low-speed capable. ICH10's port-routing logic determines whether a USB port is controlled by one of the UHCI or EHCI controllers. See Section 5.18 and Section 5.19 for details.

Gigabit Ethernet Controller

The Gigabit Ethernet Controller provides a system interface via a PCI function. The controller provides a full memory-mapped or IO mapped interface along with a 64 bit address master support for systems using more than 4 GB of physical memory and DMA (Direct Memory Addressing) mechanisms for high performance data transfers. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large configurable transmit and receive FIFOs (up to 20 KB each) help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS).

The LAN controller can operate at multiple speeds (10/100/1000 MB/s) and in either full duplex or half duplex mode. In full duplex mode the LAN controller adheres with the *IEEE 802.3x Flow Control* Specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism. See Section 5.3 for details.

RTC

The ICH10 contains a Motorola MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3 V battery.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on ICH10 configuration.

Enhanced Power Management

The ICH10's power management functions include enhanced clock control and various low-power (suspend) states (e.g., Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The ICH10 contains full support for the *Advanced Configuration and Power Interface (ACPI) Specification,* Revision 3.0a.

Intel® Active Management Technology (Intel® AMT) (Not available on all ICH10 components)

Intel® Active Management Technology is the next generation of client manageability via the wired network. Intel AMT is a set of advanced manageability features developed as a direct result of IT customer feedback gained through Intel market research. With the new implementation of System Defense in ICH10, the advanced manageability feature set of Intel AMT is further enhanced. See Section 1.3 for details on component feature availability.

Manageability

In addition to Intel AMT, ICH10 integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

- **TCO Timer.** The ICH10's integrated programmable TCO timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.
- **Processor Present Indicator.** The ICH10 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH10 will reboot the system.
- **ECC Error Reporting.** When detecting an ECC error, the host controller has the ability to send one of several messages to the ICH10. The host controller can instruct the ICH10 to generate either an SMI#, NMI, SERR#, or TCO interrupt.
- **Function Disable.** The ICH10 provides the ability to disable the following integrated functions: LAN, USB, LPC, Intel HD Audio, SATA, PCI Express or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.
- **Intruder Detect.** The ICH10 provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH10 can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

System Management Bus (SMBus 2.0)

The ICH10 contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. Special I^2C commands are implemented.

The ICH10's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the ICH10 supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification,* Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

ICH10's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

Intel® High Definition Audio Controller

The *Intel® High Definition Audio Specification* defines a digital interface that can be used to attach different types of codecs, such as audio and modem codecs. The ICH10 Intel® HD Audio controller supports up to 4 codecs. The link can operate at either 3.3 V or 1.5 V.

With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel® HD Audio controller provides audio quality that can deliver CE levels of audio experience. On the input side, the ICH10 adds support for an array of microphones.

Intel® Quiet System Technology (Intel® QST)

The ICH10 integrates four fan speed sensors (four TACH signals) and 3 fan speed controllers (three Pulse Width Modulator signals), which enables monitoring and controlling up to four fans on the system. With the new implementation of the single-wire Simple Serial Transport (SST) 1.0 bus and Platform Environmental Control Interface (PECI), the ICH10 provides an easy way to connect to SST-based thermal sensors and access the processor thermal data. In addition, coupled with the new sophisticated fan speed control algorithms, Intel® QST provides effective thermal and acoustic management for the platform.

Note: Intel® Quiet System Technology functionality requires a correctly configured system, including an appropriate (G)MCH with Intel ME, Intel ME firmware, and system BIOS support.

Intel® Trusted Platform Module (Corporate Only)

The Intel Trusted Platform Module (Intel® TPM) implementation consists of firmware, Intel® Management Engine resources and dedicated hardware within the ICH and the (G)MCH. The Intel TPM supports all requirements of the TPM Specification Version 1.2, Revision 103, as published by the Trusted Computing Group. The Intel TPM behaves like a discrete TPM device, and can support third party applications, as well as Microsoft* specific functionality in the Windows Vista* OS.

Note: Intel TPM functionality requires a correctly configured system, including an appropriate (G)MCH with Intel Management Engine firmware, ICH10 and SPI Flash.

JTAG Boundary-Scan (Corporate Only)

ICH10 adds the industry standard JTAG interface and enables Boundary-Scan in place of the XOR chains used in previous generations of the ICH. Boundary-Scan can be used to ensure device connectivity during the board manufacturing process. The JTAG interface allows system manufacturers to improve efficiency by using industry available tools to test the ICH on an assembled board. Since JTAG is a serial interface, it eliminates the need to create probe points for every pin in an XOR chain. This eases pin breakout and trace routing and simplifies the interface between the system and a bed-of-nails tester.

Note: Contact your local Intel Field Sales Representative for additional information about JTAG usage on ICH10.

1.3 Intel® ICH10 Family High-Level Component Differences

Table 1-3. Intel® ICH10 Components

Feature		Consumer		Corporate	
		ICH10	ICH10R	ICH10D	ICH10DO
Component Name		ICH10 Consumer Base	ICH10 RAID	ICH10 Corporate Base	ICH10 Digital Office
Intel® Turbo Memory Support		No	Yes	No	No
Intel® Matrix Storage Technology	AHCI	No[3]	Yes	Yes	Yes
	RAID 0/1/5/10 Support	No	Yes	No	Yes
Intel® Active Management Technology Release 5.0	Basic	No	No	Yes	No
	Professional	No	No	No	Yes
Intel® Trusted Platform Module (Intel® TPM)		No	No	Yes	Yes
Wake on VoIP		Yes[4]	Yes[4]	No	No
Intel® Viiv™ Processor Technology Support		Yes	Yes	No	No
Intel® Remote Wake Technology (Intel® RWT) Support		Yes	Yes	No	No
JTAG Boundary Scan		No	No	Yes	Yes

NOTES:
1. Contact your local Intel Field Sales Representative for currently available ICH10 components.
2. Table above shows feature difference between ICH10 components. If a feature is not listed in the table it is considered a Base feature that is included in all components.
3. ICH10 Consumer Base provides hardware support for AHCI functionality when enabled by appropriate system configuration and software driver.
4. Wake on VoIP support provided by Intel® Remote Wake Technology (Intel® RWT) Support.
5. All components support 6 SATA, 6 PCIe*, and 14 USB ports.

§ §

2 Signal Description

This chapter provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

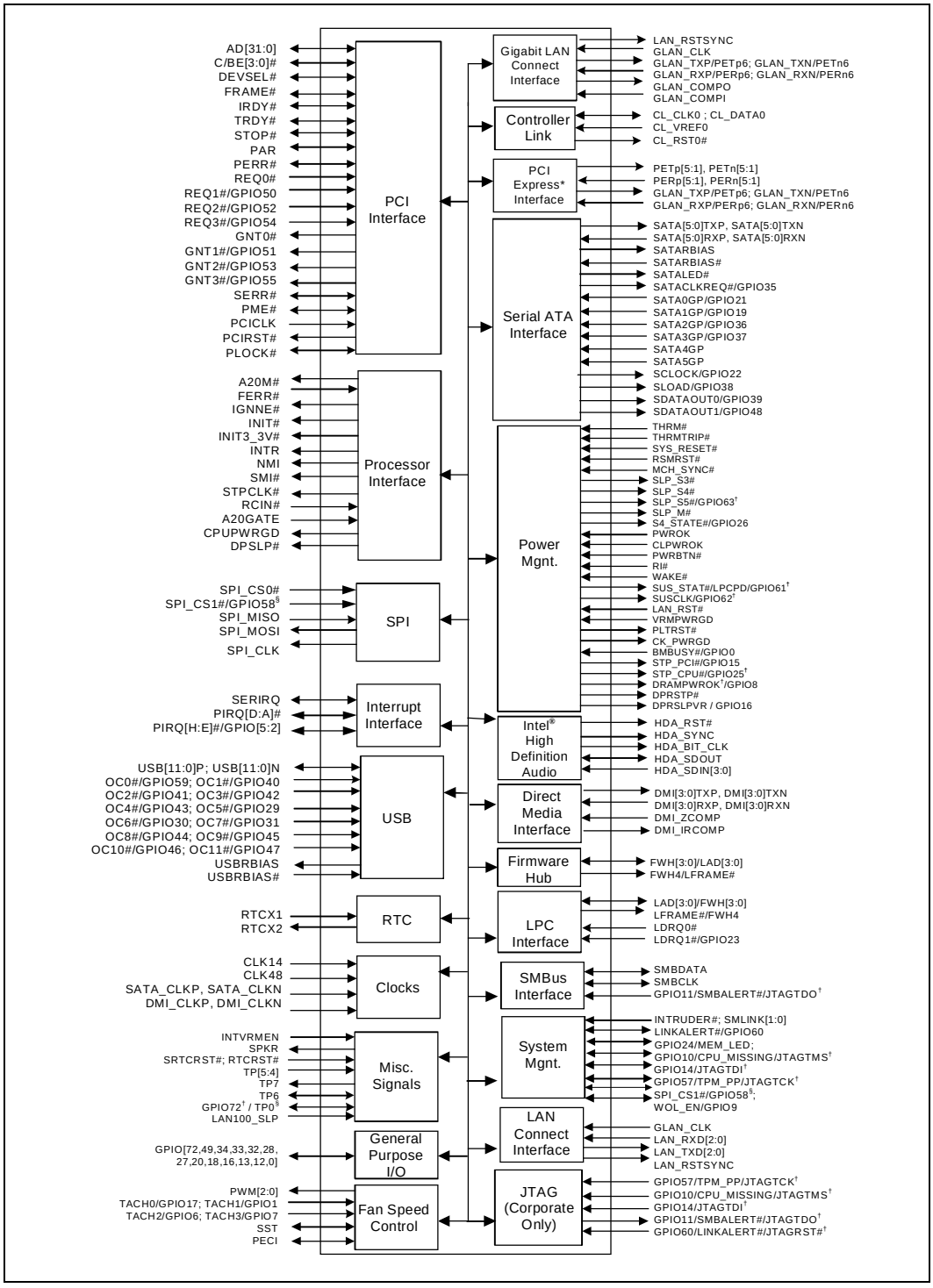
The "#" symbol at the end of the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input Pin
O	Output Pin
OD O	Open-drain Output Pin.
I/OD	Bi-directional Input/Open-drain Output Pin.
I/O	Bi-directional Input / Output Pin.

The "Type" for each signal is indicative of the functional operating mode of the signal. Unless otherwise noted in Section 3.2 or Section 3.3, a signal is considered to be in the functional operating mode after RTCRST# deasserts for signals in the RTC well, after RSMRST# deasserts for signals in the suspend well, after PWROK asserts for signals in the core well, and after LAN_RST# deasserts for signals in the LAN well.

Figure 2-1. Intel® ICH10 Interface Signals Block Diagram



NOTES:

1. § symbol indicates a particular use of a pin is Cunsumer Only.
2. † symbol indicates a particular use of a pin is Corporate Only.

2.1 Direct Media Interface (DMI) to Host Controller

Table 2-1. Direct Media Interface Signals

Name	Type	Description
DMI0TXP, DMI0TXN	O	**Direct Media Interface Differential Transmit Pair 0**
DMI0RXP, DMI0RXN	I	**Direct Media Interface Differential Receive Pair 0**
DMI1TXP, DMI1TXN	O	**Direct Media Interface Differential Transmit Pair 1**
DMI1RXP, DMI1RXN	I	**Direct Media Interface Differential Receive Pair 1**
DMI2TXP, DMI2TXN	O	**Direct Media Interface Differential Transmit Pair 2**
DMI2RXP, DMI2RXN	I	**Direct Media Interface Differential Receive Pair 2**
DMI3TXP, DMI3TXN	O	**Direct Media Interface Differential Transmit Pair 3**
DMI3RXP, DMI3RXN	I	**Direct Media Interface Differential Receive Pair 3**
DMI_ZCOMP	I	**Impedance Compensation Input:** Determines DMI input impedance.
DMI_IRCOMP	O	**Impedance/Current Compensation Output:** Determines DMI output impedance and bias current.

2.2 PCI Express* Interface

Table 2-2. PCI Express* Signals

Name	Type	Description
PETp1, PETn1	O	**PCI Express* Differential Transmit Pair 1**
PERp1, PERn1	I	**PCI Express Differential Receive Pair 1**
PETp2, PETn2	O	**PCI Express Differential Transmit Pair 2**
PERp2, PERn2	I	**PCI Express Differential Receive Pair 2**
PETp3, PETn3	O	**PCI Express Differential Transmit Pair 3**
PERp3, PERn3	I	**PCI Express Differential Receive Pair 3**
PETp4, PETn4	O	**PCI Express Differential Transmit Pair 4**
PERp4, PERn4	I	**PCI Express Differential Receive Pair 4**
PETp5, PETn5	O	**PCI Express Differential Transmit Pair 5**
PERp5, PERn5	I	**PCI Express Differential Receive Pair 5**
PETp6/ GLAN_TXp, **PETn6**/ GLAN_TXn	O	**PCI Express Differential Transmit Pair 6:** The differential pair will function as the Gigabit LAN Connect Interface transmit pair when the integrated Gigabit LAN controller is enabled.
PERp6/ GLAN_RXp, **PERn6**/ GLAN_RXn	I	**PCI Express Differential Receive Pair 6:** The differential pair will function as the Gigabit LAN Connect Interface receive pair when the integrated Gigabit LAN controller is enabled.

2.3 LAN Connect Interface

Table 2-3. LAN Connect Interface Signals

Name	Type	Description
GLAN_CLK	I	**Gigabit LAN Input Clock:** Clock driven by the Platform LAN Connect device. The frequency will vary depending on link speed. **NOTE:** The clock is shared between the LAN Connect Interface and the Gigabit LAN Connect Interface.
LAN_RXD[2:0]	I	**Received Data:** The Platform LAN Connect device uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.

Table 2-3. LAN Connect Interface Signals

Name	Type	Description
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN controller uses these signals to transfer data and control information to the Platform LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** This is the reset/sync signal from the LAN Connect Interface to the physical device. The Platform LAN Connect device's Reset and Sync signals are multiplexed onto this pin. **NOTE:** The signal is shared between LAN Connect Interface and Gigabit LAN Connect Interface.
LAN_PHY_PWR_CTRL / GPIO12	O	**LAN PHY Power Control:** This signal may optionally be connected to a switch to turn 3.3 V PHY power off when LAN is disabled for additional power savings. This capability is configured in the NVM. When using an 82567 PHY solution, the LAN_PHY_PWR_CTRL signal should be connected to the PHY's LAN_DISABLE_N pin for a hardware based LAN disable mechanism. Signal can instead be used as GPIO12.

2.4 Gigabit LAN Connect Interface

Table 2-4. Gigabit LAN Connect Interface Signals

Name	Type	Description
GLAN_CLK	I	**Gigabit LAN Input Clock:** Clock driven by the Platform LAN Connect device. The frequency will vary depending on link speed. **NOTE:** The clock is shared between the LAN Connect Interface and the Gigabit LAN Connect Interface.
GLAN_TXp/PETp6; **GLAN_TXn**/PETn6	O	**Gigabit LAN Differential Transmit Pair.** Can be instead used as PCI Express port 6 differential transmit pair.
GLAN_RXp/PERp6; **GLAN_RXn**/PERn6	I	**Gigabit LAN Differential Receive Pair**. Can be instead used as PCI Express port 6 differential receive pair.
GLAN_COMPO	O	**Impedance Compensation Output pad:** Determines Gigabit LAN Connect Interface output impedance and bias current.
GLAN_COMPI	I	**Impedance Compensation Input pad:** Determines Gigabit LAN Connect Interface input impedance.
LAN_RSTSYNC	O	**LAN Reset/Sync:** This is the reset/sync signal from the Gigabit LAN interface to the physical device. The Platform LAN Connect device's Reset and Sync signals are multiplexed onto this pin. **NOTE:** The signal is shared between LAN Connect Interface and Gigabit LAN Connect Interface.

2.5 Firmware Hub Interface

Table 2-5. Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** These signals are multiplexed with the LPC address signals.
FWH4 / LFRAME#	O	**Firmware Hub Signals.** This signal is multiplexed with the LPC LFRAME# signal.
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.

2.6 PCI Interface

Table 2-6. PCI Interface Signals (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data**: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel ICH10will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables**: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH10 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select**: The ICH10 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH10 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH10 address or an address destined for DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH10-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH10 until driven by a target device.

Table 2-6. PCI Interface Signals (Sheet 2 of 3)

Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH10 when the ICH10 is the target, and FRAME# is an output from the ICH10 when the ICH10 is the initiator. FRAME# remains tri-stated by the ICH10 until driven by an initiator.
IRDY#	I/O	**Initiator Ready**: IRDY# indicates the ICH10's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH10 has valid data present on AD[31:0]. During a read, it indicates the ICH10 is prepared to latch data. IRDY# is an input to the ICH10 when the ICH10 is the target and an output from the ICH10 when the ICH10 is an initiator. IRDY# remains tri-stated by the ICH10 until driven by an initiator.
TRDY#	I/O	**Target Ready**: TRDY# indicates the ICH10's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH10, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH10, as a target is prepared to latch data. TRDY# is an input to the ICH10 when the ICH10 is the initiator and an output from the ICH10 when the ICH10 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH10 until driven by a target.
STOP#	I/O	**Stop**: STOP# indicates that the ICH10, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH10, as an initiator, to stop the current transaction. STOP# is an output when the ICH10 is a target and an input when the ICH10 is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH10 counts the number of ones within the 36 bits plus PAR and the sum is always even. The ICH10 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH10 generates PAR for address and data phases and only ensures PAR to be valid one PCI clock after the corresponding address or data phase. The ICH10 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH10 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH10 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH10 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH10 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH10 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PERR#	I/O	**Parity Error**: An external PCI device drives PERR# when it receives data that has a parity error. The ICH10 drives PERR# when it detects a parity error. The ICH10 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).

Table 2-6. PCI Interface Signals (Sheet 3 of 3)

Name	Type	Description
REQ0# **REQ1# /** GPIO50 **REQ2# /** GPIO52 **REQ3# /**GPIO54	I	**PCI Requests**: The ICH10 supports up to 4 masters on the PCI bus. REQ[3:1]# pins can instead be used as GPIO.
GNT0# **GNT1# /** GPIO51 **GNT2#**/ GPIO53 **GNT3#**/GPIO55	O	**PCI Grants**: The ICH10 supports up to 4 masters on the PCI bus. GNT[3:1]# pins can instead be used as GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. **NOTE:** GNT[3:0]# are sampled as a functional strap. See Section 2.25.1 for details.
PCICLK	I	**PCI Clock**: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	**PCI Lock**: This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH10 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	I/OD	**System Error**: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH10 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	**PCI Power Management Event**: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH10 may drive PME# active due to an internal wake event. The ICH10 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

2.7 Serial ATA Interface

Table 2-7. Serial ATA Interface Signals (Sheet 1 of 3)

Name	Type	Description
SATA0TXP **SATA0TXN**	O	**Serial ATA 0 Differential Transmit Pairs:** These are outbound high-speed differential signals to Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA0RXP **SATA0RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA1TXP **SATA1TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1.

Table 2-7. Serial ATA Interface Signals (Sheet 2 of 3)

Name	Type	Description
SATA1RXP **SATA1RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1
SATA2TXP **SATA2TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1.
SATA2RXP **SATA2RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1
SATA3TXP **SATA3TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1
SATA3RXP **SATA3RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1
SATA4TXP **SATA4TXN**	O	**Serial ATA 4 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2
SATA4RXP **SATA4RXN**	I	**Serial ATA 4 Differential Receive Pair:** These are inbound high-speed differential signals from Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2
SATA5TXP **SATA5TXN**	O	**Serial ATA 5 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2
SATA5RXP **SATA5RXN**	I	**Serial ATA 5 Differential Receive Pair:** These are inbound high-speed differential signals from Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2
SATARBIAS	O	**Serial ATA Resistor Bias:** This is an analog connection point for an external resistor to ground.
SATARBIAS#	I	**Serial ATA Resistor Bias Complement:** This is an analog connection point for an external resistor to ground.
SATA0GP / GPIO21	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to ‘0’ to indicate that the switch is closed and to ‘1’ to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.

Table 2-7. Serial ATA Interface Signals (Sheet 3 of 3)

Name	Type	Description
SATA1GP / GPIO19	I	**Serial ATA 1 General Purpose:** Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP / GPIO36	I	**Serial ATA 2 General Purpose:** Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36. **NOTE:** This signal can also be used as GPIO36.
SATA3GP / GPIO37	I	**Serial ATA 3 General Purpose:** Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37. **NOTE:** This signal can also be used as GPIO37.
SATA4GP	I	**Serial ATA 4 General Purpose:** Same function as SATA0GP, except for SATA Port 4.
SATA5GP	I	**Serial ATA 5 General Purpose:** Same function as SATA0GP, except for SATA Port 5.
SATALED#	OD O	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for details.
SATACLKREQ# /GPIO35	OD O	**Serial ATA Clock Request:** This signal is an open-drain output pin when configured as SATACLKREQ#. It is used to connect to the system clock chip. When active, request for SATA Clock running is asserted. When tri-stated, it tells the Clock Chip that SATA Clock can be stopped. An external pull-up resistor is required.
SCLOCK/ GPIO22	OD O	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. If SGPIO interface is not used, this signal can be used as a GPIO.
SLOAD/GPIO38	OD O	**SGPIO Load:** The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as a GPIO.
SDATAOUT0/ GPIO39 **SDATAOUT1**/ GPIO48	OD O	**SGPIO Dataout:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1, 2, 3, 4, 5, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPIO.

2.8 LPC Interface

Table 2-8. LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH4	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0#, LDRQ1# / GPIO23	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

2.9 Interrupt Interface

Table 2-9. Interrupt Signals

Name	Type	Description
SERIRQ	I/OD	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.

2.10 USB Interface

Table 2-10. USB Interface Signals

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port [1:0] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The Intel ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port [3:2] Differential**: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	**Universal Serial Bus Port [5:4] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP6P, USBP6N, USBP7P, USBP7N	I/O	**Universal Serial Bus Port [7:6] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP8P, USBP8N, USBP9P, USBP9N	I/O	**Universal Serial Bus Port [9:8] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 8 and 9. These ports can be routed to UHCI controller #5 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.

Table 2-10. USB Interface Signals

Name	Type	Description
USBP10P, USBP10N, USBP11P, USBP11N	I/O	**Universal Serial Bus Port [11:10] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 10 and 11. These ports can be routed to UHCI controller #6 or the EHCI controller #2. These ports can be optionally routed to EHCI Controller #1 when bit 0 RCBA 35F0h is set. **NOTE:** No external resistors are required on these signals. The ICH10 integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC0# / GPIO59 **OC1#** / GPIO40 **OC2#** / GPIO41 **OC3#** / GPIO42 **OC4#** / GPIO43 **OC5#** / GPIO29 **OC6#** / GPIO30 **OC7#** / GPIO31 **OC8#** / GPIO44 **OC9#** / GPIO45 **OC10#** / GPIO46 **OC11#** / GPIO47	I	**Overcurrent Indicators**: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[11:0]# may optionally be used as GPIOs. **NOTE:** OC[11:0]# are not 5 V tolerant.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

2.11 Power Management Interface

Table 2-11. Power Management Interface Signals (Sheet 1 of 3)

Name	Type	Description
PLTRST#	O	**Platform Reset:** The ICH10 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, TPM, etc.). The ICH10 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH10 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH10 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
THRM#	I	**Thermal Alarm:** Active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	**Thermal Trip**: When low, this signal indicates that a thermal trip from the processor occurred, and the ICH10 will immediately transition to a S5 state. The ICH10 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control**: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power in order to use the ICH10's DRAM power-cycling feature. Refer to Chapter 5.13.10.2 for details **NOTE:** In a system with Intel AMT support, this signal should be used to control the DRAM power. In M1 state (where the host platform is in S3-S5 states and the manageability sub-system is running) the signal is forced high along with SLP_M# in order to properly maintain power to the DIMM used for manageability sub-system.
SLP_S5# / GPIO63 (Corporate Only)	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states. ICH10 Corporate Family: pin may also be used as GPIO63.
SLP_M#	O	**Manageability Sleep State Control:** This signal is used to control power planes to the Intel AMT sub-system. If no Intel Management Engine firmware is present, SLP_M# will have the same timings as SLP_S3#.
S4_STATE# / GPIO26	O	**S4 State Indication:** This signal asserts low when the host platform is in S4 or S5 state. In platforms where the Intel Management Engine is forcing the SLP_S4# high along with SLP_M#, this signal can be used by other devices on the board to know when the host platform is below the S3 state.

Table 2-11. Power Management Interface Signals (Sheet 2 of 3)

Name	Type	Description
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH10 that all power rails have been stable for 99 ms and that PCICLK has been stable for 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH10 asserts PLTRST#. **NOTE:** 1. PWROK must deassert for a minimum of three RTC clock periods in order for the ICH10 to fully reset the power and properly generate the PLTRST# output. 2. PWROK must not glitch, even if RSMRST# is low.
CLPWROK	I	**Controller Link Power OK:** When asserted, indicates that power to the Controller Link subsystem (MCH, ICH, etc.) is stable and tells the ICH to de-assert CL_RST# to the (G)MCH. **NOTES:** 1. CLPWROK must not assert before RSMRST# deasserts. 2. CLPWROK must not assert after PWROK asserts.
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1–S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset**: This pin forces an internal reset after being debounced. The ICH10 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller is in reset. This signal must be asserted until the LAN power wells (VccLAN3_3 and VccLAN1_1) and VccCL3_3 power well are valid. When deasserted, this signal is an indication that the LAN power wells are stable. **NOTES:** 1. LAN_RST# must not deassert before RSMRST# deasserts 2. LAN_RST# must not deassert after PWROK asserts. 3. LAN_RST# must not deassert until 1ms after the LAN power wells (VccLAN3_3 and VccLAN1_1 and VccCL3_3 power well are valid. 4. If integrated LAN is not used LAN_RST# must be tied to Vss. 5. LAN_RST# must assert a minimum of 20 ns before LAN Power rails become inactive.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wake up.
MCH_SYNC#	I	**MCH SYNC:** This input is internally ANDed with the PWROK input. Connect to the ICH_SYNC# output of the (G)MCH.

Table 2-11. Power Management Interface Signals (Sheet 3 of 3)

Name	Type	Description
SUS_STAT# / LPCPD# / GPIO61 (Corporate Only)	O	**Suspend Status:** This signal is asserted by the ICH10 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC interface. ICH10 Corporate Family: pin may also be used as GPIO61.
SUSCLK / GPIO62 (Corporate Only)	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock. ICH10 Corporate Family: pin may also be used as GPIO62.
VRMPWRGD	I	**VRM Power Good:** This signal should be connected to the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input. This signal is in the suspend well.
DRAMPWROK (Corporate Only) / GPIO8	OD O	**DRAM Power OK:** This signal should connect to the (G)MCH's DDR3_DRAM_PWROK pin. The ICH asserts this pin to indicate when DRAM power is off. An external pull-up resistor is required. This pin is not open-drain when operating in GPIO mode.
CK_PWRGD	O	**Clock Generator Power Good**: This signal indicates to the clock generator when the main power well is valid. This signal is asserted high when both SLP_S3# and VRMPWRGD are high.
BMBUSY# / GPIO0	I	**Bus Master Busy:** This signal is used to support the C3 state. It Indicates that a bus master device is busy. When this signal is asserted, the BM_STS bit will be set. If this signal goes active in a C3 state, it is treated as a break event. **NOTE:** This signal is internally synchronized using the PCICLK and a two-stage synchronizer. It does not need to meet any particular setup or hold time. Signal may also be used as a GPIO.
STP_PCI# / GPIO15	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. It is used to support the C3 state. This signal can instead be used as a GPIO.
STP_CPU# / GPIO25 (Corporate Only)	O	**Stop CPU Clock:** This signal is an output to the external clock generator for it to turn off the processor clock. Corporate Only: This signal can instead be used as a GPIO.
DPRSTP#	O	**Deeper Stop:** This is a copy of the DPRSLPVR and it is active low.
DPRSLPVR / GPIO16	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of the VRM during the C4 state. When the signal is high, the voltage regulator outputs the lower "Deeper Sleep" voltage. When low (default), the voltage regulator outputs the higher "Normal" voltage. This signal can instead be used as a GPIO.

2.12 Processor Interface

Table 2-12. Processor Interface Signals (Sheet 1 of 2)

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH10 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1 for Consumer Family and Offset 31FEh: bit 9 for Corporate family). If FERR# is asserted, the ICH10 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH10 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1 for Consumer Family and Offset 31FEh: bit 9 for Corporate family). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the ICH10 for 16 PCI clocks to reset the processor. ICH10 can be configured to support processor Built In Self Test (BIST).
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH10 to signal to the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH10 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/ disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH10 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH10 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.

Table 2-12. Processor Interface Signals (Sheet 2 of 2)

Name	Type	Description
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH10's other sources of INIT#. When the ICH10 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH10 will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD	O	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the processor power is valid. This is an output signal that represents a logical AND of the ICH10's PWROK and VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** DPSLP# is asserted by the ICH10 to the processor. When the signal is low, the processor enters the deep sleep state by gating off the processor Core Clock inside the processor. When the signal is high (default), the processor is not in the deep sleep state.
DPSLP#	O	**Deeper Sleep:** DPSLP# is asserted by the ICH10 to the processor. When the signal is low, the processor enters the deep sleep state by gating off the processor Core Clock inside the processor. When the signal is high (default), the processor is not in the deep sleep state.

2.13 SMBus Interface

Table 2-13. SMBus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up resistor is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up resistor is required.
SMBALERT# / GPIO11 / JTAGTDO (Corporate Only)	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. ICH10 Consumer Family: This signal may be used as GPIO11. ICH10 Corporate Family: This signal may be used as GPIO11 or JTAGTDO.

2.14 System Management Interface

Table 2-14. System Management Interface Signals (Sheet 1 of 2)

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT# / GPIO60 / JTAGRST# (Corporate Only)	O OD	**SMLink Alert:** Output of the integrated LAN controller and input to either the integrated ASF, Intel AMT or an external management controller in order for the LAN's SMLINK slave to be serviced. External pull-up resistor is required. ICH10 Consumer: This signal can instead be used as a GPIO60. ICH10 Corporate: This signal can instead be used as a GPIO60 or JTAGRST#.
MEM_LED / GPIO24	O OD	**Memory LED:** Provides DRAM-powered LED control. Allows for the blinking of an LED to indicate memory activity in all power states. This functionality is configured and controlled by the Intel Management Engine. This signal can instead be used as GPIO24.

Table 2-14. System Management Interface Signals (Sheet 2 of 2)

Name	Type	Description
WOL_EN / GPIO9	O	**Wake On LAN Power Enable**. In an Intel AMT or ASF enabled system, this output signal is driven high by the ICH to control the LAN subsystem power (VccLAN3_3, VccCL3_3, LAN PHY Power, and SPI device) to support Wake on LAN (WOL) when the Intel Management Engine is powered off. This functionality is configured and controlled by the Intel Management Engine prior to entering the powered off state. **NOTES:** 1. This signal should be OR'd with the SLP_M# signal on the motherboard to determine when to power the LAN subsystem. 2. In order to support WOL out of a G3 state, the WOL_EN pin needs to be pulled high by an external resistor until the Intel Management Engine is initialized. If ASF or Intel AMT are disabled on a board that is configured for WOL_EN support, BIOS must utilize GPIO9 to control power to the LAN subsystem when entering S3-S5. In platforms that do not support Intel AMT or ASF, this signal is used as GPIO9.
CPU_MISSING / GPIO10 / JTAGTMS (Corporate Only)	I	**CPU Missing.** This signal provides CPU Missing functionality and is configured and controlled by the Manageability Engine. This signal must be connected to the CPU SKTOCC# output to indicate to the Intel Manageability Engine that the CPU is not physically present when asserted. ICH10 Consumer Family: This signal may be used as GPIO10. ICH10 Corporate Family: This signal may be used as GPIO10 or JTAGTMS.
TPM_PP / GPIO57 / JTAGTCK (Corporate Only)	I	**TPM Physical Presence.** This signal is asserted to indicate Physical Presence to the integrated TPM module. ICH10 Consumer Family: This signal may be used as GPIO57. ICH10 Corporate Family: This signal may be used as GPIO57 or JTAGTCK.

2.15 Real Time Clock Interface

Table 2-15. Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

2.16 Other Clocks

Table 2-16. Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. Runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** Used to run the USB controller. Runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller at 100 MHz. This clock is permitted to stop during S3/S4/S5 states.
DMI_CLKP, DMI_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the Direct Media Interface. Runs at 100 MHz.

2.17 Miscellaneous Signals

Table 2-17. Miscellaneous Signals (Sheet 1 of 2)

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal VccSus1_1, VccSus1_5 and VccCL1_5 regulators. This signal must be pulled-up to VccRTC.
LAN100_SLP	I	**Internal Voltage Regulator Enable:** When connected to VccRTC, this signal enables the internal voltage regulators powering VccLAN1_1 and VccCL1_1. This signal must be pulled-up to VccRTC.
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled as a functional strap. See Section 2.25.1 for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.

Table 2-17. Miscellaneous Signals (Sheet 2 of 2)

Name	Type	Description
SRTCRST#	I	**Secondary RTC Reset:** This signal resets the manageability register bits in the RTC well when the RTC battery is removed. **NOTES:** 1. The SRTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCRST# pin must rise before the RSMRST# pin.
TP0 / GPIO72 (Corporate Only)	I	**Test Point 0:** This signal must have an external pull-up to VccSus3_3. ICH10 Corporate: Pin can instead be used as GPIO72.
TP3	I/O	**Test Point 3:** Route signal to a test point.
TP4	I/O	**Test Point 4:** Route signal to a test point.
TP5	I/O	**Test Point 5:** Route signal to a test point.
TP6	I	**Test Point 6:** Route signal to a test point.
TP7	O	**Test Point 7:** Route signal to a test point.

2.18 Intel® High Definition Audio Link

Table 2-18. Intel® High Definition Audio Link Signals

Name	Type	Description
HDA_RST#	O	**Intel® High Definition Audio Reset:** Master hardware reset to external codec(s).
HDA_SYNC	O	**Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for more details. There is a weak integrated pull-down resistor on this pin.

Table 2-18. Intel® High Definition Audio Link Signals

Name	Type	Description
HDA_BIT_CLK	O	**Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Intel ICH10). This signal has a weak internal pull-down resistor.
HDA_SDOUT	O	**Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for more details. There is a weak integrated pull-down resistor on this pin.
HDA_SDIN[3:0]	I	**Intel High Definition Audio Serial Data In [3:0]**: Serial TDM data inputs from the codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel High Definition Audio. These signals have integrated pull-down resistors, which are always enabled. **NOTE:** During enumeration, the ICH will drive this signal. During normal operation, the CODEC will drive it.

2.19 Serial Peripheral Interface (SPI)

Table 2-19. Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS0#	O	**SPI Chip Select 0**: Used as the SPI bus request signal. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for more details.
SPI_CS1#	O	**SPI Chip Select 1**: Used as the SPI bus request signal. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for more details. There is a weak integrated pull-up resistor on this pin.
SPI_MISO	I	**SPI Master IN Slave OUT**: Data input pin for ICH10.
SPI_MOSI	O	**SPI Master OUT Slave IN**: Data output pin for ICH10. **NOTE:** This signal is sampled as a functional strap. See Section 2.25.1 for more details. There is a weak integrated pull-down resistor on this pin.
SPI_CLK	O	**SPI Clock**: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

2.20 Controller Link

Table 2-20. Controller Link Signals

Signal Name	Type	Description
CL_CLK0	I/O	**Controller Link Clock 0**: bi-directional clock that connects to the (G)MCH.
CL_DATA0	I/O	**Controller Link Data 0:** bi-directional data that connects to the (G)MCH.
CL_VREF0	I	**Controller Link Reference Voltage 0:** External reference voltage for Controller Link 0. ICH10 Corporate: When using internal reference voltage as configured by CLINKVREFSEL (ICHSTRP0:bit 5), an external circuit is not required and pin is No Connect (Recommended Configuration). Optionally, an external reference voltage generation circuit may be used (requires CLINKVREFSEL = 1).
CL_RST0#	O	**Controller Link Reset 0:** North Controller Link reset that connects to the (G)MCH.

2.21 Intel® Quiet System Technology

Table 2-21. Intel® Quiet System Technology Signals

Signal Name	Type	Description
PWM[2:0]	OD O	**Fan Pulse Width Modulation Outputs:** Pulse Width Modulated duty cycle output signal that is used for Intel® Quiet System Technology. When controlling a 3-wire fan, this signal controls a power transistor that, in turn, controls power to the fan. When controlling a 4-wire fan, this signal is connected to the “Control” signal on the fan. The polarity of this signal is programmable. The output default is low. These signals are 5V tolerant.
TACH0/GPIO17 **TACH1**/GPIO1 **TACH2**/GPIO6 **TACH3**/GPIO7	I	**Fan Tachometer Inputs:** Tachometer pulse input signal that is used to measure fan speed. This signal is connected to the “Sense” signal on the fan. Can instead be used as a GPIO.

Table 2-21. Intel® Quiet System Technology Signals

Signal Name	Type	Description
SST	I/O	**Simple Serial Transport:** Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors.
PECI	I/O	**Platform Environment Control Interface:** Single-wire, serial bus. Connect to corresponding pin of the processor for accessing processor digital thermometer.
QST_BMBUSY# (Consumer Only) / JTAGTDI (Corporate Only) / GPIO14	O	**Intel QST BMBUSY# Interconnect** (Consumer Only): This signal is used for Intel ICH10 Consumer based platforms that support Intel QST and C3 and/or C4 processor states. QST_BMBUSY# is asserted by the ICH10 to ensure that Intel QST can read the processor thermal sensor since the sensor is inaccessible when the platform is in C3 or C4. QST_BMBUSY# must be externally tied to the BMBUSY# signal on the ICH10 to cause the platform to exit or prevent entry into C3 or C4. QST_BMBUSY# functionality is configured and controlled by the Intel Management Engine firmware. ICH10 Consumer: In non-Intel QST based platforms, this signal can instead be used as a GPIO14. ICH10 Corporate: This signal is instead used as a GPIO14 or JTAGTDI.

2.22 JTAG Signals (Intel® ICH10 Corporate Family Only)

Table 2-22. JTAG Signals

Name	Type	Description
JTAGTCK (Corporate Only) / GPIO57 / TPM_PP	I/O	**Test Clock Input (TCK):** The test clock input provides the clock for the JTAG test logic.
JTAGTMS (Corporate Only) / GPIO10 / CPU_MISSING	I/O	**Test Mode Select (TMS):** The signal is decoded by the Test Access Port (TAP) controller to control test operations.
JTAGTDI (Corporate Only) / GPIO14 / QST_BMBUSY#	I/O	**Test Data Input (TDI):** Serial test instructions and data are received by the test logic at TDI.
JTAGTDO (Corporate Only) / GPIO11/ SMBALERT#	I/O	**Test Data Output (TDO):** TDO is the serial output for test instructions and data from the test logic defined in this standard.
JTAGRST# (Corporate Only) / LINKALERT# / GPIO60	I/O	**Test Reset (RST):** RST is an active low asynchronous signal that can reset the Test Access Port (TAP) controller. **NOTE:** The RST signal is optional per the IEEE 114.1 specification, and is not functional for Boundary Scan Testing

NOTE: JTAG Pin definitions are from IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Std. 1149.1-2001)

2.23 General Purpose I/O Signals

Table 2-23. General Purpose I/O Signals (Sheet 1 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO72 (Corporate Only)	I/O	3.3 V	Core	Native	ICH10 Consumer Family: Pin implemented as TP0 only. ICH10 Corporate Family: Pin is multiplexed with TP0. (NOTE 13)
GPIO63 (Corporate Only)	I/O	3.3 V	Suspend	Native	ICH10 Consumer Family: Pin may only be used as SLP_S5#. ICH10 Corporate Family: Pin is multiplexed with SLP_S5# (NOTE 13)
GPIO62 (Corporate Only)	I/O	3.3 V	Suspend	Native	ICH10 Consumer Family: Pin may only be used as SUSCLK ICH10 Corporate Family: Pin is multiplexed with SUSCLK (NOTE 13)
GPIO61 (Corporate Only)	I/O	3.3 V	Suspend	Native	ICH10 Consumer Family: Pin May only be used as SUS_STAT# / LPCPD# ICH10 Corporate Family: Pin is multiplexed with SUS_STAT# / LPCPD# (NOTE 13)
GPIO60	I/O	3.3 V	Suspend	Native	ICH10 Consumer Family: Multiplexed with LINKALERT#. ICH10 Corporate Family: Multiplexed with LINKALERT# and JTAGRST#. (NOTE 13)
GPIO59	I/O	3.3 V	Suspend	Native	Multiplexed with OC[0]#. (NOTE 13)
GPIO57	I/O	3.3 V	Suspend	GPI	ICH10 Consumer Family: Can be used as TPM_PP. ICH10 Corporate Family Can be used as TPM_PP or JTAGTCK.
GPIO56	I/O	3.3 V	Suspend	GPI	UnMultiplexed
GPIO55	I/O	3.3 V	Core	Native	Multiplexed with GNT3# (Note 8).
GPIO54	I/O	5.0 V	Core	Native	Multiplexed with REQ3#. (NOTE 13)
GPIO53	I/O	3.3 V	Core	Native	Multiplexed with GNT2# (Note 8).
GPIO52	I/O	5.0 V	Core	Native	Multiplexed with REQ2#. (NOTE 13)
GPIO51	I/O	3.3 V	Core	Native	Multiplexed with GNT1# (Note 8).
GPIO50	I/O	5.0 V	Core	Native	Multiplexed with REQ1#. (NOTE 13)
GPIO49	I/O	3.3V	Core	GPO	UnMultiplexed (Note 8).
GPIO48	I/O	3.3 V	Core	GPI	Multiplexed with SDATAOUT1.
GPIO[47:44]	I/O	3.3V	Suspend	Native	Multiplexed with OC[11:8]#. (NOTE 13)
GPIO[43:40]	I/O	3.3 V	Suspend	Native	Multiplexed with OC[4:1]#. (NOTE 13)
GPIO39	I/O	3.3 V	Core	GPI	Multiplexed with SDATAOUT0.
GPIO38	I/O	3.3 V	Core	GPI	Multiplexed with SLOAD.
GPIO37	I/O	3.3 V	Core	GPI	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	GPI	Multiplexed with SATA2GP.

Table 2-23. General Purpose I/O Signals (Sheet 2 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO35	I/O	3.3 V	Core	GPO	Multiplexed with SATACLKREQ#.
GPIO34	I/O	1.5 V / 3.3 V (Note 12)	VccHDA	GPO	UnMultiplexed.
GPIO33	I/O	3.3 V	Core	GPO	UnMultiplexed.
GPIO32	I/O	3.3 V	Core	GPO	UnMultiplexed.
GPIO31	I/O	3.3 V	Suspend	Native	Multiplexed with OC7#. (NOTE 13)
GPIO30	I/O	3.3 V	Suspend	Native	Multiplexed with OC6#. (NOTE 13)
GPIO29	I/O	3.3 V	Suspend	Native	Multiplexed with OC5#. (NOTE 13)
GPIO28	I/O	3.3 V	Suspend	GPO	UnMultiplexed.
GPIO27	I/O	3.3 V	Suspend	GPO	UnMultiplexed
GPIO26	I/O	3.3 V	Suspend	Native	Multiplexed with S4_STATE#. (Note 9)
GPIO25 (Corporate Only)	I/O	3.3 V	Suspend	Native	Default as STP_CPU# (Note 3).
GPIO24	I/O	3.3 V	Suspend	GPO	Can be used as MEM_LED. GPIO24 configuration register bits are not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Native	Multiplexed with LDRQ1#. (NOTE 13)
GPIO22	I/O	3.3 V	Core	GPI	Multiplexed with SCLOCK.
GPIO21	I/O	3.3 V	Core	GPI	Multiplexed with SATA0GP.
GPIO20	I/O	3.3 V	Core	GPO	UnMultiplexed. (Note 8)
GPIO19	I/O	3.3 V	Core	GPI	Multiplexed with SATA1GP.
GPIO18	I/O	3.3 V	Core	GPO (Note 11)	UnMultiplexed.
GPIO17	I/O	3.3 V	Core	GPI	Multiplexed with TACH0.
GPIO16	I/O	3.3 V	Core	Native	May also be used as DPRSLPVR
GPIO15	I/O	3.3 V	Suspend	Native	default as STP_PCI#. (Note 3)
GPIO14	I/O	3.3 V	Suspend	GPI	ICH10 Consumer Family: Can be used as QST_BMBUSY#. ICH10 Corporate Family: Can be used as JTAGTD, or QST_BMBUSY#I.
GPIO13	I/O	3.3 V	Suspend	GPI	UnMultiplexed.
GPIO12	I/O	3.3 V	Suspend	GPO	Multiplexed with LAN_PHY_PWR_CTRL. (NOTE 13)
GPIO11	I/O	3.3 V	Suspend	Native	ICH10 Consumer Family: Can be used as SMBALERT#. (NOTE 13) ICH10 Corporate Family Can be used as SMBALERT# or JTAGTDO. (NOTE 13)
GPIO10	I/O	3.3 V	Suspend	GPI	ICH10 Consumer Family: Can be used as CPU_MISSING. ICH10 Corporate Family: Can be used as CPU_MISSING or JTAGTMS.

Table 2-23. General Purpose I/O Signals (Sheet 3 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO9	I/O	3.3 V	Suspend	Native	Can be used as WOL_EN.
GPIO8	I/O	3.3 V	Suspend	Corporate Only GPI Consumer Only Native	ICH10 Corporate Family: Can be used as DRAMPWROK. ICH10 Consumer Family: Unmultiplexed
GPIO[7:6]	I/O	3.3 V	Core	GPI	Multiplexed with TACH[3:2].
GPIO[5:2]	I/OD	5 V	Core	GPI	Multiplexed with PIRQ[H:E]# (Note 6).
GPIO1	I/O	3.3 V	Core	GPI	Multiplexed with TACH1.
GPIO0	I/O	3.3 V	Core	GPI	Multiplexed with BMBUSY#.

NOTES:

1. All GPIOs can be configured as either input or output.
2. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
3. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Also, external devices should not be driving powered down GPIOs high. Some ICH10 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH10 driving a pin to a logic 1 to another device that is powered down.
4. The functionality that is multiplexed with the GPIO may not be utilized in desktop configuration.
5. This GPIO is not an open-drain when configured as an output.
6. SPI_CS1# is located in the VccCL3_3 well.
7. When this signal is configured as GPO the output stage is an open-drain.
8. This signal is sampled as a functional strap. See Section 2.25.1 for more details.
9. The GPIO_USE_SEL bit for this signal is overridden by bit 8 in the GEN_PMCON_3 Register (D31:F0).
10. The GPIO_USE_SEL bit for this is ignored. Functionality is set by bits 9:8 of FLMAP0 register.
11. GPIO18 will toggle at a frequency of approximately 1 Hz when the ICH10 comes out of reset.
12. The tolerance of this pin is determined by the voltage of VccHDA either 3.3 V or 1.5 V.
13. When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality.

2.24 Power and Ground Signals

Table 2-24. Power and Ground Signals (Sheet 1 of 2)

Name	Description
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
Vcc1_1	1.1 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for Logic and I/O. This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for Logic and I/O. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccCL1_1	1.1V supply for Controller Link. This plane must be on in S0 and other times Controller Link is used. This voltage is generated internally (see Section 2.25.1 for strapping option) and, this pin can be left as No Connect unless decoupling is required.
VccCL1_5	1.5V supply for Controller Link. This plane must be on in S0 and other times Controller Link is used. This voltage is generated internally (see Section 2.25.1 for strapping option), and this pin can be left as No Connect unless decoupling is required.
VccCL3_3	3.3V supply for Controller Link. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0 and other times Controller Link is used. **NOTE:** VccCL3_3 must always be powered when VccLAN3_3 is powered.
VccDMI	Power supply for DMI. 1.05V, 1.25V or 1.5V depending on (G)MCH's DMI voltage.
VccDMIPLL	1.5 V supply for core well logic. This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccGLAN1_5	1.5V supply for integrated Gigabit LAN I/O buffers. This power is on in S0 and is turned of in S3, S4, S5, even it integrated Gigabit LAN is not used.
VccGLAN3_3	3.3V supply for integrated Gigabit LAN logic and I/O. This power is on in S0 and is turned of in S3, S4, S5, even it integrated Gigabit LAN is not used.
VccGLANPLL	1.5V supply for core well logic. This signal is used for the integrated Gigabit LAN PLL. This power is shut off in S3, S4, S5 and G3 states.
VccHDA	Core supply for Intel High Definition Audio. This pin can be either 1.5 or 3.3 V. This power may be shut off in S3, S4, S5 or G3 states. **NOTE:** VccSusHDA and VccHDA can be connected to either 1.5 V or 3.3 V supplies, but both pins must be connected to supplies that are the same nominal value.
VccLAN1_1	1.1 V supply for LAN controller logic. This is a separate power plane that may or may not be powered in S3–S5 states. This voltage is generated internally (see Section 2.25.1 for strapping option) and, these pins can be left as No Connect unless decoupling is required.

Table 2-24. Power and Ground Signals (Sheet 2 of 2)

Name	Description
VccLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0. **NOTE:** VccLAN3_3 must always be powered when VccCL3_3 or Vcc3_3 is powered.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. Note: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel ICH10-based platform can be done by using a jumper on RTCRST# or GPI.
VccSATAPLL	1.5 V supply for core well logic. This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if SATA is not used.
VccSus1_1	1.1 V supply for suspend well logic. This power is not expected to be shut off unless the system is unplugged. This voltage is generated internally (see Section 2.25.1 for strapping option). These pins can be left as No Connects unless decoupling is required.
VccSus1_5	1.5V supply for the suspend well I/O. This power is not expected to be shut off unless the system is unplugged. This voltage is generated internally (see Section 2.25.1 for strapping option). These pins can be left as No Connects unless decoupling is required.
VccSus3_3	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccSusHDA	Suspend supply for Intel® High Definition Audio. This pin can be either 1.5 or 3.3 V. T **NOTE:** VccSusHDA and VccHDA can be connected to either 1.5 V or 3.3 V supplies, but both pins must be connected to supplies that are the same nominal value.
VccUSBPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if USB not used.
Vss	Grounds.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals listed in Table 2-12.

2.25 Pin Straps

2.25.1 Functional Straps

The following signals are used for static configuration. They are sampled at the rising edge of PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four PCI clocks prior to the time it is sampled.

The ICH10 has implemented Soft Straps. Soft Straps are used to configure specific functions within the ICH and (G)MCH very early in the boot process before BIOS or SW intervention. When Descriptor Mode is enabled, the ICH will read Soft Strap data out of the SPI device prior to the de-assertion of reset to both the Intel Management Engine and the Host system. Refer to Section 5.23.2 for information on Descriptor Mode and Section for more information on Soft Straps and their settings.

Table 2-25. Functional Strap Definitions (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.
HDA_SDOUT	PCI Express* Port Config 1 bit 1 (Port 1-4) (Consumer Only)	Rising Edge of PWROK	When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers:Offset 224h).This signal has a weak internal pull-down.
HDA_SYNC (Consumer Only)	PCI Express Port Config 1 bit 0 (Port 1-4)	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers:Offset 224h)
GNT2# / GPIO53 (Consumer Only)	PCI Express Port Config 2 bit 2 (Port 5-6)	Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved	Rising Edge of PWROK	This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high
GNT1#/GPIO51	ESI Strap (Server/ Workstation Only)	Rising edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull-up. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop.
GNT3# / GPIO55	Top-Block Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (Intel ICH10 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.

Table 2-25. Functional Strap Definitions (Sheet 2 of 4)

Signal	Usage	When Sampled	Comment
GNT0#	Boot BIOS Destination Selection 0	Rising Edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved **NOTE:** If option 11 LPC is selected, BIOS may still be placed on LPC, but all platforms with ICH10 (Corporate Only) require SPI flash connected directly to the ICH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.

Table 2-25. Functional Strap Definitions (Sheet 3 of 4)

Signal	Usage	When Sampled	Comment
SPI_CS1#	Boot BIOS Destination Selection 1	Rising Edge of CLPWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved **NOTE:** If option 11 LPC is selected BIOS may still be placed on LPC, but all platforms with ICH10 (Corporate Only) require SPI flash connected directly to the ICH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.
SATALED# (Consumer Only)	PCI Express Lane Reversal (Lanes 1-4)	Rising Edge of PWROK	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (ICH10 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
TP3	XOR Chain Entrance	Rising Edge of PWROK	See *Intel® ICH10 Family XOR Chains In-Circuit Tester Package* for functionality information. This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low unless using XOR Chain testing.

Table 2-25. Functional Strap Definitions (Sheet 4 of 4)

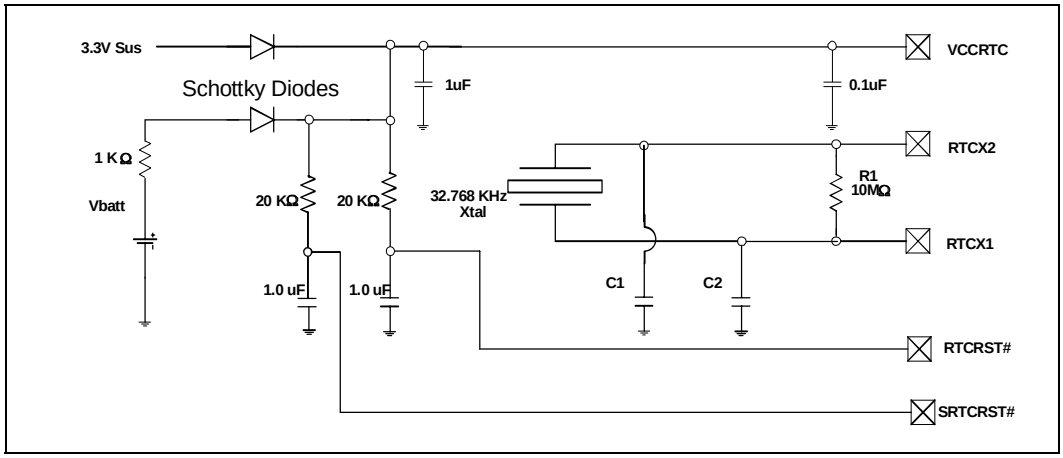
Signal	Usage	When Sampled	Comment
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap	Rising Edge of PWROK	If sampled low, the Flash Descriptor Security will be overridden. If high, the security measures defined in the Flash Descriptor will be in effect. **NOTE:** This strap should only be enabled in manufacturing environments using an external pull-down resistor. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also disable Intel Management Engine and Intel Management Engine features.
GPIO49	DMI Termination Voltage	Rising Edge of PWROK	This signal has a weak internal pull-up. **NOTE:** When DMI is DC coupled this signal should not be pulled low during the time the strap is sampled. **NOTE:** When DMI is AC coupled, this signal should be pulled low during the time the strap is sampled.
SPI_MOSI (Corporate Only)	Integrated TPM Enable	Rising Edge of CLPWROK	This signal has a weak internal pull-down resistor. When the signal is sampled low the Integrated TPM will be disabled. When the signal is sampled high, the (G)MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. **NOTE:** For Consumer applications this signal is required to be floating or pulled low.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

2.25.2 External RTC Circuitry

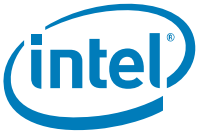
The ICH10 implements an internal oscillator circuit that is sensitive to step voltage changes in VccRTC. Figure 2-1 shows an example schematic recommended to ensure correct operation of the ICH10 RTC.

Figure 2-1. Example External RTC Circuit



NOTE: C1 and C2 depend on crystal load.

§ §



3 Intel® ICH10 Pin States

3.1 Integrated Pull-Ups and Pull-Downs

Table 3-1. Integrated Pull-Up and Pull-Down Resistors

Signal	Resistor Type	Nominal Value	Notes
CL_CLK0	Pull-up	20 kΩ	13
CL_DATA0	Pull-up	20 kΩ	13
CL_RST0#	Pull-up	10 kΩ	4
DPRSLPVR/GPIO16	Pull-down	20 kΩ	2, 10
HDA_BIT_CLK	Pull-down	20 kΩ	1, 9
HDA_DOCK_EN#/GPIO33	Pull-up	20 kΩ	3,7
HDA_RST#	Pull-down	20 kΩ	2
HDA_SDIN[3:0]	Pull-down	20 kΩ	2
HDA_SDOUT	Pull-down	20 kΩ	2, 7
HDA_SYNC	Pull-down	20 kΩ	2, 7
GLAN_DOCK#	Pull-up PUll-down	20 kΩ 20 kΩ	3, 14
GNT0#, GNT[3:1]#/GPIO[55,53,51]	Pull-up	20 kΩ	3, 11, 12
GPIO20	Pull-down	20 kΩ	3, 7
GPIO49	Pull-up	20 kΩ	3, 7
LAD[3:0]# / FHW[3:0]#	Pull-up	20 kΩ	3
LAN_RXD[2:0]	Pull-up	20 kΩ	4
LDRQ0	Pull-up	20 kΩ	3
LDRQ1 / GPIO23	Pull-up	20 kΩ	3
PME#	Pull-up	20 kΩ	3
PWRBTN#	Pull-up	20 kΩ	3
SATALED#	Pull-up	15 kΩ	8
SPI_CS1#	Pull-up	20 kΩ	3, 10
SPI_MOSI	Pull-down	20 kΩ	3, 7
SPI_MISO	Pull-up	20 kΩ	3
SPKR	Pull-down	20 kΩ	2
TACH[3:0]	Pull-up	20 kΩ	3
TP3	Pull-up	20 kΩ	6
USB[11:0] [P,N]	Pull-down	15 kΩ	5

NOTES:
1. Simulation data shows that these resistor values can range from 10 kΩ to 40 kΩ.
2. Simulation data shows that these resistor values can range from 9 kΩ to 50 kΩ.

3. Simulation data shows that these resistor values can range from 15 kΩ to 35 kΩ.
4. Simulation data shows that these resistor values can range from 7.5 kΩ to 16 kΩ.
5. Simulation data shows that these resistor values can range from 14.25 kΩ to 24.8 kΩ
6. Simulation data shows that these resistor values can range from 10 kΩ to 30 kΩ.
7. The pull-up or pull-down on this signal is only enabled at boot/reset for strapping function.
8. Simulation data shows that these resistor values can range from 10 kΩ to 20 kΩ. The internal pull-up is only enabled during PLTRST# assertion.
9. The pull-down on this signal is only enabled when in S3.
10. The pull-up or pull-down on this signal is only enabled during reset.
11. The pull-up on this signal is not enabled when PCIRST# is high.
12. The pull-up on this signal is not enabled when PWROK is low.
13. Simulation data shows that these resistor values can range from 15 kΩ to 31 kΩ.
14. The pull-up or pull-down on this pin is only active when configured for native GLAN_DOCK# functionality and is determined by the LAN controller.

3.2 Output and I/O Signals Planes and States

Table 3-2 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"High-Z"	Tri-state. ICH10 not driving the signal high or low.
"High"	ICH10 is driving the signal to a logic 1.
"Low"	ICH10 is driving the signal to a logic 0.
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Undefined"	ICH10 is driving the signal, but the value is indeterminate.
"Running"	Clock is toggling or signal is transitioning because function not stopping.
"Off"	The power plane is off; ICH10 is not driving when configured as an output or sampling when configured as an input.
"Input"	ICH10 is sampling and signal state determined by external driver.

Note: Signal levels are the same in S4 and S5, except as noted.

The ICH10 suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# deassertion. This does not apply to LAN_RST#, SLP_S3#, SLP_S4#, S4_STATE# and SLP_S5#. These signals are determinate and defined prior to RSMRST# deassertion.

The ICH10 core well signal states are indeterminate and undefined and may glitch prior to PWROK assertion. This does not apply to FERR# and THRMTRIP#. These signals are determinate and defined prior to PWROK assertion.

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 1 of 5)

Signal Name	Power Plane	During Reset[4]	Immediately after Reset[4]	C3/C4	S1	S3	S4/S5
PCI Express*							
PETp[5:1], PETn[5:1], PETp6 / GLANTXp, PETn6 / GLANTXn	Core	High	High[8]		Defined	Off	Off
DMI							
DMI[3:0]TXP, DMI[3:0]TXN	Core	High	High		Defined	Off	Off
PCI Bus							
AD[31:0]	Core	Low	Undefined		Defined	Off	Off
C/BE[3:0]#	Core	Low	Undefined		Defined	Off	Off
DEVSEL#	Core	High-Z	High-Z		High-Z	Off	Off
FRAME#	Core	High-Z	High-Z		High-Z	Off	Off
GNT0#[11], GNT[3:1]#[11]/ GPIO[55, 53, 51]	Core	High-Z	High		High	Off	Off
IRDY#, TRDY#	Core	High-Z	High-Z		High-Z	Off	Off

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 2 of 5)

Signal Name	Power Plane	During Reset[4]	Immediately after Reset[4]	C3/C4	S1	S3	S4/S5
PAR	Core	Low	Undefined		Defined	Off	Off
PCIRST#	Suspend	Low	High		High	Low	Low
PERR#	Core	High-Z	High-Z		High-Z	Off	Off
PLOCK#	Core	High-Z	High-Z		High-Z	Off	Off
STOP#	Core	High-Z	High-Z		High-Z	Off	Off
LPC Interface							
LAD[3:0] / FWH[3:0]	Core	High	High		High	Off	Off
LFRAME# / FWH[4]	Core	High	High		High	Off	Off
LPCPD# / SUS_STAT# / GPIO61 (Corporate Only)	Suspend	Low	High		High	Low	Low
Firmware Hub							
INIT3_3V#	Core	High	High		High	Off	Off
LAN Connect Interface							
LAN_RSTSYNC	LAN	High	Low		Defined	Defined	Defined
LAN_TXD[2:0]	LAN	Low	Low		Defined	Defined	Defined
Gigabit LAN Connect Interface							
GLAN_TXp / PETp6, GLAN_TXn / PETn6	GLAN	High	High		Defined	Off	Off
LAN_RSTSYNC	LAN	High	Low		Defined	Defined	Defined
SATA Interface							
SATA[5:0]TXP, SATA[5:0]TXN	Core	High-Z	High-Z		Defined	Off	Off
SATALED#[11]	Core	High-Z	High-Z		Defined	Off	Off
SATARBIAS	Core	High-Z	High-Z		Defined	Off	Off
SATACLKREQ# / GPIO35	Core	Low	Low		Defined	Off	Off
SCLOCK/GPIO22	Core	Input	Input		Defined	Off	Off
SLOAD/GPIO38	Core	Input	Input		Defined	Off	Off
SDATAOUT[1:0]/ GPIO[48,39]	Core	Input	Input		Defined	Off	Off
Interrupts							
PIRQ[A:D]#,	Core	High-Z	High-Z		High-Z	Off	Off
PIRQ[H:E]# / GPIO[5:2]	Core	Input	Input		Defined	Off	Off
SERIRQ	Core	High-Z	High-Z		High-Z	Off	Off
USB Interface							
USB[11:0][P,N]	Suspend	Low	Low		Defined	Defined	Defined
USBRBIAS	Suspend	High-Z	High-Z		Defined	Defined	Defined
Power Management							
DPRSLPVR	Core	Low	Low		High	Off	Off

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 3 of 5)

Signal Name	Power Plane	During Reset[4]	Immediately after Reset[4]	C3/C4	S1	S3	S4/S5
DPRSTP#	CPU	High	High		High	Off	Off
PLTRST#	Suspend	Low	High		High	Low	Low
SLP_M#[9]	Suspend	Low	High		High	Defined	Defined
SLP_S3#	Suspend	Low	High		High	Low	Low
SLP_S4#	Suspend	Low	High		High	High	Defined
S4_STATE# / GPIO26	Suspend	Low	Defined		Defined	Defined	Defined
SLP_S5#/ GPIO63 (Corporate Only)	Suspend	Low	High		High	High	Low[6]
SUS_STAT# / LPCPD# / GPIO61 (Corporate Only)	Suspend	Low	High		High	Low	Low
SUSCLK	Suspend	Low	Running				
CK_PWRGD	Suspend	Low	High		High	Low	Low
STP_PCI# / GPIO15	Suspend	High	High		Defined	Defined	Defined
STP_CPU# / GPIO25 (Corporate Only)	Suspend	High	High		Defined	Defined	Defined
Corporate Only: DRAMPWROK / GPIO8	Suspend	Low	Low	Defined	Defined	Defined/ Low[12]	Defined/ Low[12]
Processor Interface							
DPSLP#	CPU	High	High		High	Off	Off
A20M#	CPU	Dependant on A20GATE Signal	See Note 1		High	Off	Off
CPUPWRGD	CPU	Low[3]	High		High	Off	Off
IGNNE#	CPU	High	See Note 1		High	Off	Off
INIT#	CPU	High	High		High	Off	Off
INTR	CPU	See Note 5	See Note 5		Low	Off	Off
NMI	CPU	See Note 5	See Note 5		Low	Off	Off
SMI#	CPU	High	High		High	Off	Off
STPCLK#	CPU	High	High		Low	Off	Off
SMBus Interface							
SMBCLK, SMBDATA	Suspend	High-Z	High-Z		Defined	Defined	Defined
System Management Interface							
MEM_LED / GPIO24	Suspend	Low	Low		Defined	Defined	Defined
CPU_MISSING / GPIO10 / JTAGTMS (Corporate Only)	Suspend	Input	Input		Defined	Defined	Defined
GPIO14 / JTAGTDI (Corporate Only) / QST_BMBUSY#	Suspend	Input	Input		Defined	Defined	Defined
WOL_EN / GPIO9	Suspend	High-Z	High-Z		Defined	Defined	Defined

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 4 of 5)

Signal Name	Power Plane	During Reset[4]	Immediately after Reset[4]	C3/C4	S1	S3	S4/S5
LINKALERT# / GPIO60 / JTAGRST# (Corporate Only)	Suspend	High-Z	High-Z		Defined	Defined	Defined
TPM_PP / GPIO57 / JTAGTCK (Corporate Only)	Suspend	Input	Input		Defined	Defined	Defined
SPI_CS[1]#[11]	Suspend	High	High		Defined	Defined	Defined
SMLINK[1:0]	Suspend	High-Z	High-Z		Defined	Defined	Defined
Miscellaneous Signals							
SPKR[11]	Core	High-Z	Low		Defined	Off	Off
Intel® High Definition Audio Interface							
HDA_RST#	HDA Suspend	Low	Low[7]		Defined	Low	Low
HDA_SDOUT[11]	HDA	Low	Low		Low	Off	Off
HDA_SYNC	HDA	Low	Low		Low	Off	Off
HDA_BIT_CLK	HDA	Low	Low		Low	Off	Off
UnMultiplexed GPIO Signals							
GPIO0 / BMBUSY#	Core	Input	Input		Defined	Off	Off
Consumer Only: GPIO8	Suspend	Input	Input		Defined	Defined	Defined
GPIO12 / LAN_PHY_PWR_CTRL	Suspend	Low	Low		Defined	Defined	Defined
GPIO13	Suspend	Input	Input		Defined	Defined	Defined
GPIO16/DPRSLPVR	Core	Low	Low		Defined	Off	Off
GPIO18	Core	High	See Note 2		Defined	Off	Off
GPIO20[11]	Core	Low	High		Defined	Off	Off
GPIO[28:27]	Suspend	Low	Low		Defined	Defined	Defined
GPIO33[11], GPIO32	Core	High	High		Defined	Off	Off
GPIO34	HDA	Low	Low		Defined	Off	Off
GPIO49[11]	Core	High	High		Defined	Off	Off
GPIO56	Suspend	Input	Input		Defined	Defined	Defined
SPI Interface							
SPI_CS0#	Controller Link	High	High		Defined	Defined	Defined
SPI_CS1#[11]	Controller Link	High	High		Defined	Defined	Defined
SPI_MOSI[11]	Controller Link	Low	Low		Defined	Defined	Defined
SPI_CLK	Controller Link	Low	Low		Running	Defined	Defined
Controller Link							
CL_CLK0	Controller Link	Low	Low		Defined[10]	Defined[10]	Defined[10]

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 5 of 5)

Signal Name	Power Plane	During Reset[4]	Immediately after Reset[4]	C3/C4	S1	S3	S4/S5
CL_DATA0	Controller Link	Low	Low		Defined[10]	Defined[10]	Defined[10]
CL_RST0#	Suspend	Low	High		Defined[10]	Defined[10]	Defined[10]
Intel® Quiet System Technology							
PWM[2:0]	Core	High-Z	Low		Defined	Off	Off
SST	Controller Link	High-Z	Low		Defined	Off	Off
PECI	CPU	High-Z	Low		Defined	Off	Off

NOTES:

1. ICH10 drives these signals High after the processor Reset
2. GPIO[18] will toggle at a frequency of approximately 1 Hz when the ICH10 comes out of reset
3. CPUPWRGD represents a logical AND of the ICH10's VRMPWRGD and PWROK signals, and thus will be driven low by ICH10 when either VRMPWRGD or PWROK are inactive. During boot, or during a hard reset with power cycling, CPUPWRGD will be expected to transition from low to High-Z.
4. The states of Core and processor signals are evaluated at the times During PLTRST# and Immediately after PLTRST#. The states of the LAN and GLAN signals are evaluated at the times During LAN_RST# and Immediately after LAN_RST#. The states of the Controller Link signals are taken at the times During CL_RST# and Immediately after CL_RST#. The states of the Suspend signals are evaluated at the times During RSMRST# and Immediately after RSMRST#. The states of the HDA signals are evaluated at the times During HDA_RST# and Immediately after HDA_RST#.
5. ICH10 drives these signals Low before PWROK rising and Low after the processor Reset.
6. SLP_S5# signals will be high in the S4 state.
7. Low until Intel High Definition Audio Controller Reset bit set (D27:F0:Offset HDBAR+08h:bit 0), at which time HDA_RST# will be High and HDA_BIT_CLK will be Running.
8. PETp/n[6:1] high until port is enabled by software.
9. The SLP_M# state will be determined by Intel AMT Policies.
10. The state of signals in S3-5 will be defined by Intel AMT Policies.
11. This signal is sampled as a functional strap during reset.
12. The state of DRAMPWROK during S3/S4/S5 is dependent on the SLP_S4# and CLPWROK signals.

3.3 Power Planes for Input Signals

Table 3-3 shows the power plane associated with each input signal, as well as what device drives the signal at various times. Valid states include:

High
Low
Static: Will be high or low, but will not change
Driven: Will be high or low, and is allowed to change
Running: For input clocks

The ICH10 suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# deassertion. This does not apply to LAN_RST#, SLP_S3#, SLP_S4#, S4_STATE# and SLP_S5#. These signals are determinate and defined prior to RSMRST# deassertion.

The ICH10 core well signal states are indeterminate and undefined and may glitch prior to PWROK assertion. This does not apply to FERR# and THRMTRIP#. These signals are determinate and defined prior to PWROK assertion.

Table 3-3. Power Plane for Input Signals for Configurations (Sheet 1 of 3)

Signal Name	Power Well	Driver During Reset	C3/C4	S1	S3	S4/S5
DMI						
DMI_CLKP, DMI_CLKN	Core	Clock Generator		Running	Off	Off
DMI[3:0]RXP, DMI[3:0]RXN	Core	(G)MCH		Driven	Off	Off
PCI Express*						
PERp[5:1], PERn[5:1], PERp6 / GLAN_RXp, PERn6 / GLAN_RXn	Core	PCI Express* Device		Driven	Off	Off
PCI Bus						
REQ0#, REQ1# / GPIO50[1] REQ2# / GPIO52[1] REQ3# / GPIO54[1]	Core	External Pull-up		Driven	Off	Off
PCICLK	Core	Clock Generator		Running	Off	Off
PME#	Suspend	Internal Pull-up		Driven	Driven	Driven
SERR#	Core	PCI Bus Peripherals		High	Off	Off
LPC Interface						
LDRQ0#	Core	LPC Devices		High	Off	Off
LDRQ1# / GPIO23[1]	Core	LPC Devices		High	Off	Off
LAN Connect Interface						
GLAN_CLK	Suspend	LAN Connect Component		Driven	Off	Off
LAN_RXD[2:0]	Suspend	LAN Connect Component		Driven	Driven	Driven

Table 3-3. Power Plane for Input Signals for Configurations (Sheet 2 of 3)

Signal Name	Power Well	Driver During Reset	C3/C4	S1	S3	S4/S5
Gigabit LAN Connect Interface						
GLAN_RXp / PERp6, GLAN_RXn / PERn6	Suspend	Gigabit Lan Connect Component		Driven	Off	Off
SATA Interface						
SATA_CLKP, SATA_CLKN	Core	Clock Generator		Running	Off	Off
SATA[5:0]RXP, SATA[5:0]RXN	Core	SATA Drive		Driven	Off	Off
SATARBIAS#	Core	External Pull-down		Driven	Off	Off
SATA[5:4]GP SATA[3:0]GP / GPIO[37, 36, 19, 21][1]	Core	External Device or External Pull-up/Pull-down		Driven	Off	Off
USB Interface						
OC0# / GPIO59, OC[4:1]# / GPIO[43:40], OC[7:5]# / GPIO [31:29], OC[11:8]# / GPIO[47:44]	Suspend	External Pull-ups		Driven	Driven	Driven
USBRBIAS#	Suspend	External Pull-down		Driven	Driven	Driven
Power Management						
BMBUSY# /GPIO0[1]	Core	Graphics Component [(G)MCH]		Driven	High	Off
CLPWROK	Suspend	External Circuit		Driven	Driven	Driven
LAN_RST#	Suspend	External Circuit		High	High	High
MCH_SYNC#	Core	(G)MCH		Driven	Off	Off
PWRBTN#	Suspend	Internal Pull-up		Driven	Driven	Driven
PWROK	RTC	System Power Supply		Driven	Off	Off
RI#	Suspend	Serial Port Buffer		Driven	Driven	Driven
RSMRST#	RTC	External RC Circuit		High	High	High
SYS_RESET#	Suspend	External Circuit		Driven	Driven	Driven
THRM#	Core	Thermal Sensor		Driven	Off	Off
THRMTRIP#	CPU	Thermal Sensor		Driven	Off	Off
VRMPWRGD	Suspend	Processor Voltage Regulator		High	Low	Low
WAKE#	Suspend	External Pull-up		Driven	Driven	Driven
Processor Interface						
A20GATE	Core	External Microcontroller		Static	Off	Off
FERR#	Core	Processor		Static	Off	Off
RCIN#	Core	External Microcontroller		High	Off	Off

Table 3-3. Power Plane for Input Signals for Configurations (Sheet 3 of 3)

Signal Name	Power Well	Driver During Reset	C3/C4	S1	S3	S4/S5
SMBus Interface						
SMBALERT# / GPIO11 / JTAGTDO[1] (Corporate Only)	Suspend	External Pull-up		Driven	Driven	Driven
System Management Interface						
INTRUDER#	RTC	External Switch		Driven	High	High
Miscellaneous Signals						
INTVRMEN	RTC	External Pull-up		High	High	High
LAN100_SLP	RTC	External Pull-up		High	High	High
RTCRST#	RTC	External RC Circuit		High	High	High
SRTCRST#	RTC	External RC Circuit		High	High	High
CL_VREF0	Controller Link	Consumer Only: External Circuit[2] Corporate Only: Internal Circuit[3]		Driven	Driven	Driven
TP0 / GPIO72 (Corporate Only)	Suspend	External Pull-up		High	High	High
Intel® High Definition Audio Interface						
HDA_SDIN[3:0]	Suspend	Intel High Definition Audio Codec		Low	Low	Low
SPI Interface						
SPI_MISO	Controller Link	Internal Pull-up		Driven	Driven	Driven
Intel® Quiet System Technology						
TACH[3:0]/ GPIO[7,6,1,17][1]	Core	External Pull-up		Driven	Off	Off
Clocks						
CLK14	Core	Clock Generator		Running	Off	Off
CLK48	Core	Clock Generator		Running	Off	Off

NOTES:
1. These signals can be configured as outputs in GPIO mode.The state of the DPRSLPVR and DPRSTP# signals in C4 are high if Deeper Sleep is enabled or low if it is disabled.
2. Consumer Only: CL_VREF0 is driven by an external circuit except on platforms where the MCH does not support Controller Link. In these platforms, the signal is not driven.
3. Corporate Only: CL_VREF0 may optionally be driven by an external circuit, as configured by CLINKVREFSEL (ICHSTRP0:bit 5).

§ §

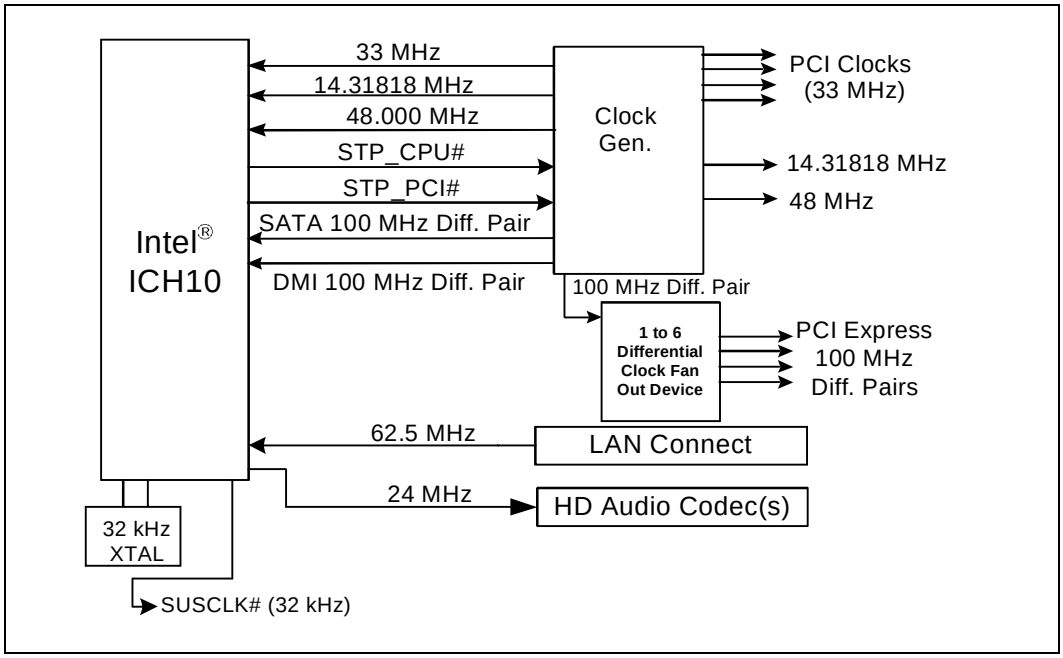
4 Intel® ICH10 and System Clock Domains

Table 4-1 shows the system clock domains. Figure 4-1 shows the assumed connection of the various system components, including the clock generator. For complete details of the system clocking solution, refer to the system's clock generator component specification.

Table 4-1. Intel® ICH10 and System Clock Domains

Clock Domain	Frequency	Source	Usage
ICH10 SATA_CLKP, SATA_CLKN	100 MHz	Main Clock Generator	Differential clock pair used for SATA.
ICH10 DMI_CLKP, DMI_CLKN	100 MHz	Main Clock Generator	Differential clock pair used for DMI.
ICH10 PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to Intel ICH10. This clock remains on during S0 and S1 state, and is expected to be shut off during S3 or below.
System PCI	33 MHz	Main Clock Generator	PCI Bus, LPC I/F. These only go to external PCI and LPC devices.
ICH10 CLK48	48.000 MHz	Main Clock Generator	Super I/O, USB controllers. Expected to be shut off during S3.
ICH10 CLK14	14.31818 MHz	Main Clock Generator	Used for ACPI timer and HPET timers. Expected to be shut off during S3.
GLAN_CLK	5 to 62.5 MHz	LAN Connect Component	Generated by the LAN Connect component. Expected to be shut off during S3.
SPI_CLK	17.86 MHz/ 31.25 MHz	ICH	Generated by the ICH. Expected to be shut off during S3.

Figure 4-1. ICH10 Conceptual System Clock Diagram



§ §

§

5 Functional Description

This chapter describes the functions and interfaces of the Intel ICH10 family.

5.1 DMI-to-PCI Bridge (D30:F0)

The DMI-to-PCI bridge resides in PCI Device 30, Function 0 on bus #0. This portion of the ICH10 implements the buffering and control logic between PCI and Direct Media Interface (DMI). The arbitration for the PCI bus is handled by this PCI device. The PCI decoder in this device must decode the ranges for the DMI. All register contents are lost when core well power is removed.

Direct Media Interface (DMI) is the chip-to-chip connection between the Memory Controller Hub / Graphics and Memory Controller Hub ((G)MCH) and I/O Controller Hub 10 (ICH10). This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH10 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH10 and (G)MCH).

Configuration registers for DMI, virtual channel support, and DMI active state power management (ASPM) are in the RCRB space in the Chipset Config Registers (Chapter 10).

DMI is also capable of operating in an Enterprise Southbridge Interface (ESI) compatible mode. ESI is a chip-to-chip connection for server chipsets. In this ESI-compatible mode, the DMI signals require AC coupling. A hardware strap is used to configure DMI in ESI-compatible mode see Section 2.25 for details.

5.1.1 PCI Bus Interface

The ICH10 PCI interface supports *PCI Local Bus Specification,* Revision 2.3, at 33 MHz. The ICH10 integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal ICH10 requests.

5.1.2 PCI Bridge As an Initiator

The bridge initiates cycles on the PCI bus when granted by the PCI arbiter. The bridge generates the cycle types listed in Table 5-1.

Table 5-1. PCI Bridge Initiator Cycle Types

Command	C/BE#	Notes
I/O Read/Write	2h/3h	Non-posted
Memory Read/Write	6h/7h	Writes are posted
Configuration Read/Write	Ah/Bh	Non-posted
Special Cycles	1h	Posted

5.1.2.1 Memory Reads and Writes

The bridge bursts memory writes on PCI that are received as a single packet from DMI.

5.1.2.2 I/O Reads and Writes

The bridge generates single DW I/O read and write cycles. When the cycle completes on the PCI bus, the bridge generates a corresponding completion on DMI. If the cycle is retried, the cycle is kept in the down bound queue and may be passed by a postable cycle.

5.1.2.3 Configuration Reads and Writes

The bridge generates single DW configuration read and write cycles. When the cycle completes on the PCI bus, the bridge generates a corresponding completion. If the cycle is retried, the cycle is kept in the down bound queue and may be passed by a postable cycle.

5.1.2.4 Locked Cycles

The bridge propagates locks from DMI per the *PCI Local Bus Specification*. The PCI bridge implements bus lock, which means the arbiter will not grant to any agent except DMI while locked.

If a locked read results in a target or master abort, the lock is not established (as per the *PCI Local Bus Specification*). Agents north of the ICH10 must not forward a subsequent locked read to the bridge if they see the first one finish with a failed completion.

5.1.2.5 Target / Master Aborts

When a cycle initiated by the bridge is master/target aborted, the bridge will not re-attempt the same cycle. For multiple DW cycles, the bridge increments the address and attempts the next DW of the transaction. For all non-postable cycles, a target abort response packet is returned for each DW that was master or target aborted on PCI. The bridge drops posted writes that abort.

5.1.2.6 Secondary Master Latency Timer

The bridge implements a Master Latency Timer via the SMLT register which, upon expiration, causes the de-assertion of FRAME# at the next legal clock edge when there is another active request to use the PCI bus.

5.1.2.7 Dual Address Cycle (DAC)

The bridge will issue full 64-bit dual address cycles for device memory-mapped registers above 4 GB.

5.1.2.8 Memory and I/O Decode to PCI

The PCI bridge in the ICH10 is a **subtractive decode agent**, which follows the following rules when forwarding a cycle from DMI to the PCI interface:

- The PCI bridge will **positively** decode any memory/IO address within its window registers, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set for memory windows and PCICMD.IOSE (D30:F0:Offset 04h:bit 0) is set for IO windows.
- The PCI bridge will **subtractively** decode any 64-bit memory address not claimed by another agent, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set.
- The PCI bridge will **subtractively** decode any 16-bit I/O address not claimed by another agent assuming PCICMD.IOSE (D30:F0:Offset 04h:bit 0) is set.
- If BCTRL.IE (D30:F0:Offset 3Eh:bit 2) is set, the PCI bridge will **not positively** forward from primary to secondary called out ranges in the IO window per *PCI Local Bus Specification* (I/O transactions addressing the last 768 bytes in each, 1 KB block: offsets 100h to 3FFh). The PCI bridge will still take them subtractively assuming the above rules.
- If BCTRL.VGAE (D30:F0:Offset 3Eh:bit 3) is set, the PCI bridge will **positively** forward from primary to secondary I/O and memory ranges as called out in the *PCI Bridge Specificatio*n, assuming the above rules are met.

5.1.3 Parity Error Detection and Generation

PCI parity errors can be detected and reported. The following behavioral rules apply:

- When a parity error is detected on PCI, the bridge sets the SECSTS.DPE (D30:F0:Offset 1Eh:bit 15).
- If the bridge is a master and BCTRL.PERE (D30:F0:Offset 3Eh:bit 0) is set and one of the parity errors defined below is detected on PCI, then the bridge will set SECSTS.DPD (D30:F0:Offset 1Eh:bit 8) and will also generate an internal SERR#.
  - — During a write cycle, the PERR# signal is active, or
  - — A data parity error is detected while performing a read cycle
- If an address or command parity error is detected on PCI and PCICMD.SEE (D30:F0:Offset 04h:bit 8), BCTRL.PERE, and BCTRL.SEE (D30:F0:Offset 3Eh:bit 1) are all set, the bridge will set PSTS.SSE (D30:F0:Offset 06h:bit 14) and generate an internal SERR#.
- If the PSTS.SSE is set because of an address parity error and the PCICMD.SEE is set, the bridge will generate an internal SERR#
- When bad parity is detected from DMI, bad parity will be driven on all data from the bridge.
- When an address parity error is detected on PCI, the PCI bridge will never claim the cycle. This is a slight deviation from the PCI bridge specification, which says that a cycle should be claimed if BCTRL.PERE is not set. However, DMI does not have a concept of address parity error, so claiming the cycle could result in the rest of the system seeing a bad transaction as a good transaction.

5.1.4 PCIRST#

The PCIRST# pin is generated under two conditions:

- PLTRST# active
- BCTRL.SBR (D30:F0:Offset 3Eh:bit 6) set to 1

The PCIRST# pin is in the suspend well. PCIRST# should be tied to PCI bus agents, but not other agents in the system.

5.1.5 Peer Cycles

The PCI bridge may be the initiator of peer cycles. Peer cycles include memory, IO, and configuration cycle types. Peer cycles are only allowed through VC0, and are enabled with the following bits:

- BPC.PDE (D30:F0:Offset 4Ch:bit 2) – Memory and I/O cycles
- BPC.CDE (D30:F0:Offset 4Ch:bit 1) – Configuration cycles

When enabled for peer for one of the above cycle types, the PCI bridge will perform a peer decode to see if a peer agent can receive the cycle. When not enabled, memory cycles (posted and/or non-posted) are sent to DMI, and I/O and/or configuration cycles are not claimed.

Configuration cycles have special considerations. Under the *PCI Local Bus Specification*, these cycles are not allowed to be forwarded upstream through a bridge. However, to enable things such as manageability, BPC.CDE can be set. When set, type 1 cycles are allowed into the part. The address format of the type 1 cycle is slightly different from a standard PCI configuration cycle to allow addressing of extended PCI space. The format is shown in Table 5-2.

Table 5-2. Type 1 Address Format

Bits	Definition
31:27	Reserved (same as the *PCI Local Bus Specification*)
26:24	Extended Configuration Address – allows addressing of up to 4K. These bits are combined with bits 7:2 to get the full register.
23:16	Bus Number (same as the *PCI Local Bus Specification*)
15:11	Device Number (same as the *PCI Local Bus Specification*)
10:8	Function Number (same as the *PCI Local Bus Specification*)
7:2	Register (same as the *PCI Local Bus Specification*)
1	0
0	Must be 1 to indicate a type 1 cycle. Type 0 cycles are not decoded.

Note: The ICH10's USB controllers cannot perform peer-to-peer traffic.

5.1.6 PCI-to-PCI Bridge Model

From a software perspective, the ICH10 contains a PCI-to-PCI bridge. This bridge connects DMI to the PCI bus. By using the PCI-to-PCI bridge software model, the ICH10 can have its decode ranges programmed by existing plug-and-play software such that PCI ranges do not conflict with graphics aperture ranges in the Host controller.

5.1.7 IDSEL to Device Number Mapping

When addressing devices on the external PCI bus (with the PCI slots), the ICH10 asserts one address signal as an IDSEL. When accessing device 0, the ICH10 asserts AD16. When accessing Device 1, the ICH10 asserts AD17. This mapping continues all the way up to device 15 where the ICH10 asserts AD31. Note that the ICH10's internal functions (Intel High Definition Audio, USB, SATA and PCI Bridge) are enumerated like they are off of a separate PCI bus (DMI) from the external PCI bus.

5.1.8 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The *PCI Local Bus Specification,* Revision 2.3 defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the ICH10. The *PCI Local Bus Specification,* Revision 2.3 defines two mechanisms to access configuration space, Mechanism 1 and Mechanism 2. The ICH10 only supports Mechanism 1.

Warning: Configuration writes to internal devices, when the devices are disabled, are invalid and may cause undefined results.

5.2 PCI Express* Root Ports (D28:F0,F1,F2,F3,F4,F5)

There are six root ports available in ICH10. These all reside in device 28, and take function 0 – 5. Port 1 is function 0, port 2 is function 1, port 3 is function 2, port 4 is function 3, port 5 is function 4, and port 6 is function 5.

PCI Express Root Ports 1-4 can be statically configured as four x1 Ports or ganged together to form one x4 port. Ports 5 and 6 can only be used as two x1 ports. The port configuration is set by RCBA 224h [Bits 1:0] see Section 10.1.38 for more details.

5.2.1 Interrupt Generation

The root port generates interrupts on behalf of Hot-Plug and power management events, when enabled. These interrupts can either be pin based, or can be MSIs, when enabled.

When an interrupt is generated via the legacy pin, the pin is internally routed to the ICH10 interrupt controllers. The pin that is driven is based upon the setting of the chipset configuration registers. Specifically, the chipset configuration registers used are the D28IP (Base address + 310Ch) and D28IR (Base address + 3146h) registers.

Table 5-3 summarizes interrupt behavior for MSI and wire-modes. In the table “bits” refers to the Hot-Plug and PME interrupt bits.

Table 5-3. MSI versus PCI IRQ Actions

Interrupt Register	Wire-Mode Action	MSI Action
All bits 0	Wire inactive	No action
One or more bits set to 1	Wire active	Send message
One or more bits set to 1, new bit gets set to 1	Wire active	Send message
One or more bits set to 1, software clears some (but not all) bits	Wire active	Send message
One or more bits set to 1, software clears all bits	Wire inactive	No action
Software clears one or more bits, and one or more bits are set on the same clock	Wire active	Send message

5.2.2 Power Management

5.2.2.1 S3/S4/S5 Support

Software initiates the transition to S3/S4/S5 by performing an IO write to the Power Management Control register in the ICH10. After the IO write completion has been returned to the processor, each root port will send a PME_Turn_Off TLP (Transaction Layer Packet) message on its downstream link. The device attached to the link will eventually respond with a PME_TO_Ack TLP message followed by sending a PM_Enter_L23 DLLP (Data Link Layer Packet) request to enter the L2/L3 Ready state. When all of the ICH10 root ports links are in the L2/L3 Ready state, the ICH10 power management control logic will proceed with the entry into S3/S4/S5.

Prior to entering S3, software is required to put each device into $D3_{HOT}$. When a device is put into $D3_{HOT}$ it will initiate entry into a L1 link state by sending a PM_Enter_L1 DLLP. Thus under normal operating conditions when the root ports sends the PME_Turn_Off message the link will be in state L1. However, when the root port is instructed to send the PME_Turn_Off message, it will send it whether or not the link was in L1. Endpoints attached to ICH can make no assumptions about the state of the link prior to receiving a PME_Turn_Off message.

5.2.2.2 Resuming from Suspended State

The root port contains enough circuitry in the suspend well to detect a wake event through the WAKE# signal and to wake the system. When WAKE# is detected asserted, an internal signal is sent to the power management controller of the ICH10 to cause the system to wake up. This internal message is not logged in any register, nor is an interrupt/GPE generated due to it.

5.2.2.3 Device Initiated PM_PME Message

When the system has returned to a working state from a previous low power state, a device requesting service will send a PM_PME message continuously, until acknowledge by the root port. The root port will take different actions depending upon whether this is the first PM_PME has been received, or whether a previous message has been received but not yet serviced by the operating system.

If this is the first message received (RSTS.PS - D28:F0/F1/F2/F3/F4/F5:Offset 60h:bit 16 is cleared), the root port will set RSTS.PS, and log the PME Requester ID into RSTS.RID (D28:F0/F1/F2/F3/F4/F5:Offset 60h:bits 15:0). If an interrupt is enabled via RCTL.PIE (D28:F0/F1/F2/F3/F4/F5:Offset 5Ch:bit 3), an interrupt will be generated. This interrupt can be either a pin or an MSI if MSI is enabled via MC.MSIE (D28:F0/F1/F2/F3/F4/F5:Offset 82h:bit 0). See Section 5.2.2.4 for SMI/SCI generation.

If this is a subsequent message received (RSTS.PS is already set), the root port will set RSTS.PP (D28:F0/F1/F2/F3/F4/F5:Offset 60h:bit 17) and log the PME Requester ID from the message in a hidden register. No other action will be taken.

When the first PME event is cleared by software clearing RSTS.PS, the root port will set RSTS.PS, clear RSTS.PP, and move the requester ID from the hidden register into RSTS.RID.

If RCTL.PIE is set, an interrupt will be generated. If RCTL.PIE is not set, a message will be sent to the power management controller so that a GPE can be set. If messages have been logged (RSTS.PS is set), and RCTL.PIE is later written from a 0 to a 1, and interrupt will be generated. This last condition handles the case where the message was received prior to the operating system re-enabling interrupts after resuming from a low power state.

5.2.2.4 SMI/SCI Generation

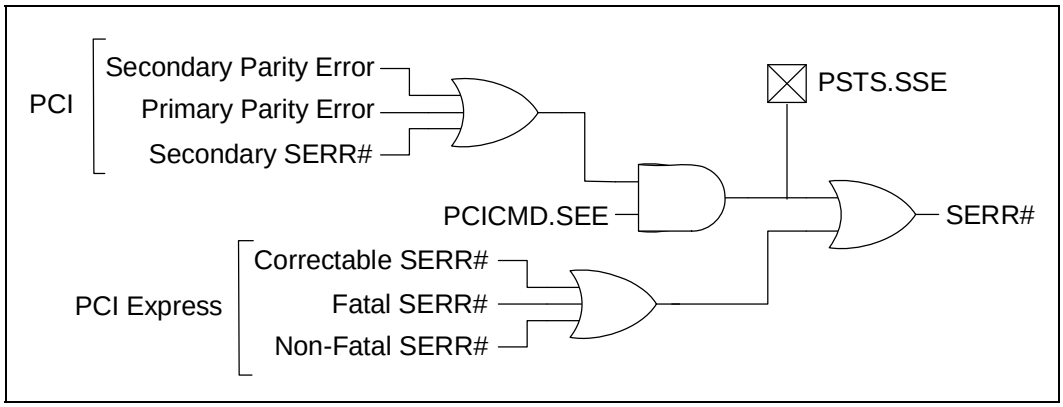
Interrupts for power management events are not supported on legacy operating systems. To support power management on non-PCI Express aware operating systems, PM events can be routed to generate SCI. To generate SCI, MPC.PMCE must be set. When set, a power management event will cause SMSCS.PMCS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 31) to be set.

Additionally, BIOS workarounds for power management can be supported by setting MPC.PMME (D28:F0/F1/F2/F3/F4/F5:Offset D8h:bit 0). When this bit is set, power management events will set SMSCS.PMMS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 0), and SMI # will be generated. This bit will be set regardless of whether interrupts or SCI is enabled. The SMI# may occur concurrently with an interrupt or SCI.

5.2.3 SERR# Generation

SERR# may be generated via two paths – through PCI mechanisms involving bits in the PCI header, or through PCI Express* mechanisms involving bits in the PCI Express capability structure.

Figure 5-1. Generation of SERR# to Platform



5.2.4 Hot-Plug

Each root port implements a Hot-Plug controller which performs the following:

- Messages to turn on / off / blink LEDs
- Presence and attention button detection
- Interrupt generation

The root port only allows Hot-Plug with modules (e.g., ExpressCard*). Edge-connector based Hot-Plug is not supported.

5.2.4.1 Presence Detection

When a module is plugged in and power is supplied, the physical layer will detect the presence of the device, and the root port sets SLSTS.PDS (D28:F0/F1/F2/F3/F4/F5:Offset 5Ah:bit 6) and SLSTS.PDC (D28:F0/F1/F2/F3:Offset 6h:bit 3). If SLCTL.PDE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 3) and SLCTL.HPE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 5) are both set, the root port will also generate an interrupt.

When a module is removed (via the physical layer detection), the root port clears SLSTS.PDS and sets SLSTS.PDC. If SLCTL.PDE and SLCTL.HPE are both set, the root port will also generate an interrupt.

5.2.4.2 Message Generation

When system software writes to SLCTL.AIC (D28:F0/F1/F2/F3F4/F5:Offset 58h:bits 7:6) or SLCTL.PIC (D28:F0/F1/F2/F3F4/F5:Offset 58h:bits 9:8), the root port will send a message down the link to change the state of LEDs on the module.

Writes to these fields are non-postable cycles, and the resulting message is a postable cycle. When receiving one of these writes, the root port performs the following:

- Changes the state in the register.
- Generates a completion into the upstream queue
- Formulates a message for the downstream port if the field is written to regardless of if the field changed.
- Generates the message on the downstream port
- When the last message of a command is transmitted, sets SLSTS.CCE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 4) to indicate the command has completed. If SLCTL.CCE and SLCTL.HPE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 5) are set, the root port generates an interrupt.

The command completed register (SLSTS.CC) applies only to commands issued by software to control the Attention Indicator (SLCTL.AIC), Power Indicator (SLCTL.PIC), or Power Controller (SLCTL.PCC). However, writes to other parts of the Slot Control Register would invariably end up writing to the indicators, power controller fields; Hence, any write to the Slot Control Register is considered a command and if enabled, will result in a command complete interrupt. The only exception to this rule is a write to disable the command complete interrupt which will not result in a command complete interrupt.

A single write to the Slot Control register is considered to be a single command, and hence receives a single command complete, even if the write affects more than one field in the Slot Control Register.

5.2.4.3 Attention Button Detection

When an attached device is ejected, an attention button could be pressed by the user. This attention button press will result in a the PCI Express message "Attention_Button_Pressed" from the device. Upon receiving this message, the root port will set SLSTS.ABP (D28:F0/F1/F2/F3F4/F5:Offset 5Ah:bit 0).

If SLCTL.ABE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 0) and SLCTL.HPE (D28:F0/F1/F2/F3F4/F5:Offset 58h:bit 5) are set, the Hot-Plug controller will also generate an interrupt. The interrupt is generated on an edge-event. For example, if SLSTS.ABP is already set, a new interrupt will not be generated.

5.2.4.4 SMI/SCI Generation

Interrupts for Hot-Plug events are not supported on legacy operating systems. To support Hot-Plug on non-PCI Express aware operating systems, Hot-Plug events can be routed to generate SCI. To generate SCI, MPC.HPCE (D28:F0/F1/F2/F3F4/F5:Offset D8h:bit 30) must be set. When set, enabled Hot-Plug events will cause SMSCS.HPCS (D28:F0/F1/F2/F3F4/F5:Offset DCh:bit 30) to be set.

Additionally, BIOS workarounds for Hot-Plug can be supported by setting MPC.HPME (D28:F0/F1/F2/F3F4/F5:Offset D8h:bit 1). When this bit is set, Hot-Plug events can cause SMI status bits in SMSCS to be set. Supported Hot-Plug events and their corresponding SMSCS bit are:

- Command Completed - SCSCS.HPCCM (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 3)
- Presence Detect Changed - SMSCS.HPPDM (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 1)
- Attention Button Pressed - SMSCS.HPABM (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 2)
- Link Active State Changed - SMSCS.HPLAS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:bit 4)

When any of these bits are set, SMI # will be generated. These bits are set regardless of whether interrupts or SCI is enabled for Hot-Plug events. The SMI# may occur concurrently with an interrupt or SCI.

5.3 Gigabit Ethernet Controller (B0:D25:F0)

The ICH10 integrates a Gigabit Ethernet Controller. The integrated Gigabit Ethernet controller is compatible with Gigabit Ethernet PHY (Intel® 82567 Gigabit Platform LAN Connect device). The integrated Gigabit Ethernet controller provides two interfaces: LAN Connect Interface (LCI) for 10/100 operation and Gigabit LAN Connect Interface (GLCI) for Gigabit Ethernet operation. The GLCI is shared with the ICH10's PCI Express port 6 and can be enabled via a soft strap that is stored in system SPI flash, see Section for details.

The ICH10 integrated Gigabit Ethernet controller supports multi speed operation, 10/100/1000 MB/s. The integrated Gigabit Ethernet can operate in full-duplex at all supported speeds or half-duplex at 10/100 MB/s, and adheres with the *IEEE 802.3x Flow Control Specification.*

Note: Gigabit Ethernet (1000Mb/s) is only supported in S0.

The controller provides a system interface via a PCI function. A full memory-mapped or IO-mapped interface is provided to the software, along with DMA mechanisms for high performance data transfer.

The following summarizes the ICH10 integrated Gigabit Ethernet controller features:

- Configurable LED operation for customization of LED display.
- IPv4 and IPv6 Checksum Offload support (receive, transmit, and large send).
- 64-bit address master support for system using more than 4 GB of physical memory.
- Configurable receive and transmit data FIFO, programmable in 1 KB increments.
- Intelligent interrupt generation to enhance driver performance.
- Compliance with Advanced Configuration and Power Interface and PCI Power Management standards.
- ACPI register set and power down functionality supporting D0 and D3 states.
- Full wake-up support (APM and ACPI).
- Magic Packet wake-up enable with unique MAC address.
- Fragmented UDP checksum off load for package reassembly.
- Jumbo frames supported.
- LinkSec support (802.3ae compliant)
- TimeSync support (802.1as compliant)

5.3.1 Gigabit Ethernet PCI Bus Interface

The Gigabit Ethernet controller has a PCI interface to the host processor and host memory. The following sections detail the transaction on the bus.

5.3.1.1 Transaction Layer

The upper layer of the host architecture is the transaction layer. The transaction layer connects to the device core using an implementation specific protocol. Through this core-to-transaction-layer protocol, the application-specific parts of the device interact with the subsystem and transmit and receive requests to or from the remote agent, respectively.

5.3.1.2 Data Alignment

5.3.1.2.1 4 K Boundary

PCI requests must never specify an Address/Length combination that causes a Memory Space access to cross a 4 K boundary. It is the HW responsibility to break requests into 4 K-aligned requests (if needed). This does not pose any requirement on SW. However, if SW allocates a buffer across a 4 K boundary, HW will issue multiple requests for the buffer. SW should consider aligning buffers to 4 KB boundary in cases where it improves performance.

The alignment to the 4 K boundaries is done in the core. The Transaction layer will not do any alignment according to these boundaries.

5.3.1.2.2 64 Bytes

PCI requests are multiples of 64 bytes and aligned to make better use of memory controller resources. Writes, however, can be on any boundary and can cross a 64 byte alignment boundary

5.3.1.3 Configuration Request Retry Status

The LAN Controller might have a delay in initialization due to NVM read. If the NVM configuration read operation is not completed and the device receives a Configuration Request, the device will respond with a Configuration Request Retry Completion Status to terminate the Request, and thus effectively stall the Configuration Request until such time that the subsystem has completed local initialization and is ready to communicate with the host.

5.3.2 Error Events and Error Reporting

5.3.2.1 Data Parity Error

The PCI Host bus does not provide parity protection, but it does forward parity errors from bridges. The LAN Controller recognizes parity errors through the internal bus interface and will set the Parity Error bit in PCI Configuration space. If parity errors are enabled in configuration space, a system error will be indicated on the PCI Host bus to the chipset. The offending cycle with a parity error will be dropped and not processed by the LAN Controller.

5.3.2.2 Completion with Unsuccessful Completion Status

A completion with unsuccessful completion status (any status other than "000") will be dropped and not processed by the LAN Controller. Furthermore, the request that corresponds to the unsuccessful completion will not be retried. When this unsuccessful completion status is received, the System Error bit in the PCI Configuration space will be set. If the system errors are enabled in configuration space, a system error will be indicated on the PCI Host bus to the chipset.

5.3.3 Ethernet Interface

The integrated LAN controller provides a complete CSMA/CD function supporting IEEE 802.3 (10Mb/s), 802.3u (100Mb/s) implementations. It also supports the IEEE 802.3z and 802.3ab (1000Mb/s) implementations. The device performs all of the functions required for transmission, reception and collision handling called out in the standards.

The mode used to communicate between the LAN controller and the LAN connect device supports 10/100/1000 Mbps operation, with both half- and full-duplex operation at 10/100 Mbps, and full-duplex operation at 1000 Mbps.

5.3.3.1 MAC/LAN Connect Interface

The integrated LAN controller and LAN Connect Device communicate through either the platform LAN connect interface (LCI) or Gigabit LAN connect interface (GLCI). All controller configuration is performed using device control registers mapped into system memory or I/O space. The LAN Connect Device is configured via the LCI or Gigabit Ethernet Lan connect interface.

The integrated MAC supports various modes as summarized in the following table

Table 5-4. LAN Mode Support

Mode	Interface Active	Connections
Normal 10/100/1000	LCI, GLCI	Intel® 82567 Gigabit Platform LAN Connect Device

5.3.4 PCI Power Management

The LAN Controller supports the Advanced Configuration and Power Interface (ACPI) specification as well as Advanced Power Management (APM). This allows the host to be awoken (i.e., from Sx (S3-S5) to S0) by network-related activity via an internal host wake signal.

The LAN controller contains power management registers for PCI, and supports D0 and D3 states. PCI transactions are only allowed in the D0 state, except for host accesses to the LAN controller's PCI configuration registers.

5.3.4.1 Wake-Up

The LAN Controller supports two types of wakeup mechanisms:

1. Advanced Power Management (APM) Wakeup
2. ACPI Power Management Wakeup

Both mechanisms use an internal WAKE# signal to wake the system up. This signal is connected to the suspend wake logic in the ICH10. The wake-up steps are as follows:

1. Host Wake Event occurs (note that packet is not delivered to host)
2. PME_STATUS bit is set
3. Internal WAKE# signal asserted by Host LAN function
4. System wakes from Sx state to S0 state
5. The Host LAN function is transitioned to D0
6. The Host clears the PME_STATUS bit
7. Internal WAKE# signal is deasserted by Host LAN function

5.3.4.1.1 Advanced Power Management Wakeup

Advanced Power Management Wakeup, or APM Wakeup, was previously known as Wake on LAN. It is a feature that has existed in the 10/100 Mbps NICs for several generations. The basic premise is to receive a broadcast or unicast packet with an explicit data pattern, and then to assert a signal to wake-up the system. In the earlier generations, this was accomplished by using a special signal that ran across a cable to a defined connector on the motherboard. The NIC would assert the signal for approximately 50ms to signal a wakeup. The LAN Controller uses (if configured to) an in-band PM_PME message for this.

On power-up, the LAN Controller will read the APM Enable bits from the NVM PCI Init Control Word into the APM Enable (APME) bits of the Wakeup Control Register (WUC). These bits control enabling of APM Wakeup.

When APM Wakeup is enabled, the LAN Controller checks all incoming packets for Magic Packets.

Once the LAN Controller receives a matching magic packet, it will:

- Set the Magic Packet Received bit in the Wake Up Status Register (WUS).
- Set the PME_Status bit in the Power Management Control / Status Register (PMCSR) and assert the internal WAKE# signal.

APM Wakeup is supported in all power states and only disabled if a subsequent NVM read results in the APM Wake Up bit being cleared or the software explicitly writes a 0 to the APM Wake Up (APM) bit of the WUC register.

5.3.4.1.2 ACPI Power Management Wakeup

The LAN Controller supports ACPI Power Management based Wakeups. It can generate system wake-up events from three sources:

- Reception of a Magic Packet.
- Reception of a Network Wakeup Packet.
- Detection of a link change of state.

Activating ACPI Power Management Wakeup requires the following steps:

- The driver programs the Wake Up Filter Control Register (WUFC) to indicate the packets it wishes to wake up from and supplies the necessary data to the Ipv4 Address Table (IP4AT) and the Flexible Filter Mask Table (FFMT), Flexible Filter Length Table (FFLT), and the Flexible Filter Value Table (FFVT). It can also set the Link Status Change Wake Up Enable (LNKC) bit in the Wake Up Filter Control Register (WUFC) to cause wakeup when the link changes state.
- The OS (at configuration time) writes a 1 to the PME_EN bit of the Power Management Control / Status Register (PMCSR.8).

Normally, after enabling wakeup, the OS will write 11b to the lower two bits of the PMCSR to put the LAN Controller into low-power mode.

Once Wakeup is enabled, the LAN Controller monitors incoming packets, first filtering them according to its standard address filtering method, then filtering them with all of the enabled wakeup filters. If a packet passes both the standard address filtering and at least one of the enabled wakeup filters, the LAN Controller will:

- Set the PME_Status bit in the Power Management Control / Status Register (PMCSR)
- If the PME_EN bit in the Power Management Control / Status Register (PMCSR) is set, assert the internal WAKE# signal.
- Set one or more of the Received bits in the Wake Up Status Register (WUS). (More than one bit will be set if a packet matches more than one filter.)

If enabled, a link state change wakeup will cause similar results, setting PME_Status, asserting the internal WAKE# signal and setting the Link Status Changed (LNKC) bit in the Wake Up Status Register (WUS) when the link goes up or down.

The internal WAKE# signal will remain asserted until the OS either writes a 1 to the PME_Status bit of the PMCSR register or writes a 0 to the PME_En bit.

After receiving a wakeup packet, the LAN Controller will ignore any subsequent wakeup packets until the driver clears all of the Received bits in the Wake Up Status Register (WUS). It will also ignore link change events until the driver clears the Link Status Changed (LNKC) bit in the Wake Up Status Register (WUS).

5.3.5 Configurable LEDs

The LAN Controller supports 3 controllable and configurable LEDs that are driven from the LAN Connect Device. Each of the three LED outputs can be individually configured to select the particular event, state, or activity, which will be indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indication.

The configuration for LED outputs is specified via the LEDCTL register. Furthermore, the hardware-default configuration for all the LED outputs, can be specified via NVM fields, thereby supporting LED displays configurable to a particular OEM preference.

Each of the 3 LED's may be configured to use one of a variety of sources for output indication. The MODE bits control the LED source:

- LINK_100/1000 is asserted when link is established at either 100 or 1000Mbps.
- LINK_10/1000 is asserted when link is established at either 10 or 1000Mbps.
- LINK_UP is asserted when any speed link is established and maintained. ACTIVITY is asserted when link is established and packets are being transmitted or received.
- LINK/ACTIVITY is asserted when link is established AND there is NO transmit or receive activity
- LINK_10 is asserted when a 10Mbps link is established and maintained.
- LINK_100 is asserted when a 100Mbps link is established and maintained.
- LINK_1000 is asserted when a 1000Mbps link is established and maintained.
- FULL_DUPLEX is asserted when the link is configured for full duplex operation.
- COLLISION is asserted when a collision is observed.
- PAUSED is asserted when the device's transmitter is flow controlled.
- LED_ON is always asserted; LED_OFF is always de-asserted.

The IVRT bits allow the LED source to be inverted before being output or observed by the blink-control logic. LED outputs are assumed to normally be connected to the negative side (cathode) of an external LED.

The BLINK bits control whether the LED should be blinked while the LED source is asserted, and the blinking frequency (either 200 ms on and 200 ms off or 83 ms on and 83 ms off). The blink control may be especially useful for ensuring that certain events, such as ACTIVITY indication, cause LED transitions, which are sufficiently visible to a human eye. The same blinking rate is shared by all LEDs.

5.3.6 Function Level Reset Support (FLR)

The Gigabit LAN Controller supports the Function Level Reset (FLR) capability. The FLR capability can be used in conjunction with Intel Virtualization Technology. FLR allows an Operating System in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the Operating System to reset the whole device as if a PCI reset was asserted.

5.3.6.1 FLR Steps

5.3.6.1.1 FLR Initialization

1. A FLR is initiated by software writing a 1 to the Initiate FLR bit.
2. All subsequent requests targeting the Function will not be claimed and will be Master Abort Immediate on the bus. This includes any configuration, I/O or Memory cycles, however, the Function shall continue to accept completions targeting the Function.

5.3.6.1.2 FLR Operation

Function will Reset all configuration, I/O and memory registers of the Function except those indicated otherwise and reset all internal states of the Function to the default or initial condition.

5.3.6.1.3 FLR Completion

The Initiate FLR bit is reset (cleared) when the FLR reset is completed. This bit can be used to indicate to the software that the FLR reset is completed.

Note: From the time Initiate FLR bit is written to 1 software must wait at least 100 ms before accessing the function.

5.4 LPC Bridge (w/ System and Management Functions) (D31:F0)

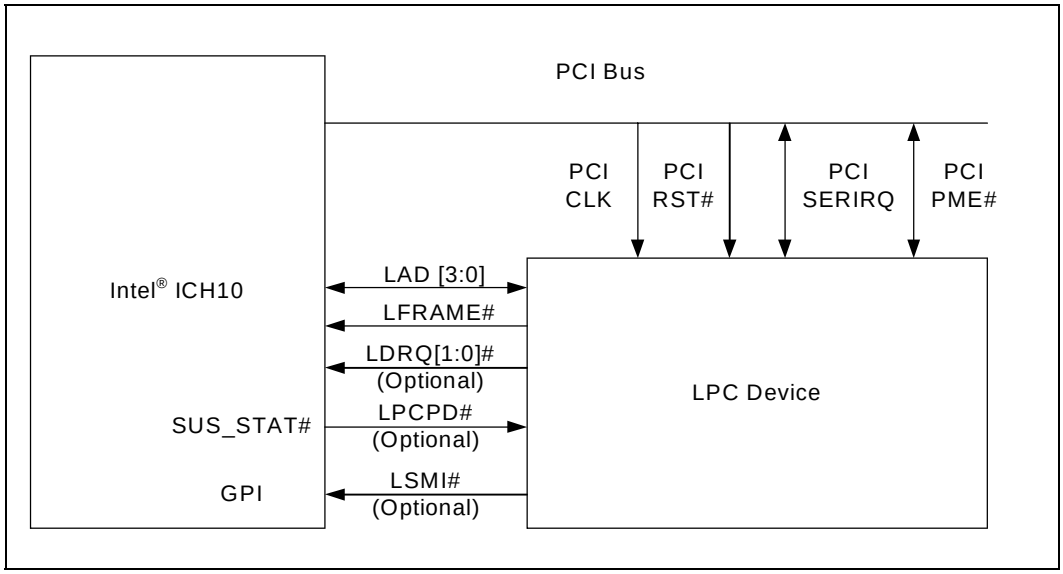
The LPC bridge function of the ICH10 resides in PCI Device 31:Function 0. In addition to the LPC bridge function, D31:F0 contains other functional units including DMA, Interrupt controllers, Timers, Power Management, System Management, GPIO, and RTC. In this chapter, registers and functions associated with other functional units (power management, GPIO, USB, etc.) are described in their respective sections.

Note: The LPC bridge cannot be configured as a subtractive decode agent.

5.4.1 LPC Interface

The ICH10 implements an LPC interface as described in the *Low Pin Count Interface Specification,* Revision 1.1. The LPC interface to the ICH10 is shown in Figure 5-2. Note that the ICH10 implements all of the signals that are shown as optional, but peripherals are not required to do so.

Figure 5-2. LPC Interface Diagram



5.4.1.1 LPC Cycle Types

The ICH10 (Corporate only) implements all of the cycle types described in the *Low Pin Count Interface Specification,* Revision 1.1. ICH10 Consumer does not provide a generic mechanism for decoding memory ranges and forwarding them as standard LPC Memory cycles on the LPC bus. Table 5-5 shows the cycle types supported by the ICH10.

Table 5-5. LPC Cycle Types Supported

Cycle Type	Comment
Memory Read (Corporate only)	1 byte only. (See Note 1 below)
Memory Write (Corporate only)	1 byte only. (See Note 1 below)
I/O Read	1 byte only. Intel ICH10 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
I/O Write	1 byte only. ICH10 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes. (See Note 2 below)
Bus Master Write	Can be 1, 2, or 4 bytes. (See Note 2 below)

NOTES:
1. ICH10 (Corporate only) provides a single generic memory range (LGMR) for decoding memory cycles and forwarding them as LPC Memory cycles on the LPC bus. The LGMR memory decode range is 64 KB in size and can be defined as being anywhere in the 4 GB memory space. This range needs to be configured by BIOS during POST to provide the necessary memory resources. BIOS should advertise the LPC Generic Memory Range as Reserved to the OS in order to avoid resource conflict. For larger transfers, the ICH10 performs multiple 8-bit transfers. If the cycle is not claimed by any peripheral, it is subsequently aborted, and the ICH10 returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds.
2. Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word-aligned (i.e., with an address where A0=0). A dword transfer must be dword-aligned (i.e., with an address where A1 and A0 are both 0).

5.4.1.2 Start Field Definition

Table 5-6. Start Field Bit Definitions

Bits[3:0] Encoding	Definition
0000	Start of cycle for a generic target
0010	Grant for bus master 0
0011	Grant for bus master 1
1111	Stop/Abort: End of a cycle for a target.

NOTE: All other encodings are RESERVED.

5.4.1.3 Cycle Type / Direction (CYCTYPE + DIR)

The ICH10 always drives bit 0 of this field to 0. Peripherals running bus master cycles must also drive bit 0 to 0. Table 5-7 shows the valid bit encodings.

Table 5-7. Cycle Type Bit Definitions

Bits[3:2]	Bit1	Definition
00	0	I/O Read
00	1	I/O Write
01	0	Memory Read
01	1	Memory Read
10	0	DMA Read
10	1	DMA Write
11	x	Reserved. If a peripheral performing a bus master cycle generates this value, the Intel ICH10 aborts the cycle.

5.4.1.4 Size

Bits[3:2] are reserved. The ICH10 always drives them to 00. Peripherals running bus master cycles are also supposed to drive 00 for bits 3:2; however, the ICH10 ignores those bits. Bits[1:0] are encoded as listed in Table 5-8.

Table 5-8. Transfer Size Bit Definition

Bits[1:0]	Size
00	8-bit transfer (1 byte)
01	16-bit transfer (2 bytes)
10	Reserved. The Intel ICH10 never drives this combination. If a peripheral running a bus master cycle drives this combination, the ICH10 may abort the transfer.
11	32-bit transfer (4 bytes)

5.4.1.5 SYNC

Valid values for the SYNC field are shown in Table 5-9.

Table 5-9. SYNC Bit Definition

Bits[3:0]	Indication
0000	**Ready:** SYNC achieved with no error. For DMA transfers, this also indicates DMA request deassertion and no more transfers desired for that channel.
0101	**Short Wait:** Part indicating wait-states. For bus master cycles, the Intel® ICH10 does not use this encoding. Instead, the ICH10 uses the Long Wait encoding (see next encoding below).
0110	**Long Wait:** Part indicating wait-states, and many wait-states will be added. This encoding driven by the ICH10 for bus master cycles, rather than the Short Wait (0101).
1001	**Ready More (Used only by peripheral for DMA cycle):** SYNC achieved with no error and more DMA transfers desired to continue after this transfer. This value is valid only on DMA transfers and is not allowed for any other type of cycle.
1010	**Error:** Sync achieved with error. This is generally used to replace the SERR# or IOCHK# signal on the PCI/ISA bus. It indicates that the data is to be transferred, but there is a serious error in this transfer. For DMA transfers, this not only indicates an error, but also indicates DMA request deassertion and no more transfers desired for that channel.

NOTES:
1. All other combinations are RESERVED.
2. If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

5.4.1.6 SYNC Time-Out

There are several error cases that can occur on the LPC interface. The ICH10 responds as defined in section 4.2.1.9 of the *Low Pin Count Interface Specification*, Revision 1.1 to the stimuli described therein. There may be other peripheral failure conditions; however, these are not handled by the ICH10.

5.4.1.7 SYNC Error Indication

The ICH10 responds as defined in section 4.2.1.10 of the *Low Pin Count Interface Specification,* Revision 1.1.

Upon recognizing the SYNC field indicating an error, the ICH10 treats this as an SERR by reporting this into the Device 31 Error Reporting Logic.

5.4.1.8 LFRAME# Usage

The ICH10 follows the usage of LFRAME# as defined in the *Low Pin Count Interface Specification,* Revision 1.1.

The ICH10 performs an abort for the following cases (possible failure cases):

- ICH10 starts a Memory, I/O, or DMA cycle, but no device drives a valid SYNC after four consecutive clocks.
- ICH10 starts a Memory, I/O, or DMA cycle, and the peripheral drives an invalid SYNC pattern.
- A peripheral drives an invalid address when performing bus master cycles.
- A peripheral drives an invalid value.

5.4.1.9 I/O Cycles

For I/O cycles targeting registers specified in the ICH10's decode ranges, the ICH10 performs I/O cycles as defined in the *Low Pin Count Interface Specification,* Revision 1.1. These are 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the ICH10 breaks the cycle up into multiple 8-bit transfers to consecutive I/O addresses.

Note: If the cycle is not claimed by any peripheral (and subsequently aborted), the ICH10 returns a value of all 1s (FFh) to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

5.4.1.10 Bus Master Cycles

The ICH10 supports Bus Master cycles and requests (using LDRQ#) as defined in the *Low Pin Count Interface Specification,* Revision 1.1. The ICH10 has two LDRQ# inputs, and thus supports two separate bus master devices. It uses the associated START fields for Bus Master 0 (0010b) or Bus Master 1 (0011b).

Note: The ICH10 does not support LPC Bus Masters performing I/O cycles. LPC Bus Masters should only perform memory read or memory write cycles.

5.4.1.11 LPC Power Management

LPCPD# Protocol

Same timings as for SUS_STAT#. Upon driving SUS_STAT# low, LPC peripherals drive LDRQ# low or tri-state it. ICH10 shuts off the LDRQ# input buffers. After driving SUS_STAT# active, the ICH10 drives LFRAME# low, and tri-states (or drive low) LAD[3:0].

Note: The *Low Pin Count Interface Specification,* Revision 1.1 defines the LPCPD# protocol where there is at least 30 µs from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The ICH10 asserts both SUS_STAT# (connects to LPCPD#) and PLTRST# (connects to LRST#) at the same time when the core logic is reset (via CF9h, PWROK, or SYS_RESET#, etc.). This is not inconsistent with the LPC LPCPD# protocol.

5.4.1.12 Configuration and Intel® ICH10 Implications

LPC I/F Decoders

To allow the I/O cycles and memory mapped cycles to go to the LPC interface, the ICH10 includes several decoders. During configuration, the ICH10 must be programmed with the same decode ranges as the peripheral. The decoders are programmed via the Device 31:Function 0 configuration space.

Note: The ICH10 cannot accept PCI write cycles from PCI-to-PCI bridges or devices with similar characteristics (specifically those with a "Retry Read" feature which is enabled) to an LPC device if there is an outstanding LPC read cycle towards the same PCI device or bridge. These cycles are not part of normal system operation, but may be encountered as part of platform validation testing using custom test fixtures.

Bus Master Device Mapping and START Fields

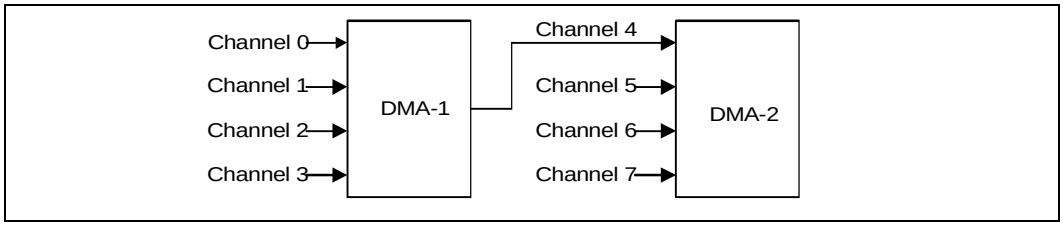
Bus Masters must have a unique START field. In the case of the ICH10 that supports two LPC bus masters, it drives 0010 for the START field for grants to bus master #0 (requested via LDRQ0#) and 0011 for grants to bus master #1 (requested via LDRQ1#.). Thus, no registers are needed to configure the START fields for a particular bus master.

5.5 DMA Operation (D31:F0)

The ICH10 supports LPC DMA using the ICH10's DMA controller. The DMA controller has registers that are fixed in the lower 64 KB of I/O space. The DMA controller is configured using registers in the PCI configuration space. These registers allow configuration of the channels for use by LPC DMA.

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Figure 5-3). DMA controller 1 (DMA-1) corresponds to DMA channels 0–3 and DMA controller 2 (DMA-2) corresponds to channels 5–7. DMA channel 4 is used to cascade the two controllers and defaults to cascade mode in the DMA Channel Mode (DCM) Register. Channel 4 is not available for any other purpose. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that software initiates. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

Figure 5-3. Intel® ICH10 DMA Controller



Each DMA channel is hardwired to the compatible settings for DMA device size: channels [3:0] are hardwired to 8-bit, count-by-bytes transfers, and channels [7:5] are hardwired to 16-bit, count-by-words (address shifted) transfers.

ICH10 provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-Compatible Current Register which holds the 16 least-significant bits of the 24-bit address, an ISA-Compatible Page Register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and auto-initialization following a DMA termination.

5.5.1 Channel Priority

For priority resolution, the DMA consists of two logical channel groups: channels 0–3 and channels 4–7. Each group may be in either fixed or rotate mode, as determined by the DMA Command Register.

DMA I/O slaves normally assert their DREQ line to arbitrate for DMA service. However, a software request for DMA service can be presented through each channel's DMA Request Register. A software request is subject to the same prioritization as any hardware request. See the detailed register description for Request Register programming information in Section 13.2.

5.5.1.1 Fixed Priority

The initial fixed priority structure is as follows:

High priority	Low priority
0, 1, 2, 3	5, 6, 7

The fixed priority ordering is 0, 1, 2, 3, 5, 6, and 7. In this scheme, channel 0 has the highest priority, and channel 7 has the lowest priority. Channels [3:0] of DMA-1 assume the priority position of channel 4 in DMA-2, thus taking priority over channels 5, 6, and 7.

5.5.1.2 Rotating Priority

Rotation allows for “fairness” in priority resolution. The priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group (0–3, 5–7).

Channels 0–3 rotate as a group of 4. They are always placed between channel 5 and channel 7 in the priority list.

Channel 5–7 rotate as part of a group of 4. That is, channels (5–7) form the first three positions in the rotation, while channel group (0–3) comprises the fourth position in the arbitration.

5.5.2 Address Compatibility Mode

When the DMA is operating, the addresses do not increment or decrement through the High and Low Page Registers. Therefore, if a 24-bit address is 01FFFFh and increments, the next address is 010000h, not 020000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 02FFFFh, not 01FFFFh. However, when the DMA is operating in 16-bit mode, the addresses still do not increment or decrement through the High and Low Page Registers but the page boundary is now 128 K. Therefore, if a 24-bit address is 01FFFEh and increments, the next address is 000000h, not 0100000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 03FFFEh, not 02FFFEh. This is compatible with the 82C37 and Page Register implementation used in the PC-AT. This mode is set after CPURST is valid.

5.5.3 Summary of DMA Transfer Sizes

Table 5-10 lists each of the DMA device transfer sizes. The column labeled “Current Byte/Word Count Register” indicates that the register contents represents either the number of bytes to transfer or the number of 16-bit words to transfer. The column labeled “Current Address Increment/Decrement” indicates the number added to or taken from the Current Address register after each DMA transfer cycle. The DMA Channel Mode Register determines if the Current Address Register will be incremented or decremented.

5.5.3.1 Address Shifting When Programmed for 16-Bit I/O Count by Words

Table 5-10. DMA Transfer Size

DMA Device Date Size And Word Count	Current Byte/Word Count Register	Current Address Increment/ Decrement
8-Bit I/O, Count By Bytes	Bytes	1
16-Bit I/O, Count By Words (Address Shifted)	Words	1

The ICH10 maintains compatibility with the implementation of the DMA in the PC AT that used the 82C37. The DMA shifts the addresses for transfers to/from a 16-bit device count-by-words.

Note: The least significant bit of the Low Page Register is dropped in 16-bit shifted mode. When programming the Current Address Register (when the DMA channel is in this mode), the Current Address must be programmed to an even address with the address value shifted right by one bit.

The address shifting is shown in Table 5-11.

Table 5-11. Address Shifting in 16-Bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address (Ch 0–3)	16-Bit I/O Programmed Address (Ch 5–7) (Shifted)
A0 A[16:1] A[23:17]	A0 A[16:1] A[23:17]	0 A[15:0] A[23:17]

NOTE: The least significant bit of the Page Register is dropped in 16-bit shifted mode.

5.5.4 Autoinitialize

By programming a bit in the DMA Channel Mode Register, a channel may be set up as an autoinitialize channel. When a channel undergoes autoinitialization, the original values of the Current Page, Current Address and Current Byte/Word Count Registers are automatically restored from the Base Page, Address, and Byte/Word Count Registers of that channel following TC. The Base Registers are loaded simultaneously with the Current Registers by the microprocessor when the DMA channel is programmed and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize, the channel is ready to perform another DMA service, without processor intervention, as soon as a valid DREQ is detected.

5.5.5 Software Commands

There are three additional special software commands that the DMA controller can execute. The three software commands are:

- Clear Byte Pointer Flip-Flop
- Master Clear
- Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

5.6 LPC DMA

DMA on LPC is handled through the use of the LDRQ# lines from peripherals and special encodings on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8 bit channels. Channels 5–7 are 16-bit channels. Channel 4 is reserved as a generic bus master request.

5.6.1 Asserting DMA Requests

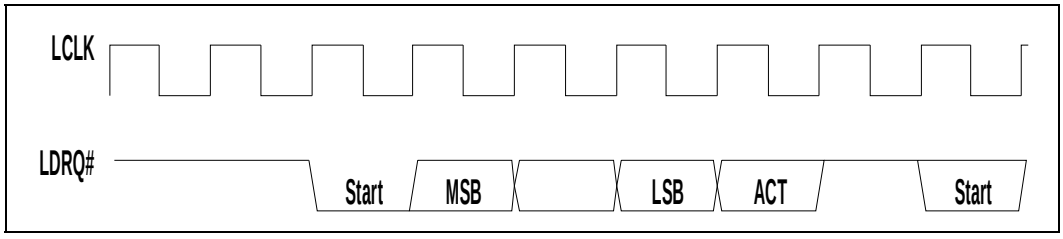
Peripherals that need DMA service encode their requested channel number on the LDRQ# signal. To simplify the protocol, each peripheral on the LPC I/F has its own dedicated LDRQ# signal (they may not be shared between two separate peripherals). The ICH10 has two LDRQ# inputs, allowing at least two devices to support DMA or bus mastering.

LDRQ# is synchronous with LCLK (PCI clock). As shown in Figure 5-4, the peripheral uses the following serial encoding sequence:

- Peripheral starts the sequence by asserting LDRQ# low (start bit). LDRQ# is high during idle conditions.
- The next three bits contain the encoded DMA channel number (MSB first).
- The next bit (ACT) indicates whether the request for the indicated DMA channel is active or inactive. The ACT bit is 1 (high) to indicate if it is active and 0 (low) if it is inactive. The case where ACT is low is rare, and is only used to indicate that a previous request for that channel is being abandoned.
- After the active/inactive indication, the LDRQ# signal must go high for at least 1 clock. After that one clock, LDRQ# signal can be brought low to the next encoding sequence.

If another DMA channel also needs to request a transfer, another sequence can be sent on LDRQ#. For example, if an encoded request is sent for channel 2, and then channel 3 needs a transfer before the cycle for channel 2 is run on the interface, the peripheral can send the encoded request for channel 3. This allows multiple DMA agents behind an I/O device to request use of the LPC interface, and the I/O device does not need to self-arbitrate before sending the message.

Figure 5-4. DMA Request Assertion through LDRQ#



5.6.2 Abandoning DMA Requests

DMA Requests can be deasserted in two fashions: on error conditions by sending an LDRQ# message with the 'ACT' bit set to 0, or normally through a SYNC field during the DMA transfer. This section describes boundary conditions where the DMA request needs to be removed prior to a data transfer.

There may be some special cases where the peripheral desires to abandon a DMA transfer. The most likely case of this occurring is due to a floppy disk controller which has overrun or underrun its FIFO, or software stopping a device prematurely.

In these cases, the peripheral wishes to stop further DMA activity. It may do so by sending an LDRQ# message with the ACT bit as 0. However, since the DMA request was seen by the ICH10, there is no assurance that the cycle has not been granted and will shortly run on LPC. Therefore, peripherals must take into account that a DMA cycle may still occur. The peripheral can choose not to respond to this cycle, in which case the host will abort it, or it can choose to complete the cycle normally with any random data.

This method of DMA deassertion should be prevented whenever possible, to limit boundary conditions both on the ICH10 and the peripheral.

5.6.3 General Flow of DMA Transfers

Arbitration for DMA channels is performed through the 8237 within the host. Once the host has won arbitration on behalf of a DMA channel assigned to LPC, it asserts LFRAME# on the LPC I/F and begins the DMA transfer. The general flow for a basic DMA transfer is as follows:

1. ICH10 starts transfer by asserting 0000b on LAD[3:0] with LFRAME# asserted.
2. ICH10 asserts 'cycle type' of DMA, direction based on DMA transfer direction.
3. ICH10 asserts channel number and, if applicable, terminal count.
4. ICH10 indicates the size of the transfer: 8 or 16 bits.
5. If a DMA read…
   - The ICH10 drives the first 8 bits of data and turns the bus around.
   - The peripheral acknowledges the data with a valid SYNC.
   - If a 16-bit transfer, the process is repeated for the next 8 bits.
6. If a DMA write…
   - The ICH10 turns the bus around and waits for data.
   - The peripheral indicates data ready through SYNC and transfers the first byte.
   - If a 16-bit transfer, the peripheral indicates data ready and transfers the next byte.
7. The peripheral turns around the bus.

5.6.4 Terminal Count

Terminal count is communicated through LAD[3] on the same clock that DMA channel is communicated on LAD[2:0]. This field is the CHANNEL field. Terminal count indicates the last byte of transfer, based upon the size of the transfer.

For example, on an 8-bit transfer size (SIZE field is 00b), if the TC bit is set, then this is the last byte. On a 16-bit transfer (SIZE field is 01b), if the TC bit is set, then the second byte is the last byte. The peripheral, therefore, must internalize the TC bit when the CHANNEL field is communicated, and only signal TC when the last byte of that transfer size has been transferred.

5.6.5 Verify Mode

Verify mode is supported on the LPC interface. A verify transfer to the peripheral is similar to a DMA write, where the peripheral is transferring data to main memory. The indication from the host is the same as a DMA write, so the peripheral will be driving data onto the LPC interface. However, the host will not transfer this data into main memory.

5.6.6 DMA Request Deassertion

An end of transfer is communicated to the ICH10 through a special SYNC field transmitted by the peripheral. An LPC device must not attempt to signal the end of a transfer by deasserting LDREQ#. If a DMA transfer is several bytes (e.g., a transfer from a demand mode device) the ICH10 needs to know when to deassert the DMA request based on the data currently being transferred.

The DMA agent uses a SYNC encoding on each byte of data being transferred, which indicates to the ICH10 whether this is the last byte of transfer or if more bytes are requested. To indicate the last byte of transfer, the peripheral uses a SYNC value of 0000b (ready with no error), or 1010b (ready with error). These encodings tell the ICH10 that this is the last piece of data transferred on a DMA read (ICH10 to peripheral), or the byte that follows is the last piece of data transferred on a DMA write (peripheral to ICH10).

When the ICH10 sees one of these two encodings, it ends the DMA transfer after this byte and deasserts the DMA request to the 8237. Therefore, if the ICH10 indicated a 16-bit transfer, the peripheral can end the transfer after one byte by indicating a SYNC value of 0000b or 1010b. The ICH10 does not attempt to transfer the second byte, and deasserts the DMA request internally.

If the peripheral indicates a 0000b or 1010b SYNC pattern on the last byte of the indicated size, then the ICH10 only deasserts the DMA request to the 8237 since it does not need to end the transfer.

If the peripheral wishes to keep the DMA request active, then it uses a SYNC value of 1001b (ready plus more data). This indicates to the 8237 that more data bytes are requested after the current byte has been transferred, so the ICH10 keeps the DMA request active to the 8237. Therefore, on an 8-bit transfer size, if the peripheral indicates a SYNC value of 1001b to the ICH10, the data will be transferred and the DMA request will remain active to the 8237. At a later time, the ICH10 will then come back with another START–CYCTYPE–CHANNEL–SIZE etc. combination to initiate another transfer to the peripheral.

The peripheral must not assume that the next START indication from the ICH10 is another grant to the peripheral if it had indicated a SYNC value of 1001b. On a single mode DMA device, the 8237 will re-arbitrate after every transfer. Only demand mode DMA devices can be assured that they will receive the next START indication from the ICH10.

Note: Indicating a 0000b or 1010b encoding on the SYNC field of an odd byte of a 16-bit channel (first byte of a 16-bit transfer) is an error condition.

Note: The host stops the transfer on the LPC bus as indicated, fills the upper byte with random data on DMA writes (peripheral to memory), and indicates to the 8237 that the DMA transfer occurred, incrementing the 8237's address and decrementing its byte count.

5.6.7 SYNC Field / LDRQ# Rules

Since DMA transfers on LPC are requested through an LDRQ# assertion message, and are ended through a SYNC field during the DMA transfer, the peripheral must obey the following rule when initiating back-to-back transfers from a DMA channel.

The peripheral must not assert another message for eight LCLKs after a deassertion is indicated through the SYNC field. This is needed to allow the 8237, that typically runs off a much slower internal clock, to see a message deasserted before it is re-asserted so that it can arbitrate to the next agent.

Under default operation, the host only performs 8-bit transfers on 8-bit channels and 16-bit transfers on 16-bit channels.

The method by which this communication between host and peripheral through system BIOS is performed is beyond the scope of this specification. Since the LPC host and LPC peripheral are motherboard devices, no “plug-n-play” registry is required.

The peripheral must not assume that the host is able to perform transfer sizes that are larger than the size allowed for the DMA channel, and be willing to accept a SIZE field that is smaller than what it may currently have buffered.

To that end, it is recommended that future devices that may appear on the LPC bus, that require higher bandwidth than 8-bit or 16-bit DMA allow, do so with a bus mastering interface and not rely on the 8237.

5.7 8254 Timers (D31:F0)

The ICH10 contains three counters that have fixed uses. All registers and functions associated with the 8254 timers are in the core well. The 8254 unit is clocked by a 14.31818 MHz clock.

Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value 1 counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation and only impacts the period of the REF_TOGGLE bit in Port 61. The initial count value is loaded one counter period after being written to the counter I/O address. The REF_TOGGLE bit will have a square wave behavior (alternate between 0 and 1) and will toggle at a rate based on the value in the counter. Programming the counter to anything other than Mode 2 will result in undefined behavior for the REF_TOGGLE bit.

Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see NMI Status and Control ports).

5.7.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word bits 5, 4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 5-12 lists the six operating modes for the interval counters.

Table 5-12. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

5.7.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

5.7.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through port 40h (counter 0), 41h (counter 1), or 42h (counter 2).

Note: Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of counter 2, the count can be stopped by writing to the GATE bit in port 61h.

5.7.2.2 Counter Latch Command

The Counter Latch command, written to port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

5.7.2.3 Read Back Command

The Read Back command, written to port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

5.8 8259 Interrupt Controllers (PIC) (D31:F0)

The ICH10 incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, mouse, and DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 core supports eight interrupts, numbered 0–7. Table 5-13 shows how the cores are connected.

Table 5-13. Interrupt Controller Core Connections

8259	8259 Input	Typical Interrupt Source	Connected Pin / Function
Master	0	Internal	Internal Timer / Counter 0 output / HPET #0
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave controller INTR output
	3	Serial Port A	IRQ3 via SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 via SERIRQ, PIRQ#
	5	Parallel Port / Generic	IRQ5 via SERIRQ, PIRQ#
	6	Floppy Disk	IRQ6 via SERIRQ, PIRQ#
	7	Parallel Port / Generic	IRQ7 via SERIRQ, PIRQ#
Slave	0	Internal Real Time Clock	Internal RTC / HPET #1
	1	Generic	IRQ9 via SERIRQ, SCI, TCO, or PIRQ#
	2	Generic	IRQ10 via SERIRQ, SCI, TCO, or PIRQ#
	3	Generic	IRQ11 via SERIRQ, SCI, TCO, or PIRQ#, or HPET #2
	4	PS/2 Mouse	IRQ12 via SERIRQ, SCI, TCO, or PIRQ#, or HPET #3
	5	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.
	6	SATA	SATA Primary (legacy mode), or via SERIRQ or PIRQ#
	7	SATA	SATA Secondary (legacy mode) or via SERIRQ or PIRQ#

The ICH10 cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the ICH10 PIC.

Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

Note: Active-low interrupt sources (e.g., the PIRQ#s) are inverted inside the ICH10. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term “high” indicates “active,” which means “low” on an originating PIRQ#.

5.8.1 Interrupt Handling

5.8.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 5-14 defines the IRR, ISR, and IMR.

Table 5-14. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode. This bit is set whether or not the interrupt is masked. However, a masked interrupt will not generate INTR.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

5.8.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated by the host bridge into a PCI Interrupt Acknowledge Cycle to the ICH10. The PIC translates this command into two internal INTA# pulses expected by the 8259 cores. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon bits [7:3] of the corresponding ICW2 register, combined with three bits representing the interrupt within that controller.

Table 5-15. Content of Interrupt Vector Byte

Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

5.8.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle. The cycle is translated into a PCI interrupt acknowledge cycle by the host bridge. This command is broadcast over PCI by the ICH10.
4. Upon observing its own interrupt acknowledge cycle on PCI, the ICH10 converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

5.8.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the ICH10, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

5.8.2.1 ICW1

An I/O write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the ICH10 PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

5.8.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

5.8.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the ICH10, IRQ2 is used. Therefore, bit 2 of ICW3 on the master controller is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

5.8.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

5.8.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

5.8.4 Modes of Operation

5.8.4.1 Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt. Interrupt priorities can be changed in the rotating priority mode.

5.8.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

5.8.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2; the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the rotate in automatic EOI mode which is set by (R=1, SL=0, EOI=0).

5.8.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO–L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=1, and LO–L2=IRQ level to receive bottom priority.

5.8.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in bit 7 if there is an interrupt, and the binary code of the highest priority level in bits 2:0.

5.8.4.6 Cascade Mode

The PIC in the ICH10 has one master 8259 and one slave 8259 cascaded onto the master through IRQ2. This configuration can handle up to 15 separate priority levels. The master controls the slaves through a three bit internal bus. In the ICH10, when the master drives 010b on this bus, the slave controller takes responsibility for returning the interrupt vector. An EOI command must be issued twice: once for the master and once for the slave.

5.8.4.7 Edge and Level Triggered Mode

In ISA systems this mode is programmed using bit 3 in ICW1, which sets level or edge for the entire controller. In the ICH10, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/ Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

5.8.4.8 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when AEOI bit in ICW4 is set to 1.

5.8.4.9 Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the ICH10, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI. An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

5.8.4.10 Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

5.8.5 Masking Interrupts

5.8.5.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

5.8.5.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern. The special mask mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

5.8.6 Steering PCI Interrupts

The ICH10 can be programmed to allow PIRQA#-PIRQH# to be routed internally to interrupts 3–7, 9–12, 14 or 15. The assignment is programmable through the PIRQx Route Control registers, located at 60–63h and 68–6Bh in Device 31:Function 0. One or more PIRQx# lines can be routed to the same IRQx input. If interrupt steering is not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line across the connector. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The ICH10 internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

Internal sources of the PIRQs, including SCI and TCO interrupts, cause the external PIRQ to be asserted. The ICH10 receives the PIRQ input, like all of the other external sources, and routes it accordingly.

5.9 Advanced Programmable Interrupt Controller (APIC) (D31:F0)

In addition to the standard ISA-compatible PIC described in the previous chapter, the ICH10 incorporates the APIC. While the standard interrupt controller is intended for use in a uni-processor system, APIC can be used in either a uni-processor or multi-processor system.

5.9.1 Interrupt Handling

The I/O APIC handles interrupts very differently than the 8259. Briefly, these differences are:

- **Method of Interrupt Transmission.** The I/O APIC transmits interrupts through memory writes on the normal datapath to the processor, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- **Interrupt Priority.** The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 can be given a higher priority than interrupt 3.
- **More Interrupts.** The I/O APIC in the ICH10 supports a total of 24 interrupts.
- **Multiple Interrupt Controllers.** The I/O APIC architecture allows for multiple I/O APIC devices in the system with their own interrupt vectors.

5.9.2 Interrupt Mapping

The I/O APIC within the ICH10 supports 24 APIC interrupts. Each interrupt has its own unique vector assigned by software. The interrupt vectors are mapped as follows, and match “Config 6” of the *Multi-Processor Specification*.

Table 5-16. APIC Interrupt Mapping[1] (Sheet 1 of 2)

IRQ #	Via SERIRQ	Direct from Pin	Via PCI Message	Internal Modules
0	No	No	No	Cascade from 8259 #1
1	Yes	No	Yes	
2	No	No	No	8254 Counter 0, HPET #0 (legacy mode)
3	Yes	No	Yes	
4	Yes	No	Yes	
5	Yes	No	Yes	
6	Yes	No	Yes	
7	Yes	No	Yes	
8	No	No	No	RTC, HPET #1 (legacy mode)
9	Yes	No	Yes	Option for SCI, TCO
10	Yes	No	Yes	Option for SCI, TCO
11	Yes	No	Yes	HPET #2, Option for SCI, TCO (Note2)
12	Yes	No	Yes	HPET #3 (Note 3)
13	No	No	No	FERR# logic
14	Yes	No	Yes	SATA Primary (legacy mode)
15	Yes	No	Yes	SATA Secondary (legacy mode)

Table 5-16. APIC Interrupt Mapping[1] (Sheet 2 of 2)

IRQ #	Via SERIRQ	Direct from Pin	Via PCI Message	Internal Modules
16	PIRQA#	PIRQA#	Yes	Internal devices are routable; see Section 10.1.54 though Section 10.1.60.
17	PIRQB#	PIRQB#		
18	PIRQC#	PIRQC#		
19	PIRQD#	PIRQD#		
20	N/A	PIRQE#[4]	Yes	Option for SCI, TCO, HPET #0,1,2, 3. Other internal devices are routable; see Section 10.1.54 through Section 10.1.60.
21	N/A	PIRQF#[4]		
22	N/A	PIRQG#[4]		
23	N/A	PIRQH#[4]		

NOTES:
1. When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources.
2. If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET #2. ICH10 hardware does not prevent sharing of IRQ 11.
3. If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET #3. ICH10 hardware does not prevent sharing of IRQ 12.
4. PIRQ[E:H] are Multiplexed with GPIO pins. Interrupts PIRQ[E:H] will not be exposed if they are configured as GPIOs.

5.9.3 PCI / PCI Express* Message-Based Interrupts

When external devices through PCI / PCI Express wish to generate an interrupt, they will send the message defined in the *PCI Express* Base Specification,* Revision 1.0a for generating INTA# - INTD#. These will be translated internal assertions/de-assertions of INTA# – INTD#.

5.9.4 Front Side Bus Interrupt Delivery

For processors that support Front Side Bus (FSB) interrupt delivery, the ICH10 requires that the I/O APIC deliver interrupt messages to the processor in a parallel manner, rather than using the I/O APIC serial scheme.

This is done by the ICH10 writing (via DMI) to a memory location that is snooped by the processor(s). The processor(s) snoop the cycle to know which interrupt goes active.

The following sequence is used:

1. When the ICH10 detects an interrupt event (active edge for edge-triggered mode or a change for level-triggered mode), it sets or resets the internal IRR bit associated with that interrupt.
2. Internally, the ICH10 requests to use the bus in a way that automatically flushes upstream buffers. This can be internally implemented similar to a DMA device request.
3. The ICH10 then delivers the message by performing a write cycle to the appropriate address with the appropriate data. The address and data formats are described below in Section 5.9.4.4.

Note: FSB Interrupt Delivery compatibility with processor clock control depends on the processor, not the ICH10.

5.9.4.1 Edge-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt.

5.9.4.2 Level-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt. If after the EOI the interrupt is still active, then another “Assert Message” is sent to indicate that the interrupt is still active.

5.9.4.3 Registers Associated with Front Side Bus Interrupt Delivery

Capabilities Indication: The capability to support Front Side Bus interrupt delivery is indicated via ACPI configuration techniques. This involves the BIOS creating a data structure that gets reported to the ACPI configuration software.

5.9.4.4 Interrupt Message Format

The ICH10 writes the message to PCI (and to the Host controller) as a 32-bit memory write cycle. It uses the formats shown in Table 5-17 and Table 5-18 for the address and data.

The local APIC (in the processor) has a delivery mode option to interpret Front Side Bus messages as a SMI in which case the processor treats the incoming interrupt as a SMI instead of as an interrupt. This does not mean that the ICH10 has any way to have a SMI source from ICH10 power management logic cause the I/O APIC to send an SMI message (there is no way to do this). The ICH10’s I/O APIC can only send interrupts due to interrupts which do not include SMI, NMI or INIT. This means that in IA-32/ Intel® 64 based platforms, Front Side Bus interrupt message format delivery modes 010 (SMI/PMI), 100 (NMI), and 101 (INIT) as indicated in this section, must not be used and is not supported. Only the hardware pin connection is supported by ICH10.

Table 5-17. Interrupt Message Address Format

Bit	Description
31:20	Will always be FEEh
19:12	**Destination ID:** This is the same as bits 63:56 of the I/O Redirection Table entry for the interrupt associated with this message.
11:4	**Extended Destination ID**: This is the same as bits 55:48 of the I/O Redirection Table entry for the interrupt associated with this message.
3	**Redirection Hint:** This bit is used by the processor host bridge to allow the interrupt message to be redirected. 0 = The message will be delivered to the agent (processor) listed in bits 19:12. 1 = The message will be delivered to an agent with a lower interrupt priority This can be derived from bits 10:8 in the Data Field (see below). The Redirection Hint bit will be a 1 if bits 10:8 in the delivery mode field associated with corresponding interrupt are encoded as 001 (Lowest Priority). Otherwise, the Redirection Hint bit will be 0
2	**Destination Mode:** This bit is used only the Redirection Hint bit is set to 1. If the Redirection Hint bit and the Destination Mode bit are both set to 1, then the logical destination mode is used, and the redirection is limited only to those processors that are part of the logical group as based on the logical ID.
1:0	Will always be 00.

Table 5-18. Interrupt Message Data Format

Bit	Description
31:16	Will always be 0000h.
15	**Trigger Mode:** 1 = Level, 0 = Edge. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
14	**Delivery Status:** 1 = Assert, 0 = Deassert. Only Assert messages are sent. This bit is always 1.
13:12	Will always be 00
11	**Destination Mode:** 1 = Logical. 0 = Physical. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
10:8	**Delivery Mode:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt. 000 = Fixed 100 = NMI 001 = Lowest Priority 101 = INIT 010 = SMI/PMI 110 = Reserved 011 = Reserved 111 = ExtINT
7:0	**Vector:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt.

5.9.5 IOxAPIC Address Remapping

To support Intel® Virtualization Technology, interrupt messages are required to go through similar address remapping as any other memory request. Address remapping allows for domain isolation for interrupts, so a device assigned in one domain is not allowed to generate an interrupt to another domain.

The address remapping is based on the Bus: Device: Function field associated with the requests. The internal APIC is required to initiate the interrupt message using a unique Bus: Device: function.

ICH10 allows BIOS to program the unique Bus: Device: Function address for the internal APIC. This address field does not change the APIC functionality and the APIC is not promoted as a stand-alone PCI device. See Device 31: Function 0 Offset 6Ch for additional information.

5.9.6 External Interrupt Controller Support

The ICH10 supports external APICs off of PCI Express ports, and does not support APICs on the PCI bus. The EOI special cycle is only forwarded to PCI Express ports.

5.10 Serial Interrupt (D31:F0)

The ICH10 supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the host, the ICH10, and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to PCI clock, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase.** Signal driven low
- **R** – **Recovery Phase.** Signal driven high
- **T** – **Turn-around Phase.** Signal released

The ICH10 supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 2–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: When the SATA controller is configured for legacy IDE mode, IRQ14 and IRQ15 are expected to behave as ISA legacy interrupts, which cannot be shared (i.e., through the Serial Interrupt pin). If IRQ14 and IRQ15 are shared with Serial Interrupt pin, then abnormal system behavior may occur. For example, IRQ14/15 may not be detected by ICH10's interrupt controller. When the SATA controller is not running in Native IDE mode, IRQ14 and IRQ15 are used as special interrupts. If the SATA controller is in native modes, these interrupts can be mapped to other devices accordingly.

5.10.1 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame. These two modes are: Continuous, where the ICH10 is solely responsible for generating the start frame; and Quiet, where a serial IRQ peripheral is responsible for beginning the start frame.

The mode that must first be entered when enabling the serial IRQ protocol is continuous mode. In this mode, the ICH10 asserts the start frame. This start frame is 4, 6, or 8 PCI clocks wide based upon the Serial IRQ Control Register, bits 1:0 at 64h in Device 31:Function 0 configuration space. This is a polling mode.

When the serial IRQ stream enters quiet mode (signaled in the Stop Frame), the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives the SERIRQ signal low. The ICH10 senses the line low and continues to drive it low for the remainder of the Start Frame. Since the first PCI clock of the start frame was driven by the peripheral in this mode, the ICH10 drives the SERIRQ line low for 1 PCI clock less than in continuous mode. This mode of operation allows for a quiet, and therefore, lower power operation.

5.10.2 Data Frames

Once the Start frame has been initiated, all of the SERIRQ peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase.** During this phase, the SERIRQ device drives SERIRQ low if the corresponding interrupt signal is low. If the corresponding interrupt is high, then the SERIRQ devices tri-state the SERIRQ signal. The SERIRQ line remains high due to pull-up resistors (there is no internal pull-up resistor on this signal, an external pull-up resistor is required). A low level during the IRQ0–1 and IRQ2–15 frames indicates that an active-high ISA interrupt is not being requested, but a low level during the PCI INT[A:D], SMI#, and IOCHK# frame indicates that an active-low interrupt is being requested.
- **Recovery Phase.** During this phase, the device drives the SERIRQ line high if in the Sample Phase it was driven low. If it was not driven in the sample phase, it is tri-stated in this phase.
- **Turn-around Phase.** The device tri-states the SERIRQ line.

5.10.3 Stop Frame

After all data frames, a Stop Frame is driven by the ICH10. The SERIRQ signal is driven low by the ICH10 for 2 or 3 PCI clocks. The number of clocks is determined by the SERIRQ configuration register. The number of clocks determines the next mode (see Table 5-19).

Table 5-19. Stop Frame Explanation

Stop Frame Width	Next Mode
2 PCI clocks	**Quiet Mode.** Any SERIRQ device may initiate a Start Frame
3 PCI clocks	**Continuous Mode.** Only the host (Intel® ICH10) may initiate a Start Frame

5.10.4 Specific Interrupts Not Supported via SERIRQ

There are three interrupts seen through the serial stream that are not supported by the ICH10. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0. Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8#. RTC interrupt can only be generated internally.
- IRQ13. Floating point error interrupt generated off of the processor assertion of FERR#.

The ICH10 ignores the state of these interrupts in the serial stream, and does not adjust their level based on the level seen in the serial stream.

5.10.5 Data Frame Format

Table 5-20 shows the format of the data frames. For the PCI interrupts (A–D), the output from the ICH10 is AND'd with the PCI input signal. This way, the interrupt can be signaled via both the PCI interrupt input signal and via the SERIRQ signal (they are shared).

Table 5-20. Data Frame Format

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can only be generated via the internal 8524
2	IRQ1	5	
3	SMI#	8	Causes SMI# if low. Will set the SERIRQ_SMI_STS bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally.
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	
14	IRQ13	41	Ignored. IRQ13 can only be generated from FERR#
15	IRQ14	44	Not attached to SATA logic
16	IRQ15	47	Not attached to SATA logic
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	Drive PIRQA#
19	PCI INTB#	56	Drive PIRQB#
20	PCI INTC#	59	Drive PIRQC#
21	PCI INTD#	62	Drive PIRQD#

5.11 Real Time Clock (D31:F0)

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 µs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is no longer supported. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in register B. It is up to the programmer to make sure that data stored in these locations is within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0–FFh in the Alarm bytes to indicate a don't care situation. All Alarm conditions must match to trigger an Alarm Flag, which could trigger an Alarm Interrupt if enabled. The SET bit must be 1 while programming these locations to avoid clashes with an update cycle. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read do not necessarily represent the true contents of those locations. Any RAM writes under the same conditions are ignored.

Note: The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions. The logic simply assumes that all years divisible by 4 are leap years. According to the Royal Observatory Greenwich, years that are divisible by 100 are typically not leap years. In every fourth century (years divisible by 400, like 2000), the 100-year-exception is over-ridden and a leap-year occurs. Note that the year 2100 will be the first time in which the current RTC implementation would incorrectly calculate the leap-year.

The ICH10 does not implement month/year alarms.

5.11.1 Update Cycles

An update cycle occurs once a second, if the SET bit of register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow is checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle will start at least 488 µs after the UIP bit of register A is asserted, and the entire cycle does not take more than 1984 µs to complete. The time and date RAM locations (0–9) are disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur at two times. When a updated-ended interrupt is detected, almost 999 ms is available to read and write the valid time and date data. If the UIP bit of Register A is detected to be low, there is at least 488 µs before the update cycle begins.

Warning: The overflow conditions for leap years adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before leap year occurs.

5.11.2 Interrupts

The real-time clock interrupt is internally routed within the ICH10 both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the ICH10, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

5.11.3 Lockable RAM Ranges

The RTC's battery-backed RAM supports two 8-byte ranges that can be locked via the configuration space. If the locking bits are set, the corresponding range in the RAM will not be readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

5.11.4 Century Rollover

The ICH10 detects a rollover when the Year byte (RTC I/O space, index offset 09h) transitions form 99 to 00. Upon detecting the rollover, the ICH10 sets the NEWCENTURY_STS bit (TCOBASE + 04h, bit 7). If the system is in an S0 state, this causes an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with century value. If the system is in a sleep state (S1–S5) when the century rollover occurs, the ICH10 also sets the NEWCENTURY_STS bit, but no SMI# is generated. When the system resumes from the sleep state, BIOS should check the NEWCENTURY_STS bit and update the century value in the RTC RAM.

5.11.5 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an ICH10-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

Using RTCRST# to Clear CMOS

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC_PWR_STS bit (D31:F0:A4h bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor. Table 5-21 shows which bits are set to their default state when RTCRST# is asserted. This RTCRST# jumper technique allows the jumper to be moved and then replaced—all while the system is powered off. Then, once booted, the RTC_PWR_STS can be detected in the set state.

Table 5-21. Configuration Bits Reset by RTCRST# Assertion

Bit Name	Register	Location	Bit(s)	Default State
Alarm Interrupt Enable (AIE)	Register B (General Configuration) (RTC_REGB)	I/O space (RTC Index + 0Bh)	5	X
Alarm Flag (AF)	Register C (Flag Register) (RTC_REGC)	I/O space (RTC Index + 0Ch)	5	X
SWSMI_RATE_SEL	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	7:6	0
SLP_S4# Minimum Assertion Width	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	5:4	0
SLP_S4# Assertion Stretch Enable	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	3	0
RTC Power Status (RTC_PWR_STS)	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	2	0
Power Failure (PWR_FLR)	General PM Configuration 3 Register (GEN_PMCON_3)	D31:F0:A4h	1	0
AFTERG3_EN	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	0	0
Power Button Override Status (PRBTNOR_STS)	Power Management 1 Status Register (PM1_STS)	PMBase + 00h	11	0
RTC Event Enable (RTC_EN)	Power Management 1 Enable Register (PM1_EN)	PMBase + 02h	10	0
Sleep Type (SLP_TYP)	Power Management 1 Control (PM1_CNT)	PMBase + 04h	12:10	0
PME_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	11	0
BATLOW_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	10	0
RI_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	8	0
NEWCENTURY_STS	TCO1 Status Register (TCO1_STS)	TCOBase + 04h	7	0
Intruder Detect (INTRD_DET)	TCO2 Status Register (TCO2_STS)	TCOBase + 06h	0	0
Top Swap (TS)	Backed Up Control Register (BUC)	Chipset Config Registers:Offset 3414h	0	X

Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS would detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note: The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

Warning: Do not implement a jumper on VccRTC to clear CMOS.

5.12 Processor Interface (D31:F0)

The ICH10 interfaces to the processor with a variety of signals

- Standard Outputs to processor: A20M#, SMI#, NMI, INIT#, INTR, STPCLK#, IGNNE#, CPUPWRGD, DPSLP#
- Standard Input from processor: FERR#, THRMTRIP#

Most ICH10 outputs to the processor use standard buffers. The ICH10 has separate V_{CPU_IO} signals that are pulled up at the system level to the processor voltage, and thus determines VOH for the outputs to the processor.

5.12.1 Processor Interface Signals

This section describes each of the signals that interface between the ICH10 and the processor(s). Note that the behavior of some signals may vary during processor reset, as the signals are used for frequency strapping.

5.12.1.1 A20M# (Mask A20)

The A20M# signal is active (low) when both of the following conditions are true:

- The ALT_A20_GATE bit (Bit 1 of PORT92 register) is a 0
- The A20GATE input signal is a 0

The A20GATE input signal is expected to be generated by the external microcontroller (KBC).

5.12.1.2 INIT# (Initialization)

The INIT# signal is active (driven low) based on any one of several events described in Table 5-22. When any of these events occur, INIT# is driven low for 16 PCI clocks, then driven high.

Note: The 16-clock counter for INIT# assertion halts while STPCLK# is active. Therefore, if INIT# is supposed to go active while STPCLK# is asserted, it actually goes active after STPCLK# goes inactive.

This section refers to INIT#, but applies to two signals: INIT# and INIT3_3V#, as INIT3_3V# is functionally identical to INIT#, but signaling at 3.3 V.

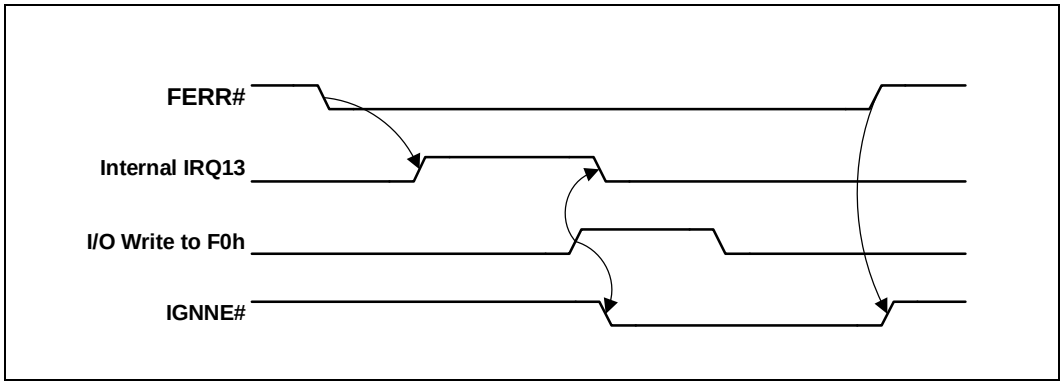
Table 5-22. INIT# Going Active

Cause of INIT# Going Active	Comment
Shutdown special cycle from processor observed on ICH-(G)MCH interconnect (from (G)MCH).	INIT# assertion based on value of Shutdown Policy Select register (SPS)
PORT92 write, where INIT_NOW (bit 0) transitions from 0-to-1.	
PORTCF9 write, where SYS_RST (bit 1) was a 0 and RST_CPU (bit 2) transitions from 0-to-1.	
RCIN# input signal goes low. RCIN# is expected to be driven by the external microcontroller (KBC).	0-to-1 transition on RCIN# must occur before the Intel® ICH10 will arm INIT# to be generated again. **NOTE:** RCIN# signal is expected to be low during S3, S4, and S5 states. Transition on the RCIN# signal in those states (or the transition to those states) may not necessarily cause the INIT# signal to be generated to the processor.
CPU BIST	To enter BIST, software sets CPU_BIST_EN bit and then does a full processor reset using the CF9 register.

5.12.1.3 FERR# / IGNNE# (Numeric Coprocessor Error / Ignore Numeric Error)

The ICH10 supports the coprocessor error function with the FERR#/IGNNE# pins. The function is enabled via the COPROC_ERR_EN bit (Chipset Config Registers:Offset 31FFh: bit 1 for Consumer Family and Offset 31FEh: bit 9 for Corporate family). FERR# is tied directly to the Coprocessor Error signal of the processor. If FERR# is driven active by the processor, IRQ13 goes active (internally). When it detects a write to the COPROC_ERR register (I/O Register F0h), the ICH10 negates the internal IRQ13 and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. IGNNE# is never driven active unless FERR# is active.

Figure 5-5. Coprocessor Error Timing Diagram



If COPROC_ERR_EN is not set, the assertion of FERR# will not generate an internal IRQ13, nor will the write to F0h generate IGNNE#.

5.12.1.4 NMI (Non-Maskable Interrupt)

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 5-23.

Table 5-23. NMI Sources

Cause of NMI	Comment
SERR# goes active (either internally, externally via SERR# signal, or via message from (G)MCH)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).
IOCHK# goes active via SERIRQ# stream (ISA system Error)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).

5.12.1.5 Stop Clock Request (STPCLK#)

The ICH10 power management logic controls this active-low signal. Refer to Section 5.13 for more information on the functionality of this signal.

5.12.1.6 CPU Power Good (CPUPWRGD)

This signal is connected to the processor's PWRGOOD input. This signal represents a logical AND of the ICH10's PWROK and VRMPWRGD signals.

5.12.1.7 Deeper Sleep (DPSLP#)

This active-low signal controls the internal gating of the processor's core clock. This signal asserts before and deasserts after the STP_CPU# signal to effectively stop the processor's clock (internally) in the states in which STP_CPU# can be used to stop the processor's clock externally.

5.12.2 Dual-Processor Issues

5.12.2.1 Signal Differences

In dual-processor designs, some of the processor signals are unused or used differently than for uniprocessor designs.

Table 5-24. DP Signal Differences

Signal	Difference
A20M# / A20GATE	Generally not used, but still supported by Intel® ICH10.
STPCLK#	Used for S1 State as well as preparation for entry to S3–S5 Also allows for THRM# based throttling (not via ACPI control methods). Should be connected to both processors.
FERR# / IGNNE#	Generally not used, but still supported by ICH10.

5.12.2.2 Power Management

For multiple-processor (or Multiple-core) configurations in which more than one Stop Grant cycle may be generated, the (G)MCH is expected to count Stop Grant cycles and only pass the last one through to the ICH10. This prevents the ICH10 from getting out of sync with the processor on multiple STPCLK# assertions.

Because the S1 state will have the STPCLK# signal active, the STPCLK# signal can be connected to both processors. However, for ACPI implementations, the BIOS must indicate that the ICH10 only supports the C1 state for dual-processor designs.

In going to the S1 state, multiple Stop-Grant cycles will be generated by the processors. It is assumed that prior to setting the SLP_EN bit (which causes the transition to the S1 state), the processors will not be executing code that is likely to delay the Stop-Grant cycles.

In going to the S3, S4, or S5 states, the system will appear to pass through the S1 state; thus, STPCLK# and SLP# are also used. During the S3, S4, and S5 states, both processors will lose power. Upon exit from those states, the processors will have their power restored.

5.13 Power Management (D31:F0)

5.13.1 Features

- Support for *Advanced Configuration and Power Interface, Version 3.0a (ACPI)* providing power and thermal management
  - — ACPI 24-Bit Timer
  - — Software initiated throttling of processor performance for Thermal and Power Reduction
  - — Hardware Override to throttle processor performance if system too hot
  - — SCI and SMI# Generation
  - — ACPI C2 state Stop-Grant state (using STPCLK# signal) halts processor's instruction stream
- PCI PME# signal for Wake Up from Low-Power states
- System Clock Control
  - — ACPI C3 State: Ability to halt processor clock (but not memory clock)
  - — ACPI C4 State: Ability to lower processor voltage.
- System Sleep State Control
  - — ACPI S1 state: Stop Grant (using STPCLK# signal) halts processor's instruction stream (only STPCLK# active)
  - — ACPI S3 state — Suspend to RAM (STR)
  - — ACPI S4 state — Suspend-to-Disk (STD)
  - — ACPI G2/S5 state — Soft Off (SOFF)
  - — Power Failure Detection and Recovery
- Intel Management Engine Power Management Support
  - — New Wake events from the Intel Management Engine (enabled from all S-States including Catastrophic S5 conditions)
- Streamlined Legacy Power Management for APM-Based Systems

5.13.2 Intel® ICH10 and System Power States

Table 5-25 shows the power states defined for ICH10-based platforms. The state names generally match the corresponding ACPI states.

Table 5-25. General Power States for Systems Using Intel® ICH10

State / Substates	Legacy Name / Description
G0/S0/C0	**Full On:** Processor operating. Individual devices may be shut down to save power. The different processor operating levels are defined by Cx states, as shown in Table 5-26. Within the C0 state, the Intel® ICH10 can throttle the processor using the STPCLK# signal to reduce power consumption. The throttling can be initiated by software or by the operating system or BIOS.
G0/S0/C1	**Auto-Halt:** Processor has executed an AutoHalt instruction and is not executing code. The processor snoops the bus and maintains cache coherency.
G0/S0/C2	**Stop-Grant:** The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream, and remains in that state until the STPCLK# signal goes inactive. In the Stop-Grant state, the processor snoops the bus and maintains cache coherency.
G0/S0/C3	**Stop-Clock:** The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream. ICH10 then asserts DPSLP# followed by STP_CPU#, which forces the clock generator to stop the processor clock. Accesses to memory (by graphics, PCI, or internal units) is not permitted while in a C3 state.
G0/S0/C4	**Stop-Clock with Lower Processor Voltage:** This closely resembles the G0/S0/C3 state. However, after the ICH10 has asserted STP_CPU#, it then lowers the voltage to the processor. This reduces the leakage on the processor. Prior to exiting the C4 state, the ICH10 increases the voltage to the processor.
G1/S1	**Stop-Grant:** Similar to G0/S0/C2 state. Note: The behavior for this state is slightly different when supporting Intel 64 processors.
G1/S3	**Suspend-To-RAM (STR):** The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
G2/S5	**Soft Off (SOFF):** System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
G3	**Mechanical OFF (MOFF):** System context not maintained. All power is shut off except for the RTC. No “Wake” events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the “waking” logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3 bit in the GEN_PMCON3 register (D31:F0, offset A4). Refer to Table 5-33 for more details.

Table 5-26 shows the transitions rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. For example, in going from S0 to S1, it may appear to pass through the G0/S0 states. These intermediate transitions and states are not listed in the table.

Table 5-26. State Transition Rules for Intel® ICH10

Present State	Transition Trigger	Next State
G0/S0/C0	• Processor halt instruction • Level 2 Read • Level 3 Read • Level 4 Read • SLP_EN bit set • Power Button Override • Mechanical Off/Power Failure	• G0/S0/C1 • G0/S0/C2 • G0/S0/C3 or G0/S0/C4 - depending on C4onC3_EN bit (D31:F0:Offset A0h:bit 7) and BM_STS_ZERO_EN bit (D31:F0:Offset A9h:bit 2) • G1/Sx or G2/S5 state • G2/S5 • G3
G0/S0/C1	• Any Enabled Break Event • STPCLK# goes active • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0/C2 • G2/S5 • G3
G0/S0/C2	• Any Enabled Break Event • Power Button Override • Power Failure • Previously in C3/C4 and bus masters idle	• G0/S0/C0 • G2/S5 • G3 • C3 or C4 - depending on PDME bit (D31:F0: Offset A9h: bit 4)
G0/S0/C3	• Any Enabled Break Event • Any Bus Master Event • Power Button Override • Power Failure • Previously in C4 and bus masters idle	• G0/S0/C0 • G0/S0/C2 - if PUME bit (D31:F0: Offset A9h: bit 3) is set, else G0/S0/C0 • G2/S5 • G3 • C4 - depending on PDME bit (D31:F0: Offset A9h: bit 4
G0/S0/C4	• Any Enabled Break Event • Any Bus Master Event • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0/C2 - if PUME bit (D31:F0: Offset A9h: bit 3) is set, else G0/S0/C0 • G2/S5 • G3
G1/S1, G1/S3, or G1/S4	• Any Enabled Wake Event • Power Button Override • Power Failure	• G0/S0/C0 • G2/S5 • G3
G2/S5	• Any Enabled Wake Event • Power Failure	• G0/S0/C0 • G3
G3	• Power Returns	• Optional to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other wake event). (See Note 1)

NOTES:
1. Some wake events can be preserved through power failure.

5.13.3 System Power Planes

The system has several independent power planes, as described in Table 5-27. Note that when a particular power plane is shut off, it should go to a 0 V level.

Table 5-27. System Power Plane

Plane	Controlled By	Description
CPU	SLP_S3# signal	The SLP_S3# signal can be used to cut the power to the processor completely. The DPRSLPVR support allows lowering the processor's voltage during the C4 state.
MAIN	SLP_S3# signal	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. The processor, devices on the PCI bus, LPC I/F, and graphics will typically be shut off when the Main power plane is shut, although there may be small subsections powered.
MEMORY	SLP_S4# signal SLP_S5# signal	When the SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4. Since the memory context does not need to be preserved in the S4 state, the power to the memory can also be shut down. When SLP_S5# goes active, power can be shut to any circuit not required to wake the system from the S5 state. Since the memory context does not need to be preserved in the S5 state, the power to the memory can also be shut.
Link Controller	SLP_M#	This pin is asserted when the manageability platform goes to MOff. Depending on the platform, this pin may be used to control the (G)MCH, ICH controller link power planes, the clock chip power, and the SPI flash power.
DEVICE[n]	GPIO	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.

5.13.4 SMI#/SCI Generation

On any SMI# event taking place, ICH10 asserts SMI# to the processor, which causes it to enter SMM space. SMI# remains active until the EOS bit is set. When the EOS bit is set, SMI# goes inactive for a minimum of 4 PCI clocks. If another SMI event occurs, SMI# is driven active again.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts 9, 10, 11, 20, 21, 22, or 23. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not (see Section 13.1.3). The interrupt remains asserted until all SCI sources are removed.

Table 5-28 shows which events can cause an SMI# and SCI. Note that some events can be programmed to cause either an SMI# or SCI. The usage of the event for SCI (instead of SMI#) is typically associated with an ACPI-based system. Each SMI# or SCI source has a corresponding enable and status bit.

Table 5-28. Causes of SMI# and SCI (Sheet 1 of 2)

Cause	SCI	SMI	Additional Enables	Where Reported
PME#	Yes	Yes	PME_EN=1	PME_STS
PME_B0 (Internal, Bus 0, PME-Capable Agents)	Yes	Yes	PME_B0_EN=1	PME_B0_STS
PCI Express* PME Messages	Yes	Yes	PCI_EXP_EN=1 (Not enabled for SMI)	PCI_EXP_STS
PCI Express Hot Plug Message	Yes	Yes	HOT_PLUG_EN=1 (Not enabled for SMI)	HOT_PLUG_STS
Power Button Press	Yes	Yes	PWRBTN_EN=1	PWRBTN_STS
Power Button Override (Note 7)	Yes	No	None	PRBTNOR_STS
RTC Alarm	Yes	Yes	RTC_EN=1	RTC_STS
Ring Indicate	Yes	Yes	RI_EN=1	RI_STS
USB#1 wakes	Yes	Yes	USB1_EN=1	USB1_STS
USB#2 wakes	Yes	Yes	USB2_EN=1	USB2_STS
USB#3 wakes	Yes	Yes	USB3_EN=1	USB3_STS
USB#4 wakes	Yes	Yes	USB4_EN=1	USB4_STS
USB#5 wakes	Yes	Yes	USB5_EN=1	USB5_STS
USB#6 wakes	Yes	Yes	USB6_EN=1	USB6_STS
THRM# pin active	Yes	Yes	THRM_EN=1	THRM_STS
ACPI Timer overflow (2.34 sec.)	Yes	Yes	TMROF_EN=1	TMROF_STS
Any GPI	Yes	Yes	GPI[x]_Route=10 (SCI) GPI[x]_Route=01 (SMI) GPE0[x]_EN=1	GPI[x]_STS GPE0_STS
TCO SCI Logic	Yes	No	TCOSCI_EN=1	TCOSCI_STS
TCO SCI message from (G)MCH	Yes	No	none	MCHSCI_STS
TCO SMI Logic	No	Yes	TCO_EN=1	TCO_STS
TCO SMI — Year 2000 Rollover	No	Yes	none	NEWCENTURY_STS
TCO SMI — TCO TIMEROUT	No	Yes	none	TIMEOUT
TCO SMI — OS writes to TCO_DAT_IN register	No	Yes	none	OS_TCO_SMI
TCO SMI — Message from (G)MCH	No	Yes	none	MCHSMI_STS
TCO SMI — NMI occurred (and NMIs mapped to SMI)	No	Yes	NMI2SMI_EN=1	NMI2SMI_STS
TCO SMI — INTRUDER# signal goes active	No	Yes	INTRD_SEL=10	INTRD_DET
TCO SMI[8] — Change of the BIOSWP bit from 0 to 1	No	Yes	BC.LE=1	BIOSWR_STS

Table 5-28. Causes of SMI# and SCI (Sheet 2 of 2)

Cause	SCI	SMI	Additional Enables	Where Reported
TCO SMI — Write attempted to BIOS	No	Yes	BIOSWP=1	BIOSWR_STS
BIOS_RLS written to	Yes	No	GBL_EN=1	GBL_STS
GBL_RLS written to	No	Yes	BIOS_EN=1	BIOS_STS
Write to B2h register	No	Yes	APMC_EN = 1	APM_STS
Periodic timer expires	No	Yes	PERIODIC_EN=1	PERIODIC_STS
64 ms timer expires	No	Yes	SWSMI_TMR_EN=1	SWSMI_TMR_STS
Enhanced USB Legacy Support Event	No	Yes	LEGACY_USB2_EN = 1	LEGACY_USB2_STS
Enhanced USB Intel Specific Event	No	Yes	INTEL_USB2_EN = 1	INTEL_USB2_STS
UHCI USB Legacy logic	No	Yes	LEGACY_USB_EN=1	LEGACY_USB_STS
Serial IRQ SMI reported	No	Yes	none	SERIRQ_SMI_STS
Device monitors match address in its range	No	Yes	none	DEVTRAP_STS
SMBus Host Controller	No	Yes	SMB_SMI_EN Host Controller Enabled	SMBus host status reg.
SMBus Slave SMI message	No	Yes	none	SMBUS_SMI_STS
SMBus SMBALERT# signal active	No	Yes	none	SMBUS_SMI_STS
SMBus Host Notify message received	No	Yes	HOST_NOTIFY_INTREN	SMBUS_SMI_STS HOST_NOTIFY_STS
Access microcontroller 62h/66h	No	Yes	MCSMI_EN	MCSMI_STS
SLP_EN bit written to 1	No	Yes	SMI_ON_SLP_EN=1	SMI_ON_SLP_EN_STS
USB Per-Port Registers Write Enable bit changes to 1.	No	Yes	USB2_EN=1, Write_Enable_SMI_Enable=1	USB2_STS, Write Enable Status
Write attempted to BIOS	No	Yes	BIOSWPD = 0	BIOSWR_STS
GPIO Lockdown Enable bit changes from ‘1’ to ‘0’.	No	Yes	GPIO_UNLOCK_SMI_EN=1	GPIO_UNLOCK_SMI_STS

NOTES:
1. SCI_EN must be 1 to enable SCI. SCI_EN must be 0 to enable SMI.
2. SCI can be routed to cause interrupt 9:11 or 20:23 (20:23 only available in APIC mode).
3. GBL_SMI_EN must be 1 to enable SMI.
4. EOS must be written to 1 to re-enable SMI for the next 1.
5. ICH10 must have SMI# fully enabled when ICH10 is also enabled to trap cycles. If SMI# is not enabled in conjunction with the trap enabling, then hardware behavior is undefined.
6. Only GPI[15:0] may generate an SMI# or SCI.
7. When a power button override first occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PRBTNOR_STS) is not cleared prior to setting SCI_EN.
8. This SMI is a synchronous event.

PCI Express ports and the (G)MCH (via DMI) have the ability to cause PME using messages. When a PME message is received, ICH10 will set the PCI_EXP_STS bit. If the PCI_EXP_EN bit is also set, the ICH10 can cause an SCI via the GPE1_STS register.

PCI Express has a Hot-Plug mechanism and is capable of generating a SCI via the GPE1 register. It is also capable of generating an SMI. However, it is not capable of generating a wake event.

5.13.5 Dynamic Processor Clock Control

The ICH10 has extensive control for dynamically starting and stopping system clocks. The clock control is used for transitions among the various S0/Cx states, and processor throttling. Each dynamic clock control method is described in this section. The various sleep states may also perform types of non-dynamic clock control.

The ICH10 supports the ACPI C0, C1, C2, C3, and C4 states.

The Dynamic Processor Clock control is handled using the following signals:

- STPCLK#: Used to halt processor instruction stream.
- STP_CPU#: Used to stop processor's clock
- DPSLP#: Used to force Deeper Sleep for processor.
- DPRSLPVR: Used to lower voltage of VRM during C4 state.
- DPRSTP#: Used to alert the processor of C4 state. Also works in conjunction with DPRSLPVR to communicate to the VRM whether a slow or fast voltage ramp should be used.

The C1 state is entered based on the processor performing an auto halt instruction.

The C2 state is entered based on the processor reading the Level 2 register in the ICH10.

The C2 state can also be entered from C3 or C4 states if bus masters require snoops and the PUME bit (D31:F0: Offset A9h: bit 3) is set.

The C3 state is entered based on the processor reading the Level 3 register in the ICH10 and when the C4onC3_EN bit is clear (D31:F0:Offset A0:bit 7). This state can also be entered after a temporary return to C2 from a prior C3 or C4 state.

The C4 state is entered based on the processor reading the Level 4 register in the ICH10, or by reading the Level 3 register when the C4onC3_EN bit is set. This state can also be entered after a temporary return to C2 from a prior C4 state.

A C1, C2, C3, or C4 state ends due to a Break event. Based on the break event, the ICH10 returns the system to C0 state.

Table 5-29 lists the possible break events from C2, C3, or C4. The break events from C1 are indicated in the processor's datasheet.

Table 5-29. Break Events

Event	Breaks from	Comment
Any unmasked interrupt goes active	C2	IRQ[0:15] when using the 8259s, IRQ[0:23] for I/O APIC. Since SCI is an interrupt, any SCI will also be a break event.
Any internal event that cause an NMI or SMI#	C2	Many possible sources
Any internal event that cause INIT# to go active	C2	Could be indicated by the keyboard controller via the RCIN input signal.
Any bus master request (internal, external or DMA, or BMBUSY#) goes active and BM_RLD=1 (D31:F0:Offset PMBASE+04h: bit 1)	C3, C4	Need to wake up processor so it can do snoops Note: If the PUME bit (D31:F0: Offset A9h: bit 3) is set, then bus master activity will NOT be treated as a break event. Instead, there will be a return only to the C2 state.
Processor Pending Break Event Indication	C2	Only available if FERR# enabled for break event indication (See FERR# Mux Enable in GCS, Chipset Config Registers:Offset 3410h:bit 6)
REQ-C0 Message from (G)MCH	C2	Can be sent at any time after the Ack-C2 message and before the Ack-C0 message, when not in C0 state.

5.13.5.1 Slow C4 Exit

In order to eliminate the audible noise caused by aggressive voltage ramps when exiting C4 the states at a regular, periodic frequency, the ICH10 supports a method to slow down the voltage ramp at the processor VR for certain break events. If enabled for this behavior, the ICH10 treats IRQ0 and IRQ8 as “slow” break events since both of these can be the system timer tick interrupt. Rather than carefully tracking the interrupt and timer configuration information to track the one correct interrupt, it was deemed acceptable to simplify the logic and slow the break exit sequence for both interrupts. Other break event sources invoke the normal exit timings.

The ICH10 indicates that a slow voltage ramp is desired by deasserting DPRSTP# (high) and leaving DPRSLPVR asserted (high). The normal voltage ramp rate is communicated by deasserting DPRSTP# (high) and deasserting DPRSLPVR (low).

The ICH10 waits an additional delay before starting the normal voltage ramp timer during the C4 or C5 exit sequence. If a “fast” break event occurs during the additional, slow-Exit time delay, the ICH10 quickly deasserts DPRSLPVR (low), thereby speeding up the voltage ramp and reducing the delay to a value that is typically seen by the device in the past. In the event that a fast break event and a slow break event occur together, the fast flow is taken.

5.13.5.2 Transition Rules among S0/Cx and Throttling States

The following priority rules and assumptions apply among the various S0/Cx and throttling states:

- Entry to any S0/Cx state is mutually exclusive with entry to any S1–S5 state. This is because the processor can only perform one register access at a time and Sleep states have higher priority than thermal throttling.
- When the SLP_EN bit is set (system going to a S1 - S5 sleep state), the THTL_EN and FORCE_THTL bits can be internally treated as being disabled (no throttling while going to sleep state).
- If the THTL_EN or FORCE_THTL bits are set, and a Level 2, Level 3 or Level 4 read then occurs, the system should immediately go and stay in a C2, C3 or C4 state until a break event occurs. A Level 2, Level 3 or Level 4 read has higher priority than the software initiated throttling.
- After an exit from a C2, C3 or C4 state (due to a Break event), and if the THTL_EN or FORCE_THTL bits are still set the system will continue to throttle STPCLK#. Depending on the time of break event, the first transition on STPCLK# active can be delayed by up to one THRM period (1024 PCI clocks = 30.72 µs).
- The Host controller must post Stop-Grant cycles in such a way that the processor gets an indication of the end of the special cycle prior to the ICH10 observing the Stop-Grant cycle. This ensures that the STPCLK# signals stays active for a sufficient period after the processor observes the response phase.
- If in the C1 state and the STPCLK# signal goes active, the processor will generate a Stop-Grant cycle, and the system should go to the C2 state. When STPCLK# goes inactive, it should return to the C1 state.

5.13.5.3 Deferred C3/C4

Due to the new DMI protocol, if there is any bus master activity (other than true isochronous), then the C0 to C3 transition will pause at the C2 state. ICH10 will keep the processor in a C2 state until:

- ICH10 sees no bus master activity.
- A break event occurs. In this case, the ICH10 will perform the C2 to C0 sequence. Note that bus master traffic is not a break event in this case.

To take advantage of the Deferred C3/C4 mode, the BM_STS_ZERO_EN bit must be set. This will cause the BM_STS bit to read as 0 even if some bus master activity is present. If this is not done, then the software may avoid even attempting to go to the C3 or C4 state if it sees the BM_STS bit as 1.

If the PUME bit (D31:F0: Offset A9h: bit 3) is 0, then the ICH10 will treat bus master activity as a break event. When reaching the C2 state, if there is any bus master activity, the ICH10 will return the processor to a C0 state.

5.13.5.4 POPUP (Auto C3/C4 to C2)

When the PUME bit (D31:F0: Offset A9h: bit 3) is set, the ICH10 enables a mode of operation where standard (non-isochronous) bus master activity will not be treated as a full break event from the C3 or C4 states. Instead, these will be treated merely as bus master events and return the platform to a C2 state, and thus allow snoops to be performed.

After returning to the C2 state, the bus master cycles will be sent to the (G)MCH, even if the ARB_DIS bit is set.

5.13.5.5 POPDOWN (Auto C2 to C3/C4)

After returning to the C2 state from C3/C4, it the PDME bit (D31:F0: Offset A9h: bit 4) is set, the platform can return to a C3 or C4 state (depending on where it was prior to going back up to C2). This behaves similar to the Deferred C3/C4 transition, and will keep the processor in a C2 state until:

- Bus masters are no longer active.
- A break event occurs. Note: Bus master traffic is not a break event in this case.

5.13.6 Sleep States

5.13.6.1 Sleep State Overview

The ICH10 directly supports different sleep states (S1–S5), which are entered by setting the SLP_EN bit, or due to a Power Button press. The entry to the Sleep states is based on several assumptions:

- Entry to a Cx state is mutually exclusive with entry to a Sleep state. This is because the processor can only perform one register access at a time. A request to Sleep always has higher priority than throttling.
- Prior to setting the SLP_EN bit, the software turns off processor-controlled throttling. Note that thermal throttling cannot be disabled, but setting the SLP_EN bit disables thermal throttling (since S1–S5 sleep state has higher priority).
- The G3 state cannot be entered via any software mechanism. The G3 state indicates a complete loss of power.

5.13.6.2 Initiating Sleep State

Sleep states (S1–S5) are initiated by:

- Masking interrupts, turning off all bus master enable bits, setting the desired type in the SLP_TYP field, and then setting the SLP_EN bit. The hardware then attempts to gracefully put the system into the corresponding Sleep state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state is less graceful, since there are no dependencies on observing Stop-Grant cycles from the processor or on clocks other than the RTC clock.
- Assertion of the THRMTRIP# signal will cause a transition to the S5 state. This can occur when system is in S0 or S1 state.

Table 5-30. Sleep Types

Sleep Type	Comment
S1	Intel ICH10 asserts the STPCLK# signal. This lowers the processor's power consumption. No snooping is possible in this state.
S3	ICH10 asserts SLP_S3#. The SLP_S3# signal controls the power to non-critical circuits. Power is only retained to devices needed to wake from this sleeping state, as well as to the memory.
S4	ICH10 asserts SLP_S3# and SLP_S4#. The SLP_S4# signal shuts off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	Same power state as S4. ICH10 asserts SLP_S3#, SLP_S4# and SLP_S5#.

5.13.6.3 Exiting Sleep States

Sleep states (S1–S5) are exited based on Wake events. The Wake events forces the system to a full on state (S0), although some non-critical subsystems might still be shut off and have to be brought back manually. For example, the hard disk may be shut off during a sleep state, and have to be enabled via a GPIO pin before it can be used.

Upon exit from the ICH10-controlled Sleep states, the WAK_STS bit is set. The possible causes of Wake Events (and their restrictions) are shown in Table 5-31.

Table 5-31. Causes of Wake Events

Cause	States Can Wake From	How Enabled
RTC Alarm	S1–S5 (Note 1)	Set RTC_EN bit in PM1_EN register
Power Button	S1–S5	Always enabled as Wake event. (Note 2).
GPI[0:15]	S1–S5 (Note 1)	GPE0_EN register **NOTE:** GPIs that are in the core well are not capable of waking the system from sleep states when the core well is not powered.
Classic USB	S1–S4	Set USB1_EN, USB 2_EN, USB3_EN, USB4_EN, USB5_EN, and USB6_EN bits in GPE0_EN register
LAN	S1–S5	Will use PME#. Wake enable set with LAN logic.
RI#	S1–S5 (Note 1)	Set RI_EN bit in GPE0_EN register
Intel® High Definition Audio	S1–S5	Event sets PME_B0_STS bit; PM_B0_EN must be enabled. Can not wake from S5 state if it was entered due to power failure or power button override.
Primary PME#	S1–S5 (Note 1)	PME_B0_EN bit in GPE0_EN register
Secondary PME#	S1–S5	Set PME_EN bit in GPE0_EN register.
PCI_EXP_WAKE#	S1–S5	PCI_EXP_WAKE bit (Note 3)
SATA	S1	Set PME_EN bit in GPE0_EN register. (Note 4)
PCI_EXP PME Message	S1	Must use the PCI Express* WAKE# pin rather than messages for wake from S3,S4, or S5.
SMBALERT#	S1–S5	Always enabled as Wake event
SMBus Slave Wake Message (01h)	S1–S5	Wake/SMI# command always enabled as a Wake event. **NOTE:** SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override. (Note 2).
SMBus Host Notify message received	S1–S5	HOST_NOTIFY_WKEN bit SMBus Slave Command register. Reported in the SMB_WAK_STS bit in the GPEO_STS register.
ME Non-Maskable Wake	S1–S5	Always enabled as Wake event. (Note 2).

NOTES:

1. This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software, or if there is a power failure.
2. If in the S5 state due to a power button override or THRMTRIP#, the possible wake events are due to Power Button, Hard Reset Without Cycling (See Command Type 3 in Table 5-53), Hard Reset System (See Command Type 4 in Table 5-53), Wake SMBus Slave Message (01h), and ME initiated non-maskable wake.

3. When the WAKE# pin is active and the PCI Express device is enabled to wake the system, the ICH10 will wake the platform.
4. SATA can only trigger a wake event in S1, but if PME is asserted prior to S3/S4/S5 entry and software does not clear the PME_B0_STS, a wake event would still result.

It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from sleep states where the core well is powered. Also, only certain GPIs are "ACPI Compliant," meaning that their Status and Enable bits reside in ACPI I/O space. Table 5-32 summarizes the use of GPIs as wake events.

Table 5-32. GPI Wake Events

GPI	Power Well	Wake From	Notes
GPI[7:0]	Core	S1	ACPI Compliant
GPI[15:8]	Suspend	S1–S5	ACPI Compliant

The latency to exit the various Sleep states varies greatly and is heavily dependent on power supply design, so much so that the exit latencies due to the ICH10 are insignificant.

5.13.6.4 PCI Express* WAKE# Signal and PME Event Message

PCI Express ports can wake the platform from any sleep state (S1, S3, S4, or S5) using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express ports and the (G)MCH (via DMI) have the ability to cause PME using messages. When a PME message is received, ICH10 will set the PCI_EXP_STS bit.

5.13.6.5 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only three possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH10 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V_{CC}-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

The ICH10 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

Note: Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.

Table 5-33. Transitions Due to Power Failure

State at Power Failure	AFTERG3_EN bit	Transition When Power Returns
S0, S1, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0

5.13.7 Thermal Management

The ICH10 has mechanisms to assist with managing thermal problems in the system.

5.13.7.1 THRM# Signal

The THRM# signal is used as a status input for a thermal sensor. Based on the THRM# signal going active, the ICH10 generates an SMI# or SCI (depending on SCI_EN).

If the THRM_POL bit is set low, when the THRM# signal goes low, the THRM_STS bit will be set. This is an indicator that the thermal threshold has been exceeded. If the THRM_EN bit is set, then when THRM_STS goes active, either an SMI# or SCI will be generated (depending on the SCI_EN bit being set).

The power management software (BIOS or ACPI) can then take measures to start reducing the temperature. Examples include shutting off unwanted subsystems, or halting the processor.

By setting the THRM_POL bit to high, another SMI# or SCI can optionally be generated when the THRM# signal goes back high. This allows the software (BIOS or ACPI) to turn off the cooling methods.

Note: THRM# assertion does not cause a TCO event message in S3 or S4. The level of the signal is not reported in the heartbeat message.

5.13.7.2 Software Initiated Passive Cooling

This mode is initiated by software setting the THTL_EN or FORCE_THTL bits.

Software sets the THTL_DTY or THRM_DTY bits to select throttle ratio and THTL_EN or FORCE_THTL bit to enable the throttling.

Throttling results in STPCLK# active for a minimum time of 12.5% and a maximum of 87.5%. The period is 1024 PCI clocks. Thus, the STPCLK# signal can be active for as little as 128 PCI clocks or as much as 896 PCI clocks. The actual slowdown (and cooling) of the processor depends on the instruction stream, because the processor is allowed to finish the current instruction. Furthermore, the ICH10 waits for the STOP-GRANT cycle before starting the count of the time the STPCLK# signal is active.

5.13.7.3 THRM# Override Software Bit

The FORCE_THTL bit allows the BIOS to force passive cooling, independent of the ACPI software (which uses the THTL_EN and THTL_DTY bits). If this bit is set, the ICH10 starts throttling using the ratio in the THRM_DTY field.

When this bit is cleared the ICH10 stops throttling, unless the THTL_EN bit is set (indicating that ACPI software is attempting throttling).

If both the THTL_EN and FORCE_THTL bits are set, then the ICH should use the duty cycle defined by the THRM_DTY field, not the THTL_DTY field.

5.13.7.4 Active Cooling

Active cooling involves fans. The GPIO signals from the ICH10 can be used to turn on/off a fan.

5.13.8 Event Input Signals and Their Usage

The ICH10 has various input signals that trigger specific events. This section describes those signals and how they should be used.

5.13.8.1 PWRBTN# (Power Button)

The ICH10 PWRBTN# signal operates as a “Fixed Power Button” as described in the *Advanced Configuration and Power Interface, Version 2.0b.* PWRBTN# signal has a 16 ms de-bounce on the input. The state transition descriptions are included in Table 5-34. Note that the transitions start as soon as the PWRBTN# is pressed (but after the debounce logic), and does not depend on when the Power Button is released.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled), the Power Button is not a wake event. Refer to Power Button Override Function section below for further detail.

Table 5-34. Transitions Due to Power Button

Present State	Event	Transition/Action	Comment
S0/Cx	PWRBTN# goes low	SMI# or SCI generated (depending on SCI_EN, PWRBTN_INIT_EN, PWRBTN_EN and GLB_SMI_EN)	Software typically initiates a Sleep state
S1–S5	PWRBTN# goes low	Wake Event. Transitions to S0 state	Standard wakeup
G3	PWRBTN# pressed	None	No effect since no power Not latched nor detected
S0–S4	PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor (e.g., Stop-Grant cycles) or any other subsystem

Power Button Override Function (ICH10 Consumer Only)

If PWRBTN# is observed active for at least four consecutive seconds, the state machine unconditionally transitions to the G2/S5 state, regardless of present state (S0-S4), even if PWROK is not active. In this case, the transition to the G2/S5 state does not depend on any particular response from the processor (e.g., a Stop-Grant cycle), nor any similar dependency from any other subsystem. The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable via the PWRBTN_LVL bit.

Note: The 4-second PWRBTN# assertion should only be used if a system lock-up has occurred.

The 4-second timer starts counting when the ICH10 is in a S0 state. If the PWRBTN# signal is asserted and held active when the system is in a suspend state (S1-S5), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled by D31:F0:A4h bit 3), the Power Button is not a wake event.

Power Button Override Function (ICH10 Corporate Only)

If PWRBTN# is observed active for at least four consecutive seconds when in S0/1 or at least nine consecutive seconds when in S3-S4, the state machine unconditionally transitions to the G2/S5 state, even if PWROK is not active. In this case, the transition to the G2/S5 state does not depend on any particular response from the processor (e.g., a Stop-Grant cycle), nor any similar dependency from any other subsystem. The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable via the PWRBTN_LVL bit.

Note: A 4 to 9 second PWRBTN# assertion should only be used if a system lock-up has occurred.

The power button override timer starts counting when PWRBTN# is asserted and will be set to 4 seconds when the platform is in S0/S1 and 9 seconds when the platform is in S3-S4 in order to trigger a power button override event.

Note: During the time that the SLP_S3#/SLP_S4# signal is stretched for the minimum assertion width (if enabled in D31:F0:A4h), a Power Button is not wake event. For this reason, the ICH10 Corporate will always extend the power button override timer to 9 seconds when in S3/S4 to allow for a wake event that is delayed by SLP_S3#/SLP_S4# stretching to be observed before accidentaly triggering a power button override event.

Sleep Button

The *Advanced Configuration and Power Interface, Version 2.0b* defines an optional Sleep button. It differs from the power button in that it only is a request to go from S0 to S1–S4 (not S5). Also, in an S5 state, the Power Button can wake the system, but the Sleep Button cannot.

Although the ICH10 does not include a specific signal designated as a Sleep Button, one of the GPIO signals can be used to create a “Control Method” Sleep Button. See the *Advanced Configuration and Power Interface, Version 2.0b* for implementation details.

5.13.8.2 RI# (Ring Indicator)

The Ring Indicator can cause a wake event (if enabled) from the S1–S5 states. Table 5-35 shows when the wake event is generated or ignored in different states. If in the G0/S0/Cx states, the ICH10 generates an interrupt based on RI# active, and the interrupt will be set up as a Break event.

Table 5-35. Transitions Due to RI# Signal

Present State	Event	RI_EN	Event
S0	RI# Active	X	Ignored
S1–S5	RI# Active	0	Ignored
		1	Wake Event

Note: Filtering/Debounce on RI# will not be done in ICH10. Can be in modem or external.

5.13.8.3 PME# (PCI Power Management Event)

The PME# signal comes from a PCI device to request that the system be restarted. The PME# signal can generate an SMI#, SCI, or optionally a Wake event. The event occurs when the PME# signal goes from high to low. No event is caused when it goes from low to high.

There is also an internal PME_B0 bit. This is separate from the external PME# signal and can cause the same effect.

5.13.8.4 SYS_RESET# Signal

When the SYS_RESET# pin is detected as active after the 16 ms debounce logic, the ICH10 attempts to perform a “graceful” reset, by waiting up to 25 ms for the SMBus to go idle. If the SMBus is idle when the pin is detected active, the reset occurs immediately; otherwise, the counter starts. If at any point during the count the SMBus goes idle the reset occurs. If, however, the counter expires and the SMBus is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYSRESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PLTRST# inactive. Note that if bit 3 of the CF9h I/O register is set then SYS_RESET# will result in a full power cycle reset.

5.13.8.5 THRMTRIP# Signal

If THRMTRIP# goes active, the processor is indicating an overheat condition, and the ICH10 immediately transitions to an S5 state. However, since the processor has overheated, it does not respond to the ICH10’s STPCLK# pin with a stop grant special cycle. Therefore, the ICH10 does not wait for one. Immediately upon seeing THRMTRIP# low, the ICH10 initiates a transition to the S5 state, drive SLP_S3#, SLP_S4#, SLP_S5# low, and set the CTS bit. The transition looks like a power button override.

When a THRMTRIP# event occurs, the ICH10 will power down immediately without following the normal S0 -> S5 path. The ICH10 will immediately drive SLP_S3#, SLP_S4#, and SLP_S5# low after sampling THRMTRIP# active.

If the processor is running extremely hot and is heating up, it is possible (although very unlikely) that components around it, such as the ICH10, are no longer executing cycles properly. Therefore, if THRMTRIP# goes active, and the ICH10 is relying on state machine logic to perform the power down, the state machine may not be working, and the system will not power down.

The ICH provides filtering for short low glitches on the THRMTRIP# signal in order to prevent erroneous system shut downs from noise. Glitches shorter than 25nsec are ignored.

During boot, THRMTRIP# is ignored until SLP_S3#, PWROK, VRMPWRGD/VGATE, and PLTRST# are all '1'. During entry into a powered-down state (due to S3, S4, S5 entry, power cycle reset, etc.) THRMTRIP# is ignored until either SLP_S3# = 0, or PWROK = 0, or VRMPWRGD/VGATE = 0.

Note: A thermal trip event will:

- Set the AFTERG3_EN bit
- Clear the PWRBTN_STS bit
- Clear all the GPE0_EN register bits
- Clear the SMB_WAK_STS bit only if SMB_SAK_STS was set due to SMBus slave receiving message and not set due to SMBAlert

5.13.8.6 BMBUSY#

The BMBUSY# signal is an input from a graphics component to indicate if it is busy. If prior to going to the C3 state, the BMBUSY# signal is active, then the BM_STS bit will be set. If after going to the C3 state, the BMBUSY# signal goes back active, the ICH10 will treat this as if one of the PCI REQ# signals went active. This is treated as a break event.

5.13.9 ALT Access Mode

Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the ICH10 implements an ALT access mode.

If the ALT access mode is entered and exited after reading the registers of the ICH10 timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1. BIOS enters ALT access mode for reading the ICH10 timer related registers.
2. BIOS exits ALT access mode.
3. BIOS continues through the execution of other needed steps and passes control to the operating system.

After getting control in step #3, if the operating system does not reprogram the system timer again, the timer ticks may be happening faster than expected. For example DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the time-outs in the software may be happening faster than expected.

Operating systems (e.g., Microsoft Windows* 98, Windows* 2000, and Windows NT*) reprogram the system timer and therefore do not encounter this problem.

For some other operating systems (e.g., Microsoft MS-DOS*) the BIOS should restore the timer back to 54.6 ms before passing control to the operating system. If the BIOS is entering ALT access mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT access mode.

5.13.9.1 Write Only Registers with Read Paths in ALT Access Mode

The registers described in Table 5-36 have read paths in ALT access mode. The access number field in the table indicates which register will be returned per access to that port.

Table 5-36. Write Only Registers with Read Paths in ALT Access Mode (Sheet 1 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
00h	2	1	DMA Chan 0 base address low byte	40h	7	1	Timer Counter 0 status, bits [5:0]
		2	DMA Chan 0 base address high byte			2	Timer Counter 0 base count low byte
01h	2	1	DMA Chan 0 base count low byte			3	Timer Counter 0 base count high byte
		2	DMA Chan 0 base count high byte			4	Timer Counter 1 base count low byte
02h	2	1	DMA Chan 1 base address low byte			5	Timer Counter 1 base count high byte
		2	DMA Chan 1 base address high byte			6	Timer Counter 2 base count low byte
03h	2	1	DMA Chan 1 base count low byte			7	Timer Counter 2 base count high byte
		2	DMA Chan 1 base count high byte	41h	1		Timer Counter 1 status, bits [5:0]
04h	2	1	DMA Chan 2 base address low byte	42h	1		Timer Counter 2 status, bits [5:0]
		2	DMA Chan 2 base address high byte	70h	1		Bit 7 = NMI Enable, Bits [6:0] = RTC Address
05h	2	1	DMA Chan 2 base count low byte	C4h	2	1	DMA Chan 5 base address low byte
		2	DMA Chan 2 base count high byte			2	DMA Chan 5 base address high byte
06h	2	1	DMA Chan 3 base address low byte	C6h	2	1	DMA Chan 5 base count low byte
		2	DMA Chan 3 base address high byte			2	DMA Chan 5 base count high byte
07h	2	1	DMA Chan 3 base count low byte	C8h	2	1	DMA Chan 6 base address low byte
		2	DMA Chan 3 base count high byte			2	DMA Chan 6 base address high byte

Table 5-36. Write Only Registers with Read Paths in ALT Access Mode (Sheet 2 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
08h	6	1	DMA Chan 0–3 Command[2]	CAh	2	1	DMA Chan 6 base count low byte
		2	DMA Chan 0–3 Request			2	DMA Chan 6 base count high byte
		3	DMA Chan 0 Mode: Bits(1:0) = 00	CCh	2	1	DMA Chan 7 base address low byte
		4	DMA Chan 1 Mode: Bits(1:0) = 01			2	DMA Chan 7 base address high byte
		5	DMA Chan 2 Mode: Bits(1:0) = 10	CEh	2	1	DMA Chan 7 base count low byte
		6	DMA Chan 3 Mode: Bits(1:0) = 11.			2	DMA Chan 7 base count high byte
20h	12	1	PIC ICW2 of Master controller	D0h	6	1	DMA Chan 4–7 Command[2]
		2	PIC ICW3 of Master controller			2	DMA Chan 4–7 Request
		3	PIC ICW4 of Master controller			3	DMA Chan 4 Mode: Bits(1:0) = 00
		4	PIC OCW1 of Master controller[1]			4	DMA Chan 5 Mode: Bits(1:0) = 01
		5	PIC OCW2 of Master controller			5	DMA Chan 6 Mode: Bits(1:0) = 10
		6	PIC OCW3 of Master controller			6	DMA Chan 7 Mode: Bits(1:0) = 11.
		7	PIC ICW2 of Slave controller				
		8	PIC ICW3 of Slave controller				
		9	PIC ICW4 of Slave controller				
		10	PIC OCW1 of Slave controller[1]				
		11	PIC OCW2 of Slave controller				
		12	PIC OCW3 of Slave controller				

NOTES:
1. The OCW1 register must be read before entering ALT access mode.
2. Bits 5, 3, 1, and 0 return 0.

5.13.9.2 PIC Reserved Bits

Many bits within the PIC are reserved, and must have certain values written in order for the PIC to operate properly. Therefore, there is no need to return these values in ALT access mode. When reading PIC registers from 20h and A0h, the reserved bits shall return the values listed in Table 5-37.

Table 5-37. PIC Reserved Bits Return Values

PIC Reserved Bits	Value Returned
ICW2(2:0)	000
ICW4(7:5)	000
ICW4(3:2)	00
ICW4(0)	0
OCW2(4:3)	00
OCW3(7)	0
OCW3(5)	Reflects bit 6
OCW3(4:3)	01

5.13.9.3 Read Only Registers with Write Paths in ALT Access Mode

The registers described in Table 5-38 have write paths to them in ALT access mode. Software restores these values after returning from a powered down state. These registers must be handled special by software. When in normal mode, writing to the base address/count register also writes to the current address/count register. Therefore, the base address/count must be written first, then the part is put into ALT access mode and the current address/count register is written.

Table 5-38. Register Write Accesses in ALT Access Mode

I/O Address	Register Write Value
08h	DMA Status Register for channels 0–3.
D0h	DMA Status Register for channels 4–7.

5.13.10 System Power Supplies, Planes, and Signals

5.13.10.1 Power Plane Control with SLP_S3#, SLP_S4#, SLP_S5# and SLP_M#

The SLP_S3# output signal can be used to cut power to the system core supply, since it only goes active for the Suspend-to-RAM state (typically mapped to ACPI S3). Power must be maintained to the ICH10 suspend well, and to any other circuits that need to generate Wake signals from the Suspend-to-RAM state. During S3 (Suspend-to-RAM) all signals attached to powered down plans will be tri-stated or driven low, unless they are pulled via a pull-up resistor.

Cutting power to the core may be done via the power supply, or by external FETs on the motherboard.

The SLP_S4# or SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done via the power supply, or by external FETs on the motherboard.

The SLP_S4# output signal is used to remove power to additional subsystems that are powered during SLP_S3#.

SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done via the power supply, or by external FETs on the motherboard.

SLP_M# output signal can be used to cut power to the Controller Link, Clock chip and SPI flash on a platform that supports Intel AMT.

5.13.10.2 SLP_S4# and Suspend-To-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The SLP_S4# signal should be used to remove power to system memory rather than the SLP_S5# signal. The SLP_S4# logic in the ICH10 provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note: To use the minimum DRAM power-down feature that is enabled by the SLP_S4# Assertion Stretch Enable bit (D31:F0:A4h bit 3), the DRAM power must be controlled by the SLP_S4# signal.

5.13.10.3 PWROK Signal

The PWROK input should go active based on the core supply voltages becoming valid. PWROK should go active no sooner than 99 ms after Vcc3_3 and Vcc1_5 have reached their nominal values. PWROK must not glitch, even if RSMRST# is low.

Note:

1. SYSRESET# is recommended for implementing the system reset button. This saves external logic that is needed if the PWROK input is used. Additionally, it allows for better handling of the SMBus and processor resets, and avoids improperly reporting power failures.
2. PWROK and RSMRST# are sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the ICH10.
3. In the case of true PWROK failure, PWROK will go low before VRMPWRGD.
4. When PWROK goes inactive, a host power cycle reset will occur. A host power cycle is the assertion of SLP_S3#, SLP_S4#, and SLP_S5#, and the deassertion of these signals 3-5 seconds later. The Intel Management Engine remains powered throughout this cycle.

5.13.10.4 CPUPWRGD Signal

This signal is connected to the processor's VRM via the VRMPWRGD signal and is internally AND'd with the PWROK signal that comes from the system power supply.

5.13.10.5 VRMPWRGD Signal

VRMPWRGD is an input from the regulator indicating that all of the outputs from the regulator are on and within specification. Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.

Note: When VRMPWRGD goes inactive, a host power cycle reset will occur. A host power cycle is the assertion of SLP_S3#, SLP_S4#, and SLP_S5#, and the deassertion of these signals 3-5 seconds later. The Intel Management Engine remains powered throughout this cycle.

5.13.10.6 DRAMPWROK Signal (Corporate Only)

The DRAMPWROK output is sent to the (G)MCH as an indication of when DRAM power is turned off. The (G)MCH uses this information as one of the conditions for asserting the DDR3 Reset signal.

The ICH10's open-drain buffer pulls the signal low when SLP_S4# is asserted and CLPWROK deasserted.

5.13.11 Clock Generators

The clock generator is expected to provide the frequencies shown in Table 5-39.

Table 5-39. Intel® ICH10 Clock Inputs

Clock Domain	Frequency	Source	Usage
SATA_CLK	100 MHz Differential	Main Clock Generator	Used by SATA controller. Stopped in S3 – S based on SLP_S3# assertion.
DMI_CLK	100 MHz Differential	Main Clock Generator	Used by DMI and PCI Express*. Stopped in S3 – S5 based on SLP_S3# assertion.
PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to ICH10. Stopped in S3 – S5 based on SLP_S3# assertion.
CLK48	48.000 MHz	Main Clock Generator	Used by USB controllers and Intel High Definition Audio controller. Stopped in S3 – S5 based on SLP_S3# assertion.
CLK14	14.318 MHz	Main Clock Generator	Used by ACPI timers. Stopped in S3 – S5 based on SLP_S3# assertion.
GLAN_CLK	5 to 62.5 MHz	Platform LAN Connect	LAN Connect Interface and Gigabit LAN Connect Interface. Control policy is determined by the clock source.

5.13.11.1 Clock Control Signals from Intel® ICH10 to Clock Synthesizer

The clock generator is assumed to have direct connect from the following ICH10 signals:

- STP_CPU#: Stops processor clocks in C3 and C4 states
- STP_PCI#: Stops system PCI clocks (not the ICH10 free-running 33 MHz clock) due to CLKRUN# protocol
- SLP_S3#: Expected to drive clock chip PWRDOWN (through inverter), to stop clocks in S3 to S5.

5.13.12 Legacy Power Management Theory of Operation

Instead of relying on ACPI software, legacy power management uses BIOS and various hardware mechanisms. The scheme relies on the concept of detecting when individual subsystems are idle, detecting when the whole system is idle, and detecting when accesses are attempted to idle subsystems.

However, the operating system is assumed to be at least APM enabled. Without APM calls, there is no quick way to know when the system is idle between keystrokes. The ICH10 does not support burst modes.

5.13.12.1 APM Power Management

The ICH10 has a timer that, when enabled by the 1MIN_EN bit in the SMI Control and Enable register, generates an SMI# once per minute. The SMI handler can check for system activity by reading the DEVACT_STS register. If none of the system bits are set, the SMI handler can increment a software counter. When the counter reaches a sufficient number of consecutive minutes with no activity, the SMI handler can then put the system into a lower power state.

If there is activity, various bits in the DEVACT_STS register will be set. Software clears the bits by writing a 1 to the bit position.

The DEVACT_STS register allows for monitoring various internal devices, or Super I/O devices (SP, PP, FDC) on LPC or PCI, keyboard controller accesses, or audio functions on LPC or PCI. Other PCI activity can be monitored by checking the PCI interrupts.

5.13.13 Reset Behavior

When a reset is triggered, the ICH10 will send a warning message to the (G)MCH to allow the (G)MCH to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the (G)MCH is ready, it will send an acknowledge message to the ICH10. Once the message is received the ICH10 asserts PLTRST#.

The ICH10 does not require an acknowledge message from the (G)MCH to trigger PLTRST#. A global reset will occur after 4 seconds if an acknowledge from the (G)MCH is not received.

Note: When the ICH10 causes a reset by asserting PLTRST# its output signals will go to their reset states as defined in Chapter 3.

A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling see Chapter 5-40 for details. If a host reset is triggered and the ICH10 times out before receiving an acknowledge message from the (G)MCH a Global Reset with power cycle will occur. A reset in which the host and ME partitions of the platform are reset is called a Global Reset.

Table 5-40 shows the various reset triggers.

Table 5-40. Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle	Host Reset with Power Cycle	Global Reset with Power Cycle
Write of 0Eh to CF9h Register when Global Reset bit = 0b (D31:F0:ACh:20)	No	Yes	No (Note 1)
Write of 06h to CF9h Register when Global Reset bit = 0b	Yes	No	No (Note 1)
Write of 06h or 0Eh to CF9h register when Global Reset bit = 1b	No	No	Yes
SYS_RESET# Asserted and CF9h bit 3 = 0	Yes	No	No (Note 1)
SYS_RESET# Asserted and CF9h bit 3 = 1	No	Yes	No (Note 1)
SMBus Slave Message received for Reset with Power Cycle	No	Yes	No (Note 1)
SMBus Slave Message received for Reset without Power Cycle	Yes	No	No (Note 1)
TCO Watchdog timer reaches zero two times	Yes	No	No (Note 1)
Power Failure: PWROK signal or VRMPWRGD signal goes inactive or RSMRST# asserts	No	No	Yes (Note 2)
Special shutdown cycle from CPU causes CF9h-like PLTRST# and CF9h Global Reset bit = 1	No	No	Yes
Special shutdown cycle from CPU causes CF9h-like PLTRST# and CF9h bit 3 = 1	No	Yes	No (Note 2)
Special Shutdown Cycle from CPU causes CF9h-like PLTRST# and CF9h Global Reset bit = 0	Yes	No	No (Note 1)
Intel® Management Engine Triggered Host Reset without power cycle	Yes	No	No (Note 1)
Intel Management Engine Triggered Host Reset with power cycle	No	Yes	No (Note 1)
Intel Management Engine Triggered Global Reset	No	No	Yes
Intel Management Engine Initiated Host Reset with power down	No	Yes (Note 3)	No (Note 1)
Intel Management Engine Watchdog Timer	No	Yes (Note 4)	No (Note 1)
Power Management Watchdog Timer	No	Yes (Note 4)	No (note 1)

NOTES:
1. Trigger will result in Global Reset with power cycle if the acknowledge message is not received by the ICH10.
2. ICH10 does not send warning message to (G)MCH, reset occurs without delay.
3. ICH10 waits for enabled wake event to complete reset.
4. System stays in S5 state.

5.14 System Management (D31:F0)

The ICH10 provides various functions to make a system easier to manage and to lower the Total Cost of Ownership (TCO) of the system. In addition, ICH10 provides integrated ASF Management support, requires use of SPI Flash and Intel Management Engine firmware. Features and functions can be augmented via external A/D converters and GPIO, as well as an external microcontroller.

The following features and functions are supported by the ICH10:

- Processor present detection
  - Detects if processor fails to fetch the first instruction after reset
- Various Error detection (such as ECC Errors) indicated by host controller
  - Can generate SMI#, SCI, SERR, NMI, or TCO interrupt
- Intruder Detect input
  - Can generate TCO interrupt or SMI# when the system cover is removed
  - INTRUDER# allowed to go active in any power state, including G3
- Detection of bad BIOS Flash (FWH or Flash on SPI) programming
  - Detects if data on first read is FFh (indicates that BIOS flash is not programmed)
- Ability to hide a PCI device
  - Allows software to hide a PCI device in terms of configuration space through the use of a device hide register (See Section 10.1.75)

Note: Voltage ID from the processor can be read via GPI signals. ASF functionality with the integrated ICH10 ASF controller requires a correctly configured system, including an appropriate SKU of the ICH10 (see Section 1.3), (G)MCH with Intel Management Engine, Intel Management Engine Firmware, system BIOS support, and appropriate Platform LAN Connect Device.

5.14.1 Theory of Operation

The System Management functions are designed to allow the system to diagnose failing subsystems. The intent of this logic is that some of the system management functionality can be provided without the aid of an external microcontroller.

5.14.1.1 Detecting a System Lockup

When the processor is reset, it is expected to fetch its first instruction. If the processor fails to fetch the first instruction after reset, the TCO timer times out twice and the ICH10 asserts PLTRST#.

5.14.1.2 Handling an Intruder

The ICH10 has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCO_STS register. The INTRD_SEL bits in the TCO_CNT register can enable the ICH10 to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.

If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

Note: The INTRD_DET bit resides in the ICH10's RTC well, and is set and cleared synchronously with the RTC clock. Thus, when software attempts to clear INTRD_DET (by writing a 1 to the bit location) there may be as much as two RTC clocks (about 65 µs) delay before the bit is actually cleared. Also, the INTRUDER# signal should be asserted for a minimum of 1 ms to ensure that the INTRD_DET bit will be set.

Note: If the INTRUDER# signal is still active when software attempts to clear the INTRD_DET bit, the bit remains set and the SMI is generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further SMIs, since the INTRD_SEL bits would select that no SMI# be generated.

5.14.1.3 Detecting Improper Firmware Hub Programming

The ICH10 can detect the case where the BIOS flash is not programmed. This results in the first instruction fetched to have a value of FFh. If this occurs, the ICH10 sets the BAD_BIOS bit. The BIOS flash may reside in FWH or flash on the SPI bus.

5.14.1.4 Heartbeat and Event Reporting via SMLink/SMBus

Heartbeat and event reporting via SMLink/SMBus is no longer supported. The Intel AMT logic in ICH10 can be programmed to generate an interrupt to the Intel Management Engine when an event occurs. The Intel Management Engine will poll the TCO registers to gather appropriate bits to send the event message to the Gigabit Ethernet controller, if Intel Management Engine is programmed to do so.

The Intel Management Engine is responsible for sending ASF 2.0 messages if programmed to do so.

In Advanced TCO BMC mode, the external micro-controller (BMC) accesses the TCO info through SMBus.

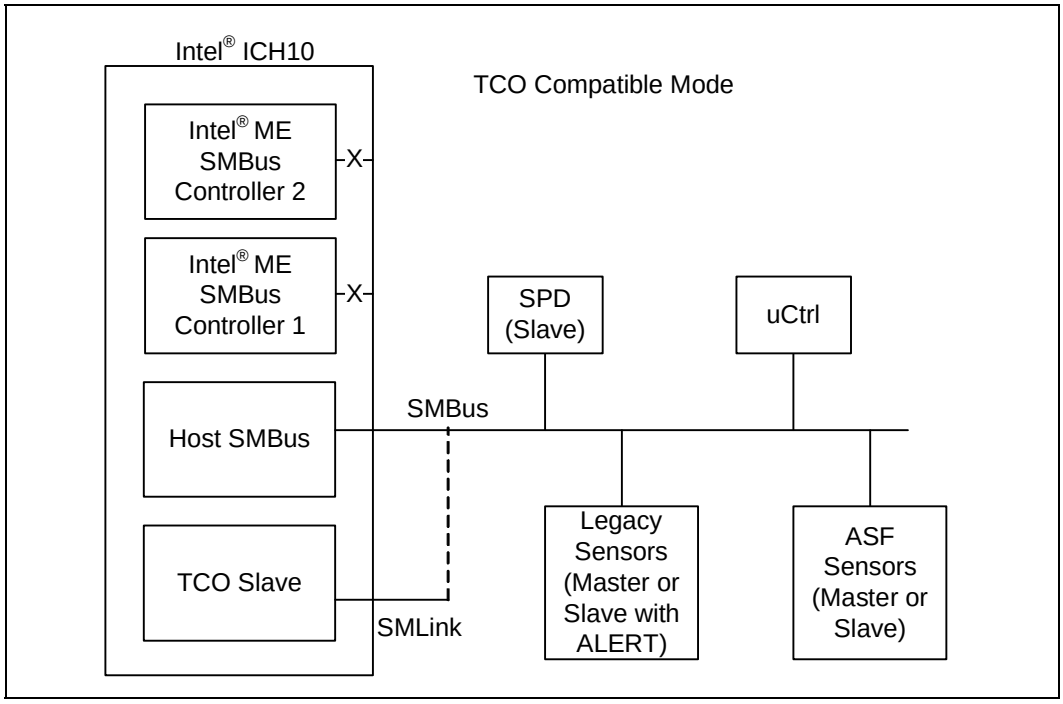
5.14.2 TCO Modes

5.14.2.1 TCO Legacy/Compatible Mode

In TCO Legacy/Compatible mode the Intel Management Engine and Intel AMT logic and SMBus controllers are disabled. To enable Legacy/Compatible TCO mode the TCOMODE bit 7 in the ICHSTRP0 register in the SPI device must be 0.

Note: SMBus and SMLink may be tied together externally, if a device has a single SMBus interface and needs access to the TCO slave and be visisble to the host SMBus controller.

Figure 5-6. TCO Legacy/Compatible Mode SMBus Configuration



In TCO Legacy/Compatible mode the Intel ICH10 can function directly with the integrated Gigabit Ethernet controller or equivalent external LAN controller to report messages to a network management console without the aid of the system processor. This is crucial in cases where the processor is malfunctioning or cannot function due to being in a low-power state. Table 5-41 includes a list of events that will report messages to the network management console.

Table 5-41. Event Transitions that Cause Messages

Event	Assertion?	Deassertion?	Comments
INTRUDER# pin	yes	no	Must be in “S1 or hung S0” state
THRM# pin	yes	yes	Must be in “S1 or hung S0” state. Note that the THRM# pin is isolated when the core power is off, thus preventing this event in S3-S5.
Watchdog Timer Expired	yes	no (NA)	“S1 or hung S0” state entered
GPIO[11]/ SMBALERT# pin	yes	yes	Must be in “S1 or hung S0” state
BATLOW#	yes	yes	Must be in “S1 or hung S0” state
CPU_PWR_FLR	yes	no	“S1 or hung S0” state entered

NOTE: The GPIO11/SMBALERT#/JTAGTDO pin will trigger an event message (when enabled by the GPIO11_ALERT_DISABLE bit) regardless of whether it is configured as a GPI or not.

5.14.2.2 Advanced TCO Mode

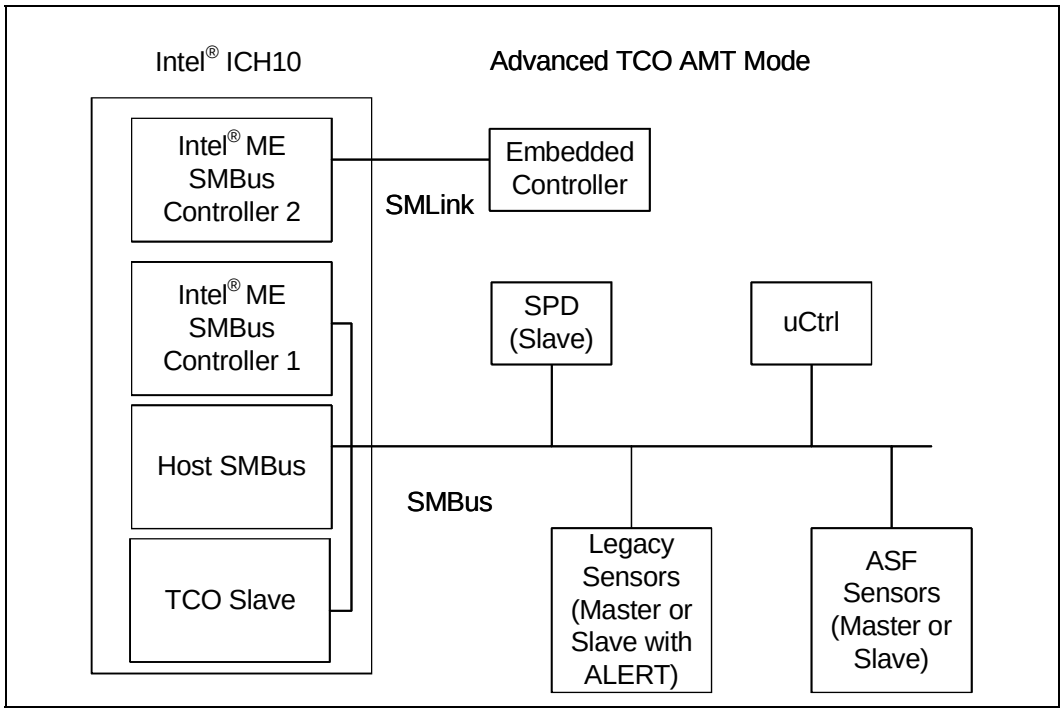
Intel ICH10 supports two modes of Advanced TCO. Intel Manageability Engine (Intel ME) mode and BMC mode. To enable Advance TCO mode (Intel ME or BMC mode) the TCOMODE bit 7 in the ICHSTRP0 register in the SPI device must be 1.

5.14.2.2.1 Advanced TCO Intel® Manageability Engine Mode

In this mode, Intel ME SMBus Controller 1, Host SMBus and SMLink are connected together internally. See Figure 5-7. This mode is enabled when the BMCMODE bit 15 in the ICHSTRP0 register in the SPI device is 0.

The Intel ME SMBus Controller 2 can be connected to either the SMBus pins or the SMLink pins by the MESM2SEL bit 23 in the ICHSTRP0 register in the SPI device. The default is to have the Intel ME SMBus Controller 2 connected to SMLink. The Intel ME SMBus Controller 2 has no connection to LINKALERT#.

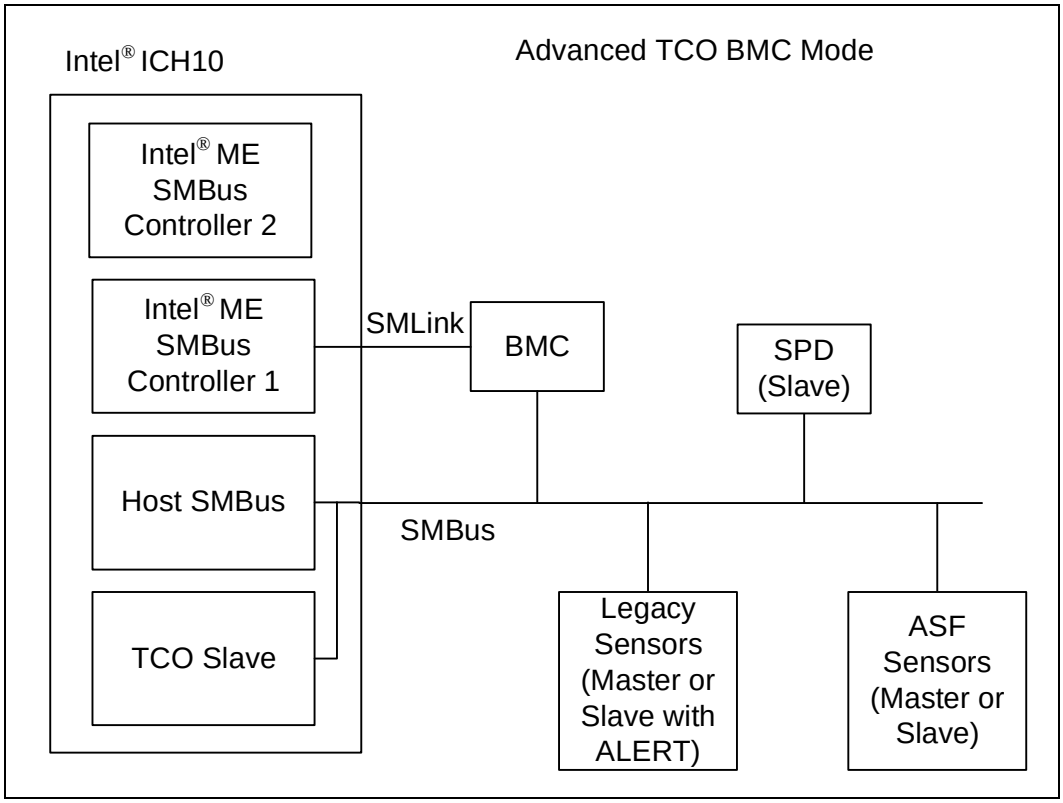
Figure 5-7. Advanced TCO Intel® ME SMBus/SMLink Configuration



5.14.2.2.2 Advanced TCO BMC Mode

In this mode, the external microcontroller (BMC) is connected to both SMLink and SMBus. The BMC communicates with Intel Management Engine through Intel ME SMBus connected to SMLink. The host and TCO slave communicated with BMC through SMBus. See Figure 5-8. This mode is enabled when the BMCMODE bit 15 in the ICHSTRP0 register in the SPI device is 1.

Figure 5-8. Advanced TCO BMC Mode SMBus/SMLink Configuration



5.15 General Purpose I/O (D31:F0)

The ICH10 contains up to 61 General Purpose Input/Output (GPIO) signals. Each GPIO can be configured as an input or output signal. The number of inputs and outputs varies depending on ICH10 configuration.

5.15.1 Power Wells

Some GPIOs exist in the suspend power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH10 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event results in the ICH10 driving a pin to a logic 1 to another device that is powered down.

5.15.2 SMI# and SCI Routing

The routing bits for GPIO[0:15] allow an input to be routed to SMI# or SCI, or neither. Note that a bit can be routed to either an SMI# or an SCI, but not both.

5.15.3 Triggering

GPIO[1:15] have “sticky” bits on the input. Refer to the GPE0_STS register. As long as the signal goes active for at least 2 clock cycles, the ICH10 keeps the sticky status bit active. The active level can be selected in the GP_LVL register. If the system is in an S0 or an S1 state, the GPI inputs are sampled at 33 MHz, so the signal only needs to be active for about 60 ns to be latched. In the S3–S5 states, the GPI inputs are sampled at 32.768 kHz, and thus must be active for at least 61 microseconds to be latched. If the input signal is still active when the latch is cleared, it will again be set. Another edge trigger is not required. This makes these signals “level” triggered inputs.

5.15.4 GPIO Registers Lockdown

The following GPIO registers are locked down when the GPIO Lockdown Enable (GLE) bit is set. The GLE bit resides in D31:F0:GPIO Control (GC) register.

- Offset 00h: GPIO_USE_SEL
- Offset 04h: GP_IO_SEL
- Offset 0Ch: GP_LVL
- Offset 30h: GPIO_USE_SEL2
- Offset 34h: GPI_IO_SEL2
- Offset 38h: GP_LVL2
- Offset 40h: GPIO_USE_SEL3 (Corporate Only)
- Offset 44h: GPI_IO_SEL3 (Corporate Only)
- Offset 48h: GP_LVL3 (Corporate Only)
- Offset 60h: GP_RST_SEL

Once these registers are locked down, they become Read-Only registers and any software writes to these registers will have no effect. To unlock the registers, the GPIO Lockdown Enable (GLE) bit is required to be cleared to ‘0’. When the GLE bit changes from a ‘1’ to a ‘0’ a System Management Interrupt (SMI#) is generated if enabled. Once the GPIO_UNLOCK_SMI bit is set, it can not be changed until a PLTRST# occurs.

This ensures that only BIOS can change the GPIO configuration. If the GLE bit is cleared by unauthorized software, BIOS will set the GLE bit again when the SMI# is triggered and these registers will continue to be locked down.

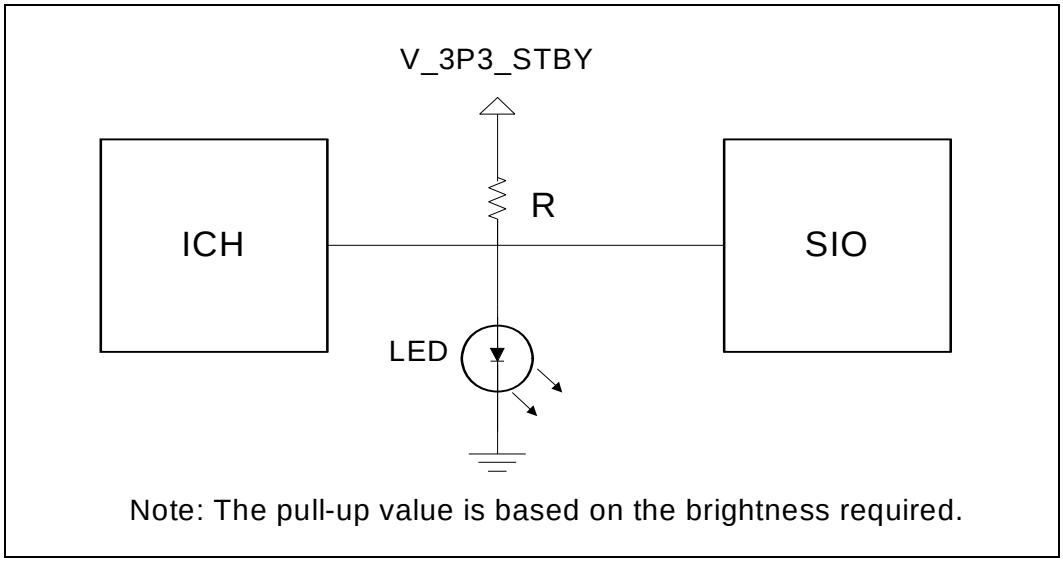
5.15.5 Serial POST Codes Over GPIO

ICH10 adds the extended capability allowing system software to serialize POST or other messages on GPIO. This capability negates the requirement for dedicated diagnostic LEDs on the platform. Additionally, based on the newer BTX form factors, the PCI bus as a target for POST codes is increasingly difficult to support as the total number of PCI devices supported are decreasing.

5.15.5.1 Theory of operation

For the ICH10 generation POST code serialization logic will be shared with GPIO. These GPIOs will likely be shared with LED control offered by the Super I/O (SIO) component. The following reference diagram shows a likely configuration.

Figure 5-9. Serial Post over GPIO Reference Circuit



The anticipated usage model is that either the ICH10 or the SIO can drive a pin low to turn off an LED. In the case of the power LED, the SIO would normally leave its corresponding pin in a high-Z state to allow the LED to turn on. In this state, the ICH10 can blink the LED by driving its corresponding pin low and subsequently tri-stating the buffer.

An external optical sensing device can detect the on/off state of the LED. By externally post-processing the information from the optical device, the serial bit stream can be recovered. The hardware will supply a 'sync' byte before the actual data transmission to allow external detection of the transmit frequency. The frequency of transmission should be limited to 1 transition every 1μs to ensure the detector can reliably sample the on/off state of the LED. To allow flexibility in pull-up resistor values for power optimization, the frequency of the transmission is programmable via the DRS field in the GP_SB_CMDSTS register (Section 13.10.6).

The serial bit stream is Manchester encoded. This choice of transmission ensures that a transition will be seen on every clock. The 1 or 0 data is based on the transmission happening during the high or low phase of the clock.

A simplified hardware/software register interface provides control and status information to track the activity of this block. Software enabling the serial blink capability should implement an algorithm referenced below to send the serialized message on the enabled GPIO.

1. Read the Go/Busy status bit in the GP_SB_CMDSTS register and verify it is cleared. This will ensure that the GPIO is idled and a previously requested message is still not in progress.
2. Write the data to serialize into the GP_SB_DATA register (Section 13.10.7).
3. Write the DLS and DRS values into the GP_SB_CMDSTS register and set the Go bit. This may be accomplished using a single write.

The reference diagram shows the LEDs being powered from the suspend supply. By providing a generic capability that can be used both in the main and the suspend power planes maximum flexibility can be achieved. A key point to make is that the ICH will not unintentionally drive the LED control pin low unless a serialization is in progress. System board connections utilizing this serialization capability are required to use the same power plane controlling the LED as the ICH10 GPIO pin. Otherwise, the ICH10 GPIO may float low during the message and prevent the LED from being controlled from the SIO. The hardware will only be serializing messages when the core power well is powered and the processor is operational.

Care should be taken to prevent the ICH10 from driving an active ‘1’ on a pin sharing the serial LED capability. Since the SIO could be driving the line to 0, having the ICH drive a 1 would create a high current path. A recommendation to avoid this condition involves choosing a GPIO defaulting to an input. The GP_SER_BLINK register (Section 13.10.7) should be set first before changing the direction of the pin to an output. This sequence ensures the open-drain capability of the buffer is properly configured before enabling the pin as an output.

5.15.5.2 Serial Message Format

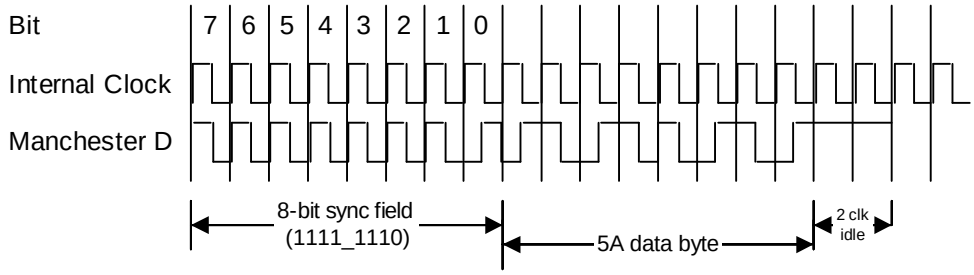
In order to serialize the data onto the GPIO, an initial state of high-Z is assumed. The SIO is required to have its LED control pin in a high-Z state as well to allow ICH10 to blink the LED (refer to the reference diagram).

The three components of the serial message include the sync, data, and idle fields. The sync field is 7 bits of ‘1’ data followed by 1 bit of ‘0’ data. Starting from the high-Z state (LED on) provides external hardware a known initial condition and a known pattern. In case one or more of the leading 1 sync bits are lost, the 1s followed by 0 provide a clear indication of ‘end of sync’. This pattern will be used to ‘lock’ external sampling logic to the encoded clock.

The data field is shifted out with the highest byte first (MSB). Within each byte, the most significant bit is shifted first (MSb).

The idle field is enforced by the hardware and is at least 2 bit times long. The hardware will not clear the Busy and Go bits until this idle time is met. Supporting the idle time in hardware prevents time-based counting in BIOS as the hardware is immediately ready for the next serial code when the Go bit is cleared. Note that the idle state is represented as a high-Z condition on the pin. If the last transmitted bit is a 1, returning to the idle state will result in a final 0-1 transition on the output Manchester data. Two full bit times of idle correspond to a count of 4 time intervals (the width of the time interval is controlled by the DRS field).

The following waveform shows a 1-byte serial write with a data byte of 5Ah. The internal clock and bit position are for reference purposes only. The Manchester D is the resultant data generated and serialized onto the GPIO. Since the buffer is operating in open-drain mode the transitions are from high-Z to 0 and back.



5.15.6 Intel Management Engine GPIOs

The following GPIOs can be used as Controller Link GPIOs: GPIO9/WOL_EN, GPIO10/ CPU_MISSING/JTAGTMS (Corporate Only), GPIO24/MEM_LED, and GPIO57/TPM_PP/ JTAGTCK (Corporate Only). Controller Link GPIOs are only available on Intel AMT or ASF enabled platforms with supporting Intel Management Engine firmware. Controller Link GPIOs are owned by the Intel Management Engine and are configured by Intel Management Engine firmware. When configured a a Controller Link GPIO the GPIO_USE_SEL bit is ignored. If the Controller Link GPIO is utilized in a platform, its associated GPIO functionality is no longer available to the host. If the Controller Link GPIO is not utilized in a platform, the signal can instead be used as its associated General Purpose I/O.

5.16 SATA Host Controller (D31:F2, F5)

The SATA function in the ICH10 has three modes of operation to support different operating system conditions. In the case of Native IDE enabled operating systems, the ICH10 utilizes two controllers to enable all six ports of the bus. The first controller (Device 31: Function 2) supports ports 0–3 and the second controller (Device 31: Function 5) supports ports 4 and 5. When using a legacy operating system, only one controller (Device 31: Function 2) is available that supports ports 0 - 3. In AHCI or RAID mode, only one controller (Device 31: Function 2) is used enabling all six ports.

The MAP register, Section 15.1.29, provides the ability to share PCI functions. When sharing is enabled, all decode of I/O is done through the SATA registers. Device 31, Function 1 (IDE controller) is hidden by software writing to the Function Disable Register (D31, F0, offset F2h, bit 1), and its configuration registers are not used.

The ICH10 SATA controllers feature six sets of interface signals (ports) that can be independently enabled or disabled (they cannot be tri-stated or driven low). Each interface is supported by an independent DMA controller.

The ICH10 SATA controllers interact with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

Note: SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

5.16.1 SATA Feature Support

Feature	ICH10 (AHCI/RAID Disabled)	ICH10 (AHCI/RAID Enabled)
Native Command Queuing (NCQ)	N/A	Supported
Auto Activate for DMA	N/A	Supported
Hot Plug Support	N/A	Supported
Asynchronous Signal Recovery	N/A	Supported
3 Gb/s Transfer Rate	Supported	Supported
ATAPI Asynchronous Notification	N/A	Supported
Host & Link Initiated Power Management	N/A	Supported
Staggered Spin-Up	Supported	Supported
Command Completion Coalescing	N/A	N/A
External SATA	N/A	Supported

Feature	Description
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Hot Plug Support	Allows for device detection without power being applied and ability to connect and disconnect devices without prior notification to the system
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug
3 Gb/s Transfer Rate	Capable of data transfers up to 3Gb/s
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host & Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host the ability to spin up hard drives sequentially to prevent power load problems on boot
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands
External SATA	Technology that allows for an outside the box connection of up to 2 meters (when using the cable defined in SATA-IO)

5.16.2 Theory of Operation

5.16.2.1 Standard ATA Emulation

The ICH10 contains a set of registers that shadow the contents of the legacy IDE registers. The behavior of the Command and Control Block registers, PIO, and DMA data transfers, resets, and interrupts are all emulated.

Note: The ICH10 will assert INTR when the master device completes the EDD command regardless of the command completion status of the slave device. If the master completes EDD first, an INTR is generated and BSY will remain '1' until the slave completes the command. If the slave completes EDD first, BSY will be '0' when the master completes the EDD command and asserts INTR. Software must wait for busy to clear (0) before completing an EDD command, as required by the ATA5 through ATA7 (T13) industry standards.

5.16.2.2 48-Bit LBA Operation

The SATA host controller supports 48-bit LBA through the host-to-device register FIS when accesses are performed via writes to the task file. The SATA host controller will ensure that the correct data is put into the correct byte of the host-to-device FIS.

There are special considerations when reading from the task file to support 48-bit LBA operation. Software may need to read all 16-bits. Since the registers are only 8-bits wide and act as a FIFO, a bit must be set in the device/control register, which is at offset 3F6h for primary and 376h for secondary (or their native counterparts).

If software clears bit 7 of the control register before performing a read, the last item written will be returned from the FIFO. If software sets bit 7 of the control register before performing a read, the first item written will be returned from the FIFO.

5.16.3 SATA Swap Bay Support

The ICH10 provides for basic SATA swap bay support using the PSC register configuration bits and power management flows. A device can be powered down by software and the port can then be disabled, allowing removal and insertion of a new device.

Note: This SATA swap bay operation requires board hardware (implementation specific), BIOS, and operating system support.

5.16.4 Hot Plug Operation

ICH10 supports Hot Plug Surprise removal and Insertion Notification in the PARTIAL, SLUMBER and Listen Mode states when used with Low Power Device Presence Detection. Software can take advantage of power savings in the low power states while enabling hot plug operation. Refer to chapter 7 of the AHCI specification for details.

5.16.4.1 Low Power Device Presence Detection

Low Power Device Presence Detection enables SATA Link Power Management to co-exist with hot plug (insertion and removal) without interlock switch or cold presence detect. The detection mechanism allows Hot Plug events to be detectable by hardware across all link power states (Active, PARTIAL, SLUMBER) as well as AHCI Listen Mode.

If the Low Power Device Presence Detection circuit is disabled the ICH10 reverts to Hot Plug Surprise Removal Notification (without an interlock switch) mode that is mutually exclusive of the PARTIAL and SLUMBER power management states.

5.16.5 Function Level Reset Support (FLR)

The SATA Host Controller supports the Function Level Reset (FLR) capability. The FLR capability can be used in conjunction with Intel Virtualization Technology. FLR allows an Operating System in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the Operating System to reset the whole device as if a PCI reset was asserted.

5.16.5.1 FLR Steps

5.16.5.1.1 FLR Initialization

1. A FLR is initiated by software writing a '1' to the Initiate FLR bit.
2. All subsequent requests targeting the Function will not be claimed and will be Master Abort Immediate on the bus. This includes any configuration, I/O or Memory cycles, however, the Function shall continue to accept completions targeting the Function.

5.16.5.1.2 FLR Operation

The Function will Reset all configuration, I/O and memory registers of the Function except those indicated otherwise and reset all internal states of the Function to the default or initial condition.

5.16.5.1.3 FLR Completion

The Initiate FLR bit is reset (cleared) when the FLR reset is completed. This bit can be used to indicate to the software that the FLR reset is completed.

Note: From the time Initiate FLR bit is written to '1' software must wait at least 100 ms before accessing the function.

5.16.6 Intel® Matrix Storage Technology Configuration

The Intel® Matrix Storage Technology offers several diverse options for RAID (redundant array of independent disks) to meet the needs of the end user. AHCI support provides higher performance and alleviates disk bottlenecks by taking advantage of the independent DMA engines that each SATA port offers in ICH10.

- RAID Level 0 performance scaling up to 4 drives, enabling higher throughput for data intensive applications such as video editing.
- Data security is offered through RAID Level 1, which performs mirroring.
- RAID Level 10 provides high levels of storage performance with data protection, combining the fault-tolerance of RAID Level 1 with the performance of RAID Level 0. By striping RAID Level 1 segments, high I/O rates can be achieved on systems that require both performance and fault-tolerance. RAID Level 10 requires 4 hard drives, and provides the capacity of two drives.
- RAID Level 5 provides highly efficient storage while maintaining fault-tolerance on 3 or more drives. By striping parity, and rotating it across all disks, fault tolerance of any single drive is achieved while only consuming 1 drive worth of capacity. That is, a 3 drive RAID 5 has the capacity of 2 drives, or a 4 drive RAID 5 has the capacity of 3 drives. RAID 5 has high read transaction rates, with a medium write rate. RAID 5 is well suited for applications that require high amounts of storage while maintaining fault tolerance.

By using the ICH10's built-in Intel Matrix Storage Technology, there is no loss of PCI resources (request/grant pair) or add-in card slot.

Intel Matrix Storage Technology functionality requires the following items:

1. ICH10 component enabled for Intel Matrix Storage Technology (see Section 1.3)
2. Intel Matrix Storage Manager RAID Option ROM must be on the platform
3. Intel Matrix Storage Manager drivers, most recent revision.
4. At least two SATA hard disk drives (minimum depends on RAID configuration).

Intel Matrix Storage Technology is not available in the following configurations:

1. The SATA controller is in compatible mode.

5.16.6.1 Intel® Matrix Storage Manager RAID Option ROM

The Intel Matrix Storage Manager RAID Option ROM is a standard PnP Option ROM that is easily integrated into any System BIOS. When in place, it provides the following three primary functions:

- Provides a text mode user interface that allows the user to manage the RAID configuration on the system in a pre-operating system environment. Its feature set is kept simple to keep size to a minimum, but allows the user to create & delete RAID volumes and select recovery options when problems occur.
- Provides boot support when using a RAID volume as a boot disk. It does this by providing Int13 services when a RAID volume needs to be accessed by DOS applications (such as NTLDR) and by exporting the RAID volumes to the System BIOS for selection in the boot order.
- At each boot up, provides the user with a status of the RAID volumes and the option to enter the user interface by pressing CTRL-I.

5.16.7 Power Management Operation

Power management of the ICH10 SATA controller and ports will cover operations of the host controller and the SATA wire.

5.16.7.1 Power State Mappings

The D0 PCI power management state for device is supported by the ICH10 SATA controller.

SATA devices may also have multiple power states. From parallel ATA, three device states are supported through ACPI. They are:

- **D0** – Device is working and instantly available.
- **D1** – device enters when it receives a STANDBY IMMEDIATE command. Exit latency from this state is in seconds
- **D3** – from the SATA device's perspective, no different than a D1 state, in that it is entered via the STANDBY IMMEDIATE command. However, an ACPI method is also called which will reset the device and then cut its power.

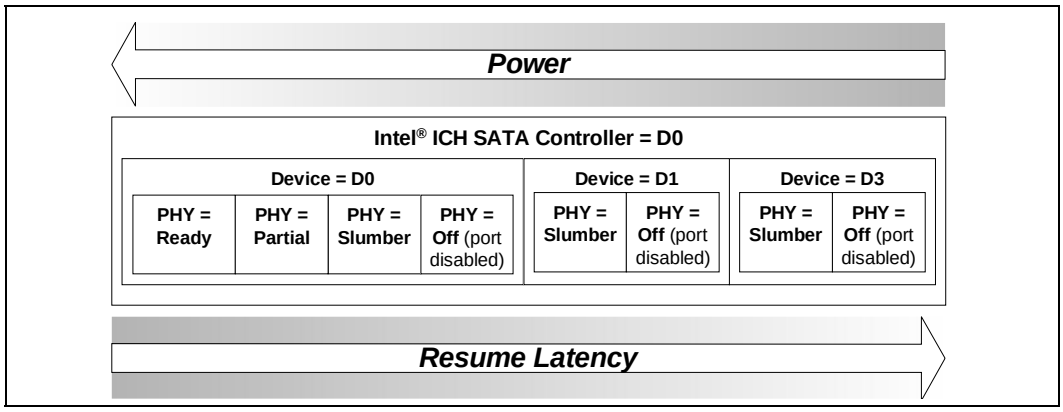
Each of these device states are subsets of the host controller's D0 state.

Finally, SATA defines three PHY layer power states, which have no equivalent mappings to parallel ATA. They are:

- **PHY READY** – PHY logic and PLL are both on and active
- **Partial** – PHY logic is powered, but in a reduced state. Exit latency is no longer than 10 ns
- **Slumber** – PHY logic is powered, but in a reduced state. Exit latency can be up to 10 ms.

Since these states have much lower exit latency than the ACPI D1 and D3 states, the SATA controller defines these states as sub-states of the device D0 state.

Figure 5-10. SATA Power States



5.16.7.2 Power State Transitions

5.16.7.2.1 Partial and Slumber State Entry/Exit

The partial and slumber states save interface power when the interface is idle. The SATA controller defines PHY layer power management (as performed via primitives) as a driver operation from the host side, and a device proprietary mechanism on the device side. The SATA controller accepts device transition types, but does not issue any transitions as a host. All received requests from a SATA device will be ACKed.

When an operation is performed to the SATA controller such that it needs to use the SATA cable, the controller must check whether the link is in the Partial or Slumber states, and if so, must issue a COM_WAKE to bring the link back online. Similarly, the SATA device must perform the same action.

5.16.7.2.2 Device D1, D3 States

These states are entered after some period of time when software has determined that no commands will be sent to this device for some time. The mechanism for putting a device in these states does not involve any work on the host controller, other then sending commands over the interface to the device. The command most likely to be used in ATA/ATAPI is the “STANDBY IMMEDIATE” command.

5.16.7.2.3 Host Controller $D3_{HOT}$ State

After the interface and device have been put into a low power state, the SATA host controller may be put into a low power state. This is performed via the PCI power management registers in configuration space. There are two very important aspects to note when using PCI power management.

1. When the power state is D3, only accesses to configuration space are allowed. Any attempt to access the memory or I/O spaces will result in master abort.
2. When the power state is D3, no interrupts may be generated, even if they are enabled. If an interrupt status bit is pending when the controller transitions to D0, an interrupt may be generated.

When the controller is put into D3, it is assumed that software has properly shut down the device and disabled the ports. Therefore, there is no need to sustain any values on the port wires. The interface will be treated as if no device is present on the cable, and power will be minimized.

When returning from a D3 state, an internal reset will not be performed.

5.16.7.2.4 Non-AHCI Mode PME# Generation

When in non-AHCI mode (legacy mode) of operation, the SATA controller does not generate PME#. This includes attach events (since the port must be disabled), or interlock switch events (via the SATAGP pins).

5.16.7.3 SMI Trapping (APM)

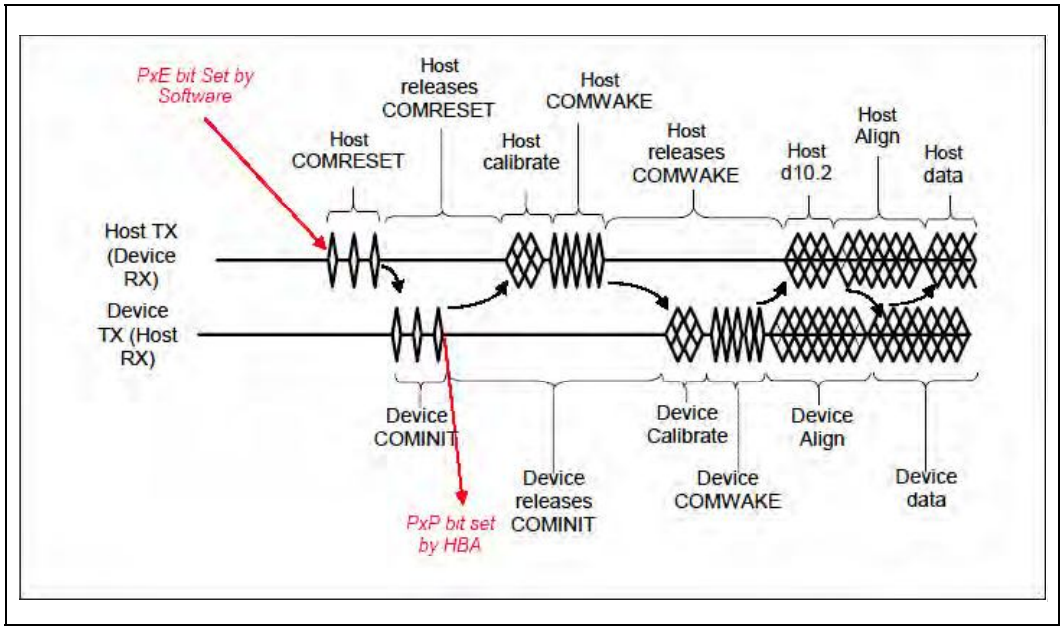
Device 31:Function2:Offset C0h (see Section 14.1.37) contain control for generating SMI# on accesses to the IDE I/O spaces. These bits map to the legacy ranges (1F0–1F7h, 3F6h, 170–177h, and 376h) and native IDE ranges defined by PCMDBA, PCTLBA, SCMDBA an SCTLBA. If the SATA controller is in legacy mode and is using these addresses, accesses to one of these ranges with the appropriate bit set causes the cycle to not be forwarded to the SATA controller, and for an SMI# to be generated. If an access to the Bus-Master IDE registers occurs while trapping is enabled for the device being accessed, then the register is updated, an SMI# is generated, and the device activity status bits (Section 14.1.38) are updated indicating that a trap occurred.

5.16.8 SATA Device Presence

In legacy mode, the SATA controller does not generate interrupts based on hot plug/ unplug events. However, the SATA PHY does know when a device is connected (if not in a partial or slumber state), and it s beneficial to communicate this information to host software as this will greatly reduce boot times and resume times.

The flow used to indicate SATA device presence is shown in Figure 5-11. The 'PxE' bit refers to PCS.P[3:0]E bits, depending on the port being checked and the 'PxP' bits refer to the PCS.P[3:0]P bits, depending on the port being checked. If the PCS/PxP bit is set a device is present, if the bit is cleared a device is not present. If a port is disabled, software can check to see if a new device is connected by periodically reenabling the port and observing if a device is present, if a device is not present it can disable the port and check again later. If a port remains enabled, software can periodically poll PCS.PxP to see if a new device is connected.

Figure 5-11. Flow for Port Enable / Device Present Bits



5.16.9 SATA LED

The SATALED# output is driven whenever the BSY bit is set in any SATA port. The SATALED# is an active-low open-drain output. When SATALED# is low, the LED should be active. When SATALED# is high, the LED should be inactive.

5.16.10 AHCI Operation

The ICH10 provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (e.g., an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The ICH10 supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface Specification*, Revision 1.2 and many optional features, such as hardware assisted native command queuing, aggressive power management, LED indicator support, and Hot-Plug through the use of interlock switch support (additional platform hardware and software may be required depending upon the implementation).

Note: For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port. See Section 7.3.1 of the *AHCI Specification* for more information.

5.16.11 Serial ATA Reference Clock Low Power Request (SATACLKREQ#)

The 100 MHz Serial ATA Reference Clock (SATACLKP, SATACLKN) is implemented on the system as a ground-terminated low-voltage differential signal pair driven by the system Clock Chip. When all the SATA links are in Slumber or disabled, the SATA Reference Clock is not needed and may be stopped and tri-stated at the clock chip allowing system-level power reductions.

The ICH10 uses the SATACLKREQ# output signal to communicate with the system Clock Chip to request either SATA clock running or to tell the system clock chip that it can stop the SATA Reference Clock. ICH10 drives this signal low to request clock running, and tristates the signal to indicate that the SATA Reference Clock may be stopped (the ICH10 never drives the pin high). When the SATACLKREQ# is tristated by the ICH10, the clock chip may stop the SATA Reference Clock within 100 ns, anytime after 100 ns, or not at all. If the SATA Reference Clock is not already running, it will start within 100 ns after a SATACLKREQ# is driven low by the ICH10.

To enable SATA Reference Clock Low Power Request:

1. Configure GPIO35 to native function
2. Set SATA Clock Request Enable (SCRE) bit to ‘1’ (Dev 31:F2:Offset 94h:bit 28).

Note: The reset default for SATACLKREQ# is low to insure that the SATA Reference Clock is running after system reset.

5.16.12 SGPIO Signals

The SGPIO signals, in accordance to the SFF-8485 specification, support per-port LED signaling. These signals are not related to SATALED#, which allows for simplified indication of SATA command activity. The SGPIO group interfaces with an external controller chip that fetches and serializes the data for driving across the SGPIO bus. The output signals then control the LEDs. This feature is only valid in AHCI/RAID mode.

5.16.12.1 Mechanism

The enclosure management for SATA Controller 1 (Device 31: Function 2) involves sending messages that control LEDs in the enclosure. The messages for this function are stored after the normal registers in the AHCI BAR, at Offset 400h bytes for ICH10 from the beginning of the AHCI BAR as specified by the EM_LOC global register (Section 14.4.1.8).

Software creates messages for transmission in the enclosure management message buffer. The data in the message buffer should not be changed if CTL.TM bit is set by software to transmit an update message. Software should only update the message buffer when CTL.TM bit is cleared by hardware otherwise the message transmitted will be indeterminate. Software then writes a register to cause hardware to transmit the message or take appropriate action based on the message content. The software should only create message types supported by the controller, which is LED messages for ICH10. If the software creates other non LED message types (e.g. SAF-TE, SES-2), the SGPIO interface may hang and the result is indeterminate.

During reset all SGPIO pins will be in tri-state state. The interface will continue to be in tri-state state after reset until the first transmission occurs when software programs the message buffer and sets the transmit bit CTL.TM. The SATA Host controller will initiate the transmission by driving SCLOCK and at the same time drive the SLOAD to '0' prior to the actual bit stream transmission. The Host will drive SLOAD low for at least 5 SCLOCK then only start the bit stream by driving the SLOAD to high. SLOAD will be driven high for 1 SCLOCK follow by vendor specific pattern that is default to "0000" if software has yet to program the value. A total of 18-bit stream from 6 ports (Port0, Port1, Port2, Port3, Port4 and Port5) of 3-bit per port LED message will be transmitted on SDATAOUT0 pin after the SLOAD is driven high for 1 SCLOCK. Only 2 ports (port4 and port5) of 6 bit total LED message follow by 12 bits of tri-state value will be transmitted out on SDATAOUT1 pin.

All the default LED message values will be high prior to software setting them, except the Activity LED message that is configured to be hardware driven that will be generated based on the activity from the respective port. All the LED message values will be driven to '1' for the port that is unimplemented as indicated in the Port Implemented register regardless of the software programmed value through the message buffer.

There are 2 different ways of resetting ICH SGPIO interface, asynchronous reset and synchronous reset. Asynchronous reset is caused by platform reset to cause the SGPIO interface to be tri-state asynchronously. Synchronous reset is caused by setting the CTL.RESET bit, clearing the GHC.AE bit or HBA reset, where Host Controller will complete the existing full bit stream transmission then only tri-state all the SGPIO pins. After the reset, both synchronous and asynchronous, the SGPIO pins will stay tri-stated.

Note: ICH Host Controller does not ensure to cause the target SGPIO device or controller to be reset. Software is responsible to keep ICH SGPIO interface in tri-state stated for 2 second in order to cause a reset on the target of the SGPIO interface.

5.16.12.2 Message Format

Messages shall be constructed with a one Dword header that describes the message to be sent followed by the actual message contents. The first Dword shall be constructed as follows:

Bit	Description
31:28	Reserved
27:24	**Message Type (MTYPE):** Specifies the type of the message. The message types are: 0h = LED 1h = SAF-TE 2h = SES-2 3h = SGPIO (register based interface) All other values reserved
23:16	**Data Size (DSIZE):** Specifies the data size in bytes. If the message (enclosure services command) has a data buffer that is associated with it that is transferred, the size of that data buffer is specified in this field. If there is no separate data buffer, this field shall have a value of '0'. The data directly follows the message in the message buffer. For ICH10, this value should always be '0'.
15:8	**Message Size (MSIZE):** Specifies the size of the message in bytes. The message size does not include the one Dword header. A value of '0' is invalid. For ICH10, the message size is always 4 bytes.
7:0	Reserved

The SAF-TE, SES-2, and SGPIO message formats are defined in the corresponding specifications, respectively. The LED message type is defined in Section 5.16.12.3. It is the responsibility of software to ensure the content of the message format is correct. If the message type is not programmed as 'LED' for this controller, the controller shall not take any action to update its LEDs. Note that for LED message type, the message size is always consisted of 4 bytes.

5.16.12.3 LED Message Type

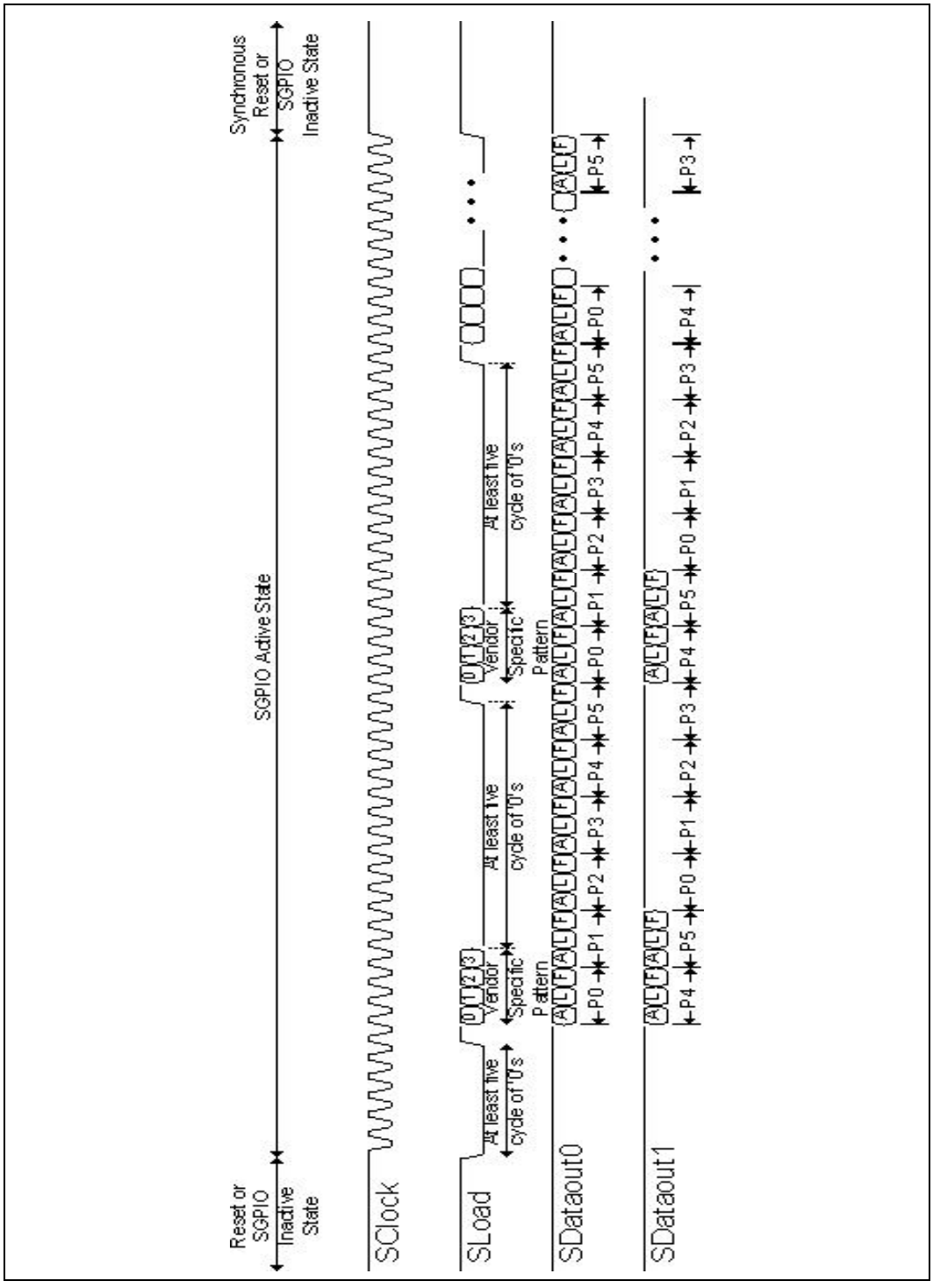
The LED message type specifies the status of up to three LEDs. Typically, the usage for these LEDs is activity, fault, and locate. Not all implementations necessarily contain all LEDs (for example, some implementations may not have a locate LED). The message identifies the HBA port number that the slot status applies to. The format of the LED message type is defined in Table 5-42. The LEDs shall retain their values until there is a following update for that particular slot.

Table 5-42. Multi-activity LED message type

Byte	Description
3-2	**Value (VAL):** This field describes the state of each LED for a particular location. There are three LEDs that may be supported by the HBA. Each LED has 3 bits of control. LED values are: 000b - LED shall be off 001b - LED shall be solid on as perceived by human eye All other values reserved The LED bit locations are: Bits 2:0 - Activity LED (may be driven by hardware) Bits 5:3 - Vendor Specific LED (e.g. locate) Bits 8:6 - Vendor Specific LED (e.g. fault) Bits 15:9 - Reserved Vendor specific message is: Bit 3:0 - Vendor Specific Pattern Bit 15:4 - Reserved Note: If Activity LED Hardware Driven (ATTR.ALHD) bit is set, host will output the hardware LED value sampled internally and will ignore software written activity value on bit [2:0]. Since ICH10 Enclosure Management does not support port multiplier based LED message, the LED message will be generated independently based on respective port's operation activity. Vendor specific LED values Locate (Bits 5:3) and Fault (Bits 8:6) always are driven by software.
1	**Port Multiplier Information:** Specifies slot specific information related to Port Multiplier. Bits 3:0 specify the Port Multiplier port number for the slot that requires the status update. If a Port Multiplier is not attached to the device in the affected slot, the Port Multiplier port number shall be '0'. Bits 7:4 are reserved. ICH10 does not support LED messages for devices behind a Port Multiplier. This byte should be 0.
0	**HBA Information:** Specifies slot specific information related to the HBA. Bits 4:0 - HBA port number for the slot that requires the status update. Bit 5 - If set to '1', Value is a vendor specific message that applies to the entire enclosure. If cleared to '0', Value applies to the port specified in bits 4:0. Bits 7:6 - Reserved

5.16.12.4 SGPIO Waveform

Figure 5-12. Serial Data transmitted over the SGPIO Interface



5.16.13 External SATA

ICH10 supports external SATA. External SATA utilizes the SATA interface outside of the system box. The usage model for this feature must comply with the Serial ATA II Cables and Connectors Volume 2 Gold specification at www.sata-io.org. Intel validates two configurations:

1. The cable-up solution involves an internal SATA cable that connects to the SATA motherboard connector and spans to a back panel PCI bracket with an e-SATA connector. A separate e-SATA cable is required to connect an e-SATA device.
2. The back-panel solution involves running a trace to the I/O back panel and connecting a device via an external SATA connector on the board.

5.17 High Precision Event Timers

This function provides a set of timers that can be used by the operating system. The timers are defined such that in the future, the operating system may be able to assign specific timers to used directly by specific applications. Each timer can be configured to cause a separate interrupt.

ICH10 provides eight (Corporate Family) or four (Consumer Family) timers. The timers are implemented as a single counter each with its own comparator and value register. This counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, it is not implemented as a standard PCI function. The BIOS reports to the operating system the location of the register space. The hardware can support an assignable decode space; however, the BIOS sets this space prior to handing it over to the operating system
(See Section 9.4). It is not expected that the operating system will move the location of these timers once it is set by the BIOS.

5.17.1 Timer Accuracy

1. The timers are accurate over any 1 ms period to within 0.05% of the time specified in the timer resolution fields.
2. Within any 100 microsecond period, the timer reports a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this represents an error of less than 0.2%.
3. The timer is monotonic. It does not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value).

The main counter is clocked by the 14.31818 MHz clock, synchronized into the 66.666 MHz domain. This results in a non-uniform duty cycle on the synchronized clock, but does have the correct average period. The accuracy of the main counter is as accurate as the 14.31818 MHz clock.

5.17.2 Interrupt Mapping

Mapping Option #1 (Legacy Replacement Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is set. This forces the mapping found in Table 5-43.

Table 5-43. Legacy Replacement Routing

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	In this case, the 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	In this case, the RTC will not cause any interrupts.
2 & 3	Per IRQ Routing Field.	Per IRQ Routing Field	
4, 5, 6, 7 (Corporate Only)	not available	not available	

NOTE: (Corporate Only) The Legacy Option does not preclude delivery of IRQ0/IRQ8 via direct FSB interrupt messages.

Mapping Option #2 (Standard Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is 0. Each timer has its own routing control. The interrupts can be routed to various interrupts in the 8259 or I/O APIC. A capabilities field indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be share with any PCI interrupts.

For the Intel ICH10, the only supported interrupt values are as follows:

Timer 0 and 1: IRQ20, 21, 22 & 23 (I/O APIC only).

Timer 2: IRQ11 (8259 or I/O APIC) and IRQ20, 21, 22, and 23 (I/O APIC only).

Timer 3: IRQ12 (8259 or I/O APIC) and IRQ 20, 21, 22, and 23 (I/O APIC only).

Interrupts from Timer 4, 5, 6, 7 (Corporate Only) can only be delivered via direct FSB interrupt messages.

5.17.3 Periodic vs. Non-Periodic Modes

Non-Periodic Mode

Timer 0 is configurable to 32 (default) or 64-bit mode, whereas Timers 1, 2 and 3 only support 32-bit mode (See Section 21.1.5).

All of the timers support non-periodic mode.

Consult Section 2.3.9.2.1 of the *IA-PC HPET Specification* for a description of this mode.

Periodic Mode

Timer 0 is the only timer that supports periodic mode. Consult Section 2.3.9.2.2 of the *IA-PC HPET Specification* for a description of this mode.

The following usage model is expected:

1. Software clears the ENABLE_CNF bit to prevent any interrupts
2. Software Clears the main counter by writing a value of 00h to it.
3. Software sets the TIMER0_VAL_SET_CNF bit.
4. Software writes the new value in the TIMER0_COMPARATOR_VAL register
5. Software sets the ENABLE_CNF bit to enable interrupts.

The Timer 0 Comparator Value register cannot be programmed reliably by a single 64-bit write in a 32-bit environment except if only the periodic rate is being changed during run-time. If the actual Timer 0 Comparator Value needs to be reinitialized, then the following software solution will always work regardless of the environment:

1. Set TIMER0_VAL_SET_CNF bit
2. Set the lower 32 bits of the Timer0 Comparator Value register
3. Set TIMER0_VAL_SET_CNF bit
4. Set the upper 32 bits of the Timer0 Comparator Value register

5.17.4 Enabling the Timers

The BIOS or operating system PnP code should route the interrupts. This includes the Legacy Rout bit, Interrupt Rout bit (for each timer), interrupt type (to select the edge or level type for each timer)

The Device Driver code should do the following for an available timer:

1. Set the Overall Enable bit (Offset 10h, bit 0).
2. Set the timer type field (selects one-shot or periodic).
3. Set the interrupt enable
4. Set the comparator value

5.17.5 Interrupt Levels

Interrupts directed to the internal 8259s are active high. See Section 5.9 for information regarding the polarity programming of the I/O APIC for detecting internal interrupts.

If the interrupts are mapped to the 8259 or I/O APIC and set for level-triggered mode, they can be shared with PCI interrupts. They may be shared although it's unlikely for the operating system to attempt to do this.

If more than one timer is configured to share the same IRQ (using the TIMERn_INT_ROUT_CNF fields), then the software must configure the timers to level-triggered mode. Edge-triggered interrupts cannot be shared.

5.17.6 Handling Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. No read is required to process the interrupt.

If a timer has been configured to level-triggered mode, then its interrupt must be cleared by the software. This is done by reading the interrupt status register and writing a 1 back to the bit position for the interrupt to be cleared.

Independent of the mode, software can read the value in the main counter to see how time has passed between when the interrupt was generated and when it was first serviced.

If Timer 0 is set up to generate a periodic interrupt, the software can check to see how much time remains until the next interrupt by checking the timer value register.

5.17.7 Issues Related to 64-Bit Timers with 32-Bit Processors

A 32-bit timer can be read directly using processors that are capable of 32-bit or 64-bit instructions. However, a 32-bit processor may not be able to directly read 64-bit timer. A race condition comes up if a 32-bit processor reads the 64-bit register using two separate 32-bit reads. The danger is that just after reading one half, the other half rolls over and changes the first half.

If a 32-bit processor needs to access a 64-bit timer, it must first halt the timer before reading both the upper and lower 32-bits of the timer. If a 32-bit processor does not want to halt the timer, it can use the 64-bit timer as a 32-bit timer by setting the TIMERn_32MODE_CNF bit. This causes the timer to behave as a 32-bit timer. The upper 32-bits are always 0.

Alternatively, software may do a multiple read of the counter while it is running. Software can read the high 32 bits, then the low 32 bits, the high 32 bits again. If the high 32 bits have not changed between the two reads, then a rollover has not happened and the low 32 bits are valid. If the high 32 bits have changed between reads, then the multiple reads are repeated until a valid read is performed.

Note: On a 64-bit platform, if software attempts a 64 bit read of the 64-bit counter, software must be aware that some platforms may split the 64 bit read into two 32 bit reads. The read maybe inaccurate if the low 32 bits roll over between the high and low reads.

5.18 USB UHCI Host Controllers (D29:F0, F1, F2, F3 and D26:F0, F1 and F2)

The ICH10 contains six USB full/low-speed host controllers that support the standard Universal Host Controller Interface (UHCI), Revision 1.1. Each UHCI Host Controller (UHC) includes a root hub with two separate USB ports each, for a total of twelve USB ports.

- Overcurrent detection on all twelve USB ports is supported. The overcurrent inputs are *not* 5 V tolerant, and can be used as GPIs if not needed.
- The ICH10's UHCI host controllers are arbitrated differently than standard PCI devices to improve arbitration latency.
- The UHCI controllers use the Analog Front End (AFE) embedded cell that allows support for USB full-speed signaling rates, instead of USB I/O buffers.

Note: D26:F2 can be configured as D29:F3 during BIOS Post.

5.18.1 Data Structures in Main Memory

Section 3.1 - 3.3 of the *Universal Host Controller Interface Specification, Revision 1.1* details the data structures used to communicate control, status, and data between software and the ICH10.

5.18.2 Data Transfers to/from Main Memory

Section 3.4 of the *Universal Host Controller Interface Specification, Revision 1.1* describes the details on how HCD and the ICH10 communicate via the Schedule data structures.

5.18.3 Data Encoding and Bit Stuffing

The ICH10 USB employs NRZI data encoding (Non-Return to Zero Inverted) when transmitting packets. Full details on this implementation are given in the *Universal Serial Bus Specification, Revision 2.0*.

5.18.4 Bus Protocol

5.18.4.1 Bit Ordering

Bits are sent out onto the bus least significant bit (LSb) first, followed by next LSb, through to the most significant bit (MSb) last.

5.18.4.2 SYNC Field

All packets begin with a synchronization (SYNC) field, which is a coded sequence that generates a maximum edge transition density. The SYNC field appears on the bus as IDLE followed by the binary string “KJKJKJKK,” in its NRZI encoding. It is used by the input circuitry to align incoming data with the local clock and is defined to be 8 bits in length. SYNC serves only as a synchronization mechanism. The last two bits in the SYNC field are a marker that is used to identify the first bit of the PID. All subsequent bits in the packet must be indexed from this point.

5.18.4.3 Packet Field Formats

All packets have distinct start and end of packet delimiters. Full details are given in the *Universal Serial Bus Specification, Revision 2.0,* in Section 8.3.1.

5.18.4.4 Address Fields

Function endpoints are addressed using the function address field and the endpoint field. Full details on this are given in the *Universal Serial Bus Specification, Revision 2.0*, in Section 8.3.2.

5.18.4.5 Frame Number Field

The frame number field is an 11-bit field that is incremented by the host on a per frame basis. The frame number field rolls over upon reaching its maximum value of 7FFh, and is sent only for SOF tokens at the start of each frame.

5.18.4.6 Data Field

The data field may range from 0 to 1023 bytes and must be an integral numbers of bytes. Data bits within each byte are shifted out LSB first.

5.18.4.7 Cyclic Redundancy Check (CRC)

CRC is used to protect the all non-PID fields in token and data packets. In this context, these fields are considered to be protected fields. Full details on this are given in the *Universal Serial Bus Specification, Revision 2.0*, in Section 8.3.5.

5.18.5 Packet Formats

The USB protocol calls out several packet types: token, data, and handshake packets. Full details on this are given in the *Universal Serial Bus Specification, Revision 2.0*, in Section 8.4.

5.18.6 USB Interrupts

There are two general groups of USB interrupt sources, those resulting from execution of transactions in the schedule, and those resulting from an ICH10 operation error. All transaction-based sources can be masked by software through the ICH10's Interrupt Enable register. Additionally, individual transfer descriptors can be marked to generate an interrupt on completion.

When the ICH10 drives an interrupt for USB, it internally drives the PIRQA# pin for USB function #0 and USB function #3, PIRQD# pin for USB function #1, and the PIRQC# pin for USB function #2, until all sources of the interrupt are cleared. In order to accommodate some operating systems, the Interrupt Pin register must contain a different value for each function of this new multi-function device.

5.18.6.1 Transaction-Based Interrupts

These interrupts are not signaled until after the status for the last complete transaction in the frame has been written back to host memory. This ensures that software can safely process through (Frame List Current Index -1) when it is servicing an interrupt.

CRC Error / Time-Out

A CRC/Time-Out error occurs when a packet transmitted from the ICH10 to a USB device or a packet transmitted from a USB device to the ICH10 generates a CRC error. The ICH10 is informed of this event by a time-out from the USB device or by the ICH10's CRC checker generating an error on reception of the packet. Additionally, a USB bus time-out occurs when USB devices do not respond to a transaction phase within 19-bit times of an EOP. Either of these conditions causes the C_ERR field of the TD to decrement.

When the C_ERR field decrements to 0, the following occurs:

- The Active bit in the TD is cleared
- The Stalled bit in the TD is set
- The CRC/Time-out bit in the TD is set.
- At the end of the frame, the USB Error Interrupt bit is set in the HC status register.

If the CRC/Time out interrupt is enabled in the Interrupt Enable register, a hardware interrupt will be signaled to the system.

Interrupt on Completion

Transfer Descriptors contain a bit that can be set to cause an interrupt on their completion. The completion of the transaction associated with that block causes the USB Interrupt bit in the HC Status Register to be set at the end of the frame in which the transfer completed. When a TD is encountered with the IOC bit set to 1, the IOC bit in the HC Status register is set to 1 at the end of the frame if the active bit in the TD is set to 0 (even if it was set to 0 when initially read).

If the IOC Enable bit of Interrupt Enable register (bit 2 of I/O offset 04h) is set, a hardware interrupt is signaled to the system. The USB Interrupt bit in the HC status register is set either when the TD completes successfully or because of errors. If the completion is because of errors, the USB Error bit in the HC status register is also set.

Short Packet Detect

A transfer set is a collection of data which requires more than one USB transaction to completely move the data across the USB. An example might be a large print file which requires numerous TDs in multiple frames to completely transfer the data. Reception of a data packet that is less than the endpoint's Max Packet size during Control, Bulk or Interrupt transfers signals the completion of the transfer set, even if there are active TDs remaining for this transfer set. Setting the SPD bit in a TD indicates to the HC to set the USB Interrupt bit in the HC status register at the end of the frame in which this event occurs. This feature streamlines the processing of input on these transfer types. If the Short Packet Interrupt Enable bit in the Interrupt Enable register is set, a hardware interrupt is signaled to the system at the end of the frame where the event occurred.

Serial Bus Babble

When a device transmits on the USB for a time greater than its assigned Max Length, it is said to be babbling. Since isochrony can be destroyed by a babbling device, this error results in the Active bit in the TD being cleared to 0 and the Stalled and Babble bits being set to 1. The C_ERR field is not decremented for a babble. The USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame. A hardware interrupt is signaled to the system.

If an EOF babble was caused by the ICH10 (due to incorrect schedule for instance), the ICH10 forces a bit stuff error followed by an EOP and the start of the next frame.

Stalled

This event indicates that a device/endpoint returned a STALL handshake during a transaction or that the transaction ended in an error condition. The TDs Stalled bit is set and the Active bit is cleared. Reception of a STALL does not decrement the error counter. A hardware interrupt is signaled to the system.

Data Buffer Error

This event indicates that an overrun of incoming data or a under-run of outgoing data has occurred for this transaction. This would generally be caused by the ICH10 not being able to access required data buffers in memory within necessary latency requirements. Either of these conditions causes the C_ERR field of the TD to be decremented.

When C_ERR decrements to 0, the Active bit in the TD is cleared, the Stalled bit is set, the USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

Bit Stuff Error

A bit stuff error results from the detection of a sequence of more that six 1s in a row within the incoming data stream. This causes the C_ERR field of the TD to be decremented. When the C_ERR field decrements to 0, the Active bit in the TD is cleared to 0, the Stalled bit is set to 1, the USB Error Interrupt bit in the HC Status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

5.18.6.2 Non-Transaction Based Interrupts

If an ICH10 process error or system error occurs, the ICH10 halts and immediately issues a hardware interrupt to the system.

Resume Received

This event indicates that the ICH10 received a RESUME signal from a device on the USB bus during a global suspend. If this interrupt is enabled in the Interrupt Enable register, a hardware interrupt is signaled to the system allowing the USB to be brought out of the suspend state and returned to normal operation.

ICH10 Process Error

The HC monitors certain critical fields during operation to ensure that it does not process corrupted data structures. These include checking for a valid PID and verifying that the MaxLength field is less than 1280. If it detects a condition that would indicate that it is processing corrupted data structures, it immediately halts processing, sets the HC Process Error bit in the HC Status register and signals a hardware interrupt to the system.

This interrupt cannot be disabled through the Interrupt Enable register.

Host System Error

The ICH10 sets this bit to 1 when a Parity error, Master Abort, or Target Abort occurs. When this error occurs, the ICH10 clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. This interrupt cannot be disabled through the Interrupt Enable register.

5.18.7 USB Power Management

The Host controller can be put into a suspended state and its power can be removed. This requires that certain bits of information are retained in the suspend power plane of the ICH10 so that a device on a port may wake the system. Such a device may be a fax-modem, which will wake up the machine to receive a fax or take a voice message. The settings of the following bits in I/O space will be maintained when the ICH10 enters the S3, S4, or S5 states.

Table 5-44. Bits Maintained in Low Power States

Register	Offset	Bit	Description
Command	00h	3	Enter Global Suspend Mode (EGSM)
Status	02h	2	Resume Detect
Port Status and Control	10h & 12h	2	Port Enabled/Disabled
		6	Resume Detect
		8	Low-speed Device Attached
		12	Suspend

When the ICH10 detects a resume event on any of its ports, it sets the corresponding USB_STS bit in ACPI space. If USB is enabled as a wake/break event, the system wakes up and an SCI generated.

5.18.8 USB Legacy Keyboard Operation

When a USB keyboard is plugged into the system, and a standard keyboard is not, the system may not boot, and MS-DOS legacy software will not run, because the keyboard will not be identified. The ICH10 implements a series of trapping operations which will snoop accesses that go to the keyboard controller, and put the expected data from the USB keyboard into the keyboard controller.

Note: The scheme described below assumes that the keyboard controller (8042 or equivalent) is on the LPC bus.

This legacy operation is performed through SMM space. Figure 5-13 shows the Enable and Status path. The latched SMI source (60R, 60W, 64R, 64W) is available in the Status Register. Because the enable is after the latch, it is possible to check for other events that didn't necessarily cause an SMI. It is the software's responsibility to logically AND the value with the appropriate enable bits.

Note also that the SMI is generated before the PCI cycle completes (e.g., before TRDY# goes active) to ensure that the processor doesn't complete the cycle before the SMI is observed.

The logic also needs to block the accesses to the 8042. If there is an external 8042, then this is simply accomplished by not activating the 8042 CS. This is done by logically ANDing the four enables (60R, 60W, 64R, 64W) with the 4 types of accesses to determine if 8042CS should go active. An additional term is required for the “pass-through” case.

The state table for Figure 5-13 is shown in Table 5-45.

Figure 5-13. USB Legacy Keyboard Flow Diagram

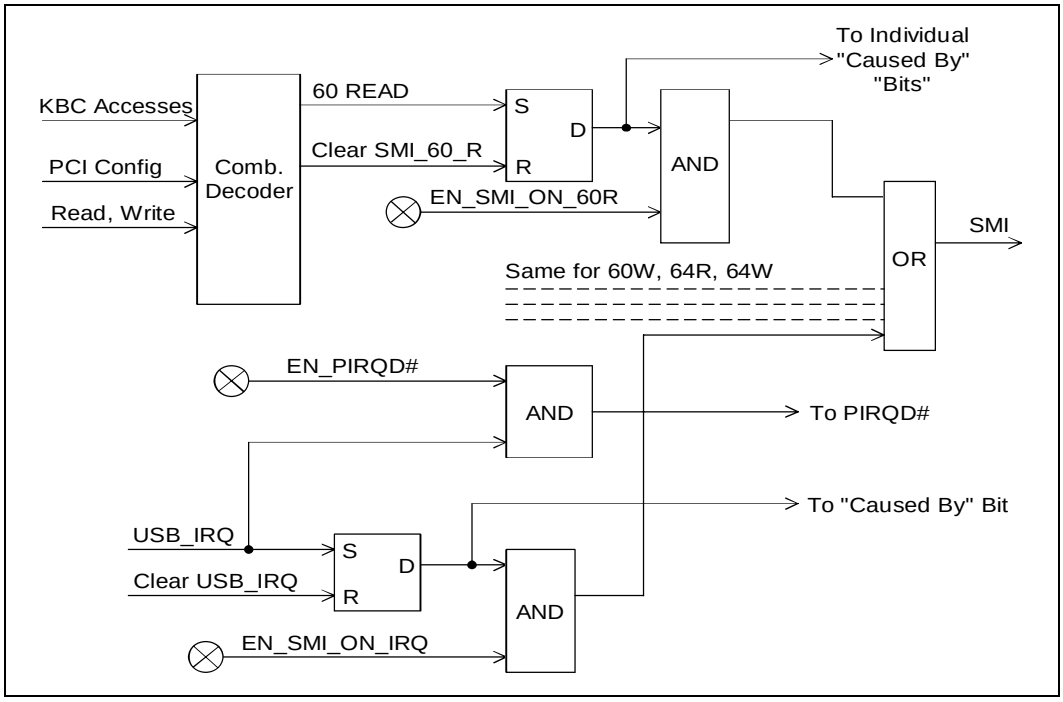


Table 5-45. USB Legacy Keyboard State Transitions (Sheet 1 of 2)

Current State	Action	Data Value	Next State	Comment
IDLE	64h / Write	D1h	GateState1	Standard D1 command. Cycle passed through to 8042. SMI# doesn't go active. PSTATE (offset C0, bit 6) goes to 1.
IDLE	64h / Write	Not D1h	IDLE	Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	64h / Read	N/A	IDLE	Bit 2 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Write	Don't Care	IDLE	Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Read	N/A	IDLE	Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
GateState1	60h / Write	XXh	GateState2	Cycle passed through to 8042, even if trap enabled in Bit 1 in Config Register. No SMI# generated. PSTATE remains 1. If data value is not DFh or DDh then the 8042 may chose to ignore it.

Table 5-45. USB Legacy Keyboard State Transitions (Sheet 2 of 2)

Current State	Action	Data Value	Next State	Comment
GateState1	64h / Write	D1h	GateState1	Cycle passed through to 8042, even if trap enabled via Bit 3 in Config Register. No SMI# generated. PSTATE remains 1. Stay in GateState1 because this is part of the double-trigger sequence.
GateState1	64h / Write	Not D1h	ILDE	Bit 3 in Config space determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState1	60h / Read	N/A	IDLE	This is an invalid sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState1	64h / Read	N/A	GateState1	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState2	64 / Write	FFh	IDLE	Standard end of sequence. Cycle passed through to 8042. PSTATE goes to 0. Bit 7 in Config Space determines if SMI# should be generated.
GateState2	64h / Write	Not FFh	IDLE	Improper end of sequence. Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState2	64h / Read	N/A	GateState2	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState2	60h / Write	XXh	IDLE	Improper end of sequence. Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState2	60h / Read	N/A	IDLE	Improper end of sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.

5.18.9 Function Level Reset Support (FLR)

The USB UHCI Controllers support the Function Level Reset (FLR) capability. The FLR capability can be used in conjunction with Intel Virtualization Technology. FLR allows an Operating System in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the Operating System to reset the whole device as if a PCI reset was asserted.

5.18.9.1 FLR Steps

5.18.9.1.1 FLR Initialization

1. A FLR is initiated by software writing a 1 to the Initiate FLR bit.
2. All subsequent requests targeting the Function will not be claimed and will be Master Abort Immediate on the bus. This includes any configuration, I/O or Memory cycles, however, the Function shall continue to accept completions targeting the Function.

5.18.9.1.2 FLR Operation

The Function will Reset all configuration, I/O and memory registers of the Function except those indicated otherwise and reset all internal states of the Function to the default or initial condition.

5.18.9.1.3 FLR Completion

The Initiate FLR bit is reset (cleared) when the FLR reset is completed. This bit can be used to indicate to the software that the FLR reset is completed.

Note: From the time Initiate FLR bit is written to 1, software must wait at least 100 ms before accessing the function.

5.19 USB EHCI Host Controllers (D29:F7 and D26:F7)

The ICH10 contains two Enhanced Host Controller Interface (EHCI) host controllers which support up to twelve USB 2.0 high-speed root ports. USB 2.0 allows data transfers up to 480 Mb/s using the same pins as the twelve USB full-speed/low-speed ports. The ICH10 contains port-routing logic that determines whether a USB port is controlled by one of the UHCI controllers or by one of the EHCI controllers. USB 2.0 based Debug Port is also implemented in the ICH10.

A summary of the key architectural differences between the USB UHCI host controllers and the EHCI host controller are shown in Table 5-46.

Table 5-46. UHCI vs. EHCI

Parameter	USB UHCI	USB EHCI
Accessible by	I/O space	Memory Space
Memory Data Structure	Single linked list	Separated into Periodic and Asynchronous lists
Differential Signaling Voltage	3.3 V	400 mV
Ports per Controller	2	6 or 8 (controller #1) and 6 or 4 (Controller #2)

5.19.1 EHC Initialization

The following descriptions step through the expected ICH10 Enhanced Host Controller (EHC) initialization sequence in chronological order, beginning with a complete power cycle in which the suspend well and core well have been off.

5.19.1.1 BIOS Initialization

BIOS performs a number of platform customization steps after the core well has powered up. Contact your Intel Field Representative for additional ICH10 BIOS information.

5.19.1.2 Driver Initialization

See Chapter 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0.

5.19.1.3 EHC Resets

In addition to the standard ICH10 hardware resets, portions of the EHC are reset by the HCRESET bit and the transition from the $D3_{HOT}$ device power management state to the D0 state. The effects of each of these resets are:

Reset	Does Reset	Does not Reset	Comments
HCRESET bit set.	Memory space registers except Structural Parameters (which is written by BIOS).	Configuration registers.	The HCRESET must only affect registers that the EHCI driver controls. PCI Configuration space and BIOS-programmed parameters can not be reset.
Software writes the Device Power State from $D3_{HOT}$ (11b) to D0 (00b).	Core well registers (except BIOS-programmed registers).	Suspend well registers; BIOS-programmed core well registers.	The D3-to-D0 transition must not cause wake information (suspend well) to be lost. It also must not clear BIOS-programmed registers because BIOS may not be invoked following the D3-to-D0 transition.

If the detailed register descriptions give exceptions to these rules, those exceptions override these rules. This summary is provided to help explain the reasons for the reset policies.

5.19.2 Data Structures in Main Memory

See Section 3 and Appendix B of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 for details.

5.19.3 USB 2.0 Enhanced Host Controller DMA

The ICH10 USB 2.0 EHC implements three sources of USB packets. They are, in order of priority on USB during each microframe:

1. The USB 2.0 Debug Port (see Section USB 2.0 Based Debug Port),
2. The Periodic DMA engine, and
3. The Asynchronous DMA engine.

The ICH10 always performs any currently-pending debug port transaction at the beginning of a microframe, followed by any pending periodic traffic for the current microframe. If there is time left in the microframe, then the EHC performs any pending asynchronous traffic until the end of the microframe (EOF1). Note that the debug port traffic is only presented on one port (Port #0), while the other ports are idle during this time.

5.19.4 Data Encoding and Bit Stuffing

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0.*

5.19.5 Packet Formats

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0*.

The ICH10 EHCI allows entrance to USB test modes, as defined in the USB 2.0 specification, including Test J, Test Packet, etc. However note that the ICH10 Test Packet test mode interpacket gap timing may not meet the USB 2.0 specification.

5.19.6 USB 2.0 Interrupts and Error Conditions

Section 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 goes into detail on the EHC interrupts and the error conditions that cause them. All error conditions that the EHC detects can be reported through the EHCI Interrupt status bits. Only ICH10-specific interrupt and error-reporting behavior is documented in this section. The EHCI Interrupts Section must be read first, followed by this section of the datasheet to fully comprehend the EHC interrupt and error-reporting functionality.

- Based on the EHC's Buffer sizes and buffer management policies, the Data Buffer Error can never occur on the ICH10.
- Master Abort and Target Abort responses from hub interface on EHC-initiated read packets will be treated as Fatal Host Errors. The EHC halts when these conditions are encountered.
- The ICH10 may assert the interrupts which are based on the interrupt threshold as soon as the status for the last complete transaction in the interrupt interval has been posted in the internal write buffers. The requirement in the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 (that the status is written to memory) is met internally, even though the write may not be seen on DMI before the interrupt is asserted.
- Since the ICH10 supports the 1024-element Frame List size, the Frame List Rollover interrupt occurs every 1024 milliseconds.
- The ICH10 delivers interrupts using PIRQH#.
- The ICH10 does not modify the CERR count on an Interrupt IN when the "Do Complete-Split" execution criteria are not met.
- For complete-split transactions in the Periodic list, the "Missed Microframe" bit does not get set on a control-structure-fetch that fails the late-start test. If subsequent accesses to that control structure do not fail the late-start test, then the "Missed Microframe" bit will get set and written back.

5.19.6.1 Aborts on USB 2.0-Initiated Memory Reads

If a read initiated by the EHC is aborted, the EHC treats it as a fatal host error. The following actions are taken when this occurs:

- The Host System Error status bit is set
- The DMA engines are halted after completing up to one more transaction on the USB interface
- If enabled (by the Host System Error Enable), then an interrupt is generated
- If the status is Master Abort, then the Received Master Abort bit in configuration space is set
- If the status is Target Abort, then the Received Target Abort bit in configuration space is set
- If enabled (by the SERR Enable bit in the function's configuration space), then the Signaled System Error bit in configuration bit is set.

5.19.7 USB 2.0 Power Management

5.19.7.1 Pause Feature

This feature allows platforms to dynamically enter low-power states during brief periods when the system is idle (i.e., between keystrokes). This is useful for enabling power management features in the ICH10. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHC is enabled, it regularly accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system, thus preventing the power managed states to be entered. Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHC's DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause only prevents the EHC from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state).

5.19.7.2 Suspend Feature

The *Enhanced Host Controller Interface (EHCI) For Universal Serial Bus Specification*, Section 4.3 describes the details of Port Suspend and Resume.

5.19.7.3 ACPI Device States

The USB 2.0 function only supports the D0 and D3 PCI Power Management states. Notes regarding the ICH10 implementation of the Device States:

1. The EHC hardware does not inherently consume any more power when it is in the D0 state than it does in the D3 state. However, software is required to suspend or disable all ports prior to entering the D3 state such that the maximum power consumption is reduced.
2. In the D0 state, all implemented EHC features are enabled.
3. In the D3 state, accesses to the EHC memory-mapped I/O range will master abort. Note that, since the Debug Port uses the same memory range, the Debug Port is only operational when the EHC is in the D0 state.
4. In the D3 state, the EHC interrupt must never assert for any reason. The internal PME# signal is used to signal wake events, etc.
5. When the Device Power State field is written to D0 from D3, an internal reset is generated. See section EHC Resets for general rules on the effects of this reset.
6. Attempts to write any other value into the Device Power State field other than 00b (D0 state) and 11b (D3 state) will complete normally without changing the current value in this field.

5.19.7.4 ACPI System States

The EHC behavior as it relates to other power management states in the system is summarized in the following list:

— The System is always in the S0 state when the EHC is in the D0 state. However, when the EHC is in the D3 state, the system may be in any power management state (including S0).

— When in D0, the Pause feature (See Section 5.19.7.1) enables dynamic processor low-power states to be entered.

— The PLL in the EHC is disabled when entering the S3/S4/S5 states (core power turns off).

— All core well logic is reset in the S3/S4/S5 states.

5.19.8 Interaction with UHCI Host Controllers

The Enhanced Host controllers share its ports with UHCI Host controllers in the ICH10. The UHC at D29:F0 shares ports 0 and 1; the UHC at D29:F1 shares ports 2 and 3; the UHC at D29:F2 shares ports 4 and 5 with the EHC at D29:F7, while the UHC at D26:F0 shares ports 6 and 7, the UHC at D26:F1 shares ports 8 and 9, and the UHC at D26:F2 shares ports 10 and 11 with EHC at D26:F7. There is very little interaction between the Enhanced and the UHCI controllers other than the muxing control which is provided as part of the EHC. Figure 5-14 shows the USB Port Connections at a conceptual level.

Note: D26:F2 can be configured as D29:F3 during BIOS post.

5.19.8.1 Port-Routing Logic

Integrated into the EHC functionality is port-routing logic, which performs the muxing between the UHCI and EHCI host controllers. The ICH10 conceptually implements this logic as described in Section 4.2 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0. If a device is connected that is not capable of USB 2.0's high-speed signaling protocol or if the EHCI software drivers are not present as indicated by the Configured Flag, then the UHCI controller owns the port. Owning the port means that the differential output is driven by the owner and the input stream is only visible to the owner. The host controller that is not the owner of the port internally sees a disconnected port.

Figure 5-14. Intel® ICH10-USB Port Connections Default Six and Six Configuration

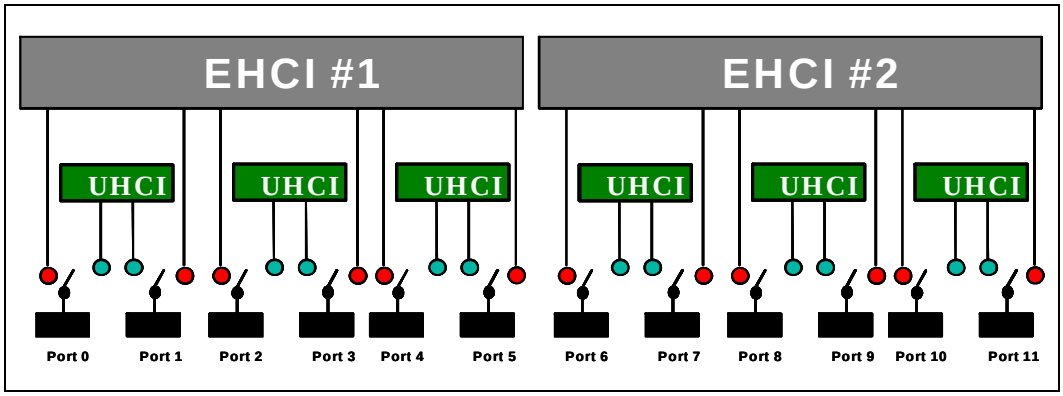
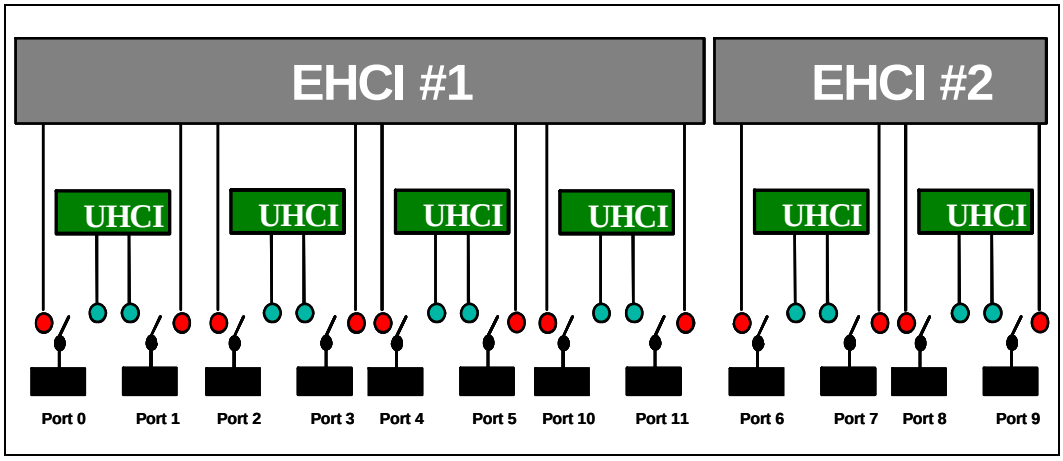


Figure 5-15. Intel® ICH10-USB Port Connections Eight and Four Configuration



Note that the port-routing logic is the only block of logic within the ICH10 that observes the physical (real) connect/disconnect information. The port status logic inside each of the host controllers observes the electrical connect/disconnect information that is generated by the port-routing logic.

Only the differential signal pairs are multiplexed/de-multiplexed between the UHCI and EHCI host controllers. The other USB functional signals are handled as follows:

- The Overcurrent inputs (OC[11:0]#) are directly routed to both controllers. An overcurrent event is recorded in both controllers' status registers.

The Port-Routing logic is implemented in the Suspend power well so that re-enumeration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

The ICH10 also allows the USB Debug Port traffic to be routed in and out of Port #0 and Port #6. When in this mode, the Enhanced Host controller is the owner of Port #0 and Port #6.

5.19.8.2 Device Connects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 describes the details of handling Device Connects in Section 4.2. There are four general scenarios that are summarized below.

1. Configure Flag = 0 and a full-speed/low-speed-only Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHC (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process.
2. Configure Flag = 0 and a high-speed-capable Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHC (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process. Since the UHC does not perform the high-speed chirp handshake, the device operates in compatible mode.
3. Configure Flag = 1 and a full-speed/low-speed-only Device is connected
   - In this case, the EHC is the owner of the port before the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHC hardware has cleared (not set) the Port Enable bit in the EHC's PORTSC register. The EHCI driver then writes a 1 to the Port Owner bit in the same register, causing the UHC to see a connect event and the EHC to see an "electrical" disconnect event. The UHCI driver and hardware handle the connection and initialization process from that point on. The EHCI driver and hardware handle the perceived disconnect.
4. Configure Flag = 1 and a high-speed-capable Device is connected
   - In this case, the EHC is the owner of the port before, and remains the owner after, the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHC hardware has set the Port Enable bit in the EHC's PORTSC register. The port is functional at this point. The UHC continues to see an unconnected port.

5.19.8.3 Device Disconnects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 describes the details of handling Device Connects in Section 4.2. There are three general scenarios that are summarized below.

1. Configure Flag = 0 and the device is disconnected
   — In this case, the UHC is the owner of the port both before and after the disconnect occurs. The EHC (except for the port-routing logic) never sees a device attached. The UHCI driver handles disconnection process.
2. Configure Flag = 1 and a full-speed/low-speed-capable Device is disconnected
   — In this case, the UHC is the owner of the port before the disconnect occurs. The disconnect is reported by the UHC and serviced by the associated UHCI driver. The port-routing logic in the EHC cluster forces the Port Owner bit to 0, indicating that the EHC owns the unconnected port.
3. Configure Flag = 1 and a high-speed-capable Device is disconnected
   — In this case, the EHC is the owner of the port before, and remains the owner after, the disconnect occurs. The EHCI hardware and driver handle the disconnection process. The UHC never sees a device attached.

5.19.8.4 Effect of Resets on Port-Routing Logic

As mentioned above, the Port Routing logic is implemented in the suspend power well so that remuneration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

Reset Event	Effect on Configure Flag	Effect on Port Owner Bits
Suspend Well Reset	cleared (0)	set (1)
Core Well Reset	no effect	no effect
D3-to-D0 Reset	no effect	no effect
HCRESET	cleared (0)	set (1)

5.19.9 USB 2.0 Legacy Keyboard Operation

The ICH10 must support the possibility of a keyboard downstream from either a full-speed/low-speed or a high-speed port. The description of the legacy keyboard support is unchanged from USB 1.1 (See Section 5.18.8).

The EHC provides the basic ability to generate SMIs on an interrupt event, along with more sophisticated control of the generation of SMIs.

5.19.10 USB 2.0 Based Debug Port

The ICH10 supports the elimination of the legacy COM ports by providing the ability for new debugger software to interact with devices on a USB 2.0 port.

High-level restrictions and features are:

- Operational before USB 2.0 drivers are loaded.
- Functions even when the port is disabled.
- Works even though non-configured port is default-routed to the UHCI. Note that the Debug Port can not be used to debug an issue that requires a full-speed/low-speed device on Port #0 using the UHCI drivers.
- Allows normal system USB 2.0 traffic in a system that may only have one USB port.
- Debug Port device (DPD) must be high-speed capable and connect directly to Port #0 and Port #6 on ICH10 systems (e.g., the DPD cannot be connected to Port #0/Port #6 through a hub).
- Debug Port FIFO always makes forward progress (a bad status on USB is simply presented back to software).
- The Debug Port FIFO is only given one USB access per microframe.

The Debug port facilitates operating system and device driver debug. It allows the software to communicate with an external console using a USB 2.0 connection. Because the interface to this link does not go through the normal USB 2.0 stack, it allows communication with the external console during cases where the operating system is not loaded, the USB 2.0 software is broken, or where the USB 2.0 software is being debugged. Specific features of this implementation of a debug port are:

- Only works with an external USB 2.0 debug device (console)
- Implemented for a specific port on the host controller
- Operational anytime the port is not suspended AND the host controller is in D0 power state.
- Capability is interrupted when port is driving USB RESET

5.19.10.1 Theory of Operation

There are two operational modes for the USB debug port:

1. Mode 1 is when the USB port is in a disabled state from the viewpoint of a standard host controller driver. In Mode 1, the Debug Port controller is required to generate a “keepalive” packets less than 2 ms apart to keep the attached debug device from suspending. The keepalive packet should be a standalone 32-bit SYNC field.
2. Mode 2 is when the host controller is running (i.e., host controller’s *Run/Stop#* bit is 1). In Mode 2, the normal transmission of SOF packets will keep the debug device from suspending.

Behavioral Rules

1. In both modes 1 and 2, the Debug Port controller must check for software requested debug transactions at least every 125 microseconds.
2. If the debug port is enabled by the debug driver, and the standard host controller driver resets the USB port, USB debug transactions are held off for the duration of the reset and until after the first SOF is sent.
3. If the standard host controller driver suspends the USB port, then USB debug transactions are held off for the duration of the suspend/resume sequence and until after the first SOF is sent.
4. The ENABLED_CNT bit in the debug register space is independent of the similar port control bit in the associated Port Status and Control register.

Table 5-47 shows the debug port behavior related to the state of bits in the debug registers as well as bits in the associated Port Status and Control register.

Table 5-47. Debug Port Behavior

OWNER_CNT	ENABLED_CT	Port Enable	Run / Stop	Suspend	Debug Port Behavior
0	X	X	X	X	Debug port is not being used. Normal operation.
1	0	X	X	X	Debug port is not being used. Normal operation.
1	1	0	0	X	Debug port in Mode 1. SYNC keepalives sent plus debug traffic
1	1	0	1	X	Debug port in Mode 2. SOF (and only SOF) is sent as keepalive. Debug traffic is also sent. Note that no other normal traffic is sent out this port, because the port is not enabled.
1	1	1	0	0	invalid. Host controller driver should never put controller into this state (enabled, not running and not suspended).
1	1	1	0	1	Port is suspended. No debug traffic sent.
1	1	1	1	0	Debug port in Mode 2. Debug traffic is interspersed with normal traffic.
1	1	1	1	1	Port is suspended. No debug traffic sent.

5.19.10.1.1 OUT Transactions

An Out transaction sends data to the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is set

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   - — USB_ADDRESS_CNF
   - — USB_ENDPOINT_CNF
   - — DATA_BUFFER[63:0]
   - — TOKEN_PID_CNT[7:0]
   - — SEND_PID_CNT[15:8]
   - — DATA_LEN_CNT
   - — WRITE_READ#_CNT: (note: this will always be 1 for OUT transactions)
   - — GO_CNT: (note: this will always be 1 to initiate the transaction)

2. The debug port controller sends a token packet consisting of:
   — SYNC
   — TOKEN_PID_CNT field
   — USB_ADDRESS_CNT field
   — USB_ENDPOINT_CNT field
   — 5-bit CRC field
3. After sending the token packet, the debug port controller sends a data packet consisting of:
   — SYNC
   — SEND_PID_CNT field
   — The number of data bytes indicated in DATA_LEN_CNT from the DATA_BUFFER
   — 16-bit CRC

   NOTE: ‘A DATA_LEN_CNT value of 0 is valid in which case no data bytes would be included in the packet.
4. After sending the data packet, the controller waits for a handshake response from the debug device.

- If a handshake is received, the debug port controller:
  — a. Places the received PID in the RECEIVED_PID_STS field
  — b. Resets the ERROR_GOOD#_STS bit
  — c. Sets the DONE_STS bit
- If no handshake PID is received, the debug port controller:
  — a. Sets the EXCEPTION_STS field to 001b
  — b. Sets the ERROR_GOOD#_STS bit
  — c. Sets the DONE_STS bit

5.19.10.1.2 IN Transactions

An IN transaction receives data from the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is reset

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   — USB_ADDRESS_CNF
   — USB_ENDPOINT_CNF
   — TOKEN_PID_CNT[7:0]
   — DATA_LEN_CNT
   — WRITE_READ#_CNT: (Note: This will always be 0 for IN transactions.)
   — GO_CNT: (Note: This will always be 1 to initiate the transaction.)

2. The debug port controller sends a token packet consisting of:
   — SYNC
   — TOKEN_PID_CNT field
   — USB_ADDRESS_CNT field
   — USB_ENDPOINT_CNT field
   — 5-bit CRC field.
3. After sending the token packet, the debug port controller waits for a response from the debug device.
   If a response is received:
   — The received PID is placed into the RECEIVED_PID_STS field
   — Any subsequent bytes are placed into the DATA_BUFFER
   — The DATA_LEN_CNT field is updated to show the number of bytes that were received after the PID.
4. If a valid packet was received from the device that was one byte in length (indicating it was a handshake packet), then the debug port controller:
   — Resets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit
5. If a valid packet was received from the device that was more than one byte in length (indicating it was a data packet), then the debug port controller:
   — Transmits an ACK handshake packet
   — Resets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit
6. If no valid packet is received, then the debug port controller:
   — Sets the EXCEPTION_STS field to 001b
   — Sets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit.

5.19.10.1.3 Debug Software

Enabling the Debug Port

There are two mutually exclusive conditions that debug software must address as part of its startup processing:

- The EHCI has been initialized by system software
- The EHCI has not been initialized by system software

Debug software can determine the current ‘initialized’ state of the EHCI by examining the Configure Flag in the EHCI USB 2.0 Command Register. If this flag is set, then system software has initialized the EHCI. Otherwise the EHCI should not be considered initialized. Debug software will initialize the debug port registers depending on the state of the EHCI. However, before this can be accomplished, debug software must determine which root USB port is designated as the debug port.

Determining the Debug Port

Debug software can easily determine which USB root port has been designated as the debug port by examining bits 20:23 of the EHCI Host Controller Structural Parameters register. This 4-bit field represents the numeric value assigned to the debug port (i.e., 0000 = port 0).

Debug Software Startup with Non-Initialized EHCI

Debug software can attempt to use the debug port if after setting the OWNER_CNT bit, the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected to the port, then debug software must reset/enable the port. Debug software does this by setting and then clearing the Port Reset bit the PORTSC register. To ensure a successful reset, debug software should wait at least 50 ms before clearing the Port Reset bit. Due to possible delays, this bit may not change to 0 immediately; reset is complete when this bit reads as 0. Software must not continue until this bit reads 0.

If a high-speed device is attached, the EHCI will automatically set the Port Enabled/Disabled bit in the PORTSC register and the debug software can proceed. Debug software should set the ENABLED_CNT bit in the Debug Port Control/Status register, and then reset (clear) the Port Enabled/Disabled bit in the PORTSC register (so that the system host controller driver does not see an enabled port when it is first loaded).

Debug Software Startup with Initialized EHCI

Debug software can attempt to use the debug port if the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected, then debug software must set the OWNER_CNT bit and then the ENABLED_CNT bit in the Debug Port Control/Status register.

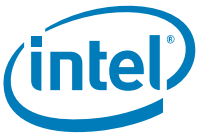
Determining Debug Peripheral Presence

After enabling the debug port functionality, debug software can determine if a debug peripheral is attached by attempting to send data to the debug peripheral. If all attempts result in an error (Exception bits in the Debug Port Control/Status register indicates a Transaction Error), then the attached device is not a debug peripheral. If the debug port peripheral is not present, then debug software may choose to terminate or it may choose to wait until a debug peripheral is connected.

5.19.11 USB Pre-Fetch Based Pause

The Pre-Fetch Based Pause is a power management feature in USB (EHCI) host controllers to ensure maximum C3/C4 processor power state time with C2 popup. This feature applies to the period schedule, and works by allowing the DMA engine to identify periods of idleness and preventing the DMA engine from accessing memory when the periodic schedule is idle. Typically in the presence of periodic devices with multiple millisecond poll periods, the periodic schedule will be idle for several frames between polls.

The USB Pre-Fetch Based Pause feature is disabled by setting bit 4 of EHCI Configuration Register Section 17.1.30.



5.19.12 Function Level Reset Support (FLR)

The USB EHCI Controllers support the Function Level Reset (FLR) capability. The FLR capability can be used in conjunction with Intel Virtualization Technology. FLR allows an Operating System in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the Operating System to reset the whole device as if a PCI reset was asserted.

5.19.12.1 FLR Steps

5.19.12.1.1 FLR Initialization

1. A FLR is initiated by software writing a '1' to the Initiate FLR bit.
2. All subsequent requests targeting the Function will not be claimed and will be Master Abort Immediate on the bus. This includes any configuration, I/O or Memory cycles, however, the Function shall continue to accept completions targeting the Function.

5.19.12.1.2 FLR Operation

The Function will Reset all configuration, I/O and memory registers of the Function except those indicated otherwise and reset all internal states of the Function to the default or initial condition.

5.19.12.1.3 FLR Completion

The Initiate FLR bit is reset (cleared) when the FLR reset is completed. This bit can be used to indicate to the software that the FLR reset is completed.

Note: From the time Initiate FLR bit is written to 1, software must wait at least 100 ms before accessing the function.

5.20 SMBus Controller (D31:F3)

The ICH10 provides an System Management Bus (SMBus) 2.0 host controller as well as an SMBus Slave Interface. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The ICH10 is also capable of operating in a mode in which it can communicate with I^2C compatible devices.

The ICH10 can perform SMBus messages with either packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking is performed in hardware by the ICH10.

The Slave Interface allows an external master to read from or write to the ICH10. Write cycles can be used to cause certain events or pass messages, and the read cycles can be used to determine the state of various status bits. The ICH10's internal host controller cannot access the ICH10's internal Slave Interface.

The ICH10 SMBus logic exists in Device 31:Function 3 configuration space, and consists of a transmit data path, and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The ICH10 SMBus controller logic is clocked by RTC clock.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the new Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done via the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.

The ICH10 SMBus host controller checks for parity errors as a target. If an error is detected, the detected parity error bit in the PCI Status Register (Device 31:Function 3:Offset 06h:bit 15) is set. If bit 6 and bit 8 of the PCI Command Register (Device 31:Function 3:Offset 04h) are set, an SERR# is generated and the signaled SERR# bit in the PCI Status Register (bit 14) is set.

5.20.1 Host Controller

The SMBus host controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification, Version 2.0*): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, Block Write–Block Read Process Call, and Host Notify.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the “active registers” (Host Control, Host Command, Transmit Slave Address, Data 0, Data 1) should not be changed or read until the interrupt status bit (INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

The ICH10 supports the *System Management Bus (SMBus) Specification, Version 2.0*. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals can be tied together externally depending on TCO mode used. Refer to Section 5.14.2 for more details.

Using the SMB host controller to send commands to the ICH10’s SMB slave port is not supported.

5.20.1.1 Command Protocols

In all of the following commands, the Host Status Register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST_BUSY bit is set. If the command completes successfully, the INTR bit will be set in the Host Status Register. If the device does not respond with an acknowledge, and the transaction times out, the DEV_ERR bit is set. If software sets the KILL bit in the Host Control Register while the command is running, the transaction will stop and the FAILED bit will be set.

Quick Command

When programmed for a Quick Command, the Transmit Slave Address Register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the PEC_EN bit to 0 when performing the Quick Command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.1 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address and Device Command Registers are sent.

For the Receive Byte command, the Transmit Slave Address Register is sent. The data received is stored in the DATA0 register. Software must force the I2C_EN bit to 0 when running this command.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Write Byte / Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address, Device Command, and Data0 Registers are sent. In addition, the Data1 Register is sent on a Write Word command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.4 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Read Byte / Word

Reading data is slightly more complicated than writing data. First the ICH10 must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data. Software must force the I2C_EN bit to 0 when running this command.

When programmed for the read byte/word command, the Transmit Slave Address and Device Command Registers are sent. Data is received into the DATA0 on the read byte, and the DAT0 and DATA1 registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the ICH10 transmits the Transmit Slave Address, Host Command, DATA0 and DATA1 registers. Data received from the device is stored in the DATA0 and DATA1 registers. The Process Call command with I2C_EN set and the PEC_EN bit set produces undefined results. Software must force either I2C_EN or PEC_EN to 0 when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: For process call command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

Note: If the I2C_EN bit is set, the protocol sequence changes slightly: the Command Code (bits 18:11 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 19 in the sequence).

Block Read / Write

The ICH10 contains a 32-byte buffer for read and write data which can be enabled by setting bit 1 of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the ICH10, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

The byte count field is transmitted but ignored by the ICH10 as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force the I2C_EN bit or both the PEC_EN and AAC bits to 0 when running this command.

The block write begins with a slave address and a write condition. After the command code the ICH10 issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address, Device Command, and Data0 (count) registers are sent. Data is then sent from the Block Data Byte register; the total data sent being the value stored in the Data0 Register. On block read commands, the first byte received is stored in the Data0 register, and the remaining bytes are stored in the Block Data Byte register. See section 5.5.7 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: For Block Write, if the I2C_EN bit is set, the format of the command changes slightly. The ICH10 will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message. Also, the Block Write protocol sequence changes slightly: the Byte Count (bits 27:20 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 28 in the sequence).

I²C Read

This command allows the ICH10 to perform block reads to certain I²C devices, such as serial E²PROMs. The SMBus Block Read supports the 7-bit addressing mode only.

However, this does not allow access to devices using the I²C "Combined Format" that has data bytes after the address. Typically these data bytes correspond to an offset (address) within the serial memory chips.

Note: This command is supported independent of the setting of the I2C_EN bit. The I²C Read command with the PEC_EN bit set produces undefined results. Software must force both the PEC_EN and AAC bit to 0 when running this command.

For I²C Read command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

The format that is used for the command is shown in Table 5-48.

Table 5-48. I²C Block Read

Bit	Description
1	Start
8:2	Slave Address — 7 bits
9	Write
10	Acknowledge from slave
18:11	Send DATA1 register
19	Acknowledge from slave
20	Repeated Start
27:21	Slave Address — 7 bits
28	Read
29	Acknowledge from slave
37:30	Data byte 1 from slave — 8 bits
38	Acknowledge
46:39	Data byte 2 from slave — 8 bits
47	Acknowledge
–	Data bytes from slave / Acknowledge
–	Data byte N from slave — 8 bits
–	NOT Acknowledge
–	Stop

The ICH10 will continue reading data from the peripheral until the NAK is received.

Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- $M \geq 1$ byte
- $N \geq 1$ byte
- $M + N \leq 32$ bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the command register (offset 2h) to reset the 32 byte buffer pointer prior to reading the block data register.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

Note: E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

5.20.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. The ICH10 continuously monitors the SMBDATA line. When the ICH10 is attempting to drive the bus to a 1 by letting go of the SMBDATA line, and it samples SMBDATA low, then some other master is driving the bus and the ICH10 will stop transferring data.

If the ICH10 sees that it has lost arbitration, the condition is called a collision. The ICH10 will set the BUS_ERR bit in the Host Status Register, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

When the ICH10 is a SMBus master, it drives the clock. When the ICH10 is sending address or command as an SMBus master, or data bytes as a master on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The ICH10 will also ensure minimum time between SMBus transactions as a master.

Note: The ICH10 supports the same arbitration protocol for both the SMBus and the System Management (SMLINK) interfaces.

5.20.3 Bus Timing

5.20.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the ICH10 as an SMBus master would like. They have the capability of stretching the low time of the clock. When the ICH10 attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The ICH10 monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

5.20.3.2 Bus Time Out (Intel® ICH10 as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The ICH10 will discard the cycle and set the DEV_ERR bit. The time out minimum is 25 ms (800 RTC clocks). The time-out counter inside the ICH10 will start after the last bit of data is transferred by the ICH10 and it is waiting for a response.

The 25 ms timeout counter will not count under the following conditions:

1. BYTE_DONE_STATUS bit (SMBus I/O Offset 00h, bit 7) is set
2. The SECOND_TO_STS bit (TCO I/O Offset 06h, bit 1) is not set (this indicates that the system has not locked up).

5.20.4 Interrupts / SMI#

The ICH10 SMBus controller uses PIRQB# as its interrupt pin. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS_SMI_EN bit (Device 31:Function 0:Offset 40h:bit 1).

Table 5-50 and Table 5-51 specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 5-49. Enable for SMBALERT#

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 11h, Bit 2)	Result
SMBALERT# asserted low (always reported in Host Status Register, Bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

Table 5-50. Enables for SMBus Slave Write and SMBus Host Events

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit1)	Event
Slave Write to Wake/SMI# Command	X	X	Wake generated when asleep. Slave SMI# generated when awake (SMBUS_SMI_STS).
Slave Write to SMLINK_SLAVE_SMI Command	X	X	Slave SMI# generated when in the S0 state (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 5-51. Enables for the Host Notify Command

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 11h, bit 0)	SMB_SMI_EN (Host Config Register, D31:F3:Off40h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 11h, bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

5.20.5 SMBALERT#

SMBALERT# is multiplexed with GPIO[11]. When enable and the signal is asserted, The ICH10 can generate an interrupt, an SMI#, or a wake event from S1–S5.

5.20.6 SMBus CRC Generation and Checking

If the AAC bit is set in the Auxiliary Control register, the ICH10 automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the PEC register for CRC. The PEC bit must not be set in the Host Control register if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the DEV_ERR bit and the CRCE bit in the Auxiliary Status register at offset 0Ch will be set.

5.20.7 SMBus Slave Interface

The ICH10's SMBus Slave interface is accessed via the SMBus. The SMBus slave logic will not generate or handle receiving the PEC byte and will only act as a Legacy Alerting Protocol device. The slave interface allows the ICH10 to decode cycles, and allows an external microcontroller to perform specific actions. Key features and capabilities include:

- Supports decode of three types of messages: Byte Write, Byte Read, and Host Notify.
- Receive Slave Address register: This is the address that the ICH10 decodes. A default value is provided so that the slave interface can be used without the processor having to program this register.
- Receive Slave Data register in the SMBus I/O space that includes the data written by the external microcontroller.
- Registers that the external microcontroller can read to get the state of the ICH10.
- Status bits to indicate that the SMBus slave logic caused an interrupt or SMI# due to the reception of a message that matched the slave address.
  - — Bit 0 of the Slave Status Register for the Host Notify command
  - — Bit 16 of the SMI Status Register (Section 13.8.3.13) for all others

Note: The external microcontroller should not attempt to access the Intel ICH10's SMBus slave logic until either:

- — 800 milliseconds after both: RTCRST# is high and RSMRST# is high, OR
- — The PLTRST# deasserts

If a master leaves the clock and data bits of the SMBus interface at 1 for 50 µs or more in the middle of a cycle, the ICH10 slave logic's behavior is undefined. This is interpreted as an unexpected idle and should be avoided when performing management activities to the slave logic.

Note: When an external microcontroller accesses the SMBus Slave Interface over the SMBus a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the ICH10 slave address (RCV_SLVA) is left at 44h (default), the external micro controller would use an address of 88h/89h (write/read).

5.20.7.1 Format of Slave Write Cycle

The external master performs Byte Write commands to the ICH10 SMBus Slave I/F. The "Command" field (bits 11:18) indicate which register is being accessed. The Data field (bits 20:27) indicate the value that should be written to that register.

Table 5-52 has the values associated with the registers.

Table 5-52. Slave Write Registers

Register	Function
0	Command Register. See Table 5-53 below for legal values written to this register.
1–3	Reserved
4	Data Message Byte 0
5	Data Message Byte 1
6–7	Reserved
8	Reserved
9–FFh	Reserved

NOTE: The external microcontroller is responsible to make sure that it does not update the contents of the data byte registers until they have been read by the system processor. The ICH10 overwrites the old value with any new value received. A race condition is possible where the new value is being written to the register just at the time it is being read. ICH10 will not attempt to cover this race condition (i.e., unpredictable results in this case).

Table 5-53. Command Types (Sheet 1 of 2)

Command Type	Description
0	Reserved
1	**WAKE/SMI#.** This command wakes the system if it is not already awake. If system is already awake, an SMI# is generated. **NOTE:** The SMB_WAK_STS bit will be set by this command, even if the system is already awake. The SMI handler should then clear this bit.
2	**Unconditional Powerdown.** This command sets the PWRBTNOR_STS bit, and has the same effect as the Powerbutton Override occurring.
3	**HARD RESET WITHOUT CYCLING:** This command causes a hard reset of the system (does not include cycling of the power supply). This is equivalent to a write to the CF9h register with bits 2:1 set to 1, but bit 3 set to 0.
4	**HARD RESET SYSTEM.** This command causes a hard reset of the system (including cycling of the power supply). This is equivalent to a write to the CF9h register with bits 3:1 set to 1.
5	**Disable the TCO Messages.** This command will disable the Intel ICH10 from sending Heartbeat and Event messages (as described in Section 5.14). Once this command has been executed, Heartbeat and Event message reporting can only be re-enabled by assertion and deassertion of the RSMRST# signal.
6	**WD RELOAD:** Reload watchdog timer.
7	Reserved

Table 5-53. Command Types (Sheet 2 of 2)

Command Type	Description
8	**SMLINK_SLV_SMI.** When ICH10 detects this command type while in the S0 state, it sets the SMLINK_SLV_SMI_STS bit (see Section 13.9.5). This command should only be used if the system is in an S0 state. If the message is received during S1–S5 states, the ICH10 acknowledges it, but the SMLINK_SLV_SMI_STS bit does not get set. **NOTE:** It is possible that the system transitions out of the S0 state at the same time that the SMLINK_SLV_SMI command is received. In this case, the SMLINK_SLV_SMI_STS bit may get set but not serviced before the system goes to sleep. Once the system returns to S0, the SMI associated with this bit would then be generated. Software must be able to handle this scenario.
9-FFh	Reserved.

5.20.7.2 Format of Read Command

The external master performs Byte Read commands to the ICH10 SMBus Slave interface. The “Command” field (bits 18:11) indicate which register is being accessed. The Data field (bits 30:37) contain the value that should be read from that register.

Table 5-54. Slave Read Cycle Format

Bit	Description	Driven by	Comment
1	Start	External Microcontroller	
2-8	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
9	Write	External Microcontroller	Always 0
10	ACK	Intel ICH10	
11-18	Command code – 8 bits	External Microcontroller	Indicates which register is being accessed. See Table 5-55 below for list of implemented registers.
19	ACK	Intel ICH10	
20	Repeated Start	External Microcontroller	
21-27	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
28	Read	External Microcontroller	Always 1
29	ACK	Intel ICH10	
30-37	Data Byte	Intel ICH10	Value depends on register being accessed. Table 5-55 below for list of implemented registers.
38	NOT ACK	External Microcontroller	
39	Stop	External Microcontroller	

Table 5-55. Data Values for Slave Read Registers (Sheet 1 of 2)

Register	Bits	Description
0	7:0	Reserved for capabilities indication. Should always return 00h. Future chips may return another value to indicate different capabilities.
1	2:0	System Power State 000 = S0 001 = S1 010 = Reserved 011 = S3 100 = S4 101 = S5 110 = Reserved 111 = Reserved
	7:3	Reserved
2	3:0	Reserved
	7:4	Reserved
3	5:0	**Watchdog Timer current value** Note that Watchdog Timer has 10 bits, but this field is only 6 bits. If the current value is greater than 3Fh, ICH10 will always report 3Fh in this field.
	7:6	Reserved
4	0	1 = The **Intruder Detect** (INTRD_DET) bit is set. This indicates that the system cover has probably been opened.
	1 (Consumer Only)	1 = BTI **Temperature Event** occurred. This bit will be set if the Intel ICH10's THRM# input signal is at a valid low voltage state. This bit will be clear if the THRM# input signal is at a valid high voltage state. **NOTE:** This bit interprets the behavior if the THRM# pin as active low. This bit is set independent of the TRM#_POL bit setting.
	1 (Corporate Only)	1 = **BTI Temperature Event** occurred. This bit will be set if the Intel ICH10's THRM# input signal is active. Else this bit will read 0. **NOTE:** The THRM# pin is in core well and accurate reflection of the THRM# pin is dependent on the platform being in S0.
	2	**DOA CPU Status**. This bit will be 1 to indicate that the processor is dead
	3	1 = **SECOND_TO_STS** bit set. This bit will be set after the second time-out (SECOND_TO_STS bit) of the Watchdog Timer occurs.
	6:4	Reserved. Will always be 0, but software should ignore.
	7	Reflects the value of the GPIO[11]/SMBALERT# pin (and is dependent upon the value of the GPI_INV[11] bit. If the GPI_INV[11] bit is 1, then the value in this bit equals the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0). If the GPI_INV[11] bit is 0, then the value of this bit will equal the inverse of the level of the GPIO[11]/SMBALERT# pin (high = 0, low = 1).
5	0	**FWH bad bit.** This bit will be 1 to indicate that the FWH read returned FFh, which indicates that it is probably blank.
	1	Reserved
	2	**CPU Power Failure Status:** '1' if the CPUPWR_FLR bit in the GEN_PMCON_2 register is set.
	3	**INIT# due to receiving Shutdown message:** This event is visible from the reception of the shutdown message until a platform reset is done if the Shutdown Policy Select bit (SPS) is configured to drive INIT#. When the SPS bit is configured to generate PLTRST# based on shutdown, this register bit will always return 0. Events on signal will not create a event message
	4	Reserved

Table 5-55. Data Values for Slave Read Registers (Sheet 2 of 2)

Register	Bits	Description
	5	**POWER_OK_BAD:** Indicates the failure core power well ramp during boot/resume. This bit will be active if the SLP_S3# pin is de-asserted and PWROK pin is not asserted.
	6	**Thermal Trip:** This bit will shadow the state of processor Thermal Trip status bit (CTS) (16.2.1.2, GEN_PMCON_2, bit 3). Events on signal will not create a event message
	7	Reserved: Default value is "X" Note: Software should not expect a consistent value when this bit is read through SMBUS/SMLINK
6	7:0	Contents of the Message 1 register. Refer to Section 13.9.8 for the description of this register.
7	7:0	Contents of the Message 2 register. Refer to Section 13.9.8 for the description of this register.
8	7:0	Contents of the TCO_WDCNT register. Refer to Section 13.9.9 for the description of this register.
9	7:0	Seconds of the RTC
A	7:0	Minutes of the RTC
B	7:0	Hours of the RTC
C	7:0	"Day of Week" of the RTC
D	7:0	"Day of Month" of the RTC
E	7:0	Month of the RTC
F	7:0	Year of the RTC
10h–FFh	7:0	Reserved

5.20.7.2.1 Behavioral Notes

According to SMBus protocol, Read and Write messages always begin with a Start bit – Address– Write bit sequence. When the ICH10 detects that the address matches the value in the Receive Slave Address register, it will assume that the protocol is always followed and ignore the Write bit (bit 9) and signal an Acknowledge during bit 10. In other words, if a Start –Address–Read occurs (which is invalid for SMBus Read or Write protocol), and the address matches the ICH10's Slave Address, the ICH10 will still grab the cycle.

Also according to SMBus protocol, a Read cycle contains a Repeated Start–Address–Read sequence beginning at bit 20. Once again, if the Address matches the ICH10's Receive Slave Address, it will assume that the protocol is followed, ignore bit 28, and proceed with the Slave Read cycle.

Note: An external microcontroller must not attempt to access the ICH10's SMBus Slave logic until at least 1 second after both RTCRST# and RSMRST# are deasserted (high).

5.20.7.3 Slave Read of RTC Time Bytes

The ICH10 SMBus slave interface allows external SMBus master to read the internal RTC's time byte registers.

The RTC time bytes are internally latched by the ICH10's hardware whenever RTC time is not changing and SMBus is idle. This ensures that the time byte delivered to the slave read is always valid and it does not change when the read is still in progress on the bus. The RTC time will change whenever hardware update is in progress, or there is a software write to the RTC time bytes.

The ICH10 SMBus slave interface only supports Byte Read operation. The external SMBus master will read the RTC time bytes one after another. It is software's responsibility to check and manage the possible time rollover when subsequent time bytes are read.

For example, assuming the RTC time is 11 hours: 59 minutes: 59 seconds. When the external SMBus master reads the hour as 11, then proceeds to read the minute, it is possible that the rollover happens between the reads and the minute is read as 0. This results in 11 hours: 0 minute instead of the correct time of 12 hours: 0 minutes. Unless it is certain that rollover will not occur, software is required to detect the possible time rollover by reading multiple times such that the read time bytes can be adjusted accordingly if needed.

5.20.7.4 Format of Host Notify Command

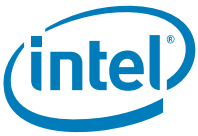
The ICH10 tracks and responds to the standard Host Notify command as specified in the *System Management Bus (SMBus) Specification,* Version 2.0. The host address for this command is fixed to 0001000b. If the ICH10 already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the HOST_NOTIFY_STS bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the HOST_NOTIFY_STS bit after completing any necessary reads of the address and data registers.

Table 5-56 shows the Host Notify format.

Table 5-56. Host Notify Format

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMB Host Address — 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	Intel® ICH10	ICH10 NACKs if HOST_NOTIFY_STS is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the Notify Device Address Register
18	Unused — Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	ICH10	
27:20	Data Byte Low — 8 bits	External Master	Loaded into the Notify Data Low Byte Register
28	ACK	ICH10	
36:29	Data Byte High — 8 bits	External Master	Loaded into the Notify Data High Byte Register
37	ACK	ICH10	
38	Stop	External Master	



5.21 Intel® High Definition Audio Overview

The ICH10's High Definition Audio (HDA) controller communicates with the external codec(s) over the Intel High Definition Audio serial link. The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The ICH10 implements four output DMA engines and 4 input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. ICH10 implements a single Serial Data Output signal (HDA_SDOUT) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The ICH10 implements four Serial Digital Input signals (HDA_SDI[3:0]) supporting up to four codecs.

Audio software renders outbound and processes inbound data to/from buffers in system memory. The location of individual buffers is described by a Buffer Descriptor List (BDL) that is fetched and processed by the controller. The data in the buffers is arranged in a predefined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bit/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the external codecs over the Intel High Definition Audio link. The input DMA engines receive data from the codecs over the Intel High Definition Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one stream of data. A single codec can accept or generate multiple streams of data, one for each A-D or D-A converter in the codec. Multiple codecs can accept the same output stream processed by a single DMA engine.

Codec commands and responses are also transported to and from the codecs using DMA engines.

5.22 Intel® Active Management Technology (Intel® AMT) (Corporate Only)

Intel Active Management Technology is a set of advanced manageability features developed as a direct result of IT customer feedback gained through Intel market research. Reducing the Total Cost of Ownership (TCO) through improved asset tracking, remote manageability, and fewer desk-side visits were identified as key IT priorities. Intel AMT extends the capabilities of existing management solutions by making the asset information, remote diagnostics, recovery and contain capabilities always available, or Out of Band (OOB), even when the system is in a low-power "off" state or the OS is hung.

Another feature of Intel AMT is System Defense. System Defense is used to stop the propagation of worms and viruses. Programmable packet filters in the integrated LAN Controller are used to accomplish this. These filters inspect all incoming and all outgoing packets and decide whether to block or pass the packets as configured. There is no indication to the host that a packet has been blocked or accepted.

The logic can be used to accept or block reception to host or transmission to network paths. Additionally, counter logic can be used to count the number or filter matches for a given filter. This feature allows for statistical sampling of connections as well as rate limiting of connections.

5.22.1 Intel® AMT Features

- E-Asset Tag
- OOB HW and SW Inventory Logs
- OOB Alerts
- IDE Redirect
- Serial over LAN for Remote Control
- Remote Diagnostics Execution
- OS Lock-Up Alert
- OS Repair
- Remote BIOS Recovery and Update

5.22.2 Intel® AMT Requirements

Intel AMT is a platform-level solution that utilizes multiple system components including:

- Intel AMT-Ready ICH10 SKU
- Intel Gigabit Ethernet PHY (Intel® 82567 Gigabit Platform LAN Connect device) with Intel Active Management Technology for remote access
- SPI flash memory with 4KB or 8KB sector erase that meets requirements set in Section 5.23.4 (32 Mb minimum for Intel AMT) to store asset information, management software code, and logs
- BIOS to provide asset detection and POST diagnostics (BIOS and Intel AMT can optionally share same flash memory device)
- Familiar ISV software packages to take advantage of Intel AMT's platform management capabilities

5.23 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a lower-cost alternative for system flash versus the Firmware Hub on the LPC bus.

The 4-pin SPI interface consists of clock (CLK), master data out (Master Out Slave In (MOSI)), master data in (Master In Slave Out (MISO)) and an active low chip select (SPI_CS[1:0]#).

The ICH10 supports up to two SPI flash devices using two separate Chip Select pins. Each SPI flash device can be up to 16 MBytes. The ICH10 SPI interface supports 20 MHz and 33 MHz SPI devices.

Communication on the SPI bus is done with a Master – Slave protocol. The Slave is connected to the ICH10 and is implemented as a tri-state bus.

Note: If option 11 LPC is selected BIOS may still be placed on LPC, but all platforms with ICH10 (Corporate Only) require SPI flash connected directly to the ICH's SPI bus with a valid descriptor in order to boot.

Note: When SPI is selected by the Boot BIOS Destination Strap and a SPI device is detected by the ICH10, LPC based BIOS flash is disabled.

5.23.1 SPI Supported Feature Overview

SPI Flash on the ICH10 has two operational modes, descriptor and non-descriptor.

5.23.1.1 Non-Descriptor Mode

Non-descriptor mode is similar to the flash functionality of ICH7. In this mode, SPI Flash can only be used for BIOS. Direct read and writes are not supported. BIOS has read/write access only through register accesses. Through those register accesses BIOS can read and write to the entire flash without security checking. There is also no support for the integrated Gigabit Ethernet, Intel Management Engine, chipset soft straps, as well multiple SPI Flash components.

5.23.1.2 Descriptor Mode

Descriptor Mode enables many new features of the chipset:

- Integrated Gigabit Ethernet and Host processor for Gigabit Ethernet Software
- Intel Active Management Technology
- Intel Quiet System Technology
- Supports two SPI Flash components using two separate chip select pins
- Hardware enforced security restricting master accesses to different regions
- Chipset Soft Strap region provides the ability to use Flash NVM as an alternative to hardware pull-up/pull-down resistors for both ICH and (G)MCH
- Supports the SPI Fast Read instruction and frequencies of 33 MHz
- Uses standardized Flash Instruction Set

5.23.1.2.1 SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions:

Region	Content
0	Flash Descriptor
1	BIOS
2	Intel Management Engine
3	Gigabit Ethernet
4	Platform Data

Only three masters can access the four regions: Host processor running BIOS code, Integrated Gigabit Ethernet and Host processor running Gigabit Ethernet Software, and Intel Management Engine. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of device 0 (offset 0).

Flash Region Sizes

SPI flash space requirements differ by platform and configuration. The Flash Descriptor requires one 4 KB or larger block. GbE requires two 4 KB or larger blocks. The Platform Data Region is 32 KB. The amount of flash space consumed is dependent on the erase granularity of the flash part and the platform requirements for the Intel ME and BIOS regions. The Intel ME region will contain firmware to support Intel Quiet System Technology, Intel Active Management Technology, ASF 2.0 and Intel Trusted Platform Module.

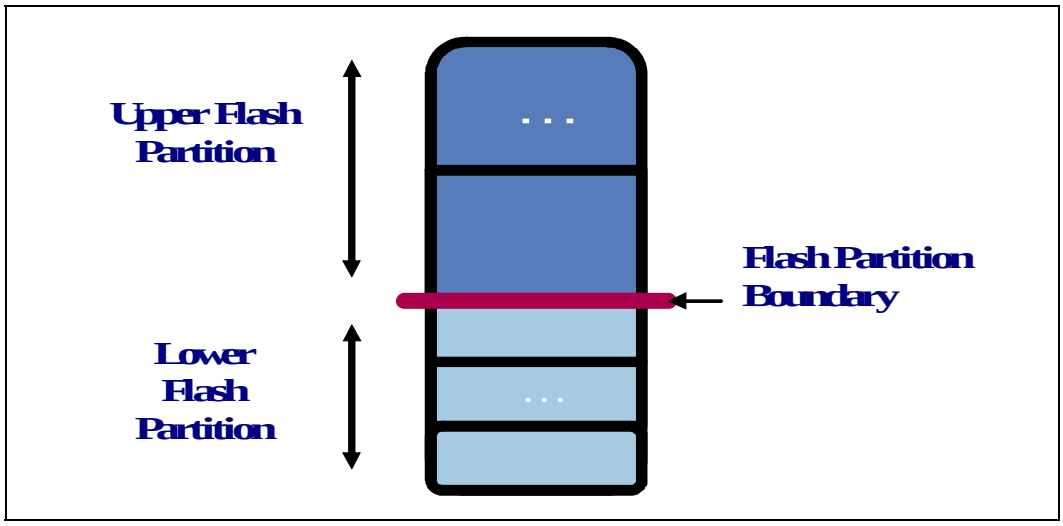
Table 5-57. Region Size versus Erase Granularity of Flash Components

Region	Size with 4 KB Blocks	Size with 64 KB Blocks
Descriptor	4 KB	64 KB
GbE	8 KB	128 KB
Platform Data Region	32 KB	**Not Supported**
BIOS	Varies by Platform	Varies by Platform
Intel ME	Varies by Platform	Varies by Platform

5.23.1.3 Device Partitioning

The ICH10 SPI Flash controller supports two sets of attributes in SPI flash space. This allows for supporting an asymmetric flash component that has two separate sets of attributes in the upper and lower part of the memory array. An example of this is a flash part that has different erase granularities in two different parts of the memory array. This allows for the usage of two separate flash vendors if using two different flash parts.

Figure 5-16. Flash Partition Boundary

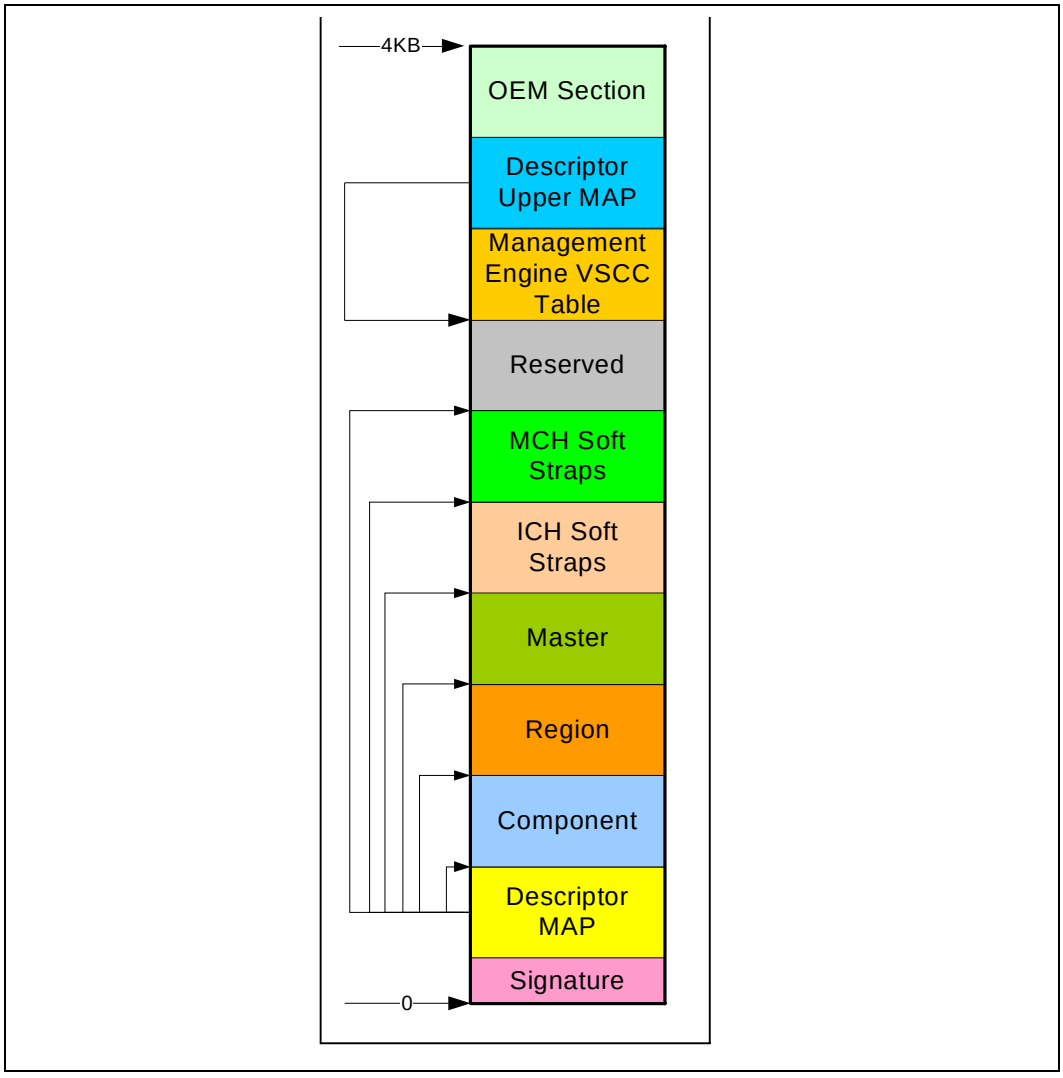


5.23.2 Flash Descriptor

The maximum size of the Flash Descriptor is 4 KB. If the block/sector size of the SPI flash device is greater than 4 KB, the flash descriptor will only use the first 4 KB of the first block. The flash descriptor requires its own block at the bottom of memory (0x00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read only when the computer leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections:

Figure 5-17. Flash Descriptor Sections



1. The Flash signature selects Descriptor Mode as well as verifies if the flash is programmed and functioning. The data at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
2. The Descriptor map has pointers to the other five descriptor sections as well as the size of each.

3. The component section has information about the SPI flash in the system including: the number of components, density of each, invalid instructions (such as chip erase), and frequencies for read, fast read and write/erase instructions.
4. The Region section points to the three other regions as well as the size of each region.
5. The master region contains the security settings for the flash, granting read/write permissions for each region and identifying each master by a requestor ID. See Section 5.23.2.1 for more information.

6 & 7. The (G)MCH and ICH chipset soft strap sections contain (G)MCH and ICH configurable parameters.

8. The Reserved region between the top of the (G)MCH strap section and the bottom of the OEM Section is reserved for future chipset usages.
9. The Descriptor Upper MAP determines the length and base address of the Intel Management Engine VSCC Table.
10. The Intel Management Engine VSCC Table holds the JEDEC ID and the VSCC information of the entire SPI Flash supported by the NVM image.
11. OEM Section is 256 Bytes reserved at the top of the Flash Descriptor for use by OEM.

5.23.2.1 Descriptor Master Region

The master region defines read and write access setting for each region of the SPI device. The master region recognizes three masters: BIOS, Gigabit Ethernet, and Intel Management Engine. Each master is only allowed to do direct reads of its primary regions.

Table 5-58. Region Access Control Table

Master Read/Write Access			
Region	**CPU and BIOS**	**Intel ME/(G)MCH**	**GbE Controller**
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Intel Management Engine	Read / Write	Intel ME can always read from and write to Intel ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

5.23.3 Flash Access

There are two types of flash accesses:

Direct Access:

- Masters are allowed to do direct read only of their primary region
  - Gigabit Ethernet region can only be directly accessed by the Gigabit Ethernet controller. Gigabit Ethernet software must use Program Registers to access the Gigabit Ethernet region.
- Master's Host or Intel Management Engine virtual read address is converted into the SPI Flash Linear Address (FLA) using the Flash Descriptor Region Base/Limit registers

Program Register Access:

- Program Register Accesses are not allowed to cross a 4 KB boundary and can not issue a command that might extend across two components
- Software programs the FLA corresponding to the region desired
  - Software must read the devices Primary Region Base/Limit address to create a FLA.

5.23.3.1 Direct Access Security

- Requester ID of the device must match that of the primary Requester ID in the Master Section
- Calculated Flash Linear Address must fall between primary region base/limit
- Direct Write not allowed
- Direct Read Cache contents are reset to 0s on a read from a different master
  - Supports the same cache flush mechanism in the ICH7, which includes Program Register Writes

5.23.3.2 Register Access Security

- Only primary region masters can access the registers

Note: Processor running Gigabit Ethernet software can access Gigabit Ethernet registers

- Masters are only allowed to read or write those regions they have read/write permission
- Using the Flash Region Access Permissions, one master can give another master read/write permissions to their area
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses
  - Example: BIOS may want to protect different regions of BIOS from being erased
  - Ranges can extend across region boundaries

5.23.4 Serial Flash Device Compatibility Requirements

A variety of serial flash devices exist in the market. For a serial flash device to be compatible with the Intel ICH10 SPI bus, it must meet the minimum requirements detailed in the following sections.

5.23.4.1 Intel® ICH10 SPI Based BIOS Requirements

A serial flash device must meet the following minimum requirements when used explicitly for system BIOS storage.

- Erase size capability of at least one of the following: 64 KB, 8 KB, 4 KB, or 256 bytes.
- Device must support multiple writes to a page without requiring a preceding erase cycle (Refer to Section 5.23.5)
- Serial flash device must ignore the upper address bits such that an address of FFFFFFh aliases to the top of the flash memory.
- SPI Compatible Mode 0 support (clock phase is 0 and data is latched on the rising edge of the clock).
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must complete the cycle gracefully without any impact on the flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, etc.) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command mst automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- Hardware Sequencing requirements are optional in BIOS only platforms.
- SPI flash parts that do not meet Hardware sequencing command set requirements may work in BIOS only platforms via software sequencing.

5.23.4.2 Integrated LAN Firmware SPI Flash Requirements

A serial flash device that will be used for system BIOS and Integrated LAN or Integrated LAN only must meet all the SPI Based BIOS Requirements plus:

- Hardware sequencing
- 4, 8 or 64 KBytes erase capability must be supported.

5.23.4.2.1 SPI Flash Unlocking Requirements for Integrated LAN

BIOS must ensure there is no SPI flash based read/write/erase protection on the GbE region. GbE firmware and drivers for the integrated LAN need to be able to read, write and erase the GbE region at all times.

5.23.4.3 Intel® Management Engine Firmware SPI Flash Requirements

Intel Management Engine Firmware must meet the SPI flash based BIOS Requirements plus:

- Hardware Sequencing.
- Flash part must be uniform 4 KB erasable block throughout the entire device.
- Write protection scheme must meet SPI flash unlocking requirements for Intel Management Engine.

5.23.4.3.1 SPI Flash Unlocking Requirements for Intel Management Engine

Flash devices must be globally unlocked (read, write and erase access on the Intel ME region) from power on by writing 00h to the flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire part. If the SPI flash's status register has non-volatile bits that must be written to, bits [5:2] of the flash's status register must be all 0h to indicate that the flash is unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, BIOS has the ability to lock down small sections of the flash as long as they do not involve the Intel ME or GbE region.

5.23.4.4 Hardware Sequencing Requirements

Table 5-59 contains a list of commands and the associated opcodes that a SPI-based serial flash device must support in order to be compatible with hardware sequencing.

Table 5-59. Hardware Sequencing Commands and Opcode Requirements

Commands	Opcode	Notes
Write to Status Register	01h	Writes a byte to SPI flash's status register. Enable Write to Status Register command must be run prior to this command.
Program Data	02h	Single byte or 64 byte write as determined by flash part capabilities and software.
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of SPI flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	50h or 60h	Enables a bit in the status register to allow an update to the status register
Erase	Program mable	256B, 4 Kbyte, 8 Kbyte or 64 Kbyte
Full Chip Erase	C7h	
JEDEC ID	9Fh	See Section .

5.23.4.4.1 JEDEC ID

Since each serial flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV.

5.23.5 Multiple Page Write Usage Model

The system BIOS and Intel Active Management Technology firmware usage models require that the serial flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Intel AMT firmware usage model requires the capability for multiple data updates within any given page. These data updates occur via byte-writes without executing a preceding erase to the given page. Both the BIOS and Intel AMT firmware multiple page write usage models apply to sequential and non-sequential data writes.

Note: This usage model requirement is based on any given bit only being written once from a 1-to-0 without requiring the preceding erase. An erase would be required to change bits back to the 1 state.

5.23.5.1 Soft Flash Protection

There are two types of flash protection that are not defined in the flash descriptor supported by ICH10:

1. BIOS Range Write Protection
2. SMI#-Based Global Write Protection

Both mechanisms are logically OR'd together such that if any of the mechanisms indicate that the access should be blocked, then it is blocked. Table 5-60 provides a summary of the mechanisms.

Table 5-60. Flash Protection Mechanism Summary

Mechanism	Accesses Blocked	Range Specific?	Reset-Override or SMI#-Override?	Equivalent Function on FWH
BIOS Range Write Protection	Writes	Yes	Reset Override	FWH Sector Protection
Write Protect	Writes	No	SMI# Override	Same as Write Protect in previous ICHs for FWH

A blocked command will appear to software to finish, except that the Blocked Access status bit is set in this case.

5.23.5.2 BIOS Range Write Protection

The ICH10 provides a method for blocking writes to specific ranges in the SPI flash when the Protected BIOS Ranges are enabled. This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) and the address of the requested command against the base and limit fields of a Write Protected BIOS range.

Note: Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

5.23.5.3 SMI# Based Global Write Protection

The ICH provides a method for blocking writes to the SPI flash when the Write Protected bit is cleared (i.e., protected). This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) of the requested command.

The Write Protect and Lock Enable bits interact in the same manner for SPI BIOS as they do for the FWH BIOS.

5.23.6 Flash Device Configurations

The ICH10-based platform may use the serial flash in multiple configurations. The following table focuses on the supported configurations involving the ICH10 and Intel Active Management Technology.

Configuration	System BIOS Storage	Intel® ICH10 Firmware	Minimum Number of SPI Device(s)
1	SPI	No	1
2	Non-SPI	Yes	1
3	SPI	Yes	1
4	Non-SPI	No	0

Note: When SPI is selected for BIOS and a SPI device is detected by the ICH10, LPC based BIOS flash is disabled.

Note: Firmware includes Intel Active Management Technology, ASF, Intel Quiet System Technology and Gigabit Ethernet.

5.23.7 SPI Flash Device Recommended Pinout

The table below contains the recommended serial flash device pin-out for an 8-pin device. Use of the recommended pin-out on an 8-pin device reduces complexities involved with designing the serial flash device onto a motherboard and allows for support of a common footprint usage model (refer to Section 5.23.8.1).

Table 5-61. Recommended Pinout for 8-Pin Serial Flash Device

Pin #	Signal
1	Chips Select
2	Data Output
3	Write Protect
4	Ground
5	Data Input
6	Serial Clock
7	Hold / Reset
8	Supply Voltage

Although an 8-pin device is preferred over a 16-pin device due to footprint compatibility, the following table contains the recommended serial flash device pin-out for a 16-pin SOIC.

5.23.8 Serial Flash Device Package

Table 5-62. Recommended Pinout for 16-Pin Serial Flash Device

Pin #	Signal	Pin #	Signal
1	Hold / Reset	9	Write Protect
2	Supply Voltage	10	Ground
3	No Connect	11	No Connect
4	No Connect	12	No Connect
5	No Connect	13	No Connect
6	No Connect	14	No Connect
7	Chip Select	15	Serial Data In
8	Serial Data Out	16	Serial Clock

5.23.8.1 Common Footprint Usage Model

To minimize platform motherboard redesign and to enable platform Bill of Material (BOM) selectability, many PC System OEM's design their motherboard with a single common footprint. This common footprint allows population of a soldered down device or a socket that accepts a leadless device. This enables the board manufacturer to support, via selection of the appropriate BOM, either of these solutions on the same system without requiring any board redesign.

The common footprint usage model is desirable during system debug and by flash content developers since the leadless device can be easily removed and reprogrammed without damage to device leads. When the board and flash content is mature for high-volume production, both the socketed leadless solution and the soldered down leaded solution are available through BOM selection.

5.23.8.2 Serial Flash Device Package Recommendations

It is highly recommended that the common footprint usage model be supported. An example of how this can be accomplished is as follows:

- The recommended pinout for 8-pin serial flash devices is used (refer to Section 5.23.7).
- The 8-pin device is supported in either an 8-contact VDFPN (6x5 mm MLP) package or an 8-contact WSON (5x6 mm) package. These packages can fit into a socket that is land pattern compatible with the wide body SO8 package.
- The 8-pin device is supported in the SO8 (150 mil) and in the wide-body SO8 (200 mil) packages.

The 16-pin device is supported in the SO16 (300 mil) package.

5.24 Intel® Quiet System Technology (Intel® QST)

The ICH10 implements three PWM and 4 TACH signals for Intel Quiet System Technology (QST).

Note: Intel Quiet System Technology functionality requires a correctly configured system, including an appropriate (G)MCH with Intel ME, Intel ME Firmware, and system BIOS support.

5.24.1 PWM Outputs

This signal is driven as open-drain. An external pull-up resistor is integrated into the fan to provide the rising edge of the PWM output signal. The PWM output is driven low during reset, which represents 0% duty cycle to the fans. After reset de-assertion, the PWM output will continue to be driven low until one of the following occurs:

- The internal PWM control register is programmed to a non-zero value by the Intel QST firmware.
- The watchdog timer expires (enabled and set at 4 seconds by default).
- The polarity of the signal is inverted by the Intel QST firmware.

Note that if a PWM output will be programmed to inverted polarity for a particular fan, then the low voltage driven during reset represents 100% duty cycle to the fan.

5.24.2 TACH Inputs

This signal is driven as an open-collector or open-drain output from the fan. An external pull-up is expected to be implemented on the motherboard to provide the rising edge of the TACH input. This signal has analog hysteresis and digital filtering due to the potentially slow rise and fall times. This signal has a weak internal pull-up resistor to keep the input buffer from floating if the TACH input is not connected to a fan.

5.25 Thermal Sensors

ICH10 integrates two thermal sensors that monitor the temperature within its die. The thermal sensors are used for Intel Quiet System Technology (Intel QST). The Intel QST firmware can internally access the temperature measured by the sensors and use the data as a factor to determine how to control the fans.

The ICH10 thermal sensors also provide the capability to protect the ICH10 under a catastrophic thermal situation. When the sensors are enabled and correctly programmed by the system BIOS, the ICH10 will shut down the system when the ICH10 thermal limit is reached. Refer to the Thermal Memory Mapped Configuration Registers Section 23.2 for more info on the catastrophic settings.

5.26 Feature Capability Mechanism

A set of registers is included in the ICH10 LPC Interface (Device 31, Function 0, offset E0h - EBh) that allows the system software or BIOS to easily determine the features supported by ICH10. These registers can be accessed through LPC PCI configuration space, thus allowing for convenient single point access mechanism for chipset feature detection.

This set of registers consists of:
Capability ID (FDCAP)
Capability Length (FDLEN)
Capability Version and Vendor-Specific Capability ID (FDVER)
Feature Vector (FVECT)

5.27 Integrated Trusted Platform Module (Corporate Only)

The integrated Trusted Platform Module (TPM) implementation consists of firmware, Intel Management Engine resources and dedicated hardware within the ICH and the (G)MCH. The integrated TPM supports all requirements of the TPM Specification Version 1.2, Level 2 Revision 103, as published by the Trusted Computing Group.

Note: Integrated TPM functionality requires a correctly configured system, including an appropriate (G)MCH with Intel Management Engine firmware, ICH10 and SPI Flash.

5.27.1 Integrated TPM Hardware Requirements

The following hardware components are required for TPM 1.2 functionality:

1. SPI Flash Memory: The SPI flash component connected to the ICH (SPI interface) provides non-volatile storage requirement for the integrated TPM. It contains the FW code which is loaded by the Intel Management Engine upon power on.
2. Monotonic Counters: The ICH10 contains four TPM 1.2 compliant monotonic counters that reside in the RTC well which maintains values programmed by the integrated TPM across power cycles. The counters are only incremented by TPM software (host or Intel ME) and are not controlled by the ICH hardware.
3. Physical Presence: Physical presence indication is required in order to enable certain TPM commands. These commands are generally used to bypass owner authorized commands when the authorization data is unavailable or to set the integrated TPM to a non-owner state. The Intel Management Engine Firmware uses the TPM_PP pin on the ICH10 to indicate Physical Presence to the platform when pulled high. In addition, Physical Presence flags can be set to force Physical Presence by firmware.
4. Chipset: An ICH10 and (G)MCH with Intel Management Engine enabled is required for integrated TPM support.

5.27.2 Enabling integrated TPM

The integrated TPM is enabled based on the combination of a functional straps on both the ICH and the (G)MCH and a soft strap bit found in the SPI Descriptor. When the integrated TPM is enabled, Front Side Bus cycles that would otherwise propagate to the LPC bus will be routed by the Config Bus Decoder to the integrated TPM Host Decoder. Either Functional strap or the soft strap bit may be used to disable the integrated TPM.

- **ICH Functional Strap**: The ICH10 enables Integrated TPM when SPI_MOSI is sampled high on the rising edge of CLPWROK and disabled if the SPI_MOSI signal is sampled low. See Section 2.25.1 for details. The SPI_MOSI signal requires an external pull-up resistor to enable the integrated TPM. SPI_MOSI has an integrated pull-down resistor enabled at reset only and does not require an external pull-down resistor to disable integrated TPM.
- **Soft Strap**: The integrated TPM Disable bit (bit 2) in the (G)MCHSTRP0 register (FSMBA + 0h) within the flash descriptor can act as an override to the functional straps on both the ICH and (G)MCH. When set, the integrated TPM will be disabled regardless of the values of the functional straps on the ICH and/or (G)MCH. This bit along with both functional straps must be appropriately configured to enable integrated TPM.
- **(G)MCH Functional Strap:** For (G)MCH functional strap information, consult the appropriate (G)MCH documentation.

§ §

6 Ballout Definition

This chapter contains the Intel® ICH10 ballout information.

6.1 Intel® ICH10 Ballout

This section contains the ICH10 ballout. Figure 6-1 and Figure 6-2 show the ballout from a top of the package view. Table 6-1 is the BGA ball list, sorted alphabetically by signal name.

Note: Notes for Figure 6-1, Figure 6-2, and Table 6-1

1. § symbol indicates a particular use of a pin is Cunsumer Only.
2. † symbol indicates a particular use of a pin is Corporate Only.

Figure 6-1. Intel® ICH10 Ballout (Top view–Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	Vss	Vcc3_3	PIRQD#	AD11	AD4	V5REF	GNT1# / GPIO51	GPIO12	GPIO14 / JTAGDI† / QST_BMBUSY#§	VccLAN1_1	GPIO27	VccLAN3_3	SLP_S3#	GPIO24 / MEM_LED	SMLINK0	A
B	Vcc3_3	Vss	PCICLK	AD9	Vss	AD8	AD7	Vss	Vcc3_3	VccLAN1_1	Vss	VccLAN3_3	SLP_S4#	Vss	SMLINK1	B
C	AD24	AD25	AD26	C/BE2#	AD14	DEVSEL#	GNT2# / GPIO53	AD1	AD3	AD0	S4_STATE# / GPIO26	GPIO57 / TPM_PP / JTAGTCK†	GPIO72† / TP0	PLTRST#	STP_PCI# / GPIO15	C
D	AD27	AD15	AD21													D
E	PIRQB#	Vss	PAR		AD16	TRDY#	AD10	C/BE3#	AD2	AD6	AD18	AD5	LAN_RXD2	LAN_RSTSYNC	Vss	E
F	PIRQC#	PIRQG# / GPIO4	AD29		PERR#	Vss	GNT3# / GPIO55	AD13	Vss	STOP#	C/BE0#	Vss	REQ2# / GPIO52	LAN_TXD1	LAN_TXD0	F
G	AD30	PIRQH# / GPIO5	Vcc3_3		AD23	AD20	AD17	REQ3# / GPIO54	C/BE1#	AD19	Vcc3_3	FRAME#	REQ1# / GPIO50	LAN_TXD2	LAN_RXD0	G
H	FWH1 / LAD1	Vss	AD31		GNT0#	AD22	Vcc3_3	PLOCK#	Vss	Vcc1_5_A	Vcc1_5_A	AD12	Vss	LAN_RXD1	VccSus3_3	H
J	FWH3 / LAD3	Vcc3_3	LDRQ1# / GPIO23		PIRQA#	Vss	AD28	IRDY#								J
K	GPIO18	GPIO32	FWH0 / LAD0		SERR#	PIRQE# / GPIO2	REQ0#	Vcc3_3								K
L	SATACLKREQ# / GPIO35	Vss	RCIN#		FWH4 / LFRAME#	LDRQ0#	PIRQF# / GPIO3	Vcc3_3								L
M	OC7# / GPIO31	GPIO16 / DPRSLPVR	INIT3_3V#		CLK14	Vss	FWH2 / LAD2	Vss				Vcc1_1	Vcc1_1	Vss	Vcc1_1	M
N	OC5# / GPIO29	OC4# / GPIO43	OC1# / GPIO40		OC6# / GPIO30	SERIRQ	GPIO0 / BMBUSY#	SPKR				Vcc1_1	Vss	Vss	Vss	N
P	OC11# / GPIO47	Vss	OC8# / GPIO44		OC0# / GPIO59	Vss	OC2# / GPIO41	A20GATE				Vss	Vss	Vss	Vss	P
R	SUS_STAT# / LPCPD / GPIO61†	PCIRST#	PME#		SUSCLK / GPIO62†	OC9# / GPIO45	OC3# / GPIO42	Vss				Vcc1_1	Vss	Vss	Vss	R
T	Vcc1_5_A	Vss	PWRBTN#		Vss	CLPWROK	OC10# / GPIO46	CK_PWRGD				Vss	Vss	Vss	Vss	T
U	VccSus3_3	VccSus3_3	VccSus3_3		VccSus3_3	VccSus3_3	VccSus3_3	VccSus3_3				Vcc1_1	Vss	Vss	Vss	U
V	USBP11N	USBP11P	Vss		USBP9P	USBP9N	Vss	VccSus3_3				Vcc1_1	Vss	Vss	Vss	V
W	Vss	USBP10N	USBP10P		Vss	Vss	VccSus3_3	VccSus3_3				Vcc1_1	Vcc1_1	Vss	Vcc1_1	W
Y	USBP8N	USBP8P	Vss		USBP6P	USBP6N	Vss	VccSus3_3								Y
AA	Vss	USBP7P	USBP7N		Vss	Vss	Vcc1_5_A	Vcc1_5_A								AA
AB	USBP5N	USBP5P	Vss		USBP3P	USBP3N	Vcc1_5_A	Vcc1_5_A								AB
AC	Vss	USBP4P	USBP4N		Vss	Vss	VccSus1_1	Vss	VccSusHDA	VccHDA	Vcc1_5_A	Vss	Vcc1_5_A	Vcc1_5_A	Vcc1_5_A	AC
AD	USBP2N	USBP2P	Vss		USBP0P	USBP0N	Vss	VccSus1_5	Vss	Vcc3_3	Vcc1_5_A	Vcc1_5_A	Vcc1_5_A	Vss	Vss	AD
AE	Vss	USBP1P	USBP1N		Vss	Vss	SATALED#	Vss	Vss	Vss	Vcc1_5_A	Vss	Vss	Vss	Vss	AE
AF	V5REF_Sus	VccSus3_3	Vss		GPIO20	GPIO33	Vss	SATA5TXN	Vss	SATA4TXN	Vcc1_5_A	SATA3TXN	Vss	SATA2TXP	Vss	AF
AG	USBRBIAS#	USBRBIAS	CLK48													AG
AH	HDA_SDIN2	Vss	HDA_BIT_CLK	HDA_SDIN1	GPIO34	Vss	SATA5TXP	Vss	SATA4TXP	Vcc1_5_A	Vcc1_5_A	SATA3TXP	Vss	SATA2TXN	Vss	AH
AJ	HDA_RST#	HDA_SDOUT	HDA_SDIN3	Vss	Vss	SATARBIAS	SATA5RXN	Vss	SATA4RXN	Vcc1_5_A	SATA3RXN	Vss	SATA2RXN	Vss	SATA1RXN	AJ
AK	HDA_SYNC	Vss	HDA_SDIN0	Vcc3_3	VccUSBPLL	SATARBIAS#	SATA5RXP	Vss	SATA4RXP	Vcc1_5_A	SATA3RXP	Vss	SATA2RXP	Vss	SATA1RXP	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 6-2. Intel® ICH10 Ballout (Top view–Right Side)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
A	TP6	VccSus3_3	GPIO9	GPIO13	DRAMPWROK† / GPIO8	RTCX1	VccRTC	VccCL1_1	Vcc1_1	RTCRST#	VccCL1_5	VccGLAN3_3	VccGLANPLL	GLAN_COMPO	Vss	A
B	TP7	Vss	STP_CPU# / GPIO25†	Vss	VccSus3_3	RTCX2	Vss	VccCL3_3	Vcc1_1	Vss	SPI_MISO	Vss	Vss	GLAN_COMPI	VccGLAN1_5	B
C	SMBALERT# / GPIO11 / JTAGTDO†	GPIO10 / CPU_MISSING / JTAGTMS†	TP5	SST	VccSus3_3	LAN_RST#	VRMPWRGD	VccCL3_3	Vcc1_1	PWROK	SPI_MOSI	CL_VREF0	VccGLAN1_5	VccGLAN1_5	VccGLAN1_5	C
D													Vss	PERn6 / GLAN_RXN	PERp6 / GLAN_RXP	D
E	SMBDATA	VccSus3_3	Vss	TP4	WAKE#	LAN100_SLP	Vss	INTVRMEN	Vcc1_1	SPI_CS0#	PETn6 / GLAN_TXN		PETp6 / GLAN_TXP	Vss	Vss	E
F	GPIO56	SLP_M#	LINKALERT# / GPIO60 / JTAGRST#†	SYS_RESET#	TP3	Vss	RSMRST#	SPI_CS1#	Vcc1_1	GLAN_CLK	Vss		Vss	PERp5	PERn5	F
G	Vss	SLP_S5# / GPIO63†	GPIO28	RI#	CL_RST0#	INTRUDER#	CL_CLK0	SPI_CLK	Vcc1_1	Vss	PETn5		PETp5	Vss	Vss	G
H	SMBCLK	VccSus1_1	VccSus1_5	Vss	SRTCRST#	CL_DATA0	Vss	Vcc1_1	Vcc1_1	Vss	Vss		Vss	PERp4	PERn4	H
J								Vcc1_1	Vcc1_5_B	Vcc1_5_B	PETn4		PETp4	Vss	Vss	J
K								Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vss		Vss	PERp3	PERn3	K
L								Vss	Vcc1_5_B	Vcc1_5_B	PETn3		PETp3	Vss	Vss	L
M	Vss	Vcc1_1	Vcc1_1	Vcc1_1				Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vss		Vss	PERp2	PERn2	M
N	Vss	Vss	Vss	Vcc1_1				Vss	Vcc1_5_B	Vcc1_5_B	PETn2		PETp2	Vss	Vss	N
P	Vss	Vss	Vss	Vss				Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vss		Vss	PERp1	PERn1	P
R	Vss	Vss	Vss	Vcc1_1				Vss	Vcc1_5_B	Vcc1_5_B	PETn1		PETp1	Vss	Vss	R
T	Vss	Vss	Vss	Vss				Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vcc1_5_B		Vcc1_5_B	Vss	VccDMIPLL	T
U	Vss	Vss	Vss	Vcc1_1				Vss	Vcc1_5_B	DMI_CLKP	DMI_CLKN		Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	U
V	Vss	Vss	Vss	Vcc1_1				Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vss		Vss	DMI0TXP	DMI0TXN	V
W	Vss	Vcc1_1	Vcc1_1	Vcc1_1				Vss	Vcc1_5_B	Vcc1_5_B	DMI0RXP		DMI0RXN	Vss	Vss	W
Y								Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	Vss		Vss	DMI1TXP	DMI1TXN	Y
AA								Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	DMI1RXN		DMI1RXP	Vss	Vss	AA
AB								Vcc1_5_A	Vcc1_5_B	Vcc1_5_B	Vss		Vss	DMI2TXP	DMI2TXN	AB
AC	Vcc1_5_A	Vcc1_5_A	Vcc1_5_A	Vcc3_3	Vcc1_5_A	Vcc3_3	IGNNE#	PECI	Vss	Vcc1_5_B	DMI2RXN		DMI2RXP	Vss	Vss	AC
AD	Vss	Vcc1_5_A	Vss	Vss	SDATAOUT1 / GPIO48	SATA5GP	Vss	CPUPWRGD	THRMTRIP#	Vcc1_5_B	Vcc1_5_B		Vcc1_5_B	DMI3TXN	DMI3TXP	AD
AE	Vss	Vcc1_5_A	Vss	Vss	SATA1GP / GPIO19	SATA2GP / GPIO36	SATA3GP / GPIO37	INIT#	DPSLP#	Vss	DMI3RXP		Vcc1_5_B	Vcc1_5_B	Vcc1_5_B	AE
AF	SATA1TXP	Vcc1_5_A	SATA_CLKN	SATA_CLKP	Vss	Vcc3_3	SATA4GP	Vss	NMI	Vss	DMI3RXN		DMI_IRCOMP	Vss	DMI_ZCOMP	AF
AG													Vss	VccDMI	VccDMI	AG
AH	SATA1TXN	Vcc1_5_A	Vcc1_5_A	Vss	Vss	TACH0 / GPIO17	TACH2 / GPIO6	SDATAOUT0 / GPIO39	Vcc3_3	MCH_SYNC#	SMI#	INTR	V_CPU_IO	Vss	Vcc3_3	AH
AJ	Vss	SATA0RXP	Vcc1_5_A	SATA0TXP	Vss	PWM0	PWM1	Vss	SCLOCK / GPIO22	GPIO49	Vss	FERR#	A20M#	STPCLK#	V_CPU_IO	AJ
AK	Vss	SATA0RXN	Vcc1_5_A	SATA0TXN	VccSATAPLL	TACH1 / GPIO1	PWM2	TACH3 / GPIO7	SLOAD / GPIO38	SATA0GP / GPIO21	THRM#	Vss	DPRSTP#	Vss	Vss	AK
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
A20GATE	P8
A20M#	AJ28
AD0	C10
AD1	C8
AD2	E9
AD3	C9
AD4	A5
AD5	E12
AD6	E10
AD7	B7
AD8	B6
AD9	B4
AD10	E7
AD11	A4
AD12	H12
AD13	F8
AD14	C5
AD15	D2
AD16	E5
AD17	G7
AD18	E11
AD19	G10
AD20	G6
AD21	D3
AD22	H6
AD23	G5
AD24	C1
AD25	C2
AD26	C3
AD27	D1
AD28	J7
AD29	F3
AD30	G1
AD31	H3
C/BE0#	F11
C/BE1#	G9
C/BE2#	C4
C/BE3#	E8
CK_PWRGD	T8

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
CL_CLK0	G22
CL_DATA0	H21
CL_RST0#	G20
CL_VREF0	C27
CLK14	M5
CLK48	AG3
CLPWROK	T6
CPUPWRGD	AD23
DEVSEL#	C6
DMI_CLKN	U26
DMI_CLKP	U25
DMI_IRCOMP	AF28
DMI_ZCOMP	AF30
DMI0RXN	W28
DMI0RXP	W26
DMI0TXN	V30
DMI0TXP	V29
DMI1RXN	AA26
DMI1RXP	AA28
DMI1TXN	Y30
DMI1TXP	Y29
DMI2RXN	AC26
DMI2RXP	AC28
DMI2TXN	AB30
DMI2TXP	AB29
DMI3RXN	AF26
DMI3RXP	AE26
DMI3TXN	AD29
DMI3TXP	AD30
DRAMPWROK† / GPIO8	A20
FERR#	AJ27
FRAME#	G12
FWH0 / LAD0	K3
FWH1 / LAD1	H1
FWH2 / LAD2	M7
FWH3 / LAD3	J1
FWH4 / LFRAME#	L5
GLAN_CLK	F25

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
GLAN_COMPI	B29
GLAN_COMPO	A29
GNT0#	H5
GNT1# / GPIO51	A7
GNT2# / GPIO53	C7
GNT3# / GPIO55	F7
GPIO0	N7
GPIO10 / CPU_MISSING / JTAGTMS†	C17
GPIO12	A8
GPIO13	A19
GPIO14 / JTAGTDI† / QST_BMBUSY#§	A9
GPIO16 / DPRSLPVR	M2
GPIO18	K1
GPIO20	AF5
GPIO24	A14
GPIO27	A11
GPIO28	G18
GPIO32	K2
GPIO33	AF6
GPIO34	AH5
GPIO49	AJ25
GPIO56	F16
GPIO57 / TPM_PP / JTAGTCK†	C12
GPIO72† / TP0	C13
GPIO9	A18
HDA_BIT_CLK	AH3
HDA_RST#	AJ1
HDA_SDIN0	AK3
HDA_SDIN1	AH4
HDA_SDIN2	AH1
HDA_SDIN3	AJ3
HDA_SDOUT	AJ2
HDA_SYNC	AK1
IGNNE#	AC22
INIT#	AE23
INIT3_3V#	M3

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
INTR	AH27
INTRUDER#	G21
INTVRMEN	E23
IRDY#	J8
LAN_RST#	C21
LAN_RSTSYNC	E14
LAN_RXD0	G15
LAN_RXD1	H14
LAN_RXD2	E13
LAN_TXD0	F15
LAN_TXD1	F14
LAN_TXD2	G14
LAN100_SLP	E21
LDRQ0#	L6
LDRQ1# / GPIO23	J3
LINKALERT# / GPIO60 / JTAGRST#†	F18
MCH_SYNC#	AH25
NMI	AF24
OC0# / GPIO59	P5
OC1# / GPIO40	N3
OC2# / GPIO41	P7
OC3# / GPIO42	R7
OC4# / GPIO43	N2
OC5# / GPIO29	N1
OC6# / GPIO30	N5
OC7# / GPIO31	M1
OC8# / GPIO44	P3
OC9# / GPIO45	R6
OC10# / GPIO46	T7
OC11# / GPIO47	P1
PAR	E3
PCICLK	B3
PCIRST#	R2
PECI	AC23
PERn1	P30
PERn2	M30
PERn3	K30
PERn4	H30

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
PERn5	F30
PERn6 / GLAN_RXN	D29
PERp1	P29
PERp2	M29
PERp3	K29
PERp4	H29
PERp5	F29
PERp6 / GLAN_RXP	D30
PERR#	F5
PETn1	R26
PETn2	N26
PETn3	L26
PETn4	J26
PETn5	G26
PETn6 / GLAN_TXN	E26
PETp1	R28
PETp2	N28
PETp3	L28
PETp4	J28
PETp5	G28
PETp6 / GLAN_TXP	E28
PIRQA#	J5
PIRQB#	E1
PIRQC#	F1
PIRQD#	A3
PIRQE# / GPIO2	K6
PIRQF# / GPIO3	L7
PIRQG# / GPIO4	F2
PIRQH# / GPIO5	G2
PLOCK#	H8
PLTRST#	C14
PME#	R3
PWM0	AJ21
PWM1	AJ22
PWM2	AK22
PWRBTN#	T3
PWROK	C25
RCIN#	L3
REQ0#	K7

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
REQ1# / GPIO50	G13
REQ2# / GPIO52	F13
REQ3# / GPIO54	G8
RI#	G19
RSMRST#	F22
RTCRST#	A25
RTCX1	A21
RTCX2	B21
S4_STATE# / GPIO26	C11
SATA_CLKN	AF18
SATA_CLKP	AF19
SATA0GP / GPIO21	AK25
SATA0RXN	AK17
SATA0RXP	AJ17
SATA0TXN	AK19
SATA0TXP	AJ19
SATA1GP / GPIO19	AE20
SATA1RXN	AJ15
SATA1RXP	AK15
SATA1TXN	AH16
SATA1TXP	AF16
SATA2GP / GPIO36	AE21
SATA2RXN	AJ13
SATA2RXP	AK13
SATA2TXN	AH14
SATA2TXP	AF14
SATA3GP / GPIO37	AE22
SATA3RXN	AJ11
SATA3RXP	AK11
SATA3TXN	AF12
SATA3TXP	AH12
SATA4GP	AF22
SATA4RXN	AJ9
SATA4RXP	AK9
SATA4TXN	AF10
SATA4TXP	AH9
SATA5GP	AD21
SATA5RXN	AJ7

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
SATA5RXP	AK7
SATA5TXN	AF8
SATA5TXP	AH7
SATACLKREQ# / GPIO35	L1
SATALED#	AE7
SATARBIAS	AJ6
SATARBIAS#	AK6
SCLOCK / GPIO22	AJ24
SDATAOUT0 / GPIO39	AH23
SDATAOUT1 / GPIO48	AD20
SERIRQ	N6
SERR#	K5
SLOAD / GPIO38	AK24
SLP_M#	F17
SLP_S3#	A13
SLP_S4#	B13
SLP_S5# / GPIO63†	G17
SMBALERT# / GPIO11 / JTAGTDO†	C16
SMBCLK	H16
SMBDATA	E16
SMI#	AH26
SMLINK0	A15
SMLINK1	B15
SPI_CLK	G23
SPI_CS0#	E25
SPI_CS1#	F23
SPI_MISO	B26
SPI_MOSI	C26
SPKR	N8
SRTCRST#	H20
SST	C19
STOP#	F10
STP_CPU# / GPIO25†	B18
STP_PCI# / GPIO15	C15
STPCLK#	AJ29

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
SUS_STAT# / LPCPD / GPIO61†	R1
SUSCLK / GPIO62†	R5
SYS_RESET#	F19
TACH0 / GPIO17	AH21
TACH1 / GPIO1	AK21
TACH2 / GPIO6	AH22
TACH3 / GPIO7	AK23
THRM#	AK26
THRMTRIP#	AD24
DPRSTP#	AK28
DPSLP#	AE24
TP3	F20
TP4	E19
TP5	C18
TP6	A16
TP7	B16
TRDY#	E6
USBP0N	AD6
USBP0P	AD5
USBP10N	W2
USBP10P	W3
USBP11N	V1
USBP11P	V2
USBP1N	AE3
USBP1P	AE2
USBP2N	AD1
USBP2P	AD2
USBP3N	AB6
USBP3P	AB5
USBP4N	AC3
USBP4P	AC2
USBP5N	AB1
USBP5P	AB2
USBP6N	Y6
USBP6P	Y5
USBP7N	AA3
USBP7P	AA2
USBP8N	Y1

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
USBP8P	Y2
USBP9N	V6
USBP9P	V5
USBRBIAS	AG2
USBRBIAS#	AG1
V_CPU_IO	AH28
V_CPU_IO	AJ30
V5REF	A6
V5REF_Sus	AF1
Vcc1_1	A24
Vcc1_1	B24
Vcc1_1	C24
Vcc1_1	E24
Vcc1_1	F24
Vcc1_1	G24
Vcc1_1	H23
Vcc1_1	H24
Vcc1_1	J23
Vcc1_1	M12
Vcc1_1	M13
Vcc1_1	M15
Vcc1_1	M17
Vcc1_1	M18
Vcc1_1	M19
Vcc1_1	N12
Vcc1_1	N19
Vcc1_1	R12
Vcc1_1	R19
Vcc1_1	U12
Vcc1_1	U19
Vcc1_1	V12
Vcc1_1	V19
Vcc1_1	W12
Vcc1_1	W13
Vcc1_1	W15
Vcc1_1	W17
Vcc1_1	W18
Vcc1_1	W19
Vcc1_5_A	AA7

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vcc1_5_A	AA8
Vcc1_5_A	AB7
Vcc1_5_A	AB8
Vcc1_5_A	AB23
Vcc1_5_A	AC11
Vcc1_5_A	AC13
Vcc1_5_A	AC14
Vcc1_5_A	AC15
Vcc1_5_A	AC16
Vcc1_5_A	AC17
Vcc1_5_A	AC18
Vcc1_5_A	AC20
Vcc1_5_A	AD11
Vcc1_5_A	AD12
Vcc1_5_A	AD13
Vcc1_5_A	AD17
Vcc1_5_A	AE11
Vcc1_5_A	AE17
Vcc1_5_A	AF11
Vcc1_5_A	AF17
Vcc1_5_A	AH10
Vcc1_5_A	AH11
Vcc1_5_A	AH17
Vcc1_5_A	AH18
Vcc1_5_A	AJ10
Vcc1_5_A	AJ18
Vcc1_5_A	AK10
Vcc1_5_A	AK18
Vcc1_5_A	H10
Vcc1_5_A	H11
Vcc1_5_A	T1
Vcc1_5_B	AA23
Vcc1_5_B	AA24
Vcc1_5_B	AA25
Vcc1_5_B	AB24
Vcc1_5_B	AB25
Vcc1_5_B	AC25
Vcc1_5_B	AD25
Vcc1_5_B	AD26

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vcc1_5_B	AD28
Vcc1_5_B	AE28
Vcc1_5_B	AE29
Vcc1_5_B	AE30
Vcc1_5_B	J24
Vcc1_5_B	J25
Vcc1_5_B	K23
Vcc1_5_B	K24
Vcc1_5_B	K25
Vcc1_5_B	L24
Vcc1_5_B	L25
Vcc1_5_B	M23
Vcc1_5_B	M24
Vcc1_5_B	M25
Vcc1_5_B	N24
Vcc1_5_B	N25
Vcc1_5_B	P23
Vcc1_5_B	P24
Vcc1_5_B	P25
Vcc1_5_B	R24
Vcc1_5_B	R25
Vcc1_5_B	T23
Vcc1_5_B	T24
Vcc1_5_B	T25
Vcc1_5_B	T26
Vcc1_5_B	T28
Vcc1_5_B	U24
Vcc1_5_B	U28
Vcc1_5_B	U29
Vcc1_5_B	U30
Vcc1_5_B	V23
Vcc1_5_B	V24
Vcc1_5_B	V25
Vcc1_5_B	W24
Vcc1_5_B	W25
Vcc1_5_B	Y23
Vcc1_5_B	Y24
Vcc1_5_B	Y25
Vcc3_3	AC19

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vcc3_3	AC21
Vcc3_3	AD10
Vcc3_3	AF21
Vcc3_3	AH24
Vcc3_3	AH30
Vcc3_3	AK4
Vcc3_3	A2
Vcc3_3	B1
Vcc3_3	B9
Vcc3_3	G3
Vcc3_3	G11
Vcc3_3	H7
Vcc3_3	J2
Vcc3_3	K8
Vcc3_3	L8
VccCL1_1	A23
VccCL1_5	A26
VccCL3_3	B23
VccCL3_3	C23
VccDMI	AG29
VccDMI	AG30
VccDMIPLL	T30
VccGLAN1_5	B30
VccGLAN1_5	C28
VccGLAN1_5	C29
VccGLAN1_5	C30
VccGLAN3_3	A27
VccGLANPLL	A28
VccHDA	AC10
VccLAN1_1	A10
VccLAN1_1	B10
VccLAN3_3	A12
VccLAN3_3	B12
VccRTC	A22
VccSATAPLL	AK20
VccSus1_1	AC7
VccSus1_1	H17
VccSus1_5	AD8
VccSus1_5	H18

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
VccSus3_3	AF2
VccSus3_3	A17
VccSus3_3	B20
VccSus3_3	C20
VccSus3_3	E17
VccSus3_3	H15
VccSus3_3	U1
VccSus3_3	U2
VccSus3_3	U3
VccSus3_3	U5
VccSus3_3	U6
VccSus3_3	U7
VccSus3_3	U8
VccSus3_3	V8
VccSus3_3	W7
VccSus3_3	W8
VccSus3_3	Y8
VccSusHDA	AC9
VccUSBPLL	AK5
VRMPWRGD	C22
Vss	AA1
Vss	AA5
Vss	AA6
Vss	AA29
Vss	AA30
Vss	AB3
Vss	AB26
Vss	AB28
Vss	AC1
Vss	AC5
Vss	AC6
Vss	AC8
Vss	AC12
Vss	AC24
Vss	AC29
Vss	AC30
Vss	AD3
Vss	AD7
Vss	AD9

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vss	AD14
Vss	AD15
Vss	AD16
Vss	AD18
Vss	AD19
Vss	AD22
Vss	AE1
Vss	AE5
Vss	AE6
Vss	AE8
Vss	AE9
Vss	AE10
Vss	AE12
Vss	AE13
Vss	AE14
Vss	AE15
Vss	AE16
Vss	AE18
Vss	AE19
Vss	AE25
Vss	AF3
Vss	AF7
Vss	AF9
Vss	AF13
Vss	AF15
Vss	AF20
Vss	AF23
Vss	AF25
Vss	AF29
Vss	AG28
Vss	AH2
Vss	AH6
Vss	AH8
Vss	AH13
Vss	AH15
Vss	AH19
Vss	AH20
Vss	AH29
Vss	AJ4

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vss	AJ5
Vss	AJ8
Vss	AJ12
Vss	AJ14
Vss	AJ16
Vss	AJ20
Vss	AJ23
Vss	AJ26
Vss	AK2
Vss	AK8
Vss	AK12
Vss	AK14
Vss	AK16
Vss	AK27
Vss	AK29
Vss	AK30
Vss	A1
Vss	A30
Vss	B2
Vss	B5
Vss	B8
Vss	B11
Vss	B14
Vss	B17
Vss	B19
Vss	B22
Vss	B25
Vss	B27
Vss	B28
Vss	D28
Vss	E2
Vss	E15
Vss	E18
Vss	E22
Vss	E29
Vss	E30
Vss	F6
Vss	F9
Vss	F12

Table 6-1. Intel® ICH10 Ballout by Signal Name

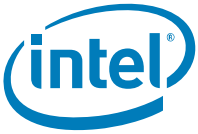
Ball Name	Ball #
Vss	F21
Vss	F26
Vss	F28
Vss	G16
Vss	G25
Vss	G29
Vss	G30
Vss	H2
Vss	H9
Vss	H13
Vss	H19
Vss	H22
Vss	H25
Vss	H26
Vss	H28
Vss	J6
Vss	J29
Vss	J30
Vss	K26
Vss	K28
Vss	L2
Vss	L23
Vss	L29
Vss	L30
Vss	M6
Vss	M8
Vss	M14
Vss	M16
Vss	M26
Vss	M28
Vss	N13
Vss	N14
Vss	N15
Vss	N16
Vss	N17
Vss	N18
Vss	N23
Vss	N29
Vss	N30

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vss	P2
Vss	P6
Vss	P12
Vss	P13
Vss	P14
Vss	P15
Vss	P16
Vss	P17
Vss	P18
Vss	P19
Vss	P26
Vss	P28
Vss	R8
Vss	R13
Vss	R14
Vss	R15
Vss	R16
Vss	R17
Vss	R18
Vss	R23
Vss	R29
Vss	R30
Vss	T2
Vss	T5
Vss	T12
Vss	T13
Vss	T14
Vss	T15
Vss	T16
Vss	T17
Vss	T18
Vss	T19
Vss	T29
Vss	U13
Vss	U14
Vss	U15
Vss	U16
Vss	U17
Vss	U18

Table 6-1. Intel® ICH10 Ballout by Signal Name

Ball Name	Ball #
Vss	U23
Vss	V3
Vss	V7
Vss	V13
Vss	V14
Vss	V15
Vss	V16
Vss	V17
Vss	V18
Vss	V26
Vss	V28
Vss	W1
Vss	W5
Vss	W6
Vss	W14
Vss	W16
Vss	W23
Vss	W29
Vss	W30
Vss	Y3
Vss	Y7
Vss	Y26
Vss	Y28
WAKE#	E20



7 Package Information

7.1 Intel® ICH10 Package

The ICH10 package information is shown in Figure 7-1, Figure 7-2, and Figure 7-3.

Note: All dimensions, unless otherwise specified, are in millimeters.

Figure 7-1. Intel® ICH10 Package (Top View)

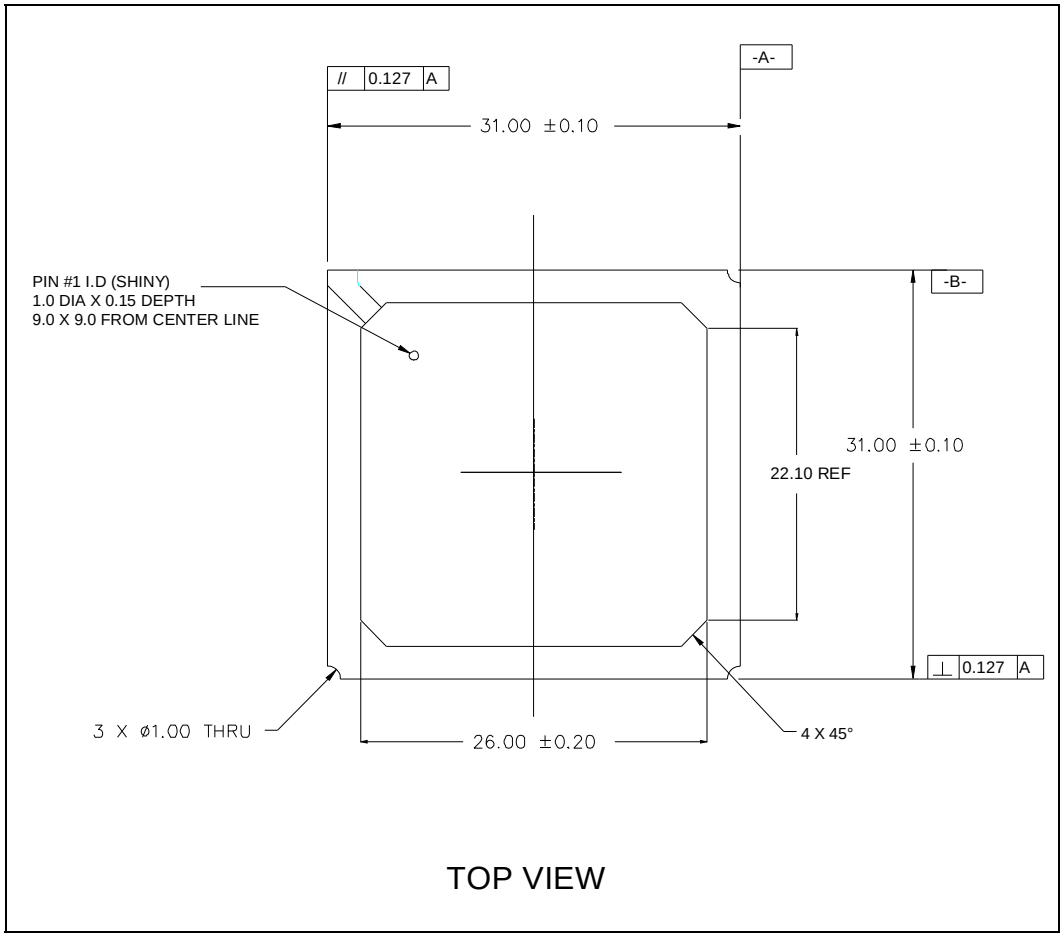


Figure 7-2. Intel® ICH10 Package (Bottom View)

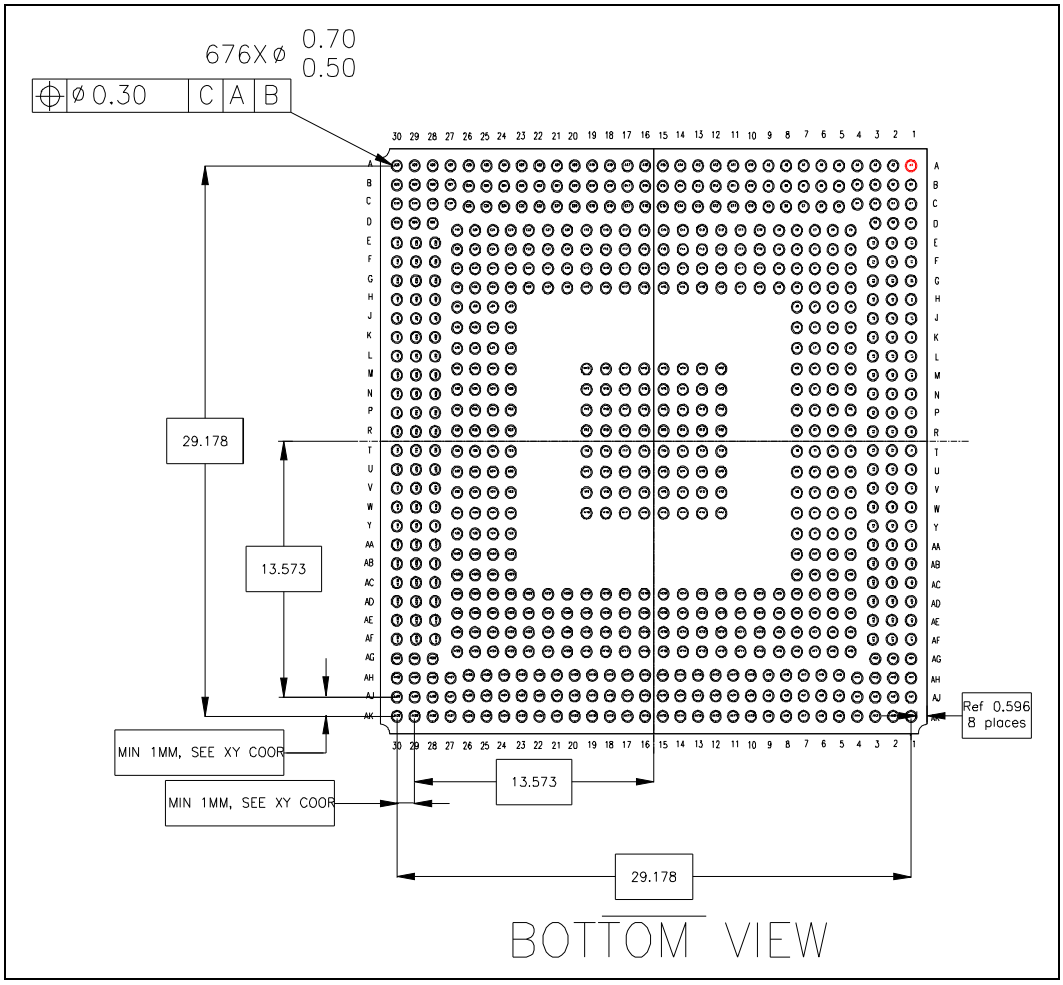
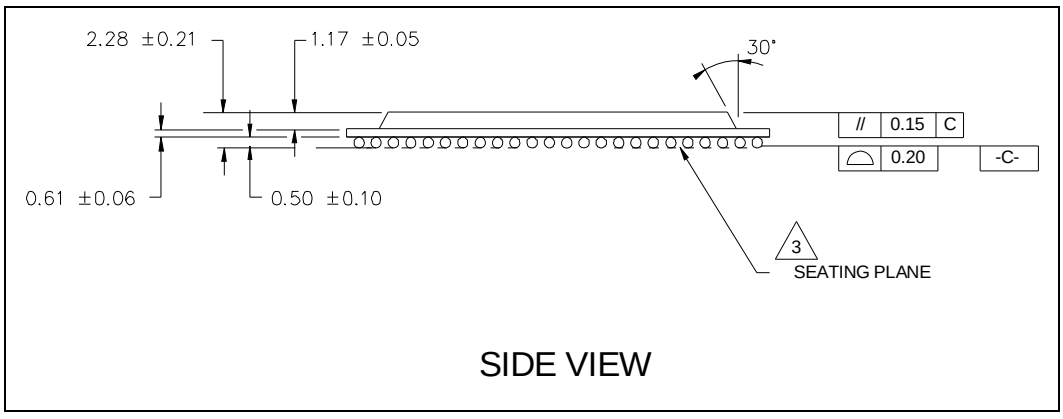


Figure 7-3. Intel® ICH10 Package (Side View)



§ §§

8 Electrical Characteristics

This chapter contains the DC and AC characteristics for the ICH10. AC timing diagrams are included.

8.1 Thermal Specifications

Refer to the *Intel® I/O Controller Hub (ICH10) Thermal Design Guidelines* document for ICH10 thermal information.

8.2 Absolute Maximum Ratings

Table 8-1. Intel® ICH10 Absolute Maximum Ratings

Parameter	Maximum Limits
Voltage on any 3.3 V Pin with respect to Ground	-0.5 to Vcc3_3 + 0.5 V
Voltage on any 5 V Tolerant Pin with respect to Ground (V5REF = 5 V)	-0.5 to V5REF + 0.5 V
1.1 V Supply Voltage with respect to VSS	-0.5 to 2.1 V
1.25 V Supply Voltage with respect to VSS	-0.5V to 2.1V
1.5 V Supply Voltage with respect to VSS	-0.5 to 2.1 V
3.3 V Supply Voltage with respect to VSS	-0.5 to 4.6 V
5.0 V Supply Voltage with respect to VSS	-0.5 to 5.5 V
V_CPU_IO Supply Voltage with respect to VSS	-0.5 to 2.1 V

8.3 DC Characteristics

Table 8-2. DC Current Characteristics (Consumer Only)[1]

Power Plane	Maximum Power Consumption			
Symbol	S0	S3	S4/S5	G3
V5REF	2 mA	N/A	N/A	N/A
V5REF_Sus	2 mA	1 mA	1 mA	N/A
Vcc3_3	308 mA	N/A	N/A	N/A
VccSus3_3	212 mA	53 mA	53 mA	N/A
VccHDA[6]	32mA	N/A	N/A	N/A
$VccSusHDA_6$	32 mA	1 mA	1 mA	N/A
VccGLAN3_3	1 mA	N/A	N/A	N/A
VccGLAN1_5	80 mA	N/A	N/A	N/A
VccLAN3_3[5]	19 mA	78 mA	78 mA	N/A

Table 8-2. DC Current Characteristics (Consumer Only)[1]

Power Plane	Maximum Power Consumption			
Symbol	S0	S3	S4/S5	G3
VccLAN1_1[2, 5]	Powered by Vcc1_1 in S0	Powered by VccLAN3_3 in S3	Powered by VccLAN3_3 in S4/S5	N/A
VccCL3_3	19 mA	73 mA	73 mA	N/A
VccCL1_5[2]	Powered by Vcc1_5_A in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S4/S5	N/A
VccCL1_12	Powered by Vcc1_1 in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S4/S5	N/A
Vcc1_5_A	1.644 A	N/A	N/A	N/A
Vcc1_5_B	646 mA	N/A	N/A	N/A
VccSus1_52	Powered by Vcc1_5_A in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S4/S5	N/A
Vcc1_1	1.634 A	N/A	N/A	N/A
VccSus1_12	Powered by Vcc1_1 in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S4/S5	N/A
VccRTC[3, 4]	N/A	N/A	N/A	6 µA
VccDMI[7]	50 mA	N/A	N/A	N/A
V_CPU_IO	2 mA	N/A	N/A	N/A
VccGLANPLL	23 mA	N/A	N/A	N/A
VccUSBPLL	11 mA	N/A	N/A	N/A
VccDMIPLL[7]	23 mA	N/A	N/A	N/A
VccSATAPLL	47 mA	N/A	N/A	N/A

NOTES:
1. These are estimated DC current numbers.
2. Internal voltage regulators power these wells inside the Intel ICH10 and current for these rails are accounted for in the sourcing voltage rail current requirements.
3. Only the G3 state of this rail is shown to provide an estimate of battery life.
4. Icc (RTC) data is taken with VccRTC at 3.0 V while the system is in a mechanical off (G3) state at room temperature.
5. The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.
6. The current for this rail was measured with VccHDA and VccSusHDA set to 3.3 V.
7. The current for this rail was measured with VccDMI set to 1.5 V.

Table 8-3. DC Current Characteristics (Corporate Only)

Power Plane	Maximum Power Consumption			
Symbol	**S0**	**S3**	**S4/S5**	**G3**
V5REF	1 mA	N/A	N/A	N/A
V5REF_Sus	2 mA	1 mA	1 mA	N/A
Vcc3_3	273 mA	N/A	N/A	N/A
VccSus3_3	212 mA	95 mA	95 mA	N/A
VccHDA[6]	30 mA	N/A	N/A	N/A
VccSusHDA[6]	31 mA	1 mA	1 mA	N/A
VccHDA[8]	10 mA	N/A	N/A	N/A
VccSusHDA[8]	11 mA	1 mA	1 mA	N/A
VccGLAN3_3	1 mA	N/A	N/A	N/A
VccGLAN1_5	62 mA	N/A	N/A	N/A
VccLAN3_3[5]	17 mA	77 mA	77 mA	N/A
VccLAN1_1[2, 5]	Powered by Vcc1_1 in S0	Powered by VccLAN3_3 in S3	Powered by VccLAN3_3 in S3	N/A
VccCL3_3	16 mA	70 mA	70 mA	N/A
VccCL1_5[2]	Powered by Vcc1_5_A in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S3	N/A
VccCL1_1[2]	Powered by Vcc1_1 in S0	Powered by VccCL3_3 in S3	Powered by VccCL3_3 in S3	N/A
Vcc1_5_A	1.390 A	N/A	N/A	N/A
Vcc1_5_B	591 mA	N/A	N/A	N/A
VccSus1_5[2]	Powered by Vcc1_5_A in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S3	N/A
Vcc1_1	2.553 A	N/A	N/A	N/A
VccSus1_1[2]	Powered by Vcc1_1 in S0	Powered by VccSus3_3 in S3	Powered by VccSus3_3 in S3	N/A
VccRTC[3, 4]	N/A	N/A	N/A	6 µA
VccDMI[7]	55 mA	N/A	N/A	N/A
V_CPU_IO	1 mA	N/A	N/A	N/A
VccGLANPLL	23 mA	N/A	N/A	N/A
VccUSBPLL	10 mA	N/A	N/A	N/A
VccDMIPLL[7]	22 mA	N/A	N/A	N/A
VccSATAPLL	42 mA	N/A	N/A	N/A

NOTES:
1. These are estimated DC current numbers.
2. Internal voltage regulators power these wells inside the Intel ICH10 and current for these rails are accounted for in the sourcing voltage rail current requirements.
3. Only the G3 state of this rail is shown to provide an estimate of battery life.
4. Icc (RTC) data is taken with VccRTC at 3.0 V while the system is in a mechanical off (G3) state at room temperature.
5. The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.
6. The current for this rail was measured with VccHDA and VccSusHDA set to 3.3 V.
7. The current for this rail was measured with VccDMI set to 1.5 V.
8. The current for this rail was measured with VccHDA and VccSusHDA set to 1.5 V.

Table 8-4. DC Characteristic Input Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{IH1}/V_{IL1} (5V Tolerant)	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, PAR, PERR#, PLOCK#, REQ[3:0]#, SERR#, STOP#, TRDY# **Interrupt Signals:** PIRQ[D:A]#, PIRQ[H:E]# **GPIO Signals:** GPIO[54, 52, 50, 5:2]
V_{IH2}/V_{IL2}	**Gigabit LAN Connect Signals:** GLAN_RX[p,n]
V_{IH3}/V_{IL3}	**Clock Signals:** CLK48 **Power Management Signals:** MCH_SYNC#, THRM#, VRMPWRGD, LAN_RST#, CLPWROK **SATA Signals:** SATAGP[5:4, 1:0]SATAGP[3:2] **Interrupt Signals:** SERIRQ **Processor Signals:** RCIN#, A20GATE **USB Signals:** OC[11:0]# **GPIO Signals:** GPIO[59, 55, 53, 51, 49:36, 35, 31:29, 22:16, 7:6, 1, 0], GPIO32 **Intel® Quiet System Technology Signals**: TACH[3:0] **Strap Signals:** GNT[3:0]#,SPKR, SATALED# (Strap purposes only)
V_{IH4}/V_{IL4}	**Clock Signals:** CLK14, PCICLK **LPC/Firmware Hub Signals:** LAD[3:0]/FWH[3:0], LDRQ0#, LDRQ1# **PCI Signals:** PME# **SPI Signals:** SPI_MISO **GPIO Signals:** GPIO[33, 23] **Strap Signals:** SPI_MOSI, GNT0# (Strap purposes only)
V_{IH5}/V_{IL5}	**SMBus Signals:** SMBCLK, SMBDATA, SMBALERT# **System Management Signals:** SMLINK[1:0], LINKALERT# **GPIO Signals**: GPIO[60, 11]
V_{IH6}/V_{IL6}	**LAN Signals:** GLAN_CLK, LAN_RXD[2:0]
V_{IH7}/V_{IL7}	**Processor Signals:** FERR#, THRMTRIP#
V_{IMIN8}/V_{IMAX8}	**PCI Express* Data RX Signals:** PER[p,n][6:1]
V_{IH9}/V_{IL9}	**Real Time Clock Signals:** RTCX1
V_{IMIN10}/V_{IMAX10}	**SATA Signals:** SATA[3:0]RX[P,N], SATA[5:4]RX[P,N]
V_{IH11}/V_{IL11}	**Intel® High Definition Audio Signals:** HDA_SDIN[3:0] **Strap Signals:** HDA_SDOUT, HDA_SYNC (Strap purposes only) **GPIO Signals**: GPIO34 **NOTE:** See V_{IL_HDA}/V_{IH_HDA} for High Definition Audio Low Voltage Mode
$V_{IH12}/V_{IL12}/V_{cross(abs)}$	**Clock Signals:** DMI_CLKN, DMI_CLKP, SATA_CLKN, SATA_CLKP
V_{IH13}/V_{IL13}	**Power Management Signals:** PWRBTN#, RI#, SYS_RESET#, WAKE# **GPIO Signals:** GPIO[60, 57:56, 28:26, 24, 14:12, 10:8], GPIO[25, 15]
V_{IH14}/V_{IL14}	**Power Management Signals:** PWROK, RSMRST# **System Management Signals:** INTRUDER# **Miscellaneous Signals:** INTVRMEN, LAN100_SLP, RTCRST#, SRTCRST#

Table 8-4. DC Characteristic Input Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
V_{IH_CL}/V_{IL_CL}	**Controller Link:** CL_CLK0, CL_DATA0
V_{DI} / V_{CM} / V_{SE} (5 V Tolerant)	**USB Signals:** USBP[11:0][P,N] (Low-speed and Full-speed)
V_{HSSQ} / V_{HSDSC} / V_{HSCM} (5 V Tolerant)	**USB Signals:** USBP[11:0][P,N] (in High-speed Mode)
V_{IH_HDA} / V_{IL_HDA}	**Intel® High Definition Audio Signals:** HDA_SDIN[3:0] **Strap Signals:** HDA_SDOUT, HDA_SYNC (Strap purposes only) **NOTE:** Only applies when running in Low Voltage Mode (1.5 V)
V_{IH_SST}/V_{IL_SST}	**Intel® Quiet System Technology Signals:** SST
V_{IH_PECI}/V_{IL_PECI}	**Intel® Quiet System Technology Signals:** PECI

1. V_{DI} = | USBPx[P] – USBPx[N]
2. Includes VDI range
3. Applies to Low-Speed/High-Speed USB
4. PCI Express mVdiff p-p = 2*|PETp[x] – PETn[x]|
5. GLAN mVdiff p-p = 2* |GLAN_RXp – GLAN_RXn|
6. SATA Vdiff, RX (VIMAX10/MIN10) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]RXP – SATA[x]RXN|
7. VccRTC is the voltage applied to the VccRTC well of the ICH10. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VccSus3_3.
8. CL_Vref = 0.27 (VccCL1_5). CL_VREF0 applies to all configurations.
9. Applies to Ultra DMA Modes greater than Ultra DMA Mode 4.
10. This is an AC Characteristic that represents transient values for these signals.
11. Applies to Hogh-Speed USB 2.0.

Table 8-5. DC Input Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	–0.5	0.3(Vcc3_3)	V	
V_{IH1}	Input High Voltage	0.5(Vcc3_3)	V5REF + 0.5	V	
V_{IL2}	Minimum Input Voltage	200	—	mVdiff p-p	Note 5
V_{IH2}	Maximum Input Voltage	—	1350	mVdiff p-p	Note 5
V_{IL3}	Input Low Voltage	–0.5	0.8	V	
V_{IH3}	Input High Voltage	2.0	3.3 V + 0.5	V	Note 12
V_{IL4}	Input Low Voltage	–0.5	0.3(3.3 V)	V	Note 12
V_{IH4}	Input High Voltage	0.5(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL5}	Input Low Voltage	–0.5	0.8	V	
V_{IH5}	Input High Voltage	2.1	3.3 V + 0.5	V	Note 12
V_{IL6}	Input Low Voltage	-0.5	0.3(3.3 V)	V	Note 12
V_{IH6}	Input High Voltage	0.6(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL7}	Input Low Voltage	–0.5	0.58(V_CPU_IO)	V	
V_{IH7}	Input High Voltage	0.73(V_CPU_IO)	V_CPU_IO + 0.5	V	
V_{IMIN8}	Minimum Input Voltage	175	—	mVdiff p-p	Note 4
V_{IMAX8}	Maximum Input Voltage	—	1200	mVdiff p-p	Note 4
V_{IL9}	Input Low Voltage	–0.5	0.10	V	
V_{IH9}	Input High Voltage	0.40	1.2	V	
$V_{IMIN10\text{- }Gen1i}$	Minimum Input Voltage - 1.5 Gb/s internal SATA	325	—	mVdiff p-p	6
$V_{IMAX10\text{-}Gen1i}$	Maximum Input Voltage - 1.5 Gb/s internal SATA	—	600	mVdiff p-p	6
$V_{IMIN10\text{-}Gen1m}$	Minimum Input Voltage - 1.5 Gb/s eSATA	240	—	mVdiff p-p	6
$V_{IMAX10\text{-}Gen1m}$	Maximum Input Voltage - 1.5 Gb/s eSATA	—	600	mVdiff p-p	6
$V_{IMIN10\text{-}Gen2i}$	Minimum Input Voltage - 3.0 Gb/s internal SATA	275	—	mVdiff p-p	6
$V_{IMAX10\text{-}Gen2i}$	Maximum Input Voltage - 3.0 Gb/s internal SATA	—	750	mVdiff p-p	6
$V_{IMIN10\text{-}Gen2m}$	Minimum Input Voltage - 3.0 Gb/s eSATA	240	—	mVdiff p-p	6

Table 8-5. DC Input Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IMAX10-Gen2m}$	Maximum Input Voltage - 3.0 Gb/s eSATA	—	750	mVdiff p-p	6
V_{IL11}	Input Low Voltage	–0.5	0.35(3.3 V)	V	Note 12
V_{IH11}	Input High Voltage	0.65(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL12}	Input Low Voltage	-0.150	0.150	V	
V_{IH12}	Input High Voltage	0.660	0.850	V	
V_{IL13}	Input Low Voltage	–0.5	0.8	V	
V_{IH13}	Input High Voltage	2.0	3.3 V + 0.5	V	Note 12
V_{IL14}	Input Low Voltage	–0.5	0.78	V	
V_{IH14}	Input High Voltage	2.0	VccRTC + 0.5	V	Note 7
V_{IL_CL}	Input Low Voltage	–0.3	(CL_VREF - 0.075)	V	Note 8
V_{IH_CL}	Input High Voltage	(CL_VREF + 0.075)	1.2	V	Note 8
V_{IL_CL2}	Input Low Voltage	–0.5	0.3(VccCL3_3)	V	
V_{IH_CL2}	Input High Voltage	0.5(VccCL3_3)	VccCL3_3 + 0.5	V	
$V_{cross(abs)}$	Absolute Crossing Point	0.250	0.550	V	
V_{DI}	Differential Input Sensitivity	0.2	—	V	Note 1,3
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Note 2,3
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	Note 3
V_{HSSQ}	HS Squelch Detection Threshold	100	150	mV	Note 11
V_{HSDSC}	HS Disconnect Detection Threshold	525	625	mV	Note 11
V_{HSCM}	HS Data Signaling Common Mode Voltage Range	–50	500	mV	Note 11
V_{IL_HDA}	Input Low Voltage	—	0.4(Vcc_HDA)	V	
V_{IH_HDA}	Input High Voltage	0.6(Vcc_HDA)	—	V	
V_{IL_SST}	Input Low Voltage	-0.5	0.4	V	
V_{IH_SST}	Input High Voltage	1.1	Vcc + 0.5	V	
V_{IL_PECI}	Input Low Voltage	-0.5	0.275(V_CPU_IO)	V	
V_{IH_PECI}	Input High Voltage	0.725(V_CPU_IO)	V_CPU_IO + 0.5	V	

NOTES:
1. V_{DI} = | USBPx[P] – USBPx[N]
2. Includes VDI range
3. Applies to Low-Speed/Full-Speed USB
4. PCI Express mVdiff p-p = 2*|PETp[x] - PETn[x]|
5. GLAN mVdiff p-p = 2* |GLAN_RXp - GLAN_RXn|
6. SATA Vdiff, RX (VIMAX10/MIN10) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]RXP - SATA[x]RXN|

7. VccRTC is the voltage applied to the VccRTC well of the ICH10. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VccSus3_3.
8. CL_Vref = 0.27 (VccCL1_5). CL_VREF0 applies to all configurations.
9. Applies to Ultra DMA Modes greater than Ultra DMA Mode 4
10. This is an AC Characteristic that represents transient values for these signals
11. Applies to Hogh-Speed USB 2.0.
12. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well. See Table 3-2 or Table 3-3 for signal and power well association.

Table 8-6. DC Characteristic Output Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
V_{OH1}/V_{OL1}	**Processor Signals:** A20M#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#, CPUPWRGD, DPSLP# **Power Management Signals:** DPRSTP#
V_{OH2}/V_{OL2}	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, PAR, PERR#, PLOCK#, SERR#(1), STOP#, TRDY# **Intel® High Definition Audio Signals:** HDA_RST#, HDA_SDOUT, HDA_SYNC, HDA_BIT_CLK **NOTE:** See V_{OH_HDA}/V_{OL_HDA} for High Definition Audio Low Voltage Mode **GPIO Signals:** GPIO33
V_{OH3}/V_{OL3}	**SMBus Signals:** SMBCLK (1), SMBDATA (1) **System Management Signals:** SMLINK[1:0](1), LINKALERT# **GPIO Signals:** GPIO[60, 11]
V_{OH4}/V_{OL4}	**Power Management Signals:** SLP_S3#, SLP_S4#, SLP_S5#, SLP_M#, SUSCLK, SUS_STAT#/LPCPD#, CK_PWRGD, S4_STATE#, DPRSLPVR **SATA Signals**: SATACLKREQ#, SATALED#, SLOAD, SDATAOUT[1:0] **GPIO Signals:** GPIO[49:48, 39:35, 32:31, 26, 21:18, 16, 7:6, 0], GPIO32 **Other Signals:** SPKR **Interrupt Signals:** SERIRQ
V_{OH5}/V_{OL5}	**USB Signals**: USBP[11:0][P,N] in Low-speed and Full-speed Modes
V_{OMIN6}/V_{OMAX6}	**PCI Express* Data TX Signals:** PET[p,n][6:1]
V_{OMIN7}/V_{OMAX7}	**SATA Signals:** SATA[5:4, 1:0]TX[P,N], SATA[3:2]TX[P,N]
V_{OH8}/V_{OL8}	**LPC/Firmware Hub Signals:** LAD[3:0]/FWH[3:0], LFRAME#/FWH[4], INIT3_3V# **Power Management Signal:** PLTRST# **PCI Signals:** PCIRST#, GNT[3:0]#, PME#(1) **Interrupt Signals:** PIRQ[D:A], PIRQ[H:E]#(1) **GPIO Signals:** GPIO[58, 55:50, 34, 23:22, 17, 5:2, 1] **SATA Signals:** SCLOCK **SPI Signals:** SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_CLK **LAN Signals:** LAN_RSTSYNC, LAN_TXD[2:0]

Table 8-6. DC Characteristic Output Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
V_{OH9}/V_{OL9}	**Power Management Signals:** STP_CPU#, STP_PCI# **GPIO Signals:** GPIO[60, 59, 57:56, 47:40, 31:27, 24, 15:12, 10:8], GPIO[25, 15] **System Management Signals:** LINKALERT#,
V_{OMIN10}/V_{OMAX10}	**Gigabit Lan Connect Signals:** GLAN_TX[p,n]
V_{HSOI} V_{HSOH} V_{HSOL} V_{CHIRPJ} V_{CHIRPK}	**USB Signals:** USBP[11:0][P:N] in High-speed Mode
V_{OH_HDA}/V_{OL_HDA}	**Intel® High Definition Audio Signals:** HDA_RST#, HDA_SDOUT, HDA_SYNC **NOTE:** Only applies when running in Low Voltage Mode (1.5 V)
V_{OH_PWM}/ V_{OL_PWM}	**Intel® Quiet System Technology PWM:** PWM[2:0](1)
V_{OH_CL1}/V_{OL_CL1}	**Link Controller Signals:** CL_CLK0, CL_DATA0
V_{OH_CL2}/V_{OL_CL2}	**Link Controller Signals:** CL_RST0#
V_{OH_SST}/V_{OL_SST}	**SST signal:** SST
V_{OH_PECI}/ V_{OL_PECI}	**PECI signal:** PECI

NOTE:
1. These signals are open-drain.

Table 8-7. DC Output Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL1}	Output Low Voltage	—	0.255	V	3 mA	Note 4
V_{OH1}	Output High Voltage	V_CPU_IO - 0.3	—	V	-3 mA	
V_{OL2}	Output Low Voltage	—	0.1(3.3 V)	V	1.5 mA	Note 7
V_{OH2}	Output High Voltage	0.9(3.3 V)	—	V	-0.5 mA	Note 7
V_{OL3}	Output Low Voltage	—	0.4	V	4 mA	
V_{OH3}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 1
V_{OL4}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH4}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 7
V_{OL5}	Output Low Voltage	—	0.4	V	5 mA	
V_{OH5}	Output High Voltage	3.3 V – 0.5	—	V	-2 mA	Note 7
V_{OMIN6}	Minimum Output Voltage	800	—	mVdif fp-p		Note 2
V_{OMAX6}	Maximum Output Voltage	—	1200	mVdif fp-p		Note 2
$V_{OMIN7\text{-}Gen1i,m}$	Minimum Output Voltage	400	—	mVdif fp-p		Note 3
$V_{OMAX7\text{-}Gen1i,m}$	Maximum Output Voltage	—	600	mVdif fp-p		Note 3
$V_{OMIN7\text{-}Gen2i,m}$	Minimum Output Voltage	400	—	mVdif fp-p		Note 3
$V_{OMAX7\text{-}Gen2i,m}$	Maximum Output Voltage	—	700	mVdif fp-p		Note 3
V_{OL8}	Output Low Voltage	—	0.1(3.3 V)	V	1.5 mA	Note 7
V_{OH8}	Output High Voltage	0.9(3.3 V)	—	V	-0.5 mA	Note 1, 7
V_{OL9}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH9}	Output High Voltage	3.3 V - 0.5	—	V	-0.5 mA	Note 7
V_{OMIN10}	Minimum Output Voltage	750	—	mVdif fp-p		Note 6
V_{OMAX10}	Maximum Output Voltage	—	1350	mVdif fp-p		Note 6
V_{HSOI}	HS Idle Level	–10.0	10.0	mV		
V_{HSOH}	HS Data Signaling High	360	440	mV		
V_{HSOL}	HS Data Signaling Low	–10.0	10.0	mV		
V_{CHIRPJ}	Chirp J Level	700	1100	mV		
V_{CHIRPK}	Chirp K Level	–900	–500	mV		

Table 8-7. DC Output Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL_PWM}	Output Low Voltage	—	0.4	V	5 mA	
V_{OH_PWM}	Output High Voltage	—	—			Note 1
V_{OL_CL1}	Output Low Voltage	—	0.15	V	1 mA	
V_{OH_CL1}	Output High Voltage	0.485(VccCL1_5)	—	V		
V_{OL_CL2}	Output Low Voltage	—	0.1(VccCL1_5)	V	1.5 mA	
V_{OH_CL2}	Output High Voltage	0.9(VccCL1_5)	—	V	-1.5 mA	
V_{OL_CL3}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH_CL3}	Output High Voltage	VccCL3_3 -0.5	—	V	-0.5 mA	
V_{OL_SST}	Output Low Voltage	—	0.3	V	0.5 mA	
V_{OH_SST}	Output High Voltage	1.1	—	V	-6 mA	
V_{OL_PECI}	Output Low Voltage	—	0.25(V_CPU_IO)	V	0.5 mA	
V_{OH_PECI}	Output High Voltage	0.75(V_CPU_IO)	—		-6 mA	
VOL_HDA	Output Low Voltage	—	0.1(VccHDA)	V	1.5 mA	
VOH_HDA	Output High Voltage	0.9(VccHDA)	—	V	-0.5 mA	

NOTES:

1. The SERR#, PIRQ[H:A], SMBDATA, SMBCLK, LINKALERT#, SMLINK[1:0], and PWM[2:0] signal has an open-drain driver and SATALED# has an open-collector driver, and the V_{OH} specification does not apply. This signal must have external pull up resistor.
2. PCI Express mVdiff p-p = 2*|PETp[x] – PETn[x]|
3. SATA Vdiff, tx (V_{OMIN7}/V_{OMAX7}) is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]TXP – SATA[x]TXN|
4. Maximum Iol for CPUPWRGD is 12 mA for short durations (<500 mS per 1.5 s) and 9 mA for long durations.
5. For INIT3_3V only, for low current devices, the following applies: V_{OL5} Max is 0.15 V at an I_{OL5} of 2 mA.
6. GLAN mVdiff p-p = 2*|GLAN_TXp – GLAN_TXn|
7. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well. See Table 3-2 or Table 3-3 for signal and power well association.

Table 8-8. Other DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_CPU_IO	Processor I/F	0.945	—	1.3	V	1
V5REF	ICH10 Core Well Reference Voltage	4.75	5	5.25	V	1
CL_VREF	Controller Link Reference Voltage	0.385	0.405	0.425	V	1, 3
Vcc3_3	I/O Buffer Voltage	3.135	3.3	3.465	V	1
Vcc1_5_A, Vcc1_5_B, VccUSBPLL, VccSATAPLL, VccDMIPLL VccGLANPLL	Internal Logic and I/O Buffer Voltage	1.425	1.5	1.575	V	1
V5REF_Sus	Suspend Well Reference Voltage	4.75	5	5.25	V	1
VccSus3_3	Suspend Well I/O Buffer Voltage	3.135	3.3	3.465	V	1
Vcc1_1 (Consumer Only)	Internal Logic Voltage	0.998	1.1	1.155	V	1
Vcc1_1 (Corporate Only)	Internal Logic Voltage	1.045	1.1	1.155	V	1
VccHDA	High Definition Audio Controller Core Voltage	3.135	3.3	3.465	V	1
VccHDA (low voltage 1.5 V)	High Definition Audio Controller Low Voltage Mode Core Voltage	1.425	1.5	1.575	V	1
Vcc_DMI	DMI Buffer Voltage	1.188	1.25	1.312	V	
Vcc_DMI (ESI Mode Only)	DMI Buffer Voltage	1.425	1.5	1.575	V	
VccLAN3_3	LAN Controller I/O Buffer Voltage	3.135	3.3	3.465	V	1
VccGLAN1_5	Gigabit Lan Transmitter and Receiver Voltage	1.425	1.5	1.575	V	1
VccGLAN3_3	Gigabit Lan Internal Logic and I/O Buffer Voltage	3.135	3.3	3.465	V	1
VccCL3_3	Controller Link Buffer Voltage	3.135	—	3.465	V	1
VccRTC (G3-S0)	Battery Voltage	2	—	3.465	V	1
VccSusHDA	High Definition Audio Controller Suspend Voltage	3.135	3.3	3.465	V	1
VccSusHDA (low voltage)	High Definition Audio Controller Low Voltage Mode Suspend Voltage	1.425	1.5	1.575	V	1
V_{DI}	Differential Input Sensitivity	0.2	—	—	V	|(USBPx+,USBPx–)|
V_{CM}	Differential Common Mode Range	0.8	—	2.5	V	Includes V_{DI}
V_{CRS}	Output Signal Crossover Voltage	1.3	—	2.0	V	
V_{SE}	Single Ended Rcvr Threshold	0.8	—	2.0	V	
I_{LI1}	ATA Input Leakage Current	–200	—	200	µA	(0 V < V_{IN} < 5V)

Table 8-8. Other DC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
I_{LI2}	PCI_3V Hi-Z State Data Line Leakage	–10	—	10	µA	(0 V < VIN < Vcc3_3)
I_{LI3}	PCI_5V Hi-Z State Data Line Leakage	–70	—	70	µA	Max V_{IN} = 2.7 V Min V_{IN} = 0.5 V
I_{LI4}	Input Leakage Current – Clock signals	–100	—	+100	µA	2
C_{IN}	Input Capacitance – All Other	—	—	12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance	—	—	12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance	—	—	12	pF	F_C = 1 MHz
		Typical Value				
C_L	XTAL1	6			pF	
C_L	XTAL2	6			pF	

NOTES:
1. The I/O buffer supply voltage is measured at the ICH package pins. The tolerances shown in Table 8-8 are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.
2. Includes CLK14, CLK48, GLAN_CLK and PCICLK
3. CL_VREF voltage applies when pin is driven by external circuit.

8.4 AC Characteristics

Table 8-9. Clock Timings (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes	Figure
PCI Clock (PCICLK)						
t1	Period	30	33.3	ns		8-1
t2	High Time	12	—	ns		8-1
t3	Low Time	12	—	ns		8-1
t4	Rise Time	—	3	ns		8-1
t5	Fall Time	—	3	ns		8-1
14 MHz Clock (CLK14)						
t6	Period	67	70	ns		8-1
t7	High Time	20	—	ns		8-1
t8	Low Time	20	—	ns		8-1
t41	Rising Edge Rate	1.0	4.0	V/ns	5	
t42	Falling Edge Rate	1.0	4.0	V/ns	5	
48 MHz Clock (CLK48)						
f_{clk48}	Operating Frequency	48.000	—	MHz	1	
t9	Frequency Tolerance	—	100	ppm		
t10	High Time	7	—	ns		8-1
t11	Low Time	7	—	ns		8-1
t12	Rise Time	—	1.2	ns		8-1
t13	Fall Time	—	1.2	ns		8-1
SMBus Clock (SMBCLK)						
f_{smb}	Operating Frequency	10	100	KHz		
t18	High time	4.0	50	µs	2	8-10
t19	Low time	4.7	—	µs		8-10
t20	Rise time	—	1000	ns		8-10
t21	Fall time	—	300	ns		8-10
HDA_BIT_CLK (Intel® High Definition Audio)						
f_{HDA}	Operating Frequency	24.0		MHz		
	Frequency Tolerance	—	100	ppm		
t26a	Input Jitter (refer to Clock Chip Specification)	—	300	ppm		
t27a	High Time (Measured at 0.75 Vcc)	18.75	22.91	ns		8-1
t28a	Low Time (Measured at 0.35 Vcc)	18.75	22.91	ns		8-1
SATA Clock (SATA_CLKP, SATA_CLKN) / DMI Clock (DMI_CLKP, DMI_CLKN)						
t36	Period	9.997	10.0533	ns		

Table 8-9. Clock Timings (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes	Figure
tsatasl	Slew rate	1	8	V/ns	7	
Suspend Clock (SUSCLK)						
f_{susclk}	Operating Frequency	32		kHz	4	
t39	High Time	10	—	µs	4	
t39a	Low Time	10	—	µs	4	
Gigabit Internet Clock (GLAN_CLK)						
tglanclk	Operating Fequency	5	62.5	MHz	6	
tglanhi	High Time	6.4	—	ns		
tglanlo	Low Time	6.4	—	ns		
tglansl	Slew rate	1.0	4	V/ns		
Intel® Quiet System Technology						
f_{pwm}	PWM Operating Frequency	10	28,000	Hz		

NOTES:
1. The CLK48 expects a 40/60% duty cycle.
2. The maximum high time (t18 Max) provide a simple ensured method for devices to detect bus idle conditions.
3. BITCLK Rise and Fall times are measured from 10%VDD and 90%VDD.
4. SUSCLK duty cycle can range from 30% minimum to 70% maximum.
5. CLK14 edge rates in a system as measured from 0.8 V to 2.0 V.
6. The active frequency can be 5 MHz, 50 MHz or 62.5 MHz depending on the interface speed. Dynamic changes of the normal operating frequency are not allowed.
7. See *CK505 Clock Synthesizer Specification* for measurement procedure.

Table 8-10. PCI Interface Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t40	AD[31:0] Valid Delay	2	11	ns	1	8-2
t41	AD[31:0] Setup Time to PCICLK Rising	7	—	ns		8-3
t42	AD[31:0] Hold Time from PCICLK Rising	0	—	ns		8-3
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, DEVSEL# Valid Delay from PCICLK Rising	2	11	ns	1	8-2
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, IDSEL, DEVSEL# Output Enable Delay from PCICLK Rising	2		ns		8-6
t45	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PERR#, PLOCK#, DEVSEL#, GNT[A:B]# Float Delay from PCICLK Rising	2	28	ns		8-4
t46	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, Setup Time to PCICLK Rising	7		ns		8-3

Table 8-10. PCI Interface Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t47	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, REQ[A:B]# Hold Time from PCLKIN Rising	0	—	ns		8-3
t48	PCIRST# Low Pulse Width	1		ms		8-5
t49	GNT[3:0]# Valid Delay from PCICLK Rising	2	12	ns		
t50	REQ[3:0]# Setup Time to PCICLK Rising	12	—	ns		

NOTE:
1. Refer to note 3 of table 4-4 in Section 4.2.2.2 and note 2 of table 4-6 in Section 4.2.3.2 of the *PCI Local Bus Specification,* Revision 2.3 for measurement details.

Table 8-11. Universal Serial Bus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
Full-speed Source (Note 7)						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	8-7
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	8-7
t102	Source Differential Driver Jitter - To Next Transition - For Paired Transitions	 –3.5 –4	 3.5 4	 ns ns	2, 3	8-8
t103	Source SE0 interval of EOP	160	175	ns	4	8-9
t104	Source Jitter for Differential Transition to SE0 Transition	–2	5	ns	5	
t105	Receiver Data Jitter Tolerance - T o Next Transition - For Paired Transitions	 –18.5 –9	 18.5 9	 ns ns	3	8-8
t106	EOP Width: Must accept as EOP	82	—	ns	4	8-9
t107	Width of SE0 interval during differential transition	—	14	ns		
Low-speed Source (Note 8)						
t108	USBPx+, USBPx – Driver Rise Time	75	300	ns	1, 6 C_L = 50 pF C_L = 350 pF	8-7
t109	USBPx+, USBPx – Driver Fall Time	75	300	ns	1,6 C_L = 50 pF C_L = 350 pF	8-7
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	 –25 –14	 25 14	 ns ns	2, 3	8-8
t111	Source SE0 interval of EOP	1.25	1.50	µs	4	8-9
t112	Source Jitter for Differential Transition to SE0 Transition	–40	100	ns	5	

Table 8-11. Universal Serial Bus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
Full-speed Source (Note 7)						
t113	Receiver Data Jitter Tolerance - To Next Transition- For Paired Transitions	–152 –200	152 200	ns ns	3	8-8
t114	EOP Width: Must accept as EOP	670	—	ns	4	8-9
t115	Width of SE0 interval during differential transition	—	210	ns		

NOTES:
1. Driver output resistance under steady state drive is spec'd at 28 ohms at minimum and 43 ohms at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full-speed Data Rate has minimum of 11.97 Mb/s and maximum of 12.03 Mb/s.
8. Low-speed Data Rate has a minimum of 1.48 Mb/s and a maximum of 1.52 Mb/s.

Table 8-12. SATA Interface Timings

Sym	Parameter	Min	Max	Units	Notes	Figure
UI	Gen I Operating Data Period	666.43	670.23	ps		
UI-2	Gen II Operating Data Period (3Gb/s)	333.21	335.11	ps		
t120	Rise Time	0.15	0.41	UI	1	
t121	Fall Time	0.15	0.41	UI	2	
t122	TX differential skew	—	20	ps		
t123	COMRESET	310.4	329.6	ns	3	
t124	COMWAKE transmit spacing	103.5	109.9	ns	3	
t125	OOB Operating Data period	646.67	686.67	ns	4	

NOTES:
1. 20% – 80% at transmitter
2. 80% – 20% at transmitter
3. As measured from 100 mV differential crosspoints of last and first edges of burst.
4. Operating data period during Out-Of-Band burst transmissions.

Table 8-13. SMBus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t130	Bus Free Time Between Stop and Start Condition	4.7	—	µs		8-10
t131	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0	—	µs		8-10
t132	Repeated Start Condition Setup Time	4.7	—	µs		8-10
t133	Stop Condition Setup Time	4.0	—	µs		8-10
t134	Data Hold Time	0	—	ns	4	8-10
t135	Data Setup Time	250	—	ns		8-10
t136	Device Time Out	25	35	ms	1	
t137	Cumulative Clock Low Extend Time (slave device)	—	25	ms	2	8-11
t138	Cumulative Clock Low Extend Time (master device)	—	10	ms	3	8-11

NOTES:
1. A device will timeout when any clock low exceeds this value.
2. t137 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t138 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack or ack-to-stop.
4. t134 has a minimum timing for I^2C of 0 ns, while the minimum timing for SMBus is 300 ns.

Table 8-14. Intel® High Definition Audio Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t143	Time duration for which HDA_SDOUT is valid before HDA_BIT_CLK edge.	7	—	ns		8-13
t144	Time duration for which HDA_SDOUT is valid after HDA_BIT_CLK edge.	7	—	ns		8-13
t145	Setup time for HDA_SDIN[3:0] at rising edge of HDA_BIT_CLK	15	—	ns		8-13
t146	Hold time for HDA_SDIN[3:0] at rising edge of HDA_BIT_CLK	0	—	ns		8-13

Table 8-15. LPC Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t150	LAD[3:0] Valid Delay from PCICLK Rising	2	11	ns		8-2
t151	LAD[3:0] Output Enable Delay from PCICLK Rising	2		ns		8-6
t152	LAD[3:0] Float Delay from PCICLK Rising	—	28	ns		8-4
t153	LAD[3:0] Setup Time to PCICLK Rising	7	—	ns		8-3
t154	LAD[3:0] Hold Time from PCICLK Rising	0	—	ns		8-3
t155	LDRQ[1:0]# Setup Time to PCICLK Rising	12	—	ns		8-3
t156	LDRQ[1:0]# Hold Time from PCICLK Rising	0	—	ns		8-3
t157	LFRAME# Valid Delay from PCICLK Rising	2	12	ns		8-2

Table 8-16. Miscellaneous Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t160	SERIRQ Setup Time to PCICLK Rising	7	—	ns		8-3
t161	SERIRQ Hold Time from PCICLK Rising	0	—	ns		8-3
t162	RI#, EXTSMI#, GPIO, USB Resume Pulse Width	2	—	RTCCLK		8-5
t163	SPKR Valid Delay from OSC Rising	—	200	ns		8-2
t164	SERR# Active to NMI Active	—	200	ns		
t165	IGNNE# Inactive from FERR# Inactive	—	230	ns		

Table 8-17. SPI Timings (20 MHz)

Sym	Parameter	Min	Max	Units	Notes	Fig
t180	Serial Clock Frequency - 20M Hz Operation	17.2	18.4	MHz	1	
t182	SPI Clock Duty cycle at the host	40%	60%			8-12
t183	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	13	ns		8-12
t184	Setup of SPI_MISO with respect to serial clock falling edge at the host	16	—	ns		8-12
t185	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	—	ns		8-12
t186	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		8-12
t187	Hold of SPI_CS[1:0]# deassertion with respect to serial clock falling at the host	30	—	ns		8-12

NOTE:
1. The typical clock frequency driven by the ICH10 is 17.86 MHz.

Table 8-18. SPI Timings (33 MHz)

Sym	Parameter	Min	Max	Units	Notes	Fig
t180b	Serial Clock Frequency - 33 MHz Operation	30.3	32.19	MHz	1	
t182b	SPI Clock Duty cycle at the host	48%	52%			8-12
t183b	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	5	ns		8-12
t184b	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	—	ns		8-12
t185b	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	—	ns		8-12
t186b	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		8-12
t187b	Hold of SPI_CS[1:0]# deassertion with respect to serial clock falling at the host	30	—	ns		8-12

NOTE:
1. The typical clock frequency driven by the ICH10 is 31.25 MHz.

Table 8-19. SST Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t_{BIT}	Bit time (overall time evident on SST) Bit time driven by an originator	0.495 0.495	500 250	µs µs	1	-
$t_{BIT,}$jitter	Bit time jitter between adjacent bits in an SST message header or data bytes after timing has been negotiated	—	—	%		
t_{BIT},drift	Change in bit time across a SST address or SST message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	—	—	%		
t_{H1}	High level time for logic '1'	0.6	0.8	x t_{BIT}	2	
t_{H0}	High level time for logic '0'	0.2	0.4	x t_{BIT}		
t_{SSTR}	Rise time (measured from V_{OL} = 0.3V to $V_{IH,min}$)	—	25 + 5	ns/ node		
t_{SSTF}	Fall time (measured from V_{OH} = 1.1V to $V_{IL,max}$)	—	33	ns/ node		

NOTES:
1. The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µs. t_{BIT} limits apply equally to t_{BIT-A} and t_{BIT-M}. ICH10 is targeted on 1 Mbps which is 1 µs bit time.
2. The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse.
3. t_{BIT-A} is the negotiated address bit time and t_{BIT-M} is the negotiated message bit time.

Table 8-20. PECI Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t_{BIT}	Bit time (overall time evident on PECI) Bit time driven by an originator	0.495 0.495	500 250	µs µs	1	
t_{BIT},jitter	Bit time jitter between adjacent bits in an PECI message header or data bytes after timing has been negotiated	—	—	%		
t_{BIT},drift	Change in bit time across a PECI address or PECI message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	—	—	%		
t_{H1}	High level time for logic '1'	0.6	0.8	x t_{BIT}	2	
t_{H0}	High level time for logic '0'	0.2	0.4	x t_{BIT}		
t_{PECIR}	Rise time (measured from VOL to VIH,min, Vtt(nom) -5%)	—	30 + 5	ns/ node	3	
t_{PECIF}	Fall time (measured from V_{OH} to V_{IL},max, Vtt(nom) +5%)	—	30	ns/ node	3	

NOTES:
1. The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µs. tBIT limits apply equally to t_{BIT-A} and t_{BIT-M}. ICH10 is targeted on 2 MHz which is 500 ns bit time.
2. The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse.
3. Extended trace lengths may appear as additional nodes.
4. t_{BIT-A} is the negotiated address bit time and t_{BIT-M} is the negotiated message bit time.

Table 8-21. Power Sequencing and Reset Signal Timings (Sheet 1 of 2)

Sym	Parameter	Min	Max	Units	Notes	Fig
t200	VccRTC active to RTCRST# inactive	18	—	ms		8-14
t201	V5REF_Sus active to VccSus3_3 active	0	—	ms	1	8-14
t202	VccSus3_3 active to VccSus1_1 active	—	—	—	2	8-14
t203	VccRTC supply active to VccSus supplies active	0	—	ms	3, 9	8-14
t204	VccSus supplies active to RSMRST# inactive	10	—	ms	9	8-14 8-15
t209	V5REF active to Vcc3_3 active	0	—	ms	1	8-14
t211	Vcc1_5 active to V_CPU_IO active	—	—	–	4	8-14
t212	VRMPWRGD active to PWROK active	5	—	ms		8-15 8-17
t213	VccSus supplies active to Vcc supplies active	0	—	ms	9, 10	8-14

Table 8-21. Power Sequencing and Reset Signal Timings (Sheet 2 of 2)

Sym	Parameter	Min	Max	Units	Notes	Fig
t214	Vcc supplies active to PWROK Note: PWROK assertion indicates that PCICLK has been stable for at least 1 ms.	99	—	ms	10	8-14 8-15 8-17
t217	PWROK and VRMPWRGD active to SUS_STAT# inactive and Processor interface signals latched to strap value (Consumer Only)	33	71	RTCCLK	5, 6, 8	8-15 8-17
t217	PWROK and VRMPWRGD active to SUS_STAT# inactive and Processor interface signals latched to strap value (Corporate Only)	33	—	RTCCLK	5, 6, 8	8-15 8-17
t218	SUS_STAT# inactive to PLTRST# inactive (Consumer Only)	2	—	RTCCLK	6	8-15 8-17
t218	SUS_STAT# inactive to PLTRST# inactive (Corporate Only)	60	—	µs		8-15 8-17
t219	PLTRST# assertion to VccGLANPLL inactive for platforms using ICH10 integrated GbE LAN	200	—	µs	7	
t228	HDA_RST# active low pulse width	1	—	µs		
t229	HDA_RST# inactive to HDA_BIT_CLK startup delay	162.8	—	ns		

NOTES:

1. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.
2. The associated 3.3 V and 1.1 V supplies are assumed to power up or down 'together'.
3. The VccSus supplies must **never** be active while the VccRTC supply is inactive.
4. a) Vcc1_5 must power up before V_CPU_IO or after V_CPU_IO within 0.7 V, b) V_CPU_IO must power down before Vcc1_5 or after Vcc1_5 within 0.7 V.
5. INIT# value determined by value of the CPU BISTEnable bit (Chipset Configuration Register Offset 3414h: bit 2).
6. These transitions are clocked off the internal RTC. 1 RTC clock is approximately from 28.992 µs to 32.044 µs
7. "VccGLANPLL inactive" is defined for this timing to be when VccGLANPLL drops to 1.425 V or less, as measured at the ICH10. This timing applies only to platforms using ICH10 integrated GbE LAN.
8. Maximum timing may be exceeded in a Intel Management Engine enabled system.
9. VccSus supplies include VccSus3_3, V5REF_Sus, VccSusHDA, VccLAN3_3 (if LAN powered in S3/S4/S5), and VccCL3_3 (if controller link powered in S3/S4/S5).
10. Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_1, VccUSBPLL, VccDMIPLL, VccSATAPLL, V5REF, V_CPU_IO, VccDMI, VccHDA, VccGLANPLL, VccGLAN3_3 and VccGLAN1_5 (if integrated Gigabit LAN enabled), VccLAN3_3 (if LAN only power in S0), and VccCL3_3 (if controller link only powered in S0).

.

Table 8-22. Power Management Timings (Sheet 1 of 3)

Sym	Parameter	Min	Max	Units	Notes	Fig
t230	VccSus active to SLP_S5#, SLP_S4#, SLP_S3#, SUS_STAT#, PLTRST# and PCIRST#active	—	50	ns		8-15
t231 t232	RSMRST# inactive to SUSCLK running, SLP_S5# inactive	—	110	ms	6, 22	8-15
t233	SLP_S5# inactive to SLP_S4# inactive	See Note Below			8	8-15
t234	SLP_S4# inactive to SLP_S3# inactive	1	Note 16	RTCCLK	1	8-15 8-17 8-21 8-22
t250	Processor I/F signals latched prior to STPCLK# active	0	—		9	8-18 8-19 8-20
t251	Bus Master Idle to DPSLP# active	3.36	—	µs	11	8-19 8-20
t252	DMI message to PMSYNC# assertion	0	—	PCICLK		
t253	DPSLP# active to STP_CPU# active	1	1	PCICLK	3	8-19 8-20
t254	STP_CPU# active to processor clock stopped	0	—	PCICLK	3, 10	8-19 8-20
t255	STP_CPU# active to DPRSTP#, DPRSLPVR active	0	—			8-20
t265	Break Event to DPRSTP#, DPRSLPVR inactive (C4 Exit)	1.5	1.8	µs	12	8-20
t266a	DPRSLPVR, DPRSTP# inactive to STP_CPU# inactive and CPU Vcc ramped	Programable. See D31:F0:AA, bits 3:2		µs		8-20
t267	Break Event to STP_CPU# inactive (C3 Exit)	6	Note 14	PCICLK	3, 13, 14	8-19
t268	STP_CPU# inactive to processor clock running	0	3	PCICLK	3, 10	8-19 8-20
t269	STP_CPU# inactive to DPSLP# inactive	1	1	PCICLK	3, 7	8-19 8-20
t270	DPSLP# inactive to STPCLK# inactive	0		µs		8-19 8-20
t273	Break Event to STPCLK# inactive (C2 Exit)	0		ns		8-18
t274	STPCLK# inactive to processor I/F signals unlatched	8	9	PCICLK	3, 9	8-18 8-19 8-20
t280	STPCLK# active to DMI Message	0		PCICLK	2	8-16 8-17
t281	DMI Message to CPUSLP# active	60	63	PCICLK	3	8-16

Table 8-22. Power Management Timings (Sheet 2 of 3)

Sym	Parameter	Min	Max	Units	Notes	Fig
t283	DMI Message to SUS_STAT# active	2		RTCCLK	1	8-17
t284	SUS_STAT# active to PLTRST#, PCIRST# active	7	17	RTCCLK	1	8-17
t287	PLTRST#, PCIRST# active to SLP_S3# active (Consumer Only)	1	2	RTCCLK	1	8-17
t287	PLTRST#, PCIRST# active to SLP_S3# active (Corporate Only)	1	—	RTCCLK	1	8-17
t289	SLP_S3# active to PWROK, VRMPWRGD inactive	0		ms	4	8-17
t291	SLP_S3# active to SLP_S4# active (Consumer Only)	1	2	RTCCLK	1	8-17
t291	SLP_S3# active to SLP_S4# active (Corporate Only)	1	—	RTCCLK	1	8-17
t294	PWROK, VRMPWRGD inactive to Vcc supplies inactive (nominal voltage -5%)	20		ns	23, 25	8-17 8-25
t295	SLP_S4# active to SLP_S5# active (Consumer Only)	1	2	RTCCLK	1, 5	8-17
t295	SLP_S4# active to SLP_S5# active (Corporate Only)	1	—	RTCCLK	1, 5	8-17
t296	Wake Event to SLP_S5# inactive	1	10	RTCCLK	1	8-17
t297	SLP_S5# inactive to SLP_S4# inactive	1	—	RTCCLK	8	8-17 8-21 8-22 8-23
t298	S4_STATE# inactive to SLP_S3# inactive (Consumer Only)	1	Note 16	RTCCLK	1	8-23
t298	S4_STATE# inactive to SLP_S3# inactive (Corporate Only)	1	—	RTCCLK	1	8-23
t299	S4 Wake Event to SLP_S4# inactive (S4 Wake)	See Note Below			8	8-17
t300	S3 Wake Event to SLP_S3# inactive (S3 Wake) (Consumer Only)	0	small as possible	RTCCLK	1	8-17
t300	S3 Wake Event to SLP_S3# inactive (S3 Wake) (Corporate Only)	0	—	RTCCLK	1	8-17
t301	S1 Wake Event to STPCLK# inactive	9		PCICLK		8-16
t302	SLP_M# inactive to SLP_S3# inactive		±10	ns		8-21
t304	RSMRST# deassertion to LAN_RST# deassertion	0		ms	17	

Table 8-22. Power Management Timings (Sheet 3 of 3)

Sym	Parameter	Min	Max	Units	Notes	Fig
t305a	LAN Power Rails active to LAN_RST# deassertion	1		ms	18	
t305b	LAN_RST# assertion to LAN Power Rails inactive	20		ns	25	
t306	LANRST# assertion to PWROK assertion	0		ms		
t307	SLP_S3# active to Vcc supplies inactive (nominal voltage -5%)	5		us	24	8-17
t308a	RSMRST# deassertion to CLPWROK assertion	0		ms		
t308b	Controller Link Power Rails active to CLPWROK assertion	1		ms		
t308c	CLPWROK assertion to PWROK assertion	0		ms		
Other Timings						
t310	THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active		175	ns		
t311	RSMRST# rising edge transition from 20% to 80%		50	µs		
t312	RSMRST# falling edge transition				21	
t313	SLP_M# active to RSMRST# active	500		µs		

NOTES:

1. These transitions are clocked off the internal RTC. 1 RTC clock is approximately from 28.992 µs to 32.044 µs.
2. The ICH10 STPCLK# assertion will trigger the processor to send a stop grant acknowledge cycle. The timing for this cycle getting to the ICH10 is dependant on the processor and the memory controller.
3. These transitions are clocked off the 33 MHz PCICLK. 1 PCICLK is approximately 30 ns.
4. The ICH10 has no maximum timing requirement for this transition. It is up to the system designer to determine if the SLP_S3#, SLP_S4# and SLP_S5# signals are used to control the power planes.
5. If the transition to S5 is due to Power Button Override, SLP_S3#, SLP_S4# and SLP_S5# are asserted together similar to timing t287 (PCIRST# active to SLP_S3# active).
6. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and RSMRST# inactive to SUSCLK toggling may be as much as 2.5 s.
7. This value is programmable in multiples of 1024 PCI CLKs. Maximum is 8192 PCI CLKs (245.6 µs).
8. The Min/Max times depend on the programming of the “SLP_S4# Minimum Assertion Width” and the “SLP_S4# Assertion Stretch Enable bits (D31:F0:A4h bits 5:3)”.
9. Note that this does not apply for synchronous SMIs.
10. This is a clock generator specification
11. If the (G)MCH does not have the CPUSLP# signal, then the minimum value can be 16 PCICLK.
12. This is non-zero to enforce the minimum assert time for DPRSLPVR. If the minimum assert time for DPRSLPVR has been met, then this is permitted to be 0.
13. This is non-zero to enforce the minimum assert time for STP_CPU#. If the minimum assert time for STP_CPU# has been met, then this is permitted to be 0.
14. This value should be at most a few clocks greater than the minimum.
15. When Intel AMT enabled, S4_STATE# indicates if system is in S4 state or below.
16. For t234 and t298, the SLP_M# stretching logic can push the Max value much larger than the Min (e.g., up to 3 seconds). With the installation of the Intel Manageability Engine

firmware, the Max value of t234 and t298 is 99 ms. Without the installation of the firmware, the Max value is 4 RTC clocks.

17. RSMRST# must de-assert at or before LAN_RST# de-assertion.
18. Measured from VccLAN3_3 or VccLAN1_1 power within voltage specification (which ever is later in time) to LAN_RST# = (Vih+Vil)/2. It is acceptable to use an RC circuit sourced from VccLAN3_3 to create LAN_RST#. The rising edge of LAN_RST# needs to be a clean, monotonic edge for frequency content below 10 MHz.
19. If Integrated LAN is supported, LAN_RST# must be de-asserted at or before PWROK assertion.
20. If Integrated LAN is not supported, LAN_RST# should be tied to ground and must never de-assert.
21. RSMRST# falling edge must transition to 0.8 V or less before VccSus3_3 drops to 2.1 V
22. If bit 0 of Section 13.8.1.3 is set to a 1, SLP_S5# will not be de-asserted until a wake event is detected. If bit 0 is set to 0, SLP_S5# will de-assert within the specification listed in the table.
23. t294 is not applied to V5REF. V5REF timings are bounded by power sequencing. t294 applies during S0 to S3/S4/S5 and S0 to G3 transitions.
24. t307 is applicable in S0 to Sx transitions.
25. A Power rail is considered to be inactive when the rail is at its nominal voltage minus 5% or less.

8.5 Timing Diagrams

Figure 8-1. Clock Timing

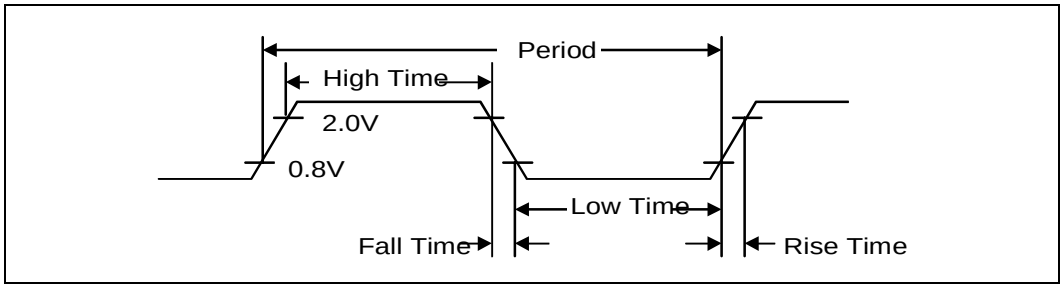


Figure 8-2. Valid Delay from Rising Clock Edge

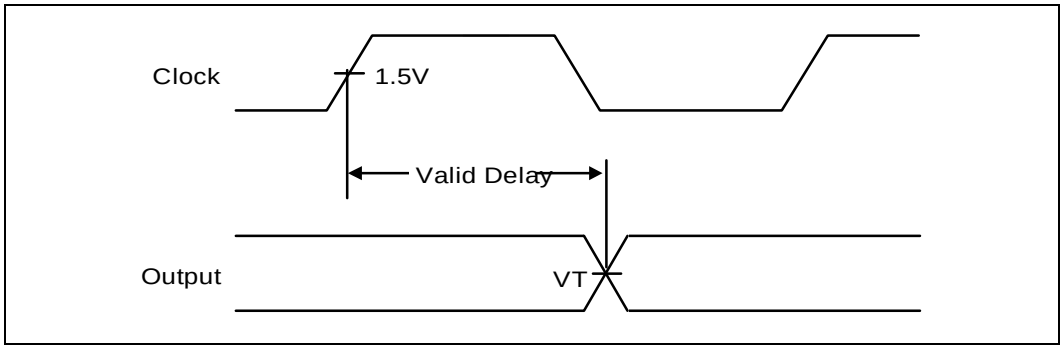


Figure 8-3. Setup and Hold Times

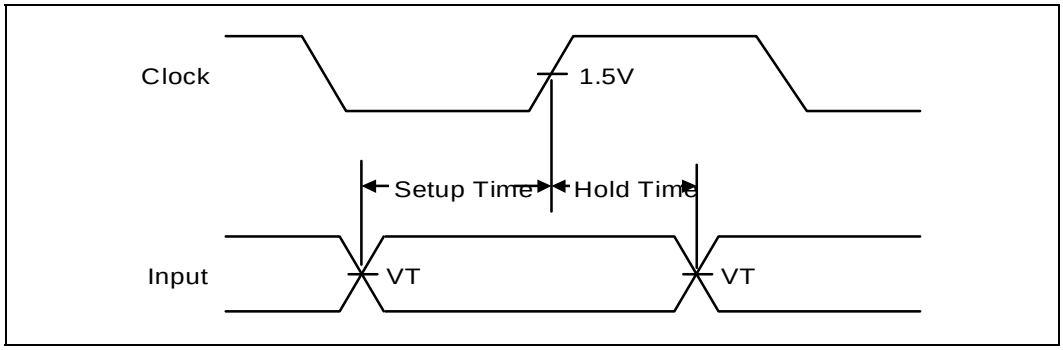


Figure 8-4. Float Delay

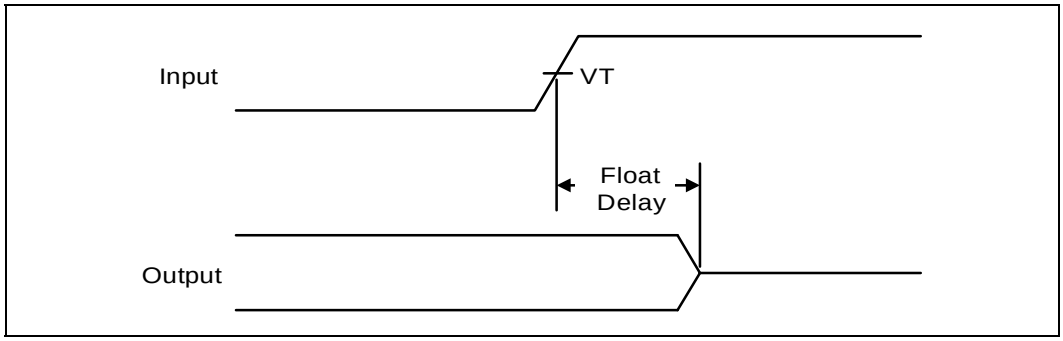


Figure 8-5. Pulse Width

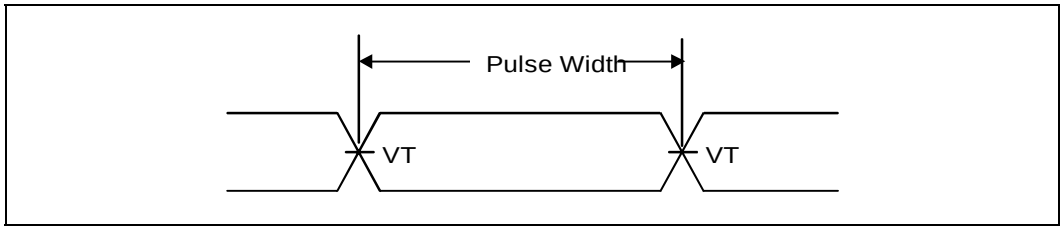


Figure 8-6. Output Enable Delay

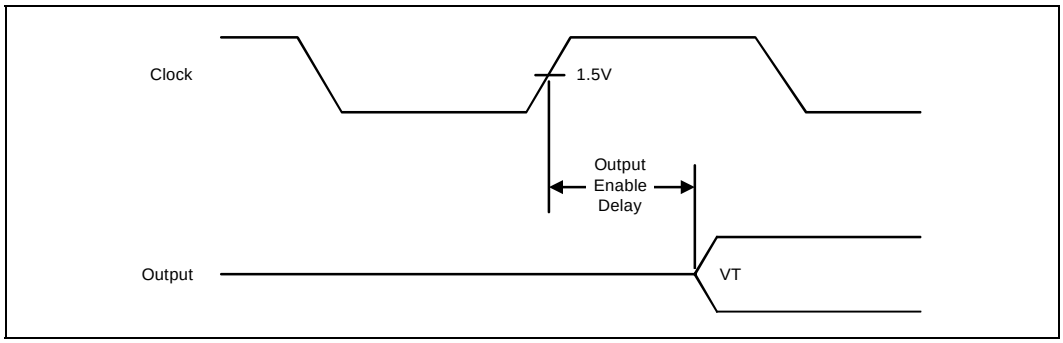


Figure 8-7. USB Rise and Fall Times

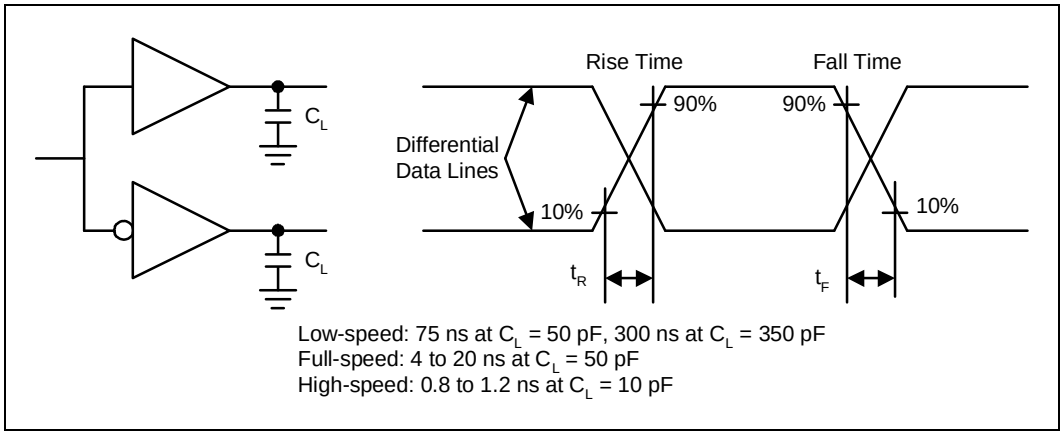


Figure 8-8. USB Jitter

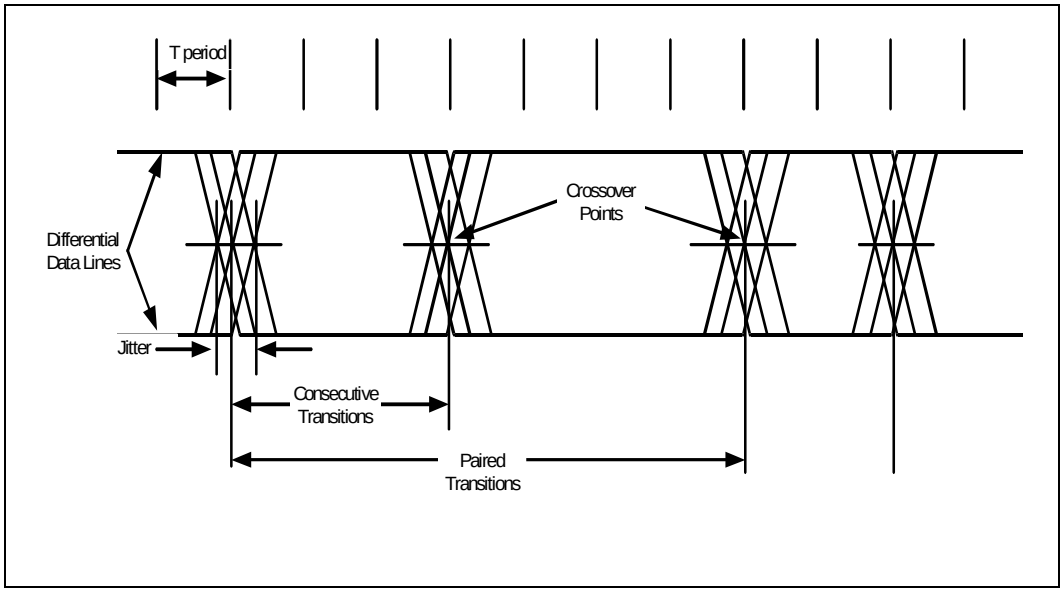


Figure 8-9. USB EOP Width

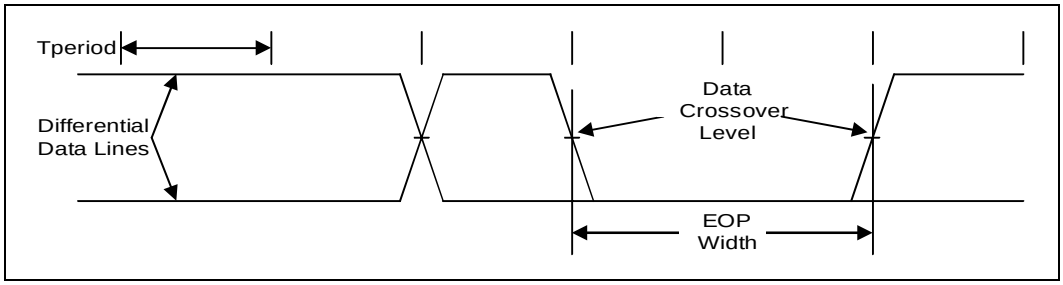


Figure 8-10. SMBus Transaction

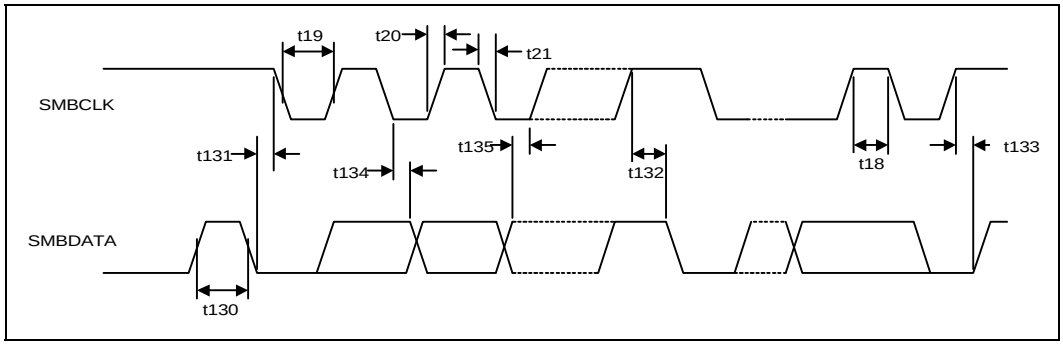


Figure 8-11. SMBus Timeout

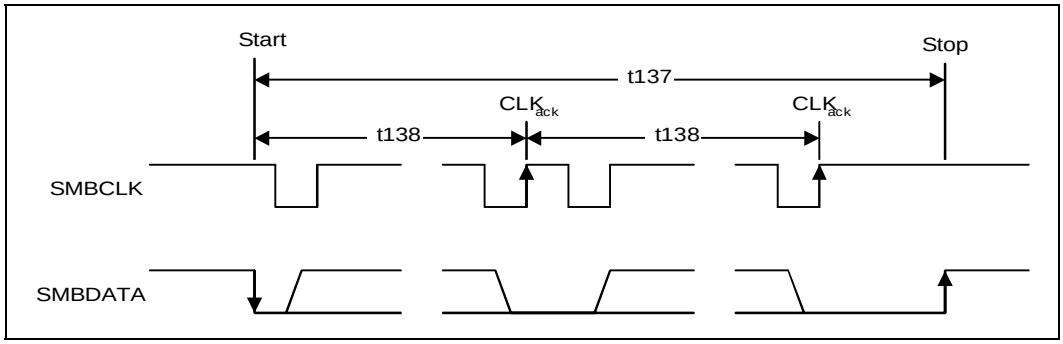


Figure 8-12. SPI Timings

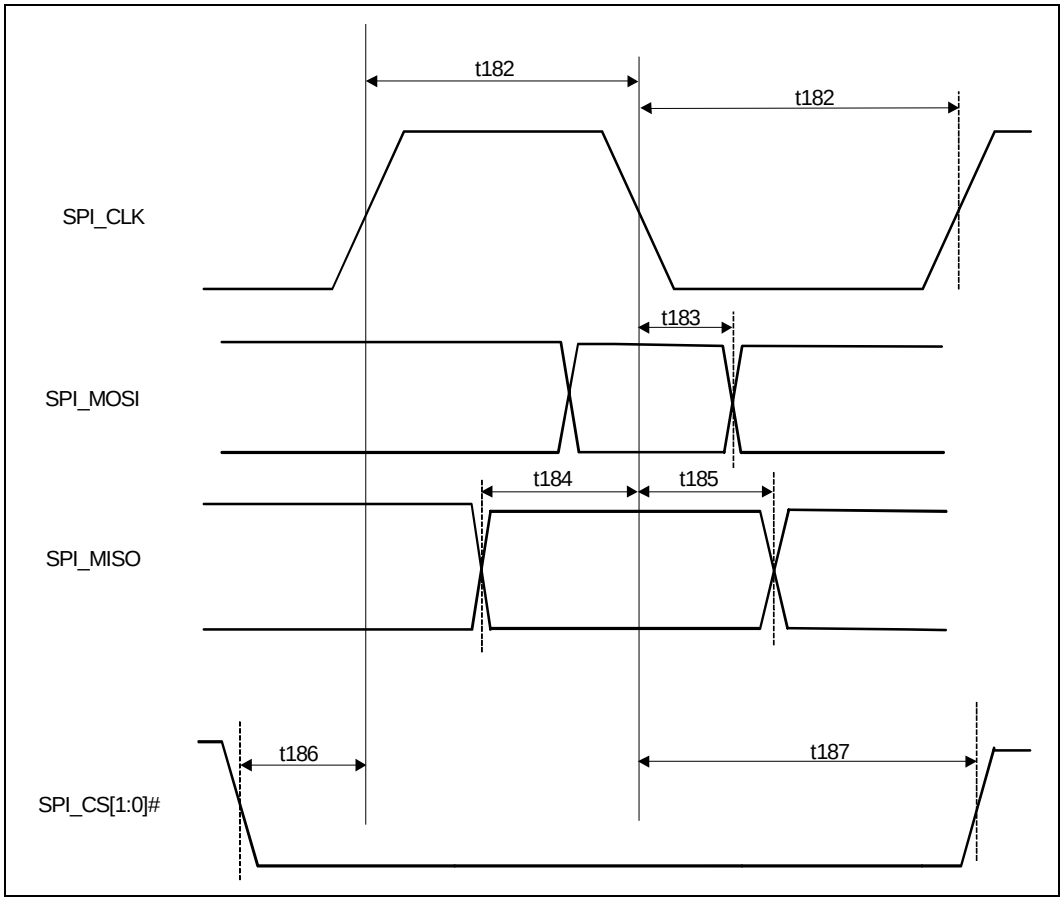


Figure 8-13. Intel® High Definition Audio Input and Output Timings

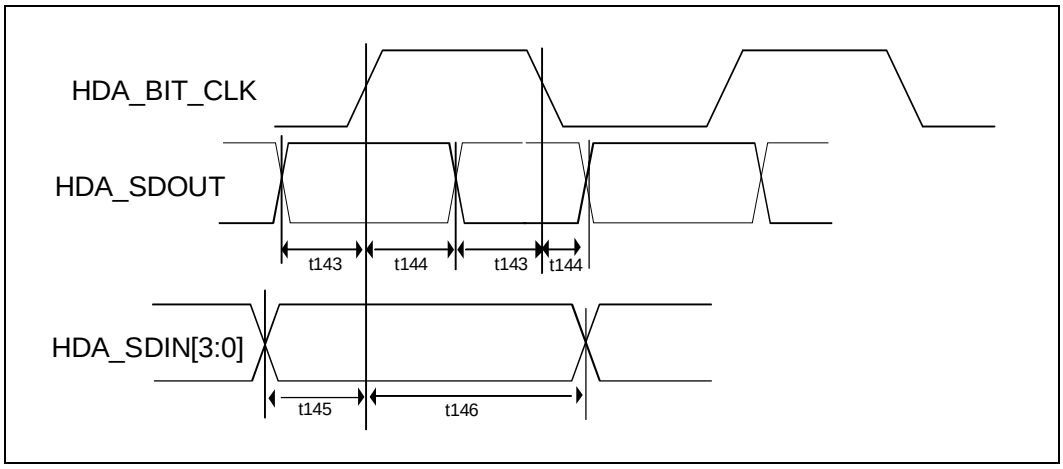
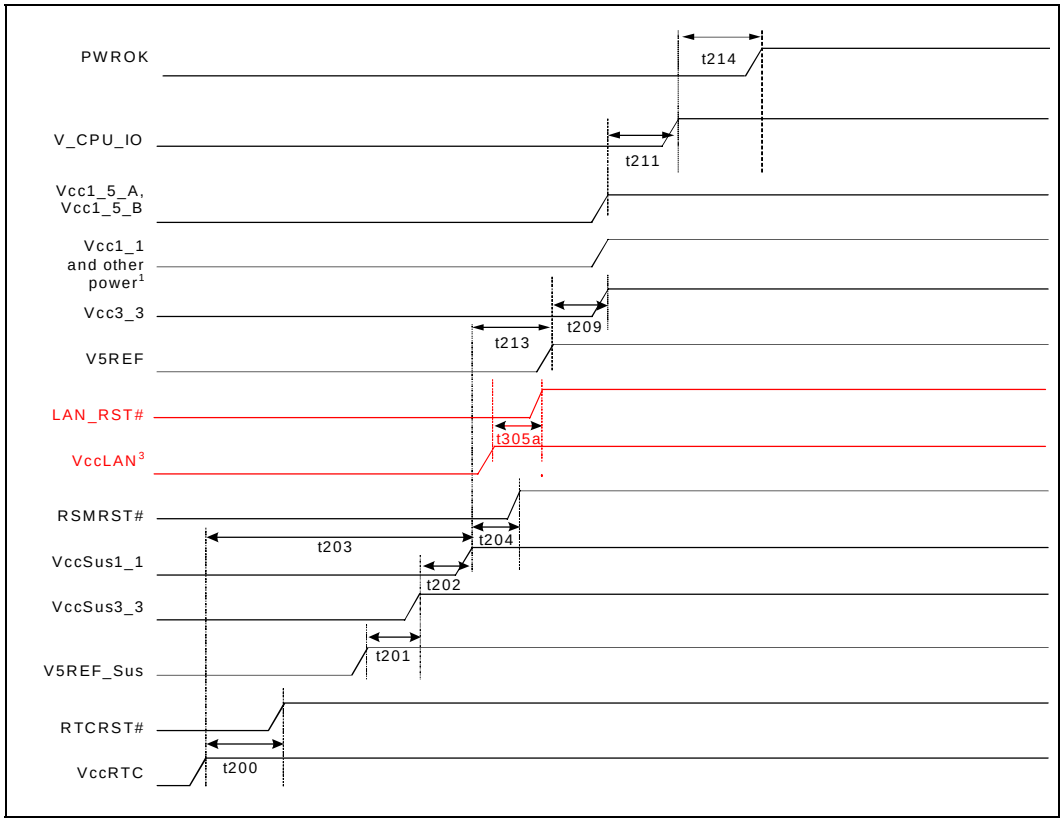


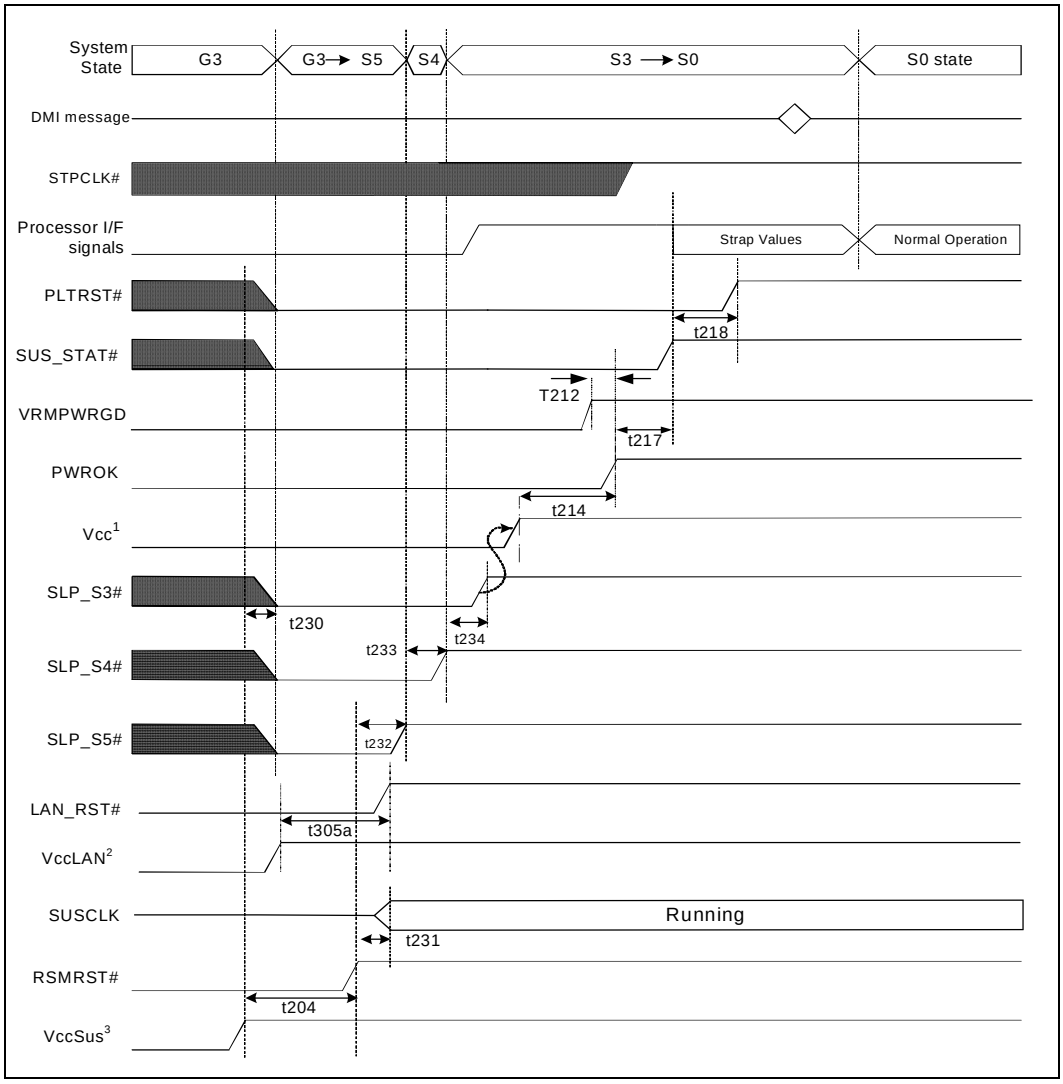
Figure 8-14. Power Sequencing and Reset Signal Timings



NOTES:

1. Other power includes VccUSBPLL, VccDMIPLL, and VccSATAPLL. All of these power signals must independently meet the timings shown in the figure. There are no timing interdependencies between Vcc1_1 and these other power signals. There are also no timing interdependencies for these power signals, including Vcc1_1, to Vcc3_3 and Vcc1_5_A/Vcc1_5_B.
2. PWROK must not glitch, even if RSMRST# is low.
3. VccLAN includes VccLAN3_3, VccLAN1_1, and VccCL3_3.
4. Other power

Figure 8-15. G3 (Mechanical Off) to S0 Timings



NOTE:

1. Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_1, VccUSBPLL, VccDMIPLL, VccSATAPLL, V5REF, V_CPU_IO, VccDMI, VccHDA, VccGLANPLL, VccGLAN3_3 and VccGLAN1_5 (if integrated Gigabit LAN enabled), VccLAN3_3 (if LAN only power in S0), and VccCL3_3 (if controller link only powered in S0).
2. VccLAN includes VccLAN3_3, VccLAN1_1, and VccCL3_3.
3. VccSus includes VccSus3_3, V5REF_Sus, VccSusHDA, VccLAN3_3 (if LAN powered in S3/S4/S5), and VccCL3_3 (if controller link powered in S3/S4/S5).

Figure 8-16. S0 to S1 to S0 Timings

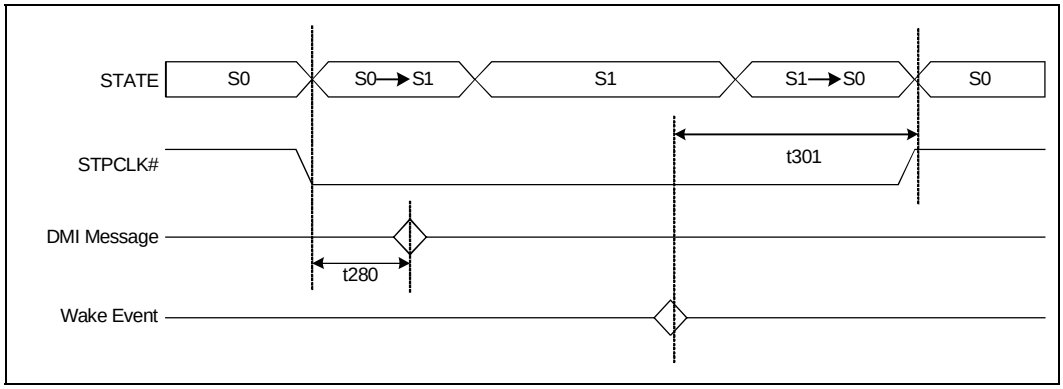
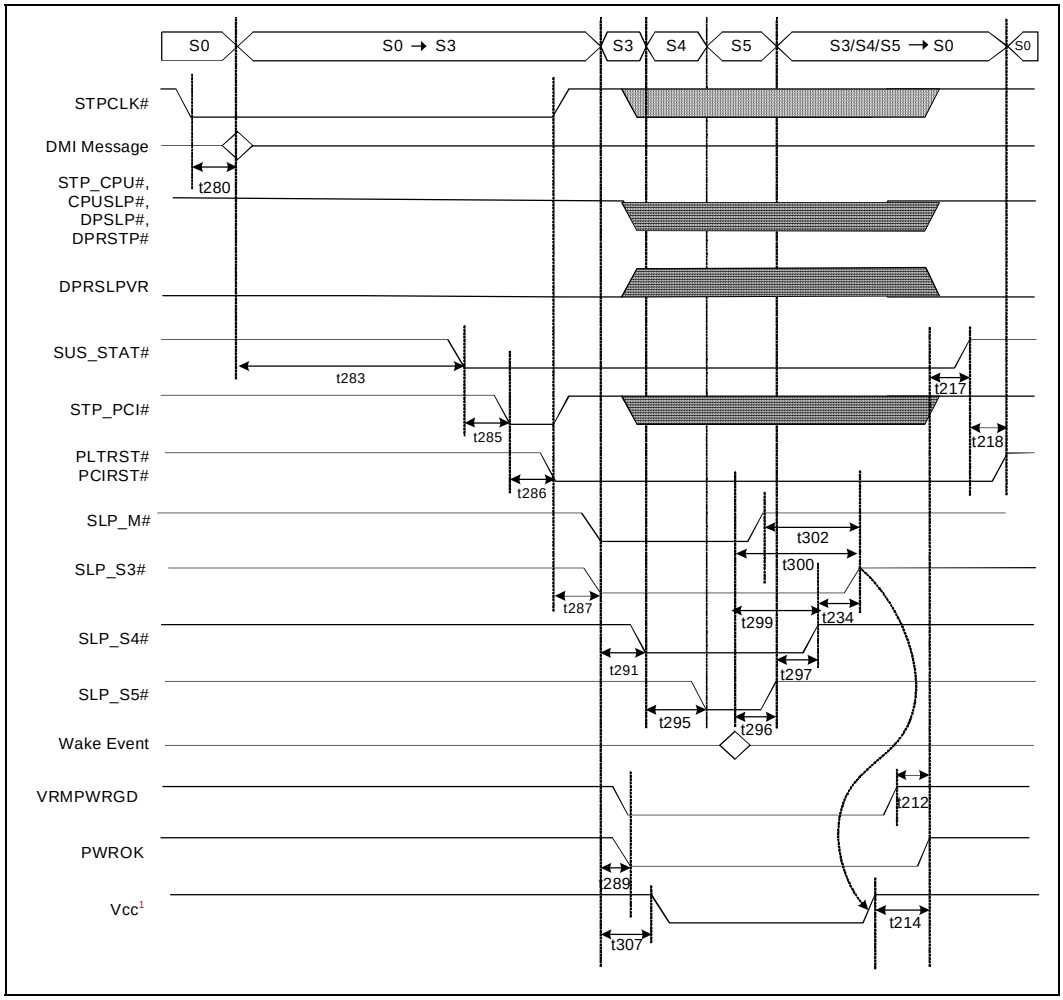


Figure 8-17. S0 to S5 to S0 Timings



NOTE: Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_1, VccUSBPLL, VccDMIPLL, and VccSATAPLL.

Figure 8-18. C0 to C2 to C0 Timings

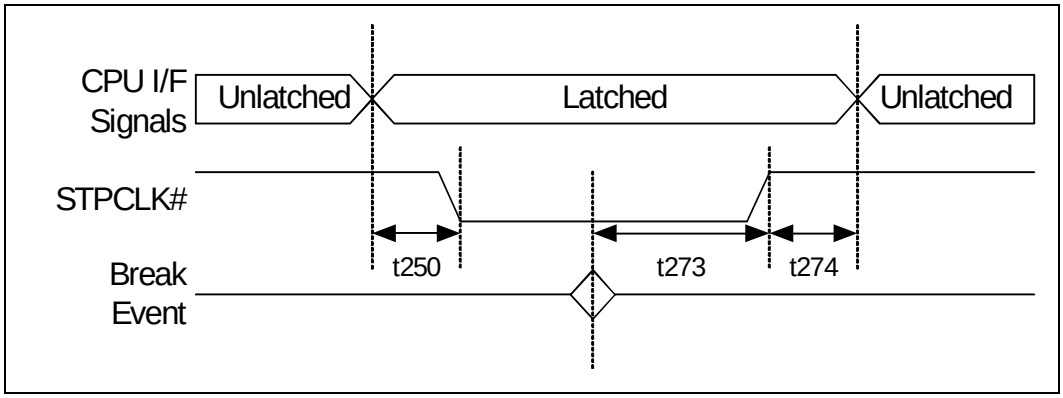


Figure 8-19. C0 to C3 to C0 Timings

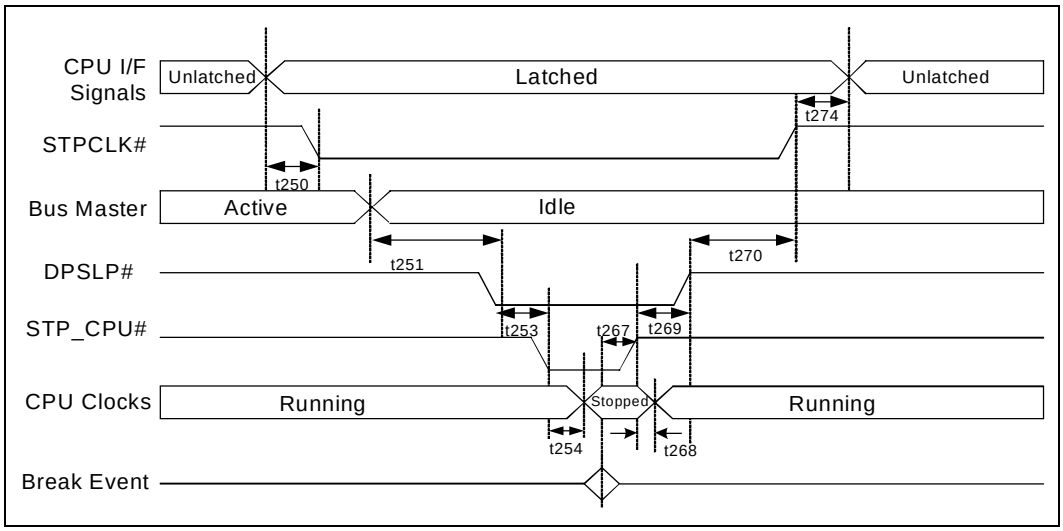


Figure 8-20. C0 to C4 to C0 Timings

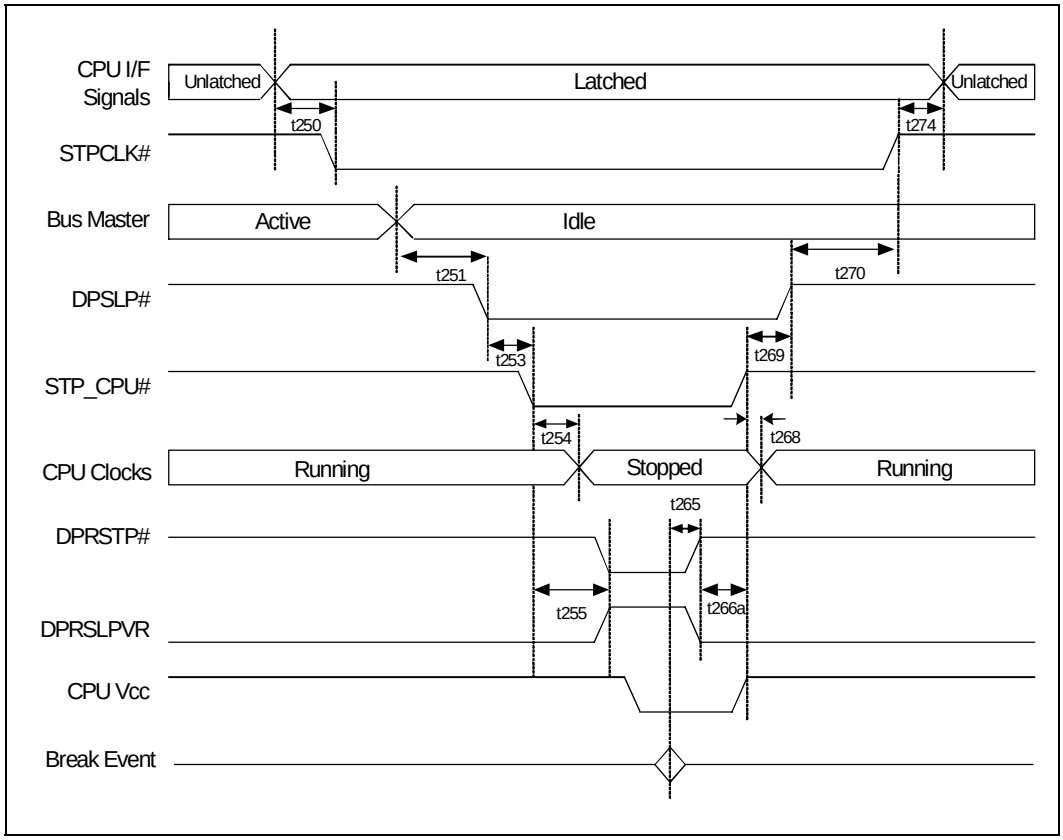
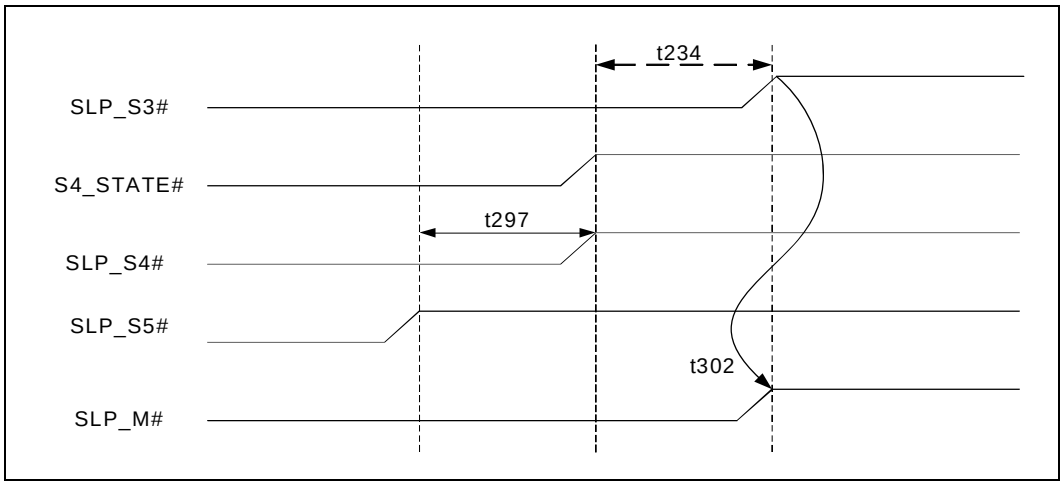


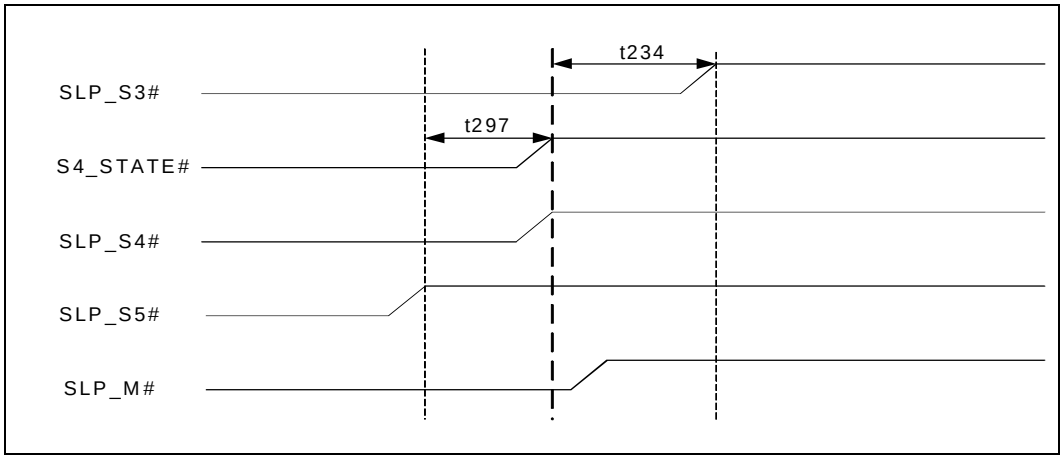
Figure 8-21. Sleep control signal relationship - Host boots and Intel Management Engine off



NOTES:

1. t290 is also applicable when the system transitions from S0 to G3.

Figure 8-22. Sleep control signal relationship - Host and Intel Management Engine boot after G3



NOTE: When both the host and Intel Management Engine boot after G3, SLP_M# does not have any timing dependency on other sleep control signals. SLP_M# will be de-asserted some time between SLP_S5# de-assertion and SLP_S3# de-assertion.

Figure 8-23. Sleep control signal relationship - Host stays in S5 and Intel Management Engine boots after G3

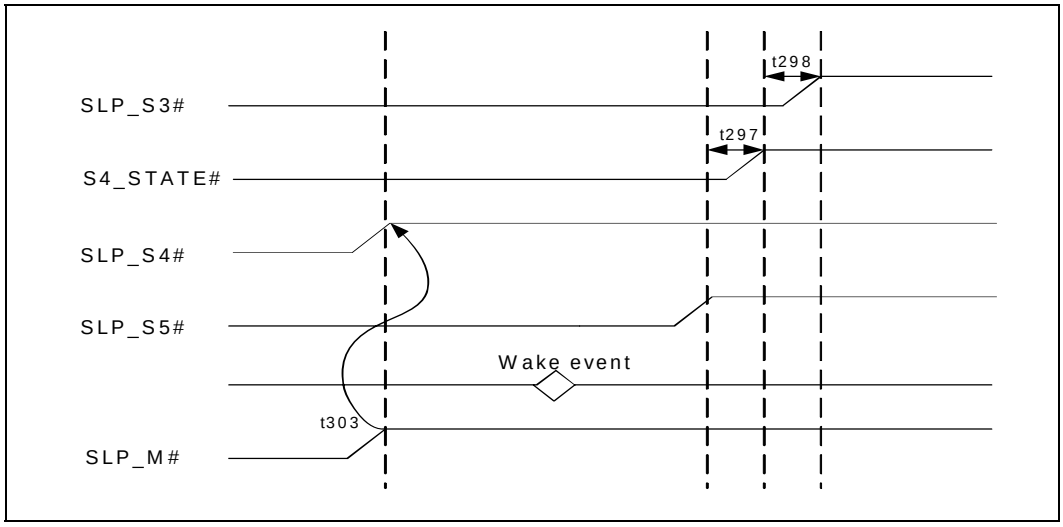
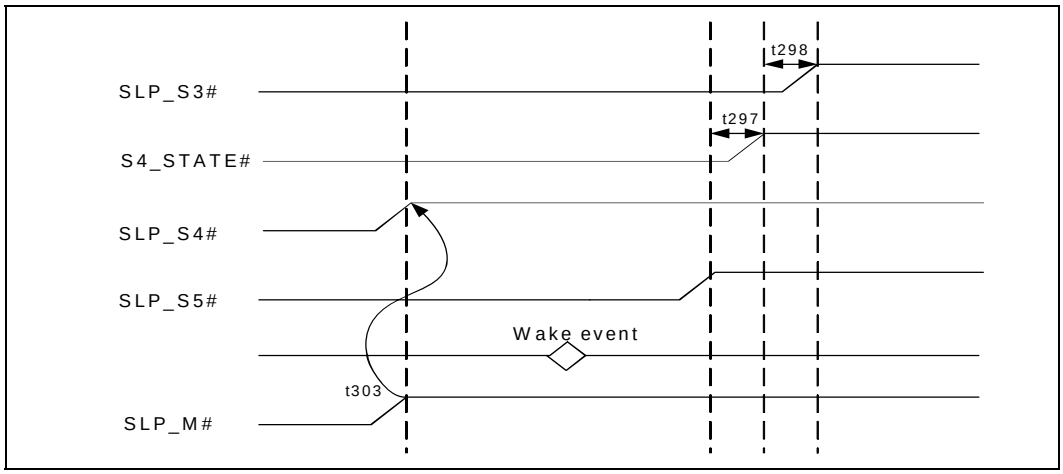
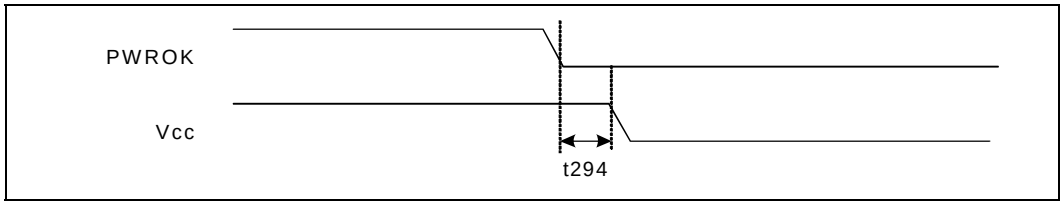


Figure 8-24. S4, S5 / M1 to S0 / M0



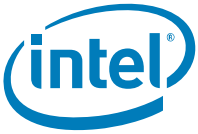
NOTE: Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_1, VccUSBPLL, VccDMIPLL, and VccSATAPLL.

Figure 8-25. S0 to S3 / S4 / S5 and G3 Timings



§ §

§ §



9 Register and Memory Mapping

The ICH10 contains registers that are located in the processor's I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes the ICH10 I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and Individual register bit descriptions are provided in the following chapters. The following notations and definitions are used in the register/instruction description chapters.

RO	Read Only. In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only. In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R/W	Read/Write. A register with this attribute can be read and written.
R/WC	Read/Write Clear. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
R/WO	Read/Write-Once. A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once. A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Reserved	The value of reserved bits must never be changed. For details see **Section 9.2**.
Default	When ICH10 is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the ICH10 registers accordingly.
Bold	Register bits that are highlighted in bold text indicate that the bit is implemented in the ICH10. Register bits that are not implemented or are hardwired will remain in plain text.

9.1 PCI Devices and Functions

The Intel ICH10 incorporates a variety of PCI devices and functions, as shown in Table 9-1. There are seven logical devices for consumer components, and 8 logical devices for Corporate components. The first is the DMI-To-PCI bridge (Device 30). The second device (Device 31) contains most of the standard PCI functions that always existed in the PCI-to-ISA bridges (South Bridges), such as the Intel PIIX4. The third and fourth (Device 29 and Device 26) are the USB and USB2 host controller devices. The fifth (Device 28) is PCI Express device. The sixth (Device 27) is HD Audio controller device. The seventh (Device 25) is the Gigabit Ethernet controller device.

If for some reason, the particular system platform does not want to support any one of the Device Functions, with the exception of D30:F0, they can individually be disabled. The integrated Gigabit Ethernet controller will be disabled if no Platform LAN Connect component is detected (See Chapter 5.3). When a function is disabled, it does not appear at all to the software. A disabled function will not respond to any register reads or writes, insuring that these devices appear hidden to software.

Table 9-1. PCI Devices and Functions

Bus:Device:Function	Function Description
Bus 0:Device 30:Function 0	PCI-to-PCI Bridge
Bus 0:Device 31:Function 0	LPC Controller[1]
Bus 0:Device 31:Function 2	SATA Controller #1
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 31:Function 5	SATA Controller #2[3]
Bus 0:Device 31:Function 6	Thermal Subsystem
Bus 0:Device 29:Function 0	USB UHCI Controller #1
Bus 0:Device 29:Function 1	USB UHCI Controller #2
Bus 0:Device 29:Function 2	USB UHCI Controller #3
Bus 0:Device 29:Function 3	USB UHCI Controller #6[2]
Bus 0:Device 29:Function 7	USB EHCI Controller #1
Bus 0:Device 26:Function 0	USB UCHI Controller #4
Bus 0:Device 26:Function 1	USB UHCI Controller #5
Bus 0:Device 26:Function 2	USB UHCI Controller #6[2]
Bus 0:Device 26:Fucntion 7	USB EHCI Controller #2
Bus 0:Device 28:Function 0	PCI Express* Port 1
Bus 0:Device 28:Function 1	PCI Express Port 2
Bus 0:Device 28:Function 2	PCI Express Port 3
Bus 0:Device 28:Function 3	PCI Express Port 4
Bus 0:Device 28:Function 4	PCI Express Port 5
Bus 0:Device 28:Function 5	PCI Express Port 6
Bus 0:Device 27:Function 0	Intel® High Definition Audio Controller
Bus 0:Device 25:Function 0	Gigabit Ethernet Controller

NOTES:
1. The PCI-to-LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, and DMA.

2. The ICH10 can optionally configure the USB ports from a 6-6 configuration into a 8-4 configuration, with 8 ports on D29:F7 EHCI and 4 ports on D26:F7 EHCI. In the 8-4 configuration UHCI #6 will be mapped to D29:F3. In the 6-6 configuration UHCI #6 will be mapped to D26:F2.
3. SATA controller 2 (D31:F5) is only visible in ICH10 desktop components and when D31:F2 CC.SCC=01h.

9.2 PCI Configuration Map

Each PCI function on the ICH10 has a set of PCI configuration registers. The register address map tables for these register sets are included at the beginning of the chapter for the particular function.

Configuration Space registers are accessed through configuration cycles on the PCI bus by the Host bridge using configuration mechanism #1 detailed in the *PCI Local Bus Specification, Revision 2.3*.

Some of the PCI registers contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the configuration space contains reserved locations. Software should not write to reserved PCI configuration locations in the device-specific region (above address offset 3Fh).

9.3 I/O Map

The I/O map is divided into Fixed and Variable address ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

9.3.1 Fixed I/O Address Ranges

Table 9-2 shows the Fixed I/O decode ranges from the processor perspective. Note that for each I/O range, there may be separate behavior for reads and writes. DMI (Direct Media Interface) cycles that go to target ranges that are marked as “Reserved” will not be decoded by the ICH10, and will be passed to PCI unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0). If a PCI master targets one of the fixed I/O target ranges, it will be positively decoded by the ICH10 in medium speed.

Address ranges that are not listed or marked “Reserved” are **not** decoded by the ICH10 (unless assigned to one of the variable ranges).

Table 9-2. Fixed I/O Ranges Decoded by Intel® ICH10 (Sheet 1 of 2)

I/O Address	Read Target	Write Target	Internal Unit
00h–08h	DMA Controller	DMA Controller	DMA
09h–0Eh	RESERVED	DMA Controller	DMA
0Fh	DMA Controller	DMA Controller	DMA
10h–18h	DMA Controller	DMA Controller	DMA
19h–1Eh	RESERVED	DMA Controller	DMA
1Fh	DMA Controller	DMA Controller	DMA
20h–21h	Interrupt Controller	Interrupt Controller	Interrupt
24h–25h	Interrupt Controller	Interrupt Controller	Interrupt
28h–29h	Interrupt Controller	Interrupt Controller	Interrupt
2Ch–2Dh	Interrupt Controller	Interrupt Controller	Interrupt
2E–2F	LPC SIO	LPC SIO	Forwarded to LPC
30h–31h	Interrupt Controller	Interrupt Controller	Interrupt
34h–35h	Interrupt Controller	Interrupt Controller	Interrupt
38h–39h	Interrupt Controller	Interrupt Controller	Interrupt
3Ch–3Dh	Interrupt Controller	Interrupt Controller	Interrupt
40h–42h	Timer/Counter	Timer/Counter	PIT (8254)
43h	RESERVED	Timer/Counter	PIT
4E–4F	LPC SIO	LPC SIO	Forwarded to LPC
50h–52h	Timer/Counter	Timer/Counter	PIT
53h	RESERVED	Timer/Counter	PIT
60h	Microcontroller	Microcontroller	Forwarded to LPC
61h	NMI Controller	NMI Controller	Processor I/F
62h	Microcontroller	Microcontroller	Forwarded to LPC
64h	Microcontroller	Microcontroller	Forwarded to LPC
66h	Microcontroller	Microcontroller	Forwarded to LPC
70h	RESERVED	NMI and RTC Controller	RTC
71h	RTC Controller	RTC Controller	RTC
72h	RTC Controller	NMI and RTC Controller	RTC
73h	RTC Controller	RTC Controller	RTC
74h	RTC Controller	NMI and RTC Controller	RTC
75h	RTC Controller	RTC Controller	RTC
76h	RTC Controller	NMI and RTC Controller	RTC
77h	RTC Controller	RTC Controller	RTC
80h	DMA Controller, or LPC, or PCI	DMA Controller and LPC or PCI	DMA
81h–83h	DMA Controller	DMA Controller	DMA

Table 9-2. Fixed I/O Ranges Decoded by Intel® ICH10 (Sheet 2 of 2)

I/O Address	Read Target	Write Target	Internal Unit
84h–86h	DMA Controller	DMA Controller and LPC or PCI	DMA
87h	DMA Controller	DMA Controller	DMA
88h	DMA Controller	DMA Controller and LPC or PCI	DMA
89h–8Bh	DMA Controller	DMA Controller	DMA
8Ch–8Eh	DMA Controller	DMA Controller and LPC or PCI	DMA
08Fh	DMA Controller	DMA Controller	DMA
90h–91h	DMA Controller	DMA Controller	DMA
92h	Reset Generator	Reset Generator	Processor I/F
93h–9Fh	DMA Controller	DMA Controller	DMA
A0h–A1h	Interrupt Controller	Interrupt Controller	Interrupt
A4h–A5h	Interrupt Controller	Interrupt Controller	Interrupt
A8h–A9h	Interrupt Controller	Interrupt Controller	Interrupt
ACh–ADh	Interrupt Controller	Interrupt Controller	Interrupt
B0h–B1h	Interrupt Controller	Interrupt Controller	Interrupt
B2h–B3h	Power Management	Power Management	Power Management
B4h–B5h	Interrupt Controller	Interrupt Controller	Interrupt
B8h–B9h	Interrupt Controller	Interrupt Controller	Interrupt
BCh–BDh	Interrupt Controller	Interrupt Controller	Interrupt
C0h–D1h	DMA Controller	DMA Controller	DMA
D2h–DDh	RESERVED	DMA Controller	DMA
DEh–DFh	DMA Controller	DMA Controller	DMA
F0h	PCI and Master Abort[1]	FERR#/IGNNE# / Interrupt Controller	Processor I/F
170h–177h	SATA Controller or PCI	SATA Controller or PCI	Forwarded to SATA
1F0h–1F7h	SATA Controller or PCI	SATA Controller or PCI	Forwarded to SATA
376h	SATA Controller or PCI	SATA Controller or PCI	Forwarded to SATA
3F6h	SATA Controller or PCI	SATA Controller or PCI	Forwarded to SATA
4D0h–4D1h	Interrupt Controller	Interrupt Controller	Interrupt
CF9h	Reset Generator	Reset Generator	Processor I/F

NOTE:
1. A read to this address will subtractively go to PCI, where it will master abort.

9.3.2 Variable I/O Decode Ranges

Table 9-3 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various PCI configuration spaces. The PNP software (PCI or ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The Variable I/O Ranges should not be set to conflict with the Fixed I/O Ranges. Unpredictable results if the configuration software allows conflicts to occur. The ICH10 does not perform any checks for conflicts.

Table 9-3. Variable I/O Decode Ranges

Range Name	Mappable	Size (Bytes)	Target
ACPI	Anywhere in 64 KB I/O Space	64	Power Management
IDE Bus Master	Anywhere in 64 KB I/O Space	16	IDE Unit
Native IDE Command	Anywhere in 64 KB I/O Space	8	IDE Unit
Native IDE Control	Anywhere in 64 KB I/O Space	4	IDE Unit
USB UHCI Controller #1	Anywhere in 64 KB I/O Space	32	USB Unit 1
USB UHCI Controller #2	Anywhere in 64 KB I/O Space	32	USB Unit 2
USB UHCI Controller #3	Anywhere in 64 KB I/O Space	32	USB Unit 3
USB UHCI Controller #4	Anywhere in 64 KB I/O Space	32	USB Unit 4
USB UHCI Controller #5	Anywhere in 64 KB I/O Space	32	USB Unit 5
USB UHCI Controller #6	Anywhere in 64 KB I/O Space	32	USB Unit 6
SMBus	Anywhere in 64 KB I/O Space	32	SMB Unit
TCO	96 Bytes above ACPI Base	32	TCO Unit
GPIO	Anywhere in 64 KB I/O Space	64	GPIO Unit
Parallel Port	3 Ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 1	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 2	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Floppy Disk Controller	2 Ranges in 64 KB I/O Space	8	LPC Peripheral
LAN	Anywhere in 64 KB I/O Space	32	LAN Unit
LPC Generic 1	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 2	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 3	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 4	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
I/O Trapping Ranges	Anywhere in 64 KB I/O Space	1 to 256	Trap on Backbone

NOTE:
1. Decode range size determined by D31:F0:ADh:bits 5:4

9.4 Memory Map

Table 9-4 shows (from the processor perspective) the memory ranges that the ICH10 decodes. Cycles that arrive from DMI that are not directed to any of the internal memory targets that decode directly from DMI will be driven out on PCI unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0).

PCI cycles generated by external PCI masters will be positively decoded unless they fall in the PCI-to-PCI bridge memory forwarding ranges (those addresses are reserved for PCI peer-to-peer traffic). If the cycle is not in the internal LAN controller's range, it will be forwarded up to DMI. Software must not attempt locks to the ICH10's memory-mapped I/O ranges for EHCI and HPET. If attempted, the lock is not honored which means potential deadlock conditions may occur.

Table 9-4. Memory Decode Ranges from Processor Perspective (Sheet 1 of 2)

Memory Range	Target	Dependency/Comments
0000 0000h–000D FFFFh 0010 0000h–TOM (Top of Memory)	Main Memory	TOM registers in Host controller
000E 0000h–000E FFFFh	Firmware Hub	Bit 6 in Firmware Hub Decode Enable register is set
000F 0000h–000F FFFFh	Firmware Hub	Bit 7 in Firmware Hub Decode Enable register is set
FEC_ _000h–FEC_ _040h (Corporate Only)	IO(x) APIC inside ICH10	_ _is controlled via APIC Range Select (ASEL) field and APIC Enable (AEN) bit
FEC0 _000h–FEC0 _040h (Consumer Only)	IO(x) APIC inside ICH10	_ is controlled via APIC Range Select (ASEL) field and APIC Enable (AEN) bit
FEC1 0000h–FEC1 7FFF	PCI Express* Port 1	PCI Express* Root Port 1 I/OxAPIC Enable (PAE) set
FEC1 8000h–FEC1 8FFFh	PCI Express* Port 2	PCI Express* Root Port 2 I/OxAPIC Enable (PAE) set
FEC2 0000h–FEC2 7FFFh	PCI Express* Port 3	PCI Express* Root Port 3 I/OxAPIC Enable (PAE) set
FEC2 8000h–FEC2 8FFFh	PCI Express* Port 4	PCI Express* Root Port 4 I/OxAPIC Enable (PAE) set
FEC3 0000h–FEC3 7FFFh	PCI Express* Port 5	PCI Express* Root Port 5 I/OxAPIC Enable (PAE) set
FEC3 8000h–FEC3 8FFFh	PCI Express* Port 6	PCI Express* Root Port 6 I/OxAPIC Enable (PAE) set
FED4 0000h–FED4 BFFFh	TPM on LPC	
FFC0 0000h–FFC7 FFFFh FF80 0000h–FF87 FFFFh	Firmware Hub (or PCI)[2]	Bit 8 in Firmware Hub Decode Enable register is set
FFC8 0000h–FFCF FFFFh FF88 0000h–FF8F FFFFh	Firmware Hub (or PCI)[2]	Bit 9 in Firmware Hub Decode Enable register is set
FFD0 0000h–FFD7 FFFFh FF90 0000h–FF97 FFFFh	Firmware Hub (or PCI)[2]	Bit 10 in Firmware Hub Decode Enable register is set
FFD8 0000h–FFDF FFFFh FF98 0000h–FF9F FFFFh	Firmware Hub (or PCI)[2]	Bit 11 in Firmware Hub Decode Enable register is set

Table 9-4. Memory Decode Ranges from Processor Perspective (Sheet 2 of 2)

Memory Range	Target	Dependency/Comments
FFE0 000h–FFE7 FFFFh FFA0 0000h–FFA7 FFFFh	Firmware Hub (or PCI)[2]	Bit 12 in Firmware Hub Decode Enable register is set
FFE8 0000h–FFEF FFFFh FFA8 0000h–FFAF FFFFh	Firmware Hub (or PCI)[3]	Bit 13 in Firmware Hub Decode Enable register is set
FFF0 0000h–FFF7 FFFFh FFB0 0000h–FFB7 FFFFh	Firmware Hub (or PCI)[2]	Bit 14 in Firmware Hub Decode Enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	Firmware Hub (or PCI)[2]	Always enabled. The top two, 64 KB blocks of this range can be swapped, as described in Section 7.4.1.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	Firmware Hub (or PCI)[2]	Bit 3 in Firmware Hub Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	Firmware Hub (or PCI)[2]	Bit 2 in Firmware Hub Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	Firmware Hub (or PCI)[2]	Bit 1 in Firmware Hub Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	Firmware Hub (or PCI)[2]	Bit 0 in Firmware Hub Decode Enable register is set
128 KB anywhere in 4-GB range	Integrated LAN Controller	Enable via BAR in Device 25:Function 0 (Integrated LAN Controller)
1 KB anywhere in 4-GB range	USB EHCI Controller #1[1]	Enable via standard PCI mechanism (Device 29, Function 7)
1 KB anywhere in 4-GB range	USB EHCI Controller #2[1]	Enable via standard PCI mechanism (Device 26, Function 7)
512 B anywhere in 64-bit addressing space	Intel® High Definition Audio Host Controller	Enable via standard PCI mechanism (Device 27, Function 0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers [1]	BIOS determines the “fixed” location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
All other	PCI	None

NOTES:
1. Software must not attempt locks to memory mapped I/O ranges for USB EHCI or High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.
2. PCI is the target when the Boot BIOS Destination selection bits are set to 10b (Chipset Config Registers:Offset 3401 bits 11:10). When PCI selected, the Firmware Hub Decode Enable bits have no effect.

9.4.1 Boot-Block Update Scheme

The ICH10 supports a “top-block swap” mode that has the ICH10 swap the top block in the Firmware Hub (the boot block) with another location. This allows for safe update of the Boot Block (even if a power failure occurs). When the “TOP_SWAP” Enable bit is set, the ICH10 will invert A16 for cycles targeting Firmware Hub space. When this bit is 0, the ICH10 will not invert A16. This bit is automatically set to 0 by RTCRST#, but not by PLTRST#.

The scheme is based on the concept that the top block is reserved as the “boot” block, and the block immediately below the top block is reserved for doing boot-block updates.

The algorithm is:

1. Software copies the top block to the block immediately below the top
2. Software checks that the copied block is correct. This could be done by performing a checksum calculation.
3. Software sets the TOP_SWAP bit. This will invert A16 for cycles going to the Firmware Hub. processor access to FFFF_0000h through FFFF_FFFFh will be directed to FFFE_0000h through FFFE_FFFFh in the Firmware Hub, and processor accesses to FFFE_0000h through FFFE_FFFF will be directed to FFFF_0000h through FFFF_FFFFh.
4. Software erases the top block
5. Software writes the new top block
6. Software checks the new top block
7. Software clears the TOP_SWAP bit
8. Software sets the Top_Swap Lock-Down bit

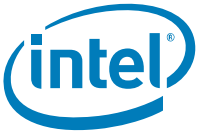
If a power failure occurs at any point after step 3, the system will be able to boot from the copy of the boot block that is stored in the block below the top. This is because the TOP_SWAP bit is backed in the RTC well.

Note: The top-block swap mode may be forced by an external strapping option (See Section 2.25.1). When top-block swap mode is forced in this manner, the TOP_SWAP bit cannot be cleared by software. A re-boot with the strap removed will be required to exit a forced top-block swap mode.

Note: Top-block swap mode only affects accesses to the Firmware Hub space, not feature space.

Note: The top-block swap mode has no effect on accesses below FFFE_0000h.

§ §



10 Chipset Configuration Registers

This section describes all registers and base functionality that is related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express*). It contains the root complex register block, which describes the behavior of the upstream internal link.

This block is mapped into memory space, using the Root Complex Base Address (RCBA) register of the PCI-to-LPC bridge. Accesses in this space must be limited to 32-(DW) bit quantities. Burst accesses are not allowed.

All Chipset Configuration Registers are located in the core well unless otherwise indicated.

10.1 Chipset Configuration Registers (Memory Space)

Note: Address locations that are not shown should be treated as Reserved (see Section 9.2 for details).

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 1 of 4)

Offset	Mnemonic	Register Name	Default	Type
0000–0003h	VCH	Virtual Channel Capability Header	10010002h	R/WO
0004–0007h	VCAP1	Virtual Channel Capability #1	00000801h	RO, R/WO
0008–000Bh	VCAP2	Virtual Channel Capability #2	00000001h	RO
000C–000Dh	PVC	Port VC Control	0000h	RO, R/W
000E–000Fh	PVS	Port VC Status	0000h	RO
0010–0013h	V0CAP	VC 0 Resource Capability	00000001h	RO
0014–0017h	V0CTL	VC 0 Resource Control	800000FFh	R/W, RO
001A–001Bh	V0STS	VC 0 Resource Status	0000h	RO
001C–001Fh	V1CAP	VC 1 Resource Capability	03008011h	R/WO, RO
0020–0023h	V1CTL	VC 1 Resource Control	00000000h	R/W
0026–0027h	V1STS	VC 1 Resource Status	0000h	RO
0030-006Fh (Corporate Only)	—	Reserved	—	—
0030-006Fh (Consumer Only)	PAT	Port Arbitration Table		
0088-008Bh	CIR1	Chipset Initialization Register 1	00000000h	R/WO
00AC-00AFh	REC	Root Error Command	0000h	R/W
0100–0103h	RCTCL	Root Complex Topology Capability List	1A010005h	RO
0104–0107h	ESD	Element Self Description	00000802h	R/WO, RO
0110–0113h	ULD	Upstream Link Descriptor	00000001h	R/WO, RO

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 2 of 4)

Offset	Mnemonic	Register Name	Default	Type
0118–011Fh	ULBA	Upstream Link Base Address	0000000000000000h	R/WO
0120–0123h	RP1D	Root Port 1 Descriptor	01xx0002h	R/WO, RO
0128–012Fh	RP1BA	Root Port 1 Base Address	00000000000E0000h	RO
0130–0133h	RP2D	Root Port 2 Descriptor	02xx0002h	R/WO, RO
0138–013Fh	RP2BA	Root Port 2 Base Address	00000000000E1000h	RO
0140–0143h	RP3D	Root Port 3 Descriptor	03xx0002h	R/WO, RO
0148–014Fh	RP3BA	Root Port 3 Base Address	00000000000E2000h	RO
0150–0153h	RP4D	Root Port 4 Descriptor	04xx0002h	R/WO, RO
0158–015Fh	RP4BA	Root Port 4 Base Address	00000000000E3000h	RO
0160–0163h	HDD	Intel® High Definition Audio Descriptor	15xx0002h	R/WO, RO
0168–016Fh	HDBA	Intel High Definition Audio Base Address	00000000000D8000h	RO
0170–0173h	RP5D	Root Port 5 Descriptor	05xx0002h	R/WO, RO
0178–017Fh	RP5A	Root Port 5 Base Address	00000000000E4000h	RO
0180–0183h	RP6D	Root Port 6 Descriptor	06xx0002h	R/WO, RO
0188–018Fh	RP6BA	Root Port 6 Base Address	00000000000E5000h	RO
01A0–01A3h	ILCL	Internal Link Capability List	00010006h	RO
01A4–01A7h	LCAP	Link Capabilities	00012841h	RO, R/WO
01A8–01A9h	LCTL	Link Control	0000h	R/W
01AA–01ABh	LSTS	Link Status	0041h	RO
01F4-01F7h	CIR2	Chipset Initialization Register 2	00000000h	R/W
01FC-01FDh	CIR3	Chipset Initialization Register 3	0000h	R/W
0220-0223h	BCR	Backbone Configuration	00000000h	R/W
0224–0227h	RPC	Root Port Configuration	0000000yh	R/W, RO
0234-0327h	DMIC	DMI Control	00000000h	R/W, RO
0238–023Bh	RPFN	Root Port Function Number for PCI Express Root Ports	00543210h	R/WO, RO
0290-0293h	FPSS	Function Level Reset Pending Status Summary	00000000h	RO
0F20-0F23h	CIR13	Chipset Initialization Register 13	B2B477CCh	R/W
1D40-1D47h	CIR5	Chipset Initialization Register 5	0000000000000000h	R/W
1E00–1E03h	TRSR	Trap Status Register	00000000h	R/WC, RO
1E10–1E17h	TRCR	Trapped Cycle Register	0000000000000000h	RO
1E18-1E1Fh	TWDR	Trapped Write Data Register	0000000000000000h	RO
1E80-1E87h	IOTR0	I/O Trap Register 0	0000000000000000h	R/W
1E88-1E8Fh	IOTR1	I/O Trap Register 1	0000000000000000h	R/W
1E90-1E97h	IOTR2	I/O Trap Register 2	0000000000000000h	R/W

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 3 of 4)

Offset	Mnemonic	Register Name	Default	Type
1E98-1E9Fh	IOTR3	I/O Trap Register 3	0000000000000000h	R/W
2010-2013h	DMC	DMI Miscellaneous Control register	00000002h	R/W
2034-2037h	CIR7	Chipset Initialization Register 7	B2B477CCh	R/W
3000–3000h	TCTL	TCO Control	00h	R/W
3100–3103h	D31IP	Device 31 Interrupt Pin	03243200h	R/W, RO
3104–3107h	D30IP	Device 30 Interrupt Pin	00000000h	RO
3108–310Bh	D29IP	Device 29 Interrupt Pin	10004321h	R/W
310C–310Fh	D28IP	Device 28 Interrupt Pin	00214321h	R/W
3110–3113h	D27IP	Device 27 Interrupt Pin	00000001h	R/W
3114–3117h	D26IP	Device 26 Interrupt Pin	30000321h	R/W
3118–311Bh	D25IP	Device 25 Interrupt Pin	00000001h	R/W
3140–3141h	D31IR	Device 31 Interrupt Route	3210h	R/W
3142–3143h	D30IR	Device 30 Interrupt Route	0000h	RO
3144–3145h	D29IR	Device 29 Interrupt Route	3210h	R/W
3146–3147h	D28IR	Device 28 Interrupt Route	3210h	R/W
3148–3149h	D27IR	Device 27 Interrupt Route	3210h	R/W
314C–314Dh	D26IR	Device 26 Interrupt Route	3210h	R/W
3150–3151h	D25IR	Device 25 Interrupt Route	3210h	R/W
31FE–31FFh (Corporate Only)	OIC	Other Interrupt Control	0000h	R/W
31FF–31FFh (Consumer Only)	OIC	Other Interrupt Control	00h	R/W
3300-3303h	SBEMC3	Scheduled Break Event C3	00000000h	R/W
3304-3307h	SBEMC4	Schedule Break Event C4	00000000h	R/W
3310–3313h (Corporate Only)	PRSTS	Power and Reset Status		
3400–3403h	RC	RTC Configuration	00000000h	R/W, R/WLO
3404–3407h	HPTC	High Precision Timer Configuration	00000000h	R/W
3410–3413h	GCS	General Control and Status	000000yy0h	R/W, R/WLO
3414–3414h	BUC	Backed Up Control	00h	R/W
3418–341Bh	FD	Function Disable	00000000h	R/W
341C–341Fh	CG	Clock Gating	00000000h	R/W
3420–3420h	PDSW	Function Disable SUS Well	00h	R/W
3430-3433h	CIR8	Chipset Initialization Register 8	00000000h	R/W

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 4 of 4)

Offset	Mnemonic	Register Name	Default	Type
350C-350Fh	CIR9	Chipset Initialization Register 9	00000000h	R/W
3524–3525h	PPO	USB Port Power Off	0000h	R/W
352C-352Fh	CIR10	Chipset Initialization Register 10	0008C008hh	R/W
35F0-35F3h	MAP	USB Remap Control	00000000h	R/WO

10.1.1 VCH—Virtual Channel Capability Header Register

Offset Address: 0000–0003h Attribute: R/WO
Default Value: 10010002h Size: 32-bit

Bit	Description
31:20	**Next Capability Offset (NCO)** — R/WO. Indicates the next item in the list.
19:16	**Capability Version (CV**) — R/WO. Indicates support as a version 1 capability structure.
15:0	**Capability ID (CID)** — R/WO. Indicates this is the Virtual Channel capability item.

10.1.2 VCAP1—Virtual Channel Capability #1 Register

Offset Address: 0004–0007h Attribute: RO, R/WO
Default Value: 00000801h Size: 32-bit

Bit	Description
31:12	Reserved
11:10	**Port Arbitration Table Entry Size (PATS)** — RO. Indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports).
9:8	**Reference Clock (RC)** — RO. Fixed at 100 ns.
7	Reserved
6:4	**Low Priority Extended VC Count (LPEVC)** — RO. Indicates that there are no additional VCs of low priority with extended capabilities.
3	Reserved
2:0	**Extended VC Count (EVC)** — R/WO. Indicates that there is one additional VC (VC1) that exists with extended capabilities.

10.1.3 VCAP2—Virtual Channel Capability #2 Register

Offset Address: 0008–000Bh Attribute: RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**VC Arbitration Table Offset (ATO)** — RO. Indicates that no table is present for VC arbitration since it is fixed.
23:8	Reserved
7:0	**VC Arbitration Capability (AC)** — RO. Indicates that the VC arbitration is fixed in the root complex.

10.1.4 PVC—Port Virtual Channel Control Register

Offset Address: 000C–000Dh Attribute: RO, R/W
Default Value: 0000h Size: 16-bit

Bit	Description
15:04	Reserved
3:1	**VC Arbitration Select (AS)** — R/W. Indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	**Load VC Arbitration Table (LAT)** — RO. Indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

10.1.5 PVS—Port Virtual Channel Status Register

Offset Address: 000E–000Fh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:1	Reserved
0	**VC Arbitration Table Status (VAS)** — RO. Indicates the coherency status of the VC Arbitration table when it is being updated. This field is always 0 in the root complex since there is no VC arbitration table.

10.1.6 V0CAP—Virtual Channel 0 Resource Capability Register

Offset Address: 0010–0013h Attribute: RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** — RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved
22:16	**Maximum Time Slots (MTS)** — RO. This VC implements fixed arbitration, and therefore this field is not used.
15	**Reject Snoop Transactions (RTS)** — RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** — RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved
7:0	**Port Arbitration Capability (PAC)** — RO. Indicates that this VC uses fixed port arbitration.

10.1.7 V0CTL—Virtual Channel 0 Resource Control Register

Offset Address: 0014–0017h Attribute: R/W, RO
Default Value: 800000FFh Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)** — RO. Always set to 1. VC0 is always enabled and cannot be disabled.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)** — RO. Indicates the ID to use for this virtual channel.
23:20	Reserved
19:17	**Port Arbitration Select (PAS)** — R/W. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** — RO. The root complex does not implement an arbitration table for this virtual channel.
15:8	Reserved
7:1	**Transaction Class / Virtual Channel Map (TVM)** — R/W. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0	Reserved

10.1.8 V0STS—Virtual Channel 0 Resource Status Register

Offset Address: 001A–001Bh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:2	Reserved
1	**VC Negotiation Pending (NP)** — RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)** — RO. There is no port arbitration table for this VC, so this bit is reserved at 0.

10.1.9 V1CAP—Virtual Channel 1 Resource Capability Register

Offset Address: 001C–001Fh Attribute: R/WO, RO
Default Value: 03008011h (Consumer)
00008001h (Corporate) Size: 32-bit

Bit	Description
31:24 (Corporate Only)	**Port Arbitration Table Offset (AT)** — RO. Indicates the location of the port arbitration table in the root complex. A value of 0h indicates the table is not present
31:24 (Consumer Only)	**Port Arbitration Table Offset (AT)** — RO. Indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23	Reserved
22:16	**Maximum Time Slots (MTS)** — R/WO. This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	**Reject Snoop Transactions (RTS)** — RO. All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	**Advanced Packet Switching (APS)** — RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved
7:0 (Corporate Only)	**Port Arbitration Capability (PAC)** — RO. Indicates the port arbitration capability is hardware-fixed.
7:0 (Consumer Only)	**Port Arbitration Capability (PAC)** — RO. Indicates the port arbitration capability is time-based WRR of 128 phases.

10.1.10 V1CTL—Virtual Channel 1 Resource Control Register

Offset Address: 0020–0023h
Default Value: 00000000h (Consumer)
00000000h (Corporate)
Attribute: R/W, RO
Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)** — R/W. Enables the VC when set. Disables the VC when cleared.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)** — R/W. Indicates the ID to use for this virtual channel.
23:20	Reserved
19:17 (Corporate Only)	**Port Arbitration Select (PAS)** —RO. The only permissible value of this field is 0h for fixed arbitration.
19:17 (Consumer Only)	**Port Arbitration Select (PAS)** — R/W. Indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16 (Corporate Only)	Reserved
16 (Consumer Only)	**Load Port Arbitration Table (LAT)** — R/W. When set, the port arbitration table loaded based upon the PAS field in this register. This bit always returns 0 when read.
15:8	Reserved
7:1	**Transaction Class / Virtual Channel Map (TVM)** — R/W. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0	Reserved

10.1.11 V1STS—Virtual Channel 1 Resource Status Register

Offset Address: 0026–0027h
Default Value: 0000h
Attribute: RO
Size: 16-bit

Bit	Description
15:2	Reserved
1	**VC Negotiation Pending (NP)** — RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)** — RO. Indicates the coherency status of the port arbitration table. This bit is set when LAT (offset 000Ch:bit 0) is written with value 1 and PAS (offset 0014h:bits19:17) has value of 4h. This bit is cleared after the table has been updated.

10.1.12 PAT—Port Arbitration Table (Consumer Only)

Offset Address: 0030-006Fh Attribute:
Default Value: Size: 64-Byte

This a 64-byte register that contains the arbitration table to be loaded into the port arbitration table. Every 4-bits contains an entry for one of the downstream PCI Express* ports or a 0h to indicate idle. The ports are mapped as follows:

- Port 1: Value used is 1h.
- Port 2: Value used is 2h.
- Port 3: Value used is 3h.
- Port 4: Value used is 4h.
- Port 5: Value used is 5h.
- Port 6: Value used is 6h.
- Intel High Definition Audio: Value used is Fh.

10.1.13 CIR1—Chipset Initialization Register 1

Offset Address: 0088–008Bh Attribute: R/WO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:21	Reserved
20	**CIR1 Field 3** — R/WO. BIOS must set this bit.
19:16	Reserved
15	**CIR1 Field 2** — R/WO. BIOS must set this bit.
14:13	Reserved
12	**CIR1 Field 1**— R/WO. BIOS must set this bit.
11:0	Reserved

10.1.14 REC—Root Error Command Register

Offset Address: 00AC–00AFh Attribute: R/W
Default Value: 0000h Size: 32-bit

Bit	Description
31	**Drop Poisoned Downstream Packets (DPDP)** — R/W. Determines how downstream packets on DMI are handled that are received with the EP field set, indicating poisoned data: 1: This packet and all subsequent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to master Abort downstream. Packets without data such as memory, IO and config read requests are allowed to proceed. 0: Packets are forwarded downstream without forcing the UT field set.
30:0	Reserved

10.1.15 RCTCL—Root Complex Topology Capabilities List Register

Offset Address: 0100–0103h Attribute: RO
Default Value: 1A010005h Size: 32-bit

Bit	Description
31:20	**Next Capability (NEXT)** — RO. Indicates the next item in the list.
19:16	**Capability Version (CV)** — RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID)** — RO. Indicates this is a PCI Express* link capability section of an RCRB.

10.1.16 ESD—Element Self Description Register

Offset Address: 0104–0107h Attribute: R/WO, RO
Default Value: 00000802h Size: 32-bit

Bit	Description
31:24	**Port Number (PN)** — RO. A value of 0 to indicate the egress port for the Intel ICH10.
23:16	**Component ID (CID)** — R/WO. Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset.
15:8	**Number of Link Entries (NLE)** — RO. Indicates that one link entry (corresponding to DMI), 6 root port entries (for the downstream ports), and the Intel High Definition Audio device are described by this RCRB.
7:4	Reserved
3:0	**Element Type (ET)** — RO. Indicates that the element type is a root complex internal link.

10.1.17 ULD—Upstream Link Descriptor Register

Offset Address: 0110–0113h Attribute: R/WO, RO
Default Value: 00000001h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — R/WO. This field is programmed by platform BIOS to match the port number of the (G)MCH RCRB that is attached to this RCRB.
23:16	**Target Component ID (TCID)** — R/WO. This field is programmed by platform BIOS to match the component ID of the (G)MCH RCRB that is attached to this RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to the (G)MCH RCRB.
0	**Link Valid (LV)** — RO. Indicates that the link entry is valid.

10.1.18 ULBA—Upstream Link Base Address Register

Offset Address: 0118–011Fh Attribute: R/WO
Default Value: 0000000000000000h Size: 64-bit

Bit	Description
63:32	**Base Address Upper (BAU)** — R/WO. This field is programmed by platform BIOS to match the upper 32-bits of base address of the (G)MCH RCRB that is attached to this RCRB.
31:0	**Base Address Lower (BAL)** — R/WO. This field is programmed by platform BIOS to match the lower 32-bits of base address of the (G)MCH RCRB that is attached to this RCRB.

10.1.19 RP1D—Root Port 1 Descriptor Register

Offset Address: 0120–0123h Attribute: R/WO, RO
Default Value: 01xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 1h (root port #1).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When FD.PE1D (offset 3418h, bit 16) is set, this link is not valid (returns 0). When FD.PE1D is cleared, this link is valid (returns 1).

10.1.20 RP1BA—Root Port 1 Base Address Register

Offset Address: 0128–012Fh Attribute: RO
Default Value: 00000000000E0000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #0.
11:0	Reserved

10.1.21 RP2D—Root Port 2 Descriptor Register

Offset Address: 0130–0133h Attribute: R/WO, RO
Default Value: 02xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 2h (root port #2).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When RPC.PC (offset 0224h, bits 1:0) is '01', '10', or '11', or FD.PE2D (offset 3418h, bit 17) is set, the link for this root port is not valid (return 0). When RPC.PC is '00' and FD.PE2D is cleared, the link for this root port is valid (return 1).

10.1.22 RP2BA—Root Port 2 Base Address Register

Offset Address: 0138–013Fh Attribute: RO
Default Value: 00000000000E1000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #1.
11:0	Reserved

10.1.23 RP3D—Root Port 3 Descriptor Register

Offset Address: 0140–0143h Attribute: R/WO, RO
Default Value: 03xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 3h (root port #3).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When RPC.PC (offset 0224h, bits 1:0) is '11', or FD.PE3D (offset 3418h, bit 18) is set, the link for this root port is not valid (return 0). When RPC.PC is '00', '01', or "10', and FD.PE3D is cleared, the link for this root port is valid (return 1).

10.1.24 RP3BA—Root Port 3 Base Address Register

Offset Address: 0148–014Fh Attribute: RO
Default Value: 00000000000E2000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #2.
11:0	Reserved

10.1.25 RP4D—Root Port 4 Descriptor Register

Offset Address: 0150–0153h Attribute: R/WO, RO
Default Value: 04xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 4h (root port #4).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When RPC.PC (offset 0224h, bits 1:0) is ‘10’ or ‘11’, or FD.PE4D (offset 3418h, bit 19) is set, the link for this root port is not valid (return 0). When RPC.PC is ‘00’ or ‘01’ and FD.PE4D is cleared, the link for this root port is valid (return 1).

10.1.26 RP4BA—Root Port 4 Base Address Register

Offset Address: 0158–015Fh Attribute: RO
Default Value: 00000000000E3000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #3.
11:0	Reserved

10.1.27 HDD—Intel® High Definition Audio Descriptor Register

Offset Address: 0160–0163h Attribute: R/WO, RO
Default Value: 0Fxx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 15h (Intel High Definition Audio).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When FD.ZD (offset 3418h, bit 4) is set, the link to Intel High Definition Audio is not valid (return 0). When FD.ZD is cleared, the link to Intel High Definition Audio is valid (return 1).

10.1.28 HDBA—Intel® High Definition Audio Base Address Register

Offset Address: 0168–016Fh Attribute: RO
Default Value: 00000000000D8000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the High Definition Audio captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #27.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #0.
11:0	Reserved

10.1.29 RP5D—Root Port 5 Descriptor Register

Offset Address: 0170–0173h Attribute: R/WO, RO
Default Value: 05xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 5h (root port #5).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When FD.PE5D (offset 3418h, bit 20) is set, the link for this root port is not valid (return 0). When FD.PE5D is cleared, the link for this root port is valid (return 1).

10.1.30 RP5BA—Root Port 5 Base Address Register

Offset Address: 0178–017Fh Attribute: RO
Default Value: 00000000000E4000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #4.
11:0	Reserved

10.1.31 RP6D—Root Port 6 Descriptor Register

Offset Address: 0180–0183h Attribute: R/WO, RO
Default Value: 06xx0002h Size: 32-bit

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the target port number is 6h (root port #6).
23:16	**Target Component ID (TCID)** — R/WO. This field returns the value of the ESD.CID (offset 0104h, bits 23:16) field programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved
1	**Link Type (LT)** — RO. Indicates that the link points to a root port.
0	**Link Valid (LV)** — RO. When RPC.PC2 (offset 0224h, bits 1:0) is ‘01’ or FD.PE6D (offset 3418h, bit 21) is set, the link for this root port is not valid (return 0). When RPC.PC is ‘00’ and FD.PE6D is cleared, the link for this root port is valid (return 1).

10.1.32 RP6BA—Root Port 6 Base Address Register

Offset Address: 0188–018Fh Attribute: RO
Default Value: 00000000000E5000h Size: 64-bit

Bit	Description
63:28	Reserved
27:20	**Bus Number (BN)** — RO. Indicates the root port captured bus number.
19:15	**Device Number (DN)** — RO. Indicates the root port is on device #28.
14:12	**Function Number (FN)** — RO. Indicates the root port is on function #5.
11:0	Reserved

10.1.33 ILCL—Internal Link Capabilities List Register

Offset Address: 01A0–01A3h
Attribute: RO
Default Value: 00010006h
Size: 32-bit

Bit	Description
31:20	**Next Capability Offset (NEXT)** — RO. Indicates this is the last item in the list.
19:16	**Capability Version (CV)** — RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID)** — RO. Indicates this is capability for DMI.

10.1.34 LCAP—Link Capabilities Register

Offset Address: 01A4–01A7h
Attribute: R/WO, RO
Default Value: 00012841h
Size: 32-bit

Bit	Description
31:18	Reserved
17:15	Reserved
14:12	**L0s Exit Latency (EL0)** — R/WO. This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	**Active State Link PM Support (APMS)** — R/WO. Indicates that L0s and L1 are supported on DMI.
9:4	**Maximum Link Width (MLW)** — RO. Indicates the maximum link width is 4 ports.
3:0	**Maximum Link Speed (MLS)** — RO. Indicates the link speed is 2.5 Gb/s.

10.1.35 LCTL—Link Control Register

Offset Address: 01A8–01A9h
Attribute: R/W
Default Value: 0000h
Size: 16-bit

Bit	Description
15:8	Reserved
7	**Extended Synch (ES)** — R/W. When set, forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0.
6:2	Reserved
1:0	**Active State Link PM Control (ASPM)** — R/W. Indicates whether DMI should enter L0s. 00 = Disabled 01 = L0s entry enabled 10 = Reserved 11 = Reserved Corporate Only: The value of this register is used unless the DMI ASPM Override Enable register is set, in which case the DMI ASPM Override is used.

10.1.36 LSTS—Link Status Register

Offset Address: 01AA–01ABh Attribute: RO
Default Value: 0041h Size: 16-bit

Bit	Description
15:10	Reserved
9:4	**Negotiated Link Width (NLW)** — RO. Negotiated link width is x4 (000100b).
3:0	**Link Speed (LS)** — RO. Link is 2.5 Gb/s.

10.1.37 CIR2 — Chipset Initialization Register 2

Offset Address: 01F4–01F7h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:0	**CIR2 Field 1** — R/W. BIOS shall program to 86000040h

10.1.38 CIR3 — Chipset Initialization Register 3

Offset Address: 01FC–01FDh Attribute: R/W
Default Value: 0000h Size: 16-bit

Bit	Description
15:11	Reserved
10:8	**CIR3 Field 3** — R/W. BIOS must program this field to 110b.
7:4	Reserved
3	**CIR3 Field 2** — R/W. BIOS must set this bit.
2	Reserved
1:0	**CIR3 Field 1** — R/W. BIOS must program this field to 11b.

10.1.39 BCR — Backbone Configuration Register

Offset Address: 0220–0223h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:7	Reserved
6	**BCR Field 2** — R/W. BIOS must set this bit.
5:3	Reserved
2:0	**BCR Field 1** — R/W. BIOS program this field to 101b

10.1.40 RPC—Root Port Configuration Register

Offset Address: 0224–0227h Attribute: R/W, RO
Default Value: 0000000yh (y = 00xxb) Size: 32-bit

Bit	Description
31:8	Reserved
7	**High Priority Port Enable (HPE)** — R/W. 0 = The high priority path is not enabled. 1 = The port selected by the HPP field in this register is enabled for high priority. It will be arbitrated above all other VC0 (including integrated VC0) devices.
6:4	**High Priority Port (HPP)** — R/W. This controls which port is enabled for high priority when the HPE bit in this register is set. 111 = Reserved 110 = Reserved 101 = Port 6 100 = Port 5 101 = Port 4 010 = Port 3 001 = Port 2 000 = Port 1
3	Reserved
2	**Port Configuration2 (PC2)** — RO. This controls how the PCI bridges are organized in various modes of operation for Ports 5 and 6. Corporate only: This bit is set by the PCIEPCS2[1:0] soft strap. 1 = Reserved 0 = 2 x1s, Port 5 (x1), Port 6 (x1) This bit is in the resume well and is only reset by RSMRST#.
1:0	**Port Configuration (PC)** — RO. This controls how the PCI bridges are organized in various modes of operation for Ports 1-4. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. Consumer Only: These bits represent the strap values of HDA_SDOUT (bit 1) and HDA_SYNC (bit 0) when TP[3] is not pulled low at the rising edge of PWROK. Corporate Only: These bits are set by the PCIEPCS1[1:0] soft strap. 11 = 1 x4, Port 1 (x4) 10 = Reserved 01 = Reserved 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1) These bits are in the resume well and are only reset by RSMRST#.

10.1.41 DMIC—DMI Control Register

Offset Address: 0234–0237h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:19	Reserved
18 Corporate Only	**ASPM Control Override Enable (ASPMCOEN)** — RW. 1 = DMI will use the values in the ASPM Control Override registers 0 = DMI will use the ASPM Registers in the Link Control register. **NOTES:**This register allows BIOS to control the DMI ASPM settings instead of the OS.
18 (Consumer Only)	Reserved
17:16 (Corporate Only)	**ASPM Control Override (ASPMO)** — RW. Provides BIOS control of whether DMI should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
17:16 (Consumer Only)	Reserved
15:2	Reserved
1:0	**DMI Clock Gate Enable (DMICGEN)** — R/W. BIOS must program this field to 11b.

10.1.42 RPFN—Root Port Function Number and Hide for PCI Express* Root Ports

Offset Address: 0238–023Ch Attribute: R/WO, RO
Default Value: 00543210h Size: 32-bit

For the PCI Express root ports, the assignment of a function number to a root port is not fixed. BIOS may re-assign the function numbers on a port by port basis. This capability will allow BIOS to disable/hide any root port and still have functions 0 thru N-1 where N is the total number of enabled root ports.

Port numbers will remain fixed to a physical root port.

The existing root port Function Disable registers operate on physical ports (not functions).

Port Configuration (1x4, 4x1, etc.) is not affected by the logical function number assignment and is associated with physical ports.

Bit	Description
31:24	Reserved
23	**Root Port 6 Config Hide (RP6CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
22:20	**Root Port 6 Function Number (RP6FN)** — R/WO. These bits set the function number for PCI Express Root Port 6. This root port function number must be a unique value from the other root port function numbers
19	**Root Port 5 Config Hide (RP5CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
18:16	**Root Port 5 Function Number (RP5FN)** — R/WO. These bits set the function number for PCI Express Root Port 5. This root port function number must be a unique value from the other root port function numbers
15	**Root Port 4 Config Hide (RP4CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
14:12	**Root Port 4 Function Number (RP4FN)** — R/WO. These bits set the function number for PCI Express Root Port 4. This root port function number must be a unique value from the other root port function numbers
11	**Root Port 3 Config Hide (RP3CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
10:8	**Root Port 3 Function Number (RP3FN)** — R/WO. These bits set the function number for PCI Express Root Port 3. This root port function number must be a unique value from the other root port function numbers
7	**Root Port 2 Config Hide (RP2CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
6:4	**Root Port 2 Function Number (RP2FN)** — R/WO. These bits set the function number for PCI Express Root Port 2. This root port function number must be a unique value from the other root port function numbers
3	**Root Port 1 Config Hide (RP1CH)** — RW. This bit is used to hide the root port and any devices behind it from being discovered by the OS. When set to '1' the root port will not claim any downstream configuration transactions.
2:0	**Root Port 1 Function Number (RP1FN)** — R/WO. These bits set the function number for PCI Express Root Port 1. This root port function number must be a unique value from the other root port function numbers

10.1.43 FLRSTAT—FLR Pending Status Register

Offset Address: 0290–0293h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:24	Reserved.
23	**FLR Pending Status for D29:F7, EHCI #1** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
22:20	Reserved.
19	**FLR Pending Status for D29:F3, UHCI #6** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
18	**FLR Pending Status for D29:F2, UHCI #3** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
17	**FLR Pending Status for D29:F1, UHCI #2** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
16	**FLR Pending Status for D29:F0, UHCI #1** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
15	**FLR Pending Status for D26:F7, EHCI #2** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
14:11	Reserved.
10	**FLR Pending Status for D26:F2, UHCI #6** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
9	**FLR Pending Status for D26:F1, UHCI #5** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
8	**FLR Pending Status for D26:F0, UHCI #4** — R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
7:0	Reserved.

10.1.44 CIR13—Chipset Initialization Register 13

Offset Address: 0F20h–0F23h
Attribute: R/W
Default Value: B2B477CCh
Size: 32-bit

Bit	Description
31:20	Reserved
19:16	**CIR13 Field 1** — R/W. BIOS must program this field to 0101b.
15:0	Reserved

10.1.45 CIR5—Chipset Initialization Register 5

Offset Address: 1D40h–1D47h
Attribute: R/W
Default Value: 0000000000000000h
Size: 64-bit

Bit	Description
63:1	Reserved
0	**CIR5 Field 1** — R/W. BIOS must program this field to 1b.

10.1.46 TRSR—Trap Status Register

Offset Address: 1E00–1E03h
Attribute: R/WC, RO
Default Value: 00000000h
Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**Cycle Trap SMI# Status (CTSS)** — R/WC. These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space. Note that the SMI# and trapping must be enabled in order to set these bits. These bits are set before the completion is generated for the trapped cycle, thereby ensuring that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a 1 to the corresponding bit location in this register.

10.1.47 TRCR—Trapped Cycle Register

Offset Address: 1E10–1E17h Attribute: RO
Default Value: 0000000000000000h Size: 64-bit

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Bit	Description
63:25	Reserved
24	**Read/Write# (RWI)** — RO. 0 = Trapped cycle was a write cycle. 1 = Trapped cycle was a read cycle.
23:20	Reserved
19:16	**Active-high Byte Enables (AHBE)** — RO. This is the dword-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	**Trapped I/O Address (TIOA)** — RO. This is the dword-aligned address of the trapped cycle.
1:0	Reserved

10.1.48 TWDR—Trapped Write Data Register

Offset Address: 1E18–1E1Fh Attribute: RO
Default Value: 0000000000000000h Size: 64-bit

This register saves the data from I/O write cycles that are trapped for software to read.

Bit	Description
63:32	Reserved
31:0	**Trapped I/O Data (TIOD)** — RO. Dword of I/O write data. This field is undefined after trapping a read cycle.

10.1.49 IOTRn — I/O Trap Register (0-3)

Offset Address: 1E80–1E87h Register 0, 1E88–1E8Fh Register 1, 1E90–1E97h Register 2, 1E98–1E9Fh Register 3
Attribute: R/W
Default Value: 0000000000000000h
Size: 64-bit

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit	Description
63:50	Reserved
49	**Read/Write Mask (RWM)** — R/W. 0 = The cycle must match the type specified in bit 48. 1 = Trapping logic will operate on both read and write cycles.
48	**Read/Write# (RWIO)** — R/W. 0 = Write 1 = Read **NOTE:** The value in this field does not matter if bit 49 is set.
47:40	Reserved
39:36	**Byte Enable Mask (BEM)** — R/W. A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
35:32	**Byte Enables (TBE)** — R/W. Active-high dword-aligned byte enables.
31:24	Reserved
23:18	**Address[7:2] Mask (ADMA)** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the dword address, allowing for traps on address ranges up to 256 bytes in size.
17:16	Reserved
15:2	**I/O Address[15:2] (IOAD)** — R/W. dword-aligned address
1	Reserved
0	**Trap and SMI# Enable (TRSE)** — R/W. 0 = Trapping and SMI# logic disabled. 1 = The trapping logic specified in this register is enabled.

10.1.50 DMC—DMI Miscellaneous Control Register

Offset Address: 2010–2013h Attribute: R/W
Default Value: 00000002h Size: 32-bit

Bit	Description
31:20	Reserved
19	**DMI Misc. Control Field 1** — R/W. BIOS shall always program this field as per the BIOS Specification. 0 = Disable DMI Power Savings. 1 = Enable DMI Power Savings.
18:0	Reserved

10.1.51 CIR6—Chipset Initialization Register 6

Offset Address: 2024–2027h Attribute: R/W
Default Value: 0B4030C0h Size: 32-bit

Bit	Description
31:8	Reserved
7	**CIR6 Field 1** — R/W. BIOS must clear this bit.
6:0	Reserved

10.1.52 CIR7—Chipset Initialization Register 7

Offset Address: 2034–2037h Attribute: R/W
Default Value: B2B477CCh Size: 32-bit

Bit	Description
31:20	Reserved
19:16	**CIR7 Field 1** — R/W. BIOS must program this field to 0101b.
15:0	Reserved

10.1.53 TCTL—TCO Configuration Register

Offset Address: 3000–3000h Attribute: R/W
Default Value: 00h Size: 8-bit

Bit	Description
7	**TCO IRQ Enable (IE)** — R/W. 0 = TCO IRQ is disabled. 1 = TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field.
6:3	Reserved
2:0	**TCO IRQ Select (IS)** — R/W. Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9-11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20-23, and can be shared with other interrupt. 000 = IRQ 9 001 = IRQ 10 010 = IRQ 11 011 = Reserved 100 = IRQ 20 (only if APIC enabled) 101 = IRQ 21 (only if APIC enabled) 110 = IRQ 22 (only if APIC enabled) 111 = IRQ 23 (only if APIC enabled) When setting the these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

10.1.54 D31IP—Device 31 Interrupt Pin Register

Offset Address: 3100–3103h
Default Value: 03243200h
Attribute: R/W, RO
Size: 32-bit

Bit	Description
31:28	Reserved
27:24	**Thermal Throttle Pin (TTIP)** — R/W. Indicates which pin the Thermal Throttle controller drives as its interrupt 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
23:20	**SATA Pin 2 (SIP2)** — R/W. Indicates which pin the SATA controller 2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
19:16	Reserved
15:12	**SMBus Pin (SMIP)** — R/W. Indicates which pin the SMBus controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
11:8	**SATA Pin (SIP)** — R/W. Indicates which pin the SATA controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
7:4	Reserved
3:0	LPC Bridge Pin (LIP) — RO. Currently, the LPC bridge does not generate an interrupt, so this field is read-only and 0.

10.1.55 D30IP—Device 30 Interrupt Pin Register

Offset Address: 3104–3107h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	PCI Bridge Pin (PIP) — RO. Currently, the PCI bridge does not generate an interrupt, so this field is read-only and 0.

10.1.56 D29IP—Device 29 Interrupt Pin Register

Offset Address: 3108–310Bh Attribute: R/W
Default Value: 10004321h Size: 32-bit

Bit	Description
31:28	**EHCI Pin (EIP)** — R/W. Indicates which pin the EHCI controller #1 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
27:16	Reserved
15:12	**UHCI #6 Pin (U3P)** — R/W. Indicates which pin the UHCI controller #6 (Device 29 Function 3) drives as its interrupt, if controller exists 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# (Default) 5h-7h = Reserved **NOTE:** This field should be set to 0h when UHCI Controller #6 Remap bit (RCBA offset 35F0h:bit 0) is set to 0.
11:8	**UHCI #3 Pin (U2P)** — R/W. Indicates which pin the UHCI controller #3 (Device 29 Function 2) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-7h = Reserved

Bit	Description
7:4	**UHCI #2 Pin (U1P)** — R/W. Indicates which pin the UHCI controller #2 (Device 29 Function 1) drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	**UHCI #1 Pin (U0P)** — R/W. Indicates which pin the UHCI controller #1 (Device 29 Function 0) drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

10.1.57 D28IP—Device 28 Interrupt Pin Register

Offset Address: 310C–310Fh Attribute: R/W
Default Value: 00214321h Size: 32-bit

Bit	Description
31:16	Reserved
23:20	**PCI Express* #6 Pin (P6IP)** — R/W. Indicates which pin the PCI Express* port #6 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h-7h = Reserved
19:16	**PCI Express #5 Pin (P5IP)** — R/W. Indicates which pin the PCI Express port #5 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved
15:12	**PCI Express #4 Pin (P4IP)** — R/W. Indicates which pin the PCI Express* port #4 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# (Default) 5h-7h = Reserved

Bit	Description
11:8	**PCI Express #3 Pin (P3IP)** — R/W. Indicates which pin the PCI Express port #3 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-7h = Reserved
7:4	**PCI Express #2 Pin (P2IP)** — R/W. Indicates which pin the PCI Express port #2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	**PCI Express #1 Pin (P1IP)** — R/W. Indicates which pin the PCI Express port #1 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

10.1.58 D27IP—Device 27 Interrupt Pin Register

Offset Address: 3110–3113h Attribute: R/W
Default Value: 00000001h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**Intel® High Definition Audio Pin (ZIP)** — R/W. Indicates which pin the Intel High Definition Audio controller drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-Fh = Reserved

10.1.59 D26IP—Device 26 Interrupt Pin Register

Offset Address: 3114–3117h Attribute: R/W
Default Value: 30000321h Size: 32-bit

Bit	Description
31:28	**EHCI #2 Pin (E2IP)** — R/W. Indicates which pin the EHCI controller #2 drives as its interrupt: 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-Fh = Reserved
27:12	Reserved
11:8	**UHCI #6 Pin (U2P)** — R/W. Indicates which pin UHCI controller #6 (Device 26 Function 2) drives as its interrupt, if controller exists. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-Fh = Reserved **NOTE:** This field should be set to 0h when UHCI Controller #6 Remap bit (RCBA offset 35F0h:bit 0) is set to 1.
7:4	**UHCI #5 Pin (U1P)** — R/W. Indicates which pin UHCI controller #5 (Device 26 Function 1), drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h-Fh = Reserved
3:0	**UHCI #4 Pin (U0P)** — R/W. Indicates which pin UHCI controller #4 (Device 26 Function 0), drives as its interrupt. 0h = No Interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-Fh = Reserved

10.1.60 D25IP—Device 25 Interrupt Pin Register

Offset Address: 3118–311Bh Attribute: R/W
Default Value: 00000001h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**GBE LAN Pin (LIP)** — R/W. Indicates which pin the internal GbE LAN controller drives as its interrupt 0h = No Interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-Fh = Reserved

10.1.61 D31IR—Device 31 Interrupt Route Register

Offset Address: 3140–3141h Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** — R/W. Indicates which physical pin on the Intel ICH is connected to the INTD# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved

Bit	Description
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 31 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.62 D30IR—Device 30 Interrupt Route Register

Offset Address: 3142–3143h Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:0	Reserved. No interrupts generated from Device 30.

10.1.63 D29IR—Device 29 Interrupt Route Register

Offset Address: 3144–3145h Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** — R/W. Indicates which physical pin on the Intel ICH is connected to the INTD# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 29 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.64 D28IR—Device 28 Interrupt Route Register

Offset Address: 3146–3147h
Default Value: 3210h
Attribute: R/W
Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** — R/W. Indicates which physical pin on the Intel ICH is connected to the INTD# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 28 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.65 D27IR—Device 27 Interrupt Route Register

Offset Address: 3148–3149h Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)** — R/W. Indicates which physical pin on the Intel ICH is connected to the INTD# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 27 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.66 D26IR—Device 26 Interrupt Route Register

Offset Address: 314C–314Dh Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR) —** R/W. Indicates which physical pin on the ICH is connected to the INTD# pin reported for device 26 functions: 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 26 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 26 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 26 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.67 D25IR—Device 25 Interrupt Route Register

Offset Address: 3150–3151h Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR):** — R/W. Indicates which physical pin on the ICH is connected to the INTD# pin reported for device 25 functions: 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)** — R/W. Indicates which physical pin on the ICH is connected to the INTC# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)** — R/W. Indicates which physical pin on the ICH is connected to the INTB# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)** — R/W. Indicates which physical pin on the ICH is connected to the INTA# pin reported for device 25 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.68 OIC—Other Interrupt Control Register (Corporate Only)

Offset Address: 31FE–31FFh
Default Value: 0000h
Attribute: R/W
Size: 16-bit

Bit	Description
15:10	Reserved
9	**Coprocessor Error Enable (CEN)** — R/W. 0 = FERR# will not generate IRQ13 nor IGNNE#. 1 = If FERR# is low, the Intel ICH10 generates IRQ13 internally and holds it until an I/O port F0h write. It will also drive IGNNE# active.
8	**APIC Enable (AEN)** — R/W. 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode. **NOTE:** SW should read this register after modifying APIC enable bit prior to access to the IOxAPIC address range.
7:0	**APIC Range Select (ASEL)** — R/W.These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior ICH products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

NOTE: FEC10000h – FEC3FFFFh is allocated to PCIe when I/OxApic Enable (PAE) bit is set.

10.1.69 OIC—Other Interrupt Control Register (Consumer Only)

Offset Address: 31FF–31FFh
Default Value: 00h
Attribute: R/W
Size: 8-bit

Bit	Description
7:4	**APIC Range Select (ASEL)** — R/W.These bits define address bits 15:12 for the IOxAPIC range. The default value of 0h enables compatibility with prior ICH products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.
3:2	Reserved
1	**Coprocessor Error Enable (CEN)** — R/W. 0 = FERR# will not generate IRQ13 nor IGNNE#. 1 = If FERR# is low, the Intel® ICH10 generates IRQ13 internally and holds it until an I/O port F0h write. It will also drive IGNNE# active.
0	**APIC Enable (AEN)** — R/W. 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode. **NOTE:** SW should read this register after modifying APIC enable bit prior to access to the IOxAPIC address range.

10.1.70 SBEMC3—Scheduled Break Event C3 Exit Latency

Offset Address: 3300–3303h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:23	Reserved.
22:16	**Present State C3 Future State C3 Exit Latency (C3C3EL)** — R/W. Sets exit latency if present and future C-state is C3.
15	Reserved.
14:8	**Present State C2 Future State C3 Exit Latency (C2C3EL)** — R/W. Sets exit latency if present C-state is C2 and future C-state is C3.
7	Reserved.
6:0	**Present State C0 Future State C3 Exit Latency (C0C3EL)** — R/W. Sets exit latency if present C-state is C0 and future C-state is C3.

10.1.71 SBEMC4—Scheduled Break Event C4 Exit Latency

Offset Address: 3304–3307h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31	Reserved.
30:24	**Present State C4 Future State C4 Exit Latency (C4C4EL)** — R/W. Sets exit latency if present and future C-state is C4.
22:16	**Present State C3 Future State C4 Exit Latency (C3C4EL)** — R/W. Sets exit latency if present C-state is C3 and future C-state is C4.
15	Reserved.
14:8	**Present State C2 Future State C4 Exit Latency (C2C4EL)** — R/W. Sets exit latency if present C-state is C2 and future C-state is C4.
7	Reserved.
6:0	**Present State C0 Future State C4 Exit Latency (C0C4EL)** — R/W. Sets exit latency if present C-state is C0 and future C-state is C4.

10.1.72 PRSTS—Power and Reset Status (Corporate Only)

Offset Address: 3310–3313h Attribute: RO, R/WC
Default Value: TBDh Size: 32-bit

Bit	Description
31:16	Reserved
15	**Power Management Watchdog Timer-**R/WC. This bit is set when the Power Management watchdog timer causes a global reset.
14:7	Reserved
6	**Intel® Management Engine Watchdog Timer Status**-R/WC. This bit is set when the Intel® Management Engine watchdog timer causes a global reset.
5	**Wake On Lan Override Wake Status (WOL_OVR_WK_STS)** — R/WC. This bit gets set when all of the following conditions are met: • Integrated LAN Signals a Power Management Event • The system is not in S0 • The “WOL Enable Override” bit is set in configuration space. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	Reserved
3	**ME Host Power Down (ME_HOST_PWRDN)** — R/WC.This bit is set when the Intel ME generates a host reset with power down.
2	**ME Host Reset Warm Status (ME_HRST_WARM_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Host reset without power cycling. Software clears this bit by writing a 1 to this bit position.
1	**ME Host Reset Cold Status (ME_HRST_COLD_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Host reset with power cycling. Software clears this bit by writing a 1 to this bit position.
0	**ME WAKE STATUS (ME_WAKE_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Non-Maskable wake event, and is not affected by any other enable bit. When this bit is set, the Host Power Management logic wakes to S0.

10.1.73 RC—RTC Configuration Register

Offset Address: 3400–3403h Attribute: R/W, R/WLO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:5	Reserved
4	**Upper 128 Byte Lock (UL)** — R/WLO. 0 = Bytes not locked. 1 = Bytes 38h-3Fh in the upper 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
3	**Lower 128 Byte Lock (LL)** — R/WLO. 0 = Bytes not locked. 1 = Bytes 38h-3Fh in the lower 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
2	**Upper 128 Byte Enable (UE)** — R/W. 0 = Bytes locked. 1 = The upper 128-byte bank of RTC RAM can be accessed.
1:0	Reserved

10.1.74 HPTC—High Precision Timer Configuration Register

Offset Address: 3404–3407h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:8	Reserved
7	**Address Enable (AE)** — R/W. 0 = Address disabled. 1 = The Intel® ICH10 will decode the High Precision Timer memory address range selected by bits 1:0 below.
6:2	Reserved
1:0	**Address Select (AS)** — R/W. This 2-bit field selects 1 of 4 possible memory address ranges for the High Precision Timer functionality. The encodings are: 00 = FED0_0000h – FED0_03FFh 01 = FED0_1000h – FED0_13FFh 10 = FED0_2000h – FED0_23FFh 11 = FED0_3000h – FED0_33FFh

10.1.75 GCS—General Control and Status Register

Offset Address: 3410–3413h Attribute: R/W, R/WLO
Default Value: 00000yy0h (yy = xx0000x0b) Size: 32-bit

Bit	Description
31:13	Reserved.
12	**Function Level Reset Capability Structure Select (FLRCSSEL)** — R/W. 0 = Function Level Reset (FLR) will utilize the standard capability structure with unique capability ID assigned by PCISIG. 1 = Vendor Specific Capability Structure is selected for FLR.
11:10	**Boot BIOS Straps (BBS)** — R/W. This field determines the destination of accesses to the BIOS memory range. The default values for these bits represent the strap values of GNT0# (bit 11) at the rising edge of PWROK and SPI_CS1#(bit 10) at the rising edge of CLPWROK. **Bits 11:10** — **Description** 0xb — SPI 10b — PCI 11b — LPC When PCI is selected, the top 16 MB of memory below 4 GB (FF00_0000h to FFFF_FFFFh) is accepted by the primary side of the PCI P2P bridge and forwarded to the PCI bus. This allows systems with corrupted or unprogrammed flash to boot from a PCI device. The PCI-to-PCI bridge Memory Space Enable bit does not need to be set (nor any other bits) in order for these cycles to go to PCI. Note that BIOS decode range bits and the other BIOS protection bits have no effect when PCI is selected. This functionality is intended for debug/testing only. When SPI or LPC is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set. **NOTE:** Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.
9	**Server Error Reporting Mode (SERM)** — R/W. 0 = The Intel® ICH10 is the final target of all errors. The (G)MCH sends a messages to the ICH for the purpose of generating NMI. 1 = The (G)MCH is the final target of all errors from PCI Express* and DMI. In this mode, if the ICH10 detects a fatal, non-fatal, or correctable error on DMI or its downstream ports, it sends a message to the (G)MCH. If the ICH10 receives an ERR_* message from the downstream port, it sends that message to the (G)MCH.
8:7	Reserved
6	**FERR# MUX Enable (FME)** — R/W. This bit enables FERR# to be a processor break event indication. 0 = Disabled. 1 = The ICH10 examines FERR# during a C2, C3, or C4 state as a break event. See Chapter 5.13.5 for a functional description.

Bit	Description
5	**No Reboot (NR)** — R/W. This bit is set when the “No Reboot” strap (SPKR pin on ICH10) is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates “No Reboot”. 0 = System will reboot upon the second timeout of the TCO timer. 1 = The TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
4	**Alternate Access Mode Enable (AME)** — R/W. 0 = Disabled. 1 = Alternate access read only registers can be written, and write only registers can be read. Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the ICH implements an alternate access mode. For a list of these registers see Section 5.13.9.
3	**Shutdown Policy Select (SPS)** — R/W. When cleared (default), the ICH10 will drive INIT# in response to the shutdown Vendor Defined Message (VDM). When set to 1, ICH10 will treat the shutdown VDM similar to receiving a CF9h I/O write with data value06h, and will drive PLTRST# active.
2	**Reserved Page Route (RPR)** — R/W. Determines where to send the reserved page registers. These addresses are sent to PCI or LPC for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h, 84h, 85h, 86h, 88h, 8Ch, 8Dh, and 8Eh. 0 = Writes will be forwarded to LPC, shadowed within the ICH, and reads will be returned from the internal shadow 1 = Writes will be forwarded to PCI, shadowed within the ICH, and reads will be returned from the internal shadow. Note, if some writes are done to LPC/PCI to these I/O ranges, and then this bit is flipped, such that writes will now go to the other interface, the reads will not return what was last written. Shadowing is performed on each interface. The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are always decoded to LPC.
1	Reserved
0	**BIOS Interface Lock-Down (BILD)** — R/WLO. 0 = Disabled. 1 = Prevents BUC.TS (offset 3414, bit 0) and GCS.BBS (offset 3410h, bits 11:10) from being changed. This bit can only be written from 0 to 1 once.

10.1.76 BUC—Backed Up Control Register

Offset Address: 3414–3414h Attribute: R/W
Default Value: 0000000xb Size: 8-bit

All bits in this register are in the RTC well and only cleared by RTCRST#

Bit	Description
7:6	Reserved
5	**LAN Disable** — R/W. 0 = LAN is Enabled 1 = LAN is Disabled. This bit is locked by the Function Disable SUS Well Lockdown register. Once locked this bit can not be changed by software.
4	**Daylight Savings Override (SDO)** — R/W. 0 = Daylight Savings is Enabled. 1 = The DSE bit in RTC Register B is set to Read-only with a value of 0 to disable daylight savings.
3	**Reserved**
2	**CPU BIST Enable (CBE)** — R/W. This bit is in the resume well and is reset by RSMRST#, but not PLTRST# nor CF9h writes. 0 = Disabled. 1 = The INIT# signals will be driven active when CPURST# is active. INIT# and INIT3_3V# will go inactive with the same timings as the other processor interface signals (hold time after CPURST# inactive).
1	Reserved
0	**Top Swap (TS)** — R/W. 0 = Intel® ICH10 will not invert A16. 1 = ICH10 will invert A16 for cycles going to the BIOS space (but not the feature space) in the FWH. If ICH is strapped for Top-Swap (GNT3# is low at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

10.1.77 FD—Function Disable Register

Offset Address: 3418–341Bh Attribute: R/W
Default Value: See bit description Size: 32-bit

The UHCI functions must be disabled from highest function number to lowest within each PCI device (Device 29 or Device 26). For example, if only two UHCIs are wanted on Device 29, software must disable UHCI #3 (UD3 bit set). When disabling UHCIs, the EHCI Structural Parameters Registers must be updated with coherent information in "Number of Companion Controllers" and "N_Ports" fields.

When disabling a function, only the configuration space is disabled. Software must ensure that all functionality within a controller that is not desired (such as memory spaces, I/O spaces, and DMA engines) is disabled prior to disabling the function.

When a function is disabled, software must not attempt to re-enable it. A disabled function can only be re-enabled by a platform reset.

Bit	Description
31:26	Reserved
25	**Serial ATA Disable 2 (SAD2)** — R/W. Default is 0. 0 = The SATA controller #2 (D31:F5) is enabled. 1 = The SATA controller #2 (D31:F5) is disabled.
24	**Thermal Throttle Disable (TTD)** — R/W. Default is 0. 0 = Thermal Throttle is enabled. 1 = Thermal Throttle is disabled.
23:22	Reserved
21	**PCI Express* 6 Disable (PE6D)** — R/W. Default is 0. When disabled, the link for this port is put into the "link down" state. 0 = PCI Express* port #6 is enabled. 1 = PCI Express port #6 is disabled.
20	**PCI Express 5 Disable (PE5D)** — R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #5 is enabled. 1 = PCI Express port #5 is disabled.
19	**PCI Express 4 Disable (PE4D)** — R/W. Default is 0. When disabled, the link for this port is put into the "link down" state. 0 = PCI Express port #4 is enabled. 1 = PCI Express port #4 is disabled. **NOTE:** This bit must be set when Port 1 is configured as a x4.
18	**PCI Express 3 Disable (PE3D)** — R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #3 is enabled. 1 = PCI Express port #3 is disabled. **NOTE:** This bit must be set when Port 1 is configured as a x4.
17	**PCI Express 2 Disable (PE2D)** — R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #2 is enabled. 1 = PCI Express port #2 is disabled. **NOTE:** This bit must be set when Port 1 is configured as a x4 or a x2.

Bit	Description
16	**PCI Express 1 Disable (PE1D)** — R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #1 is enabled. 1 = PCI Express port #1 is disabled.
15	**EHCI #1 Disable (EHCI1D)** — R/W. Default is 0. 0 = The EHCI #1 is enabled. 1 = The EHCI #1 is disabled.
14	**LPC Bridge Disable (LBD)** — R/W. Default is 0. 0 = The LPC bridge is enabled. 1 = The LPC bridge is disabled. Unlike the other disables in this register, the following additional spaces will no longer be decoded by the LPC bridge: • · Memory cycles below 16 MB (1000000h) • · I/O cycles below 64 KB (10000h) • · The Internal I/OxAPIC at FEC0_0000 to FECF_FFFF Memory cycles in the LPC BIOS range below 4 GB will still be decoded when this bit is set, but the aliases at the top of 1 MB (the E and F segment) no longer will be decoded.
13	**EHCI #2 Disable (EHCI2D)** — R/W. Default is 0. 0 = The EHCI #2 is enabled. 1 = The EHCI #2 is disabled. Note: When this bit is set, the UHCI #5 function is not available and the UHCI #4 must be disabled by setting bit 11 in this register.
12	**UHCI #5 Disable (U5D)** — R/W. Default is 0 0 = The UHCI #5 is enabled. 1 = The UHCI #5 is disabled. When the EHCI #2 Device Disable (EHCI2D) is set, this bit is a don't care
11	**UHCI #4 Disable (U4D)** — R/W. Default is 0. 0 = The 4th UHCI (ports 6 and 7) is enabled. 1 = The 4th UHCI (ports 6 and 7) is disabled. Note that UHCI #4 must be disabled when EHCI #2 is disabled with bit 13 in this register.
10	**UHCI #3 Disable (U3D)** — R/W. Default is 0. 0 = The 3rd UHCI (ports 4 and 5) is enabled. 1 = The 3rd UHCI (ports 4 and 5) is disabled.
9	**UHCI #2 Disable (U2D)** — R/W. Default is 0. 0 = The 2nd UHCI (ports 2 and 3) is enabled. 1 = The 2nd UHCI (ports 2 and 3) is disabled.
8	**UHCI #1 Disable (U1D)** — R/W. Default is 0. 0 = The 1st UHCI (ports 0 and 1) is enabled. 1 = The 1st UHCI (ports 0 and 1) is disabled.
7	**UHCI #6 Disable (U6D)** — R/W. Default is 0. 0 = The 6th UHCI (ports 10 and 11) is enabled. 1 = The 6th UHCI (ports 10 and 11) is disabled.
6:5 (Corporate Only)	**USB Test Devices #1 and #2 — R/W**. Default is 0. BIOS must set these bits to 11b. **NOTE:** These bits only apply to ICH10 Corporate A0, A1, and B0 Samples and are reserved for ICH10 Corporate Production units.

Bit	Description
6:5 (Consumer Only)	Reserved
4	**Intel® High Definition Audio Disable (HDAD)** — R/W. Default is 0. 0 = The Intel High Definition Audio controller is enabled. 1 = The Intel High Definition Audio controller is disabled and its PCI configuration space is not accessible.
3	**SMBus Disable (SD)** — R/W. Default is 0. 0 = The SMBus controller is enabled. 1 = The SMBus controller is disabled. In ICH5 and previous, this also disabled the I/O space. In ICH10, it only disables the configuration space.
2	**Serial ATA Disable 1 (SAD1)** — R/W. Default is 0. 0 = The SATA controller #1 (D31:F2) is enabled. 1 = The SATA controller #1 (D31:F2) is disabled.
1	Reserved
0	BIOS must set this bit to 1b.

10.1.78 CG—Clock Gating

Offset Address: 341C–341Fh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**Legacy (LPC) Dynamic Clock Gate Enable** — R/W. 0 = Legacy Dynamic Clock Gating is Disabled 1 = Legacy Dynamic Clock Gating is Enabled
30	Reserved
29:28	**USB UHCI Dynamic Clock Gate Enable** — R/W. 0 = USB UHCI Dynamic Clock Gating is Disabled 1 = USB UHCI Dynamic Clock Gating is Enabled 0 = Reserved 1 = Reserved
27	**SATA Port 3 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 3 Dynamic Clock Gating is Disabled 1 = SATA Port 3 Dynamic Clock Gating is Enabled
26	**SATA Port 2 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 2 Dynamic Clock Gating is Disabled 1 = SATA Port 2 Dynamic Clock Gating is Enabled
25	**SATA Port 1 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 1 Dynamic Clock Gating is Disabled 1 = SATA Port 1 Dynamic Clock Gating is Enabled
24	**SATA Port 0 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 0 Dynamic Clock Gating is Disabled 1 = SATA Port 0 Dynamic Clock Gating is Enabled

Bit	Description
23	**LAN Static Clock Gating Enable (LANSCGE)** — R/W. 0 = LAN Static Clock Gating is Disabled 1 = LAN Static Clock Gating is Enabled when the LAN Disable bit is set in the Backed Up Control RTC register.
22	**High Definition Audio Dynamic Clock Gate Enable** — R/W. 0 = High Definition Audio Dynamic Clock Gating is Disabled 1 = High Definition Audio Dynamic Clock Gating is Enabled
21	**High Definition Audio Static Clock Gate Enable** — R/W. 0 = High Definition Audio Static Clock Gating is Disabled 1 = High Definition Audio Static Clock Gating is Enabled
20	**USB EHCI Static Clock Gate Enable** — R/W. 0 = USB EHCI Static Clock Gating is Disabled 1 = USB EHCI Static Clock Gating is Enabled
19	**USB EHCI Dynamic Clock Gate Enable** — R/W. 0 = USB EHCI Dynamic Clock Gating is Disabled 1 = USB EHCI Dynamic Clock Gating is Enabled
18	**SATA Port 5 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 5 Dynamic Clock Gating is Disabled 1 = SATA Port 5 Dynamic Clock Gating is Enabled
17	**SATA Port 4 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 4 Dynamic Clock Gating is Disabled 1 = SATA Port 4 Dynamic Clock Gating is Enabled
16	**PCI Dynamic Gate Enable** — R/W. 0 = PCI Dynamic Gating is Disabled 1 = PCI Dynamic Gating is Enabled
15:6	Reserved
5	**SMBus Clock Gating Enable (SMBCGEN)** — R/W. 0 = SMBus Clock Gating is Disabled. 1 = SMBus Clock Gating is Enabled.
4	**PCI Express* RX Clock Gating Enable (PRXCGEN)** — R/W. 0 = AFE RX Clock Gating is Disabled 1 = AFE RX Clock Gating is Enabled whenever all PCIe ports RX are in squelch
3	**DMI and PCI Express* RX Dynamic Clock Gate Enable** — R/W. 0 = DMI and PCI Express root port RX Dynamic Clock Gating is Disabled 1 = DMI and PCI Express root port RX Dynamic Clock Gating is Enabled
2	**PCI Express TX Dynamic Clock Gate Enable** — R/W. 0 = PCI Express root port TX Dynamic Clock Gating is Disabled 1 = PCI Express root port TX Dynamic Clock Gating is Enabled
1	**DMI TX Dynamic Clock Gate Enable** — R/W. 0 = DMI TX Dynamic Clock Gating is Disabled 1 = DMI TX Dynamic Clock Gating is Enabled
0	**PCI Express Root Port Static Clock Gate Enable** — R/W. 0 = PCI Express root port Static Clock Gating is Disabled 1 = PCI Express root port Static Clock Gating is Enabled

10.1.79 FDSW—Function Disable SUS Well

Offset Address: 3420h Attribute: R/W
Default Value: 00h Size: 8-bit

Bit	Description
7	**Function Disable SUS Well Lockdown (FDSWL)**— R/W 0 = FDSW registers are not locked down 1 = FDSW registers are locked down
6:0	Reserved

10.1.80 CIR8—Chipset Initialization Register 8

Offset Address: 3430-3433h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
7:2	Reserved
1:0	**CIR8 Field 1** — R/W. BIOS must program this field to 10b.

10.1.81 CIR9—Chipset Initialization Register 9

Offset Address: 350Ch–350Fh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:28	Reserved
27:26	**CIR9 Field 1** — R/W. BIOS must program this field to 10b.
25:0	Reserved

10.1.82 PPO—Port Power Off

Offset Address: 3524–3525h Attribute: R/W
Default Value: 0000h Size: 16-bit

Bit	Description
15:12	Reserved
11:0	**USB Port Power Off**— R/W 1 = The corresponding EHCI and UHCI ports are electrically disconnected in this mode. ***Warning:*** The platform must ensure that the powered off ports are not routed to any internal USB header or external USB connector. The ICH provides pull-down termination resistors. This register can not be written when the USB Per-Port Registers Write Enable bit (UPRWC register, PMBASE + 3C, bit 1) is 0.

10.1.83 CIR10—Chipset Initialization Register 10

Offset Address: 352C–352Fh Attribute: R/W
Default Value: 0008C008h Size: 32-bit

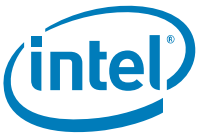
Bit	Description
32:18	Reserved
17:16	**CIR10 Field 1**— R/W. BIOS must program this field to 11b.
15:0	Reserved

10.1.84 MAP—Remap Control Register

Offset Address: 35F0–35F3h Attribute: R/WO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:01	Reserved
0	**UHCI Controller # 6 Remap** — R/WO 1 = UHCI Controller #6 is mapped to Device 29 Function 3 0 = UHCI Controller #6 is mapped to Device 26 Function 2 Note: When this bit is set, SW should reprogram the HCSPARAMS register (Section 17.2.1.3) to reflect the correct value for N_CC (bits 15:12) and N_Ports (bits 3:0) in each EHCI controller.

§ §



11 PCI-to-PCI Bridge Registers (D30:F0)

The ICH10 PCI bridge resides in PCI Device 30, Function 0 on bus #0. This implements the buffering and control logic between PCI and the backbone. The arbitration for the PCI bus is handled by this PCI device.

11.1 PCI Configuration Registers (D30:F0)

Note: Address locations that are not shown should be treated as Reserved (see Section 9.2 for details).

Table 11-1. PCI Bridge Register Address Map (PCI-PCI—D30:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PSTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	060401h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	01h	RO
18h–1Ah	BNUM	Bus Number	000000h	RO
1Bh	SMLT	Secondary Master Latency Timer	00h	R/W
1Ch–1Dh	IOBASE_LIMIT	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SECSTS	Secondary Status	0280h	R/WC, RO
20h–23h	MEMBASE_LIMIT	Memory Base and Limit	00000000h	R/W
24h–27h	PREF_MEM_BASE_LIMIT	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capability List Pointer	50h	RO
3Ch–3Dh	INTR	Interrupt Information	0000h	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control	0000h	R/WC, RO, R/W
40h–41h	SPDH	Secondary PCI Device Hiding	0000h	R/W, RO
44h–47h	DTC	Delayed Transaction Control	00000000h	R/W
48h–4Bh	BPS	Bridge Proprietary Status	00000000h	R/WC, RO

Table 11-1. PCI Bridge Register Address Map (PCI-PCI—D30:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
4Ch–4Fh	BPC	Bridge Policy Configuration	00001200h	R/W RO
50–51h	SVCAP	Subsystem Vendor Capability Pointer	000Dh	RO
54h–57h	SVID	Subsystem Vendor IDs	00000000	R/WO

11.1.1 VID— Vendor Identification Register (PCI-PCI—D30:F0)

Offset Address: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

11.1.2 DID— Device Identification Register (PCI-PCI—D30:F0)

Offset Address: 02h–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** — RO.This is a 16-bit value assigned to the PCI bridge. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Device ID Register.

11.1.3 PCICMD—PCI Command (PCI-PCI—D30:F0)

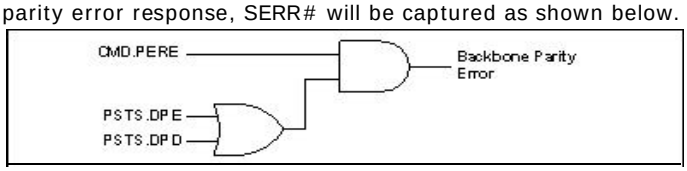
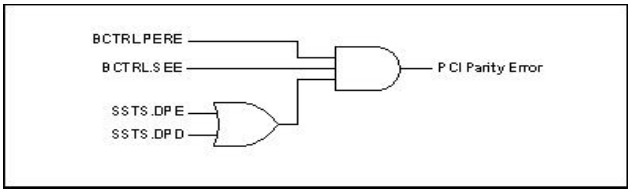
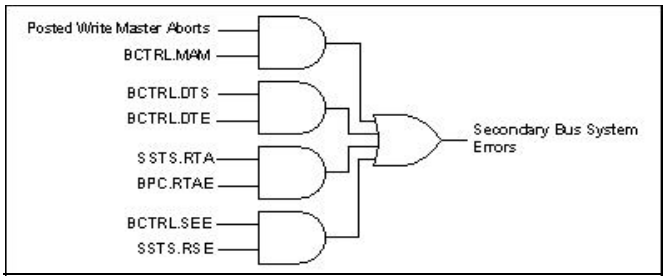
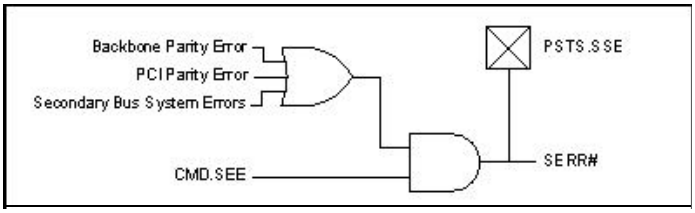
Offset Address: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	Interrupt Disable (ID) — RO. Hardwired to 0. The PCI bridge has no interrupts to disable
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
8	**SERR# Enable (SERR_EN)** — R/W. 0 = Disable. 1 = Enable the ICH10 to generate an NMI (or SMI# if NMI routed to SMI#) when the D30:F0 SSE bit (offset 06h, bit 14) is set.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
6	**Parity Error Response (PER)** — R/W. 0 = The ICH10 ignores parity errors on the PCI bridge. 1 = The ICH10 will set the SSE bit (D30:F0, offset 06h, bit 14) when parity errors are detected on the PCI bridge.
5	VGA Palette Snoop (VPS) — RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
4	Memory Write and Invalidate Enable (MWE) — RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*
3	Special Cycle Enable (SCE) — RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a* and the *PCI- to-PCI Bridge Specification.*
2	**Bus Master Enable (BME)** — R/W. 0 = Disable 1 = Enable. Allows the PCI-to-PCI bridge to accept cycles from PCI.
1	**Memory Space Enable (MSE)** — R/W. Controls the response as a target for memory cycles targeting PCI. 0 = Disable 1 = Enable
0	**I/O Space Enable (IOSE)** — R/W. Controls the response as a target for I/O cycles targeting PCI. 0 = Disable 1 = Enable

11.1.4 PSTS—PCI Status Register (PCI-PCI—D30:F0)

Offset Address: 06h–07h Attribute: R/WC, RO
Default Value: 0010h Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = Parity error Not detected. 1 = Indicates that the ICH10 detected a parity error on the internal backbone. This bit gets set even if the Parity Error Response bit (D30:F0:04 bit 6) is not set.
14	**Signaled System Error (SSE)** — R/WC. Several internal and external sources of the bridge can cause SERR#. The first class of errors is parity errors related to the backbone. The PCI bridge captures generic data parity errors (errors it finds on the backbone) as well as errors returned on backbone cycles where the bridge was the master. If either of these two conditions is met, and the primary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  As with the backbone, the PCI bus captures the same sets of errors. The PCI bridge captures generic data parity errors (errors it finds on PCI) as well as errors returned on PCI cycles where the bridge was the master. If either of these two conditions is met, and the secondary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  The final class of errors is system bus errors. There are three status bits associated with system bus errors, each with a corresponding enable. The diagram capturing this is shown below.  After checking for the three above classes of errors, an SERR# is generated, and PSTS.SSE logs the generation of SERR#, if CMD.SEE (D30:F0:04, bit 8) is set, as shown below. 
13	**Received Master Abort (RMA)** — R/WC. 0 = No master abort received. 1 = Set when the bridge receives a master abort status from the backbone.

Bit	Description
12	**Received Target Abort (RTA)** — R/WC. 0 = No target abort received. 1 = Set when the bridge receives a target abort status from the backbone.
11	**Signaled Target Abort (STA)** — R/WC. 0 = No signaled target abort 1 = Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	Reserved.
8	**Data Parity Error Detected (DPD)** — R/WC. 0 = Data parity error Not detected. 1 = Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set (D30:F0:04 bit 6).
7:5	Reserved.
4	**Capabilities List (CLIST)** — RO. Hardwired to 1. Capability list exist on the PCI bridge.
3	**Interrupt Status (IS)** — RO. Hardwired to 0. The PCI bridge does not generate interrupts.
2:0	Reserved

11.1.5 RID—Revision Identification Register (PCI-PCI—D30:F0)

Offset Address: 08h — Attribute: RO
Default Value: See bit description — Size: 8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

11.1.6 CC—Class Code Register (PCI-PCI—D30:F0)

Offset Address: 09h-0Bh — Attribute: RO
Default Value: 060401h — Size: 24 bits

Bit	Description
23:16	**Base Class Code (BCC)** — RO. Hardwired to 06h. Indicates this is a bridge device.
15:8	**Sub Class Code (SCC)** — RO. Hardwired to 04h. Indicates this device is a PCI-to-PCI bridge.
7:0	**Programming Interface (PI)** — RO. Hardwired to 01h. Indicates the bridge is subtractive decode

11.1.7 PMLT—Primary Master Latency Timer Register (PCI-PCI—D30:F0)

Offset Address: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:3	Master Latency Timer Count (MLTC) — RO. Reserved per the *PCI Express* Base Specification, Revision 1.0a*.
2:0	Reserved

11.1.8 HEADTYP—Header Type Register (PCI-PCI—D30:F0)

Offset Address: 0Eh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD)** — RO. A 0 indicates a single function device
6:0	**Header Type (HTYPE)** — RO. This 7-bit field identifies the header layout of the configuration space, which is a PCI-to-PCI bridge in this case.

11.1.9 BNUM—Bus Number Register (PCI-PCI—D30:F0)

Offset Address: 18h-1Ah
Default Value: 000000h
Attribute: R/W
Size: 24 bits

Bit	Description
23:16	**Subordinate Bus Number (SBBN)** — R/W. This field indicates the highest PCI bus number below the bridge.
15:8	**Secondary Bus Number (SCBN)** — R/W. This field indicates the bus number of PCI.
7:0	**Primary Bus Number (PBN)** — R/W. This field is default to 00h. In a multiple-ICH system, programmable PBN allows an ICH to be located on any bus. System configuration software is responsible for initializing these registers to appropriate values. PBN is not used by hardware in determining its bus number.

11.1.10 SMLT—Secondary Master Latency Timer Register (PCI-PCI—D30:F0)

Offset Address: 1Bh
Default Value: 00h
Attribute: R/W
Size: 8 bits

This timer controls the amount of time the ICH10 PCI-to-PCI bridge will burst data on its secondary interface. The counter starts counting down from the assertion of FRAME#. If the grant is removed, then the expiration of this counter will result in the de-assertion of FRAME#. If the grant has not been removed, then the ICH10 PCI-to-PCI bridge may continue ownership of the bus.

Bit	Description
7:3	**Master Latency Timer Count (MLTC)** — R/W. This 5-bit field indicates the number of PCI clocks, in 8-clock increments, that the ICH10 remains as master of the bus.
2:0	Reserved

11.1.11 IOBASE_LIMIT—I/O Base and Limit Register (PCI-PCI—D30:F0)

Offset Address: 1Ch-1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:12	**I/O Limit Address Limit bits**[15:12] — R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	**I/O Limit Address Capability (IOLC)** — RO. This field indicates that the bridge does not support 32-bit I/O addressing.
7:4	**I/O Base Address (IOBA)** — R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Base Address Capability (IOBC)** — RO. This field indicates that the bridge does not support 32-bit I/O addressing.

11.1.12 SECSTS—Secondary Status Register (PCI-PCI—D30:F0)

Offset Address: 1Eh–1Fh
Default Value: 0280h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = Parity error **not** detected. 1 = Intel® ICH10 PCI bridge detected an address or data parity error on the PCI bus
14	**Received System Error** (**RSE)** — R/WC. 0 = SERR# assertion **not** received 1 = SERR# assertion is received on PCI.
13	**Received Master Abort (RMA)** — R/WC. 0 = No master abort. 1 = This bit is set whenever the bridge is acting as an initiator on the PCI bus and the cycle is master-aborted. For (G)MCH/ICH10 interface packets that have completion required, this must also cause a target abort to be returned and sets PSTS.STA. (D30:F0:06 bit 11)
12	**Received Target Abort (RTA)** — R/WC. 0 = No target abort. 1 = This bit is set whenever the bridge is acting as an initiator on PCI and a cycle is target-aborted on PCI. For (G)MCH/ICH10 interface packets that have completion required, this event must also cause a target abort to be returned, and sets PSTS.STA. (D30:F0:06 bit 11).
11	**Signaled Target Abort (STA)** — R/WC. 0 = No target abort. 1 = This bit is set when the bridge is acting as a target on the PCI Bus and signals a target abort.
10:9	DEVSEL# Timing (DEVT) — RO. 01h = Medium decode timing.
8	**Data Parity Error Detected (DPD)** — R/WC. 0 = Conditions described below **not** met. 1 = The ICH10 sets this bit when all of the following three conditions are met: • The bridge is the initiator on PCI. • PERR# is detected asserted or a parity error is detected internally • BCTRL.PERE (D30:F0:3E bit 0) is set.
7	Fast Back to Back Capable (FBC) — RO. Hardwired to 1 to indicate that the PCI to PCI target logic is capable of receiving fast back-to-back cycles.
6	Reserved
5	66 MHz Capable (66MHZ_CAP) — RO. Hardwired to 0. This bridge is 33 MHz capable only.
4:0	Reserved

11.1.13 MEMBASE_LIMIT—Memory Base and Limit Register (PCI-PCI—D30:F0)

Offset Address:	20h–23h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register defines the base and limit, aligned to a 1-MB boundary, of the non-prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31:20	**Memory Limit** (ML) — R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19:16	Reserved
15:4	**Memory Base** (MB) — R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	Reserved

11.1.14 PREF_MEM_BASE_LIMIT—Prefetchable Memory Base and Limit Register (PCI-PCI—D30:F0)

Offset Address:	24h–27h	Attribute:	R/W, RO
Default Value:	00010001h	Size:	32-bit

Defines the base and limit, aligned to a 1-MB boundary, of the prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31:20	**Prefetchable Memory Limit (PML)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19:16	64-bit Indicator (I64L) — RO. Indicates support for 64-bit addressing.
15:4	**Prefetchable Memory Base (PMB)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	64-bit Indicator (I64B) — RO. Indicates support for 64-bit addressing.

11.1.15 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI-PCI—D30:F0)

Offset Address: 28h–2Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)** — R/W. Upper 32-bits of the prefetchable address base.

11.1.16 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI-PCI—D30:F0)

Offset Address: 2C–2Fh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)** — R/W. Upper 32-bits of the prefetchable address limit.

11.1.17 CAPP—Capability List Pointer Register (PCI-PCI—D30:F0)

Offset Address: 34h
Default Value: 50h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)** — RO. This field indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

11.1.18 INTR—Interrupt Information Register (PCI-PCI—D30:F0)

Offset Address: 3Ch–3Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)** — RO. The PCI bridge does not assert an interrupt.
7:0	**Interrupt Line (ILINE)** — R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Since the bridge does not generate an interrupt, BIOS should program this value to FFh as per the PCI bridge specification.

11.1.19 BCTRL—Bridge Control Register (PCI-PCI—D30:F0)

Offset Address: 3Eh–3Fh
Default Value: 0000h
Attribute: R/WC, RO, R/W
Size: 16 bits

Bit	Description
15:12	Reserved
11	**Discard Timer SERR# Enable (DTE)** — R/W. This bit controls the generation of SERR# on the primary interface in response to the DTS bit being set: 0 = Do not generate SERR# on a secondary timer discard 1 = Generate SERR# in response to a secondary timer discard
10	**Discard Timer Status (DTS)** — R/WC. This bit is set to 1 when the secondary discard timer (see the SDT bit below) expires for a delayed transaction in the hard state.
9	**Secondary Discard Timer (SDT)** — R/W. This bit sets the maximum number of PCI clock cycles that the Intel® ICH10 waits for an initiator on PCI to repeat a delayed transaction request. The counter starts once the delayed transaction data is has been returned by the system and is in a buffer in the ICH10 PCI bridge. If the master has not repeated the transaction at least once before the counter expires, the ICH10 PCI bridge discards the transaction from its queue. 0 = The PCI master timeout value is between 2^{15} and 2^{16} PCI clocks 1 = The PCI master timeout value is between 2^{10} and 2^{11} PCI clocks
8	**Primary Discard Timer (PDT)** — R/W. This bit is R/W for software compatibility only.
7	Fast Back to Back Enable (FBE) — RO. Hardwired to 0. The PCI logic will not generate fast back-to-back cycles on the PCI bus.
6	**Secondary Bus Reset (SBR)** — R/W. This bit controls PCIRST# assertion on PCI. 0 = Bridge de-asserts PCIRST# 1 = Bridge asserts PCIRST#. When PCIRST# is asserted, the delayed transaction buffers, posting buffers, and the PCI bus are initialized back to reset conditions. The rest of the part and the configuration registers are not affected.
5	**Master Abort Mode (MAM)** — R/W. This bit controls the ICH10 PCI bridge's behavior when a master abort occurs: Master Abort on (G)MCH/ICH10 Interconnect (DMI): 0 = Bridge asserts TRDY# on PCI. It drives all 1s for reads, and discards data on writes. 1 = Bridge returns a target abort on PCI. Master Abort PCI (non-locked cycles): 0 = Normal completion status will be returned on the (G)MCH/ICH10 interconnect. 1 = Target abort completion status will be returned on the (G)MCH/ICH10 interconnect. **NOTE:** All locked reads will return a completer abort completion status on the (G)MCH/ICH10 interconnect.
4	**VGA 16-Bit Decode (V16D)** — R/W. This bit enables the ICH10 PCI bridge to provide 16-bits decoding of VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGAE bit in this register be set.

Bit	Description
3	**VGA Enable (VGAE)** — R/W. When set to a 1, the ICH10 PCI bridge forwards the following transactions to PCI regardless of the value of the I/O base and limit registers. The transactions are qualified by CMD.MSE (D30:F0:04 bit 1) and CMD.IOSE (D30:F0:04 bit 0) being set. • Memory addresses: 000A0000h-000BFFFFh • I/O addresses: 3B0h-3BBh and 3C0h-3DFh. For the I/O addresses, bits [63:16] of the address must be 0, and bits [15:10] of the address are ignored (i.e., aliased). The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be claimed.
2	**ISA Enable (IE)** — R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. If this bit is set, the ICH10 PCI bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SEE)** — R/W. This bit controls the forwarding of secondary interface SERR# assertions on the primary interface. When set, the PCI bridge will forward SERR# pin. • SERR# is asserted on the secondary interface. • This bit is set. • CMD.SEE (D30:F0:04 bit 8) is set.
0	Parity Error Response Enable (PERE) — R/W. 0 = Disable 1 = The ICH10 PCI bridge is enabled for parity error reporting based on parity errors on the PCI bus.

11.1.20 SPDH—Secondary PCI Device Hiding Register (PCI-PCI—D30:F0)

Offset Address: 40h–41h
Attribute: R/W, RO
Default Value: 0000h
Size: 16 bits

This register allows software to hide the PCI devices, either plugged into slots or on the motherboard.

Bit	Description
15:4	Reserved
3	**Hide Device 3 (HD3)** — R/W, RO. Same as bit 0 of this register, except for device 3 (AD[19])
2	**Hide Device 2 (HD2)** — R/W, RO. Same as bit 0 of this register, except for device 2 (AD[18])
1	**Hide Device 1 (HD1)** — R/W, RO. Same as bit 0 of this register, except for device 1 (AD[17])
0	**Hide Device 0 (HD0)** — R/W, RO. 0 = The PCI configuration cycles for this slot are not affected. 1 = Intel® ICH10 hides device 0 on the PCI bus. This is done by masking the IDSEL (keeping it low) for configuration cycles to that device. Since the device will not see its IDSEL go active, it will not respond to PCI configuration cycles and the processor will think the device is not present. AD[16] is used as IDSEL for device 0.

11.1.21 DTC—Delayed Transaction Control Register (PCI-PCI—D30:F0)

Offset Address: 44h–47h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31	**Discard Delayed Transactions (DDT)** — R/W. 0 = Logged delayed transactions are kept. 1 = The ICH10 PCI bridge will discard any delayed transactions it has logged. This includes transactions in the pending queue, and any transactions in the active queue, whether in the hard or soft DT state. The prefetchers will be disabled and return to an idle state. **NOTES:** If a transaction is running on PCI at the time this bit is set, that transaction will continue until either the PCI master disconnects (by de-asserting FRAME#) or the PCI bridge disconnects (by asserting STOP#). This bit is cleared by the PCI bridge when the delayed transaction queues are empty and have returned to an idle state. Software sets this bit and polls for its completion
30	**Block Delayed Transactions (BDT)** — R/W. 0 = Delayed transactions accepted 1 = The ICH10 PCI bridge will not accept incoming transactions which will result in delayed transactions. It will blindly retry these cycles by asserting STOP#. All postable cycles (memory writes) will still be accepted.
29:8	Reserved
7:6	**Maximum Delayed Transactions (MDT)** — R/W. This field controls the maximum number of delayed transactions that the ICH10 PCI bridge will run. Encodings are: 00 =) 2 Active, 5 pending 01 =) 2 active, no pending 10 =) 1 active, no pending 11 =) Reserved
5	Reserved
4	**Auto Flush After Disconnect Enable (AFADE)** — R/W. 0 = The PCI bridge will retain any fetched data until required to discard by producer/consumer rules. 1 = The PCI bridge will flush any prefetched data after either the PCI master (by de-asserting FRAME#) or the PCI bridge (by asserting STOP#) disconnects the PCI transfer.
3	**Never Prefetch (NP)** — R/W. 0 = Prefetch enabled 1 = The ICH10 will only fetch a single DW and will not enable prefetching, regardless of the command being an Memory read (MR), Memory read line (MRL), or Memory read multiple (MRM).

Bit	Description
2	**Memory Read Multiple Prefetch Disable (MRMPD)** — R/W. 0 = MRM commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read multiple (MRM) commands will fetch only up to a single, 64-byte aligned cache line.
1	**Memory Read Line Prefetch Disable (MRLPD)** — R/W. 0 = MRL commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read line (MRL) commands will fetch only up to a single, 64-byte aligned cache line.
0	**Memory Read Prefetch Disable (MRPD)** — R/W. 0 = MR commands will fetch up to a 64-byte aligned cache line. 1 = Memory read (MR) commands will fetch only a single DW.

11.1.22 BPS—Bridge Proprietary Status Register (PCI-PCI—D30:F0)

Offset Address: 48h–4Bh
Attribute: R/WC, RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:17	Reserved
16	**PERR# Assertion Detected (PAD)** — R/WC. This bit is set by hardware whenever the PERR# pin is asserted on the rising edge of PCI clock. This includes cases in which the chipset is the agent driving PERR#. It remains asserted until cleared by software writing a 1 to this location. When enabled by the PERR#-to-SERR# Enable bit (in the Bridge Policy Configuration register), a 1 in this bit can generate an internal SERR# and be a source for the NMI logic. This bit can be used by software to determine the source of a system problem.
15:7	Reserved
6:4	**Number of Pending Transactions (NPT)** — RO. This field indicates to debug software how many transactions are in the pending queue. Possible values are: 000 = No pending transaction 001 = 1 pending transaction 010 = 2 pending transactions 011 = 3 pending transactions 100 = 4 pending transactions 101 = 5 pending transactions 110 - 111 = Reserved **NOTE:** This field is not valid if DTC.MDT (offset 44h:bits 7:6) is any value other than '00'.
3:2	Reserved
1:0	**Number of Active Transactions (NAT)** — RO. This field indicates to debug software how many transactions are in the active queue. Possible values are: 00 = No active transactions 01 = 1 active transaction 10 = 2 active transactions 11 = Reserved

11.1.23 BPC—Bridge Policy Configuration Register (PCI-PCI—D30:F0)

Offset Address: 4Ch–4Fh
Default Value: 00001200h
Attribute: R/W
Size: 32 bits

Bit	Description
31:14	Reserved
13:8	**Upstream Read Latency Threshold (URLT)** — R/W: This field specifies the number of PCI clocks after internally enqueuing an upstream memory read request at which point the PCI target logic should insert wait states in order to optimize lead-off latency. When the master returns after this threshold has been reached and data has not arrived in the Delayed Transaction completion queue, then the PCI target logic will insert wait states instead of immediately retrying the cycle. The PCI target logic will insert up to 16 clocks of target initial latency (from FRAME# assertion to TRDY# or STOP# assertion) before retrying the PCI read cycle (if the read data has not arrived yet). Note that the starting event for this Read Latency Timer is not explicitly visible externally. A value of 0h disables this policy completely such that wait states will never be inserted on the read lead-off data phase. The default value (12h) specifies 18 PCI clocks (540 ns) and is approximately 4 clocks less than the typical idle lead-off latency expected for desktop ICH10 systems. This value may need to be changed by BIOS, depending on the platform.
7	**Subtractive Decode Policy (SDP)** — R/W. 0 = The PCI bridge always forwards memory and I/O cycles that are not claimed by any other device on the backbone (primary interface) to the PCI bus (secondary interface). 1 = The PCI bridge will not claim and forward memory or I/O cycles at all unless the corresponding Space Enable bit is set in the Command register. **NOTE:** The Boot BIOS Destination Selection strap can force the BIOS accesses to PCI. **CMD.MSE** | **BPC.SDP** | **Range** | **Forwarding Policy** 0 | 0 | Don't Care | Forward unclaimed cycles 0 | 1 | Don't Care | Forwarding Prohibited 1 | X | Within range | Positive decode and forward 1 | X | Outside | Subtractive decode & forward
6	**PERR#-to-SERR# Enable (PSE)** — R/W. When this bit is set, a 1 in the PERR# Assertion status bit (in the Bridge Proprietary Status register) will result in an internal SERR# assertion on the primary side of the bridge (if also enabled by the SERR# Enable bit in the primary Command register). SERR# is a source of NMI.
5	**Secondary Discard Timer Testmode (SDTT)** — R/W. 0 = The secondary discard timer expiration will be defined in BCTRL.SDT (D30:F0:3E, bit 9) 1 = The secondary discard timer will expire after 128 PCI clocks.
4:3	Reserved

Bit	Description
2	**Peer Decode Enable (PDE)** — R/W. 0 = The PCI bridge assumes that all memory cycles target main memory, and all I/O cycles are not claimed. 1 = The PCI bridge will perform peer decode on any memory or I/O cycle from PCI that falls outside of the memory and I/O window registers
1	Reserved
0	**Received Target Abort SERR# Enable (RTAE)** — R/W. When set, the PCI bridge will report SERR# when PSTS.RTA (D30:F0:06 bit 12) or SSTS.RTA (D30:F0:1E bit 12) are set, and CMD.SEE (D30:F0:04 bit 8) is set.

11.1.24 SVCAP—Subsystem Vendor Capability Register (PCI-PCI—D30:F0)

Offset Address: 50h–51h Attribute: RO
Default Value: 000Dh Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Value of 00h indicates this is the last item in the list.
7:0	**Capability Identifier (CID)** — RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

11.1.25 SVID—Subsystem Vendor IDs Register (PCI-PCI—D30:F0)

Offset Address: 54h–57h Attribute: R/WO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	**Subsystem Identifier (SID)** — R/WO. This field indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID)** — R/WO. This field indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

§ §

12 Gigabit LAN Configuration Registers

12.1 Gigabit LAN Configuration Registers (Gigabit LAN — D25:F0)

Note: Register address locations that are not shown in Table 12-1 should be treated as Reserved.

Table 12-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN —D25:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	020000h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MBARA	Memory Base Address A	00000000h	R/W, RO
14h–17h	MBARB	Memory Base Address B	00000000h	R/W, RO
18h–1Bh	MBARC	Memory Base Address C	00000001h	R/W, RO
2Ch–2Dh	SID	Subsystem ID	See register description	RO
2Eh–2Fh	SVID	Subsystem Vendor ID	See register description	RO
30h–33h	ERBA	Expansion ROM Base Address	See register description	RO
34h	CAPP	Capabilities List Pointer	C8h	RO
3Ch–3Dh	INTR	Interrupt Information	See register description	R/W, RO
3Eh	MLMG	Maximum Latency/Minimum Grant	00h	RO
C8h–C9h	CLIST1	Capabilities List 1	D001h	RO
CAh–CBh	PMC	PCI Power Management Capability	See register description	RO
CCh–CDh	PMCS	PCI Power Management Control and Status	See register description	R/WC, R/W, RO

Table 12-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN —D25:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
CFh	DR	Data Register	See register description	RO
D0h–D1h	CLIST2	Capabilities List 2	E005h	R/WO, RO
D2h–D3h	MCTL	Message Control	0080h	R/W, RO
D4h–D7h	MADDL	Message Address Low	See register description	R/W
D8h–DBh	MADDH	Message Address High	See register description	R/W
DCh–DDh	MDAT	Message Data	See register description	R/W
E0h–E1h	FLRCAP	Function Level Reset Capability	0009h	RO
E2h–E3h	FLRCLV	Function Level Reset Capability Length and Value	See register description	R/WO, RO
E4h–E5h	DEVCTRL	Device Control	0000h	R/W, RO

12.1.1 VID—Vendor Identification Register (Gigabit LAN—D25:F0)

Address Offset: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. The field may be auto-loaded from the NVM at address 0Eh during init time depending on the "Load Vendor/Device ID" bit field in NVM word 0Ah with a default value of 8086h.

12.1.2 DID—Device Identification Register (Gigabit LAN—D25:F0)

Address Offset: 02h–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 Gigabit LAN controller. The field may be auto-loaded from the NVM word 0Dh during initialization time depending on the "Load Vendor/Device ID" bit field in NVM word 0Ah.

12.1.3 PCICMD—PCI Command Register (Gigabit LAN—D25:F0)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0.
8	**SERR# Enable (SEE)** — R/W. 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0.
6	**Parity Error Response (PER)** — R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	Palette Snoop Enable (PSE) — RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) — RO. Hardwired to 0.
3	Special Cycle Enable (SCE) — RO. Hardwired to 0.
2	**Bus Master Enable (BME)** — R/W. 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN* device.
1	**Memory Space Enable (MSE)** — R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the Gigabit LAN device.
0	**I/O Space Enable (IOSE)** — R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the Gigabit LAN device.

12.1.4 PCISTS—PCI Status Register (Gigabit LAN—D25:F0)

Address Offset: 06h–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
14	**Signaled System Error (SSE)** — R/WC. 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
13	**Received Master Abort (RMA)** — R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the Gb LAN controller receives a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)** — R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.
11	**Signaled Target Abort (STA)** — R/WC. 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS) — RO. Hardwired to 0.
8	**Master Data Parity Error Detected (DPED)** — R/WC. 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backbone and PCIMD.PER (D25:F0, bit 6) is set.
7	Fast Back to Back Capable (FB2BC) — RO. Hardwired to 0.
6	Reserved
5	66 MHz Capable — RO. Hardwired to 0.
4	Capabilities List — RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status** — RO. Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).
2:0	Reserved

12.1.5 RID—Revision Identification Register (Gigabit LAN—D25:F0)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

12.1.6 CC—Class Code Register (Gigabit LAN—D25:F0)

Address Offset: 09h–0Bh
Default Value: 020000h
Attribute: RO
Size: 24 bits

Bit	Description
23:0	**Class Code**— RO. Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.

12.1.7 CLS—Cache Line Size Register (Gigabit LAN—D25:F0)

Address Offset: 0Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Cache Line Size** — R/W. This field is implemented by PCI devices as a read write field for legacy compatibility purposes but has no impact on any device functionality.

12.1.8 PLT—Primary Latency Timer Register (Gigabit LAN—D25:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Latency Timer (LT) — RO. Hardwired to ‘0’.

12.1.9 HT—Header Type Register (Gigabit LAN—D25:F0)

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Header Type (HT)** — RO. 00h = Indicates this is a single function device.

12.1.10 MBARA—Memory Base Address Register A (Gigabit LAN—D25:F0)

Address Offset:	10h–13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register. SW may only access whole DWord at a time.

Bit	Description
31:17	**Base Address (BA) — R/W**. Software programs this field with the base address of this region.
16:4	**Memory Size (MSIZE) — R/W**. Memory size is 128 KB.
3	**Prefetchable Memory (PM)** — RO. The GbE LAN controller does not implement prefetchable memory.
2:1	**Memory Type (MT)** — RO. Set to 00b indicating a 32 bit BAR.
0	**Memory / IO Space (MIOS)** — RO. Set to ‘0’ indicating a Memory Space BAR.

12.1.11 MBARB—Memory Base Address Register B (Gigabit LAN—D25:F0)

Address Offset:	14h–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

The internal registers that are used to access the LAN Space in the External FLASH device. Access to these registers are direct memory mapped offsets from the base address register. Software may only access a DWord at a time.

Bit	Description
31:12	**Base Address (BA) — R/W**. Software programs this field with the base address of this region.
11:4	**Memory Size (MSIZE) — R/W**. Memory size is 4 KB.
3	**Prefetchable Memory (PM)** — RO. The Gb LAN controller does not implement prefetchable memory.
2:1	**Memory Type (MT)** — RO. Set to 00b indicating a 32 bit BAR.
0	**Memory / IO Space (MIOS)** — RO. Set to ‘0’ indicating a Memory Space BAR.

12.1.12 MBARC—Memory Base Address Register C (Gigabit LAN—D25:F0)

Address Offset: 18h–1Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Internal registers, and memories, can be accessed using I/O operations. There are two 4B registers in the IO mapping window: Addr Reg and Data Reg. SW may only access a Dword at a time.

Bit	Description
31:5	**Base Address (BA) — R/W**. Software programs this field with the base address of this region.
4:1	**I/O Size (IOSIZE)** — RO. I/O space size is 32 Bytes.
0	**Memory / IO Space (MIOS)** — RO. Set to '1' indicating an I/O Space BAR.

12.1.13 SVID—Subsystem Vendor ID Register (Gigabit LAN—D25:F0)

Address Offset: 2Ch–2Dh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — RO. This value may be loaded automatically from the NVM Word 0Ch upon power up depending on the "Load Subsystem ID" bit field in NVM word 0Ah. A value of 8086h is default for this field upon power up if the NVM does not respond or is not programmed. All functions are initialized to the same value.

12.1.14 SID—Subsystem ID Register (Gigabit LAN—D25:F0)

Address Offset: 2Eh–2Fh
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** — RO. This value may be loaded automatically from the NVM Word 0Bh upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah with a default value of 0000h. This value is loadable from NVM word location 0Bh.

12.1.15 ERBA—Expansion ROM Base Address Register (Gigabit LAN—D25:F0)

Address Offset: 30h–33h
Default Value: See bit description
Attribute: RO
Size: 32 bits

Bit	Description
32:0	**Expansion ROM Base Address (ERBA)** — RO. This register is used to define the address and size information for boot-time access to the optional FLASH memory. If no Flash memory exists this register reports 00000000h.

12.1.16 CAPP—Capabilities List Pointer Register (Gigabit LAN—D25:F0)

Address Offset: 34h
Default Value: C8h
Attribute: R0
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)** — RO. Indicates that the pointer for the first entry in the capabilities list is at C8h in configuration space.

12.1.17 INTR—Interrupt Information Register (Gigabit LAN—D25:F0)

Address Offset: 3Ch–3Dh
Default Value: 0100h
Function Level Reset: No
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)** — RO. Indicates the interrupt pin driven by the Gb LAN controller. 01h = The Gb LAN controller implements legacy interrupts on INTA.
7:0	**Interrupt Line (ILINE)** — R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

12.1.18 MLMG—Maximum Latency/Minimum Grant Register (Gigabit LAN—D25:F0)

Address Offset: 3Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Maximum Latency/Minimum Grant (MLMG) — RO. Not used. Hardwired to 00h.

12.1.19 CLIST 1—Capabilities List Register 1 (Gigabit LAN—D25:F0)

Address Offset: C8h–C9h
Default Value: D001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Value of D0h indicates the location of the next pointer.
7:0	**Capability ID (CID)** — RO. Indicates the linked list item is a PCI Power Management Register.

12.1.20 PMC—PCI Power Management Capabilities Register (Gigabit LAN—D25:F0)

Address Offset: CAh–CBh Attribute: RO
Default Value: See bit descriptions Size: 16 bits
Function Level Reset: No (Bits 15:11 only)

Bit	Description
15:11	**PME_Support (PMES)** — RO. This five-bit field indicates the power states in which the function may assert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: **Condition** / **Function** / **Value** PM Ena=0 / No PME at all states / 0000b PM Ena & AUX-PWR=0 / PME at D0 and D3hot / 01001b PM Ena & AUX-PWR=1 / PME at D0, D3hot and D3cold / 11001b These bits are not reset by Function Level Reset.
10	**D2_Support (D2S)** — RO. The D2 state is not supported.
9	**D1_Support (D1S)** — RO. The D1 state is not supported.
8:6	**Aux_Current (AC)** — RO. Required current defined in the Data Register.
5	**Device Specific Initialization (DSI)** — RO. Set to ‘1’. The GbE LAN Controller requires its device driver to be executed following transition to the D0 un-initialized state.
4	Reserved
3	PME Clock (PMEC) — RO. Hardwired to ‘0’.
2:0	**Version (VS)** — RO. Hardwired to 010b to indicate support for *Revision 1.1 of the PCI Power Management Specification*.

12.1.21 PMCS—PCI Power Management Control and Status Register (Gigabit LAN—D25:F0)

Address Offset:	CCh–CDh	Attribute:	R/WC, R/W, RO
Default Value:	See bit description	Size:	16 bits
Function Level Reset:	No (Bit 8 only)		

Bit	Description
15	**PME Status (PMES)** — R/WC. This bit is set to '1' when the function detects a wake-up event independent of the state of the PMEE bit. Writing a "1" will clear this bit.
14:13	**Data Scale (DSC)** — R/W. This field indicates the scaling factor to be used when interpreting the value of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Else it equals 00b. For the manageability functions this field equals 10b (indicating 0.01 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Else it equals 00b.
12:9	**Data Select (DSL)** — R/W. This four-bit field is used to select which data is to be reported through the Data register (offset CFh) and Data_Scale field. These bits are writeable only when the Power Management is enabled via NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	**PME Enable (PMEE)** — R/W. If Power Management is enabled in the NVM, writing a '1' to this register will enable Wakeup. If Power Management is disabled in the NVM, writing a "1" to this bit has no affect, and will not set the bit to "1". This bit is not reset by Function Level Reset.
7:2	Reserved - Returns a value of '000000'.
1:0	**Power State (PS)** — R/W. This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enables in the NVM or this cycle will be ignored).

12.1.22 DR—Data Register (Gigabit LAN—D25:F0)

Address Offset: CFh
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Reported Data (RD)** — RO. This register is used to report power consumption and heat dissipation. This register is controlled by the Data_Select field in the PMCS (Offset CCh, bits 12:9), and the power scale is reported in the Data_Scale field in the PMCS (Offset CCh, bits 14:13). The data of this field is loaded from the NVM if PM is enabled in the NVM or with a default value of 00h otherwise.

12.1.23 CLIST 2—Capabilities List Register 2 (Gigabit LAN—D25:F0)

Address Offset: D0h–D1h
Default Value: E005h
Function Level Reset: No (Bits 15:8 only)
Attribute: R/WO, RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — R/WO. Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	**Capability ID (CID)** — RO. Indicates the linked list item is a Message Signaled Interrupt Register.

12.1.24 MCTL—Message Control Register (Gigabit LAN—D25:F0)

Address Offset: D2h–D3h
Default Value: 0080h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64-bit Capable (CID)** — RO. Set to '1' to indicate that the GbE LAN Controller is capable of generating 64-bit message addresses.
6:4	**Multiple Message Enable (MME)** — RO. Returns 000b to indicate that the GbE LAN controller only supports a single message.
3:1	**Multiple Message Capable (MMC)** — RO. The GbE LAN controller does not support multiple messages.
0	**MSI Enable (MSIE)** — R/W. 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.

12.1.25 MADDL—Message Address Low Register (Gigabit LAN—D25:F0)

Address Offset: D4h–D7h
Attribute: R/W
Default Value: See bit description
Size: 32 bits

Bit	Description
31:0	**Message Address Low (MADDL)** — R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

12.1.26 MADDH—Message Address High Register (Gigabit LAN—D25:F0)

Address Offset: D8h–DBh
Attribute: R/W
Default Value: See bit description
Size: 32 bits

Bit	Description
31:0	**Message Address High (MADDH)** — R/W. Written by the system to indicate the upper 32 bits of the address to use for the MSI memory write transaction.

12.1.27 MDAT—Message Data Register (Gigabit LAN—D25:F0)

Address Offset: DCh–DDh
Attribute: R/W
Default Value: See bit description
Size: 16 bits

Bit	Description
31:0	**Message Data (MDAT)** — R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWord transaction. The upper 16 bits of the transaction are written as 0000h.

12.1.28 FLRCAP—Function Level Reset Capability (Gigabit LAN—D25:F0)

Address Offset: E0h–E1h
Attribute: RO
Default Value: 0009h
Size: 16 bits

Bit	Description
15:8	**Next Pointer** — RO. This field provides an offset to the next capability item in the capability list. The value of 00h indicates the last item in the list.
7:0	**Capability ID** — RO. The value of this field depends on the FLRCSSEL bit. 13h = If FLRCSSEL = 0 09h = If FLRCSSEL = 1, indicating vendor specific capability.

12.1.29 FLRCLV—Function Level Reset Capability Length and Version (Gigabit LAN—D25:F0)

Address Offset:	E2h–E3h	Attribute:	R/WO, RO
Default Value:	See Description.	Size:	16 bits
Function Level Reset:	No (Bits 9:8 Only When FLRCSSEL = 0)		

When FLRCSSEL = 0, this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**Function Level Reset Capability** — R/WO. 1 = Support for Function Level Reset. This bit is not reset by Function Level Reset.
8	**TXP Capability** — R/WO. 1 = Indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length** — RO. The value of this field indicates the number of bytes of the vendor specific capability as require by the PCI spec. It has the value of 06h for the Function Level Reset capability.

When FLRCSSEL = 1, this register is defined as follows:

Bit	Description
15:12	**Vendor Specific Capability ID** — RO. A value of 2h in this field identifies this capability as Function Level Reset.
11:8	**Capability Version**— RO. The value of this field indicates the version of the Function Level Reset Capability. Default is 0h.
7:0	**Capability Length** — RO. The value of this field indicates the number of bytes of the vendor specific capability as require by the PCI spec. It has the value of 06h for the Function Level Reset capability.

12.1.30 DEVCTRL—Device Control (Gigabit LAN—D25:F0)

Address Offset:	E4-E5h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)** — R/W. 1 = Indicates the controller has issued Non-Posted requests which have not been completed. 0 = Indicates that completions for all Non-Posted requests have been received.
7:1	Reserved
0	**Initiate Function Level Reset** — RO. This bit is used to initiate an FLT transition. A write of '1' initiates the transition. Since hardware must not respond to any cycles until Function Level Reset completion, the value read by software from this bit is 0.

12.2 MBARA—Gigabit LAN Base Address A Registers

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register. This block is mapped into memory space, using the MBARA Base Address register see Section 12.1.10. SW may only access whole DWord at a time.

Table 12-2. Gigabit LAN Base Address A Registers Address Map (Gigabit LAN— D25:F0)

MBARA+Offset	Mnemonic	Register Name	Default	Type
00–03h	LDR4	LAN Device Initialization 4	14200100h	R/W
08–0Bh	LDR3	LAN Device Initialization 3	00080xxxh	RO
18–1Bh	LDCR2	LAN Device Control 2	01500000h	R/W
20–23h	LDCR4	LAN Device Control 4	1000xxxxh	R/W
F00h-F03h	LDCR5	LAN Device Control 5	00000000h	R/W
3004–3007h	LDR2	LAN Device Initialization 2	B2B577CCh	R/W
3024-3027h	LDR1	LAN Device Initialization 1	600060006h	R/W

12.2.1 LDR4—LAN Device Initialization Register 4 (Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + 0h
Default Value: 14200100h
Attribute: RO
Size: 32 bits

Bit	Description
31:25	Reserved
24	**LDR4 Field 1** — R/W. BIOS may set this bit to 1.
23:0	Reserved

12.2.2 LDR3—LAN Device Initialization Register 3 (Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + 8h
Default Value: 00080xxxh
Attribute: RO
Size: 32 bits

Bit	Description
31	**LDR3 Field 1** — RO. When set, this bit enables the automatic reduction of DMA frequency. This bit is loaded from word 13h in the NVM.
30:0	Reserved

12.2.3 LDCR2—LAN Device Control Register 2
(Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + 18h
Default Value: 01500000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:21	Reserved
20	**LAN PHY Power Down Enable (LPPDE)** — R/W. When set, enables the PHY to enter a low-power state when the LAN controller is at the DMoff / D3 or Dr and no WoL. This bit is loaded from word 13h in the NVM.
19	**LDCR2 Field 1** — R/W. This bit is loaded from word 13h in the NVM.
19:0	Reserved

12.2.4 LDCR4—LAN Device Control Register 4
(Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + 20h
Default Value: 1000xxxxh
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	BIOS may program this field.

12.2.5 LDR5—LAN Device Control Register 5
(Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + F00h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:6	Reserved
5	**LDCR5 Field 1** — R/W. BIOS may set this bit.
4:0	Reserved

12.2.6 LDR1—LAN Device Initialization Register 1
(Gigabit LAN Memory Mapped Base Address Register)

Address Offset: MBARA + 3024h
Default Value: 60006006h
Attribute: R/W
Size: 32 bits

Bit	Description
31:17	Reserved
16	**LDR1 Field 1** — R/W. BIOS must program this field to 1b.
15:0	Reserved

§ §§

13 LPC Interface Bridge Registers (D31:F0)

The LPC bridge function of the ICH10 resides in PCI Device 31:Function 0. This function contains many other functional units, such as DMA and Interrupt controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers.

Registers and functions associated with other functional units (EHCI, UHCI, etc.) are described in their respective sections.

13.1 PCI Configuration Registers (LPC I/F—D31:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 13-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0007h	R/W, RO
06h–07h	PCISTS	PCI Status	0210h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	06h	RO
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	80h	RO
2Ch–2Fh	SS	Sub System Identifiers	00000000h	R/WO
40h–43h	PMBASE	ACPI Base Address	00000001h	R/W, RO
44h	ACPI_CNTL	ACPI Control	00h	R/W
48h–4Bh	GPIOBASE	GPIO Base Address	00000001h	R/W, RO
4C	GC	GPIO Control	00h	R/W
60h–63h	PIRQ[*n*]_ROUT	PIRQ[A–D] Routing Control	80808080h	R/W
64h	SIRQ_CNTL	Serial IRQ Control	10h	R/W, RO
68h–6Bh	PIRQ[*n*]_ROUT	PIRQ[E–H] Routing Control	80808080h	R/W
6Ch–6Dh	LPC_IBDF	IOxAPIC Bus:Device:Function	00F8h	R/W
70h-71h	H0BDF	HPET 0 Bus:Device:Function(H0BDF)	00F8h	RW
72h-73h	H1BDF	HPET 1 Bus:Device:Function(H1BDF)	00F8h	RW

Table 13-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
74h-75h	H2BDF	HPET 2 Bus:Device:Function(H2BDF)	00F8h	RW
76h-77h	H3BDF	HPET 3 Bus:Device:Function(H3BDF)	00F8h	RW
78h-79h	H4BDF	HPET 4 Bus:Device:Function(H4BDF)	00F8h	RW
7Ah-7Bh	H5BDF	HPET 5 Bus:Device:Function(H5BDF)	00F8h	RW
7Ch-7Dh	H6BDF	HPET 6 Bus:Device:Function(H6BDF)	00F8h	RW
7Eh-7Fh	H7BDF	HPET 7 Bus:Device:Function(H7BDF)	00F8h	RW
80h	LPC_I/O_DEC	I/O Decode Ranges	0000h	R/W
82h–83h	LPC_EN	LPC I/F Enables	0000h	R/W
84h–87h	GEN1_DEC	LPC I/F Generic Decode Range 1	00000000h	R/W
88h–8Bh	GEN2_DEC	LPC I/F Generic Decode Range 2	00000000h	R/W
8Ch–8Eh	GEN3_DEC	LPC I/F Generic Decode Range 3	00000000h	R/W
90h–93h	GEN4_DEC	LPC I/F Generic Decode Range 4	00000000h	R/W
98h-9Bh	LGMR	LPC Generic Memory Range (Corporate Only)	00000000h	R/W
A0h–CFh		Power Management (See Section 13.8.1)		
D0h–D3h	FWH_SEL1	Firmware Hub Select 1	00112233h	R/W, RO
D4h–D5h	FWH_SEL2	Firmware Hub Select 2	4567h	R/W
D8h–D9h	FWH_DEC_EN1	Firmware Hub Decode Enable 1	FFCFh	R/W, RO
DCh	BIOS_CNTL	BIOS Control	00h	R/WLO, R/W, RO
E0h-E1h	FDCAP	Feature Detection Capability ID	0009h	RO
E2h	FDLEN	Feature Detection Capability Length	0Ch	RO
E3h	FDVER	Feature Detection Version	10h	RO
E4h-EBh	FDVCT	Feature Vector	See Description	RO
F0h-F3h	RCBA	Root Complex Base Address	00000000h	R/W

13.1.1 VID—Vendor Identification Register (LPC I/F—D31:F0)

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

13.1.2 DID—Device Identification Register (LPC I/F—D31:F0)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 LPC bridge. Refer to the *Intel® I/O Controller Hub (ICH10) Family* for the value of the Device ID Register.

13.1.3 PCICMD—PCI COMMAND Register (LPC I/F—D31:F0)

Offset Address:	04h–05h	Attribute:	R/W, RO
Default Value:	0007h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)** — R/W. The LPC bridge generates SERR# if this bit is set.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0.
6	**Parity Error Response Enable (PERE)** — R/W. 0 = No action is taken when detecting a parity error. 1 = Enables the ICH10 LPC bridge to respond to parity errors detected on backbone interface.
5	VGA Palette Snoop (VPS) — RO. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) — RO. Hardwired to 0.
3	Special Cycle Enable (SCE) — RO. Hardwired to 0.
2	Bus Master Enable (BME) — RO. Bus Masters cannot be disabled.
1	Memory Space Enable (MSE) — RO. Memory space cannot be disabled on LPC.
0	I/O Space Enable (IOSE) — RO. I/O space cannot be disabled on LPC.

13.1.4 PCISTS—PCI Status Register (LPC I/F—D31:F0)

Offset Address:	06h–07h	Attribute:	RO, R/WC
Default Value:	0210h	Size:	16-bit
Lockable:	No	Power Well:	Core

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. This bit is set when the LPC bridge detects a parity error on the internal backbone. The bit is set even if the PCICMD.PERE bit (D31:F0:04, bit 6) is 0. 0 = Parity Error Not detected. 1 = Parity Error detected.
14	**Signaled System Error (SSE)**— R/WC. This bit is set when the LPC bridge signals a system error to the internal SERR# logic.
13	**Master Abort Status (RMA)** — R/WC. 0 = Unsupported request status not received. 1 = The bridge received a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)** — R/WC. 0 = Completion abort not received. 1 = Completion with completion abort received from the backbone.
11	**Signaled Target Abort (STA)** — R/WC. 0 = Target abort Not generated on the backbone. 1 = LPC bridge generated a completion packet with target abort status on the backbone.
10:9	**DEVSEL# Timing Status (DEV_STS)** — RO. 01 = Medium Timing.
8	**Data Parity Error Detected (DPED)** — R/WC. 0 = All conditions listed below Not met. 1 = Set when all three of the following conditions are met: • LPC bridge receives a completion packet from the backbone from a previous request, • Parity error has been detected (D31:F0:06, bit 15) • PCICMD.PERE bit (D31:F0:04, bit 6) is set.
7	Fast Back to Back Capable (FBC): Reserved – bit has no meaning on the internal backbone.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) — Reserved – bit has no meaning on the internal backbone.
4	**Capabilities List (CLIST)** — RO. Capability list exists on the LPC bridge.
3	**Interrupt Status (IS)** — RO. The LPC bridge does not generate interrupts.
2:0	Reserved.

13.1.5 RID—Revision Identification Register (LPC I/F—D31:F0)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

13.1.6 PI—Programming Interface Register (LPC I/F—D31:F0)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface** — RO.

13.1.7 SCC—Sub Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Sub Class Code** — RO. 8-bit value that indicates the category of bridge for the LPC bridge. 01h = PCI-to-ISA bridge.

13.1.8 BCC—Base Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Bh Attribute: RO
Default Value: 06h Size: 8 bits

Bit	Description
7:0	**Base Class Code** — RO. This field is an 8-bit value that indicates the type of device for the LPC bridge. 06h = Bridge device.

13.1.9 PLT—Primary Latency Timer Register (LPC I/F—D31:F0)

Offset Address: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Master Latency Count (MLC) — Reserved.
2:0	Reserved.

13.1.10 HEADTYP—Header Type Register (LPC I/F—D31:F0)

Offset Address:	0Eh	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7	**Multi-Function Device** — RO. This bit is 1 to indicate a multi-function device.
6:0	**Header Type** — RO. This 7-bit field identifies the header layout of the configuration space.

13.1.11 SS—Sub System Identifiers Register (LPC I/F—D31:F0)

Offset Address:	2Ch–2Fh	Attribute:	R/WO
Default Value:	00000000h	Size:	32 bits

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Bit	Description
31:16	**Subsystem ID (SSID)** — R/WO. This is written by BIOS. No hardware action taken on this value.
15:0	**Subsystem Vendor ID (SSVID)** — R/WO. This is written by BIOS. No hardware action taken on this value.

13.1.12 PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)

Offset Address:	40h–43h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

This register sets base address for ACPI I/O registers, GPIO registers, and TCO I/O registers. These registers can be mapped anywhere in the 64-KB I/O space on 128-Byte boundaries.

Bit	Description
31:16	Reserved
15:7	**Base Address** — R/W. This field provides 128 bytes of I/O space for ACPI, GPIO, and TCO logic. This is placed on a 128-byte boundary.
6:1	Reserved
0	Resource Type Indicator (RTE) — RO. Hardwired to 1 to indicate I/O space.

13.1.13 ACPI_CNTL—ACPI Control Register (LPC I/F — D31:F0)

Offset Address:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Bit	Description
7	**ACPI Enable (ACPI_EN)** — R/W. 0 = Disable. 1 = Decode of the I/O range pointed to by the ACPI base register is enabled, and the ACPI power management function is enabled. Note that the APM power management ranges (B2/B3h) are always enabled and are not affected by this bit.
6:3	Reserved
2:0	**SCI IRQ Select (SCI_IRQ_SEL)** — R/W. Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20–23, and can be shared with other interrupts. **Bits** — **SCI Map** 000b — IRQ9 001b — IRQ10 010b — IRQ11 011b — Reserved 100b — IRQ20 (Only available if APIC enabled) 101b — IRQ21 (Only available if APIC enabled) When the interrupt is mapped to APIC interrupts 9, 10, or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

13.1.14 GPIOBASE—GPIO Base Address Register (LPC I/F — D31:F0)

Offset Address:	48h–4Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bit

Bit	Description
31:16	Reserved. Always 0.
15:7	**Base Address (BA) — RW**. Provides the 128 bytes of I/O space for GPIO.
6:1	Reserved. Always 0
0	RO. Hardwired to 1 to indicate I/O space.

13.1.15 GC—GPIO Control Register (LPC I/F — D31:F0)

Offset Address: 4Ch
Default Value: 00h
Attribute: R/W
Size: 8 bit

Bit	Description
7:5	Reserved.
4	**GPIO Enable (EN)** — R/W. This bit enables/disables decode of the I/O range pointed to by the GPIO Base Address register (D31:F0:48h) and enables the GPIO function. 0 = Disable. 1 = Enable.
3:1	Reserved.
0	**GPIO Lockdown Enable (GLE)** — R/W. This bit enables lockdown of the following GPIO registers: • Offset 00h: GPIO_USE_SEL • Offset 04h: GP_IO_SEL • Offset 0Ch: GP_LVL • Offset 30h: GPIO_USE_SEL2 • Offset 34h: GP_IO_SEL2 • Offset 38h: GP_LVL2 • Offset 40h: GPIO_USE_SEL3 (Corporate Only) • Offset 44h: GP_IO_SEL3 (Corporate Only) • Offset 48h: GP_LVL3 (Corporate Only) • Offset 60h: GP_RST_SEL 0 = Disable. 1 = Enable. When this bit is written from a 1-to-0 an SMI# is generated, if enabled. This ensures that only SMM code can change the above GPIO registers after they are locked down.

13.1.16 PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQA – 60h, PIRQB – 61h, PIRQC – 62h, PIRQD – 63h	Attribute:	R/W
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)** — R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. **NOTE:** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing** — R/W. (ISA compatible.) **Value** / **IRQ** / **Value** / **IRQ** 0000b Reserved — 1000b Reserved 0001b Reserved — 1001b IRQ9 0010b Reserved — 1010b IRQ10 0011b IRQ3 — 1011b IRQ11 0100b IRQ4 — 1100b IRQ12 0101b IRQ5 — 1101b Reserved 0110b IRQ6 — 1110b IRQ14 0111b IRQ7 — 1111b IRQ15

13.1.17 SIRQ_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0)

Offset Address:	64h	Attribute:	R/W, RO
Default Value:	10h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Serial IRQ Enable (SIRQEN)** — R/W. 0 = The buffer is input only and internally SERIRQ will be a 1. 1 = Serial IRQs will be recognized. The SERIRQ pin will be configured as SERIRQ.
6	**Serial IRQ Mode Select (SIRQMD)** — R/W. 0 = The serial IRQ machine will be in quiet mode. 1 = The serial IRQ machine will be in continuous mode. **NOTE:** For systems using Quiet Mode, this bit should be set to 1 (Continuous Mode) for at least one frame after coming out of reset before switching back to Quiet Mode. Failure to do so will result in the ICH10 not recognizing SERIRQ interrupts.
5:2	**Serial IRQ Frame Size (SIRQSZ)** — RO. Fixed field that indicates the size of the SERIRQ frame as 21 frames.
1:0	**Start Frame Pulse Width (SFPW)** — R/W. This is the number of PCI clocks that the SERIRQ pin will be driven low by the serial IRQ machine to signal a start frame. In continuous mode, the ICH10 will drive the start frame for the number of clocks specified. In quiet mode, the ICH10 will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. 00 = 4 clocks 01 = 6 clocks 10 = 8 clocks 11 = Reserved

13.1.18 PIRQ[n]_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQE – 68h, PIRQF – 69h, PIRQG – 6Ah, PIRQH – 6Bh	Attribute:	R/W
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)** — R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. **NOTE:** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing** — R/W. (ISA compatible.) **Value** **IRQ** **Value** **IRQ** 0000b Reserved 1000b Reserved 0001b Reserved 1001b IRQ9 0010b Reserved 1010b IRQ10 0011b IRQ3 1011b IRQ11 0100b IRQ4 1100b IRQ12 0101b IRQ5 1101b Reserved 0110b IRQ6 1110b IRQ14 0111b IRQ7 1111b IRQ15

13.1.19 LPC_IBDF—IOxAPIC Bus:Device:Function (LPC I/F—D31:F0)

Offset Address: 6Ch-6Dh
Default Value: 00F8h
Attribute: R/W
Size: 16 bit

Bit	Description
15:0	**IOxAPIC Bus:Device:Function (IBDF)**— R/W. This field specifies the bus:device:function that ICH10's IOxAPIC will be using for the following: • As the Requester ID when initiating Interrupt Messages to the processor. • As the Completer ID when responding to the reads targeting the IOxAPIC's Memory-Mapped I/O registers. The 16-bit field comprises the following: **Bits** — **Description** 15:8 — Bus Number 7:3 — Device Number 2:0 — Function Number This field defaults to Bus 0: Device 31: Function 0 after reset. BIOS can program this field to provide a unique bus:device:function number for the internal IOxAPIC.

13.1.20 LPC_HnBDF – HPET n Bus:Device:Function (LPC I/F—D31:F0)

Offset Address: H0BDF 70h-71h
H1BDF 72h-73h
H2BDF 74h-75h
H3BDF 76h-77h
H4BDF 78h-79h
H5BDF 7Ah-7Bh
H6BDF 7Ch-7Dh
H7BDF 7Eh-7Fh
Default Value: 00F8h
Attribute: R/W
Size: 16 bit

Bit	Description
15:0	**HPET n Bus:Device:Function (HnBDF)**— R/W. This field specifies the bus:device:function that ICH10's HPET n will be using in the following: • As the Requester ID when initiating Interrupt Messages to the CPU • As the Completer ID when responding to the reads targeting the corresponding HPET's Memory-Mapped I/O registers The 16-bit field comprises the following: **Bits** — **Description** 15:8 — Bus Number 7:3 — Device Number 2:0 — Function Number This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

13.1.21 LPC_I/O_DEC—I/O Decode Ranges Register (LPC I/F—D31:F0)

Offset Address: 80h
Default Value: 0000h
Attribute: R/W
Size: 16 bit

Bit	Description
15:13	Reserved
12	**FDD Decode Range** — R/W. This bit determines which range to decode for the FDD Port. 0 = 3F0h – 3F5h, 3F7h (Primary) 1 = 370h – 375h, 377h (Secondary)
11:10	Reserved
9:8	**LPT Decode Range** — R/W. This field determines which range to decode for the LPT Port. 00 = 378h – 37Fh and 778h – 77Fh 01 = 278h – 27Fh (port 279h is read only) and 678h – 67Fh 10 = 3BCh –3BEh and 7BCh – 7BEh 11 = Reserved
7	Reserved
6:4	**COMB Decode Range** — R/W. This field determines which range to decode for the COMB Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)
3	Reserved
2:0	**COMA Decode Range** — R/W. This field determines which range to decode for the COMA Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)

13.1.22 LPC_EN—LPC I/F Enables Register (LPC I/F—D31:F0)

Offset Address: 82h – 83h
Default Value: 0000h
Attribute: R/W
Size: 16 bit
Power Well: Core

Bit	Description
15:14	Reserved
13	**CNF2_LPC_EN** — R/W. Microcontroller Enable #2. 0 = Disable. 1 = Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface. This range is used for a microcontroller.
12	**CNF1_LPC_EN** — R/W. Super I/O Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface. This range is used for Super I/O devices.
11	**MC_LPC_EN** — R/W. Microcontroller Enable #1. 0 = Disable. 1 = Enables the decoding of the I/O locations 62h and 66h to the LPC interface. This range is used for a microcontroller.
10	**KBC_LPC_EN** — R/W. Keyboard Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 60h and 64h to the LPC interface. This range is used for a microcontroller.
9	**GAMEH_LPC_EN** — R/W. High Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 208h to 20Fh to the LPC interface. This range is used for a gameport.
8	**GAMEL_LPC_EN** — R/W. Low Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 200h to 207h to the LPC interface. This range is used for a gameport.
7:4	Reserved
3	**FDD_LPC_EN** — R/W. Floppy Drive Enable 0 = Disable. 1 = Enables the decoding of the FDD range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 12).
2	**LPT_LPC_EN** — R/W. Parallel Port Enable 0 = Disable. 1 = Enables the decoding of the LPTrange to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 9:8).
1	**COMB_LPC_EN** — R/W. Com Port B Enable 0 = Disable. 1 = Enables the decoding of the COMB range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 6:4).
0	**COMA_LPC_EN** — R/W. Com Port A Enable 0 = Disable. 1 = Enables the decoding of the COMA range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 3:2).

13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)

Offset Address: 84h – 87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)** — R/W. This address is aligned on a 128-byte boundary, and must have address lines 31:16 as 0. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN)** — R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F.

13.1.24 GEN2_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0)

Offset Address: 88h – 8Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask —** R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 2 Base Address (GEN1_BASE)** — R/W. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 2 Enable (GEN2_EN)** — R/W. 0 = Disable. 1 = Enable the GEN2 I/O range to be forwarded to the LPC I/F.

13.1.25 GEN3_DEC—LPC I/F Generic Decode Range 3 Register (LPC I/F—D31:F0)

Offset Address: 8Ch – 8Eh
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 3 Base Address (GEN3_BASE)** — R/W. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 3 Enable (GEN3_EN)** — R/W. 0 = Disable. 1 = Enable the GEN3 I/O range to be forwarded to the LPC I/F.

13.1.26 GEN4_DEC—LPC I/F Generic Decode Range 4 Register (LPC I/F—D31:F0)

Offset Address: 90h – 93h
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 4 Base Address (GEN4_BASE)** — R/W. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 4 Enable (GEN4_EN)** — R/W. 0 = Disable. 1 = Enable the GEN4 I/O range to be forwarded to the LPC I/F.

13.1.27 LGMR — LPC I/F Generic Memory Range (LPC I/F—D31:F0) (Corporate Only)

Offset Address: 98h – 9Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:16	**Memory Address[31:16]** — R/W. This field specifies a 64 KB memory block anywhere in the 4 GB memory space that will be decoded to LPC as standard LPC memory cycle if enabled.
15:1	Reserved
0	**LPC Memory Range Decode Enable** — R/W. When this bit is set to 1, then the range specified in bits 31:16 of this register is enabled for decoding to LPC.

13.1.28 FWH_SEL1—Firmware Hub Select 1 Register (LPC I/F—D31:F0)

Offset Address: D0h–D3h
Attribute: R/W, RO
Default Value: 00112233h
Size: 32 bits

Bit	Description
31:28	**FWH_F8_IDSEL** — RO. IDSEL for two 512-KB Firmware Hub memory ranges and one 128-KB memory range. This field is fixed at 0000. The IDSEL programmed in this field addresses the following memory ranges: FFF8 0000h – FFFF FFFFh FFB8 0000h – FFBF FFFFh 000E 0000h – 000F FFFFh
27:24	**FWH_F0_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h – FFF7 FFFFh FFB0 0000h – FFB7 FFFFh
23:20	**FWH_E8_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h – FFEF FFFFh FFA8 0000h – FFAF FFFFh
19:16	**FWH_E0_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h – FFE7 FFFFh FFA0 0000h – FFA7 FFFFh
15:12	**FWH_D8_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h – FFDF FFFFh FF98 0000h – FF9F FFFFh
11:8	**FWH_D0_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h – FFD7 FFFFh FF90 0000h – FF97 FFFFh
7:4	**FWH_C8_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h – FFCF FFFFh FF88 0000h – FF8F FFFFh
3:0	**FWH_C0_IDSEL** — R/W. IDSEL for two 512-KB Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h – FFC7 FFFFh FF80 0000h – FF87 FFFFh

13.1.29 FWH_SEL2—Firmware Hub Select 2 Register (LPC I/F—D31:F0)

Offset Address: D4h–D5h
Default Value: 4567h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	**FWH_70_IDSEL** — R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
11:8	**FWH_60_IDSEL** — R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
7:4	**FWH_50_IDSEL** — R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
3:0	**FWH_40_IDSEL** — R/W. IDSEL for two, 1-M Firmware Hub memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

13.1.30 FWH_DEC_EN1—Firmware Hub Decode Enable Register (LPC I/F—D31:F0)

Offset Address: D8h–D9h
Default Value: FFCFh
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	**FWH_F8_EN** — RO. This bit enables decoding two 512-KB Firmware Hub memory ranges, and one 128-KB memory range. 0 = Disable 1 = Enable the following ranges for the Firmware Hub FFF80000h – FFFFFFFFh FFB80000h – FFBFFFFFh
14	**FWH_F0_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFF00000h – FFF7FFFFh FFB00000h – FFB7FFFFh
13	**FWH_E8_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFE80000h – FFEFFFFFh FFA80000h – FFAFFFFFh
12	**FWH_E0_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub: FFE00000h – FFE7FFFFh FFA00000h – FFA7FFFFh
11	**FWH_D8_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFD80000h – FFDFFFFFh FF980000h – FF9FFFFFh
10	**FWH_D0_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFD00000h – FFD7FFFFh FF900000h – FF97FFFFh
9	**FWH_C8_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFC80000h – FFCFFFFFh FF880000h – FF8FFFFFh

Bit	Description
8	**FWH_C0_EN** — R/W. This bit enables decoding two 512-KB Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FFC00000h – FFC7FFFFh FF800000h – FF87FFFFh
7	**FWH_Legacy_F_EN** — R/W. This enables the decoding of the legacy 64KB range at F0000h – FFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the Firmware Hub F0000h – FFFFFh **NOTE:** The decode for the BIOS legacy F segment is enabled only by this bit and is not affected by the GEN_PMCON_1.iA64_EN bit.
6	**FWH_Legacy_E_EN** — R/W. This enables the decoding of the legacy 64KB range at E0000h – EFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the Firmware Hub E0000h – EFFFFh **NOTE:** The decode for the BIOS legacy E segment is enabled only by this bit and is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	Reserved
3	**FWH_70_EN** — R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
2	**FWH_60_EN** — R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
1	**FWH_50_EN** — R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
0	**FWH_40_EN** — R/W. Enables decoding two 1-M Firmware Hub memory ranges. 0 = Disable. 1 = Enable the following ranges for the Firmware Hub FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

NOTE: This register effects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. The ICH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

13.1.31 BIOS_CNTL—BIOS Control Register (LPC I/F—D31:F0)

Offset Address:	DCh	Attribute:	R/WLO, R/W, RO
Default Value:	00h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved
4	**Top Swap Status (TSS)** — RO. This bit provides a read-only path to view the state of the Top Swap bit that is at offset 3414h, bit 0.
3:2	**SPI Read Configuration (SRC)** — R/W. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 = Prefetch Enable Bit 2 = Cache Disable Settings are summarized below: **Bits 3:2** — **Description** 00b — **No prefetching, but caching enabled.** 64B demand reads load the read buffer cache with "valid" data, allowing repeated code fetches to the same line to complete quickly 01b — **No prefetching and no caching.** One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10b — **Prefetching and Caching enabled.** This mode is used for long sequences of short reads to consecutive addresses (i.e., shadowing). 11b — **Reserved. This is an invalid configuration**, caching must be enabled when prefetching is enabled.
1	**BIOS Lock Enable (BLE)** — R/WLO. 0 = Setting the BIOSWE will not cause SMIs. 1 = Enables setting the BIOSWE bit to cause SMIs. Once set, this bit can only be cleared by a PLTRST#.
0	**BIOS Write Enable (BIOSWE)** — R/W. 0 = Only read cycles result in Firmware Hub I/F cycles. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS Lock Enable (BLE) is also set, an SMI# is generated. This ensures that only SMI code can update BIOS.

13.1.32 FDCAP—Feature Detection Capability ID (LPC I/F—D31:F0)

Offset Address: E0h-E1h
Default Value: 0009h
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:8	**Next Item Pointer (NEXT)** — RO. Configuration offset of the next Capability Item. 00h indicates the last item in the Capability List.
7:0	**Capability ID** — RO. Indicates a Vendor Specific Capability.

13.1.33 FDLEN—Feature Detection Capability Length (LPC I/F—D31:F0)

Offset Address: E2h
Default Value: 0Ch
Attribute: RO
Size: 8 bit
Power Well: Core

Bit	Description
7:0	**Capability Length** — RO. Indicates the length of this Vendor Specific capability, as required by the PCI Specification.

13.1.34 FDVER—Feature Detection Version (LPC I/F—D31:F0)

Offset Address: E3h
Default Value: 10h
Attribute: RO
Size: 8 bit
Power Well: Core

Bit	Description
7:4	**Vendor-Specific Capability ID** — RO. A value of 1h in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	**Capability Version** — RO. This field indicates the version of the Feature Detection capability.

13.1.35 FDVCT—Feature Vector (LPC I/F—D31:F0)

Offset Address: E4h-EBh
Default Value: See Description
Attribute: RO
Size: 64 bit
Power Well: Core

Bit	Description
63:42	Reserved
41	Intel® Active Management Technology Release 5.0 Support Capability — RO. 0 = Professional 1 = Basic
40:38	Reserved
37	Intel Active Management Technology Capability — RO. 0 = Capable 1 = Disabled
36:6	Reserved
5	SATA RAID 0/1/5/10 Capability— RO. 0 = Capable 1 = Disabled
4:0	Reserved

13.1.36 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0)

Offset Address: F0-F3h
Default Value: 00000000h
Attribute: R/W
Size: 32 bit

Bit	Description
31:14	**Base Address (BA)** — R/W. Base Address for the root complex register block decode range. This address is aligned on a 16-KB boundary.
13:1	Reserved
0	**Enable (EN)** — R/W. When set, enables the range specified in BA to be claimed as the Root Complex Register Block.

13.2 DMA I/O Registers (LPC I/F—D31:F0)

Table 13-2. DMA Registers (Sheet 1 of 2)

Port	Alias	Register Name	Default	Type
00h	10h	Channel 0 DMA Base & Current Address	Undefined	R/W
01h	11h	Channel 0 DMA Base & Current Count	Undefined	R/W
02h	12h	Channel 1 DMA Base & Current Address	Undefined	R/W
03h	13h	Channel 1 DMA Base & Current Count	Undefined	R/W
04h	14h	Channel 2 DMA Base & Current Address	Undefined	R/W
05h	15h	Channel 2 DMA Base & Current Count	Undefined	R/W
06h	16h	Channel 3 DMA Base & Current Address	Undefined	R/W
07h	17h	Channel 3 DMA Base & Current Count	Undefined	R/W
08h	18h	Channel 0–3 DMA Command	Undefined	WO
		Channel 0–3 DMA Status	Undefined	RO
0Ah	1Ah	Channel 0–3 DMA Write Single Mask	000001XXb	WO
0Bh	1Bh	Channel 0–3 DMA Channel Mode	000000XXb	WO
0Ch	1Ch	Channel 0–3 DMA Clear Byte Pointer	Undefined	WO
0Dh	1Dh	Channel 0–3 DMA Master Clear	Undefined	WO
0Eh	1Eh	Channel 0–3 DMA Clear Mask	Undefined	WO
0Fh	1Fh	Channel 0–3 DMA Write All Mask	0Fh	R/W
80h	90h	Reserved Page	Undefined	R/W
81h	91h	Channel 2 DMA Memory Low Page	Undefined	R/W
82h	—	Channel 3 DMA Memory Low Page	Undefined	R/W
83h	93h	Channel 1 DMA Memory Low Page	Undefined	R/W
84h–86h	94h–96h	Reserved Pages	Undefined	R/W
87h	97h	Channel 0 DMA Memory Low Page	Undefined	R/W
88h	98h	Reserved Page	Undefined	R/W
89h	99h	Channel 6 DMA Memory Low Page	Undefined	R/W
8Ah	9Ah	Channel 7 DMA Memory Low Page	Undefined	R/W
8Bh	9Bh	Channel 5 DMA Memory Low Page	Undefined	R/W
8Ch–8Eh	9Ch–9Eh	Reserved Page	Undefined	R/W
8Fh	9Fh	Refresh Low Page	Undefined	R/W
C0h	C1h	Channel 4 DMA Base & Current Address	Undefined	R/W
C2h	C3h	Channel 4 DMA Base & Current Count	Undefined	R/W
C4h	C5h	Channel 5 DMA Base & Current Address	Undefined	R/W
C6h	C7h	Channel 5 DMA Base & Current Count	Undefined	R/W
C8h	C9h	Channel 6 DMA Base & Current Address	Undefined	R/W
CAh	CBh	Channel 6 DMA Base & Current Count	Undefined	R/W
CCh	CDh	Channel 7 DMA Base & Current Address	Undefined	R/W

Table 13-2. DMA Registers (Sheet 2 of 2)

Port	Alias	Register Name	Default	Type
CEh	CFh	Channel 7 DMA Base & Current Count	Undefined	R/W
D0h	D1h	Channel 4–7 DMA Command	Undefined	WO
		Channel 4–7 DMA Status	Undefined	RO
D4h	D5h	Channel 4–7 DMA Write Single Mask	000001XXb	WO
D6h	D7h	Channel 4–7 DMA Channel Mode	000000XXb	WO
D8h	D9h	Channel 4–7 DMA Clear Byte Pointer	Undefined	WO
DAh	DBh	Channel 4–7 DMA Master Clear	Undefined	WO
DCh	DDh	Channel 4–7 DMA Clear Mask	Undefined	WO
DEh	DFh	Channel 4–7 DMA Write All Mask	0Fh	R/W

13.2.1 DMABASE_CA—DMA Base and Current Address Registers (LPC I/F—D31:F0)

I/O Address: Ch. #0 = 00h; Ch. #1 = 02h; Ch. #2 = 04h; Ch. #3 = 06h; Ch. #5 = C4h Ch. #6 = C8h Ch. #7 = CCh;
Attribute: R/W
Size: 16 bit (per channel), but accessed in two 8-bit quantities
Default Value: Undefined
Lockable: No
Power Well: Core

Bit	Description
15:0	**Base and Current Address** — R/W. This register determines the address for the transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Address* register and copied to the *Current Address* register. On reads, the value is returned from the *Current Address* register. The address increments/decrements in the Current Address register after each transfer, depending on the mode of the transfer. If the channel is in auto-initialize mode, the Current Address register will be reloaded from the Base Address register after a terminal count is generated. For transfers to/from a 16-bit slave (channels 5–7), the address is shifted left one bit location. Bit 15 will be shifted into Bit 16. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing an address register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

13.2.2 DMABASE_CC—DMA Base and Current Count Registers (LPC I/F—D31:F0)

I/O Address: Ch. #0 = 01h; Ch. #1 = 03h; Ch. #2 = 05h; Ch. #3 = 07h; Ch. #5 = C6h; Ch. #6 = CAh; Ch. #7 = CEh;
Attribute:R/W
Size:16-bit (per channel), but accessed in two 8-bit quantities
Default Value: Undefined
Lockable: No
Power Well:Core

Bit	Description
15:0	**Base and Current Count** — R/W. This register determines the number of transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Count* register and copied to the *Current Count* register. On reads, the value is returned from the *Current Count* register. The actual number of transfers is one more than the number programmed in the Base Count Register (i.e., programming a count of 4h results in 5 transfers). The count is decrements in the Current Count register after each transfer. When the value in the register rolls from 0 to FFFFh, a terminal count is generated. If the channel is in auto-initialize mode, the Current Count register will be reloaded from the Base Count register after a terminal count is generated. For transfers to/from an 8-bit slave (channels 0–3), the count register indicates the number of bytes to be transferred. For transfers to/from a 16-bit slave (channels 5–7), the count register indicates the number of words to be transferred. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing a count register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

13.2.3 DMAMEM_LP—DMA Memory Low Page Registers (LPC I/F—D31:F0)

I/O Address: Ch. #0 = 87h; Ch. #1 = 83h; Ch. #2 = 81h; Ch. #3 = 82h; Ch. #5 = 8Bh; Ch. #6 = 89h; Ch. #7 = 8Ah;
Attribute:R/W
Size: 8-bit
Default Value: Undefined
Lockable: No
Power Well:Core

Bit	Description
7:0	**DMA Low Page** (ISA Address bits [23:16]) — R/W. This register works in conjunction with the DMA controller's Current Address Register to define the complete 24-bit address for the DMA channel. This register remains static throughout the DMA transfer. Bit 16 of this register is ignored when in 16 bit I/O count by words mode as it is replaced by the bit 15 shifted out from the current address register.

13.2.4 DMACMD—DMA Command Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 08h; Ch. #4–7 = D0h — Attribute:WO
Default Value: Undefined — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:5	Reserved. Must be 0.
4	**DMA Group Arbitration Priority** — WO. Each channel group is individually assigned either fixed or rotating arbitration priority. At part reset, each group is initialized in fixed priority. 0 = Fixed priority to the channel group 1 = Rotating priority to the group.
3	Reserved. Must be 0.
2	**DMA Channel Group Enable** — WO. Both channel groups are enabled following part reset. 0 = Enable the DMA channel group. 1 = Disable. Disabling channel group 4–7 also disables channel group 0–3, which is cascaded through channel 4.
1:0	Reserved. Must be 0.

13.2.5 DMASTA—DMA Status Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 08h; Ch. #4–7 = D0h — Attribute:RO
Default Value: Undefined — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:4	**Channel Request Status** — RO. When a valid DMA request is pending for a channel, the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware or a software request. Note that channel 4 is the cascade channel, so the request status of channel 4 is a logical OR of the request status for channels 0 through 3. 4 = Channel 0 5 = Channel 1 (5) 6 = Channel 2 (6) 7 = Channel 3 (7)
3:0	**Channel Terminal Count Status** — RO. When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Channel 4 is programmed for cascade, so the TC bit response for channel 4 is irrelevant. 0 = Channel 0 1 = Channel 1 (5) 2 = Channel 2 (6) 3 = Channel 3 (7)

13.2.6 DMA_WRSMSK—DMA Write Single Mask Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Ah; Ch. #4–7 = D4h — Attribute: WO
Default Value: 0000 01xx — Size: 8-bit
Lockable: No — Power Well: Core

Bit	Description
7:3	Reserved. Must be 0.
2	**Channel Mask Select** — WO. 0 = Enable DREQ for the selected channel. The channel is selected through bits [1:0]. Therefore, only one channel can be masked / unmasked at a time. 1 = Disable DREQ for the selected channel.
1:0	**DMA Channel Select** — WO. These bits select the DMA Channel Mode Register to program. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

13.2.7 DMACH_MODE—DMA Channel Mode Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Bh; Ch. #4–7 = D6h — Attribute:WO
Default Value: 0000 00xx — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:6	**DMA Transfer Mode** — WO. Each DMA channel can be programmed in one of four different modes: 00 = Demand mode 01 = Single mode 10 = Reserved 11 = Cascade mode
5	**Address Increment/Decrement Select** — WO. This bit controls address increment/decrement during DMA transfers. 0 = Address increment. (default after part reset or Master Clear) 1 = Address decrement.
4	**Autoinitialize Enable** — WO. 0 = Autoinitialize feature is disabled and DMA transfers terminate on a terminal count. A part reset or Master Clear disables autoinitialization. 1 = DMA restores the Base Address and Count registers to the current registers following a terminal count (TC).
3:2	**DMA Transfer Type** — WO. These bits represent the direction of the DMA transfer. When the channel is programmed for cascade mode, (bits[7:6] = 11) the transfer type is irrelevant. 00 = Verify – No I/O or memory strobes generated 01 = Write – Data transferred from the I/O devices to memory 10 = Read – Data transferred from memory to the I/O device 11 = Invalid
1:0	**DMA Channel Select** — WO. These bits select the DMA Channel Mode Register that will be written by bits [7:2]. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

13.2.8 DMA Clear Byte Pointer Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Ch; Ch. #4–7 = D8h — Attribute:WO
Default Value: xxxx xxxx — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:0	**Clear Byte Pointer** — WO. No specific pattern. Command enabled with a write to the I/O port address. Writing to this register initializes the byte pointer flip/flop to a known state. It clears the internal latch used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared by part reset and by the Master Clear command. This command precedes the first access to a 16-bit DMA controller register. The first access to a 16-bit register will then access the significant byte, and the second access automatically accesses the most significant byte.

13.2.9 DMA Master Clear Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Dh; Ch. #4–7 = DAh — Attribute:WO
Default Value: xxxx xxxx — Size: 8-bit

Bit	Description
7:0	**Master Clear** — WO. No specific pattern. Enabled with a write to the port. This has the same effect as the hardware Reset. The Command, Status, Request, and Byte Pointer flip/flop registers are cleared and the Mask Register is set.

13.2.10 DMA_CLMSK—DMA Clear Mask Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Eh; Ch. #4–7 = DCh — Attribute:WO
Default Value: xxxx xxxx — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:0	**Clear Mask Register** — WO. No specific pattern. Command enabled with a write to the port.

13.2.11 DMA_WRMSK—DMA Write All Mask Register (LPC I/F—D31:F0)

I/O Address: Ch. #0–3 = 0Fh; Ch. #4–7 = DEh — Attribute:R/W
Default Value: 0000 1111 — Size: 8-bit
Lockable: No — Power Well:Core

Bit	Description
7:4	Reserved. Must be 0.
3:0	**Channel Mask Bits** — R/W. This register permits all four channels to be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Mask Register – Write Single Mask Bit. In addition, this register has a read path to allow the status of the channel mask bits to be read. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count (unless the channel is in auto-initialization mode). Setting the bit(s) to a 1 disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). Bits [3:0] are set to 1 upon part reset or Master Clear. When read, bits [3:0] indicate the DMA channel [3:0] ([7:4]) mask status. Bit 0 = Channel 0 (4)1 = Masked, 0 = Not Masked Bit 1 = Channel 1 (5)1 = Masked, 0 = Not Masked Bit 2 = Channel 2 (6)1 = Masked, 0 = Not Masked Bit 3 = Channel 3 (7)1 = Masked, 0 = Not Masked **NOTE:** Disabling channel 4 also disables channels 0–3 due to the cascade of channels 0–3 through channel 4.

13.3 Timer I/O Registers (LPC I/F—D31:F0)

Port	Aliases	Register Name	Default Value	Type
40h	50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 0 Counter Access Port	Undefined	R/W
41h	51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 1 Counter Access Port	Undefined	R/W
42h	52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 2 Counter Access Port	Undefined	R/W
43h	53h	Timer Control Word	Undefined	WO
		Timer Control Word Register	XXXXXXX0b	WO
		Counter Latch Command	X0h	WO

13.3.1 TCW—Timer Control Word Register (LPC I/F—D31:F0)

I/O Address:	43h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following part reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Description
7:6	**Counter Select** — WO. The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command
5:4	**Read/Write Select** — WO. These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Counter Mode Selection** — WO. These bits select one of six possible modes of operation for the selected counter. **Bit Value** — **Mode** 000b — Mode 0 Out signal on end of count (=0) 001b — Mode 1 Hardware retriggerable one-shot x10b — Mode 2 Rate generator (divide by n counter) x11b — Mode 3 Square wave output 100b — Mode 4 Software triggered strobe 101b — Mode 5 Hardware triggered strobe
0	Binary/BCD Countdown Select — WO. 0 = Binary countdown is used. The largest possible binary count is 2^{16} 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 10^4

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described as follows:

RDBK_CMD—Read Back Command (LPC I/F—D31:F0)

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read. Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	**Read Back Command.** Must be 11 to select the Read Back Command
5	**Latch Count of Selected Counters**. 0 = Current count value of the selected counters will be latched 1 = Current count will not be latched
4	**Latch Status of Selected Counters**. 0 = Status of the selected counters will be latched 1 = Status will not be latched
3	**Counter 2 Select**. 1 = Counter 2 count and/or status will be latched
2	**Counter 1 Select**. 1 = Counter 1 count and/or status will be latched
1	**Counter 0 Select**. 1 = Counter 0 count and/or status will be latched.
0	Reserved. Must be 0.

LTCH_CMD—Counter Latch Command (LPC I/F—D31:F0)

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format, i.e., if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit	Description
7:6	**Counter Selection.** These bits select the counter for latching. If “11” is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4	**Counter Latch Command**. 00 = Selects the Counter Latch Command.
3:0	Reserved. Must be 0.

13.3.2 SBYTE_FMT—Interval Timer Status Byte Format Register (LPC I/F—D31:F0)

I/O Address: Counter 0 = 40h, Counter 1 = 41h, Counter 2 = 42h
Attribute: RO
Size: 8 bits per counter
Default Value: Bits[6:0] undefined, Bit 7=0

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit	Description
7	**Counter OUT Pin State** — RO. 0 = OUT pin of the counter is also a 0 1 = OUT pin of the counter is also a 1
6	**Count Register Status** — RO. This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading. 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	**Read/Write Selection Status** — RO. These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Mode Selection Status** — RO. These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Mode 0 — Out signal on end of count (=0) 001 = Mode 1 — Hardware retriggerable one-shot x10 = Mode 2 — Rate generator (divide by n counter) x11 = Mode 3 — Square wave output 100 = Mode 4 — Software triggered strobe 101 = Mode 5 — Hardware triggered strobe
0	**Countdown Type Status** — RO. This bit reflects the current countdown type. 0 = Binary countdown 1 = Binary Coded Decimal (BCD) countdown.

13.3.3 Counter Access Ports Register (LPC I/F—D31:F0)

I/O Address:	Counter 0 – 40h, Counter 1 – 41h, Counter 2 – 42h	Attribute:	R/W
Default Value:	All bits undefined	Size:	8 bit

Bit	Description
7:0	**Counter Port** — R/W. Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

13.4 8259 Interrupt Controller (PIC) Registers (LPC I/F—D31:F0)

13.4.1 Interrupt Controller I/O MAP (LPC I/F—D31:F0)

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ 0–7), and at A0h and A1h for the slave controller (IRQ 8–13). These registers have multiple functions, depending upon the data written to them. Table 13-3 shows the different register possibilities for each address.

Table 13-3. PIC Registers (LPC I/F—D31:F0)

Port	Aliases	Register Name	Default Value	Type
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Master PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Master PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Master PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Master PIC ICW4 Init. Cmd Word 4	01h	WO
		Master PIC OCW1 Op Ctrl Word 1	00h	R/W
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Slave PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Slave PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Slave PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Slave PIC ICW4 Init. Cmd Word 4	01h	WO
		Slave PIC OCW1 Op Ctrl Word 1	00h	R/W
4D0h	–	Master PIC Edge/Level Triggered	00h	R/W
4D1h	–	Slave PIC Edge/Level Triggered	00h	R/W

Note: Refer to note addressing active-low interrupt sources in 8259 Interrupt Controllers section (Section 5.8).

13.4.2 ICW1—Initialization Command Word 1 Register (LPC I/F—D31:F0)

Offset Address:	Master Controller – 20h Slave Controller – A0h	Attribute:	WO
		Size:	8 bit /controller
Default Value:	All bits undefined		

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special mask mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Description
7:5	**ICW/OCW Select** — WO. These bits are MCS-85 specific, and not needed. 000 = Should be programmed to “000”
4	**ICW/OCW Select** — WO. 1 = This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	**Edge/Level Bank Select (LTIM)** — WO. Disabled. Replaced by the edge/level triggered control registers (ELCR, D31:F0:4D0h, D31:F0:4D1h).
2	ADI — WO. 0 = Ignored for the ICH10. Should be programmed to 0.
1	**Single or Cascade (SNGL)** — WO. 0 = Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	**ICW4 Write Required (IC4)** — WO. 1 = This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

13.4.3 ICW2—Initialization Command Word 2 Register (LPC I/F—D31:F0)

Offset Address:	Master Controller – 21h Slave Controller – A1h	Attribute:	WO
		Size:	8 bit /controller
Default Value:	All bits undefined		

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the processor to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:3</td><td>Interrupt Vector Base Address — WO. Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.</td></tr>
<tr><td>2:0</td><td>Interrupt Request Level — WO. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code:

<table>
<tr><th>Code</th><th>Master Interrupt</th><th>Slave Interrupt</th></tr>
<tr><td>000b</td><td>IRQ0</td><td>IRQ8</td></tr>
<tr><td>001b</td><td>IRQ1</td><td>IRQ9</td></tr>
<tr><td>010b</td><td>IRQ2</td><td>IRQ10</td></tr>
<tr><td>011b</td><td>IRQ3</td><td>IRQ11</td></tr>
<tr><td>100b</td><td>IRQ4</td><td>IRQ12</td></tr>
<tr><td>101b</td><td>IRQ5</td><td>IRQ13</td></tr>
<tr><td>110b</td><td>IRQ6</td><td>IRQ14</td></tr>
<tr><td>111b</td><td>IRQ7</td><td>IRQ15</td></tr>
</table>
</td></tr>
</table>

13.4.4 ICW3—Master Controller Initialization Command Word 3 Register (LPC I/F—D31:F0)

Offset Address: 21h Attribute: WO
Default Value: All bits undefined Size: 8 bits

Bit	Description
7:3	0 = These bits must be programmed to 0.
2	**Cascaded Interrupt Controller IRQ Connection** — WO. This bit indicates that the slave controller is cascaded on IRQ2. When IRQ8#–IRQ15 is asserted, it goes through the slave controller's priority resolver. The slave controller's INTR output onto IRQ2. IRQ2 then goes through the master controller's priority solver. If it wins, the INTR signal is asserted to the processor, and the returning interrupt acknowledge returns the interrupt vector for the slave controller. 1 = This bit must always be programmed to a 1.
1:0	0 = These bits must be programmed to 0.

13.4.5 ICW3—Slave Controller Initialization Command Word 3 Register (LPC I/F—D31:F0)

Offset Address: A1h Attribute: WO
Default Value: All bits undefined Size: 8 bits

Bit	Description
7:3	0 = These bits must be programmed to 0.
2:0	**Slave Identification Code** — WO. These bits are compared against the slave identification code broadcast by the master controller from the trailing edge of the first internal INTA# pulse to the trailing edge of the second internal INTA# pulse. These bits must be programmed to 02h to match the code broadcast by the master controller. When 02h is broadcast by the master controller during the INTA# sequence, the slave controller assumes responsibility for broadcasting the interrupt vector.

13.4.6 ICW4—Initialization Command Word 4 Register (LPC I/F—D31:F0)

Offset Address: Master Controller – 021h Attribute:WO
Slave Controller – 0A1h Size: 8 bits
Default Value: 01h

Bit	Description
7:5	0 = These bits must be programmed to 0.
4	**Special Fully Nested Mode (SFNM)** — WO. 0 = Should normally be disabled by writing a 0 to this bit. 1 = Special fully nested mode is programmed.
3	**Buffered Mode (BUF)** — WO. 0 = Must be programmed to 0 for the ICH10. This is non-buffered mode.
2	**Master/Slave in Buffered Mode** — WO. Not used. 0 = Should always be programmed to 0.
1	**Automatic End of Interrupt (AEOI)** — WO. 0 = This bit should normally be programmed to 0. This is the normal end of interrupt. 1 = Automatic End of Interrupt (AEOI) mode is programmed.
0	**Microprocessor Mode** — WO. 1 = Must be programmed to 1 to indicate that the controller is operating in an Intel Architecture-based system.

13.4.7 OCW1—Operational Control Word 1 (Interrupt Mask) Register (LPC I/F—D31:F0)

Offset Address: Master Controller – 021h Attribute:R/W
Slave Controller – 0A1h Size: 8 bits
Default Value: 00h

Bit	Description
7:0	**Interrupt Request Mask** — R/W. When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

13.4.8 OCW2—Operational Control Word 2 Register (LPC I/F—D31:F0)

Offset Address: Master Controller – 020h Attribute:WO
Slave Controller – 0A0h Size: 8 bits
Default Value: Bit[4:0]=undefined, Bit[7:5]=001

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI) — WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used
4:3	**OCW2 Select** — WO. When selecting OCW2, bits 4:3 = “00”
2:0	**Interrupt Level Select** (L2, L1, L0) — WO. L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. **Code / Interrupt Level**: 000b IRQ0/8; 001b IRQ1/9; 010b IRQ2/10; 011b IRQ3/11 **Code / Interrupt Level**: 000b IRQ4/12; 001b IRQ5/13; 010b IRQ6/14; 011b IRQ7/15

13.4.9 OCW3—Operational Control Word 3 Register (LPC I/F—D31:F0)

Offset Address: Master Controller – 020h Attribute:WO
Slave Controller – 0A0h Size: 8 bits
Default Value: Bit[6,0]=0, Bit[7,4:2]=undefined, Bit[5,1]=1

Bit	Description
7	Reserved. Must be 0.
6	**Special Mask Mode (SMM)** — WO. 1 = The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits. Bit 5, the ESMM bit, must be set for this bit to have any meaning.
5	**Enable Special Mask Mode (ESMM)** — WO. 0 = Disable. The SMM bit becomes a “don't care”. 1 = Enable the SMM bit to set or reset the Special Mask Mode.
4:3	**OCW3 Select** — WO. When selecting OCW3, bits 4:3 = 01
2	**Poll Mode Command** — WO. 0 = Disable. Poll Command is not issued. 1 = Enable. The next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	**Register Read Command** — WO. These bits provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1=0, bit 0 will not affect the register read selection. When bit 1=1, bit 0 selects the register status returned following an OCW3 read. If bit 0=0, the IRR will be read. If bit 0=1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be “read IRR”. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

13.4.10 ELCR1—Master Controller Edge/Level Triggered Register (LPC I/F—D31:F0)

Offset Address: 4D0h
Default Value: 00h
Attribute: R/W
Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The cascade channel, IRQ2, the heart beat timer (IRQ0), and the keyboard controller (IRQ1), cannot be put into level mode.

Bit	Description
7	**IRQ7 ECL** — R/W. 0 = Edge. 1 = Level.
6	**IRQ6 ECL** — R/W. 0 = Edge. 1 = Level.
5	**IRQ5 ECL** — R/W. 0 = Edge. 1 = Level.
4	**IRQ4 ECL** — R/W. 0 = Edge. 1 = Level.
3	**IRQ3 ECL** — R/W. 0 = Edge. 1 = Level.
2:0	Reserved. Must be 0.

13.4.11 ELCR2—Slave Controller Edge/Level Triggered Register (LPC I/F—D31:F0)

Offset Address: 4D1h
Default Value: 00h
Attribute: R/W
Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The real time clock, IRQ8#, and the floating point error interrupt, IRQ13, cannot be programmed for level mode.

Bit	Description
7	**IRQ15 ECL** — R/W. 0 = Edge 1 = Level
6	**IRQ14 ECL** — R/W. 0 = Edge 1 = Level
5	Reserved. Must be 0.
4	**IRQ12 ECL** — R/W. 0 = Edge 1 = Level
3	**IRQ11 ECL** — R/W. 0 = Edge 1 = Level
2	**IRQ10 ECL** — R/W. 0 = Edge 1 = Level
1	**IRQ9 ECL** — R/W. 0 = Edge 1 = Level
0	Reserved. Must be 0.

13.5 Advanced Programmable Interrupt Controller (APIC)(D31:F0)

13.5.1 APIC Register Map (LPC I/F—D31:F0)

The APIC is accessed via an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The address bits 15:12 (Consumer Only) and 19:12 (Corporate Only) of the address range are programmable through bits 7:4 (Consumer Only) and 7:0 (Corporate Only) of OIC register (Chipset Config Registers:Offset 31FFh for Consumer Family and Offset 31FEh for Corporate family) The registers are shown in Table 13-4.

Table 13-4. APIC Direct Registers (LPC I/F—D31:F0)

Address	Mnemonic	Register Name	Size	Type
FEC_ _0000h (Corporate Only)	IND	Index	8 bits	R/W
FEC0_0000h (Consumer Only)	IND	Index	8 bits	R/W
FEC_ _0010h (Corporate Only)	DAT	Data	32 bits	R/W
FEC0_0010h (Consumer Only)	DAT	Data	32 bits	R/W
FEC_ _0040h (Corporate Only)	EOIR	EOI	32 bits	WO
FECO_0040h (Consumer Only)	EOIR	EOI	32 bits	WO

Table 13-5 lists the registers which can be accessed within the APIC via the Index Register. When accessing these registers, accesses must be done one dword at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Table 13-5. APIC Indirect Registers (LPC I/F—D31:F0)

Index	Mnemonic	Register Name	Size	Type
00	ID	Identification	32 bits	R/W
01	VER	Version	32 bits	RO
02–0F	—	Reserved	—	RO
10–11	REDIR_TBL0	Redirection Table 0	64 bits	R/W, RO
12–13	REDIR_TBL1	Redirection Table 1	64 bits	R/W, RO
…	…	…	…	…
3E–3F	REDIR_TBL23	Redirection Table 23	64 bits	R/W, RO
40–FF	—	Reserved	—	RO

13.5.2 IND—Index Register (LPC I/F—D31:F0)

Memory Address FEC0_0000h (Consumer Only) Attribute: R/W
FEC_ _0000h (Corporate Only)
Default Value: 00h Size: 8 bits

The Index Register will select which APIC indirect register to be manipulated by software. The selector values for the indirect registers are listed in Table 13-5. Software will program this register to select the desired APIC internal register

Bit	Description
7:0	**APIC Index** — R/W. This is an 8-bit pointer into the I/O APIC register table.

13.5.3 DAT—Data Register (LPC I/F—D31:F0)

Memory Address FEC0_0000h (Consumer Only) Attribute: R/W
FEC_ _0000h (Corporate Only)
Default Value: 00000000h Size: 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Index register. This register can only be accessed in dword quantities.

Bit	Description
7:0	**APIC Data** — R/W. This is a 32-bit register for the data to be read or written to the APIC indirect register (Figure 13-5) pointed to by the Index register (Memory Address FEC0_0000h).

13.5.4 EOIR—EOI Register (LPC I/F—D31:F0)

Memory Address	FEC0_0000h (Consumer Only) FEC_ _0000h (Corporate Only)	Attribute:	R/W
Default Value:	N/A	Size:	32 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/O APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit (Index Offset 10h, bit 14) for that I/O Redirection Entry will be cleared.

Note: If multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to 0. The interrupt which was prematurely reset will not be lost because if its input remained active when the Remote_IRR bit is cleared, the interrupt will be reissued and serviced at a later time. Note: Only bits 7:0 are actually used. Bits 31:8 are ignored by the ICH10.

Note: To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.

Bit	Description
31:8	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.
7:0	**Redirection Entry Clear** — WO. When a write is issued to this register, the I/O APIC will check this field, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

13.5.5 ID—Identification Register (LPC I/F—D31:F0)

Index Offset:	00h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Bit	Description
31:28	Reserved
27:24	**APIC ID** — R/W. Software must program this value before using the APIC.
23:16	Reserved
15	Scratchpad Bit.
14:0	Reserved

13.5.6 VER—Version Register (LPC I/F—D31:F0)

Index Offset:	01h	Attribute:	RO, RWO
Default Value:	00170020h	Size:	32 bits

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information also is in this register, to let software know how many interrupt are supported by this APIC.

Bit	Description
31:24	Reserved
23:16	**Maximum Redirection Entries (MRE)** — RWO. This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range 0 through 239. In the ICH10 this field is hardwired to 17h to indicate 24 interrupts. BIOS must write to this field after PLTRST# to lockdown the value. this allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to the OS.
15	**Pin Assertion Register Supported (PRQ)** — RO. Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	Reserved
7:0	**Version (VS)** — RO. This is a version number that identifies the implementation version.

13.5.7 REDIR_TBL—Redirection Table (LPC I/F—D31:F0)

Index Offset: 10h–11h (vector 0) through 3E–3Fh (vector 23)
Attribute: R/W, RO
Default Value: Bit 16 = 1. All other bits undefined
Size: 64 bits each, (accessed as two 32 bit quantities)

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgment from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request Register bit to go from 0 to 1. (In other words, if the interrupt was not already pending at the destination.)

Bit	Description
63:56	**Destination** — R/W. If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	**Extended Destination ID (EDID)** — RO. These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	Reserved
16	**Mask** — R/W. 0 = Not masked: An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked: Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	**Trigger Mode** — R/W. This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge triggered. 1 = Level triggered.
14	**Remote IRR** — R/W. This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received from a local APIC. 1 = Set when Local APIC/s accept the level interrupt sent by the I/O APIC.
13	**Interrupt Input Pin Polarity** — R/W. This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	**Delivery Status** — RO. This field contains the current status of the delivery of this interrupt. Writes to this bit have no effect. 0 = Idle. No activity for this interrupt. 1 = Pending. Interrupt has been injected, but delivery is not complete.

Bit	Description
11	**Destination Mode** — R/W. This field determines the interpretation of the Destination field. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with the Logical Destination in the Destination Format Register and Logical Destination Register in each Local APIC.
10:8	**Delivery Mode** — R/W. This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are listed in the note below:
7:0	**Vector** — R/W. This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

NOTE: Delivery Mode encoding:

000 = Fixed. Deliver the signal on the INTR signal of all processor cores listed in the destination. Trigger Mode can be edge or level.

001 = Lowest Priority. Deliver the signal on the INTR signal of the processor core that is executing at the lowest priority among all the processors listed in the specified destination. Trigger Mode can be edge or level.

010 = SMI (System Management Interrupt). Requires the interrupt to be programmed as edge triggered. The vector information is ignored but must be programmed to all 0s for future compatibility: **not supported**

011 = Reserved

100 = NMI. Deliver the signal on the NMI signal of all processor cores listed in the destination. Vector information is ignored. NMI is treated as an edge triggered interrupt even if it is programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The NMI delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the NMI pin is reached again, the interrupt will be sent again: **not supported**

101 = INIT. Deliver the signal to all processor cores listed in the destination by asserting the INIT signal. All addressed local APICs will assume their INIT state. INIT is always treated as an edge triggered interrupt even if programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The INIT delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the INIT pin is reached again, the interrupt will be sent again: **not supported**

110 = Reserved

111 = ExtINT. Deliver the signal to the INTR signal of all processor cores listed in the destination as an interrupt that originated in an externally connected 8259A compatible interrupt controller. The INTA cycle that corresponds to this ExtINT delivery will be routed to the external controller that is expected to supply the vector. Requires the interrupt to be programmed as edge triggered.

13.6 Real Time Clock Registers

13.6.1 I/O Register Address Map

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and will be accessible even when the RTC module is disabled (via the RTC configuration register). Registers A–D do not physically exist in the RAM.

All data movement between the host processor and the real-time clock is done through registers mapped to the standard I/O space. The register map appears in Table 13-6.

Table 13-6. RTC I/O Registers

I/O Locations	If U128E bit = 0	Function
70h and 74h	Also alias to 72h and 76h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Also alias to 73h and 77h	Real-Time Clock (Standard RAM) Target Register
72h and 76h		Extended RAM Index Register (if enabled)
73h and 77h		Extended RAM Target Register (if enabled)

NOTES:

1. I/O locations 70h and 71h are the standard legacy location for the real-time clock. The map for this bank is shown in Table 13-7. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid. If the extended RAM is not needed, it may be disabled.
2. Software must preserve the value of bit 7 at I/O addresses 70h and 74h. When writing to this address, software must first read the value, and then write the same value for bit 7 during the sequential address write. Note that port 70h is not directly readable. The only way to read this register is through Alt Access mode. Although RTC Index bits 6:0 are readable from port 74h, bit 7 will always return 0. If the NMI# enable is not changed during normal operation, software can alternatively read this bit once and then retain the value for all subsequent writes to port 70h.

13.6.2 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in Table 13-7.

Table 13-7. RTC (Standard) RAM Bank

Index	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh–7Fh	114 Bytes of User RAM

13.6.2.1 RTC_REGA—Register A

RTC Index:	0A	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other ICH10 reset signal.

Bit	Description
7	**Update In Progress (UIP)** — R/W. This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 488 µs. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	**Division Chain Select (DV[2:0])** — R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	**Rate Select (RS[3:0])** — R/W. Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to 0. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 µs 0100 = 244.141 µs 0101 = 488.281 µs 0110 = 976.5625 µs 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111= 500 ms

13.6.2.2 RTC_REGB—Register B (General Configuration)

RTC Index:	0Bh	Attribute:	R/W
Default Value:	U0U00UUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Update Cycle Inhibit (SET)** — R/W. Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to 0. When set is one, the BIOS may initialize time and calendar bytes safely. **NOTE:** This bit should be set then cleared early in BIOS POST after each powerup directly after coin-cell battery insertion.
6	**Periodic Interrupt Enable (PIE)** — R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur with a time base set with the RS bits of register A.
5	**Alarm Interrupt Enable (AIE)** — R/W. This bit is cleared by RTCRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or one a month.
4	**Update-Ended Interrupt Enable (UIE)** — R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the update cycle ends.
3	**Square Wave Enable (SQWE)** — R/W. This bit serves no function in the ICH10. It is left in this register bank to provide compatibility with the Motorola 146818B. The ICH10 has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	**Data Mode (DM)** — R/W. This bit specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD 1 = Binary
1	**Hour Format (HOURFORM)** — R/W. This bit indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = Twelve-hour mode. In twelve-hour mode, the seventh bit represents AM as 0 and PM as one. 1 = Twenty-four hour mode.
0	**Daylight Savings Legacy Software Support (DSLSWS)** — R/W. Daylight savings functionality is no longer supported. This bit is used to maintain legacy software support and has no associated functionality. If BUC.DSO bit is set, the DSLSWS bit continues to be R/W.

13.6.2.3 RTC_REGC—Register C (Flag Register)

RTC Index:	0Ch	Attribute:	RO
Default Value:	00U00000 (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Writes to Register C have no effect.

Bit	Description
7	**Interrupt Request Flag (IRQF)** — RO. IRQF = (PF * PIE) + (AF * AIE) + (UF *UFE). This bit also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	**Periodic Interrupt Flag (PF)** — RO. This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified via the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 when the tap specified by the RS bits of register A is 1.
5	**Alarm Flag (AF)** — RO. 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	**Update-Ended Flag (UF)** — RO. 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	Reserved. Will always report 0.

13.6.2.4 RTC_REGD—Register D (Flag Register)

RTC Index:	0Dh	Attribute:	R/W
Default Value:	10UUUUUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Valid RAM and Time Bit (VRT)** — R/W. 0 = This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	Reserved. This bit always returns a 0 and should be set to 0 for write cycles.
5:0	**Date Alarm** — R/W. These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return 0s to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

13.7 Processor Interface Registers (LPC I/F—D31:F0)

Table 13-8 is the register address map for the processor interface registers.

Table 13-8. Processor Interface PCI Register Address Map (LPC I/F—D31:F0)

Offset	Mnemonic	Register Name	Default	Type
61h	NMI_SC	NMI Status and Control	00h	R/W, RO
70h	NMI_EN	NMI Enable	80h	R/W (special)
92h	PORT92	Fast A20 and Init	00h	R/W
F0h	COPROC_ERR	Coprocessor Error	00h	WO
CF9h	RST_CNT	Reset Control	00h	R/W

13.7.1 NMI_SC—NMI Status and Control Register (LPC I/F—D31:F0)

I/O Address: 61h
Default Value: 00h
Lockable: No
Attribute: R/W, RO
Size: 8-bit
Power Well: Core

Bit	Description
7	**SERR# NMI Source Status (SERR#_NMI_STS)** — RO. 1 = Bit is set if a PCI agent detected a system error and pulses the PCI SERR# line and if bit 2 (PCI_SERR_EN) is cleared. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. When writing to port 61h, this bit must be 0. **NOTE:** This bit is set by any of the ICH10 internal sources of SERR; this includes SERR assertions forwarded from the secondary PCI bus, errors on a PCI Express* port, or other internal functions that generate SERR#.
6	**IOCHK# NMI Source Status (IOCHK_NMI_STS)** — RO. 1 = Bit is set if an LPC agent (via SERIRQ) asserted IOCHK# and if bit 3 (IOCHK_NMI_EN) is cleared. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. When writing to port 61h, this bit must be a 0.
5	**Timer Counter 2 OUT Status (TMR2_OUT_STS)** — RO. This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	**Refresh Cycle Toggle (REF_TOGGLE)** — RO. This signal toggles from either 0 to 1 or 1 to 0 at a rate that is equivalent to when refresh cycles would occur. When writing to port 61h, this bit must be a 0.
3	**IOCHK# NMI Enable (IOCHK_NMI_EN)** — R/W. 0 = Enabled. 1 = Disabled and cleared.
2	**PCI SERR# Enable (PCI_SERR_EN)** — R/W. 0 = SERR# NMIs are enabled. 1 = SERR# NMIs are disabled and cleared.

Bit	Description
1	**Speaker Data Enable (SPKR_DAT_EN)** — R/W. 0 = SPKR output is a 0. 1 = SPKR output is equivalent to the Counter 2 OUT signal value.
0	**Timer Counter 2 Enable (TIM_CNT2_EN)** — R/W. 0 = Disable 1 = Enable

13.7.2 NMI_EN—NMI Enable (and Real Time Clock Index) Register (LPC I/F—D31:F0)

I/O Address:	70h	Attribute:	R/W (special)
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Note: The RTC Index field is write-only for normal operation. This field can only be read in Alt-Access Mode. Note, however, that this register is aliased to Port 74h (documented in), and all bits are readable at that address.

Bits	Description
7	**NMI Enable (NMI_EN)** — R/W (special). 0 = Enable NMI sources. 1 = Disable All NMI sources.
6:0	**Real Time Clock Index Address (RTC_INDX)** — R/W (special). This data goes to the RTC to select which register or CMOS RAM address is being accessed.

13.7.3 PORT92—Fast A20 and Init Register (LPC I/F—D31:F0)

I/O Address:	92h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:2	Reserved
1	**Alternate A20 Gate (ALT_A20_GATE)** — R/W. This bit is Or'd with the A20GATE input signal to generate A20M# to the processor. 0 = A20M# signal can potentially go active. 1 = This bit is set when INIT# goes active.
0	**INIT_NOW** — R/W. When this bit transitions from a 0 to a 1, the ICH10 will force INIT# active for 16 PCI clocks.

13.7.4 COPROC_ERR—Coprocessor Error Register (LPC I/F—D31:F0)

I/O Address:	F0h	Attribute:	WO
Default Value:	00h	Size:	8-bits
Lockable:	No	Power Well:	Core

Bits	Description
7:0	**Coprocessor Error (COPROC_ERR)** — WO. Any value written to this register will cause IGNNE# to go active, if FERR# had generated an internal IRQ13. For FERR# to generate an internal IRQ13, the COPROC_ERR_EN bit (Chipset Config Registers:Offset 31FFh: bit 1 for Consumer Family and Offset 31FEh: bit 9 for Corporate family) must be 1.

13.7.5 RST_CNT—Reset Control Register (LPC I/F—D31:F0)

I/O Address:	CF9h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved
3	**Full Reset (FULL_RST)** — R/W. This bit is used to determine the states of SLP_S3#, SLP_S4#, and SLP_S5# after a CF9 hard reset (SYS_RST =1 and RST_CPU is set to 1), after PWROK going low (with RSMRST# high), or after two TCO timeouts. 0 = ICH10 will keep SLP_S3#, SLP_S4# and SLP_S5# high. 1 = ICH10 will drive SLP_S3#, SLP_S4# and SLP_S5# low for 3 – 5 seconds. **NOTE:** When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	**Reset CPU (RST_CPU)** — R/W. When this bit transitions from a 0 to a 1, it initiates a hard or soft reset, as determined by the SYS_RST bit (bit 1 of this register).
1	**System Reset (SYS_RST)** — R/W. This bit is used to determine a hard or soft reset to the processor. 0 = When RST_CPU bit goes from 0 to 1, the ICH10 performs a soft reset by activating INIT# for 16 PCI clocks. 1 = When RST_CPU bit goes from 0 to 1, the ICH10 performs a hard reset by activating PLTRST# and SUS_STAT# active for about 5-6 milliseconds. In this case, SLP_S3#, SLP_S4# and SLP_S5# state (assertion or de-assertion) depends on FULL_RST bit setting. The ICH10 main power well is reset when this bit is 1. It also resets the resume well bits (except for those noted throughout the EDS).
0	Reserved

13.8 Power Management Registers (PM—D31:F0)

The power management registers are distributed within the PCI Device 31: Function 0 space, as well as a separate I/O range. Each register is described below. Unless otherwise indicate, bits are in the main (core) power well.

Bits not explicitly defined in each register are assumed to be reserved. When writing to a reserved bit, the value should always be 0. Software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

13.8.1 Power Management PCI Configuration Registers (PM—D31:F0)

Table 13-9 shows a small part of the configuration space for PCI Device 31: Function 0. It includes only those registers dedicated for power management. Some of the registers are only used for Legacy Power management schemes.

Table 13-9. Power Management PCI Register Address Map (PM—D31:F0)

Offset	Mnemonic	Register Name	Default	Type
A0h	GEN_PMCON_1	General Power Management Configuration 1	0000h	R/W,, R/WO, RO
A2h	GEN_PMCON_2	General Power Management Configuration 2	00h	R/W, R/WC
A4h	GEN_PMCON_3	General Power Management Configuration 3	00h	R/W, R/WC
A6h	GEN_PMCON_LOCK	General Power Management Configuration Lock	00h	RO, R/WLO
A9h	Cx-STATE_CNF	Cx State Configuration	00h	R/W
AAh	C4-TIMING_CNT	C4 Timing Control	00h	R/W
ABh	BM_BREAK_EN	BM_BREAK_EN	00h	R/W
ACh	PMIR	Power Management Initialization	00000000h	R/W, R/WL
B8–BBh	GPI_ROUT	GPI Route Control	00000000h	R/W

13.8.1.1 GEN_PMCON_1—General PM Configuration 1 Register (PM—D31:F0)

Offset Address: A0h
Default Value: 0000h
Lockable: No

Attribute: R/W, RO, R/WO
Size: 16-bit
Usage: ACPI, Legacy
Power Well: Core

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>15:13</td><td>Reserved</td></tr>
<tr><td>12</td><td>C4 Disable — R/W. This bit disables the C4 feature.
0 = Enables C4
1 = Disables C4.
When C4 Disable is 1:
• I/O reads to the LVL4 register will be retried normally, but with no other action
• All C4 transition attempts are disabled, overriding C4onC3 and Pop-Down transition.</td></tr>
<tr><td>11</td><td>BMBUSY# Select (BMSEL)— R/W. This bit along with GPIO_USE_SEL[0] bit enables selection of BM_BUSY#/GPIO0 function on ICH pin as shown below:
<table>
<tr><th>GPIO_USE_SEL[0]</th><th>BMSEL</th><th>Pin Function</th></tr>
<tr><td>1</td><td>X</td><td>GPIO0</td></tr>
<tr><td>0</td><td>0</td><td>BMBUSY#</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>10</td><td>BIOS_PCI_EXP_EN — R/W. This bit acts as a global enable for the SCI associated with the PCI Express* ports.
0 = The various PCI Express ports and (G)MCH cannot cause the PCI_EXP_STS bit to go active.
1 = The various PCI Express ports and (G)MCH can cause the PCI_EXP_STS bit to go active.</td></tr>
<tr><td>9</td><td>PWRBTN_LVL — RO. This bit indicates the current state of the PWRBTN# signal.
0 = Low.
1 = High.</td></tr>
<tr><td>8</td><td>Reserved</td></tr>
<tr><td>7</td><td>Enter C4 When C3 Invoked (C4onC3_EN) — R/W. If this bit is set, then when software does a LVL3 read, the ICH10 transitions to the C4 state.</td></tr>
<tr><td>6 (Corporate Only)</td><td>Ignore Stop-Grant - R/W. Software sets this bit to indicate that the ICH must not wait for the Stop Grant (aka REQ_C2) cycle. This bit must be set for iA64 processors and CSI processors.</td></tr>
<tr><td>6 (Consumer Only)</td><td>i64_EN. Software sets this bit to indicate that the processor is an IA_64 processor, not an IA_32 processor. This may be used in various state machines where there are behavioral differences.</td></tr>
<tr><td>5 (Corporate Only)</td><td>Reserved</td></tr>
</table>

Bit	Description
5 (Consumer Only)	**CPU SLP# Enable (CPUSLP_EN)** — R/W. 0 = Disable. 1 = Enables the CPUSLP# signal to go active in the S1 state. This reduces the processor power. **NOTE:** CPUSLP# will go active on entry to C3 and C4 states even if this bit is not set.
4	**SMI_LOCK** — R/WO. When this bit is set, writes to the GLB_SMI_EN bit (PMBASE + 30h, bit 0) will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e., once set, this bit can only be cleared by PLTRST#).
3	Reserved
2	**PCI CLKRUN# Enable (CLKRUN_EN)** — R/W. 0 = Disable. ICH10 drives the CLKRUN# signal low. 1 = Enable CLKRUN# logic to control the system PCI clock via the CLKRUN# and STP_PCI# signals. **NOTE:** When the SLP_EN# bit is set, the ICH10 drives the CLKRUN# signal low regardless of the state of the CLKRUN_EN bit. This ensures that the PCI and LPC clocks continue running during a transition to a sleep state.
1:0	**Periodic SMI# Rate Select (PER_SMI_SEL)** — R/W. Set by software to control the rate at which periodic SMI# is generated. 00 = 64 seconds 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds

13.8.1.2 GEN_PMCON_2—General PM Configuration 2 Register (PM—D31:F0)

Offset Address:	A2h	Attribute:	R/W, R/WC
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Resume

Bit	Description
7	**DRAM Initialization Bit** — R/W. This bit does not effect hardware functionality in any way. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. • If the bit is 1, then the DRAM initialization was interrupted. • This bit is reset by the assertion of the RSMRST# pin.
6:5	**CPU PLL Lock Time (CPLT)** — R/W. This field indicates the amount of time that the processor needs to lock its PLLs. This is used wherever timing t270 (Chapter 8) applies. 00 = min 30.7 µs (Default) 01 = min 61.4 µs 10 = min 122.8 µs 11 = min 42 µs (min) to 48 µs (max) It is the responsibility of the BIOS to program the correct value in this field prior to the first transition to C3 or C4 states. **NOTES:** 1. The DPSLP-TO-(G)MCH Message bits (D31:F0:AAh, bits 1:0) act as an override to these bits. 2. These bits are not cleared by any type of reset except RSMRST# or a CF9h write.
4	**System Reset Status (SRS)** — R/WC. Software clears this bit by writing a 1 to it. 0 = SYS_RESET# button Not pressed. 1 = ICH10 sets this bit when the SYS_RESET# button is pressed. BIOS is expected to read this bit and clear it, if it is set. **NOTES:** 1. This bit is also reset by RSMRST# and CF9h resets. 2. The SYS_RESET# is implemented in the Main power well. This pin must be properly isolated and masked to prevent incorrectly setting this Suspend well status bit.
3	**CPU Thermal Trip Status (CTS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when PLTRST# is inactive and THRMTRIP# goes active while the system is in an S0 or S1 state. **NOTES:** 1. This bit is also reset by RSMRST#, and CF9h resets. It is not reset by the shutdown and reboot associated with the CPUTHRMTRIP# event. 2. The CF9h reset in the description refers to CF9h type core well reset which includes SYS_RST#, PWROK/VRMPWRGD low, SMBus hard reset, TCO Timeout. This type of reset will clear CTS bit.

Bit	Description
2	**Minimum SLP_S4# Assertion Width Violation Status** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31:F0:Offset A4h:bits 5:4). The ICH10 begins the timer when SLP_S4# is asserted during S4/S5 entry, or when the RSMRST# input is deasserted during G3 exit. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable (D31:F0:Offset A4h:bit 3). **NOTE:** This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
1	**CPU Power Failure (CPUPWR_FLR)** — R/W. 0 = Software (typically BIOS) clears this bit by writing a 0 to it. 1 = Indicates that the VRMPWRGD signal from the processor's VRM went low while the system was in an S0 or S1 state. **NOTE:** VRMPWRGD is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the Intel ICH10.
0	**PWROK Failure (PWROK_FLR)** — R/WC. 0 = Software clears this bit by writing a 1 to it, or when the system goes into a G3 state. 1 = This bit will be set any time PWROK goes low, when the system was in S0, or S1 state. The bit will be cleared only by software by writing a 1 to this bit or when the system goes to a G3 state. **NOTE:** See Chapter 5.13.6.3 for more details about the PWROK pin functionality. **NOTE:** In the case of true PWROK failure, PWROK will go low first before the VRMPWRGD.

13.8.1.3 GEN_PMCON_3—General PM Configuration 3 Register (PM—D31:F0)

Offset Address:	A4h	Attribute:	R/W, R/WC
Default Value:	0000h Consumer Only 0200h Corporate Only	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	RTC, SUS

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>15
(Corporate Only)</td><td>PME B0 S5 Disable (PME_B0_S5_DIS)— R/W. When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'.
Wakes from power states other than S5 are not affected by this policy bit.
The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below:
Y = Wake; N = Don't wake; B0 = PME_B0_EN; OV = WOL Enable Override
<table>
<tr><th>B0/OV</th><th>S1/S3/S4</th><th>S5</th></tr>
<tr><td>00</td><td>N</td><td>N</td></tr>
<tr><td>01</td><td>N</td><td>Y (LAN only)</td></tr>
<tr><td>11</td><td>Y (all PME B0 sources)</td><td>Y (LAN only)</td></tr>
<tr><td>01</td><td>Y (all PME B0 sources)</td><td>N</td></tr>
</table>
This bit is cleared by the RTCRST# pin.</td></tr>
<tr><td>15
(Consumer Only)</td><td>Reserved</td></tr>
<tr><td>14
(Corporate Only)</td><td>MAC Power Down During WOL Disable — R/W.
0 = MAC power down WOL is enabled if the hardware and software requirements are met.
1 = Integrated MAC remains powered whenever external suspend rails are powered.</td></tr>
<tr><td>13
(Corporate Only)</td><td>WOL Enable Override — R/W.
0 = WOL policies are determined by PMEB0 enable bit and appropriate LAN status bits
1 = Enable integrated LAN to wake the system in S5 only regardless of the value in the PME_B0_EN bit in the GPE0_EN register.
This bit is cleared by the RTCRST# pin.</td></tr>
<tr><td>12
(Corporate Only)</td><td>Disable SLP_S4# Stretching after G3:
0 = Enables stretching on SLP_S4# in conjunction with SLP_S4# Assertion Stretch Enable (bit 3) and the Minimum Assertion Width (bits 5:4)
1 = Disables stretching on SLP_S4# regardless of the state of the SLP_S4# Assertion Stretch Enable (bit 3).
This bit is cleared by the RTCRST# pin.
NOTE: This field is RO when the SLP_Sx# Stretching Policy Lock- Down bit is set.</td></tr>
</table>

Bit	Description
11:10 (Corporate Only)	**SLP_S3# Minimum Assertion Width:** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to ensure that the Main power supplies have been fully power-cycled. Valid Settings are: 00 = 60–100 us 01 = 1–1.2 ms 10 = 50–50.2 ms 11 = 2–2.0002 s This bit is cleared by the RSMRST# pin. **NOTE:** This field is RO when the SLP_Sx# Stretching Policy Lock-Down bit is set.
14:10 (Consumer Only)	Reserved
9	**General Reset Status** (GEN_RST_STS) — R/WC. This bit is set by hardware whenever PLTRST# asserts for any reason other than going into a software-entered sleep state (via PM1CNT.SLP_EN write) or a suspend well power failure (RSMRST# pin assertion). BIOS is expected to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on PM1_STS.WAK_STS = 1. If GEN_RST_STS = '1', the cold reset boot path should be followed rather than the resume path, regardless of the setting of WAK_STS. This bit is cleared by the RSMRST# pin.
8	**S4_STATE# Pin Disable** — R/W. 0 = The traditional SLP_S4# signal (without Intel Management Engine Overrides) is driven on the S4_STATE# Pin. GPIO26 defaults to its native functionality, S4_STATE#. 1 = The S4_STATE# pin functionality is disabled. The pin is configured as GPIO26, default as an output. **NOTE:** This bit is cleared by RTCRST#. This bit acts as an override for GPIO_USE_SEL[26].
7:6	**SWSMI_RATE_SEL** — R/W. This field indicates when the SWSMI timer will time out. Valid values are: 00 = 1.5 ms ± 0.6 ms 01 = 16 ms ± 4 ms 10 = 32 ms ± 4 ms 11 = 64 ms ± 4 ms These bits are not cleared by any type of reset except RTCRST#.
5:4	**SLP_S4# Minimum Assertion Width** — R/W. This field indicates the minimum assertion width of the SLP_S4# signal to ensure that the DRAMs have been safely power-cycled. Valid values are: 11 = 1 to 2 seconds 10 = 2 to 3 seconds 01 = 3 to 4 seconds 00 = 4 to 5 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered. 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. RTCRST# forces this field to the conservative default state (00b). **NOTE:** This field is RO when the SLP_S4# Stretching Policy Lock-Down bit is set.

Bit	Description
3	**SLP_S4# Assertion Stretch Enable** — R/W. 0 = The SLP_S4# minimum assertion time is 1 to 2 RTCCLK. 1 = The SLP_S4# signal minimally assert for the time specified in bits 5:4 of this register. This bit is cleared by RTCRST#. **NOTE:** This bit is RO when the SLP_S4# Stretching Policy Lock-Down bit is set.
2	**RTC Power Status (RTC_PWR_STS)** — R/W. This bit is set when RTCRST# indicates a weak or missing battery. The bit is not cleared by any type of reset. The bit will remain set until the software clears it by writing a 0 back to this bit position.
1 (Corporate Only)	**Power Failure (PWR_FLR)** — R/WC. This bit is in the SUS well, and defaults to a '1' based on RSMRST# assertion (not cleared by any type of reset). 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to it. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed.
1 (Consumer Only)	**Power Failure (PWR_FLR)** — R/WC. This bit is in the RTC well, and is not cleared by any type of reset except RTCRST#. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to it. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. **NOTE:** Clearing CMOS in an ICH-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
0 (Corporate Only)	**AFTERG3_EN** — R/W. This bit determines what state to go to when power is re-applied after a power failure (G3 state). 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is cleared by RTCRST#.
0 (Consumer Only)	**AFTERG3_EN** — R/W. This bit determines what state to go to when power is re-applied after a power failure (G3 state). This bit is in the RTC well and is only cleared by writes of 06h or 0Eh to CF9h (when the CF9h global reset bit is clear), receiving hard reset command with or without power cycle from SMBus or RTCRST#. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure. **NOTE:** This bit is set any time a Power Button Override occurs (i.e., the power button is pressed for at least 4 consecutive seconds), due to the corresponding bit in the SMBus unconditional power down message, due to an internal thermal sensor catastrophic condition and the assertion of THRMTRIP#.

NOTE: RSMRST# is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the ICH10.

13.8.1.4 GEN_PMCON_LOCK- General Power Management Configuration Lock Register

Offset Address:	A6h	Attribute:	RO, R/WLO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
7	**Unlocked C-State Transition** — RO. This bit is set by hardware when a processor power state (C-State) transition deeper than C2 occurs and the C-STATE_CONFIG_LOCK bit is not set. This bit is cleared by PLTRST# and is not writable by software.
6:3	Reserved
2	**SLP_S4# Stretching Policy Lock-Down** — R/WLO. When set to 1, this bit locks down the SLP_S4# Minimum Assertion Width, the SLP_S4# Assertion Stretch Enable (Corporate Only), the Disable SLP_S4# Stretching after G3 (Corporate Only) and SLP_S4# Assertion Stretch Enable (Consumer Only) bits in the GEN_PMCON_3 register, making them read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. This bit is cleared by platform reset.
1	**ACPI_BASE_LOCK** — R/WLO. When set to 1, this bit locks down the ACPI Base Address Register (ABASE) at offset 40h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
0	C-STATE_CONFIG_LOCK — R/WLO. When set to 1, this bit locks down the C-State configuration parameters. The following configuration bits become read-only when this bit is set: • IA64_EN (GEN_PMCON_1, bit 6) • C4_DISABLE (GEN_PMCON_1, bit 12) • CPU_PLL_LOCK_TIME (GEN_PMCON_2, bits 6:5) • The entire C4 Timing Control Register (C4_TIMING_CNT) This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

13.8.1.5 Cx-STATE_CNF—Cx State Configuration Register (PM—D31:F0)

Offset Address:	A9h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

This register is used to enable C-state related modes.

Bit	Description
7	**SCRATCHPAD (SP)** — R/W.
6:5	Reserved
4	**Popdown Mode Enable (PDME)** — R/W. This bit is used in conjunction with the PUME bit (D31:F0:A9h, bit 3). If PUME is 0, then this bit must also be 0. 0 = The ICH10 will not attempt to automatically return to a previous C3 or C4 state. 1 = When this bit is a 1 and ICH10 observes that there are no bus master requests, it can return to a previous C3 or C4 state. **NOTE:** This bit is separate from the PUME bit to cover cases where latency issues permit POPUP but not POPDOWN.
3	**Popup Mode Enable (PUME)** — R/W. When this bit is a 0, the ICH10 behaves like ICH5, in that bus master traffic is a break event, and it will return from C3/C4 to C0 based on a break event. See Chapter 5.13.5 for additional details on this mode. 0 = The ICH10 will treat Bus master traffic a break event, and will return from C3/C4 to C0 based on a break event. 1 = When this bit is a 1 and ICH10 observes a bus master request, it will take the system from a C3 or C4 state to a C2 state and auto enable bus masters. This will let snoops and memory access occur.
2	**Report Zero for BM_STS (BM_STS_ZERO_EN)** — R/W. 0 = The ICH10 sets BM_STS (PMBASE + 00h, bit 4) if there is bus master activity from PCI, PCI Express* and internal bus masters. 1 = When this bit is a 1, ICH10 will not set the BM_STS if there is bus master activity from PCI, PCI Express and internal bus masters. **NOTES:** 1. If the BM_STS bit is already set when the BM_STS_ZERO_EN bit is set, the BM_STS bit will remain set. Software will still need to clear the BM_STS bit. 2. It is expected that if the PUME bit (this register, bit 3) is set, the BM_STS_ZERO_EN bit should also be set. 3. BM_STS will be set by LPC DMA or LPC masters, even if BM_STS_ZERO_EN is set.
1:0	Reserved

13.8.1.6 C4-TIMING_CNT—C4 Timing Control Register (PM—D31:F0)

Offset Address:	AAh	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

This register is used to enable C-state related modes.

Bit	Description
7	Reserved
6	**Slow-C4 Exit Enable** —When 1, this bit enables the Slow-C4 Exit functionality.
5:4	Reserved
3:2	**DPRSLPVR to STPCPU** — R/W. This field selects the amount of time that the ICH10 waits for from the deassertion of DPRSLPVR to the deassertion of STP_CPU#. This provides a programmable time for the processor's voltage to stabilize when exiting from a C4 state. This thus changes the value for t266a. **Bits** / **t266a$_{min}$** / **t266a$_{max}$** / **Comment** 00b — 95 µs — 101 µs — Default 01b — 22 µs — 28 µs — Value used for "Fast" VRMs 10b — 34 µs — 40 µs — Value used for "Fast" VRMs 11b — Reserved
1:0	**DPSLP-TO-MCH Message**— R/W. This field selects the DPSLP# deassertion to (G)MCH message time (t270). Normally this value is determined by the CPU_PLL_LOCK_TIME field in the GEN_PMCON_2 register. When this field is non-zero, then the values in this register have higher priority. It is software's responsibility to program these fields in a consistent manner. **Bits** / **t270** 00b — Use value is CPU_PLL_LOCK_TIME field (default is 30 µs) 01b — 20 µs 10b — 15 µs 11b — 10 µs

13.8.1.7 BM_BREAK_EN Register (PM—D31:F0)

Offset Address:	ABh	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7	**STORAGE_BREAK_EN** — R/W. 0 = Serial ATA traffic will not act as a break event. 1 = Serial ATA traffic acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. Serial ATA master activity will cause BM_STS to be set and will cause a break from C3/C4.
6	**PCIE_BREAK_EN** — R/W. 0 = PCI Express* traffic will not act as a break event. 1 = PCI Express traffic acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. PCI Express master activity will cause BM_STS to be set and will cause a break from C3/C4.
5	**PCI_BREAK_EN** — R/W. 0 = PCI traffic will not act as a break event. 1 = PCI traffic acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. PCI master activity will cause BM_STS to be set and will cause a break from C3/C4.
4:3	Reserved
2	**EHCI_BREAK_EN** — R/W. 0 = EHCI traffic will not act as a break event. 1 = EHCI traffic acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. EHCI master activity will cause BM_STS to be set and will cause a break from C3/C4.
1	**UHCI_BREAK_EN** — R/W. 0 = UHCI traffic will not act as a break event. 1 = USB traffic from any of the internal UHCIs acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. UHCI master activity will cause BM_STS to be set and will cause a break from C3/C4.
0	**HDA_BREAK_EN** — R/W. 0 = Intel® High Definition Audio traffic will not act as a break event. 1 = Intel High Definition Audio traffic acts as a break event, even if the BM_STS-ZERO_EN and POPUP_EN bits are set. Intel High Definition Audio master activity will cause BM_STS to be set and will cause a break from C3/C4.

13.8.1.8 PMIR—Power Management Initialization Register (PM—D31:F0)

Offset Address:	ACh	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit

Bit	Description
31	**CF9h Lockdown (CF9LOCK):** When set, this bit locks the bits in this register into their current value. This register is reset by a CF9h reset.
30	**PMIR Field 2 —** R/W. BIOS must program this bit to 1b.
29:21	Reserved
20	**CF9h Global Reset (CF9GR)**— R/W. When set, a CF9h write of 6h or Eh will cause a Global reset of both the Host and Intel ME partitions. If this bit is cleared, a CF9h write of 6h or Eh will only reset the host partition. This bit field is not reset by a CF9h reset.
19:15	Reserved
14	**Intel® AT Host Reset Trigger Enable - R/W.** When set this bit enables bits [1:0] in the CIR11 register.
13:10	Reserved
9:8	**PMIR Field 0** — R/W. BIOS must program these bits to 11b.
7:0	Reserved

13.8.1.9 GPIO_ROUT—GPIO Routing Control Register (PM—D31:F0)

Offset Address:	B8h – BBh	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Resume

Bit	Description
31:30	**GPIO15 Route** — R/W. See bits 1:0 for description.
Same pattern for GPIO14 through GPIO3	
5:4	**GPIO2 Route** — R/W. See bits 1:0 for description.
3:2	**GPIO1 Route** — R/W. See bits 1:0 for description.
1:0	**GPIO0 Route** — R/W. GPIO[15:0] can be routed to cause an SMI or SCI when the GPIO[n]_STS bit is set. If the GPIO0 is not set to an input, this field has no effect. If the system is in an S1–S5 state and if the GPE0_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an SMI# or SCI. 00 = No effect. 01 = SMI# (if corresponding ALT_GPI_SMI_EN bit is also set) 10 = SCI (if corresponding GPE0_EN bit is also set) 11 = Reserved

Note: GPIOs that are not implemented will not have the corresponding bits implemented in this register.

13.8.2 APM I/O Decode

Table 13-10 shows the I/O registers associated with APM support. This register space is enabled in the PCI Device 31: Function 0 space (APMDEC_EN), and cannot be moved (fixed I/O location).

Table 13-10. APM Register Map

Address	Mnemonic	Register Name	Default	Type
B2h	APM_CNT	Advanced Power Management Control Port	00h	R/W
B3h	APM_STS	Advanced Power Management Status Port	00h	R/W

13.8.2.1 APM_CNT—Advanced Power Management Control Port Register

I/O Address: B2h
Default Value: 00h
Lockable: No
Power Well: Core

Attribute: R/W
Size: 8-bit
Usage: Legacy Only

Bit	Description
7:0	Used to pass an APM command between the OS and the SMI handler. Writes to this port not only store data in the APMC register, but also generates an SMI# when the APMC_EN bit is set.

13.8.2.2 APM_STS—Advanced Power Management Status Port Register

I/O Address: B3h
Default Value: 00h
Lockable: No
Power Well: Core

Attribute: R/W
Size: 8-bit
Usage: Legacy Only

Bit	Description
7:0	Used to pass data between the OS and the SMI handler. Basically, this is a scratchpad register and is not affected by any other register or function (other than a PCI reset).

13.8.3 Power Management I/O Registers

Table 13-11 shows the registers associated with ACPI and Legacy power management support. These registers are enabled in the PCI Device 31: Function 0 space (PM_IO_EN), and can be moved to any I/O location (128-byte aligned). The registers are defined to support the ACPI 3.0a specification, and use the same bit names.

Note: All reserved bits and registers will always return 0 when read, and will have no effect when written.

Table 13-11. ACPI and Legacy I/O Register Map

PMBASE + Offset	Mnemonic	Register Name	ACPI Pointer	Default	Type
00h–01h	PM1_STS	PM1 Status	PM1a_EVT_BLK	0000h	R/WC
02h–03h	PM1_EN	PM1 Enable	PM1a_EVT_BLK+2	0000h	R/W
04h–07h	PM1_CNT	PM1 Control	PM1a_CNT_BLK	00000000h	R/W, WO
08h–0Bh	PM1_TMR	PM1 Timer	PMTMR_BLK	xx000000h	RO
0Ch–0Fh	—	Reserved	—	—	—
10h–13h	PROC_CNT	Processor Control	P_BLK	00000000h	R/W, RO, WO
14h	LV2	Level 2	P_BLK+4	00h	RO
15h	LV3	Level 3	P_BLK+5	00h	RO
16h	LV4	Level 4	P_BLK+6	00h	RO
17h–18h	—	Reserved	—	—	—
19h–1Fh	—	Reserved	—	—	—
20-27h	GPE0_STS	General Purpose Event 0 Status	GPE0_BLK	00000000h	R/WC
28-2Fh	GPE0_EN	General Purpose Event 0 Enables	GPE0_BLK+8	00000000h	R/W
30h–33h	SMI_EN	SMI# Control and Enable		00000000h (Consumer); 00000002h (Corporate)	R/W, WO, R/WO
34h–37h	SMI_STS	SMI Status		00000000h	R/WC, RO
38h–39h	ALT_GP_SMI_EN	Alternate GPI SMI Enable		0000h	R/W
3Ah–3Bh	ALT_GP_SMI_STS	Alternate GPI SMI Status		0000h	R/WC
3Ch	UPRWC	USB Per-Port Registers Write Control		0000h	R/WC, RO, R/WO
3Dh–41h	—	Reserved	—	—	—
42h	GPE_CNTL	General Purpose Event Control		00h	RO, R/W
43h	—	Reserved	—	—	—
44h–45h	DEVACT_STS	Device Activity Status		0000h	R/WC
46h–4Fh	—	Reserved			
50h	PM2_CNT	PM2 Control	PM2a_CNT_BLK	00h	R/W
51h-53h	—	Reserved			
54h–57h	C3_RES	C3-Residency Register	—	00000000h	RO
58h-5Bh	—	Reserved			
5Ch–5Fh	—	Reserved	—	—	—
60h–7Fh	—	Reserved for TCO	—	—	—

13.8.3.1 PM1_STS—Power Management 1 Status Register

I/O Address:	PMBASE + 00h (*ACPI PM1a_EVT_BLK*)	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–15: Resume, except Bit 11 in RTC		

If bit 10 or 8 in this register is set, and the corresponding _EN bit is set in the PM1_EN register, then the ICH10 will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH10 will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set.

Note: Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
15	**Wake Status (WAK_STS)** — R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the system is in one of the sleep states (via the SLP_EN bit) and an enabled wake event occurs. Upon setting this bit, the ICH10 will transition the system to the ON state. If the AFTERG3_EN bit is not set and a power failure occurs without the SLP_EN bit set, the system will return to an S0 state when power returns, and the WAK_STS bit will not be set. If the AFTERG3_EN bit is set and a power failure occurs without the SLP_EN bit having been set, the system will go into an S5 state when power returns, and a subsequent wake event will cause the WAK_STS bit to be set. Note that any subsequent wake event would have to be caused by either a Power Button press, or an enabled wake event that was preserved through the power failure (enable bit in the RTC well).
14	**PCI Express Wake Status (PCIEXPWAK_STS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. If the WAKE# pin is still active during the write or the PME message received indication has not been cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level-sensitive). 1 = This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This wakeup event can be caused by the PCI Express WAKE# pin being active or receipt of a PCI Express PME message at a root port. This bit is set only when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the state of the PCIEXP_WAKE_DIS bit. Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	Reserved

Bit	Description
11	**Power Button Override Status (PWRBTNOR_STS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a Power Button Override occurs (i.e., the power button is pressed for at least 4 consecutive seconds), due to the corresponding bit in the SMBus slave message, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down or due to an internal thermal sensor catastrophic condition. The power button override causes an unconditional transition to the S5 state, as well as sets the AFTERG3_EN bit. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is preserved through power failures. Note that if this bit is still asserted when the global SCI_EN is set then an SCI will be generated.
10	**RTC Status (RTC_STS)** — R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally if the RTC_EN bit (PMBASE + 02h, bit 10) is set, the setting of the RTC_STS bit will generate a wake event.
9	**ME_STS** — R/WC. This bit is set when the Intel Management Engine generates a Non-Maskable wake event, and is not affected by any other enable bit. When this bit is set, the Host Power Management logic wakes to S0. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#.
8	**Power Button Status** (**PWRBTN__STS)** — R/WC. This bit is not affected by hard resets caused by a CF9 write. 0 = If the PWRBTN# signal is held low for more than 4 seconds, the hardware clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, and the system transitions to the S5 state with only PWRBTN# enabled as a wake event. This bit can be cleared by software by writing a one to the bit position. 1 = This bit is set by hardware when the PWRBTN# signal is asserted Low, independent of any other enable bit. In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI# if SCI_EN is not set) will be generated. In any sleeping state S1–S5, while PWRBTN_EN (PMBASE + 02h, bit 8) and PWRBTN_STS are both set, a wake event is generated. **NOTE:** If the PWRBTN_STS bit is cleared by software while the PWRBTN# signal is sell asserted, this will not cause the PWRBN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit.
7:6	Reserved
5	**Global Status (GBL _STS)** — R/WC. 0 = The SCI handler should then clear this bit by writing a 1 to the bit location. 1 = Set when an SCI is generated due to BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit.

Bit	Description
4	**Bus Master Status (BM_STS)** — R/WC. This bit will not cause a wake event, SCI or SMI#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by the ICH10 when a bus master requests access to main memory. Bus master activity is detected by any of the PCI Requests being active, any internal bus master request being active, or REQ-C2 message received while in C3 or C4 state. **NOTE:** 1. If the BM_STS_ZERO_EN bit is set, then this bit will generally report as a 0. LPC DMA and bus master activity will always set the BM_STS bit, even if the BM_STS_ZERO_EN bit is set.
3:1	Reserved
0	**Timer Overflow Status (TMROF_STS)** — R/WC. 0 = The SCI or SMI# handler clears this bit by writing a 1 to the bit location. 1 = This bit gets set any time bit 22 of the 24-bit timer goes high (bits are numbered from 0 to 23). This will occur every 2.3435 seconds. When the TMROF_EN bit (PMBASE + 02h, bit 0) is set, then the setting of the TMROF_STS bit will additionally generate an SCI or SMI# (depending on the SCI_EN).

13.8.3.2 PM1_EN—Power Management 1 Enable Register

I/O Address:	PMBASE + 02h (*ACPI PM1a_EVT_BLK + 2*)	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–9, 11–15: Resume, Bit 10: RTC		

Bit	Description
15	Reserved
14	**PCI Express* Wake Disable(PCIEXPWAK_DIS)** — R/W. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. 0 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register enabled to wake the system. 1 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register disabled from waking the system.
13:11	Reserved
10	**RTC Event Enable (RTC_EN)** — R/W. This bit is in the RTC well to allow an RTC event to wake after a power failure. This bit is not cleared by any reset other than RTCRST# or a Power Button Override event. 0 = No SCI (or SMI#) or wake event is generated then RTC_STS (PMBASE + 00h, bit 10) goes active. 1 = An SCI (or SMI#) or wake event will occur when this bit is set and the RTC_STS bit goes active.
9	Reserved.
8	**Power Button Enable (PWRBTN_EN)** — R/W. This bit is used to enable the setting of the PWRBTN_STS bit to generate a power management event (SMI#, SCI). PWRBTN_EN has no effect on the PWRBTN_STS bit (PMBASE + 00h, bit 8) being set by the assertion of the power button. The Power Button is always enabled as a Wake event. 0 = Disable. 1 = Enable.
7:6	Reserved.
5	**Global Enable (GBL_EN)** — R/W. When both the GBL_EN and the GBL_STS bit (PMBASE + 00h, bit 5) are set, an SCI is raised. 0 = Disable. 1 = Enable SCI on GBL_STS going active.
4:1	Reserved.
0	**Timer Overflow Interrupt Enable (TMROF_EN)** — R/W. Works in conjunction with the SCI_EN bit (PMBASE + 04h, bit 0) as described below: **TMROF_EN** / **SCI_EN** / **Effect when TMROF_STS is set** 0 / X / No SMI# or SCI 1 / 0 / SMI# 1 / 1 / SCI

13.8.3.3 PM1_CNT—Power Management 1 Control

I/O Address:	PMBASE + 04h (*ACPI PM1a_CNT_BLK*)	Attribute:	R/W, WO
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–12: RTC, Bits 13–15: Resume		

Bit	Description
31:14	Reserved.
13	**Sleep Enable (SLP_EN)** — WO. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	**Sleep Type (SLP_TYP)** — R/W. This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are only reset by RTCRST#. **Code** — **Master Interrupt** 000b — ON: Typically maps to S0 state. 001b — Asserts STPCLK#. Puts processor in Stop-Grant state. Optional to assert CPUSLP# to put processor in sleep state: Typically maps to S1 state. 010b — Reserved 011b — Reserved 100b — Reserved 101b — Suspend-To-RAM. Assert SLP_S3#: Typically maps to S3 state. 110b — Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state. 111b — Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.
9:3	Reserved.
2	**Global Release (GBL_RLS)** — WO. 0 = This bit always reads as 0. 1 = ACPI software writes a 1 to this bit to raise an event to the BIOS. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events.
1	**Bus Master Reload (BM_RLD)** — R/W. This bit is treated as a scratchpad bit. This bit is reset to 0 by PLTRST# 0 = Bus master requests will not cause a break from the C3 state. 1 = Enables Bus Master requests (internal or external) to cause a break from the C3 state. If software fails to set this bit before going to C3 state, ICH10 will still return to a snoopable state from C3 or C4 states due to bus master activity.
0	**SCI Enable (SCI_EN)** — R/W. Selects the SCI interrupt or the SMI# interrupt for various events including the bits in the PM1_STS register (bit 10, 8, 0), and bits in GPE0_STS. 0 = These events will generate an SMI#. 1 = These events will generate an SCI.

13.8.3.4 PM1_TMR—Power Management 1 Timer Register

I/O Address: PMBASE + 08h (*ACPI PMTMR_BLK*)
Attribute: RO
Default Value: xx000000h
Size: 32-bit
Lockable: No
Usage: ACPI
Power Well: Core

Bit	Description
31:24	Reserved
23:0	**Timer Value (TMR_VAL)** — RO. Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (14.31818 MHz divided by 4). It is reset to 0 during a PCI reset, and then continues counting as long as the system is in the S0 state. After an S1 state, the counter will not be reset (it will continue counting from the last value in S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit (PMBASE + 00h, bit 0) is set. The High-to-Low transition will occur every 2.3435 seconds. If the TMROF_EN bit (PMBASE + 02h, bit 0) is set, an SCI interrupt is also generated.

13.8.3.5 PROC_CNT—Processor Control Register

I/O Address: PMBASE + 10h (*ACPI P_BLK*)
Attribute: R/W, RO, WO
Default Value: 00000000h
Size: 32-bit
Lockable: No (bits 7:5 are write once)
Usage: ACPI or Legacy
Power Well: Core

Bit	Description
31:18	Reserved
17	**Throttle Status (THTL_STS)** — RO. 0 = No clock throttling is occurring (maximum processor performance). 1 = Indicates that the clock state machine is throttling the processor performance. This could be due to the THT_EN bit or the FORCE_THTL bit being set.
16:9	Reserved
8	**Force Thermal Throttling (FORCE_THTL)** — R/W. Software can set this bit to force the thermal throttling function. 0 = No forced throttling. 1 = Throttling at the duty cycle specified in THRM_DTY starts immediately, and no SMI# is generated.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:5</td><td>THRM_DTY — WO. This write-once field determines the duty cycle of the throttling when the FORCE_THTL bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs. Note that the throttling only occurs if the system is in the C0 state. If in the C2, C3, or C4 state, no throttling occurs.
Once the THRM_DTY field is written, any subsequent writes will have no effect until PLTRST# goes active.

<table>
<tr><th>THRM_DTY</th><th>Throttle Mode</th><th>PCI Clocks</th></tr>
<tr><td>000b</td><td>50% (Default)</td><td>512</td></tr>
<tr><td>001b</td><td>87.5%</td><td>896</td></tr>
<tr><td>010b</td><td>75.0%</td><td>768</td></tr>
<tr><td>011b</td><td>62.5%</td><td>640</td></tr>
<tr><td>100b</td><td>50%</td><td>512</td></tr>
<tr><td>101b</td><td>37.5%</td><td>384</td></tr>
<tr><td>110b</td><td>25%</td><td>256</td></tr>
<tr><td>111b</td><td>12.5%</td><td>128</td></tr>
</table></td></tr>
<tr><td>4</td><td>THTL_EN — R/W. When set and the system is in a C0 state, it enables a processor-controlled STPCLK# throttling. The duty cycle is selected in the THTL_DTY field.
0 = Disable
1 = Enable</td></tr>
<tr><td>3:1</td><td>THTL_DTY — R/W. This field determines the duty cycle of the throttling when the THTL_EN bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted (low) while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs.

<table>
<tr><th>THTL_DTY</th><th>Throttle Mode</th><th>PCI Clocks</th></tr>
<tr><td>000b</td><td>50% (Default)</td><td>512</td></tr>
<tr><td>001b</td><td>87.5%</td><td>896</td></tr>
<tr><td>010b</td><td>75.0%</td><td>768</td></tr>
<tr><td>011b</td><td>62.5%</td><td>640</td></tr>
<tr><td>100b</td><td>50%</td><td>512</td></tr>
<tr><td>101b</td><td>37.5%</td><td>384</td></tr>
<tr><td>110b</td><td>25%</td><td>256</td></tr>
<tr><td>111b</td><td>12.5%</td><td>128</td></tr>
</table></td></tr>
<tr><td>0</td><td>Reserved</td></tr>
</table>

13.8.3.6 LV2 — Level 2 Register

I/O Address:	PMBASE + 14h (*ACPI P_BLK+4*)	Attribute:	RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
7:0	Reads to this register return all 0s, writes to this register have no effect. Reads to this register generate a “enter a level 2 power state” (C2) to the clock control logic. This will cause the STPCLK# signal to go active, and stay active until a break event occurs. Throttling (due either to THTL_EN or FORCE_THTL) will be ignored.

NOTE: This register should not be used by IA-64 processors or systems with more than 1 logical processor, unless appropriate semaphoring software has been put in place to ensure that all threads/processors are ready for the C2 state when the read to this register occurs

13.8.3.7 LV3—Level 3 Register

I/O Address:	PMBASE + 15h (ACPI P_BLK + 5)		
		Attribute:	RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
		Power Well:	Core

Bit	Description
7:0	Reads to this register return all 0s, writes to this register have no effect. Reads to this register generate a “enter a C3 power state” to the clock control logic. The C3 state persists until a break event occurs.

NOTE: If the C4onC3_EN bit is set, reads this register will initiate a LVL4 transition rather than a LVL3 transition. In the event that software attempts to simultaneously read the LVL2 and LVL3 registers (which is invalid), the ICH10 will ignore the LVL3 read, and only perform a C2 transition.

NOTE: This register should not be used by IA-64 processors or systems with more than 1 logical processor, unless appropriate semaphoring software has been put in place to ensure that all threads/processors are ready for the C3 state when the read to this register occurs.

13.8.3.8 LV4—Level 4 Register

I/O Address:	PMBASE + 16h (ACPI P_BLK + 6)		
		Attribute:	RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
		Power Well:	Core

Bit	Description
7:0	Reads to this register return all 0s, writes to this register have no effect. Reads to this register generate a “enter a C4 power state” to the clock control logic. The C4 state persists until a break event occurs.

NOTE: This register should not be used by IA-64 processors or systems with more than 1 logical processor, unless appropriate semaphoring software has been put in place to ensure that all threads/processors are ready for the C4 state when the read to this register occurs.

13.8.3.9 GPE0_STS—General Purpose Event 0 Status Register

I/O Address:	PMBASE + 20h (ACPI GPE0_BLK)	Attribute:	Bits 0:32 R/WC Bits 33:63 RO
Default Value:	0000000000000000h	Size:	64-bit
Lockable:	No	Usage:	ACPI
Power Well:	Resume		

This register is symmetrical to the General Purpose Event 0 Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the _STS bit get set, the ICH10 will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH10 will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit (PMBASE + 04h, bit 0) is not set. Bits 31:16 are reset by a CF9h write; bits 63:32 and 15:0 are not. All are reset by RSMRST#.

Bit	Description
63:33	Reserved.
32	**USB6_STS** — R/WC. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume well reset. This bit is set when USB UHCI controller #6 needs to cause a wake. Additionally if the USB6_EN bit is set, the setting of the USB6_STS bit will generate a wake event.
31:16	**GPIOn_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPIO[n]_STS bit is set: • If the system is in an S1–S5 state, the event will also wake the system. • If the system is in an S0 state (or upon waking back to an S0 state), a SCI will be caused depending on the GPIO_ROUT bits (D31:F0:B8h, bits 31:30) for the corresponding GPI. **NOTE:** Mapping is as follows: bit 31 corresponds to GPIO[15]... and bit 16 corresponds to GPIO[0].
15	Reserved
14	**USB4_STS** — R/WC. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume well reset. This bit is set when USB UHCI controller #4 needs to cause a wake. Additionally if the USB4_EN bit is set, the setting of the USB4_STS bit will generate a wake event.

Bit	Description
13	**PME_B0_STS** — R/WC. This bit will be set to 1 by the ICH10 when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit is set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_STS bit is set, and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event, and an SCI (or SMI# if SCI_EN is not set) will be generated. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. The default for this bit is 0. Writing a 1 to this bit position clears this bit. **Note**: HD audio wake events are reported in this bit. Intel Management Engine “maskable” wake events are also reported in this bit.
12	**USB3_STS** — R/WC. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume well reset. This bit is set when USB UHCI controller #3 needs to cause a wake. Additionally if the USB3_EN bit is set, the setting of the USB3_STS bit will generate a wake event.
11	**PME_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN bit is set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI or SMI# (if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1–S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event, and an SCI will be generated. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10	Reserved
9	**PCI_EXP_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware to indicate that: • The PME event message was received on one or more of the PCI Express* ports • An Assert PMEGPE message received from the (G)MCH via DMI **NOTES:** 1. The PCI WAKE# pin has no impact on this bit. 2. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. 3. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level-triggered SCI will remain active. 4. A race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the *PCI Express* Specification, Revision 1.0a*. The window for this race condition is approximately 95–105 milliseconds.
8	**RI_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RI# input signal goes active.

Bit	Description
7	**SMBus Wake Status (SMB_WAK_STS)** — R/WC. The SMBus controller can independently cause an SMI# or SCI, so this bit does not need to do so (unlike the other bits in this register). Software clears this bit by writing a 1 to it. 0 = Wake event Not caused by the ICH10's SMBus logic. 1 = Set by hardware to indicate that the wake event was caused by the ICH10's SMBus logic.This bit will be set by the WAKE/SMI# command type, even if the system is already awake. The SMI handler should then clear this bit. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. (Consumer Only) If SMB_WAK_STS is set due to SMBus slave receiving a message, it will be cleared by internal logic when a THRMTRIP# event happens or a Power Button Override event. However, THRMTRIP# or Power Button Override event will not clear SMB_WAK_STS if it is set due to SMBALERT# signal going active. 4. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:Bit 5) should be cleared by software before the SMB_WAK_STS bit is cleared.
6	**TCOSCI_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = TOC logic or thermal sensor logic did Not cause SCI. 1 = Set by hardware when the TCO logic or thermal sensor logic causes an SCI.
5	**USB5_STS**— R/WC. Software clears this bit by writing a 1 to it. 0 = USB UHCI controller 5 does NOT need to cause a wake. 1 = Set by hardware when USB UHCI controller 5 needs to cause a wake. Wake event will be generated if the corresponding USB2_EN bit is set.
4	**USB2_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = USB UHCI controller 2 does Not need to cause a wake. 1 = Set by hardware when USB UHCI controller 2 needs to cause a wake. Wake event will be generated if the corresponding USB2_EN bit is set.
3	**USB1_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = USB UHCI controller 1 does Not need to cause a wake. 1 = Set by hardware when USB UHCI controller 1 needs to cause a wake. Wake event will be generated if the corresponding USB1_EN bit is set.
2	**SWGPE_STS** — R/WC. The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	**HOT_PLUG_STS** — R/WC. 0 = This bit is cleared by writing a 1 to this bit position. 1 = When a PCI Express* Hot-Plug event occurs. This will cause an SCI if the HOT_PLUG_EN bit is set in the GEP0_EN register.
0	**Thermal Interrupt Status (THRM_STS)** — R/WC. Software clears this bit by writing a 1 to it. 0 = THRM# signal Not driven active as defined by the THRM_POL bit 1 = Set by hardware anytime the THRM# signal is driven active as defined by the THRM_POL bit. Additionally, if the THRM_EN bit is set, then the setting of the THRM_STS bit will also generate a power management event (SCI or SMI#).

13.8.3.10 GPE0_EN—General Purpose Event 0 Enables Register

I/O Address:	PMBASE + 28h (*ACPI GPE0_BLK + 8*)	Attribute:	Bits 0:32 R/W Bits 33:63 RO
Default Value:	0000000000000000h	Size:	64-bit
Lockable:	No	Usage:	ACPI
Power Well:	Bits 0–7, 9, 12, 14–63 Resume, Bits 8, 10–11, 13 RTC		

This register is symmetrical to the General Purpose Event 0 Status Register. All the bits in this register should be cleared to 0 based on a Power Button Override or processor Thermal Trip event. The resume well bits are all cleared by RSMRST#. The RTC well bits are cleared by RTCRST#.

Bit	Description
63:33	Reserved.
32	**USB6_EN** — R/W. 0 = Disable. 1 = Enable the setting of the USB4_STS bit to generate a wake event. The USB6_STS bit is set anytime USB UHCI controller #6 signals a wake event. Break events are handled via the USB interrupt.
31:16	**GPIn_EN** — R/W. These bits enable the corresponding GPI[n]_STS bits being set to cause a SCI, and/or wake event. These bits are cleared by RSMRST#. **NOTE:** Mapping is as follows: bit 31 corresponds to GPIO15... and bit 16 corresponds to GPIO0.
15	Reserved
14	**USB4_EN** — R/W. 0 = Disable. 1 = Enable the setting of the USB4_STS bit to generate a wake event. The USB4_STS bit is set anytime USB UHCI controller #4 signals a wake event. Break events are handled via the USB interrupt.
13	**PME_B0_EN** — R/W. 0 = Disable 1 = Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. PME_B0_STS can be a wake event from the S1–S4 states, or from S5 (if entered via SLP_TYP and SLP_EN) or power failure, but not Power Button Override. This bit defaults to 0. **NOTE:** It is only cleared by Software or RTCRST#. It is not cleared by CF9h writes.
12	**USB3_EN** — R/W. 0 = Disable. 1 = Enable the setting of the USB3_STS bit to generate a wake event. The USB3_STS bit is set anytime USB UHCI controller #3 signals a wake event. Break events are handled via the USB interrupt.
11	**PME_EN** — R/W. 0 = Disable. 1 = Enables the setting of the PME_STS to generate a wake event and/or an SCI. PME# can be a wake event from the S1 – S4 state or from S5 (if entered via SLP_EN, but not power button override).
10	Reserved

Bit	Description
9	**PCI_EXP_EN** — R/W. 0 = Disable SCI generation upon PCI_EXP_STS bit being set. 1 = Enables ICH10 to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express* ports, including the link to the (G)MCH, to cause an SCI due to wake/PME events.
8	**RI_EN** — R/W. The value of this bit will be maintained through a G3 state and is not affected by a hard reset caused by a CF9h write. 0 = Disable. 1 = Enables the setting of the RI_STS to generate a wake event.
7	Reserved
6	**TCOSCI_EN** — R/W. 0 = Disable. 1 = Enables the setting of the TCOSCI_STS to generate an SCI.
5	**USB5_EN** — R/W. 0 = Disable. 1 = Enables the setting of the USB5_STS to generate a wake event.
4	**USB2_EN** — R/W. 0 = Disable. 1 = Enables the setting of the USB2_STS to generate a wake event.
3	**USB1_EN** — R/W. 0 = Disable. 1 = Enables the setting of the USB1_STS to generate a wake event.
2	**SWGPE_EN**— R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1s, an SCI will be generated. If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated.
1	**HOT_PLUG_EN** — R/W. 0 = Disables SCI generation upon the HOT_PLUG_STS bit being set. 1 = Enables the ICH10 to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.
0	**THRM_EN** — R/W. 0 = Disable. 1 = Active assertion of the THRM# signal (as defined by the THRM_POL bit) will generate a power management event (SCI or SMI) if the THRM_STS bit is also set.

13.8.3.11 SMI_EN—SMI Control and Enable Register

I/O Address:	PMBASE + 30h	Attribute:	R/W, R/WO, WO
Default Value:	00000000h (Consumer)	Size:	32 bit
Default Value:	00000002h (Corporate)		
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: This register is symmetrical to the SMI status register.

Bit	Description
31:28	Reserved
27	**GPIO_UNLOCK_SMI_EN**— R/WO. Setting this bit will cause the Intel ICH10 to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST#.
26:19	Reserved
18	**INTEL_USB2_EN** — R/W. 0 = Disable 1 = Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	**LEGACY_USB2_EN** — R/W. 0 = Disable 1 = Enables legacy USB2 logic to cause SMI#.
16:15	Reserved
14	**PERIODIC_EN** — R/W. 0 = Disable. 1 = Enables the ICH10 to generate an SMI# when the PERIODIC_STS bit (PMBASE + 34h, bit 14) is set in the SMI_STS register (PMBASE + 34h).
13	**TCO_EN** — R/W. 0 = Disables TCO logic generating an SMI#. Note that if the NMI2SMI_EN bit is set, SMIs that are caused by re-routed NMIs will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, NMIs will still be routed to cause SMIs. 1 = Enables the TCO logic to generate SMI#. **NOTE:** This bit cannot be written once the TCO_LOCK bit is set.
12	Reserved
11	**MCSMI_ENMicrocontroller SMI Enable (MCSMI_EN)** — R/W. 0 = Disable. 1 = Enables ICH10 to trap accesses to the microcontroller range (62h or 66h) and generate an SMI#. Note that "trapped' cycles will be claimed by the ICH10 on PCI, but not forwarded to LPC.
10:8	Reserved
7	**BIOS Release (BIOS_RLS)** — WO. 0 = This bit will always return 0 on reads. Writes of 0 to this bit have no effect. 1 = Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. **NOTE:** GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.

Bit	Description
6	**Software SMI# Timer Enable (SWSMI_TMR_EN)** — R/W. 0 = Disable. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. 1 = Starts Software SMI# Timer. When the SWSMI timer expires (the timeout period depends upon the SWSMI_RATE_SEL bit setting), SWSMI_TMR_STS is set and an SMI# is generated. SWSMI_TMR_EN stays set until cleared by software.
5	**APMC_EN** — R/W. 0 = Disable. Writes to the APM_CNT register will not cause an SMI#. 1 = Enables writes to the APM_CNT register to cause an SMI#.
4	**SLP_SMI_EN** — R/W. 0 = Disables the generation of SMI# on SLP_EN. Note that this bit must be 0 before the software attempts to transition the system into a sleep state by writing a 1 to the SLP_EN bit. 1 = A write of 1 to the SLP_EN bit (bit 13 in PM1_CNT register) will generate an SMI#, and the system will not transition to the sleep state based on that write to the SLP_EN bit.
3	**LEGACY_USB_EN** — R/W. 0 = Disable. 1 = Enables legacy USB circuit to cause SMI#.
2	**BIOS_EN** — R/W. 0 = Disable. 1 = Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit (D31:F0:PMBase + 04h:bit 2). Note that if the BIOS_STS bit (D31:F0:PMBase + 34h:bit 2), which gets set when software writes 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	**End of SMI (EOS)** — R/W (special). This bit controls the arbitration of the SMI signal to the processor. This bit must be set for the ICH10 to assert SMI# low to the processor after SMI# has been asserted previously. 0 = Once the ICH10 asserts SMI# low, the EOS bit is automatically cleared. 1 = When this bit is set to 1, SMI# signal will be deasserted for 4 PCI clocks before its assertion. In the SMI handler, the processor should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to re-assert SMI upon detection of an SMI event and the setting of a SMI status bit. **NOTE:** ICH10 is able to generate 1st SMI after reset even though EOS bit is not set. Subsequent SMI require EOS bit is set.
0	**GBL_SMI_EN** — R/W. 0 = No SMI# will be generated by ICH10. This bit is reset by a PCI reset event. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. **NOTE:** When the SMI_LOCK bit is set, this bit cannot be changed.

13.8.3.12 SMI_STS—SMI Status Register

I/O Address:	PMBASE + 34h	Attribute:	RO, R/WC
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: If the corresponding _EN bit is set when the _STS bit is set, the ICH10 will cause an SMI# (except bits 8–10 and 12, which do not need enable bits since they are logic ORs of other registers that have enable bits). The ICH10 uses the same GPE0_EN register (I/O address: PMBase+2Ch) to enable/disable both SMI and ACPI SCI general purpose input events. ACPI OS assumes that it owns the entire GPE0_EN register per ACPI spec. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states. BIOS should define a dummy control method which prevents the ACPI OS from clearing the SMI GPE0_EN bits.

Bit	Description
31:28	Reserved
27	**GPIO_UNLOCK_SMI_STS** — R/WC. This bit will be set if the GPIO registers lockdown logic is requesting an SMI#. Writing a 1 to this bit position clears this bit to 0.
26	**SPI_STS** — RO. This bit will be set if the SPI logic is generating an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25:22	Reserved
21	**MONITOR_STS** — RO. This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the processor or a bus master accesses an assigned register (or a sequence of accesses). See Section 10.1.43 through Section 10.1.49 for details on the specific cause of the SMI.
20	**PCI_EXP_SMI_STS** — RO. PCI Express* SMI event occurred. This could be due to a PCI Express PME event or Hot-Plug event.
19	Reserved
18	**INTEL_USB2_STS** — RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. Additionally, the Port Disable Write Enable SMI is reported in this bit; the specific status bit for this event is contained in the USB Per-Port Registers Write Control Register in this I/O space. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
17	**LEGACY_USB2_STS** — RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB2 Legacy Support Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.

Bit	Description
16	**SMBus SMI Status (SMBUS_SMI_STS)** — R/WC. Software clears this bit by writing a 1 to it. 0 = This bit is set from the 64 kHz clock domain used by the SMBus. Software must wait at least 15.63 µs after the initial assertion of this bit before clearing it. 1 = Indicates that the SMI# was caused by: 1. The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a Host Notify message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The ICH10 detecting the SMLINK_SLAVE_SMI command while in the S0 state.
15	**SERIRQ_SMI_STS** — RO. 0 = SMI# was not caused by the SERIRQ decoder. 1 = Indicates that the SMI# was caused by the SERIRQ decoder. **NOTE:** This is not a sticky bit
14	**PERIODIC_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit (PMBASE + 30h, bit 14) is also set, the ICH10 generates an SMI#.
13	**TCO_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = SMI# not caused by TCO logic. 1 = Indicates the SMI# was caused by the TCO logic. Note that this is not a wake event.
12	**Device Monitor Status (DEVMON_STS)** — RO. 0 = SMI# not caused by Device Monitor. 1 = Set if bit 0 of the DEVACT_STS register (PMBASE + 44h) is set. The bit is not sticky, so writes to this bit will have no effect.
11	**Microcontroller SMI# Status** (**MCSMI_STS)** — R/WC. Software clears this bit by writing a 1 to it. 0 = Indicates that there has been no access to the power management microcontroller range (62h or 66h). 1 = Set if there has been an access to the power management microcontroller range (62h or 66h) and the Microcontroller Decode Enable #1 bit in the LPC Bridge I/O Enables configuration register is 1 (D31:F0:Offset 82h:bit 11). Note that this implementation assumes that the Microcontroller is on LPC. If this bit is set, and the MCSMI_EN bit is also set, the ICH10 will generate an SMI#.
10	**GPE0_STS** — RO. This bit is a logical OR of the bits in the ALT_GP_SMI_STS register that are also set up to cause an SMI# (as indicated by the GPI_ROUT registers) and have the corresponding bit set in the ALT_GP_SMI_EN register. Bits that are not routed to cause an SMI# will have no effect on this bit. 0 = SMI# was not generated by a GPI assertion. 1 = SMI# was generated by a GPI assertion.
9	**GPE0_STS** — RO. This bit is a logical OR of the bits 47:32, 14:10, 8, 6:2 and 0 in the GPE0_STS register (PMBASE + 28h) that also have the corresponding bit set in the GPE0_EN register (PMBASE + 2Ch). 0 = SMI# was not generated by a GPE0 event. 1 = SMI# was generated by a GPE0 event.

Bit	Description
8	**PM1_STS_REG** — RO. This is an ORs of the bits in the ACPI PM1 Status Register (offset PMBASE+00h) that can cause an SMI#. 0 = SMI# was not generated by a PM1_STS event. 1 = SMI# was generated by a PM1_STS event.
7	Reserved
6	**SWSMI_TMR_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = Software SMI# Timer has Not expired. 1 = Set by the hardware when the Software SMI# Timer expires.
5	**APM_STS** — R/WC. Software clears this bit by writing a 1 to it. 0 = No SMI# generated by write access to APM Control register with APMCH_EN bit set. 1 = SMI# was generated by a write access to the APM Control register with the APMC_EN bit set.
4	**SLP_SMI_STS** — R/WC. Software clears this bit by writing a 1 to the bit location. 0 = No SMI# caused by write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set. 1 = Indicates an SMI# was caused by a write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set.
3	**LEGACY_USB_STS** — RO. This bit is a logical OR of each of the SMI status bits in the USB Legacy Keyboard/Mouse Control Registers ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. 0 = SMI# was not generated by USB Legacy event. 1 = SMI# was generated by USB Legacy event.
2	**BIOS_STS** — R/WC. 0 = No SMI# generated due to ACPI software requesting attention. 1 = This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit (D31:F0:PMBase + 04h:bit 2). When both the BIOS_EN bit (D31:F0:PMBase + 30h:bit 2) and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to its bit position.
1:0	Reserved

13.8.3.13 ALT_GP_SMI_EN—Alternate GPI SMI Enable Register

I/O Address:	PMBASE +38h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI SMI Enable** — R/W. These bits are used to enable the corresponding GPIO to cause an SMI#. For these bits to have any effect, the following must be true. • The corresponding bit in the ALT_GP_SMI_EN register is set. • The corresponding GPI must be routed in the GPI_ROUT register to cause an SMI. • The corresponding GPIO must be implemented. **NOTE:** Mapping is as follows: bit 15 corresponds to GPIO15... bit 0 corresponds to GPIO0.

13.8.3.14 ALT_GP_SMI_STS—Alternate GPI SMI Status Register

I/O Address:	PMBASE +3Ah	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI SMI Status** — R/WC. These bits report the status of the corresponding GPIOs. 0 = Inactive. Software clears this bit by writing a 1 to it. 1 = Active These bits are sticky. If the following conditions are true, then an SMI# will be generated and the GPE0_STS bit set: • The corresponding bit in the ALT_GPI_SMI_EN register (PMBASE + 38h) is set • The corresponding GPIO must be routed in the GPI_ROUT register to cause an SMI. • The corresponding GPIO must be implemented. All bits are in the resume well. Default for these bits is dependent on the state of the GPIO pins.

13.8.3.15 UPRWC—USB Per-Port Registers Write Control

I/O Address:	PMBASE +3Ch	Attribute:	R/WC, R/W, R/WO
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:9	Reserved
8	**Write Enable Status** — R/WC 0 = This bit gets set by hardware when the “Per-Port Registers Write Enable” bit is written from 0-to-1. 1 = This bit is cleared by software writing a 1b to this bit location The setting condition takes precedence over the clearing condition in the event that both occur at once. When this bit is 1b and bit 0 is 1b, the INTEL_USB2_STS bit is set in the SMI_STS register.
7:2	Reserved.
1	Reserved
0	**Write Enable SMI Enable**— R/WO 0 = Disable 1 = enables the generation of SMI when the Per-Port Registers Write Enable (bit 1) is written from 0 to 1. Once written to 1b, this bit can not be cleared by software.

13.8.3.16 GPE_CNTL— General Purpose Control Register

I/O Address:	PMBASE +42h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
8:2	Reserved
1	**SWGPE_CTRL**— R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0.
0	**THRM#_POL** — R/W. This bit controls the polarity of the THRM# pin needed to set the THRM_STS bit. 0 = Low value on the THRM# signal will set the THRM_STS bit. 1 = HIGH value on the THRM# signal will set the THRM_STS bit.

13.8.3.17 DEVACT_STS — Device Activity Status Register

I/O Address:	PMBASE +44h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Each bit indicates if an access has occurred to the corresponding device's trap range, or for bits 6:9 if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT_STS register (PMBASE + 44h).

Note: Software clears bits that are set in this register by writing a 1 to the bit position.

Bit	Description
15:13	Reserved
12	**KBC_ACT_STS** — R/WC. KBC (60/64h). 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
11:10	Reserved
9	**PIRQDH_ACT_STS** — R/WC. PIRQ[D or H]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
8	**PIRQCG_ACT_STS** — R/WC. PIRQ[C or G]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.

Bit	Description
7	**PIRQBF_ACT_STS** — R/WC. PIRQ[B or F]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
6	**PIRQAE_ACT_STS** — R/WC. PIRQ[A or E]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
5:0	Reserved

13.8.3.18 PM2_CNT—Power Management 2 Control

I/O Address:	PMBASE + 50h (ACPI PM2_CNT_BLK)	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
7:1	Reserved
0	**Arbiter Disable (ARB_DIS)** — R/W This bit is essentially just a scratchpad bit for legacy software compatibility. Software typically sets this bit to 1 prior to entering a C3 or C4 state. When a transition to a C3 or C4 state occurs, ICH10 will automatically prevent any internal or external non-Isoch bus masters from initiating any cycles up to the (G)MCH. This blocking starts immediately upon the ICH10 sending the Go-C3 message to the (G)MCH. The blocking stops when the Ack-C2 message is received. Note that this is not really blocking, in that messages (such as from PCI Express*) are just queued and held pending.

13.8.3.19 C3_RES— C3 Residency Register

I/O Address:	PMBASE +54h	Attribute:	RO
Default Value	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI/Legacy
Power Well:	Core		

Software may only write this register during system initialization to set the state of the C3_RESIDENCY_MODE bit. It must not be written while the timer is in use.

Bit	Description
31:24	Reserved
23:0	**C3_RESIDENCY** — RO. The value in this field increments at the same rate as the Power Management Timer. This field increments while STP_CPU# is active (i.e., the processor is in a C3 or C4 state). This field will roll over in the same way as the PM Timer, however the most significant bit is NOT sticky. Software is responsible for reading this field before performing the Lvl3/4 transition. Software must also check for rollover if the maximum time in C3/C4 could be exceeded. **NOTE:** Hardware reset is the only reset of this counter field.

13.9 System Management TCO Registers (D31:F0)

The TCO logic is accessed via registers mapped to the PCI configuration space (Device 31:Function 0) and the system I/O space. For TCO PCI Configuration registers, see LPC Device 31:Function 0 PCI Configuration registers.

TCO Register I/O Map

The TCO I/O registers reside in a 32-byte range pointed to by a TCOBASE value, which is, PMBASE + 60h in the PCI config space. The following table shows the mapping of the registers within that 32-byte range. Each register is described in the following sections.

Table 13-12. TCO I/O Register Address Map

TCOBASE + Offset	Mnemonic	Register Name	Default	Type
00h–01h	TCO_RLD	TCO Timer Reload and Current Value	0000h	R/W
02h	TCO_DAT_IN	TCO Data In	00h	R/W
03h	TCO_DAT_OUT	TCO Data Out	00h	R/W
04h–05h	TCO1_STS	TCO1 Status	0000h	R/WC, RO
06h–07h	TCO2_STS	TCO2 Status	0000h	R/WC
08h–09h	TCO1_CNT	TCO1 Control	0000h	R/W, R/WLO, R/WC
0Ah–0Bh	TCO2_CNT	TCO2 Control	0008h	R/W
0Ch–0Dh	TCO_MESSAGE1, TCO_MESSAGE2	TCO Message 1 and 2	00h	R/W
0Eh	TCO_WDCNT	Watchdog Control	00h	R/W
0Fh	—	Reserved	—	—
10h	SW_IRQ_GEN	Software IRQ Generation	03h	R/W
11h	—	Reserved	—	—
12h–13h	TCO_TMR	TCO Timer Initial Value	0004h	R/W
14h–1Fh	—	Reserved	—	—

13.9.1 TCO_RLD—TCO Timer Reload and Current Value Register

I/O Address:	TCOBASE +00h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Value** — R/W. Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

13.9.2 TCO_DAT_IN—TCO Data In Register

I/O Address:	TCOBASE +02h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**TCO Data In Value** — R/W. This data register field is used for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register (D31:F0:04h).

13.9.3 TCO_DAT_OUT—TCO Data Out Register

I/O Address:	TCOBASE +03h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**TCO Data Out Value** — R/W. This data register field is used for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It will also cause an interrupt, as selected by the TCO_INT_SEL bits.

13.9.4 TCO1_STS—TCO1 Status Register

I/O Address:	TCOBASE +04h	Attribute:	R/WC, RO
Default Value:	0000h (Consumer Only) 2000h (Corporate Only)	Size:	16-bit
Lockable:	No	Power Well:	Core (Except bit 7, in RTC)

Bit	Description
15:14	Reserved
13 (Corporate Only)	**TCO_SLVSEL (TCO Slave Select) -** RO. This register bit is Read Only by Host and indicates the value of TCO Slave Select Soft Strap. Refer to the ICH Soft Straps section of the SPI Chapter for details.
13 (Consumer Only)	Reserved
12	**DMISERR_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = ICH10 received a DMI special cycle message via DMI indicating that it wants to cause an SERR#. The software must read the (G)MCH to determine the reason for the SERR#.
11	Reserved
10	**DMISMI_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = ICH10 received a DMI special cycle message via DMI indicating that it wants to cause an SMI. The software must read the (G)MCH to determine the reason for the SMI.

Bit	Description
9	**DMISCI_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = ICH10 received a DMI special cycle message via DMI indicating that it wants to cause an SCI. The software must read the (G)MCH to determine the reason for the SCI.
8	**BIOSWR_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = ICH10 sets this bit and generates and SMI# to indicate an invalid attempt to write to the BIOS. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the BLD bit is also set, or b) any write is attempted to the BIOS and the BIOSWP bit is also set. **NOTE:** On write cycles attempted to the 4 MB lower alias to the BIOS space, the BIOSWR_STS will not be set.
7	**NEWCENTURY_STS** — R/WC. This bit is in the RTC well. 0 = Cleared by writing a 1 to the bit position or by RTCRST# going active. 1 = This bit is set when the Year byte (RTC I/O space, index offset 09h) rolls over from 99 to 00. Setting this bit will cause an SMI# (but not a wake event). **NOTE:** The NEWCENTURY_STS bit is not valid when the RTC battery is first installed (or when RTC power has not been maintained). Software can determine if RTC power has not been maintained by checking the RTC_PWR_STS bit (D31:F0:A4h, bit 2), or by other means (such as a checksum on RTC RAM). If RTC power is determined to have not been maintained, BIOS should set the time to a valid value and then clear the NEWCENTURY_STS bit. The NEWCENTURY_STS bit may take up to 3 RTC clocks for the bit to be cleared after a 1 is written to the bit to clear it. After writing a 1 to this bit, software should not exit the SMI handler until verifying that the bit has actually been cleared. This will ensure that the SMI is not re-entered.
6:4	Reserved
3	**TIMEOUT** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by ICH10 to indicate that the SMI was caused by the TCO timer reaching 0.
2	**TCO_INT_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = SMI handler caused the interrupt by writing to the TCO_DAT_OUT register (TCOBASE + 03h).
1	**SW_TCO_SMI** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Software caused an SMI# by writing to the TCO_DAT_IN register (TCOBASE + 02h).
0	**NMI2SMI_STS** — RO. 0 = Cleared by clearing the associated NMI status bit. 1 = Set by the ICH10 when an SMI# occurs because an event occurred that would otherwise have caused an NMI (because NMI2SMI_EN is set).

13.9.5 TCO2_STS—TCO2 Status Register

I/O Address:	TCOBASE +06h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Resume (Except Bit 0, in RTC)

Bit	Description
15:8	Reserved
7:5 (Corporate Only)	Reserved
7 (Consumer Only)	**ME Host Reset Warm Status (ME_HRST_WARM_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Host reset without power cycling. Software clears this bit by writing a 1 to this bit position.
6 (Consumer Only)	**ME Host Reset Cold Status (ME_HRST_COLD_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Host reset with power cycling. Software clears this bit by writing a 1 to this bit position.
5 (Consumer Only)	**ME WAKE STATUS (ME_WAKE_STS)** — R/WC. This bit is set when the Intel Management Engine generates a Non-Maskable wake event, and is not affected by any other enable bit. When this bit is set, the Host Power Management logic wakes to S0. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9h write, but is reset by RSMRST.
4	**SMLink Slave SMI Status (SMLINK_SLV_SMI_STS)** — R/WC. Allow the software to go directly into pre-determined sleep state. This avoids race conditions. Software clears this bit by writing a 1 to it. 0 = The bit is reset by RSMRST#, but not due to the PCI Reset associated with exit from S3–S5 states. 1 = ICH10 sets this bit to 1 when it receives the SMI message on the SMLink's Slave Interface.
3	Reserved.
2	**BOOT_STS** — R/WC. 0 = Cleared by ICH10 based on RSMRST# or by software writing a 1 to this bit. Note that software should first clear the SECOND_TO_STS bit before writing a 1 to clear the BOOT_STS bit. 1 = Set to 1 when the SECOND_TO_STS bit goes from 0 to 1 and the processor has not fetched the first instruction. If rebooting due to a second TCO timer timeout, and if the BOOT_STS bit is set, the ICH10 will reboot using the 'safe' multiplier (1111). This allows the system to recover from a processor frequency multiplier that is too high, and allows the BIOS to check the BOOT_STS bit at boot. If the bit is set and the frequency multiplier is 1111, then the BIOS knows that the processor has been programmed to an invalid multiplier.
1	**SECOND_TO_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = ICH10 sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the ICH10 will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.

Bit	Description
0	**Intruder Detect (INTRD_DET)** — R/WC. 0 = Software clears this bit by writing a 1 to it, or by RTCRST# assertion. 1 = Set by ICH10 to indicate that an intrusion was detected. This bit is set even if the system is in G3 state. **NOTES:** 1. This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. 2. If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits (TCOBASE + 0Ah, bits 2:1), to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMI's (because the INTRD_SEL bits would select that no SMI# be generated). 3. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the

13.9.6 TCO1_CNT—TCO1 Control Register

I/O Address:	TCOBASE +08h	Attribute:	R/W, R/WLO, R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:13	Reserved
12	**TCO_LOCK** — R/WLO. When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	**TCO Timer Halt (TCO_TMR_HLT)** — R/W. 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting and prevent Alert On LAN event messages from being transmitted on the SMLINK (but not Alert On LAN* heartbeat messages).
10	Reserved
9	**NMI2SMI_EN** — R/W. 0 = Normal NMI functionality. 1 = Forces all NMIs to instead cause SMIs. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit as detailed in the following table: **NMI_EN** / **GBL_SMI_EN** / **Description** 0b / 0b / No SMI# at all because GBL_SMI_EN = 0 0b / 1b / SMI# will be caused due to NMI events 1b / 0b / No SMI# at all because GBL_SMI_EN = 0 1b / 1b / No SMI# due to NMI because NMI_EN = 1
8	**NMI_NOW** — R/WC. 0 = Software clears this bit by writing a 1 to it. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared. 1 = Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force an entry to the NMI handler.
7:0	Reserved

13.9.7 TCO2_CNT—TCO2 Control Register

I/O Address:	TCOBASE +0Ah	Attribute:	R/W
Default Value:	0008h	Size:	16-bit
Lockable:	No	Power Well:	Resume

Bit	Description
15:6	Reserved
5:4	**OS_POLICY** — R/W. OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 = Boot normally 01 = Shut down 10 = Don't load OS. Hold in pre-boot state and use LAN to determine next step 11 = Reserved **NOTE:** These are just scratchpad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	**GPIO11_ALERT_DISABLE** — R/W. At reset (via RSMRST# asserted) this bit is set and GPIO[11] alerts are disabled. 0 = Enable. 1 = Disable GPIO11/SMBALERT# as an alert source for the heartbeats and the SMBus slave.
2:1	**INTRD_SEL** — R/W. This field selects the action to take if the INTRUDER# signal goes active. 00 = No interrupt or SMI# 01 = Interrupt (as selected by TCO_INT_SEL). 10 = SMI 11 = Reserved
0	Reserved

13.9.8 TCO_MESSAGE1 and TCO_MESSAGE2 Registers

I/O Address:	TCOBASE +0Ch (Message 1) TCOBASE +0Dh (Message 2)	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Resume

Bit	Description
7:0	**TCO_MESSAGE[*n*]** — R/W. BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress

13.9.9 TCO_WDCNT—TCO Watchdog Control Register

Offset Address:	TCOBASE + 0Eh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Power Well:	Resume		

Bit	Description
7:0	The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will reset to 00h based on a RSMRST# (but not PLTRST#). The external microcontroller can read this register to monitor boot progress.

13.9.10 SW_IRQ_GEN—Software IRQ Generation Register

Offset Address:	TCOBASE + 10h	Attribute:	R/W
Default Value:	03h	Size:	8 bits
Power Well:	Core		

Bit	Description
7:2	Reserved
1	**IRQ12_CAUSE** — R/W. When software sets this bit to 1, IRQ12 will be asserted. When software sets this bit to 0, IRQ12 will be deasserted.
0	**IRQ1_CAUSE** — R/W. When software sets this bit to 1, IRQ1 will be asserted. When software sets this bit to 0, IRQ1 will be deasserted.

13.9.11 TCO_TMR—TCO Timer Initial Value Register

I/O Address:	TCOBASE +12h	Attribute:	R/W
Default Value:	0004h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Initial Value** — R/W. Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of ±1 tick (0.6s). The TCO Timer will only count down in the S0 state.

13.10 General Purpose I/O Registers (D31:F0)

The control for the general purpose I/O signals is handled through a separate 64-byte I/O space (consumer Only) and 128-byte I/O space (Corporate Only). The base offset for this space is selected by the GPIOBASE register.

Table 13-13. Registers to Control GPIO Address Map

GPIOBASE + Offset	Mnemonic	Register Name	Default	Access
00h–03h	GPIO_USE_SEL	GPIO Use Select	197F75FFh	R/W
04h–07h	GP_IO_SEL	GPIO Input/Output Select	E0EA6FFFh	R/W
08h–0Bh	—	Reserved	—	—
0Ch–0Fh	GP_LVL	GPIO Level for Input or Output	E2FEEFFFh	R/W
10h–13h	—	Reserved	—	—
14h–17h	—	Reserved	—	—
18h–1Bh	GPO_BLINK	GPIO Blink Enable	00040000h	R/W
1Ch–1Fh	GP_SER_BLINK	GP Serial Blink	00000000h	R/W
20–23h	GP_SB_CMDSTS	GP Serial Blink Command Status	00080000h	R/W
24–27h	GP_SB_DATA	GP Serial Blink Data	00000000h	R/W
28–2Bh		Reserved		
2C–2Fh	GPI_INV	GPIO Signal Invert	00000000h	R/W
30h–33h	GPIO_USE_SEL2	GPIO Use Select 2	070300FFh	R/W
34h–37h	GP_IO_SEL2	GPIO Input/Output Select 2	1B55FFF0h	R/W
38h–3Bh	GP_LVL2	GPIO Level for Input or Output 2	1FFEFFF3h	R/W
3Ch–3Fh	—	Reserved	—	—
40h–43h (Corporate Only)	GPIO_USE_SEL3	GPIO Use Select 3		R/W
44h–47h (Corporate Only)	GPIO_SEL3	GPIO Input/Output Select 3		R/W
48h–4Bh (Corporate Only)	GP_LVL3	GPIO Level for Input or Output 3		R/W
4Ch–5Fh (Corporate Only)	—	Reserved	—	—
60h–63h	GP_RST_SEL	GPIO Reset Select		R/W
64h–7Fh (Corporate Only)	—	Reserved	—	—

13.10.1 GPIO_USE_SEL—GPIO Use Select Register

Offset Address:	GPIOBASE + 00h	Attribute:	R/W
Default Value:	197F75FFh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GPIO_USE_SEL[31:0]** — R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTES:** 1. The following bits are always 1 because they are always unMultiplexed: 8, 12, 13, 17, 18, 20, 27 and 28. 2. If GPIO[n] does not exist, then, the n-bit in this register will always read as 0 and writes will have no effect. 3. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 4. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. 5. All GPIOs are reset to the default state by CF9h reset except GPIO24. 6. Bit 26 may be overridden by bit 8 in the GEN_PMCON_3 Register.

13.10.2 GP_IO_SEL—GPIO Input/Output Select Register

Offset Address:	GPIOBASE +04h	Attribute:	R/W
Default Value:	E0EA6FFFh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_IO_SEL[31:0]** — R/W. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.

13.10.3 GP_LVL—GPIO Level for Input or Output Register

Offset Address:	GPIOBASE +0Ch	Attribute:	R/W
Default Value:	E2FEEFFFh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_LVL[31:0]**— R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode.

13.10.4 GPO_BLINK—GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	00040000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_BLINK[31:0]** — R/W. The setting of this bit has no effect if the corresponding GPIO signal is programmed as an input. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set. The value of the corresponding GP_LVL bit remains unchanged during the blink process, and does not effect the blink in any way. The GP_LVL bit is not altered when programmed to blink. It will remain at its previous value. These bits correspond to GPIO in the Resume well. These bits revert to the default value based on RSMRST# or a write to the CF9h register (but not just on PLTRST#).

NOTE: GPIO18 will blink by default immediately after reset. This signal could be connected to an LED to indicate a failed boot (by programming BIOS to clear GP_BLINK18 after successful POST).

13.10.5 GP_SER_BLINK—GP Serial Blink

Offset Address:	GPIOBASE +1Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_SER_BLINK[31:0]** — R/W. The setting of this bit has no effect if the corresponding GPIO is programmed as an input or if the corresponding GPIO has the GPO_BLINK bit set. When set to a '0', the corresponding GPIO will function normally. When using serial blink, this bit should be set to a 1 while the corresponding GP_IO_SEL bit is set to 1. Setting the GP_IO_SEL bit to 0 after the GP_SER_BLINK bit ensures ICH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled. The ICH will serialize messages through an open-drain buffer configuration. The value of the corresponding GP_LVL bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.

13.10.6 GP_SB_CMDSTS—GP Serial Blink Command Status

Offset Address:	GPIOBASE +20h	Attribute:	R/W, RO
Default Value:	00000800h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:24	Reserved
23:22	**Data Length Select (DLS)** — R/W. This field determines the number of bytes to serialize on GPIO 00 = Serialize bits 7:0 of GP_SB_DATA (1 byte) 01 = Serialize bits 15:0 of GP_SB_DATA (2 bytes) 10 = Undefined - Software must not write this value 11 = Serialize bits 31:0 of GP_SB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.
21:16	**Data Rate Select (DRS)** — R/W. This field selects the number of 120ns time intervals to count between Manchester data transitions. The default of 8h results in a 960ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	Reserved
8	**Busy** — RO. This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	Reserved
0	**Go** — R/W. This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

13.10.7 GP_SB_DATA—GP Serial Blink Data

Offset Address:	GPIOBASE +24h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:0	**GP_SB_DATA[31:0]** — R/W. This register contains the data serialized out. The number of bits shifted out are selected through the DLS field in the GP_SB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

13.10.8 GPI_INV—GPIO Signal Invert Register

Offset Address:	GPIOBASE +2Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	CPU I/O for 17, Core for 16, 7:0

Bit	Description
31:0	**Input Inversion (GP_INV[n])** — R/W. This bit only has effect if the corresponding GPIO is used as an input and used by the GPE logic, where the polarity matters. When set to '1', then the GPI is inverted as it is sent to the GPE logic that is using it. This bit has no effect on the value that is reported in the GP_LVL register. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the ICH10. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register. 0 = The corresponding GPI_STS bit is set when the ICH10 detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the ICH10 detects the state of the input pin to be low.

13.10.9 GPIO_USE_SEL2—GPIO Use Select 2 Register

Offset Address:	GPIOBASE +30h	Attribute:	R/W
Default Value:	070300FFh (Consumer Only) TBDh (Corporate Only)	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0 Corporate Only	**GPIO_USE_SEL2[63:32]**— R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTES:** 1. The following bit is always 1 because it is always unMultiplexed: 17. The following bits are unMultiplexed in desktop and are also 1: 0, 1, 2, 24 and 26. 2. If GPIO[n] does not exist, then, the (n-32) bit in this register will always read as 0 and writes will have no effect. The following bits are always 0: 29, 30 and 31. 3. After a full reset RSMRST# all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 4. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. 5. Bit 26 is ignored, functionality is configured by bits 9:8 of FLMAP0 register. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32 and bit 28 corresponds to GPIO60.
31:29 Consumer Only	Always 0. No corresponding GPIO.
28:0 Consumer Only	**GPIO_USE_SEL2[63:32]**— R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTES:** 1. The following bit is always 1 because it is always unMultiplexed: 17. The following bits are unMultiplexed in desktop and are also 1: 0, 1, 2, 24 and 26. 2. If GPIO[n] does not exist, then, the (n-32) bit in this register will always read as 0 and writes will have no effect. The following bits are always 0: 29, 30 and 31. 3. After a full reset RSMRST# all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 4. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. 5. Bit 26 is ignored, functionality is configured by bits 9:8 of FLMAP0 register. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32 and bit 28 corresponds to GPIO60.

13.10.10 GP_IO_SEL2—GPIO Input/Output Select 2 Register

Offset Address:	GPIOBASE +34h	Attribute:	R/W
Default Value:	1B55FFF0h (Consumer Only) TBDh (Corporate Only)	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0 Corporate Only	**GP_IO_SEL2[63:32]** — R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.
31:29 Consumer Only	Always 0. No corresponding GPIO.
28:0 Consumer Only	**GP_IO_SEL2[63:32]** — R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.

13.10.11 GP_LVL2—GPIO Level for Input or Output 2 Register

Offset Address:	GPIOBASE +38h	Attribute:	R/W
Default Value:	1FFEFFF3h (Consumer Only) TBDh (Corporate Only)	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0 Corporate Only	**GP_LVL[63:32]** — R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.
31:29 Consumer Only	Reserved. Read-only 0
28:0 Consumer Only	**GP_LVL[63:32]** — R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.

13.10.12 GPIO_USE_SEL3—GPIO Use Select 3 Register (Corporate Only)

Offset Address:	GPIOBASE +40h	Attribute:	R/W
Default Value:	TBDh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:9	Always 0. No corresponding GPIO.
8	**GPIO_USE_SEL3[72]**— R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTES:** 1. If GPIO[n] does not exist, then, the (n-32) bit in this register will always read as 0 and writes will have no effect. 2. After a full reset RSMRST# all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 3. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64 and bit 32 corresponds to GPIO95.
7:0	Always 0. No corresponding GPIO.

13.10.13 GP_IO_SEL3—GPIO Input/Output Select 3 Register (Corporate Only)

Offset Address:	GPIOBASE +44h	Attribute:	R/W
Default Value:	00000x00h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:9	Always 0. No corresponding GPIO.
8	**GP_IO_SEL3[72]** — R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL3 register) is programmed as an input. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64.
7:0	Always 0. No corresponding GPIO.

13.10.14 GP_LVL3—GPIO Level for Input or Output 3 Register (Corporate Only)

Offset Address:	GPIOBASE +48h	Attribute:	R/W
Default Value:	1FFEFFF3h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:9	Reserved. Read-only 0
8	**GP_LVL[72]** — R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64.
7:0	Reserved. Read-only 0

13.10.15 GP_RST_SEL — GPIO Reset Select

Offset Address:	GPIOBASE +60h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:11	Reserved
10	GPIO_RST_SEL**[31:00]** - R/W. Corresponding registers will be reset by internal suspend well reset. Corresponding registers will be reset by RSMRST# pin only. **NOTE:** In ICH10, only the reset for GPIO10 is selectable between RSMRST# pin and internal resume well reset. All the GP_RST_SEL registers are only reset-able by RSMRST# pin.
9:0	Reserved

§ §

14 SATA Controller Registers (D31:F2)

14.1 PCI Configuration Registers (SATA–D31:F2)

Note: Address locations that are not shown should be treated as Reserved.

All of the SATA registers are in the core well. None of the registers can be locked.

Table 14-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	See register description	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14h–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18h–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1Ch–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20h–23h	BAR	Legacy Bus Master Base Address	00000001h	R/W, RO
24h–27h	ABAR / SIDPBA	AHCI Base Address / SATA Index Data Pair Base Address	See register description	See register description
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h-41h	IDE_TIM	Primary IDE Timing Register	0000h	R/W

Table 14-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
42h-43h	IDE_TIM	Secondary IDE Timing Register	0000h	R/W
70h–71h	PID	PCI Power Management Capability ID	See register description	RO
72h–73h	PC	PCI Power Management Capabilities	See register description	RO
74h–75h	PMCS	PCI Power Management Control and Status	See register description	R/W, RO, R/WC
80h–81h	MSICI	Message Signaled Interrupt Capability ID	7005h	RO
82h–83h	MSIMC	Message Signaled Interrupt Message Control	0000h	RO, R/W
84h–87h	MSIMA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
88h–89h	MSIMD	Message Signaled Interrupt Message Data	0000h	R/W
90h	MAP	Address Map	0000h	R/W
92h–93h	PCS	Port Control and Status	0000h	R/W, RO
94h-97h	SCGC	SATA Clock Gating Control	00000000h	R/W
9Ch-9Fh	SCLKGC	SATA Clock General Configuration	00000000h	R/W, R/WO
A8h-ABh	SCAP0	SATA Capability Register 0	0010B012h	RO, R/WO
ACh-AFh	SCAP1	SATA Capability Register 1	00000048h	RO
B0h-B1h	FLRCID	FLR Capability ID	0009h	RO
B2h-B3h	FLRCLV	FLR Capability Length and Version	See register description	R/WO, RO
B4h-B5h	FLRCTRL	FLR Control	0000h	RO, R/W
C0h	ATC	APM Trapping Control	00h	R/W
C4h	ATS	ATM Trapping Status	00h	R/WC
D0h–D3h	SP	Scratch Pad	00000000h	R/W
E0h–E3h	BFCS	BIST FIS Control/Status	00000000h	R/W, R/WC
E4h–E7h	BFTD1	BIST FIS Transmit Data, DW1	00000000h	R/W
E8h–EBh	BFTD2	BIST FIS Transmit Data, DW2	00000000h	R/W

NOTE: The ICH10 SATA controller is not arbitrated as a PCI device, therefore it does not need a master latency timer.

14.1.1 VID—Vendor Identification Register (SATA—D31:F2)

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

14.1.2 DID—Device Identification Register (SATA—D31:F2)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 SATA controller. **NOTE:** The value of this field will change dependent upon the value of the MAP Register. See Section 14.1.30

14.1.3 PCICMD—PCI Command Register (SATA–D31:F2)

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	Fast Back to Back Enable (FBE) — RO. Reserved as 0.
8	SERR# Enable (SERR_EN) — RO. Reserved as 0.
7	Wait Cycle Control (WCC) — RO. Reserved as 0.
6	**Parity Error Response (PER)** — R/W. 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS) — RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE) — RO. Reserved as 0.
3	Special Cycle Enable (SCE) — RO. Reserved as 0.
2	**Bus Master Enable (BME)** — R/W. This bit controls the ICH10's ability to act as a PCI master for IDE Bus Master transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE)** — R/W / RO. Controls access to the SATA controller's target memory space (for AHCI). This bit is RO '0' when not in AHCI/RAID modes.

Bit	Description
0	**I/O Space Enable (IOSE)** — R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set.

14.1.4 PCISTS — PCI Status Register (SATA–D31:F2)

Address Offset: 06h–07h
Default Value: 02B0h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	Signaled System Error (SSE) — RO. Reserved as 0.
13	**Received Master Abort (RMA)** — R/WC. 0 = Master abort Not generated. 1 = SATA controller, as a master, generated a master abort.
12	Reserved as 0 — RO.
11	Signaled Target Abort (STA) — RO. Reserved as 0.
10:9	**DEVSEL# Timing Status (DEV_STS)** — RO. 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	**Data Parity Error Detected (DPED)** — R/WC. For ICH10, this bit can only be set on read completions received from the bus when there is a parity error. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7	Fast Back to Back Capable (FB2BC) — RO. Reserved as 1.
6	User Definable Features (UDF) — RO. Reserved as 0.
5	66MHz Capable (66MHZ_CAP) — RO. Reserved as 1.
4	**Capabilities List (CAP_LIST)** — RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	**Interrupt Status (INTS)** — RO. Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

14.1.5 RID—Revision Identification Register (SATA—D31:F2)

Offset Address: 08h Attribute: RO

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Specification Update* for the value of the Revision ID Register

14.1.6 PI—Programming Interface Register (SATA–D31:F2)

14.1.6.1 When Sub Class Code Register (D31:F2:Offset 0Ah) = 01h

Address Offset: 09h Attribute: R/W, RO
Default Value: See bit description Size: 8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that the ICH10 supports bus master operation
6:4	Reserved. Will always return 0.
3	**Secondary Mode Native Capable (SNC)** — RO. 0 = Secondary controller only supports legacy mode. 1 = Secondary controller supports both legacy and native modes. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit reports as a 0. When MAP.MV is 00b, this bit reports as a 1.
2	**Secondary Mode Native Enable (SNE)** — R/W. Determines the mode that the secondary channel is operating in. 0 = Secondary controller operating in legacy (compatibility) mode 1 = Secondary controller operating in native PCI mode. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit is read-only (RO). When MAP.MV is 00b, this bit is read/write (R/W). If this bit is set by software, then the PNE bit (bit 0 of this register) must also be set by software. While in theory these bits can be programmed separately, such a configuration is not supported by hardware.
1	**Primary Mode Native Capable (PNC)** — RO. 0 = Primary controller only supports legacy mode. 1 = Primary controller supports both legacy and native modes. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit reports as a 0. When MAP.MV is 00b, this bit reports as a 1
0	**Primary Mode Native Enable (PNE)** — R/W. Determines the mode that the primary channel is operating in. 0 = Primary controller operating in legacy (compatibility) mode. 1 = Primary controller operating in native PCI mode. If this bit is set by software, then the SNE bit (bit 2 of this register) must also be set by software simultaneously.

14.1.6.2 When Sub Class Code Register (D31:F2:Offset 0Ah) = 04h

Address Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interface (IF)** — RO. When configured as RAID, this register becomes read only 0.

14.1.6.3 When Sub Class Code Register (D31:F2:Offset 0Ah) = 06h

Address Offset: 09h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interface (IF)** — RO. Indicates the SATA Controller supports AHCI, rev 1.2.

14.1.7 SCC—Sub Class Code Register (SATA–D31:F2)

Address Offset: 0Ah
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** This field specifies the sub-class code of the controller, per the table below: Intel® ICH10 Only: **SCC Register Attribute** — **SCC Register Value** RO — 01h (IDE Controller) Intel® Matrix Storage Technology Enabled ICH10 components Only: **MAP.SMS (D31:F2:Offset 90h:bit 7:6)** — **SCC Default Register Value** 00b — 01h (IDE Controller) 01b — 06h (AHCI Controller) 10b — 04h (RAID Controller)

14.1.8 BCC—Base Class Code Register (SATA–D31:F2)

Address Offset: 0Bh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. 01h = Mass storage device

14.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F2)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)** — RO. 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

14.1.10 HTYPE—Header Type (SATA–D31:F2)

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-function Device (MFD)** — RO. Indicates this SATA controller is not part of a multifunction device.
6:0	**Header Layout (HL)** — RO. Indicates that the SATA controller uses a target device layout.

14.1.11 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F2)

Address Offset: 10h–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address** — R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

14.1.12 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F2)

Address Offset: 14h–17h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address** — R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

14.1.13 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset: 18h–1Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address** — R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

14.1.14 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset: 1Ch–1Fh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address** — R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

14.1.15 BAR — Legacy Bus Master Base Address Register (SATA–D31:F2)

Address Offset:	20h–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte IO space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:5	**Base Address** — R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
4	**Base**— R/W / RO. When SCC is 01h, this bit will be R/W resulting in requesting 16B of I/O space. When SCC is not 01h, this bit will be Read Only 0, resulting in requesting 32B of I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

14.1.16 ABAR/SIDPBA1 — AHCI Base Address Register/Serial ATA Index Data Pair Base Address (SATA–D31:F2)

When the programming interface is not IDE (i.e. SCC is not 01h), this register is named ABAR. When the programming interface is IDE, this register becomes SIDPBA.

Note that hardware does not clear those BA bits when switching from IDE component to non-IDE component or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after component switching (as indicated by a change in SCC). In the case, this register will then have to be re-programmed to a proper value.

14.1.16.1 When SCC is not 01h

When the programming interface is not IDE, the register represents a memory BAR allocating space for the AHCI memory registers defined in Section 14.4.

.

Address Offset:	24-27h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:11	**Base Address (BA)** — R/W. Base address of register memory space (aligned to 1 KB)
10:4	Reserved
3	**Prefetchable (PF)** — RO. Indicates that this range is not pre-fetchable
2:1	**Type (TP)** — RO. Indicates that this range can be mapped anywhere in 32-bit address space.
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 0 to indicate a request for register memory space.

NOTE:
1. The ABAR register must be set to a value of 0001_0000h or greater.

14.1.16.2 When SCC is 01h

When the programming interface is IDE, the register becomes an I/O BAR allocating 16 bytes of I/O space for the I/O-mapped registers defined in Section 14.2. Note that although 16 bytes of locations are allocated, only 8 bytes are used to as SINDX and SDATA registers; with the remaining 8 bytes preserved for future enhancement.

Address Offset:	24h–27h	Attribute:	R/WO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:4	**Base Address (BA)** — R/W. Base address of the I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Indicates a request for I/O space.

14.1.17 SVID—Subsystem Vendor Identification Register (SATA–D31:F2)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset:	No		

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — R/WO. Value is written by BIOS. No hardware action taken on this value.

14.1.18 SID—Subsystem Identification Register (SATA–D31:F2)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset:	No		

Bit	Description
15:0	**Subsystem ID (SID)** — R/WO. Value is written by BIOS. No hardware action taken on this value.

14.1.19 CAP—Capabilities Pointer Register (SATA–D31:F2)

Address Offset:	34h	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** — RO. Indicates that the first capability pointer offset is 80h. This value changes to 70h if the Sub Class Code (SCC) (Dev 31:F2:0Ah) is configure as IDE mode (value of 01).

14.1.20 INT_LN—Interrupt Line Register (SATA–D31:F2)

Address Offset: 3Ch
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line** — R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to. Interrupt Line register is not reset by FLR.

14.1.21 INT_PN—Interrupt Pin Register (SATA–D31:F2)

Address Offset: 3Dh
Default Value: See Register Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin** — RO. This reflects the value of D31IP.SIP (Chipset Config Registers:Offset 3100h:bits 11:8).

14.1.22 IDE_TIM — IDE Timing Register (SATA–D31:F2)

Address Offset: Primary: 40h–41h
Secondary: 42h–43h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15	**IDE Decode Enable (IDE)** — R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the Intel® ICH10 to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary) and Control Block (3F6h for primary and 376h for secondary). This bit effects the IDE decode ranges for both legacy and native-Mode decoding. **NOTE:** This bit affects SATA operation in both combined and non-combined ATA modes. See Section 5.16 for more on ATA modes of operation.
14:0	Reserved

14.1.23 PID—PCI Power Management Capability Identification Register (SATA–D31:F2)

Address Offset: 70h–71h
Default Value: XX01h
Attribute: RO
Size: 16 bits

Bits	Description
15:8	Next Capability (NEXT) — RO. B0h — if SCC = 01h (IDE mode) indicating next item is FLR capability pointer. A8h — for all other values of SCC to point to the next capability structure.
7:0	Capability ID (CID) — RO. Indicates that this pointer is a PCI power management.

14.1.24 PC—PCI Power Management Capabilities Register (SATA–D31:F2)

Address Offset: 72h–73h
Default Value: x003h
Attribute: RO
Size: 16 bits

Bits	Description
15:11	**PME Support (PME_SUP)** — RO. 00000 = If SCC = 01h, indicates no PME support in IDE mode. 01000 = If SCC is not 01h, in a non-IDE mode, indicates PME# can be generated from the $D3_{HOT}$ state in the SATA host controller.
10	D2 Support (D2_SUP) — RO. Hardwired to 0. The D2 state is not supported
9	D1 Support (D1_SUP) — RO. Hardwired to 0. The D1 state is not supported
8:6	**Auxiliary Current (AUX_CUR)** — RO. PME# from $D3_{COLD}$ state is not supported, therefore this field is 000b.
5	**Device Specific Initialization (DSI)** — RO. Hardwired to 0 to indicate that no device-specific initialization is required.
4	Reserved
3	PME Clock (PME_CLK) — RO. Hardwired to 0 to indicate that PCI clock is not required to generate PME#.
2:0	**Version (VER)** — RO. Hardwired to 011 to indicates support for Revision 1.2 of the PCI Power Management Specification.

14.1.25 PMCS—PCI Power Management Control and Status Register (SATA–D31:F2)

Address Offset: 74h–75h
Default Value: xx08h
Function Level Reset: No (Bits 8 and 15)
Attribute: R/W, R/WC
Size: 16 bits

Bits	Description
15	**PME Status (PMES)** — R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller Note: Whenever SCC = 01h, hardware will automatically change the attribute of this bit to RO '0'. Software is advised to clear PMEE and PMES together prior to changing SCC thru MAP.SMS. This bit is not reset by Function Level Reset.
14:9	Reserved
8	**PME Enable (PMEE)** — R/W. When set, the SATA controller generates PME# form $D3_{HOT}$ on a wake event. Note: Whenever SCCSCC = 01h, hardware will automatically change the attribute of this bit to RO '0'. Software is advised to clear PMEE and PMES together prior to changing SCC thru MAP.SMS. This bit is not reset by Function Level Reset.
7:4	Reserved

Bits	Description
3	**No Soft Reset (NSFRST)** — RO. These bits are used to indicate whether devices transitioning from $D3_{HOT}$ state to D0 state will perform an internal reset. 0 = Device transitioning from $D3_{HOT}$ state to D0 state perform an internal reset. 1 = Device transitioning from $D3_{HOT}$ state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the $D3_{HOT}$ state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from $D3_{HOT}$ state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	Reserved
1:0	**Power State (PS)** — R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

14.1.26 MSICI—Message Signaled Interrupt Capability Identification (SATA–D31:F2)

Address Offset:	80h–81h	Attribute:	RO
Default Value:	7005h	Size:	16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:8	**Next Pointer (NEXT)** — RO. Indicates the next item in the list is the PCI power management pointer.
7:0	**Capability ID (CID)** — RO. Capabilities ID indicates MSI.

14.1.27 MSIMC—Message Signaled Interrupt Message Control (SATA–D31:F2)

Address Offset: 82h–83h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>15:8</td><td>Reserved</td></tr>
<tr><td>7</td><td>64 Bit Address Capable (C64) — RO. Capable of generating a 32-bit message only.</td></tr>
<tr><td>6:4</td><td>Multiple Message Enable (MME) — R/W.
= 000 (and MSIE is set), a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
For 6 port components:
<table>
<tr><th>MME</th><th>Value Driven on MSI Memory Write</th><th></th><th></th><th></th></tr>
<tr><th></th><th>Bits[15:3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr>
<tr><td>000,
001, 010</td><td>MD[15:3]</td><td>MD[2]</td><td>MD[1]</td><td>MD[0]</td></tr>
<tr><td>100</td><td>MD[15:3]</td><td>Port 0: 0
Port 1: 0
Port 2: 0
Port 3: 0
Port 4: 1
Port 5: 1</td><td>Port 0: 0
Port 1: 0
Port 2: 1
Port 3: 1
Port 4: 0
Port 5: 0</td><td>Port 0: 0
Port 1: 1
Port 2: 0
Port 3: 1
Port 4: 0
Port 5: 1</td></tr>
</table>
For 4 port components:
<table>
<tr><th>MME</th><th>Value Driven on MSI Memory Write</th><th></th><th></th><th></th></tr>
<tr><th></th><th>Bits[15:3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr>
<tr><td>000,
001, 010</td><td>MD[15:3]</td><td>MD[2]</td><td>MD[1]</td><td>MD[0]</td></tr>
<tr><td>100</td><td>MD[15:3]</td><td>Port 0: 0
Port 1: 0
Port 4: 1
Port 5: 1</td><td>Port 0: 0
Port 1: 0
Port 2: 0
Port 3: 0</td><td>Port 0: 0
Port 1: 1
Port 2: 0
Port 3: 1</td></tr>
</table>
Values ‘011b’ to ‘111b’ are reserved. If this field is set to one of these reserved values, the results are undefined.
NOTE: Note: The CCC interrupt is generated on unimplemented port (AHCI PI register bit equal to 0). If CCC interrupt is disabled, no MSI shall be generated for the port dedicated to the CCC interrupt. When CCC interrupt occurs, MD[2:0] is dependant on CCC_CTL.INT (in addition to MME).</td></tr>
</table>

Bits	Description
3:1	**Multiple Message Capable (MMC)** — RO. Indicates the number of interrupt messages supported by the ICH10 SATA controller. 000 =1 MSI Capable (When SCC bit is set to 01h. MSI is not supported in IDE mode) 100 = 8 MSI Capable
0	**MSI Enable (MSIE)** — R/W /RO. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. This bit is RW when SC.SCC is not 01h and is read-only 0 when SCC is 01h. Note that CMD.ID bit has no effect on MSI. **NOTE:** Software must clear this bit to '0' to disable MSI first before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to '0' when operating in legacy mode (when GHC.AE = 0).

14.1.28 MSIMA— Message Signaled Interrupt Message Address (SATA–D31:F2)

Address Offset: 84h–87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
31:2	**Address (ADDR)** — R/W. Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	Reserved

14.1.29 MSIMD—Message Signaled Interrupt Message Data (SATA–D31:F2)

Address Offset: 88h-89h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:0	**Data (DATA)** — R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction. Note that when the MME field is set to '001' or '010', bit [0] and bits [1:0] respectively of the MSI memory write transaction will be driven based on the source of the interrupt rather than from MD[2:0]. See the description of the MME field.

14.1.30 MAP—Address Map Register (SATA–D31:F2)

Address Offset: 90h Attribute: R/W, R/WO
Default Value: 0000h Size: 16 bits
Function Level Reset: No (Bits 7:5 and 13:8 only)

Bits	Description
15:14	Reserved
13:8	Reserved
7:6	**SATA Mode Select (SMS)** — R/W. SW programs these bits to control the mode in which the SATA Controller should operate: 00b = IDE mode 01b = AHCI mode 10b = RAID mode 11b = Reserved **NOTES:** 1. The SATA Function Device ID will change based on the value of this register. 2. When switching from AHCI or RAID mode to IDE mode, a 2 port SATA controller (Device 31, Function 5) will be enabled. 3. AHCI mode may only be selected when MV = 00 4. RAID mode may only be selected when MV = 00 5. Programming these bits with values that are invalid (e.g. selecting RAID when in combined mode) will result in indeterministic behavior by the HW 6. SW shall not manipulate SMS during runtime operation; i.e. the OS will not do this. The BIOS may choose to switch from one mode to another during POST. These bits are not reset by Function Level Reset.
5	**SATA Port-to-Controller Configuration (SC)** — R/W. This bit changes the number of SATA ports available within each SATA Controller. 0 = Up to 4 SATA ports are available for Controller 1 (Device 31 Function 2) with ports [3:0] and up to 2 SATA ports are available for Controller 2 (Device 31 Function 5) with ports [5:4]. 1 = Up to 6 SATA ports are available for Controller 1 (Device 31 Function 2) with ports [5:0] and no SATA ports are available for Controller 2 (Device 31 Function 5). **NOTE:** This bit should be set to 1 only in AHCI mode. This bit is not reset by Function Level Reset.
4:2	Reserved.
1:0	**Map Value (MV)** — RO. Reserved

14.1.31 PCS—Port Control and Status Register (SATA–D31:F2)

Address Offset: 92h–93h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits
Function Level Reset: No

By default, the SATA ports are set to the disabled state (bits [5:0] = ‘0’). When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the “off” state and cannot detect any devices.

If an AHCI-aware or RAID enabled operating system is being booted, then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port’s PxSCTL and

PxCMD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Bits	Description
15	**OOB Retry Mode (ORM)** — RW. 0 = The SATA controller will not retry after an OOB failure 1 = The SATA controller will continue to retry after an OOB failure until successful (infinite retry)
14	Reserved.
13	**Port 5 Present (P5P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P5E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 5 has been detected.
12	**Port 4 Present (P4P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P4E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 4 has been detected.
11	**Port 3 Present (P3P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P3E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 3 has been detected.
10	**Port 2 Present (P2P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P2E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 2 has been detected.
9	**Port 1 Present (P1P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P1E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected.
8	**Port 0 Present (P0P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P0E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected.
7:6	Reserved
5	**Port 5 Enabled (P5E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P5CMD.SUD (offset ABAR+298h:bit 1) If MAP.SC is '0', if SCC is '01h' this bit will be read only '0' or if MAP.SPD[5] is '1'.

Bits	Description
4	**Port 4 Enabled (P4E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P4CMD.SUD (offset ABAR+298h:bit 1) If MAP.SC is '0', if SCC is '01h' this bit will be read only '0' or if MAP.SPD[4] is '1'.
3	**Port 3 Enabled (P3E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P3CMD.SUD (offset ABAR+298h:bit 1). When MAP.SPD[3] is '1' this is reserved and is read-only 0.
2	**Port 2 Enabled (P2E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1). When MAP.SPD[2] is '1' this is reserved and is read-only 0.
1	**Port 1 Enabled (P1E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is '1' this is reserved and is read-only 0.
0	**Port 0 Enabled (P0E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **NOTE:** This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is '1' this is reserved and is read-only 0.

14.1.32 SCLKCG—SATA Clock Gating Control Register

Address Offset: 94h-97h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:30	Reserved.
29:24	**Port Clock Disable (PCD)** — 0 = All clocks to the associated port logic will operate normally. 1 = The backbone clock driven to the associated port logic is gated and will not toggle. Bit 29: Port 5 Bit 28: Port 4 Bit 27: Port 3 BIt 26: Port 2 Bit 25: Port 1 Bit 24: Port 0 If a port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bits to 1 on ports that are disabled. Software cannot set the PCD [port x]='1' if the corresponding PCS.PxE='1' in either Dev31Func2 or Dev31Func5 (dual controller IDE mode).
23:9	Reserved.
8:0	**SCLKCG Field 1** — R/W. BIOS must program these bits to 193h.

14.1.33 SCLKGC—SATA Clock General Configuration Register

Address Offset: 9Ch-9Fh
Default Value: 00000000h
Function Level Reset: No
Attribute: R/W, R/WO
Size: 32 bits

Bit	Description
31:8	Reserved
7 (ICH10 Base Only)	Reserved
7 (ICH10R, ICH10DO, and ICH10D Only)	**Alternate ID Enable (AIE)** — R/WO. 0 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the following Device ID 2822h for Desktop and the Microsoft Windows Vista* in-box version of the Intel® Matrix Storage Manager will load on the platform. 1 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the Device ID reported in the *Intel® I/O Controller Hub 10 (ICH10) Family Specification Update* to prevent the Microsoft Windows Vista in-box version of the Intel Matrix Storage Manager from loading on the platform and will require the user to perform an 'F6' installation of the appropriate Intel Matrix Storage Manager. **NOTE:** This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST#. BIOS is required to reprogram the value of this bit after resuming from S3, S4 and S5.
6:2	**SATA Traffic Monitor— R/W.** 00000b = Disable. 00011b = Enable. SATA Traffic Monitor allows for aggressive C2 Pop down by monitoring SATA bus mastering activity. When enabled, BIOS must ensure bit 3 and bit 4 of Cx_STATE_CNF (Cx State Configuration Register) are ones. Note: This field is reset by PLTRST# and BIOS is required to reprogram the value after resuming from S3–S5. All other bit combinations are Reserved.
1	**SATA2-port Configuration Indicator (SATA2PIND)** — RO. 0 = Normal configuration. 1 = One IDE Controller is implemented supporting only two ports for a Primary Master and a Secondary Master. **NOTE:** When set, BIOS must ensure that bit 2 and bit 3 of the AHCI PI registers are zeros. BIOS must also make sure that Port 2 and Port 3 are disabled (via PCS configuration register) and the port clocks are gated (via SCLKCG configuration register).
0	**SATA4-port All Master Configuration Indicator (SATA4PMIND)** — RO. 0 = Normal configuration. 1 = Two IDE Controllers are implemented, each supporting two ports for a Primary Master and a Secondary Master. **NOTE:** When set, BIOS must ensure that bit 2 and bit 3 of the AHCI PI registers are zeros. BIOS must also make sure that Port 2 and Port 3 are disabled (via PCS configuration register) and the port clocks are gated (via SCLKCG configuration register).

14.1.33.1 SATACR0—SATA Capability Register 0 (SATA–D31:F2)

Address Offset:	A8h–ABh	Attribute:	RO, R/WO
Default Value:	0010B012h	Size:	32 bits
Function Level Reset:	No (Bits 15:8 only)		

Note: This register shall be read-only 0 when SCC is 01h.

Bit	Description
31:24	Reserved
23:20	**Major Revision (MAJREV)** — RO: Major revision number of the SATA Capability Pointer implemented.
19:16	**Minor Revision (MINREV)** — RO: Minor revision number of the SATA Capability Pointer implemented.
15:8	**Next Capability Pointer (NEXT)** — R/WO: Points to the next capability structure. These bits are not reset by Function Level Reset.
7:0	**Capability ID (CAP)**— RO: This value of 12h has been assigned by the PCI SIG to designate the SATA Capability Structure.

14.1.33.2 SATACR1—SATA Capability Register 1 (SATA–D31:F2)

Address Offset:	ACh–AFh	Attribute:	RO
Default Value:	00000048h	Size:	32 bits

Note: This register shall be read-only 0 when SCC is 01h.

Bit	Description
31:16	Reserved
15:4	**BAR Offset (BAROFST)** — RO**:** Indicates the offset into the BAR where the Index/Data pair are located (in Dword granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (max 16KB)
3:0	**BAR Location (BARLOC)** — RO**:** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in Dword granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 – 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010 – 1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This isn't supported in ICH10.

14.1.34 FLRCID—FLR Capability ID (SATA–D31:F2)

Address Offset: B0-B1h Attribute: RO
Default Value: 0009h Size: 16 bits

Bit	Description
15:8	**Next Capability Pointer** — RO. 00h indicates the final item in the capability list.
7:0	**Capability ID** — RO. The value of this field depends on the FLRCSSEL bit. 13h = If PFLRCSSEL = 0 09h (Vendor Specific) = If PFLRCSSEL = 1

14.1.35 FLRCLV—FLR Capability Length and Version (SATA–D31:F2)

Address Offset: B2-B3h Attribute: RO, R/WO
Default Value: xx06h Size: 16 bits
Function Level Reset: No (Bit 9:8 Only when FLRCSSEL = '0')

When FLRCSSEL = '0', this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**FLR Capability** — R/WO. 1 = Support for Function Level reset. This bit is not reset by the Function Level Reset.
8	**TXP Capability** — R/WO. 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Vendor-Specific Capability ID** — RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

When FLRCSSEL = '1', this register is defined as follows:

Bit	Description
15:12	**Vendor-Specific Capability ID** — RO. A value of 2h identifies this capability as the Function Level Reset (FLR).
11:8	**Capability Version** — RO. This field indicates the version of the FLR capability.
7:0	**Vendor-Specific Capability ID** — RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

14.1.36 FLRC—FLR Control (SATA–D31:F2)

Address Offset: B4-B5h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)** — RO. 0 = Controller has received all non-posted requests. 1 = Controller has issued non-posted requests which has not been completed.
7:1	Reserved.
0	**Initiate FLR** — R/W. Used to initiate FLR transition. A write of '1' indicates FLR transition. Since hardware must no t respond to any cycles till FLR completion the value read by software from this bit is '0'.

14.1.37 ATC—APM Trapping Control Register (SATA–D31:F2)

Address Offset: C0h
Default Value: 00h
Attribute: R/W
Size: 8 bits
Function Level Reset: No

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST)** — R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 1 for the trap and/or SMI# to occur.
2	**Secondary Master Trap (SPT)** — R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 0 for the trap and/or SMI# to occur.
1	**Primary Slave Trap (PST)** — R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 1 for the trap and/or SMI# to occur.
0	**Primary Master Trap (PMT)** — R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 0 for the trap and/or SMI# to occur.

14.1.38 ATS—APM Trapping Status Register (SATA–D31:F2)

Address Offset: C4h
Default Value: 00h
Function Level Reset: No
Attribute: R/WC
Size: 8 bits

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST)** — R/WC. Indicates that a trap occurred to the secondary slave device.
2	**Secondary Master Trap (SPT)** — R/WC. Indicates that a trap occurred to the secondary master device.
1	**Primary Slave Trap (PST)** — R/WC. Indicates that a trap occurred to the primary slave device.
0	**Primary Master Trap (PMT)** — R/WC. Indicates that a trap occurred to the primary master device.

14.1.39 SP Scratch Pad Register (SATA–D31:F2)

Address Offset: D0h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Data (DT)** — R/W. This is a read/write register that is available for software to use. No hardware action is taken on this register.

14.1.40 BFCS—BIST FIS Control/Status Register (SATA–D31:F2)

Address Offset: E0h–E3h
Default Value: 00000000h
Attribute: R/W, R/WC
Size: 32 bits

Bits	Description
31:16	Reserved
15	**Port 5 BIST FIS Initiate (P5BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 5, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 5 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P5BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
14	**Port 4 BIST FIS Initiate (P4BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 4, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 4 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P4BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
13	**Port 3 BIST FIS Initiate (P3BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 3, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 3 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P3BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
12	**Port 2 BIST FIS Initiate (P2BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 2, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
11	**BIST FIS Successful (BFS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by ICH10 receives an R_OK completion status from the device. **NOTE:** This bit must be cleared by software prior to initiating a BIST FIS.

Bits	Description
10	**BIST FIS Failed (BFF)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by ICH10 receives an R_ERR completion status from the device. **NOTE:** This bit must be cleared by software prior to initiating a BIST FIS.
9	**Port 1 BIST FIS Initiate (P1BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 1, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
8	**Port 0 BIST FIS Initiate (P0BFI)** — R/W. When a rising edge is detected on this bit field, the ICH10 initiates a BIST FIS to the device on Port 0, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the ICH10 to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully
7:2	**BIST FIS Parameters (BFP)** — R/W. These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the ICH10. This field is not port specific — its contents will be used for any BIST FIS initiated on port 0, port 1, port 2 or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	Reserved

14.1.41 BFTD1—BIST FIS Transmit Data1 Register (SATA–D31:F2)

Address Offset: E4h–E7h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 1** — R/W. The data programmed into this register will form the contents of the second dword of any BIST FIS initiated by the ICH10. This register is not port specific — its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”, this register’s contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

14.1.42 BFTD2—BIST FIS Transmit Data2 Register (SATA–D31:F2)

Address Offset: E8h–EBh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 2** — R/W. The data programmed into this register will form the contents of the third dword of any BIST FIS initiated by the ICH10. This register is not port specific — its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”, this register’s contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

14.2 Bus Master IDE I/O Registers (D31:F2)

The bus master IDE function uses 16 bytes of I/O space, allocated via the BAR register, located in Device 31:Function 2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or dword quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. All I/O registers are reset by Function Level Reset. The description of the I/O registers is shown in Table 14-2.

Table 14-2. Bus Master IDE I/O Register Address Map

BAR+ Offset	Mnemonic	Register	Default	Type
00	BMICP	Command Register Primary	00h	R/W
01	—	Reserved	—	RO
02	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03	—	Reserved	—	RO
04–07	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08	BMICS	Command Register Secondary	00h	R/W
09	—	Reserved	—	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	—	Reserved	—	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xxxxxxxxh	R/W
10h	AIR	AHCI Index Register	00000000h	R/W, RO
14h	AIDR	AHCI Index Data Register	xxxxxxxxh	R/W

14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2)

Address Offset:	Primary: BAR + 00h Secondary: BAR + 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved. Returns 0.
3	**Read / Write Control (R/WC)** — R/W. This bit sets the direction of the bus master transfer: This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved. Returns 0.
0	**Start/Stop Bus Master (START)** — R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit (D31:F2:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F1:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. **NOTE:** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a

14.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F2)

Address Offset:	Primary: BAR + 02h Secondary: BAR + 0Ah	Attribute:	R/W, R/WC, RO
Default Value:	00h	Size:	8 bits

Bit	Description
7	**PRD Interrupt Status (PRDIS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the host controller execution of a PRD that has its PRD_INT bit set.
6	**Drive 1 DMA Capable** — R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The Intel® ICH10 does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
5	**Drive 0 DMA Capable** — R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The ICH10 does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0.
2	**Interrupt** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts via the IEN bit of the Device Control Register (see chapter 5 of the *Serial ATA Specification*, Revision 1.0a).
1	**Error** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)** — RO. 0 = This bit is cleared by the ICH10 when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the ICH10 when the Start Bus Master bit (D31:F2:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the ICH10 when the Start bit is written to the Command register.

14.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F2)

Address Offset: Primary: BAR + 04h–07h Attribute: R/W
Secondary: BAR + 0Ch–0Fh
Default Value: All bits undefined Size: 32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)** — R/W. The bits in this field correspond to bits [31:2] of the memory location of the Physical Region Descriptor (PRD). The Descriptor Table must be Dword-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

14.2.4 AIR—AHCI Index Register (D31:F2)

Address Offset: Primary: BAR + 10h Attribute: R/W
Default Value: 00000000h Size: 32 bits

This register is available only when SCC is not 01h.

Bit	Description
31:11	Reserved
10:2	**Index (INDEX)**— R/W**:** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	Reserved

14.2.5 AIDR—AHCI Index Data Register (D31:F2)

Address Offset: Primary: BAR + 14h Attribute: R/W
Default Value: All bits undefined Size: 32 bits

This register is available only when SCC is not 01h.

Bit	Description
31:0	**Data (DATA)**— R/W**:** This Data register is a “window” through which data is read or written to the AHCI memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be setup prior to the read or write to this Data register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by Index.

14.3 Serial ATA Index/Data Pair Superset Registers

All of these I/O registers are in the core well. They are exposed only when SCC is 01h (i.e., IDE programming interface).

These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software-write operations to the reserved locations will have no effect while software-read operations to the reserved locations will return 0.

Offset	Mnemonic	Register
00h–03h	SINDEX	Serial ATA Index
04h–07h	SDATA	Serial ATA Data
08h–0Ch	—	Reserved
0Ch–0Fh	—	Reserved

14.3.1 SINDX – Serial ATA Index (D31:F2)

Address Offset: SIDPBA + 00h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15.8	**Port Index (PIDX)** - R/W: This Index field is used to specify the port of the SATA controller at which the port-specific SSTS, SCTL, and SERR registers are located. 00h = Primary Master (Port 0) 01h = Primary Slave (Port 2) 02h = Secondary Master (Port 1) 03h = Secondary Slave (Port 3) All other values are Reserved.
7:0	**Register Index (RIDX)** - R/W: This index field is used to specify one out of three registers currently being indexed into. These three registers are the Serial ATA superset SStatus, SControl and SError memory registers and are port specific, hence for this SATA controller, there are four sets of these registers. Refer to Section 14.4.3.10, Section 14.4.3.11, and Section 14.4.3.12 for definitions of the SStatus, SControl, and SError registers. 00h = SSTS 01h = SCTL 02h = SERR All other values are Reserved.

14.3.2 SDATA – Serial ATA Data (D31:F2)

Address Offset: SIDPBA + 04h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Data (DATA)** - R/W: This Data register is a “window” through which data is read or written to from the register pointed to by the Serial ATA Index (SINDX) register above. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by SINDX.RIDX field.

14.3.2.1 PxSSTS—Serial ATA Status Register (D31:F2)

Address Offset: Attribute: RO
Default Value: 00000000h Size: 32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The ICH10 updates it continuously and asynchronously. When the ICH10 transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)** — RO. Indicates the current interface state: **Value** **Description** 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)** — RO. Indicates the negotiated interface communication speed. **Value** **Description** 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated All other values reserved. ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)** — RO. Indicates the interface device detection and Phy state: **Value** **Description** 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

14.3.2.2 PxSCTL — Serial ATA Control Register (D31:F2)

Address Offset: Attribute: R/W, RO
Default Value: 00000004h Size: 32 bits

SDATA when SINDX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the ICH10 or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	Port Multiplier Port (PMP) — RO. This field is not used by AHCI.
15:12	Select Power Management (SPM) — RO. This field is not used by AHCI.
11:8	**Interface Power Management Transitions Allowed (IPM)** — R/W**.** Indicates which power states the ICH10 is allowed to transition to: **Value** **Description** 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)** — R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** **Description** 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to Generation 2 communication rate All other values reserved. ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection Initialization (DET)** — R/W**.** Controls the ICH10's device detection and interface initialization. **Value** **Description** 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the ICH10 initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the ICH10 is running results in undefined behavior.

14.3.2.3 PxSERR—Serial ATA Error Register (D31:F2)

Address Offset: Attribute: R/WC
Default Value: 00000000h Size: 32 bits

SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)**: When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)**: Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
22	**Handshake (H)**: Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)**: Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)**: This field is not used by AHCI.
19	**10b to 8b Decode Error (B)**: Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)**: Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)**: Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)**: When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the ICH10, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)**: The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)**: A violation of the Serial ATA protocol was detected. Note: The ICH10 does not set this bit for all protocol violations that may occur on the SATA link.

Bit	Description
9	**Persistent Communication or Data Integrity Error (C)**: A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)**: A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)**: Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)**: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

14.4 AHCI Registers (D31:F2)

Note: These registers are AHCI-specific and available when the ICH10 is properly configured. The Serial ATA Status, Control, and Error registers are special exceptions and may be accessed on all ICH10 components if properly configured; see Section 14.3 for details.

The memory mapped registers within the SATA controller exist in non-cacheable memory space. Additionally, locked accesses are not supported. If software attempts to perform locked transactions to the registers, indeterminate results may occur. Register accesses shall have a maximum size of 64-bits; 64-bit access must not cross an 8-byte alignment boundary. All memory registers are reset by Function Level Reset unless specified otherwise.

The registers are broken into two sections – generic host control and port control. The port control registers are the same for all ports, and there are as many registers banks as there are ports.

Table 14-3. AHCI Register Address Map

ABAR + Offset	Mnemonic	Register
00–1Fh	GHC	Generic Host Control
20h–FFh	—	Reserved
100h–17Fh	P0PCR	Port 0 port control registers
180h–1FFh	P1PCR	Port 1 port control registers
200h–27Fh	P2PCR	Port 2 port control registers
280h–2FFh	P3PCR	Port 3 port control registers
300h–37Fh	P4PCR	Port 4 port control registers
380h–3FFh	P5PCR	Port 5 port control registers

14.4.1 AHCI Generic Host Control Registers (D31:F2)

Table 14-4. Generic Host Controller Register Address Map

ABAR + Offset	Mnemonic	Register	Default	Type
00–03	CAP	Host Capabilities	FF22FFC2h	R/WO, RO
04–07	GHC	Global ICH10 Control	00000000h	R/W, RO
08–0Bh	IS	Interrupt Status	00000000h	R/WC
0Ch–0Fh	PI	Ports Implemented	00000000h	R/WO, RO
10h-13h	VS	AHCI Version	00010200h	RO
14h-17h	CCC_CTL	Command Completion Coalescing Control	00010121h	R/W, RO
18h-1Bh	CCC_PORTS	Command Completion Coalescing Ports	00000000h	R/W
1Ch-1Fh	EM_LOC	Enclosure Management Location	01000002h	RO
20h-23h	EM_CTRL	Enclosure Management Control	07010000h	R/W, R/WO, RO
A0h-A3h	VSP	Vendor Specific	00000000h	RO, R/WO

14.4.1.1 CAP—Host Capabilities Register (D31:F2)

Address Offset: ABAR + 00h–03h
Attribute: R/WO, RO
Default Value: FF22FFC2h (Consumer Only)
FF22FF45h (Corporate Only)
Size: 32 bits
Function Level Reset: No

All bits in this register that are R/WO are reset only by PLTRST#.

Bit	Description
31	**Supports 64-bit Addressing (S64A)** — RO. Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	**Supports Command Queue Acceleration (SCQA)** — RO. Hardwired to 1 to indicate that the SATA controller supports SATA command queuing via the DMA Setup FIS. The Intel® ICH10 handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	Supports SNotification Register (SSNTF): — RO. The ICH10 SATA Controller does not support the SNotification register.
28	**Supports Interlock Switch (SIS)** — R/WO. Indicates whether the SATA controller supports interlock switches on its ports for use in Hot Plug operations. This value is loaded by platform BIOS prior to OS initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	**Supports Staggered Spin-up (SSS)** — R/WO. Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.

Bit	Description
26	**Supports Aggressive Link Power Management (SALP)** — R/WO. 0 = Software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	**Supports Activity LED (SAL)** — RO. Indicates that the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	**Supports Command List Override (SCLO)** — R/WO. When set to 1, indicates that the Controller supports the PxCMD.CLO bit and it's associated function. When cleared to 0, the controller is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	**Interface Speed Support (ISS)** — R/WO. Indicates the maximum speed the SATA controller can support on its ports. 2h =3.0 Gb/s.
19	Supports Non-Zero DMA Offsets (SNZO) — RO. Reserved, as per the AHCI Revision 1.2 specification
18	**Supports AHCI Mode Only (SAM)** — RO. The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only
17	**Supports Port Multiplier (PMS)** — R/WO. ICH10 does not support port multiplier. **NOTE:** This bit must be set to 0. Port multiplier is not supported by ICH10.
16	Reserved
15	**PIO Multiple DRQ Block (PMD)** — RO. The SATA controller supports PIO Multiple DRQ Command Block
14	**Slumber State Capable (SSC)** — R/WO. The SATA controller supports the slumber state.
13	**Partial State Capable (PSC)** — R/WO. The SATA controller supports the partial state.
12:8	**Number of Command Slots (NCS)** — RO. Hardwired to 1Fh to indicate support for 32 slots.
7 (Consumer Only)	**Command Completion Coalescing Supported (CCCS)** — R/WO. 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported
7 (Corporate Only)	**Command Completion Coalescing Supported (CCCS)** — RO. Command Completion Coalescing is not supported. Reads to this bit return 0.
6	**Enclosure Management Supported (EMS)** — R/WO. 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	**Supports External SATA (SXS)** — R/WO. 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, SW can examine each SATA port's Command Register (PxCMD) to determine which port is routed externally.
4:0	**Number of Ports (NPS)** — RO. Hardwired to 5h to indicate support for 6 ports. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register.

14.4.1.2 GHC—Global ICH10 Control Register (D31:F2)

Address Offset: ABAR + 04h–07h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**AHCI Enable (AE)** — R/W. When set, indicates that an AHCI driver is loaded and the controller will be talked to via AHCI mechanisms. This can be used by an ICH10 that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the controller will not be talked to as legacy. 0 = Software will communicate with the ICH10 using legacy mechanisms. 1 = Software will communicate with the ICH10 using AHCI. The ICH10 will not have to allow command processing via both AHCI and legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers.
30:3	Reserved
2	**MSI Revert to Single Message (MRSM)** — RO: When set to 1 by hardware, indicates that the host controller requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to '0', the Controller has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). "MC.MSIE = '1' (MSI is enabled) "MC.MMC > 0 (multiple messages requested) "MC.MME > 0 (more than one message allocated) "MC.MME!= MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not "reverting" to that mode. For ICH10, the Controller shall always revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit is ignored when GHC.HR = 1.
1	**Interrupt Enable (IE)** — R/W. This global bit enables interrupts from the ICH10. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	**Controller Reset (HR)** — R/W. Resets ICH10 AHCI controller. 0 = No effect 1 = When set by SW, this bit causes an internal reset of the ICH10 AHCI controller. All state machines that relate to data transfers and queuing return to an idle condition, and all ports are re-initialized via COMRESET. **NOTE:** For further details, consult section 12.3.3 of the *Serial ATA Advanced Host Controller Interface* specification.

14.4.1.3 IS—Interrupt Status Register (D31:F2)

Address Offset: ABAR + 08h–0Bh
Attribute: R/WC
Default Value: 00000000h
Size: 32 bits

This register indicates which of the ports within the controller have an interrupt pending and require service.

Bit	Description
31:7	Reserved. Returns 0.
6	**Coalescing Interrupt Pending Status (CIPS)** — R/WC. 0 = No interrupt pending. 1 = A command completion coalescing interrupt has been generated.
5	**Interrupt Pending Status Port[5] (IPS[5])** — R/WC. 0 = No interrupt pending. 1 = Port 5 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
4	**Interrupt Pending Status Port[4] (IPS[4])** — R/WC. 0 = No interrupt pending. 1 = Port 4 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
3	**Interrupt Pending Status Port[3] (IPS[3])** — R/WC. 0 = No interrupt pending. 1 = Port 3 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
2	**Interrupt Pending Status Port[2] (IPS[2])** — R/WC 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
1	**Interrupt Pending Status Port[1] (IPS[1])** — R/WC. 0 = No interrupt pending. 1 = Port 1has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	**Interrupt Pending Status Port[0] (IPS[0])** — R/WC. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

14.4.1.4 PI—Ports Implemented Register (D31:F2)

Address Offset:	ABAR + 0Ch–0Fh	Attribute:	R/WO, RO
Default Value:	00000000h	Size:	32 bits
Function Level Reset:	No		

This register indicates which ports are exposed to the ICH10. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. For ports that are not available, software must not read or write to registers within that port.

Bit	Description
31:6	Reserved. Returns 0.
5	**Ports Implemented Port 5 (PI5)** — R/WO. 0 = The port is not implemented. 1 = The port is implemented. This bit is read-only '0' if MAP.SC = '0' or SCC = '01h'.
4	**Ports Implemented Port 4 (PI4)** — R/WO. 0 = The port is not implemented. 1 = The port is implemented. This bit is read-only '0' if MAP.SC = '0' or SCC = '01h'.
3	**Ports Implemented Port 3 (PI3)** — R/WO. 0 = The port is not implemented. 1 = The port is implemented.
2	**Ports Implemented Port 2 (PI2)**— R/WO. 0 = The port is not implemented. 1 = The port is implemented.
1	**Ports Implemented Port 1 (PI1)** — R/WO. 0 = The port is not implemented. 1 = The port is implemented.
0	**Ports Implemented Port 0 (PI0)** — R/WO. 0 = The port is not implemented. 1 = The port is implemented.

14.4.1.5 VS—AHCI Version (D31:F2)

Address Offset: ABAR + 10h–13h Attribute: RO
Default Value: 00010200h Size: 32 bits

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h. The current version of the specification is 1.20 (00010200h).

Bit	Description
31:16	**Major Version Number (MJR)** — RO. Indicates the major version is 1
15:0	**Minor Version Number (MNR)** — RO. Indicates the minor version is 20.

14.4.1.6 CCC_CTL—Command Completion Coalescing Control Register (D31:F2)

Address Offset: ABAR + 14h–17h Attribute: R/W, RO
Default Value: 00010131h Size: 32 bits

This register is used to configure the command coalescing feature. This register is reserved if command coalescing is not supported (CAP_CCCS = ‘0’).

Bit	Description
31:16	**Timeout Value (TV)** — R/W. The timeout value is specified in 10 microsecond intervals. hbaCCC_Timer is loaded with this timeout value. hbaCCC_Timer is only decremented when commands are outstanding on the selected ports. The Controller will signal a CCC interrupt when hbaCCC_Timer has decremented to ‘0’. The hbaCCC_Timer is reset to the timeout value on the assertion of each CCC interrupt. A timeout value of 0 is invalid.
15:8	**Command Completions (CC)** — R/W. Specifies the number of command completions that are necessary to cause a CCC interrupt. The Controller has an internal command completion counter, hbaCCC_CommandsComplete. hbaCCC_CommandsComplete is incremented by one each time a selected port has a command completion. When hbaCCC_CommandsComplete is equal to the command completions value, a CCC interrupt is signaled. The internal command completion counter is reset to ‘0’ on the assertion of each CCC interrupt.
7:3	**Interrupt (INT)** — RO. Specifies the interrupt used by the CCC feature. This interrupt must be marked as unused in the AHCI Ports Implemented memory register by the corresponding bit being set to ‘0’. Thus, the CCC_interrupt corresponds to the interrupt for an unimplemented port on the controller. When a CCC interrupt occurs, the IS[INT] bit shall be asserted to ‘1’ regardless of whether PIRQ interrupt or MSI is used. Note that in MSI, CC interrupt may share an interrupt vector with other ports. For example, if the number of message allocated is 4, then CCC interrupt share interrupt vector 3 along with port 3, 4, and 5 but IS[6] shall get set.
2:1	Reserved
0	**Enable (EN)** — R/W. 0 = The command completion coalescing feature is disabled and no CCC interrupts are generated 1 = The command completion coalescing feature is enabled and CCC interrupts may be generated based on timeout or command completion conditions. Software shall only change the contents of the TV and CC fields when EN is cleared to '0'. On transition of this bit from '0' to '1', any updated values for the TV and CC fields shall take effect.

14.4.1.7 CCC_Ports—Command Completion Coalescing Ports Register (D31:F2)

Address Offset:	ABAR + 18h–1Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register is used to specify the ports that are coalesced as part of the CCC feature when CCC_CTL.EN = '1'. This register is reserved if command coalescing is not supported (CAP_CCCS = '0').

Bit	Description
31:0	**Ports (PRT)** — R/W. 0 = The port is not part of the command completion coalescing feature. 1 = The corresponding port is part of the command completion coalescing feature. Bits set to '1' in this register must also have the corresponding bit set to '1' in the Ports Implemented register. Bits set to '1' in this register must also have the corresponding bit set to '1' in the Ports Implemented register. An updated value for this field shall take effect within one timer increment (1 millisecond).

14.4.1.8 EM_LOC—Enclosure Management Location Register (D31:F2)

Address Offset:	ABAR + 1Ch–1Fh	Attribute:	RO
Default Value:	01000002h	Size:	32 bits

This register identifies the location and size of the enclosure management message buffer. This register is reserved if enclosure management is not supported (i.e., CAP.EMS = 0).

Bit	Description
31:16	**Offset (OFST)** — RO. The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	**Buffer Size (SZ)** — RO. Specifies the size of the transmit message buffer area in Dwords. The ICH10 SATA controller only supports transmit buffer. A value of '0' is invalid.

14.4.1.9 EM_CTRL—Enclosure Management Control Register (D31:F2)

Address Offset:	ABAR + 20h–23h	Attribute:	R/W, R/WO, RO
Default Value:	07010000h	Size:	32 bits

This register is used to control and obtain status for the enclosure management interface. This register includes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any message are pending, and is used to initiate sending messages. This register is reserved if enclosure management is not supported (CAP_EMS = '0').

Bit	Description
31:27	Reserved
26	**Activity LED Hardware Driven (ATTR.ALHD)** — R/WO. 1 = The SATA controller drives the activity LED for the LED message type in hardware and does not utilize software for this LED. The host controller does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	**Transmit Only (ATTR.XMT)** — RO. 0 = The SATA controller supports transmitting and receiving messages. 1 = The SATA controller only supports transmitting messages and does not support receiving messages.
24	**Single Message Buffer (ATTR.SMB)** — RO. 0 = There are separate receive and transmit buffers such that unsolicited messages could be supported. 1 = The SATA controller has one message buffer that is shared for messages to transmit and messages received. Unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer.
23:20	Reserved
19	**SGPIO Enclosure Management Messages (SUPP.SGPIO):** — RO. 1 = The SATA controller supports the SGPIO register interface message type.
18	**SES-2 Enclosure Management Messages (SUPP.SES2):** — RO. 1 = The SATA controller supports the SES-2 message type.
17	**SAF-TE Enclosure Management Messages (SUPP.SAFTE):** — RO. 1 = The SATA controller supports the SAF-TE message type.
16	**LED Message Types (SUPP.LED):** — RO. 1 = The SATA controller supports the LED message type.
15:10	Reserved
9	**Reset (RST):** — R/W. 0 = A write of '0' to this bit by software will have no effect. 1 = When set by software, The SATA controller shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted / received after the reset. After the SATA controller completes the reset operation, the SATA controller shall set the value to '0'.
8	**Transmit Message (CTL.TM):** — R/W. 0 = A write of '0' to this bit by software will have no effect. 1 = When set by software, The SATA controller shall transmit the message contained in the message buffer. When the message is completely sent, the SATA controller shall set the value to '0'. Software shall not change the contents of the message buffer while CTL.TM is set to '1'.
7:1	Reserved
0	**Message Received (STS.MR):** — RO. Message Received is not supported in ICH10.

14.4.2 Vendor Specific Registers (D31:F2)

14.4.2.1 VSP—Vendor Specific (D31:F2)

Address Offset: ABAR + A0h–A3h Attribute: RO, RWO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	**Supports Low Power Device Detection** (SLPD)— RWO Indicates whether SATA power management and device hot (un)pulg is supported. 0 = Not supported. 1 = Supported.

14.4.3 Port Registers (D31:F2)

Ports not available will result in the corresponding Port DMA register space being reserved. The controller shall ignore writes to the reserved space on write cycles and shall return ‘0’ on read cycle accesses to the reserved location.

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 1 of 3)

ABAR + Offset	Mnemonic	Register
100h–103h	P0CLB	Port 0 Command List Base Address
104h–107h	P0CLBU	Port 0 Command List Base Address Upper 32-Bits
108h–10Bh	P0FB	Port 0 FIS Base Address
10Ch–10Fh	P0FBU	Port 0 FIS Base Address Upper 32-Bits
110h–113h	P0IS	Port 0 Interrupt Status
114h–117h	P0IE	Port 0 Interrupt Enable
118h–11Bh	P0CMD	Port 0 Command
11Ch–11Fh	—	Reserved
120h–123h	P0TFD	Port 0 Task File Data
124h–127h	P0SIG	Port 0 Signature
128h–12Bh	P0SSTS	Port 0 Serial ATA Status
12Ch–12Fh	P0SCTL	Port 0 Serial ATA Control
130h–133h	P0SERR	Port 0 Serial ATA Error
134h–137h	P0SACT	Port 0 Serial ATA Active
138h–13Bh	P0CI	Port 0 Command Issue
13Ch–17Fh	—	Reserved
180h–183h	P1CLB	Port 1 Command List Base Address
184h–187h	P1CLBU	Port 1 Command List Base Address Upper 32-Bits
188h–18Bh	P1FB	Port 1 FIS Base Address
18Ch–18Fh	P1FBU	Port 1 FIS Base Address Upper 32-Bits
190h–193h	P1IS	Port 1 Interrupt Status
194h–197h	P1IE	Port 1 Interrupt Enable
198h–19Bh	P1CMD	Port 1 Command
19Ch–19Fh	—	Reserved
1A0h–1A3h	P1TFD	Port 1 Task File Data
1A4h–1A7h	P1SIG	Port 1 Signature

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 2 of 3)

ABAR + Offset	Mnemonic	Register
1A8h–1ABh	P1SSTS	Port 1 Serial ATA Status
1ACh–1AFh	P1SCTL	Port 1 Serial ATA Control
1B0h–1B3h	P1SERR	Port 1 Serial ATA Error
1B4h–1B7h	P1SACT	Port 1 Serial ATA Active
1B8h–1BBh	P1CI	Port 1 Command Issue
1BCh–1FFh	—	Reserved
200h–203h	P2CLB	Port 2 Command List Base Address
204h–207h	P2CLBU	Port 2 Command List Base Address Upper 32-Bits
208h–20Bh	P2FB	Port 2 FIS Base Address
20Ch–20Fh	P2FBU	Port 2 FIS Base Address Upper 32-Bits
210h–213h	P2IS	Port 2 Interrupt Status
214h–217h	P2IE	Port 2 Interrupt Enable
218h–21Bh	P2CMD	Port 2 Command
21Ch–21Fh	—	Reserved
220h–223h	P2TFD	Port 2 Task File Data
224h–227h	P2SIG	Port 2 Signature
228h–22Bh	P2SSTS	Port 2 Serial ATA Status
22Ch–22Fh	P2SCTL	Port 2 Serial ATA Control
230h–233h	P2SERR	Port 2 Serial ATA Error
234h–237h	P2SACT	Port 2 Serial ATA Active
238h–23Bh	P2CI	Port 2 Command Issue
23Ch–27Fh	—	Reserved
280h–283h	P3CLB	Port 3 Command List Base Address
284h–287h	P3CLBU	Port 3 Command List Base Address Upper 32-Bits
288h–28Bh	P3FB	Port 3 FIS Base Address
28Ch–28Fh	P3FBU	Port 3 FIS Base Address Upper 32-Bits
290h–293h	P3IS	Port 3 Interrupt Status
294h–297h	P3IE	Port 3 Interrupt Enable
298h–29Bh	P3CMD	Port 3 Command
29Ch–29Fh	—	Reserved
2A0h–2A3h	P3TFD	Port 3 Task File Data
2A4h–2A7h	P3SIG	Port 3 Signature
2A8h–2ABh	P3SSTS	Port 3 Serial ATA Status
2ACh–2AFh	P3SCTL	Port 3 Serial ATA Control
2B0h–2B3h	P3SERR	Port 3 Serial ATA Error
2B4h–2B7h	P3SACT	Port 3 Serial ATA Active
2B8h–2BBh	P3CI	Port 3 Command Issue
2BCh–2FFh	—	Reserved
300h–303h	P4CLB	Port 4 Command List Base Address
304h–307h	P4CLBU	Port 4 Command List Base Address Upper 32-Bits
308h–30Bh	P4FB	Port 4 FIS Base Address
30Ch–30Fh	P4FBU	Port 4 FIS Base Address Upper 32-Bits
310h–313h	P4IS	Port 4 Interrupt Status
314h–317h	P4IE	Port 4 Interrupt Enable
318h–31Bh	P4CMD	Port 4 Command
31Ch–31Fh	—	Reserved
320h–323h	P4TFD	Port 4 Task File Data

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 3 of 3)

ABAR + Offset	Mnemonic	Register
324h–327h	P4SIG	Port 4 Signature
328h–32Bh	P4SSTS	Port 4 Serial ATA Status
32Ch–32Fh	P4SCTL	Port 4 Serial ATA Control
330h–333h	P4SERR	Port 4 Serial ATA Error
334h–337h	P4SACT	Port 4 Serial ATA Active
338h–33Bh	P4CI	Port 4 Command Issue
33Ch–37Fh	—	Reserved
380h–383h	P5CLB	Port 5 Command List Base Address
384h–387h	P5CLBU	Port 5 Command List Base Address Upper 32-Bits
388h–38Bh	P5FB	Port 5 FIS Base Address
38Ch–38Fh	P5FBU	Port 5 FIS Base Address Upper 32-Bits
390h–393h	P5IS	Port 5 Interrupt Status
394h–397h	P5IE	Port 5 Interrupt Enable
398h–39Bh	P5CMD	Port 5 Command
39Ch–39Fh	—	Reserved
3A0h–3A3h	P5TFD	Port 5 Task File Data
3A4h–3A7h	P5SIG	Port 5 Signature
3A8h–3ABh	P5SSTS	Port 5 Serial ATA Status
3ACh–3AFh	P5SCTL	Port 5 Serial ATA Control
3B0h–3B3h	P5SERR	Port 5 Serial ATA Error
3B4h–3B7h	P5SACT	Port 5 Serial ATA Active
3B8h–3BBh	P5CI	Port 5 Command Issue
3BCh–3FFh	—	Reserved

14.4.3.1 PxCLB—Port [5:0] Command List Base Address Register (D31:F2)

Address Offset: Port 0: ABAR + 100h
Port 1: ABAR + 180h
Port 2: ABAR + 200h
Port 3: ABAR + 280h
Port 4: ABAR + 300h
Port 5: ABAR + 380h

Attribute: R/W

Default Value: Undefined

Size: 32 bits

Bit	Description
31:10	**Command List Base Address (CLB)** — R/W**.** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a Controller reset.
9:0	Reserved

14.4.3.2 PxCLBU—Port [5:0] Command List Base Address Upper 32-Bits Register (D31:F2)

Address Offset: Port 0: ABAR + 104h
Port 1: ABAR + 184h
Port 2: ABAR + 204h
Port 3: ABAR + 284h
Port 4: ABAR + 304h
Port 5: ABAR + 384h
Attribute: R/W
Default Value: Undefined
Size: 32 bits

Bit	Description
31:0	**Command List Base Address Upper (CLBU)** — R/W**.** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a Controller reset.

14.4.3.3 PxFB—Port [5:0] FIS Base Address Register (D31:F2)

Address Offset: Port 0: ABAR + 108h
Port 1: ABAR + 188h
Port 2: ABAR + 208h
Port 3: ABAR + 288h
Port 4: ABAR + 308h
Port 5: ABAR + 388h
Attribute: R/W
Default Value: Undefined
Size: 32 bits

Bit	Description
31:8	**FIS Base Address (FB)** — R/W**.** Indicates the 32-bit base for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned, as indicated by bits 31:3 being read/write. Note that these bits are not reset on a Controller reset.
7:0	Reserved

14.4.3.4 PxFBU—Port [5:0] FIS Base Address Upper 32-Bits Register (D31:F2)

Address Offset: Port 0: ABAR + 10Ch
Port 1: ABAR + 18Ch
Port 2: ABAR + 20Ch
Port 3: ABAR + 28Ch
Port 4: ABAR + 30Ch
Port 5: ABAR + 38Ch
Attribute: R/W
Default Value: Undefined
Size: 32 bits

Bit	Description
31:0	**Command List Base Address Upper (CLBU)** — R/W**.** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a Controller reset.

14.4.3.5 PxIS—Port [5:0] Interrupt Status Register (D31:F2)

Address Offset: Port 0: ABAR + 110h
Port 1: ABAR + 190h
Port 2: ABAR + 210h
Port 3: ABAR + 290h
Port 4: ABAR + 310h
Port 5: ABAR + 390h
Attribute: R/WC, RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31	**Cold Port Detect Status (CPDS)** — RO. Cold presence detect is not supported.
30	**Task File Error Status (TFES)** — R/WC. This bit is set whenever the status register is updated by the device and the error bit (PxTFD.bit 0) is set.
29	**Host Bus Fatal Error Status (HBFS)** — R/WC. Indicates that the Intel® ICH10 encountered an error that it cannot recover from due to a bad software pointer. In PCI, such an indication would be a target or master abort.
28	**Host Bus Data Error Status (HBDS)** — R/WC. Indicates that the ICH10 encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	**Interface Fatal Error Status (IFS)** — R/WC. Indicates that the ICH10 encountered an error on the SATA interface which caused the transfer to stop.
26	**Interface Non-fatal Error Status (INFS)** — R/WC. Indicates that the ICH10 encountered an error on the SATA interface but was able to continue operation.
25	Reserved
24	**Overflow Status (OFS)** — R/WC. Indicates that the ICH10 received more bytes from a device than was specified in the PRD table for the command.
23	**Incorrect Port Multiplier Status (IPMS)** — R/WC. Indicates that the ICH10 received a FIS from a device whose Port Multiplier field did not match what was expected. **NOTE:** Port Multiplier not supported by ICH10.
22	**PhyRdy Change Status (PRCS)** — RO. When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. Unlike most of the other bits in the register, this bit is RO and is only cleared when PxSERR.DIAG.N is cleared. Note that the internal PhyRdy signal also transitions when the port interface enters partial or slumber power management states. Partial and slumber must be disabled when Surprise Removal Notification is desired, otherwise the power management state transitions will appear as false insertion and removal events.
21:8	Reserved
7	**Device Interlock Status (DIS)** — R/WC. When set, indicates that a platform interlock switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support an interlock switch (CAP.SIS [ABAR+00:bit 28] set). For systems that do not support an interlock switch, this bit will always be 0.
6	**Port Connect Change Status (PCS)** — RO. This bit reflects the state of PxSERR.DIAG.X. (ABAR+130h/1D0h/230h/2D0h, bit 26) Unlike other bits in this register, this bit is only cleared when PxSERR.DIAG.X is cleared. 0 = No change in Current Connect Status. 1 = Change in Current Connect Status.
5	**Descriptor Processed (DPS)** — R/WC. A PRD with the I bit set has transferred all its data.

Bit	Description
4	**Unknown FIS Interrupt (UFS)** — RO. When set to '1' indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to '0' by software clearing the PxSERR.DIAG.F bit to '0'. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to '1' or the two bits may become out of sync.
3	**Set Device Bits Interrupt (SDBS)** — R/WC. A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	**DMA Setup FIS Interrupt (DSS)** — R/WC. A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	**PIO Setup FIS Interrupt (PSS)** — R/WC**.** A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	**Device to Host Register FIS Interrupt (DHRS)** — R/WC. A D2H Register FIS has been received with the I bit set, and has been copied into system memory.

14.4.3.6 PxIE—Port [5:0] Interrupt Enable Register (D31:F2)

Address Offset: Port 0: ABAR + 114h
Port 1: ABAR + 194h
Port 2: ABAR + 214h
Port 3: ABAR + 294h
Port 4: ABAR + 314h
Port 5: ABAR + 394h
Attribute: R/W, RO
Default Value: 00000000h
Size: 32 bits

This register enables and disables the reporting of the corresponding interrupt to system software. When a bit is set ('1') and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled ('0') are still reflected in the status registers.

Bit	Description
31	Cold Presence Detect Enable (CPDE) — RO. Cold Presence Detect is not supported.
30	**Task File Error Enable (TFEE)** — R/W**.** When set, and GHC.IE and PxTFD.STS.ERR (due to a reception of the error register from a received FIS) are set, the Intel® ICH10 will generate an interrupt.
29	**Host Bus Fatal Error Enable (HBFE)** — R/W**.** When set, and GHC.IE and PxS.HBFS are set, the ICH10 will generate an interrupt.
28	**Host Bus Data Error Enable (HBDE)** — R/W**.** When set, and GHC.IE and PxS.HBDS are set, the ICH10 will generate an interrupt.
27	**Host Bus Data Error Enable (HBDE)** — R/W. When set, GHC.IE is set, and PxIS.HBDS is set, the ICH10 will generate an interrupt.
26	**Interface Non-fatal Error Enable (INFE)** — R/W. When set, GHC.IE is set, and PxIS.INFS is set, the ICH10 will generate an interrupt.
25	Reserved
24	**Overflow Error Enable (OFE)** — R/W**.** When set, and GHC.IE and PxS.OFS are set, the ICH10 will generate an interrupt.

Bit	Description
23	**Incorrect Port Multiplier Enable (IPME)** — R/W. When set, and GHC.IE and PxIS.IPMS are set, the ICH10 will generate an interrupt. **NOTE:** Should be written as 0. Port Multiplier not supported by ICH10.
22	**PhyRdy Change Interrupt Enable (PRCE)** — R/W. When set, and GHC.IE is set, and PxIS.PRCS is set, the ICH10 shall generate an interrupt.
21:8	Reserved
7	**Device Interlock Enable (DIE)** — R/W. When set, and PxIS.DIS is set, the ICH10 will generate an interrupt. For systems that do not support an interlock switch, this bit shall be a read-only 0.
6	**Port Change Interrupt Enable (PCE)** — R/W**.** When set, and GHC.IE and PxS.PCS are set, the ICH10 will generate an interrupt.
5	**Descriptor Processed Interrupt Enable (DPE)** — R/W**.** When set, and GHC.IE and PxS.DPS are set, the ICH10 will generate an interrupt
4	**Unknown FIS Interrupt Enable (UFIE)** — R/W**.** When set, and GHC.IE is set and an unknown FIS is received, the ICH10 will generate this interrupt.
3	**Set Device Bits FIS Interrupt Enable (SDBE)** — R/W**.** When set, and GHC.IE and PxS.SDBS are set, the ICH10 will generate an interrupt.
2	**DMA Setup FIS Interrupt Enable (DSE)** — R/W**.** When set, and GHC.IE and PxS.DSS are set, the ICH10 will generate an interrupt.
1	**PIO Setup FIS Interrupt Enable (PSE)** — R/W**.** When set, and GHC.IE and PxS.PSS are set, the ICH10 will generate an interrupt.
0	**Device to Host Register FIS Interrupt Enable (DHRE)** — R/W**.** When set, and GHC.IE and PxS.DHRS are set, the ICH10 will generate an interrupt.

14.4.3.7 PxCMD—Port [5:0] Command Register (D31:F2)

Address Offset: Port 0: ABAR + 118h
Port 1: ABAR + 198h
Port 2: ABAR + 218h
Port 3: ABAR + 298h
Port 4: ABAR + 318h
Port 5: ABAR + 398h
Attribute: R/W, RO, R/WO
Default Value: 0000w00wh
where w = 00?0b (for?, see bit description)
Size: 32 bits
Function Level Reset: No (Bit 21, 19 and 18 only)

Bit	Description
31:28	**Interface Communication Control (ICC)** — R/W. This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register (Address offset Port 0:ABAR+124h, Port 1: ABAR+1A4h, Port 2: ABAR+224h, Port 3: ABAR+2A4h, Port 4: ABAR+224h, Port 5: ABAR+2A4h). **Value** — **Definition** Fh–7h — Reserved 6h — Slumber: This will cause the Intel® ICH10 to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state 5h–3h — Reserved 2h — Partial: This will cause the ICH10 to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h — Active: This will cause the ICH10 to request a transition of the interface into the active 0h — No-Op / Idle: When software reads this value, it indicates the ICH10 is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the ICH10 will perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (e.g. interface is in the active state and a request is made to go to the active state), the ICH10 will take no action and return this field to Idle. **NOTE:** When the ALPE bit (bit 26) is set, then this register should not be set to 02h or 06h.
27	**Aggressive Slumber / Partial (ASP)** — R/W. When set, and the ALPE bit (bit 26) is set, the ICH10 shall aggressively enter the slumber state when it clears the PxCI register and the PxSACT register is cleared. When cleared, and the ALPE bit is set, the ICH10 will aggressively enter the partial state when it clears the PxCI register and the PxSACT register is cleared. If CAP.SALP is cleared to '0', software shall treat this bit as reserved.
26	**Aggressive Link Power Management Enable (ALPE)** — R/W. When set, the ICH10 will aggressively enter a lower link power state (partial or slumber) based upon the setting of the ASP bit (bit 27).

Bit	Description
25	**Drive LED on ATAPI Enable (DLAE)** — R/W**.** When set, the ICH10 will drive the LED pin active for ATAPI commands (PxCLB[CHz.A] set) in addition to ATA commands. When cleared, the ICH10 will only drive the LED pin active for ATA commands. See Section 5.16.9 for details on the activity LED.
24	**Device is ATAPI (ATAPI)** — R/W. When set, the connected device is an ATAPI device. This bit is used by the ICH10 to control whether or not to generate the desktop LED when commands are active. See Section 5.16.9 for details on the activity LED.
23:22	Reserved
21	**External SATA Port (ESP)** — R/WO. 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.
20	Reserved
19	**Interlock Switch Attached to Port (ISP)** — R/WO. When interlock switches are supported in the platform (CAP.SIS [ABAR+00h:bit 28] set), this indicates whether this particular port has an interlock switch attached. This bit can be used by system software to enable such features as aggressive power management, as disconnects can always be detected regardless of PHY state with an interlock switch. When this bit is set, it is expected that HPCP (bit 18) in this register is also set. The ICH10 takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and an interlock switch toggles, the ICH10 still treats it as a proper interlock switch event. Note that these bits are not reset on a Controller reset. This bit is not reset by Function Level Reset.
18	**Hot Plug Capable Port (HPCP)** — R/WO. 0 = Port is not capable of Hot-Plug. 1 = Port is Hot-Plug capable. This indicates whether the platform exposes this port to a device which can be Hot-Plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as “eject device” to the end-user. The ICH10 takes no action on the state of this bit - it is for system software only. For example, if this bit is cleared, and a Hot-Plug event occurs, the ICH10 still treats it as a proper Hot-Plug event. Note that these bits are not reset on a Controller reset. This bit is not reset by Function Level Reset.
17	**Port Multiplier Attached (PMA)** — RO / R/W. When this bit is set, a port multiplier is attached to the ICH10 for this port. When cleared, a port multiplier is not attached to this port. This bit is RO 0 when CAP.PMS (offset ABAR+00h:bit 17) = 0 and R/W when CAP.PMS = 1. This bit may only be set when Px.CMD.ST is cleared.
16	**Port Multiplier FIS Based Switching Enable (PMFSE)** — RO. The ICH10 does not support FIS-based switching. **NOTE:** FIS Port Multiplier not supported by ICH10.
15	**Controller Running (CR)** — RO. When this bit is set, the DMA engines for a port are running. See section 5.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared by the ICH10.

Bit	Description
14	**FIS Receive Running (FR)** — RO. When set, the FIS Receive DMA engine for the port is running. See section 12.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared by the ICH10.
13	**Interlock Switch State (ISS)** — RO. For systems that support interlock switches (via CAP.SIS [ABAR+00h:bit 28]), if an interlock switch exists on this port (via ISP in this register), this bit indicates the current state of the interlock switch. A 0 indicates the switch is closed, and a 1 indicates the switch is opened. For systems that do not support interlock switches, or if an interlock switch is not attached to this port, this bit reports 0.
12:8	**Current Command Slot (CCS)** — RO**.** Indicates the current command slot the ICH10 is processing. This field is valid when the ST bit is set in this register, and is constantly updated by the ICH10. This field can be updated as soon as the ICH10 recognizes an active command slot, or at some point soon after when it begins processing the command. This field is used by software to determine the current command issue location of the ICH10. In queued mode, software shall not use this field, as its value does not represent the current command being executed. Software shall only use PxCI and PxSACT when running queued commands.
7:5	Reserved
4	**FIS Receive Enable (FRE)** — R/W. When set, the ICH10 may post received FISes into the FIS receive area pointed to by PxFB (ABAR+108h/188h/208h/288h) and PxFBU (ABAR+10Ch/18Ch/20Ch/28Ch). When cleared, received FISes are not accepted by the ICH10, except for the first D2H (device-to-host) register FIS after the initialization sequence. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit (bit 14) in this register to be cleared.
3	**Command List Override (CLO)** — R/W. Setting this bit to '1' causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to '0'. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The Controller sets this bit to '0' when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to '0'. A write to this register with a value of '0' shall have no effect. This bit shall only be set to '1' immediately prior to setting the PxCMD.ST bit to '1' from a previous value of '0'. Setting this bit to '1' at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to '0' before setting PxCMD.ST to '1'.

Bit	Description
2	**Power On Device (POD)** — RO. Cold presence detect not supported. Defaults to 1.
1	**Spin-Up Device (SUD)** — R/W / RO This bit is R/W and defaults to 0 for systems that support staggered spin-up (R/W when CAP.SSS (ABAR+00h:bit 27) is 1). Bit is RO 1 for systems that do not support staggered spin-up (when CAP.SSS is 0). 0 = No action. 1 = On an edge detect from 0 to 1, the ICH10 starts a COMRESET initialization sequence to the device. Clearing this bit to '0' does not cause any OOB signal to be sent on the interface. When this bit is cleared to '0' and PxSCTL.DET=0h, the Controller will enter listen mode.
0	**Start (ST)** — R/W. When set, the ICH10 may process the command list. When cleared, the ICH10 may not process the command list. Whenever this bit is changed from a 0 to a 1, the ICH10 starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register is cleared by the ICH10 upon the ICH10 putting the controller into an idle state. Refer to section 12.2.1 of the Serial ATA AHCI Specification for important restrictions on when ST can be set to 1.

14.4.3.8 PxTFD—Port [5:0] Task File Data Register (D31:F2)

Address Offset: Port 0: ABAR + 120h
Port 1: ABAR + 1A0h
Port 2: ABAR + 220h
Port 3: ABAR + 2A0h
Port 4: ABAR + 320h
Port 5: ABAR + 3A0h
Attribute: RO
Default Value: 0000007Fh
Size: 32 bits

This is a 32-bit register that copies specific fields of the task file when FISes are received. The FISes that contain this information are:

D2H Register FIS
PIO Setup FIS
Set Device Bits FIS

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:16</td><td>Reserved</td></tr>
<tr><td>15:8</td><td>Error (ERR) — RO. Contains the latest copy of the task file error register.</td></tr>
<tr><td>7:0</td><td>Status (STS) — RO. Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI.
<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>7</td><td>BSY</td><td>Indicates the interface is busy</td></tr>
<tr><td>6:4</td><td>N/A</td><td>Not applicable</td></tr>
<tr><td>3</td><td>DRQ</td><td>Indicates a data transfer is requested</td></tr>
<tr><td>2:1</td><td>N/A</td><td>Not applicable</td></tr>
<tr><td>0</td><td>ERR</td><td>Indicates an error during the transfer</td></tr>
</table></td></tr>
</table>

14.4.3.9 PxSIG—Port [5:0] Signature Register (D31:F2)

Address Offset:	Port 0: ABAR + 124h Port 1: ABAR + 1A4h Port 2: ABAR + 224h Port 3: ABAR + 2A4h Port 4: ABAR + 324h Port 5: ABAR + 3A4h	Attribute:	RO
Default Value:	FFFFFFFFh	Size:	32 bits

This is a 32-bit register which contains the initial signature of an attached device when the first D2H Register FIS is received from that device. It is updated once after a reset sequence.

Bit	Description
31:0	**Signature (SIG)** — RO**.** Contains the signature received from a device on the first D2H register FIS. The bit order is as follows: **Bit** **Field** 31:24 LBA High Register 23:16 LBA Mid Register 15:8 LBA Low Register 7:0 Sector Count Register

14.4.3.10 PxSSTS—Port [5:0] Serial ATA Status Register (D31:F2)

Address Offset:	Port 0: ABAR + 128h Port 1: ABAR + 1A8h Port 2: ABAR + 228h Port 3: ABAR + 2A8h Port 4: ABAR + 328h Port 5: ABAR + 3A8h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

This is a 32-bit register that conveys the current state of the interface and host. The ICH10 updates it continuously and asynchronously. When the ICH10 transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)** — RO. Indicates the current interface state: **Value** — **Description** 0h — Device not present or communication not established 1h — Interface in active state 2h — Interface in PARTIAL power management state 6h — Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)** — RO. Indicates the negotiated interface communication speed. **Value** — **Description** 0h — Device not present or communication not established 1h — Generation 1 communication rate negotiated 2h — Generation 2 communication rate negotiated All other values reserved. ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)** — RO. Indicates the interface device detection and Phy state: **Value** — **Description** 0h — No device detected and Phy communication not established 1h — Device presence detected but Phy communication not established 3h — Device presence detected and Phy communication established 4h — Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

14.4.3.11 PxSCTL — Port [5:0] Serial ATA Control Register (D31:F2)

Address Offset:	Port 0: ABAR + 12Ch Port 1: ABAR + 1ACh Port 2: ABAR + 22Ch Port 3: ABAR + 2ACh Port 4: ABAR + 32Ch Port 5: ABAR + 3ACh	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the ICH10 or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	**Port Multiplier Port (PMP)** — R/W. This field is not used by AHCI
15:12	Select Power Management (SPM) — R/W. This field is not used by AHCI
11:8	**Interface Power Management Transitions Allowed (IPM)** — R/W**.** Indicates which power states the ICH10 is allowed to transition to: **Value** — **Description** 0h — No interface restrictions 1h — Transitions to the PARTIAL state disabled 2h — Transitions to the SLUMBER state disabled 3h — Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)** — R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** — **Description** 0h — No speed negotiation restrictions 1h — Limit speed negotiation to Generation 1 communication rate 2h — Limit speed negotiation to Generation 2 communication rate ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).

Bit	Description
3:0	**Device Detection Initialization (DET)** — R/W. Controls the ICH10's device detection and interface initialization. **Value** — **Description** 0h — No device detection or initialization action requested 1h — Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h — Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the ICH10 initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the ICH10 is running results in undefined behavior. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

14.4.3.12 PxSERR—Port [5:0] Serial ATA Error Register (D31:F2)

Address Offset: Port 0: ABAR + 130h; Port 1: ABAR + 1B0h; Port 2: ABAR + 230h; Port 3: ABAR + 2B0h; Port 4: ABAR + 330h; Port 5: ABAR + 3B0h — Attribute: R/WC

Default Value: 00000000h — Size: 32 bits

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)** — R/WC. When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)** — R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)** — R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Transport state transition error (T)** — R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.

Bit	Description
22	**Handshake (H)** — R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)** — R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)** — R/WC. This field is not used by AHCI.
19	**10b to 8b Decode Error (B)** — R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)** — R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)** — R/WC. Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)** — R/WC. When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the ICH10, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)** — R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)** — R/WC. A violation of the Serial ATA protocol was detected. Note: The ICH10 does not set this bit for all protocol violations that may occur on the SATA link.
9	**Persistent Communication or Data Integrity Error (C)** — R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)** — R/WC. A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)** — R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)** — R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

14.4.3.13 PxSACT—Port [5:0] Serial ATA Active (D31:F2)

Address Offset:	Port 0: ABAR + 134h Port 1: ABAR + 1B4h Port 2: ABAR + 234h Port 3: ABAR + 2B4h Port 4: ABAR + 334h Port 5: ABAR + 3B4h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

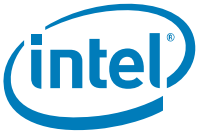
Bit	Description
31:0	**Device Status (DS)** — R/W. System software sets this bit for SATA queuing operations prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software, and as a result of a COMRESET or SRST.

14.4.3.14 PxCI—Port [5:0] Command Issue Register (D31:F2)

Address Offset:	Port 0: ABAR + 138h Port 1: ABAR + 1B8h Port 2: ABAR + 238h Port 3: ABAR + 2B8h Port 4: ABAR + 338h Port 5: ABAR + 3B8h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Commands Issued (CI)** — R/W. This field is set by software to indicate to the ICH10 that a command has been built-in system memory for a command slot and may be sent to the device. When the ICH10 receives a FIS which clears the BSY and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software.

§ §



15 SATA Controller Registers (D31:F5)

15.1 PCI Configuration Registers (SATA–D31:F5)

Note: Address locations that are not shown should be treated as Reserved.

All of the SATA registers are in the core well. None of the registers can be locked.

Table 15-1. SATA Controller PCI Register Address Map (SATA–D31:F5) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	See register description	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10h–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14h–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18h–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1Ch–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20h–23h	BAR	Legacy Bus Master Base Address	00000001h	R/W, RO
24h–27h	SIDPBA	Serial ATA Index / Data Pair Base Address	00000000h	See register description
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO

Table 15-1. SATA Controller PCI Register Address Map (SATA–D31:F5) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
40h-41h	IDE_TIM	Primary IDE Timing Register	0000h	R/W
42h-43h	IDE_TIM	Secondary IDE Timing Registers	0000h	R/W
70h–71h	PID	PCI Power Management Capability ID	See register description	RO
72h–73h	PC	PCI Power Management Capabilities	4003h	RO
74h–75h	PMCS	PCI Power Management Control and Status	0008h	R/W, RO, R/WC
80h–81h (Consumer Only)	MSICI	Message Signaled Interrupt Capability ID	7005h	RO
82h–83h (Consumer Only)	MSIMC	Message Signaled Interrupt Message Control	0000h	RO, R/W
84h–87h (Consumer Only)	MSIMA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
88h–89h (Consumer Only)	MSIMD	Message Signaled Interrupt Message Data	0000h	R/W
90h	MAP	Address Map	00h	R/W
92h–93h	PCS	Port Control and Status	0000h	R/W, RO, R/WC
A8h–ABh	SCAP0	SATA Capability Register 0	0010B012h	RO
ACh–AFh	SCAP1	SATA Capability Register 1	00000048h	RO
B0h–B1h	FLRCID	FLR Capability ID	0009h	RO
B2h–B3h	FLRCLV	FLR Capability Length and Value	2006h	RO
B4h–B5h	FLRCTRL	FLR Control	0000h	R/W, RO
C0h	ATC	APM Trapping Control	00h	R/W
C4h	ATS	ATM Trapping Status	00h	R/WC

NOTE: The ICH10 SATA controller is not arbitrated as a PCI device, therefore it does not need a master latency timer.

15.1.1 VID—Vendor Identification Register (SATA—D31:F5)

Offset Address: 00h–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

15.1.2 DID—Device Identification Register (SATA—D31:F5)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 SATA controller. **NOTE:** The value of this field will change dependent upon the value of the MAP Register. See Section 15.1.29

15.1.3 PCICMD—PCI Command Register (SATA–D31:F5)

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	Fast Back to Back Enable (FBE) — RO. Reserved as 0.
8	SERR# Enable (SERR_EN) — RO. Reserved as 0.
7	Wait Cycle Control (WCC) — RO. Reserved as 0.
6	**Parity Error Response (PER)** — R/W. 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS) — RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE) — RO. Reserved as 0.
3	Special Cycle Enable (SCE) — RO. Reserved as 0.
2	**Bus Master Enable (BME)** — R/W. This bit controls the ICH10's ability to act as a PCI master for IDE Bus Master transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE)** — RO. This controller does not support AHCI, therefore no memory space is required.
0	**I/O Space Enable (IOSE)** — R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set.

15.1.4 PCISTS — PCI Status Register (SATA–D31:F5)

Address Offset: 06h–07h
Default Value: 02B0h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	**Signaled System Error (SSE)** — RO. Reserved as 0.
13	**Received Master Abort (RMA)** — R/WC. 0 = Master abort Not generated. 1 = SATA controller, as a master, generated a master abort.
12	Reserved
11	**Signaled Target Abort (STA)** — RO. Reserved as 0.
10:9	**DEVSEL# Timing Status (DEV_STS)** — RO. 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	**Data Parity Error Detected (DPED)** — R/WC. For ICH10, this bit can only be set on read completions received from SiBUS where there is a parity error. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7	**Fast Back to Back Capable (FB2BC)** — RO. Reserved as 1.
6	**User Definable Features (UDF)** — RO. Reserved as 0.
5	**66MHz Capable (66MHZ_CAP)** — RO. Reserved as 1.
4	**Capabilities List (CAP_LIST)** — RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	**Interrupt Status (INTS)** — RO. Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

15.1.5 RID—Revision Identification Register (SATA—D31:F5)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

15.1.6 PI—Programming Interface Register (SATA–D31:F5)

Address Offset: 09h
Default Value: 85h
Attribute: RO
Size: 8 bits

When SCC = 01h

Bit	Description
7	This read-only bit is a 1 to indicate that the ICH10 supports bus master operation
6:4	Reserved.
3	**Secondary Mode Native Capable (SNC)** — RO. Indicates whether or not the secondary channel has a fixed mode of operation. 0 = Indicates the mode is fixed and is determined by the (read-only) value of bit 2. This bit will always return '0'.
2	**Secondary Mode Native Enable (SNE)** — RO. Determines the mode that the secondary channel is operating in. 1 = Secondary controller operating in native PCI mode. This bit will always return '1'.
1	**Primary Mode Native Capable (PNC)** — RO. Indicates whether or not the primary channel has a fixed mode of operation. 0 = Indicates the mode is fixed and is determined by the (read-only) value of bit 0. This bit will always return '0'.
0	**Primary Mode Native Enable (PNE)** — RO. Determines the mode that the primary channel is operating in. 1 = Primary controller operating in native PCI mode. This bit will always return '1'.

15.1.7 SCC—Sub Class Code Register (SATA–D31:F5)

Address Offset: 0Ah
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** — RO. The value of this field determines whether the controller supports legacy IDE mode.

15.1.8 BCC—Base Class Code Register (SATA–D31:F5)

Address Offset: 0Bh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. 01h = Mass storage device

15.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F5)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)** — RO. 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

15.1.10 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F5)

Address Offset: 10h–13h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address** — R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

15.1.11 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F5)

Address Offset: 14h–17h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address** — R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

15.1.12 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset: 18h–1Bh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address** — R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 8-byte I/O space is used in native mode for the Secondary Controller's Command Block.

15.1.13 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset: 1Ch–1Fh
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address** — R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

NOTE: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

15.1.14 BAR — Legacy Bus Master Base Address Register (SATA–D31:F5)

Address Offset:	20h–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte IO space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:5	**Base Address** — R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
4	**Base Address 4 (BA4)**— R/W. When SCC is 01h, this bit will be R/W resulting in requesting 16B of I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

15.1.15 SIDPBA — SATA Index/Data Pair Base Address Register (SATA–D31:F5)

Address Offset:	24h–27h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

When SCC is 01h

When the programming interface is IDE, the register represents an I/O BAR allocating 16B of I/O space for the I/O mapped registers defined in Section 15.3. Note that although 16B of locations are allocated, some maybe reserved.

Bit	Description
31:16	Reserved
15:4	**Base Address (BA)** — R/W. Base address of register I/O space
3:1	Reserved
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 1 to indicate a request for I/O space.

15.1.16 SVID—Subsystem Vendor Identification Register (SATA–D31:F5)

Address Offset: 2Ch–2Dh
Default Value: 0000h
Lockable: No
Function Level Reset: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — R/WO. Value is written by BIOS. No hardware action taken on this value.

15.1.17 SID—Subsystem Identification Register (SATA–D31:F5)

Address Offset: 2Eh–2Fh
Default Value: 0000h
Lockable: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem ID (SID)** — R/WO. Value is written by BIOS. No hardware action taken on this value.

15.1.18 CAP—Capabilities Pointer Register (SATA–D31:F5)

Address Offset: 34h
Default Value: 70h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** — RO. Indicates that the first capability pointer offset is 70h if the Sub Class Code (SCC) (Dev 31:F2:0Ah) is configure as IDE mode (value of 01).

15.1.19 INT_LN—Interrupt Line Register (SATA–D31:F5)

Address Offset: 3Ch
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line** — R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to. These bits are not reset by FLR.

15.1.20 INT_PN—Interrupt Pin Register (SATA–D31:F5)

Address Offset: 3Dh
Default Value: See Register Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin** — RO. This reflects the value of D31IP.SIP1 (Chipset Config Registers:Offset 3100h:bits 11:8).

15.1.21 IDE_TIM — IDE Timing Register (SATA–D31:F5)

Address Offset: Primary: 40h–41h Attribute: R/W
Secondary: 42h–43h
Default Value: 0000h Size: 16 bits

Bit	Description
15	**IDE Decode Enable (IDE)** — R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the Intel® ICH10 to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary) and Control Block (3F6h for primary and 376h for secondary). This bit effects the IDE decode ranges for both legacy and native-Mode decoding. **NOTE:** This bit affects SATA operation in both combined and non-combined ATA modes. See Section 5.16 for more on ATA modes of operation.
14:0	Reserved

15.1.22 PID—PCI Power Management Capability Identification Register (SATA–D31:F5)

Address Offset: 70h–71h Attribute: RO
Default Value: B001h Size: 16 bits

Bits	Description
15:8	**Next Capability (NEXT)** — RO. When SCC is 01h, this field will be B0h indicating the next item is FLR Capability Pointer in the list.
7:0	**Capability ID (CID)** — RO. Indicates that this pointer is a PCI power management.

15.1.23 PC—PCI Power Management Capabilities Register (SATA–D31:F5)

Address Offset: 72h–73h Attribute: RO
Default Value: 4003h Size: 16 bits

Bits	Description
15:11	**PME Support (PME_SUP)** — RO. By default with SCC = 01h, the default value of 00000 indicates no PME support in IDE mode.
10	D2 Support (D2_SUP) — RO. Hardwired to 0. The D2 state is not supported
9	D1 Support (D1_SUP) — RO. Hardwired to 0. The D1 state is not supported
8:6	Auxiliary Current (AUX_CUR) — RO. PME# from $D3_{COLD}$ state is not supported, therefore this field is 000b.
5	Device Specific Initialization (DSI) — RO. Hardwired to 0 to indicate that no device-specific initialization is required.
4	Reserved
3	PME Clock (PME_CLK) — RO. Hardwired to 0 to indicate that PCI clock is not required to generate PME#.
2:0	**Version (VER)** — RO. Hardwired to 011 to indicates support for Revision 1.2 of the PCI Power Management Specification.

15.1.24 PMCS—PCI Power Management Control and Status Register (SATA–D31:F5)

Address Offset:	74h–75h	Attribute:	RO, R/W, R/WC
Default Value:	0008h	Size:	16 bits
Function Level Reset:	No (Bits 8 and 15 only)		

Bits	Description
15	**PME Status (PMES)** — R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller. Note: When SCC=01h this bit will be RO '0'. Software is advised to clear PMEE together with PMES prior to changing SCC through MAP.SMS. This bit is not reset by Function Level Reset.
14:9	Reserved
8	**PME Enable (PMEE)** — R/W. When SCC is not 01h, this bit R/W. When set, the SATA controller generates PME# form $D3_{HOT}$ on a wake event. Note: When SCC=01h this bit will be RO '0'. Software is advised to clear PMEE together with PMES prior to changing SCC through MAP.SMS. This bit is not reset by Function Level Reset.
7:4	Reserved
3	**No Soft Reset (NSFRST)** — RO. These bits are used to indicate whether devices transitioning from $D3_{HOT}$ state to D0 state will perform an internal reset. 0 = Device transitioning from $D3_{HOT}$ state to D0 state perform an internal reset. 1 = Device transitioning from $D3_{HOT}$ state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the $D3_{HOT}$ state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from $D3_{HOT}$ state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	Reserved
1:0	**Power State (PS)** — R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

15.1.25 MID—Message Signal Interrupt Identifier (SATA–D31:F5) (Consumer Only)

Address Offset:	80h-81h	Attribute:	RO
Default Value:	7005h	Size:	16 bits

Bits	Description
15:8	**Next Pointer (NEXT)**— RO. Indicates the next item in the list is the PCI Power Management Pointer.
7:0	**Capability ID (CID)**— RO. Capability ID indicates Message Signal Interrupt.

15.1.26 MC—Message Signal Interrupt Message Control (SATA–D31:F5) (Consumer Only)

Address Offset: 82h-83h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bits	Description
15:8	Reserved.
7	**64 Bit Address Capable (C64)**— RO. Capable of generating a 32-bit message only.
6:4	**Multiple Message Enable (MME)**— RO. This controller supports a single interrupt message. This bit is RO '0'.
3:1	**Multiple Message Capable (MMC)**— RO. System software reads this field to determine the number of requested vectors. This controller supports a single interrupt message, this field is RO '0'.
0	**MSI Enable (MSIE)** — R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note: CMD.ID bit does not effect MSI. Software must clear this bit to 0 to disable MSI before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to '0' when operating in legacy IDE mode. This bit is R/W when SCC is not 01h and is RO '0' when SCC is 01h.

15.1.27 MA—Message Signal Interrupt Message Address (SATA–D31:F5) (Consumer Only)

Address Offset: 84h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bits	Description
31:2	**Address (ADDR)**— R/W. Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	Reserved.

15.1.28 MD—Message Signal Interrupt Message Data (SATA–D31:F5) (Consumer Only)

Address Offset: 88h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bits	Description
15:0	**Data (DATA)**— R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction. Note: When MC.MME field is set to a value other than '000', some bits of the MSI memory write transaction will be driven based on the source of the interrupt rather than from MD[2:0].

15.1.29 MAP—Address Map Register (SATA–D31:F5)16

Address Offset:	90h	Attribute:	R/W, R/WO, RO
Default Value:	00h	Size:	bits
Function Level Reset:	No (Bits 9:8 only)		

Bits	Description
15:10	Reserved.
9:8	Reserved
7:6	**SATA Mode Select (SMS)** — R/W. Software programs these bits to control the mode in which the SATA Controller should operate. 00b = IDE Mode All other combinations are reserved.
5:2	Reserved.
1:0	**Map Value (MV)**— Reserved.

15.1.30 PCS—Port Control and Status Register (SATA–D31:F5)

Address Offset: 92h–93h
Default Value: 0000h
Function Level Reset: No
Attribute: R/W, RO
Size: 16 bits

By default, the SATA ports are set to the disabled state (bits [5:0] = '0'). When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the "off" state and cannot detect any devices.

If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL and PxCMD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to 1 prior to booting the OS, regardless as to whether or not a device is currently on the port.

Bits	Description
15:10	Reserved
9	**Port 5 Present (P5P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P1E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected.
8	**Port 4 Present (P4P)** — RO. The status of this bit may change at any time. This bit is cleared when the port is disabled via P0E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected.
7:2	Reserved
1	**Port 5 Enabled (P5E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. This bit is read-only '0' when MAP.SPD[1]= 1.
0	**Port 4 Enabled (P4E)** — R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. This bit is read-only '0' when MAP.SPD[0]= 1.

15.1.31 SATACR0— SATA Capability Register 0 (SATA–D31:F5)

Address Offset:	A8h-ABh	Attribute:	RO, RWO
Default Value:	0010B012h	Size:	32 bits
Function Level Reset:	No (Bits 15:8 only)		

Note: When SCC is 01h this register is read-only 0.

Bit	Description
31:24	Reserved.
23:20	**Major Revision (MAJREV)** — RO. Major revision number of the SATA Capability Pointer implemented.
19:16	**Minor Revision (MINREV)** — RO. Minor revision number of the SATA Capability Pointer implemented.
15:8	**Next Capability Pointer (NEXT)** — RWO. Points to the next capability structure.
7:0	**Capability ID (CAP)** — RO. The value of 12h has been assigned by the PCI SIG to designate the SATA capability pointer.

15.1.32 SATACR1— SATA Capability Register 1 (SATA–D31:F5)

Address Offset:	ACh-AFh	Attribute:	RO
Default Value:	00000048h	Size:	32 bits

When SCC is 01h this register is read-only 0.

Bit	Description
31:16	Reserved.
15:4	**BAR Offset (BAROFST)** — RO. Indicates the offset into the BAR where the index/Data pair are located (in DWord granularity). The index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR (BAR4). A value of 004h indicates offset 10h.
3:0	**BAR Location (BARLOC)** — RO. Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR (BAR4) in the SATA controller. a value of 8h indicates and offset of 20h, which is LBAR (BAR4).

15.1.33 FLRCID— FLR Capability ID (SATA–D31:F5)

Address Offset:	B0h-B1h	Attribute:	RO
Default Value:	0009h	Size:	16 bits

Bit	Description
15:8	**Next Capability Pointer** — RO. A value of 00h indicates the final item in the Capability List.
7:0	**Capability ID** — RO. The value of this field depends on the FLRCSSECL bit. If FLRCSSEL = 0, this field is 13h If FLRCSSEL = 1, this field is 09h, indicating vendor specific capability.

15.1.34 FLRCLV— FLR Capability Length and Value (SATA–D31:F5)

Address Offset:	B2h-B3h	Attribute:	RO, RWO
Default Value:	2006h	Size:	16 bits
Function Level Reset:	No (Bits 9:8 only)		

When FLRCSSEL = ‘0’, this register is defined as follows.

Bit	Description
15:10	Reserved.
9	**FLR Capability** — RWO. This field indicates support for Function Level Reset.
8	**TXP Capability** — RWO. This field indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length** — RO. This field indicates the number of bytes of the Vendor Specific capability as required by the PCI spec. It has the value of 06h for FLR Capability.

When FLRCSSEL = ‘1’ , this register is defined as follows.

Bit	Description
15:12	**Vendor Specific Capability ID** — RO. A value of 02h identifies this capability as a Function Level Reset.
11:8	**Capability Version** — RO. This field indicates the version of the FLR capability.
7:0	**Capability Length** — RO. This field indicates the number of bytes of the Vendor Specific capability as required by the PCI spec. It has the value of 06h for FLR Capability.

15.1.35 FLRCTRL— FLR Control (SATA–D31:F5)

Address Offset:	B4h-B5h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)** — RO. 0 = Completions for all Non-Posted requests have been received by the controller. 1 = Controller has issued Non-Posted request which has not been completed.
7:1	Reserved.
0	**Initiate FLR** — R/W. Used to initiate FLR transition. A write of ‘1’ indicates FLR transition.

15.1.36 ATC—APM Trapping Control Register (SATA–D31:F5)

Address Offset:	C0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This SATA controller does not support legacy I/O access. Therefore, this register is reserved. Software shall not change the default values of the register; otherwise the result will be undefined.

Bit	Description
7:0	Reserved

15.1.37 ATC—APM Trapping Control (SATA–D31:F5)

Address Offset:	C4h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This SATA controller does not support legacy I/O access. Therefore, this register is reserved. Software shall not change the default values of the register; otherwise the result will be undefined.

Bit	Description
7:0	Reserved

15.2 Bus Master IDE I/O Registers (D31:F5)

The bus master IDE function uses 16 bytes of I/O space, allocated via the BAR register, located in Device 31:Function 2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or dword quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. The description of the I/O registers is shown in Table 15-2.

Table 15-2. Bus Master IDE I/O Register Address Map

BAR+ Offset	Mnemonic	Register	Default	Type
00	BMICP	Command Register Primary	00h	R/W
01	—	Reserved	—	RO
02	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03	—	Reserved	—	RO
04–07	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08	BMICS	Command Register Secondary	00h	R/W
09	—	Reserved	—	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	—	Reserved	—	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xxxxxxxxh	R/W

15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5)

Address Offset:	Primary: BAR + 00h Secondary: BAR + 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved.
3	**Read / Write Control (R/WC)** — R/W. This bit sets the direction of the bus master transfer: This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved.
0	**Start/Stop Bus Master (START)** — R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit (D31:F5:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F1:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. **NOTE:** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the ICH10 will not send DMAT to terminate the data transfer. SW intervention (e.g. sending SRST) is required to reset the interface in this condition.

15.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F5)

Address Offset: Primary: BAR + 02h
Secondary: BAR + 0Ah
Attribute: R/W, R/WC, RO
Default Value: 00h
Size: 8 bits

Bit	Description
7	**PRD Interrupt Status (PRDIS)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the host controller execution of a PRD that has its PRD_INT bit set.
6	Reserved.
5	**Drive 0 DMA Capable** — R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The ICH10 does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved.
2	**Interrupt** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts via the IEN bit of the Device Control Register (see chapter 5 of the *Serial ATA Specification*, Revision 1.0a).
1	**Error** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)** — RO. 0 = This bit is cleared by the ICH10 when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the ICH10 when the Start Bus Master bit (D31:F5:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the ICH10 when the Start bit is written to the Command register.

15.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F5)

Address Offset: Primary: BAR + 04h–07h
Secondary: BAR + 0Ch–0Fh
Attribute: R/W
Default Value: All bits undefined
Size: 32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)** — R/W. The bits in this field correspond to bits [31:2] of the memory location of the Physical Region Descriptor (PRD). The Descriptor Table must be dword-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

15.3 Serial ATA Index/Data Pair Superset Registers

All of these I/O registers are in the core well. They are exposed only when SCC is 01h (i.e. IDE programming interface) and the controller is not in combined mode. These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software-write operations to the reserved locations shall have no effect while software-read operations to the reserved locations shall return 0.

15.3.1 SINDX—SATA Index Register (D31:F5)

Address Offset:	SIDPBA + 00h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: These are Index/Data Pair Registers that are used to access the SSTS, SCTL, and SERR. The I/O space for these registers is allocated through SIDPBA.

Bit	Description
31:16	Reserved
15:8	**Port Index (PIDX)**— R/W**:** This Index field is used to specify the port of the SATA controller at which the port-specific SSTS, SCTL, and SERR registers are located. 00h = Primary Master (Port 4) 02h = Secondary Master (Port 5) All other values are Reserved.
7:0	**Register Index (RIDX)**— R/W**:** This Index field is used to specify one out of three registers currently being indexed into. 00h = SSTS 01h = SCTL 02h = SERR All other values are Reserved

15.3.2 SDATA—SATA Index Data Register (D31:F5)

Address Offset:	SIDPBA + 04h	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Note: These are Index/Data Pair Registers that are used to access the SSTS, SCTL, and SERR. The I/O space for these registers is allocated through SIDPBA.

Bit	Description
31:0	**Data (DATA)**— R/W**:** This Data register is a “window” through which data is read or written to the memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be setup prior to the read or write to this Data register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by Index.

15.3.2.1 PxSSTS—Serial ATA Status Register (D31:F5)

Address Offset: Attribute: RO
Default Value: 00000000h Size: 32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The ICH10 updates it continuously and asynchronously. When the ICH10 transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)** — RO. Indicates the current interface state: **Value** **Description** 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)** — RO. Indicates the negotiated interface communication speed. **Value** **Description** 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated All other values reserved. ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)** — RO. Indicates the interface device detection and Phy state: **Value** **Description** 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

15.3.2.2 PxSCTL — Serial ATA Control Register (D31:F5)

Address Offset: Attribute: R/W, RO
Default Value: 00000004h Size: 32 bits

SDATA when SINDX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the ICH10 or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	Port Multiplier Port (PMP) — RO. This field is not used by AHCI.
15:12	Select Power Management (SPM) — RO. This field is not used by AHCI.
11:8	**Interface Power Management Transitions Allowed (IPM)** — R/W. Indicates which power states the ICH10 is allowed to transition to: **Value** **Description** 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)** — R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** **Description** 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to Generation 2 communication rate All other values reserved. ICH10 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection Initialization (DET)** — R/W. Controls the ICH10's device detection and interface initialization. **Value** **Description** 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the ICH10 initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the ICH10 is running results in undefined behavior.

15.3.2.3 PxSERR—Serial ATA Error Register (D31:F5)

Address Offset: Attribute: R/WC
Default Value: 00000000h Size: 32 bits

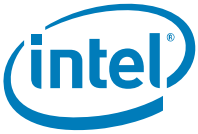
SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)** — R/WC. When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)** — R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)** — R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Transport state transition error (T)** — R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
22	**Handshake (H)** — R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)** — R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)** — R/WC. This field is not used by AHCI.
19	**10b to 8b Decode Error (B)** — R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)** — R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)** — R/WC. Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)** — R/WC. When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the ICH10, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)** — R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)** — R/WC. A violation of the Serial ATA protocol was detected. Note: The ICH10 does not set this bit for all protocol violations that may occur on the SATA link.

Bit	Description
9	**Persistent Communication or Data Integrity Error (C)** — R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)** — R/WC. A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)** — R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)** — R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

§ §



16 UHCI Controllers Registers

16.1 PCI Configuration Registers (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Note: The USB functions may be hidden based on the value of the corresponding bits in the Function Disable Register (see Chipset Configuration Registers). UHCIs must be disabled from highest number to lowest within their specific PCI device.

Table 16-1. UHCI Controller PCI Configuration Map

UHCI	PCI Device:Function	Notes
UHCI #1	D29:F0	
UHCI #2	D29:F1	
UHCI #3	D29:F2	
UHCI #4	D26:F0	
UHCI #5	D26:F1	
UHCI #6	D26:F2 or D29:F3	D26:F2 can be configured as D29:F3 during BIOS post.

Note: Register address locations that are not shown in Table 16-2 should be treated as Reserved (see Section 9.2 for details).

Table 16-2. UHCI Controller PCI Register Address Map (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Offset	Mnemonic	Register Name	UHCI #1-6 Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See register description	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0290h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	See register description	RO
20–23h	BASE	Base Address	00000001h	R/W, RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	R/WO

Table 16-2. UHCI Controller PCI Register Address Map (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Offset	Mnemonic	Register Name	UHCI #1-6 Default	Type
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50h	FLRCID	FLR Capability ID	09h	RO
51h	FLRNCP	FLR Next Capability Pointer	00h	RO
52–53h	FLRCLV	FLR Capability Length and Version	2006h	RO
54h	FLRCTRL	FLR Control	00h	R/W
55h	FLRSTAT	FLR Status	00h	RO
60h	USB_RELNUM	Serial Bus Release Number	10h	RO
C0–C1h	USB_LEGKEY	USB Legacy Keyboard/Mouse Control	2000h	R/W, RO R/WC
C4h	USB_RES	USB Resume Enable	00h	R/W
C8h	CWP	Core Well Policy	00h	R/W
CAh	UCR1	UHCI Configuration Register 1	01h	R/W

NOTE: Refer to the *Intel® I/O Controller Hub 10 (ICH10) Family Specification Update* for the value of the Revision ID Register.

16.1.1 VID—Vendor Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Vendor ID — RO. This is a 16-bit value assigned to Intel

16.1.2 DID—Device Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 02h–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	Device ID — RO. This is a 16-bit value assigned to the Intel® ICH10 USB universal host controllers. Refer to the *Intel® I/O Controller Hub (ICH10) Family* for the value of the Device ID Register.

16.1.3 PCICMD—PCI Command Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. The corresponding Interrupt Status bit is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0.
8	SERR# Enable — RO. Reserved as 0.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0.
6	Parity Error Response (PER) — RO. Hardwired to 0.
5	VGA Palette Snoop (VPS) — RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) — RO. Hardwired to 0.
3	Special Cycle Enable (SCE) — RO. Hardwired to 0.
2	**Bus Master Enable (BME)** — R/W. 0 = Disable 1 = Enable. ICH10 can act as a master on the PCI bus for USB transfers.
1	Memory Space Enable (MSE) — RO. Hardwired to 0.
0	**I/O Space Enable (IOSE)** — R/W. This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.

16.1.4 PCISTS—PCI Status Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 06h–07h
Default Value: 0290h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected. 1 = Set when a data parity error data parity error is detected on writes to the UHCI register space or on read completions returned to the host controller.
14	Reserved.
13	**Received Master Abort (RMA)** — R/WC. 0 = No master abort generated by USB. 1 = USB, as a master, generated a master abort.
12	Reserved.
11	**Signaled Target Abort (STA)** — R/WC. 0 = ICH10 did Not terminate transaction for USB function with a target abort. 1 = USB function is targeted with a transaction that the ICH10 terminates with a target abort.
10:9	**DEVSEL# Timing Status (DEV_STS)** — RO. This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the ICH10's DEVSEL# timing when performing a positive decode. ICH10 generates DEVSEL# with medium timing for USB.
8	Data Parity Error Detected (DPED) — RO. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) — RO. Hardwired to 1.
6	User Definable Features (UDF) — RO. Hardwired to 0.
5	66 MHz Capable — RO. Hardwired to 0.
4	Capabilities List — RO. Hardwired to 1. Indicates that offset 34h contains a valid capabilities pointer.
3	**Interrupt Status** — RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

16.1.5 RID—Revision Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Revision ID — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

16.1.6 PI—Programming Interface Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	Programming Interface — RO. 00h = No specific register level programming interface defined.

16.1.7 SCC—Sub Class Code Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset:	0Ah	Attribute:	RO
Default Value:	03h	Size:	8 bits

Bit	Description
7:0	Sub Class Code (SCC) — RO. 03h = USB host controller.

16.1.8 BCC—Base Class Code Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset:	0Bh	Attribute:	RO
Default Value:	0Ch	Size:	8 bits

Bit	Description
7:0	Base Class Code (BCC) — RO. 0Ch = Serial Bus controller.

16.1.9 MLT—Master Latency Timer Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset:	0Dh	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	Master Latency Timer (MLT) — RO. The USB controller is implemented internal to the ICH10 and not arbitrated as a PCI device. Therefore the device does not require a Master Latency Timer.

16.1.10 HEADTYP—Header Type Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 0Eh
Default Value: See Bit Description
Attribute: RO
Size: 8 bits

For UHCI #2, 3, 5 and 6 this register is hardwired to 00h. For UHCI #1 and UHCI #4, bit 7 is determined by the values in the USB Function Disable bits (11:8 of the Function Disable register Chipset Config Registers:Offset 3418h).

Bit	Description
7	**Multi-Function Device** — RO. Since the upper functions in this device can be individually hidden, this bit is based on the function-disable bits in Chipset Config Space: Offset 3418h as follows: 0 = Single-function device. (Default for UHCI #2, 3, 5 and 6) 1 = Multi-function device. (Default for UHCI #1 and 4)
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

16.1.11 BASE—Base Address Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 20h–23h
Default Value: 00000001h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:16	Reserved
15:5	**Base Address** — R/W. Bits [15:5] correspond to I/O address signals AD [15:5], respectively. This gives 32 bytes of relocatable I/O space.
4:1	Reserved
0	Resource Type Indicator (RTE) — RO. Hardwired to 1 to indicate that the base address field in this register maps to I/O space.

16.1.12 SVID — Subsystem Vendor Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 2Ch–2Dh
Default Value: 0000h
Lockable: No
Function Level Reset: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — R/WO. BIOS sets the value in this register to identify the Subsystem Vendor ID. The USB_SVID register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **NOTE:** The software can write to this register only once per core well reset. Writes should be done as a single, 16-bit cycle.

16.1.13 SID — Subsystem Identification Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 2Eh–2Fh
Default Value: 0000h
Lockable: No
Function Level Reset: No
Attribute: R/WO
Size: 16 bits
Power Well: Core

Bit	Description
15:0	**Subsystem ID (SID)** — R/WO. BIOS sets the value in this register to identify the Subsystem ID. The SID register, in combination with the SVID register (D29:F0/F1/F2/F3, D26:F0/F1/F2:2C), enables the operating system to distinguish each subsystem from other(s). The value read in this register is the same as what was written to the IDE_SID register. **NOTE:** The software can write to this register only once per core well reset. Writes should be done as a single, 16-bit cycle.

16.1.14 CAP_PTR—Capabilities Pointer (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 34h
Default Value: 50h
Function Level Reset: No
Attribute: R/WO
Size: 8 bits

Bit	Description
7:0	**Capability Pointer (CAP_PTR)** — R/WO. This register points to the next capability in the Function Level Reset capability structure.

16.1.15 INT_LN—Interrupt Line Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 3Ch
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — RO. This data is not used by the ICH10. It is to communicate to software the interrupt line that the interrupt pin is connected to.

16.1.16 INT_PN—Interrupt Pin Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 3Dh
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — RO. This value tells the software which interrupt pin each USB host controller uses. The upper 4 bits are hardwired to 0000b; the lower 4 bits are determine by the Interrupt Pin default values that are programmed in the memory-mapped configuration space as follows: UHCI #1 - D29IP.U0P (Chipset Config Registers:Offset 3108:bits 3:0) UHCI #2 - D29IP.U1P (Chipset Config Registers:Offset 3108:bits 7:4) UHCI #3 - D29IP.U2P (Chipset Config Registers:Offset 3108:bits 11:8) UHCI #4 - D26IP.U0P (Chipset Config Registers:Offset 3114:bits 3:0) UHCI #5 - D26IP.U1P (Chipset Config Registers:Offset 3114:bits 7:4) UHCI #6 - D26IP.U2P (Chipset Config Registers:Offset 3114:bits 11:8) or UHCI #6 - D29IP.U3P (Chipset Config Registers:Offset 3108:bits 15:12) **NOTE:** This does not determine the mapping to the PIRQ pins.

16.1.17 FLRCID—Function Level Reset Capability ID (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 50h
Default Value: 09h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID** — RO. 13h = If FLRCSSEL = 0 09h (Vendor Specific Capability) = If FLRCSSEL = 1

16.1.18 FLRNCP—Function Level Reset Next Capability Pointer (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 51h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	A value of 00h indicates that this is the last capability field.

16.1.19 FLRCLV—Function Level Reset Capability Length and Version (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 52h-53h
Default Value: 2006h
Attribute: RO, R/WO
Size: 16 bits

When FLRCSSEL = 0, this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**FLR Capability** — R/WO. 1 = Support for Function Level Reset (FLR).
8	**TXP Capability** — R/WO. 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length** — RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It ha‘s the value of 06h for the FLR Capability.

When FLRCSSEL = 1, this register is defined as follows:

Bit	Description
15:12	**Vendor Specific Capability ID** — RO. A value of 02h in this field identifies this capability a‘s Function Level Reset.
11:8	**Capability Version** — RO. This field indicates the version of the FLR capability.
7:0	**Capability Length** — RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It ha‘s the value of 06h for the FLR Capability.

16.1.20 USB_FLRCTRL—FLR Control Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 54h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**Initiate FLR**— R/W. Used to initiate FLR transition. a write of ‘1’ initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the value read by software from this bit i always ‘0’.

16.1.21 USB_FLRSTAT—FLR Status Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 55h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**Transaction Pending (TXP)**— RO. 0 = Indicates completions for all Non-Posted requests have been received. 1 = Indicates the controller has issued Non-Posted request which have not been completed.

16.1.22 USB_RELNUM—Serial Bus Release Number Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: 60h
Default Value: 10h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Serial Bus Release Number** — RO. 10h = USB controller supports the *USB Specification*, Release 1.0.

16.1.23 USB_LEGKEY—USB Legacy Keyboard/Mouse Control Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: C0h–C1h
Default Value: 2000h
Attribute: R/W, R/WC, RO
Size: 16 bits
Function Level Reset: No

This register is implemented separately in each of the USB UHCI functions. However, the enable and status bits for the trapping logic are OR'd and shared, respectively, since their functionality is not specific to any one host controller.

Bit	Description
15	**SMI Caused by End of Pass-Through (SMIBYENDPS)** — R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred
14	Reserved
13	**PCI Interrupt Enable (USBPIRQEN)** — R/W. This bit is used to prevent the USB controller from generating an interrupt due to transactions on its ports. Note that, when disabled, it will probably be configured to generate an SMI using bit 4 of this register. Default to 1 for compatibility with older USB software. 0 = Disable 1 = Enable

Bit	Description
12	**SMI Caused by USB Interrupt (SMIBYUSB)** — RO. This bit indicates if an interrupt event occurred from this controller. The interrupt from the controller is taken before the enable in bit 13 has any effect to create this read-only bit. Note that even if the corresponding enable bit is not set in Bit 4, this bit may still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software should clear the interrupts via the USB controllers. Writing a 1 to this bit will have no effect. 1 = Event Occurred.
11	**SMI Caused by Port 64 Write (TRAPBY64W)** — R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 3, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
10	**SMI Caused by Port 64 Read (TRAPBY64R)** — R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 2, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
9	**SMI Caused by Port 60 Write (TRAPBY60W)** — R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 1, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
8	**SMI Caused by Port 60 Read (TRAPBY60R)** — R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
7	**SMI at End of Pass-Through Enable (SMIATENDPS)** — R/W. This bit enables SMI at the end of a pass-through. This can occur if an SMI is generated in the middle of a pass-through, and needs to be serviced later. 0 = Disable 1 = Enable
6	**Pass Through State (PSTATE)** — RO. 0 = If software needs to reset this bit, it should set bit 5 in all of the host controllers to 0. 1 = Indicates that the state machine is in the middle of an A20GATE pass-through sequence.
5	**A20Gate Pass-Through Enable (A20PASSEN)** — R/W. 0 = Disable. 1 = Enable. Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the SMI status bits.
4	**SMI on USB IRQ Enable (USBSMIEN)** — R/W. 0 = Disable 1 = Enable. USB interrupt will cause an SMI event.

Bit	Description
3	**SMI on Port 64 Writes Enable (64WEN)** — R/W. 0 = Disable 1 = Enable. A 1 in bit 11 will cause an SMI event.
2	**SMI on Port 64 Reads Enable (64REN)** — R/W. 0 = Disable 1 = Enable. A 1 in bit 10 will cause an SMI event.
1	**SMI on Port 60 Writes Enable (60WEN)** — R/W. 0 = Disable 1 = Enable. A 1 in bit 9 will cause an SMI event.
0	**SMI on Port 60 Reads Enable (60REN)** — R/W. 0 = Disable 1 = Enable. A 1 in bit 8 will cause an SMI event.

16.1.24 USB_RES—USB Resume Enable Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: C4h
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:2	Reserved
1	**PORT1EN** — R/W. Enable port 1 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/ disconnect events.
0	**PORT0EN** — R/W. Enable port 0 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/ disconnect events.

16.1.25 CWP—Core Well Policy Register (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: C8h
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:3	Reserved
2	**Host Controller Alignment Enable** (HCAE) — R/W. Setting this bit aligns the host controller's start of the first frame to a central 1ms heartbeat. Setting this bit for each controller maintains alignment.
1	**HCHALTED Bit Read Mode** (HBM) — R/W. This bit controls what SW sees on reads of the HCHALTED bit in the interval between when SW has set the RUN bit and the first heartbeat. 0 = Software reads the delayed value of HCHALTED (sees a 1 while the controller is waiting for the heartbeat). 1 = Software reads the value it would expect to see without the delay (sees a 0 even while the controller is waiting for the heartbeat).
0	**Static Bus Master Status Policy Enable** (SBMSPE) — R/W. 0 = The UHCI host controller dynamically sets the Bus Master status bit (Power Management 1 Status Register,[PMBASE+00h], bit 4) based on the memory accesses that are scheduled. The default setting provides a more accurate indication of snoopable memory accesses in order to help with software-invoked entry to C3 and C4 power states 1 = The UHCI host controller statically forces the Bus Master Status bit in power management space to 1 whenever the HCHalted bit (USB Status Register, Base+02h, bit 5) is cleared. **NOTE:** The PCI Power Management registers are enabled in the PCI Device 31: Function 0 space (PM_IO_EN), and can be moved to any I/O location (128-byte aligned).

16.1.26 UCR1—UCHI Configuration Register 1 (USB—D29:F0/F1/F2/F3, D26:F0/F1/F2)

Address Offset: CAh
Default Value: 01h
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Initiator/Target Arbitration Disable (ITAD)** — R/W. When this bit is set to 1, the UHCI controller will force DMA read requests to return prior to completing transactions as a target. When this bit is set to 0, the UHCI controller will allow completions from target transactions to complete independent of the state of forward progress of the master.

16.2 USB I/O Registers

Some of the read/write register bits that deal with changing the state of the USB hub ports function such that on read back they reflect the current state of the port, and not necessarily the state of the last write to the register. This allows the software to poll the state of the port and wait until it is in the proper state before proceeding. A host controller reset, global reset, or port reset will immediately terminate a transfer on the affected ports and disable the port. This affects the USBCMD register, bit 4 and the PORTSC registers, bits [12,6,2]. See individual bit descriptions for more detail.

Table 16-3. USB I/O Registers

BASE + Offset	Mnemonic	Register Name	Default	Type
00–01h	USBCMD	USB Command	0000h	R/W
02–03h	USBSTS	USB Status	0020h	R/WC
04–05h	USBINTR	USB Interrupt Enable	0000h	R/W
06–07h	FRNUM	Frame Number	0000h	R/W (see Note 1)
08–0Bh	FRBASEADD	Frame List Base Address	Undefined	R/W
0Ch	SOFMOD	Start of Frame Modify	40h	R/W
0D–0Fh	—	Reserved	—	—
10–11h	PORTSC0	Port 0 Status/Control	0080h	R/WC, RO, R/W (see Note 1)
12–13h	PORTSC1	Port 1 Status/Control	0080h	R/WC, RO, R/W (see Note 1)

NOTE:
1. These registers are WORD writable only. Byte writes to these registers have unpredictable effects.

16.2.1 USBCMD—USB Command Register

I/O Offset:	Base + (00h–01h)	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed. The table following the bit description provides additional information on the operation of the Run/Stop and Debug bits.

Bit	Description
15:7	Reserved
8	**Loop Back Test Mode** — R/W. 0 = Disable loop back test mode. 1 = ICH10 is in loop back test mode. When both ports are connected together, a write to one port will be seen on the other port and the data will be stored in I/O offset 18h.
7	**Max Packet (MAXP)** — R/W. This bit selects the maximum packet size that can be used for full speed bandwidth reclamation at the end of a frame. This value is used by the host controller to determine whether it should initiate another transaction based on the time remaining in the SOF counter. Use of reclamation packets larger than the programmed size will cause a Babble error if executed during the critical window at frame end. The Babble error results in the offending endpoint being stalled. Software is responsible for ensuring that any packet which could be executed under bandwidth reclamation be within this size limit. 0 = 32 bytes 1 = 64 bytes
6	**Configure Flag (CF)** — R/W. This bit has no effect on the hardware. It is provided only as a semaphore service for software. 0 = Indicates that software has not completed host controller configuration. 1 = HCD software sets this bit as the last action in its process of configuring the host controller.
5	**Software Debug (SWDBG)** — R/W. The SWDBG bit must only be manipulated when the controller is in the stopped state. This can be determined by checking the HCHalted bit in the USBSTS register. 0 = Normal Mode. 1 = Debug mode. In SW Debug mode, the host controller clears the Run/Stop bit after the completion of each USB transaction. The next transaction is executed when software sets the Run/Stop bit back to 1.
4	**Force Global Resume (FGR)** — R/W. 0 = Software resets this bit to 0 after 20 ms has elapsed to stop sending the Global Resume signal. At that time all USB devices should be ready for bus activity. The 1 to 0 transition causes the port to send a low speed EOP signal. This bit will remain a 1 until the EOP has completed. 1 = Host controller sends the Global Resume signal on the USB, and sets this bit to 1 when a resume event (connect, disconnect, or K-state) is detected while in global suspend mode.

Bit	Description
3	**Enter Global Suspend Mode (EGSM)** — R/W. 0 = Software resets this bit to 0 to come out of Global Suspend mode. Software writes this bit to 0 at the same time that Force Global Resume (bit 4) is written to 0 or after writing bit 4 to 0. 1 = Host controller enters the Global Suspend mode. No USB transactions occur during this time. The Host controller is able to receive resume signals from USB and interrupt the system. Software must ensure that the Run/Stop bit (bit 0) is cleared prior to setting this bit.
2	**Global Reset (GRESET)** — R/W. 0 = This bit is reset by the software after a minimum of 10 ms has elapsed as specified in Chapter 7 of the USB Specification. 1 = Global Reset. The host controller sends the global reset signal on the USB and then resets all its logic, including the internal hub registers. The hub registers are reset to their power on state. Chip Hardware Reset has the same effect as Global Reset (bit 2), except that the host controller does not send the Global Reset on USB.
1	**Host Controller Reset (HCRESET)** — R/W. The effects of HCRESET on Hub registers are slightly different from Chip Hardware Reset and Global USB Reset. The HCRESET affects bits [8,3:0] of the Port Status and Control Register (PORTSC) of each port. HCRESET resets the state machines of the host controller including the Connect/Disconnect state machine (one for each port). When the Connect/Disconnect state machine is reset, the output that signals connect/disconnect are negated to 0, effectively signaling a disconnect, even if a device is attached to the port. This virtual disconnect causes the port to be disabled. This disconnect and disabling of the port causes bit 1 (connect status change) and bit 3 (port enable/disable change) of the PORTSC to get set. The disconnect also causes bit 8 of PORTSC to reset. About 64 bit times after HCRESET goes to 0, the connect and low-speed detect will take place, and bits 0 and 8 of the PORTSC will change accordingly. 0 = Reset by the host controller when the reset process is complete. 1 = Reset. When this bit is set, the host controller module resets its internal timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated.
0	**Run/Stop (RS)** — R/W. When set to 1, the ICH10 proceeds with execution of the schedule. The ICH10 continues execution as long as this bit is set. When this bit is cleared, the ICH10 completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The host controller clears this bit when the following fatal errors occur: consistency check failure, or memory access errors. 0 = Stop 1 = Run **NOTE:** This bit should only be cleared if there are no active Transaction Descriptors in the executable schedule or software will reset the host controller prior to setting this bit again.

Table 16-4. Run/Stop, Debug Bit Interaction SWDBG (Bit 5), Run/Stop (Bit 0) Operation

SWDBG (Bit 5)	Run/Stop (Bit 0)	Description
0	0	If executing a command, the host controller completes the command and then stops. The 1.0 ms frame counter is reset and command list execution resumes from start of frame using the frame list pointer selected by the current value in the FRNUM register. (While Run/Stop=0, the FRNUM register (BASE + 06h) can be reprogrammed).
0	1	Execution of the command list resumes from Start Of Frame using the frame list pointer selected by the current value in the FRNUM register. The host controller remains running until the Run/Stop bit is cleared (by software or hardware).
1	0	If executing a command, the host controller completes the command and then stops and the 1.0 ms frame counter is frozen at its current value. All status are preserved. The host controller begins execution of the command list from where it left off when the Run/Stop bit is set.
1	1	Execution of the command list resumes from where the previous execution stopped. The Run/Stop bit is set to 0 by the host controller when a TD is being fetched. This causes the host controller to stop again after the execution of the TD (single step). When the host controller has completed execution, the HC Halted bit in the Status Register is set.

When the USB host controller is in Software Debug Mode (USBCMD Register bit 5=1), the single stepping software debug operation is as follows:

To Enter Software Debug Mode:

1. HCD puts host controller in Stop state by setting the Run/Stop bit to 0.
2. HCD puts host controller in Debug Mode by setting the SWDBG bit to 1.
3. HCD sets up the correct command list and Start Of Frame value for starting point in the Frame List Single Step Loop.
4. HCD sets Run/Stop bit to 1.
5. Host controller executes next active TD, sets Run/Stop bit to 0, and stops.
6. HCD reads the USBCMD register to check if the single step execution is completed (HCHalted=1).
7. HCD checks results of TD execution. Go to step 4 to execute next TD or step 8 to end Software Debug mode.
8. HCD ends Software Debug mode by setting SWDBG bit to 0.
9. HCD sets up normal command list and Frame List table.
10. HCD sets Run/Stop bit to 1 to resume normal schedule execution.

In Software Debug mode, when the Run/Stop bit is set, the host controller starts. When a valid TD is found, the Run/Stop bit is reset. When the TD is finished, the HCHalted bit in the USBSTS register (bit 5) is set.

The SW Debug mode skips over inactive TDs and only halts after an active TD has been executed. When the last active TD in a frame has been executed, the host controller waits until the next SOF is sent and then fetches the first TD of the next frame before halting.

This HCHalted bit can also be used outside of Software Debug mode to indicate when the host controller has detected the Run/Stop bit and has completed the current transaction. Outside of the Software Debug mode, setting the Run/Stop bit to 0 always resets the SOF counter so that when the Run/Stop bit is set the host controller starts over again from the frame list location pointed to by the Frame List Index (see FRNUM Register description) rather than continuing where it stopped.

16.2.2 USBSTS—USB Status Register

I/O Offset:	Base + (02h–03h)	Attribute:	R/WC
Default Value:	0020h	Size:	16 bits

This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register.

Bit	Description
15:6	Reserved
5	**HCHalted** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (debug mode or an internal error). Default.
4	**Host Controller Process Error** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has detected a fatal error. This indicates that the host controller suffered a consistency check failure while processing a Transfer Descriptor. An example of a consistency check failure would be finding an invalid PID field while processing the packet header portion of the TD. When this error occurs, the host controller clears the Run/Stop bit in the Command register (D29:F0/F1/F2/F3, D26:F0/F1/F2:BASE + 00h, bit 0) to prevent further schedule execution. A hardware interrupt is generated to the system.
3	**Host System Error** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = A serious error occurred during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system.
2	**Resume Detect (RSM_DET)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller received a “RESUME” signal from a USB device. This is only valid if the Host controller is in a global suspend state (Command register, D29:F0/F1/F2/F3, D26:F0/F1/F2:BASE + 00h, bit 3 = 1).
1	**USB Error Interrupt** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Completion of a USB transaction resulted in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit (D29:F0/F1/F2/F3, D26:F0/F1/F2:BASE + 04h, bit 2) set, both this bit and Bit 0 are set.
0	**USB Interrupt (USBINT)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The host controller sets this bit when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. Also set when a short packet is detected (actual length field in TD is less than maximum length field in TD), and short packet detection is enabled in that TD.

16.2.3 USBINTR—USB Interrupt Enable Register

I/O Offset:	Base + (04h–05h)	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Fatal errors (host controller processor error, (D29:F0/F1/F2, D26:F0/F1:BASE + 02h, bit 4, USBSTS Register) cannot be disabled by the host controller. Interrupt sources that are disabled in this register still appear in the Status Register to allow the software to poll for events.

Bit	Description
15:5	Reserved
4	**Scratchpad (SP)** — R/W.
3	**Short Packet Interrupt Enable** — R/W. 0 = Disabled. 1 = Enabled.
2	**Interrupt on Complete Enable (IOC)** — R/W. 0 = Disabled. 1 = Enabled.
1	**Resume Interrupt Enable** — R/W. 0 = Disabled. 1 = Enabled.
0	**Timeout/CRC Interrupt Enable** — R/W. 0 = Disabled. 1 = Enabled.

16.2.4 FRNUM—Frame Number Register

I/O Offset:	Base + (06–07h)	Attribute:	R/W (Writes must be Word Writes)
Default Value:	0000h	Size:	16 bits

Bits [10:0] of this register contain the current frame number that is included in the frame SOF packet. This register reflects the count value of the internal frame number counter. Bits [9:0] are used to select a particular entry in the Frame List during scheduled execution. This register is updated at the end of each frame time.

This register must be written as a word. Byte writes are not supported. This register cannot be written unless the host controller is in the STOPPED state as indicated by the HCHalted bit (D29:F0/F1/F2/F3, D26:F0/F1/F2:BASE + 02h, bit 5). A write to this register while the Run/Stop bit is set (D29:F0/F1/F2/F3, D26:F0/F1/F2:BASE + 00h, bit 0) is ignored.

Bit	Description
15:11	Reserved
10:0	**Frame List Current Index/Frame Number** — R/W. This field provides the frame number in the SOF Frame. The value in this register increments at the end of each time frame (approximately every 1 ms). In addition, bits [9:0] are used for the Frame List current index and correspond to memory address signals [11:2].

16.2.5 FRBASEADD—Frame List Base Address Register

I/O Offset:	Base + (08h–0Bh)	Attribute:	R/W
Default Value:	Undefined	Size:	32 bits

This 32-bit register contains the beginning address of the Frame List in the system memory. HCD loads this register prior to starting the schedule execution by the host controller. When written, only the upper 20 bits are used. The lower 12 bits are written as 0s (4 KB alignment). The contents of this register are combined with the frame number counter to enable the host controller to step through the Frame List in sequence. The two least significant bits are always 00. This requires dword-alignment for all list entries. This configuration supports 1024 Frame List entries.

Bit	Description
31:12	**Base Address** — R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved

16.2.6 SOFMOD—Start of Frame Modify Register

I/O Offset:	Base + (0Ch)	Attribute:	R/W
Default Value:	40h	Size:	8 bits

This 1-byte register is used to modify the value used in the generation of SOF timing on the USB. Only the 7 least significant bits are used. When a new value is written into these 7 bits, the SOF timing of the next frame will be adjusted. This feature can be used to adjust out any offset from the clock source that generates the clock that drives the SOF counter. This register can also be used to maintain real time synchronization with the rest of the system so that all devices have the same sense of real time. Using this register, the frame length can be adjusted across the full range required by the USB specification. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. It may be reprogrammed by USB system software at any time. Its value will take effect from the beginning of the next frame. This register is reset upon a host controller reset or global reset. Software must maintain a copy of its value for reprogramming if necessary.

Bit	Description
7	Reserved
6:0	**SOF Timing Value** — R/W. Guidelines for the modification of frame time are contained in Chapter 7 of the USB Specification. The SOF cycle time (number of SOF counter clock periods to generate a SOF frame length) is equal to 11936 + value in this field. The default value is decimal 64 which gives a SOF cycle time of 12000. For a 12 MHz SOF counter clock input, this produces a 1 ms Frame period. The following table indicates what SOF Timing Value to program into this field for a certain frame period. **Frame Length (# 12 MHz Clocks) (decimal)** / **SOF Timing Value (this register) (decimal)** 11936 / 0 11937 / 1 — / — 11999 / 63 12000 / 64 12001 / 65 — / — 12062 / 126 12063 / 127

16.2.7 PORTSC[0,1]—Port Status and Control Register

I/O Offset: Port 0/2/4/6/8/10: Base + (10h–11h) Attribute: R/WC, RO,
Port 1/3/5/7/9/11: Base + (12h–13h) R/W (Word writes only)
Default Value: 0080h Size: 16 bits

Note: For UHCI #1 (D29:F0), this applies to ICH10 USB ports 0 and 1; for UHCI #2 (D29:F1), this applies to ICH10 USB ports 2 and 3; for UHCI #3 (D29:F2), this applies to ICH10 USB ports 4 and 5, for UHCI #4 (D26:F0), this applies to ICH10 USB ports 6 and 7, for UHCI #5 (D26:F1), this applies to ICH10 USB ports 8 and 9 and for UHCI #6 (D26:F2 or D29:F3), this applies to ICH10 USB ports 10 and 11.

After a power-up reset, global reset, or host controller reset, the initial conditions of a port are: no device connected, Port disabled, and the bus line status is 00 (single-ended 0).

Port Reset and Enable Sequence

When software wishes to reset a USB device it will assert the Port Reset bit in the Port Status and Control register. The minimum reset signaling time is 10 mS and is enforced by software. To complete the reset sequence, software clears the port reset bit. The Intel UHCI controller must re-detect the port connect after reset signaling is complete before the controller will allow the port enable bit to de set by software. This time is approximately 5.3 μs. Software has several possible options to meet the timing requirement and a partial list is enumerated below:

- Iterate a short wait, setting the port enable bit and reading it back to see if the enable bit is set.
- Poll the connect status bit and wait for the hardware to recognize the connect prior to enabling the port.
- Wait longer than the hardware detect time after clearing the port reset and prior to enabling the port.

Bit	Description
15:13	Reserved.
12	**Suspend** — R/W. This bit should not be written to a 1 if global suspend is active (bit 3=1 in the USBCMD register). Bit 2 and bit 12 of this register define the hub states as follows: **Bits [12,2]** — **Hub State** X,0 — Disable 0, 1 — Enable 1, 1 — Suspend When in suspend state, downstream propagation of data is blocked on this port, except for single-ended 0 resets (global reset and port reset). The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. 1 = Port in suspend state. 0 = Port not in suspend state. **NOTE:** Normally, if a transaction is in progress when this bit is set, the port will be suspended when the current transaction completes. However, in the case of a specific error condition (out transaction with babble), the ICH10 may issue a start-of-frame, and then suspend the port.
11	**Overcurrent Indicator** — R/WC. Set by hardware. 0 = Software clears this bit by writing a 1 to it. 1 = Overcurrent pin has gone from inactive to active on this port.

Bit	Description
10	**Overcurrent Active** — RO. This bit is set and cleared by hardware. 0 = Indicates that the overcurrent pin is inactive (high). 1 = Indicates that the overcurrent pin is active (low).
9	**Port Reset** — R/W. 0 = Port is not in Reset. 1 = Port is in Reset. When set, the port is disabled and sends the USB Reset signaling.
8	**Low Speed Device Attached (LS)** — RO. 0 = Full speed device is attached. 1 = Low speed device is attached to this port.
7	Reserved — RO. Always read as 1.
6	**Resume Detect (RSM_DET)** — R/W. Software sets this bit to a 1 to drive resume signaling. The host controller sets this bit to a 1 if a J-to-K transition is detected for at least 32 microseconds while the port is in the Suspend state. The ICH10 will then reflect the K-state back onto the bus as long as the bit remains a 1, and the port is still in the suspend state (bit 12,2 are '11'). Writing a 0 (from 1) causes the port to send a low speed EOP. This bit will remain a 1 until the EOP has completed. 0 = No resume (K-state) detected/driven on port. 1 = Resume detected/driven on port.
5:4	**Line Status** — RO. These bits reflect the D+ (bit 4) and D– (bit 5) signals lines' logical levels. These bits are used for fault detect and recovery as well as for USB diagnostics. This field is updated at EOF2 time (See Chapter 11 of the USB Specification).
3	**Port Enable / Disable Change** — R/WC. For the root hub, this bit gets set only when a port is disabled due to disconnect on that port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). 0 = No change. Software clears this bit by writing a 1 to the bit location. 1 = Port enabled/disabled status has changed.
2	**Port Enabled / Disabled (PORT_EN)** — R/W. Ports can be enabled by host software only. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes and that there may be a delay in disabling or enabling a port if there is a transaction currently in progress on the USB. 0 = Disable 1 = Enable
1	**Connect Status Change** — R/WC. This bit indicates that a change has occurred in the port's Current Connect Status (see bit 0). The hub device sets this bit for any changes to the port device connect status, even if system software has not cleared a connect status change. If, for example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting" an already-set bit (i.e., the bit will remain set). However, the hub transfers the change bit only once when the host controller requests a data transfer to the Status Change endpoint. System software is responsible for determining state change history in such a case. 0 = No change. Software clears this bit by writing a 1 to it. 1 = Change in Current Connect Status.
0	**Current Connect Status** — RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. 1 = Device is present on port.

§ §

17 EHCI Controller Registers (D29:F7, D26:F7)

17.1 USB EHCI Configuration Registers (USB EHCI—D29:F7, D26:F7)

Note: Register address locations that are not shown in Table 17-1 should be treated as Reserved (see Section 9.2 for details).

Table 17-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F7, D26:F7) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0290h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	20h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10h–13h	MEM_BASE	Memory Base Address	00000000h	R/W, RO
2Ch–2Dh	SVID	USB EHCI Subsystem Vendor Identification	XXXXh	R/W
2Eh–2Fh	SID	USB EHCI Subsystem Identification	XXXXh	R/W
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50h	PWR_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Item Pointer	58h	R/W
52h–53h	PWR_CAP	Power Management Capabilities	C9C2h	R/W
54h–55h	PWR_CNTL_STS	Power Management Control/ Status	0000h	R/W, R/WC, RO
58h	DEBUG_CAPID	Debug Port Capability ID	0Ah	RO
59h	NXT_PTR2	Next Item Pointer #2	98h	RO
5Ah–5Bh	DEBUG_BASE	Debug Port Base Offset	20A0h	RO
60h	USB_RELNUM	USB Release Number	20h	RO

Table 17-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F7, D26:F7) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
61h	FL_ADJ	Frame Length Adjustment	20h	R/W
62h–63h	PWAKE_CAP	Port Wake Capabilities	01FFh	R/W
64h–67h	—	Reserved	—	—
68h–6Bh	LEG_EXT_CAP	USB EHCI Legacy Support Extended Capability	00000001h	R/W, RO
6Ch–6Fh	LEG_EXT_CS	USB EHCI Legacy Extended Support Control/Status	00000000h	R/W, R/WC, RO
70h–73h	SPECIAL_SMI	Intel Specific USB 2.0 SMI	00000000h	R/W, R/WC
74h–7Fh	—	Reserved	—	—
80h	ACCESS_CNTL	Access Control	00h	R/W
84h	EHCIIR1	EHCI Initialization Register 1	01h	R/W, RWL
98h	FLR_CID	FLR Capability ID	09h	RO
99h	FLR_NEXT	FLR Next Capability Pointer	00h	RO
9Ah-9Bh	FLR_CLV	FLR Capability Length and Version	2006h	RO, R/WO
9Ch	FLR_CTRL	FLR Control	00h	R/W
9Dh	FLR_STAT	FLR Status	00h	RO
FCh	EHCIIR2	EHCI Initialization Register 2	20001706h	R/W

Note: All configuration registers in this section are in the core well and reset by a core well reset and the D3-to-D0 warm reset, except as noted.

17.1.1 VID—Vendor Identification Register (USB EHCI—D29:F7, D26:F7)

Offset Address: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel.

17.1.2 DID—Device Identification Register (USB EHCI—D29:F7, D26:F7)

Offset Address: 02h–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 USB EHCI controller. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Device ID Register.

17.1.3 PCICMD—PCI Command Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. 0 = The function is capable of generating interrupts. 1 = The function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit (D29:F7, D26:F7:06h, bit 3) is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)** — R/W 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host Controller (EHC) is capable of generating (internally) SERR# in the following cases: • When it receives a completion status other than "successful" for one of its DMA -initiated memory reads on DMI (and subsequently on its internal interface). • When it detects an address or command parity error and the Parity Error Response bit is set. • When it detects a data parity error (when the data is going into the EHC) and the Parity Error Response bit is set.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0.
6	**Parity Error Response (PER)** — R/W. 0 = The EHC is not checking for correct parity (on its internal interface). 1 = The EHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase. **NOTE:** If the EHC detects bad parity on the address or command phases when the bit is set to 1, the host controller does not take the cycle. It halts the host controller (if currently not halted) and sets the Host System Error bit in the USBSTS register. This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	VGA Palette Snoop (VPS) — RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) — RO. Hardwired to 0.
3	Special Cycle Enable (SCE) — RO. Hardwired to 0.
2	**Bus Master Enable (BME)** — R/W. 0 = Disables this functionality. 1 = Enables the ICH10 to act as a master on the PCI bus for USB transfers.
1	**Memory Space Enable (MSE)** — R/W. This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F7, D26:F7:10h) for USB 2.0 should be programmed before this bit is set.
0	I/O Space Enable (IOSE) — RO. Hardwired to 0.

17.1.4 PCISTS—PCI Status Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 06h–07h
Default Value: 0290h
Attribute: R/WC, RO
Size: 16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected. 1 = This bit is set by the ICH10 when a parity error is seen by the EHCI controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions.
14	**Signaled System Error (SSE)** — R/WC. 0 = No SERR# signaled by ICH10. 1 = This bit is set by the ICH10 when it signals SERR# (internally). The SER_EN bit (bit 8 of the Command Register) must be 1 for this bit to be set.
13	**Received Master Abort (RMA)** — R/WC. 0 = No master abort received by EHC on a memory access. 1 = This bit is set when EHC, as a master, receives a master abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit.
12	**Received Target Abort (RTA)** — R/WC. 0 = No target abort received by EHC on memory access. 1 = This bit is set when EHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit (D29:F7, D26:F7:04h, bit 8).
11	Signaled Target Abort (STA) — RO. This bit is used to indicate when the EHCI function responds to a cycle with a target abort. There is no reason for this to happen, so this bit is hardwired to 0.
10:9	DEVSEL# Timing Status (DEVT_STS) — RO. This 2-bit field defines the timing for DEVSEL# assertion.
8	**Master Data Parity Error Detected (DPED)** — R/WC. 0 = No data parity error detected on USB2.0 read completion packet. 1 = This bit is set by the ICH10 when a data parity error is detected on a USB 2.0 read completion packet on the internal interface to the EHCI host controller and bit 6 of the Command register is set to 1.
7	Fast Back to Back Capable (FB2BC) — RO. Hardwired to 1.
6	User Definable Features (UDF) — RO. Hardwired to 0.
5	66 MHz Capable (66 MHz _CAP) — RO. Hardwired to 0.
4	Capabilities List (CAP_LIST) — RO. Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	**Interrupt Status** — RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is deasserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

17.1.5 RID—Revision Identification Register (USB EHCI—D29:F7, D26:F7)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

17.1.6 PI—Programming Interface Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 09h Attribute: RO
Default Value: 20h Size: 8 bits

Bit	Description
7:0	**Programming Interface** — RO. A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.

17.1.7 SCC—Sub Class Code Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 0Ah Attribute: RO
Default Value: 03h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** — RO. 03h = Universal serial bus host controller.

17.1.8 BCC—Base Class Code Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 0Bh Attribute: RO
Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. 0Ch = Serial bus controller.

17.1.9 PMLT—Primary Master Latency Timer Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)** — RO. Hardwired to 00h. Because the EHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

17.1.10 MEM_BASE—Memory Base Address Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 10h–13h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:10	**Base Address** — R/W. Bits [31:10] correspond to memory address signals [31:10], respectively. This gives 1-KB of locatable memory space aligned to 1-KB boundaries.
9:4	Reserved
3	**Prefetchable** — RO. Hardwired to 0 indicating that this range should not be prefetched.
2:1	**Type** — RO. Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
0	**Resource Type Indicator (RTE)** — RO. Hardwired to 0 indicating that the base address field in this register maps to memory space.

17.1.11 SVID—USB EHCI Subsystem Vendor ID Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 2Ch–2Dh
Default Value: XXXXh
Reset: None
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — R/W. This register, in combination with the USB 2.0 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **NOTE:** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7, D26:F7:80h, bit 0) is set to 1.

17.1.12 SID—USB EHCI Subsystem ID Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 2Eh–2Fh
Default Value: XXXXh
Reset: None
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SID)** — R/W. BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). **NOTE:** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7, D26:F7:80h, bit 0) is set to 1.

17.1.13 CAP_PTR—Capabilities Pointer Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 34h
Default Value: 50h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** — RO. This register points to the starting offset of the USB 2.0 capabilities ranges.

17.1.14 INT_LN—Interrupt Line Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 3Ch
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — R/W. This data is not used by the Intel® ICH10. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

17.1.15 INT_PN—Interrupt Pin Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 3Dh
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin** — RO. This reflects the value of D29IP.EIP (Chipset Config Registers:Offset 3108:bits 31:28) or D26IP.EIP (Chipset Config Registers:Offset 3114:bits 31:28). **NOTE:** Bits 7:4 are always 0h

17.1.16 PWR_CAPID—PCI Power Management Capability ID Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 50h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Power Management Capability ID** — RO. A value of 01h indicates that this is a PCI Power Management capabilities field.

17.1.17 NXT_PTR1—Next Item Pointer #1 Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 51h
Default Value: 58h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer 1 Value** — R/W (special). This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit (D29:F7, D26:F7:80h, bit 0) is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Only values of 58h (Debug Port visible) and 00h (Debug Port invisible) are expected to be programmed in this register. **NOTE:** Register not reset by D3-to-D0 warm reset.

17.1.18 PWR_CAP—Power Management Capabilities Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 52h–53h
Default Value: C9C2h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	**PME Support (PME_SUP)** — R/W. This 5-bit field indicates the power states in which the function may assert PME#. The Intel® ICH10 EHC does not support the D1 or D2 states. For all other states, the ICH10 EHC is capable of generating PME#. Software should never need to modify this field.
10	D2 Support (D2_SUP) — RO. 0 = D2 State is not supported
9	D1 Support (D1_SUP) — RO. 0 = D1 State is not supported
8:6	**Auxiliary Current (AUX_CUR)** — R/W**.** The ICH10 EHC reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	**Device Specific Initialization (DSI**)— RO. The ICH10 reports 0, indicating that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PME_CLK)** — RO. The ICH10 reports 0, indicating that no PCI clock is required to generate PME#.
2:0	**Version (VER)** — RO. The ICH10 reports 010b, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

NOTES:
1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the ICH10 is used, bits 15:11 and 8:6 in this register are writable when the WRT_RDONLY bit (D29:F7, D26:F7:80h, bit 0) is set. The value written to this register does not affect the hardware other than changing the value returned during a read.
2. Reset: core well, but not D3-to-D0 warm reset.

17.1.19 PWR_CNTL_STS—Power Management Control/ Status Register (USB EHCI—D29:F7, D26:F7)

Address Offset:	54h–55h	Attribute:	R/W, R/WC, RO
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No (Bits 8 and 15 only)		

Bit	Description
15	**PME Status** — R/WC. 0 = Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). 1 = This bit is set when the ICH10 EHC would normally assert the PME# signal independent of the state of the PME_En bit. **NOTE:** This bit must be explicitly cleared by the operating system each time the operating system is loaded. This bit is not reset by Function Level Reset.
14:13	Data Scale — RO. Hardwired to 00b indicating it does not support the associated Data register.
12:9	Data Select — RO. Hardwired to 0000b indicating it does not support the associated Data register.
8	**PME Enable** — R/W. 0 = Disable. 1 = Enables Intel® ICH10 EHC to generate an internal PME signal when PME_Status is 1. **NOTE:** This bit must be explicitly cleared by the operating system each time it is initially loaded. This bit is not reset by Function Level Reset.
7:2	Reserved
1:0	**Power State** — R/W. This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the $D3_{HOT}$ state, the ICH10 must not accept accesses to the EHC memory range; but the configuration space must still be accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the PIRQH is not asserted by the ICH10 when not in the D0 state. When software changes this value from the $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

NOTE: Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.

17.1.20 DEBUG_CAPID—Debug Port Capability ID Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 58h
Default Value: 0Ah
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Debug Port Capability ID** — RO. Hardwired to 0Ah indicating that this is the start of a Debug Port Capability structure.

17.1.21 NXT_PTR2—Next Item Pointer #2 Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 59h
Default Value: 98h
Attribute: RO
Size: 8 bits
Function Level Reset: No

Bit	Description
7:0	**Next Item Pointer 2 Capability** — RO. This register points to the next capability in the Function Level Reset capability structure.

17.1.22 DEBUG_BASE—Debug Port Base Offset Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 5Ah–5Bh
Default Value: 20A0h
Attribute: RO
Size: 16 bits

Bit	Description
15:13	**BAR Number** — RO. Hardwired to 001b to indicate the memory BAR begins at offset 10h in the EHCI configuration space.
12:0	**Debug Port Offset** — RO. Hardwired to 0A0h to indicate that the Debug Port registers begin at offset A0h in the EHCI memory range.

17.1.23 USB_RELNUM—USB Release Number Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 60h
Default Value: 20h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**USB Release Number** — RO. A value of 20h indicates that this controller follows *Universal Serial Bus (USB) Specification, Revision 2.0*.

17.1.24 FL_ADJ—Frame Length Adjustment Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 61h
Default Value: 20h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
7:6	Reserved — RO. These bits are reserved for future use and should read as 00b.
5:0	**Frame Length Timing Value** — R/W. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.

Frame Length (# 480 MHz Clocks) (decimal)	Frame Length Timing Value (this register) (decimal)
59488	0
59504	1
59520	2
—	—
59984	31
60000	32
—	—

17.1.25 PWAKE_CAP—Port Wake Capability Register (USB EHCI—D29:F7, D26:F7)

Address Offset:	62–63h	Attribute:	R/W
Default Value:	01FFh	Size:	16 bits
Function Level Reset:	No		

This register is in the suspend power well. The intended use of this register is to establish a policy about which ports are to be used for wake events. Bit positions 1–8(D29) or 1–6(D26) in the mask correspond to a physical port implemented on the current EHCI controller. A 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/ connect or overcurrent events as wake-up events. This is an information-only mask register. The bits in this register **do not** affect the actual operation of the EHCI host controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. System software uses the information in this register when enabling devices and ports for remote wake-up.

These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
15:9 (D29) 15:7 (D26)	Reserved.
8:1 (D29) 6:1 (D26)	**Port Wake Up Capability Mask** — R/W. Bit positions 1 through 8 (Device 29) or 1 through 6(Device 26) correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, bit position 2 corresponds to port 2, etc.
0	**Port Wake Implemented** — R/W. A 1 in this bit indicates that this register is implemented to software.

17.1.26 LEG_EXT_CAP—USB EHCI Legacy Support Extended Capability Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 68–6Bh
Default Value: 00000001h
Power Well: Suspend
Function Level Reset: No
Attribute: R/W, RO
Size: 32 bits

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved — RO. Hardwired to 00h
24	**HC OS Owned Semaphore** — R/W. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear.
23:17	Reserved — RO. Hardwired to 00h
16	**HC BIOS Owned Semaphore** — R/W. The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software.
15:8	**Next EHCI Capability Pointer** — RO. Hardwired to 00h to indicate that there are no EHCI Extended Capability structures in this device.
7:0	**Capability ID** — RO. Hardwired to 01h to indicate that this EHCI Extended Capability is the Legacy Support Capability.

17.1.27 LEG_EXT_CS—USB EHCI Legacy Support Extended Control / Status Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 6C–6Fh
Default Value: 00000000h
Power Well: Suspend
Function Level Reset: No
Attribute: R/W, R/WC, RO
Size: 32 bits

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31	**SMI on BAR** — R/WC. Software clears this bit by writing a 1 to it. 0 = Base Address Register (BAR) not written. 1 = This bit is set to 1 when the Base Address Register (BAR) is written.
30	**SMI on PCI Command** — R/WC. Software clears this bit by writing a 1 to it. 0 = PCI Command (PCICMD) Register Not written. 1 = This bit is set to 1 when the PCI Command (PCICMD) Register is written.
29	**SMI on OS Ownership Change** — R/WC. Software clears this bit by writing a 1 to it. 0 = No HC OS Owned Semaphore bit change. 1 = This bit is set to 1 when the HC OS Owned Semaphore bit in the LEG_EXT_CAP register (D29:F7, D26:F7:68h, bit 24) transitions from 1 to 0 or 0 to 1.
28:22	Reserved.

Bit	Description
21	**SMI on Async Advance** — RO. This bit is a shadow bit of the Interrupt on Async Advance bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Interrupt on Async Advance bit in the USB2.0_STS register.
20	**SMI on Host System Error** — RO. This bit is a shadow bit of Host System Error bit in the USB2.0_STS register (D29:F7, D26:F7:CAPLENGTH + 24h, bit 4). **NOTE:** To clear this bit system software must write a 1 to the Host System Error bit in the USB2.0_STS register.
19	**SMI on Frame List Rollover** — RO. This bit is a shadow bit of Frame List Rollover bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Frame List Rollover bit in the USB2.0_STS register.
18	**SMI on Port Change Detect** — RO. This bit is a shadow bit of Port Change Detect bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Port Change Detect bit in the USB2.0_STS register.
17	**SMI on USB Error** — RO. This bit is a shadow bit of USB Error Interrupt (USBERRINT) bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the USB Error Interrupt bit in the USB2.0_STS register.
16	**SMI on USB Complete** — RO. This bit is a shadow bit of USB Interrupt (USBINT) bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the USB Interrupt bit in the USB2.0_STS register.
15	**SMI on BAR Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on BAR (D29:F7, D26:F7:6Ch, bit 31) is 1, then the host controller will issue an SMI.
14	**SMI on PCI Command Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PCI Command (D29:F7, D26:F7:6Ch, bit 30) is 1, then the host controller will issue an SMI.
13	**SMI on OS Ownership Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1 AND the OS Ownership Change bit (D29:F7, D26:F7:6Ch, bit 29) is 1, the host controller will issue an SMI.
12:6	Reserved.
5	**SMI on Async Advance Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Async Advance bit (D29:F7, D26:F7:6Ch, bit 21) is a 1, the host controller will issue an SMI immediately.
4	**SMI on Host System Error Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Host System Error (D29:F7, D26:F7:6Ch, bit 20) is a 1, the host controller will issue an SMI.

Bit	Description
3	**SMI on Frame List Rollover Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Frame List Rollover bit (D29:F7, D26:F7:6Ch, bit 19) is a 1, the host controller will issue an SMI.
2	**SMI on Port Change Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Port Change Detect bit (D29:F7, D26:F7:6Ch, bit 18) is a 1, the host controller will issue an SMI.
1	**SMI on USB Error Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Error bit (D29:F7, D26:F7:6Ch, bit 17) is a 1, the host controller will issue an SMI immediately.
0	**SMI on USB Complete Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Complete bit (D29:F7, D26:F7:6Ch, bit 16) is a 1, the host controller will issue an SMI immediately.

17.1.28 SPECIAL_SMI—Intel Specific USB 2.0 SMI Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 70h–73h
Default Value: 00000000h
Power Well: Suspend
Function Level Reset: No
Attribute: R/W, R/WC
Size: 32 bits

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:30 (D29) 31:28 (D26)	Reserved.
29:22 (D29) 27:22 (D26)	**SMI on PortOwner** — R/WC. Software clears these bits by writing a 1 to it. 0 = No Port Owner bit change. 1 = Bits 29:22, 27:22 correspond to the Port Owner bits for ports 1 (22) through 6 (27) or 8 (29). These bits are set to 1 when the associated Port Owner bits transition from 0 to 1 or 1 to 0.
21	**SMI on PMCSR** — R/WC. Software clears these bits by writing a 1 to it. 0 = Power State bits Not modified. 1 = Software modified the Power State bits in the Power Management Control/Status (PMCSR) register (D29:F7, D26:F7:54h).
20	**SMI on Async** — R/WC. Software clears these bits by writing a 1 to it. 0 = No Async Schedule Enable bit change 1 = Async Schedule Enable bit transitioned from 1 to 0 or 0 to 1.
19	**SMI on Periodic** — R/WC. Software clears this bit by writing a 1 it. 0 = No Periodic Schedule Enable bit change. 1 = Periodic Schedule Enable bit transitions from 1 to 0 or 0 to 1.

Bit	Description
18	**SMI on CF** — R/WC. Software clears this bit by writing a 1 it. 0 = No Configure Flag (CF) change. 1 = Configure Flag (CF) transitions from 1 to 0 or 0 to 1.
17	**SMI on HCHalted** — R/WC. Software clears this bit by writing a 1 it. 0 = HCHalted did Not transition to 1 (as a result of the Run/Stop bit being cleared). 1 = HCHalted transitions to 1 (as a result of the Run/Stop bit being cleared).
16	**SMI on HCReset** — R/WC. Software clears this bit by writing a 1 it. 0 = HCRESET did Not transitioned to 1. 1 = HCRESET transitioned to 1.
15:14	Reserved.
13:6	**SMI on PortOwner Enable** — R/W. 0 = Disable. 1 = Enable. When any of these bits are 1 and the corresponding SMI on PortOwner bits are 1, then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared.
5	**SMI on PMSCR Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PMSCR is 1, then the host controller will issue an SMI.
4	**SMI on Async Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Async is 1, then the host controller will issue an SMI
3	**SMI on Periodic Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Periodic is 1, then the host controller will issue an SMI.
2	**SMI on CF Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is 1 and SMI on CF is 1, then the host controller will issue an SMI.
1	**SMI on HCHalted Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCHalted is 1, then the host controller will issue an SMI.
0	**SMI on HCReset Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCReset is 1, then host controller will issue an SMI.

17.1.29 ACCESS_CNTL—Access Control Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 80h
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved
0	**WRT_RDONLY** — R/W. When set to 1, this bit enables a select group of normally read-only registers in the EHC function to be written by software. Registers that may only be written when this mode is entered are noted in the summary tables and detailed description as “Read/Write-Special”. The registers fall into two categories: 1. System-configured parameters, and 2. Status bits

17.1.30 EHCIIR1—EHCI Initialization Register 1 (USB EHCI—D29:F7, D26:F7)

Address Offset: 84h
Default Value: 01h
Attribute: R/W
Size: 8 bits

Bit	Description
7:5	Reserved
4	**Pre-fetch Based Pause Disable** — R/W. 0 = Pre-fetch Based Pause is enabled. 1 = Pre-fetch Based Pause is disabled.
3:0	Reserved

17.1.31 FLR_CID—Function Level Reset Capability ID (USB EHCI—D29:F7, D26:F7)

Address Offset: 98h
Default Value: 09h
Function Level Reset: No
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability ID** — R0. 13h = If FLRCSSEL = 0 09h (Vendor Specific Capability) = If FLRCSSEL = 1

17.1.32 FLR_NEXT—Function Level Reset Next Capability Pointer (USB EHCI—D29:F7, D26:F7)

Address Offset: 99h
Default Value: 00h
Function Level Reset: No
Attribute: RO
Size: 8 bits

Bit	Description
7:0	A value of 00h in this register indicates this is the last capability field.

17.1.33 FLR_CLV—Function Level Reset Capability Length and Version (USB EHCI—D29:F7, D26:F7)

Address Offset: 9Ah-9Bh
Default Value: 2006h
Function Level Reset: No
Attribute: R/WO, RO
Size: 16 bits

When FLRCSSEL = 0, this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**FLR Capability** — R/WO. 1 = Support for Function Level Reset (FLR).
8	**TXP Capability** — R/WO. 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length** — RO. This field indicates the # of bytes of this vendor specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

When FLRCSSEL = 1, this register is defined as follows:

Bit	Description
15:12	**Vendor Specific Capability ID** — RO. A value of 2h in this field identifies this capability as Function Level Reset.
11:8	**Capability Version** — RO. This field indicates the version of the FLR capability.
7:0	**Capability Length** — RO. This field indicates the # of bytes of this vendor specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

17.1.34 FLR_CTRL—Function Level Reset Control Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 9Ch
Default Value: 00h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Initiate FLR** — R/W. This bit is used to initiate FLR transition. A write of '1' initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the value read by software from this bit is always '0'.

17.1.35 FLR_STS—Function Level Reset Status Register (USB EHCI—D29:F7, D26:F7)

Address Offset: 9Dh
Default Value: 00h
Function Level Reset: No
Attribute: RO
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Transactions Pending (TXP)** — RO. 0 = Completions for all non-posted requests have been received. 1 = Controller has issued non-posted requests which have no bee completed.

17.1.36 EHCIIR2—EHCI Initialization Register 2 (USB EHCI—D29:F7, D26:F7)

Address Offset: FCh
Default Value: 20001706h
Attribute: R/W
Size: 32 bits

Bit	Description
31:30	Reserved
29	**EHCIIR2 Field 2** — R/W. BIOS must set this bit
28:18	Reserved
17	**EHCIIR2 Field 1** — R/W. BIOS must set this bit
16:4	Reserved
3:2	**EHCIIR2 Field 3 —** R/W. BIOS must set this field to 10b
1:0	Reserved

17.2 Memory-Mapped I/O Registers

The EHCI memory-mapped I/O space is composed of two sets of registers: Capability Registers and Operational Registers.

Note: The ICH10 EHCI controller will not accept memory transactions (neither reads nor writes) as a target that are locked transactions. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB.

Note: When the EHCI function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and result a master abort. Similarly, if the Memory Space Enable (MSE) bit (D29:F7, D26:F7:04h, bit 1) is not set in the Command register in configuration space, the memory range will not be decoded by the ICH10 enhanced host controller (EHC). If the MSE bit is not set, then the ICH10 must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

17.2.1 Host Controller Capability Registers

These registers specify the limits, restrictions and capabilities of the host controller implementation. Within the host controller capability registers, only the structural parameters register is writable. These registers are implemented in the suspend well and is only reset by the standard suspend-well hardware reset, not by HCRESET or the D3-to-D0 reset.

Note: Note that the EHCI controller does not support as a target memory transactions that are locked transactions. Attempting to access the EHCI controller Memory-Mapped I/O space using locked memory transactions will result in undefined behavior.

Note: Note that when the USB2 function is in the D3 PCI power state, accesses to the USB2 memory range are ignored and will result in a master abort Similarly, if the Memory Space Enable (MSE) bit is not set in the Command register in configuration space, the memory range will not be decoded by the Enhanced Host Controller (EHC). If the MSE bit is not set, then the EHC will not claim any memory accesses for the range specified in the BAR.

Table 17-2. Enhanced Host Controller Capability Registers

MEM_BASE + Offset	Mnemonic	Register	Default	Type
00h	CAPLENGTH	Capabilities Registers Length	20h	RO
02h–03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04h–07h	HCSPARAMS	Host Controller Structural Parameters	00103206h (D29:F7) 00102205 (D26:F7)	R/W (special), RO
08h–0Bh	HCCPARAMS	Host Controller Capability Parameters	00006871h	RO

NOTE: "Read/Write Special" means that the register is normally read-only, but may be written when the WRT_RDONLY bit is set. Because these registers are expected to be programmed by BIOS during initialization, their contents must not get modified by HCRESET or D3-to-D0 internal reset.

17.2.1.1 CAPLENGTH—Capability Registers Length Register

Offset:	MEM_BASE + 00h	Attribute:	RO
Default Value:	20h	Size:	8 bits

Bit	Description
7:0	**Capability Register Length Value** — RO. This register is used as an offset to add to the Memory Base Register (D29:F7, D26:F7:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h.

17.2.1.2 HCIVERSION—Host Controller Interface Version Number Register

Offset:	MEM_BASE + 02h–03h	Attribute:	RO
Default Value:	0100h	Size:	16 bits

Bit	Description
15:0	**Host Controller Interface Version Number** — RO. This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

17.2.1.3 HCSPARAMS—Host Controller Structural Parameters

Offset: MEM_BASE + 04h–07h Attribute: R/W, RO
Default Value: 00103206h (D29:F7) Size: 32 bits
00103206h (D26:F7)
Function Level Reset: No

Note: This register is reset by a suspend well reset and not a D3-to-D0 reset or HCRESET.

Bit	Description
31:24	Reserved.
23:20	**Debug Port Number (DP_N)** — RO. Hardwired to 1h indicating that the Debug Port is on the lowest numbered port on the EHCI.
19:16	Reserved
15:12	**Number of Companion Controllers (N_CC)** — R/W. This field indicates the number of companion controllers associated with this USB EHCI host controller. A 0 in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value of 1 or more in this field indicates there are companion USB UHCI host controller(s). Port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports. The ICH10 allows the default value of 3h (D29) or 3h (D26) to be over-written by BIOS. When removing classic controllers, they must be disabled in the following order: Function 3, Function 2, Function 1, and Function 0, which correspond to ports 11:10, 5:4, 3:2, and 1:0, respectively for Device 29. For Device 26 the following order is Function 2, Function 1 then Function 0, which correspond to ports 11:10, 9:8 and 7:6, respectively.
11:8	**Number of Ports per Companion Controller (N_PCC)** — RO. Hardwired to 2h. This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software.
7:4	Reserved. These bits are reserved and default to 0.
3:0	**N_PORTS** — R/W. This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1h to Fh. The ICH10 reports 6h for D29 and 6h for D26 by default. However, software may write a value less than the default for some platform configurations. A 0 in this field is undefined.

NOTE: This register is writable when the WRT_RDONLY bit is set.

17.2.1.4 HCCPARAMS—Host Controller Capability Parameters Register

Offset: MEM_BASE + 08h–0Bh Attribute: RO
Default Value: 00006871h Size: 32 bits

Bit	Description
31:18	Reserved
17	**Asynchronous Schedule Update Capability (ASUC)** — R/W. There is no functionality associated with this bit.
16	**Periodic Schedule Update Capability (PSUC)** — RO. This field is hardwired to 0b to indicate that the EHC hardware supports the Periodic Schedule Update Event Flag in the USB2.0_CMD register.
15:8	**EHCI Extended Capabilities Pointer (EECP)** — RO. This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	**Isochronous Scheduling Threshold** — RO. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit 7 is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit 7 is a 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. This field is hardwired to 7h.
3	Reserved.
2	**Asynchronous Schedule Park Capability** — RO. This bit is hardwired to 0 indicating that the host controller does not support this optional feature
1	**Programmable Frame List Flag** — RO. 0 = System software must use a frame list length of 1024 elements with this host controller. The USB2.0_CMD register (D29:F7, D26:F7:CAPLENGTH + 20h, bits 3:2) *Frame List Size* field is a read-only register and must be set to 0. 1 = System software can specify and use a smaller frame list and configure the host controller via the USB2.0_CMD register *Frame List Size* field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	**64-bit Addressing Capability** — RO. This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. Values for this field have the following interpretation: 0 = Data structures using 32-bit address memory pointers 1 = Data structures using 64-bit address memory pointers This bit is hardwired to 1. **NOTE:** ICH10 supports 64 bit addressing only.

17.2.2 Host Controller Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base must be dword-aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space (MEM_BASE). Since CAPLENGTH is always 20h, Table 17-3 already accounts for this offset. All registers are 32 bits in length.

Table 17-3. Enhanced Host Controller Operational Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Special Notes	Type
20h–23h	USB2.0_CMD	USB 2.0 Command	00080000h		R/W, RO
24h–27h	USB2.0_STS	USB 2.0 Status	00001000h		R/WC, RO
28h–2Bh	USB2.0_INTR	USB 2.0 Interrupt Enable	00000000h		R/W
2Ch–2Fh	FRINDEX	USB 2.0 Frame Index	00000000h		R/W,
30h–33h	CTRLDSSEGMENT	Control Data Structure Segment	00000000h		R/W, RO
34h–37h	PERODICLISTBASE	Period Frame List Base Address	00000000h		R/W
38h–3Bh	ASYNCLISTADDR	Current Asynchronous List Address	00000000h		R/W
3Ch–5Fh	—	Reserved	0h		RO
60h–63h	CONFIGFLAG	Configure Flag	00000000h	Suspend	R/W
64h–67h	PORT0SC	Port 0 Status and Control	00003000h	Suspend	R/W, R/WC, RO
68h–6Bh	PORT1SC	Port 1 Status and Control	00003000h	Suspend	R/W, R/WC, RO
6Ch–6Fh	PORT2SC	Port 2 Status and Control	00003000h	Suspend	R/W, R/WC, RO
70h–73h	PORT3SC	Port 3 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74h–77h	PORT4SC	Port 4 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78h–7Bh	PORT5SC	Port 5 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74h–77h (D29 Only)	PORT6SC	Port 6 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78h–7Bh (D29 Only)	PORT7SC	Port 7 Status and Control	00003000h	Suspend	R/W, R/WC, RO
7Ch–9Fh	—	Reserved	Undefined		RO
A0h–B3h	—	Debug Port Registers	Undefined		See register description
B4h–3FFh	—	Reserved	Undefined		RO

Note: Software must read and write these registers using only dword accesses.These registers are divided into two sets. The first set at offsets MEM_BASE + 00:3Bh are implemented in the core power well. Unless otherwise noted, the core well registers are reset by the assertion of any of the following:

- Core well hardware reset
- HCRESET
- D3-to-D0 reset

The second set at offsets MEM_BASE + 60h to the end of the implemented register space are implemented in the Suspend power well. Unless otherwise noted, the suspend well registers are reset by the assertion of either of the following:

- Suspend well hardware reset
- HCRESET

17.2.2.1 USB2.0_CMD—USB 2.0 Command Register

Offset:	MEM_BASE + 20–23h	Attribute:	R/W, RO
Default Value:	00080000h	Size:	32 bits

Bit	Description
31:24	Reserved.
23:16	**Interrupt Threshold Control** — R/W. System software uses this field to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. **Value** — **Maximum Interrupt Interval** 00h — Reserved 01h — 1 micro-frame 02h — 2 micro-frames 04h — 4 micro-frames 08h — 8 micro-frames (default, equates to 1 ms) 10h — 16 micro-frames (2 ms) 20h — 32 micro-frames (4 ms) 40h — 64 micro-frames (8 ms)
15:14	Reserved.
13	**Asynch Schedule Update (ASC)** — R/W. There is no functionality associated with this bit.
12	**Periodic Schedule Prefetch Enable** — R/W. This bit is used by software to enable the host controller to prefetch the periodic schedule even in C0. 0 = Prefetch based pause enabled only when not in C0. 1 = Prefetch based pause enable in C0. Once software has written a 1b to this bit to enable periodic schedule prefetching, it must disable prefecthing by writing a 0b to this bit whenever periodic schedule updates are about to begin. Software should continue to dynamically disable and re-enable the prefetcher surrounding any updates to the periodic scheduler (i.e. until the host controller has been reset via a HCRESET).
11:8	Unimplemented Asynchronous Park Mode Bits — RO. Hardwired to 000b indicating the host controller does not support this optional feature.
7	Light Host Controller Reset — RO. Hardwired to 0. The ICH10 does not implement this optional reset.

Bit	Description
6	**Interrupt on Async Advance Doorbell** — R/W. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. 0 = The host controller sets this bit to a 0 after it has set the Interrupt on Async Advance status bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register to a 1. 1 = Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USB2.0_STS register. If the *Interrupt on Async Advance Enable* bit in the USB2.0_INTR register (D29:F7, D26:F7:CAPLENGTH + 28h, bit 5) is a 1 then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. **NOTE:** Software should not write a 1 to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.
5	**Asynchronous Schedule Enable** — R/W. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0 = Do not process the Asynchronous Schedule 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4	**Periodic Schedule Enable** — R/W. This bit controls whether the host controller skips processing the Periodic Schedule. 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule.
3:2	**Frame List Size** — RO. The ICH10 hardwires this field to 00b because it only supports the 1024-element frame list size.
1	**Host Controller Reset (HCRESET)** — R/W. This control bit used by software to reset the host controller. The effects of this on root hub registers are similar to a Chip Hardware Reset (i.e., RSMRST# assertion and PWROK deassertion on the ICH10). When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. **NOTE:** PCI configuration registers and Host controller capability registers are not effected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in the EHCI spec. Software must re-initialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior. This reset me be used to leave EHCI port test modes.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>
Run/Stop (RS) — R/W.
0 = Stop (default)
1 = Run. When set to a 1, the Host controller proceeds with execution of the schedule. The Host controller continues execution as long as this bit is set. When this bit is set to 0, the Host controller completes the current transaction on the USB and then halts. The HCHalted bit in the USB2.0_STS register indicates when the Host controller has finished the transaction and has entered the stopped state.
Software should not write a 1 to this field unless the host controller is in the Halted state (i.e., HCHalted in the USBSTS register is a 1). The Halted bit is cleared immediately when the Run bit is set.
The following table explains how the different combinations of Run and Halted should be interpreted:
<table>
<tr><th>Run/Stop</th><th>Halted</th><th>Interpretation</th></tr>
<tr><td>0b</td><td>0b</td><td>In the process of halting</td></tr>
<tr><td>0b</td><td>1b</td><td>Halted</td></tr>
<tr><td>1b</td><td>0b</td><td>Running</td></tr>
<tr><td>1b</td><td>1b</td><td>Invalid - the HCHalted bit clears immediately</td></tr>
</table>
Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared.
</td></tr>
</table>

NOTE: The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

17.2.2.2 USB2.0_STS—USB 2.0 Status Register

Offset:	MEM_BASE + 24h–27h	Attribute:	R/WC, RO
Default Value:	00001000h	Size:	32 bits

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the EHCI specification for additional information concerning USB 2.0 interrupt conditions.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Description
31:16	Reserved.
15	**Asynchronous Schedule Status** — RO. This bit reports the current real status of the Asynchronous Schedule. 0 = Status of the Asynchronous Schedule is disabled. (Default) 1 = Status of the Asynchronous Schedule is enabled. **NOTE:** The Host controller is not required to *immediately* disable or enable the Asynchronous Schedule when software transitions the *Asynchronous Schedule Enable* bit (D29:F7, D26:F7:CAPLENGTH + 20h, bit 5) in the USB2.0_CMD register. When this bit and the *Asynchronous Schedule Enable* bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	**Periodic Schedule Status** — RO. This bit reports the current real status of the Periodic Schedule. 0 = Status of the Periodic Schedule is disabled. (Default) 1 = Status of the Periodic Schedule is enabled. **NOTE:** The Host controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit (D29:F7, D26:F7:CAPLENGTH + 20h, bit 4) in the USB2.0_CMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	**Reclamation** — RO. This read-only status bit is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	**HCHalted** — RO. 0 = This bit is a 0 when the Run/Stop bit is a 1. 1 = The Host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host controller hardware (e.g., internal error). (Default)
11:6	Reserved
5	**Interrupt on Async Advance** — R/WC. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the *Interrupt on Async Advance Doorbell* bit (D29:F7, D26:F7:CAPLENGTH + 20h, bit 6) in the USB2.0_CMD register. This bit indicates the assertion of that interrupt source.

Bit	Description
4	**Host System Error** — R/WC. 0 = No serious error occurred during a host system access involving the Host controller module 1 = The Host controller sets this bit to 1 when a serious error occurs during a host system access involving the Host controller module. A hardware interrupt is generated to the system. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set. When this error occurs, the Host controller clears the Run/Stop bit in the USB2.0_CMDregister (D29:F7, D26:F7:CAPLENGTH + 20h, bit 0) to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register).
3	**Frame List Rollover** — R/WC. 0 = No *Frame List Index* rollover from its maximum value to 0. 1 = The Host controller sets this bit to a 1 when the *Frame List Index* (see Section) rolls over from its maximum value to 0. Since the ICH10 only supports the 1024-entry Frame List Size, the *Frame List Index* rolls over every time FRNUM13 toggles.
2	**Port Change Detect** — R/WC. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change). Regardless of the implementation, when this bit is readable (i.e., in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the *Port Owner* bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
1	**USB Error Interrupt (USBERRINT)** — R/WC. 0 = No error condition. 1 = The Host controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	**USB Interrupt (USBINT)** — R/WC. 0 = No completion of a USB transaction whose Transfer Descriptor had its IOC bit set. No short packet is detected. 1 = The Host controller sets this bit to 1 when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. The Host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

17.2.2.3 USB2.0_INTR—USB 2.0 Interrupt Enable Register

Offset:	MEM_BASE + 28h–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USB2.0_STS Register to allow the software to poll for events. Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism (see Section 4 of the EHCI specification), or not.

Bit	Description
31:6	Reserved.
5	**Interrupt on Async Advance Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Interrupt on Async Advance bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	**Host System Error Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Host System Error Status bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 4) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	**Frame List Rollover Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Frame List Rollover bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	**Port Change Interrupt Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Port Change Detect bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	**USB Error Interrupt Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBERRINT bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit in the USB2.0_STS register.
0	**USB Interrupt Enable** — R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBINT bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit in the USB2.0_STS register.

17.2.2.4 FRINDEX—Frame Index Register

Offset:	MEM_BASE + 2Ch–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Refer to Section 4 of the EHCI specification for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be within 125 µs (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2:0] increments from 0 to 1.

Software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the **get** micro-frame number function required to client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent if chip is reset or software writes to FRINDEX. Writes to FRINDEX must also **write-through** FRINDEX[13:3] to SOFV[10:0]. In order to keep the update as simple as possible, software should never write a FRINDEX value where the three least significant bits are 111b or 000b.

Note: This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [12:3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index is fixed at 10 for the ICH10 since it only supports 1024-entry frame lists. This register must be written as a dword. Word and byte writes produce undefined results. This register cannot be written unless the Host controller is in the Halted state as indicated by the *HCHalted* bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 12). A write to this register while the Run/Stop bit (D29:F7, D26:F7:CAPLENGTH + 20h, bit 0) is set to a 1 (USB2.0_CMD register) produces undefined results. Writes to this register also effect the SOF value. See Section 4 of the EHCI specification for details.

Bit	Description
31:14	Reserved
13:0	**Frame List Current Index/Frame Number** — R/W. The value in this register increments at the end of each time frame (e.g., micro-frame). Bits [12:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.

17.2.2.5 CTRLDSSEGMENT—Control Data Structure Segment Register

Offset:	MEM_BASE + 30h–33h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. Since the ICH10 hardwires the 64-bit Addressing Capability field in HCCPARAMS to 1, then this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 GB memory segment.

Bit	Description
31:12	Upper Address[63:44] — RO. Hardwired to 0s. The ICH10 EHC is only capable of generating addresses up to 16 terabytes (44 bits of address).
11:0	**Upper Address[43:32]** — R/W. This 12-bit field corresponds to address bits 43:32 when forming a control data structure address.

17.2.2.6 PERIODICLISTBASE—Periodic Frame List Base Address Register

Offset:	MEM_BASE + 34h–37h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. Since the ICH10 host controller operates in 64-bit mode (as indicated by the 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host controller to step through the Periodic Frame List in sequence.

Bit	Description
31:12	**Base Address (Low)** — R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved.

17.2.2.7 ASYNCLISTADDR—Current Asynchronous List Address Register

Offset:	MEM_BASE + 38h–3Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed. Since the ICH10 host controller operates in 64-bit mode (as indicated by a 1 in 64-bit Addressing Capability field in the HCCPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (offset 08h). Bits [4:0] of this register cannot be modified by system software and will always return 0s when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Description
31:5	**Link Pointer Low (LPL)** — R/W. These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).
4:0	Reserved.

17.2.2.8 CONFIGFLAG—Configure Flag Register

Offset:	MEM_BASE + 60h–63h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

Bit	Description
31:1	Reserved.
0	**Configure Flag (CF)** — R/W. Host software sets this bit as the last action in its process of configuring the Host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See Chapter 4 of the EHCI specification for operation details. 0 = Port routing control logic default-routes each port to the UHCIs (default). 1 = Port routing control logic default-routes all ports to this host controller.

17.2.2.9 PORTSC—Port N Status and Control Register

Offset: Port 0, Port 6: MEM_BASE + 64h–67h
Port 1, Port 7: MEM_BASE + 68–6Bh
Port 2, Port 8: MEM_BASE + 6C–6Fh
Port 3, Port 9: MEM_BASE + 70–73h
Port 4: Port 10: MEM_BASE + 74–77h
Port 5: Port 11: MEM_BASE + 78–7Bh
Port 6: MEM_BASE + 7Ch-7Bh
Port 7: MEM_BASE + 80h-83h
Attribute: R/W, R/WC, RO
Default Value: 00003000h Size: 32 bits

A host controller must implement one or more port registers. Software uses the N_Port information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control Registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled.

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the EHCI specification for operational requirements for how change events interact with port suspend mode.

Bit	Description
31:23	Reserved.
22	**Wake on Overcurrent Enable (WKOC_E)** — R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the overcurrent Active bit (bit 4 of this register) is set.
21	**Wake on Disconnect Enable (WKDSCNNT_E)** — R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0).
20	**Wake on Connect Enable (WKCNNT_E)** — R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1).

Bit	Description
19:16	**Port Test Control** — R/W. When this field is 0s, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b – 1111b are reserved): **Value** — **Maximum Interrupt Interval** 0000b — Test mode not enabled (default) 0001b — Test J_STATE 0010b — Test K_STATE 0011b — Test SE0_NAK 0100b — Test Packet 0101b — FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 for details on each test mode.
15:14	Reserved.
13	**Port Owner** — R/W. This bit unconditionally goes to a 0 when the Configured Flag bit in the USB2.0_CMD register makes a 0 to 1 transition. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See Chapter 4 of the EHCI Specification for operational details.
12	**Port Power (PP)** — RO. Read-only with a value of 1. This indicates that the port does have power.
11:10	**Line Status**— RO.These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1. 00 = SE0 10 = J-state 01 = K-state 11 = Undefined
9	Reserved.

Bit	Description
8	**Port Reset** — R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the *USB Specification, Revision 2.0*. 1 = Port is in Reset. 0 = Port is not in Reset. **NOTE:** When software writes a 0 to this bit, there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g., set the *Port Enable* bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 0 to 1. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2 ms of software writing this bit to a 0. The HCHalted bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This bit is 0 if Port Power is 0 **NOTE:** System software should not attempt to reset a port if the *HCHalted* bit in the USB2.0_STS register is a 1. Doing so will result in undefined behavior.
7	**Suspend** — R/W. 0 = Port not in suspend state.(Default) 1 = Port in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: **Port Enabled** / **Suspend** / **Port State** 0 / X / Disabled 1 / 0 / Enabled 1 / 1 / Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port depending on the activity on the port. The host controller will unconditionally set this bit to a 0 when software sets the *Force Port Resume* bit to a 0 (from a 1). A write of 0 to this bit is ignored by the host controller. If host software sets this bit to a 1 when the port is not enabled (i.e., Port enabled bit is a 0) the results are undefined.

Bit	Description
6	**Force Port Resume** — R/W. 0 = No resume (K-state) detected/driven on port. (Default) 1 = Resume detected/driven on port. Software sets this bit to a 1 to drive resume signaling. The Host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit (D29:F7, D26:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. **NOTE:** When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification, Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle.
5	**Overcurrent Change** — R/WC. The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
4	**Overcurrent Active** — RO. 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the over current condition is removed. The ICH10 automatically disables the port when the overcurrent active bit is 1.
3	**Port Enable/Disable Change** — R/WC. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. 0 = No change in status. (Default). 1 = Port enabled/disabled status has changed.
2	**Port Enabled/Disabled** — R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)
1	**Connect Status Change** — R/WC. This bit indicates a change has occurred in the port's Current Connect Status. Software sets this bit to 0 by writing a 1 to it. 0 = No change (Default). 1 = Change in Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (i.e., the bit will remain set).
0	**Current Connect Status** — RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

17.2.3 USB 2.0-Based Debug Port Register

The Debug port's registers are located in the same memory area, defined by the Base Address Register (MEM_BASE), as the standard EHCI registers. The base offset for the debug port registers (A0h) is declared in the Debug Port Base Offset Capability Register at Configuration offset 5Ah (D29:F7, D26:F7:offset 5Ah). The specific EHCI port that supports this debug capability (Port 0 for D29:F7 and Port 6 for D26:F7) is indicated by a 4-bit field (bits 20–23) in the HCSPARAMS register of the EHCI controller. The address map of the Debug Port registers is shown in Table 17-4.

Table 17-4. Debug Port Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
A0–A3h	CNTL_STS	Control/Status	00000000h	R/W, R/WC, RO
A4–A7h	USBPID	USB PIDs	00000000h	R/W, RO
A8–AFh	DATABUF[7:0]	Data Buffer (Bytes 7:0)	00000000 00000000h	R/W
B0–B3h	CONFIG	Configuration	00007F01h	R/W

NOTES:
1. All of these registers are implemented in the core well and reset by PLTRST#, EHC HCRESET, and a EHC D3-to-D0 transition.
2. The hardware associated with this register provides no checks to ensure that software programs the interface correctly. How the hardware behaves when programmed improperly is undefined.

17.2.3.1 CNTL_STS—Control/Status Register

Offset: MEM_BASE + A0h
Default Value: 00000000h
Attribute: R/W, R/WC, RO
Size: 32 bits

Bit	Description
31	Reserved
30	**OWNER_CNT —** R/W. 0 = Ownership of the debug port is NOT forced to the EHCI controller (Default) 1 = Ownership of the debug port is forced to the EHCI controller (i.e. immediately taken away from the companion Classic USB Host controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers.
29	Reserved
28	**ENABLED_CNT —** R/W. 0 = Software can clear this by writing a 0 to it. The hardware clears this bit for the same conditions where the Port Enable/Disable Change bit (in the PORTSC register) is set. (Default) 1 = Debug port is enabled for operation. Software can directly set this bit if the port is already enabled in the associated PORTSC register (this is enforced by the hardware).
27:17	Reserved
16	**DONE_STS —** R/WC. Software can clear this by writing a 1 to it. 0 = Request Not complete 1 = Set by hardware to indicate that the request is complete.
15:12	LINK_ID_STS — RO. This field identifies the link interface. 0h = Hardwired. Indicates that it is a USB Debug Port.
11	Reserved.
10	**IN_USE_CNT —** R/W. Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.)
9:7	**EXCEPTION_STS —** RO. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 = No Error. (Default) **Note:** This should not be seen since this field should only be checked if there is an error. 001 = Transaction error: Indicates the USB 2.0 transaction had an error (CRC, bad PID, timeout, etc.) 010 = Hardware error. Request was attempted (or in progress) when port was suspended or reset. All Other combinations are reserved
6	**ERROR_GOOD#_STS —** RO. 0 = Hardware clears this bit to 0 after the proper completion of a read or write. (Default) 1 = Error has occurred. Details on the nature of the error are provided in the Exception field.

Bit	Description
5	**GO_CNT** — R/W. 0 = Hardware clears this bit when hardware sets the DONE_STS bit. (Default) 1 = Causes hardware to perform a read or write request. **NOTE:** Writing a 1 to this bit when it is already set may result in undefined behavior.
4	**WRITE_READ#_CNT —** R/W. Software clears this bit to indicate that the current request is a read. Software sets this bit to indicate that the current request is a write. 0 = Read (Default) 1 = Write
3:0	**DATA_LEN_CNT —** R/W. This field is used to indicate the size of the data to be transferred. default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1–8 indicates 1–8 bytes are to be transferred. Values 9–Fh are invalid and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1–8 indicates 1–8 bytes were received. Hardware is not allowed to return values 9–Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

NOTES:
1. Software should do Read-Modify-Write operations to this register to preserve the contents of bits not being modified. This include Reserved bits.
2. To preserve the usage of RESERVED bits in the future, software should always write the same value read from the bit until it is defined. Reserved bits will always return 0 when read.

17.2.3.2 USBPID—USB PIDs Register

Offset:	MEM_BASE + A4h–A7h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This Dword register is used to communicate PID information between the USB debug driver and the USB debug port. The debug port uses some of these fields to generate USB packets, and uses other fields to return PID information to the USB debug driver.

Bit	Description
31:24	Reserved.
23:16	**RECEIVED_PID_STS[23:16]** — RO. Hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit.
15:8	**SEND_PID_CNT[15:8]** — R/W. Hardware sends this PID to begin the data packet when sending data to USB (i.e., WRITE_READ#_CNT is asserted). Software typically sets this field to either DATA0 or DATA1 PID values.
7:0	**TOKEN_PID_CNT[7:0]** — R/W. Hardware sends this PID as the Token PID for each USB transaction. Software typically sets this field to either IN, OUT, or SETUP PID values.

17.2.3.3 DATABUF[7:0]—Data Buffer Bytes[7:0] Register

Offset:	MEM_BASE + A8h–AFh	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64 bits

This register can be accessed as 8 separate 8-bit registers or 2 separate 32-bit register.

Bit	Description
63:0	**DATABUFFER[63:0]** — R/W. This field is the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS bit (offset A0, bit 16) is cleared by the hardware, ERROR_GOOD#_STS (offset A0, bit 6) is cleared by the hardware, and the DATA_LENGTH_CNT field (offset A0, bits 3:0) indicates the number of bytes that are valid.

17.2.3.4 CONFIG—Configuration Register

Offset:	MEM_BASE + B0–B3h	Attribute:	R/W
Default Value:	00007F01h	Size:	32 bits

Bit	Description
31:15	Reserved
14:8	**USB_ADDRESS_CNF** — R/W. This 7-bit field identifies the USB device address used by the controller for all Token PID generation. (Default = 7Fh)
7:4	Reserved
3:0	**USB_ENDPOINT_CNF** — R/W. This 4-bit field identifies the endpoint used by the controller for all Token PID generation. (Default = 1h)

§ §

18 Intel® High Definition Audio Controller Registers (D27:F0)

The Intel High Definition Audio controller resides in PCI Device 27, Function 0 on bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

Note: All registers in this function (including memory-mapped registers) must be addressable in byte, word, and D-word quantities. The software must always make register accesses on natural boundaries (i.e. D-word accesses must be on D-word boundaries; word accesses on word boundaries, etc.) In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel High Definition Audio memory-mapped space, the results are undefined.

Note: Users interested in providing feedback on the Intel High Definition Audio specification or planning to implement the Intel High Definition Audio specification into a future product will need to execute the *Intel® High Definition Audio Specification Developer's Agreement*. For more information, contact nextgenaudio@intel.com.

18.1 Intel® High Definition Audio PCI Configuration Space (Intel® High Definition Audio— D27:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 18-1. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Access
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	04h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	LT	Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	HDBARL	Intel® High Definition Audio Lower Base Address (Memory)	00000004h	R/W, RO
14h–17h	HDBARU	Intel High Definition Audio Upper Base Address (Memory)	00000000h	R/W
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO

Table 18-1. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 2 of 2)

2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capability List Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Register Description	RO
40h	HDCTL	Intel High Definition Audio Control	01h	R/W, RO
44h	TCSEL	Traffic Class Select	00h	R/W
50h–51h	PID	PCI Power Management Capability ID	6001h	R/WO, RO
52h–53h	PC	Power Management Capabilities	C842h	RO
54h–57h	PCS	Power Management Control and Status	00000000h	R/W, RO, R/WC
60h–61h	MID	MSI Capability ID	7005h	RO
62h–63h	MMC	MSI Message Control	0080h	R/W, RO
64h–67h	MMLA	MSI Message Lower Address	00000000h	R/W, RO
68h–6Bh	MMUA	SMI Message Upper Address	00000000h	R/W
6Ch–6Dh	MMD	MSI Message Data	0000h	R/W
70h–71h	PXID	PCI Express* Capability Identifiers	0010h	RO
72h–73h	PXC	PCI Express Capabilities	0091h	RO
74h–77h	DEVCAP	Device Capabilities	10000000h	RO, R/WO
78h–79h	DEVC	Device Control	0800h	R/W, RO
7Ah–7Bh	DEVS	Device Status	0010h	RO
100h–103h	VCCAP	Virtual Channel Enhanced Capability Header	13010002h	R/WO
104h–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO
108h–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10Ch–10D	PVCCTL	Port VC Control	0000h	RO
10Eh–10Fh	PVCSTS	Port VC Status	0000h	RO
110h–113h	VC0CAP	VC0 Resource Capability	00000000h	RO
114h–117h	VC0CTL	VC0 Resource Control	800000FFh	R/W, RO
11Ah–11Bh	VC0STS	VC0 Resource Status	0000h	RO
11Ch–11Fh	VCiCAP	VCi Resource Capability	00000000h	RO
120h–123h	VCiCTL	VCi Resource Control	00000000h	R/W, RO
126h–127h	VCiSTS	VCi Resource Status	0000h	RO
130h–133h	RCCAP	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
134h–137h	ESD	Element Self Description	0F000100h	RO
140h–143h	L1DESC	Link 1 Description	00000001h	RO
148h–14Bh	L1ADDL	Link 1 Lower Address	See Register Description	RO
14Ch–14Fh	L1ADDU	Link 1 Upper Address	00000000h	RO

18.1.1 VID—Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset:	00h-01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

18.1.2 DID—Device Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 Intel High Definition Audio controller. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Device ID Register.

18.1.3 PCICMD—PCI Command Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)** — R/W. 0= The INTx# signals may be asserted. 1= The Intel® High Definition Audio controller's INTx# signal will be de-asserted. Note: that this bit does not affect the generation of MSI's.
9	Fast Back to Back Enable (FBE) — RO. Not implemented. Hardwired to 0.
8	**SERR# Enable (SERR_EN)** — R/W. SERR# is not generated by the ICH10 Intel High Definition Audio Controller.
7	Wait Cycle Control (WCC) — RO. Not implemented. Hardwired to 0.
6	Parity Error Response (PER) — R/W. Not implemented.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE) — RO. Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.

Bit	Description
2	**Bus Master Enable (BME)** — R/W. Controls standard PCI Express* bus mastering capabilities for Memory and I/O, reads and writes. Note that this bit also controls MSI generation since MSI's are essentially Memory writes. 0 = Disable 1 = Enable
1	**Memory Space Enable (MSE)** — R/W. Enables memory space addresses to the Intel High Definition Audio controller. 0 = Disable 1 = Enable
0	I/O Space Enable (IOSE)—RO. Hardwired to 0 since the Intel High Definition Audio controller does not implement I/O space.

18.1.4 PCISTS—PCI Status Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address: 06h–07h
Default Value: 0010h
Attribute: RO, R/WC
Size: 16 bits

Bit	Description
15	Detected Parity Error (DPE) — RO. Not implemented. Hardwired to 0.
14	SERR# Status (SERRS) — RO. Not implemented. Hardwired to 0.
13	**Received Master Abort (RMA)** — R/WC. Software clears this bit by writing a 1 to it. 0 = No master abort received. 1 = The Intel® High Definition Audio controller sets this bit when, as a bus master, it receives a master abort. When set, the Intel High Definition Audio controller clears the run bit for the channel that received the abort.
12	Received Target Abort (RTA) — RO. Not implemented. Hardwired to 0.
11	Signaled Target Abort (STA) — RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS) — RO. Does not apply. Hardwired to 0.
8	Data Parity Error Detected (DPED) — RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) — RO. Does not apply. Hardwired to 0.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP) — RO. Does not apply. Hardwired to 0.
4	**Capabilities List (CAP_LIST)** — RO. Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (IS)** — RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted. Note that this bit is not set by an MSI.
2:0	Reserved.

18.1.5 RID—Revision Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 08h Attribute: RO
Default Value: See bit description Size: 8 Bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

18.1.6 PI—Programming Interface Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface** — RO.

18.1.7 SCC—Sub Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ah Attribute: RO
Default Value: 03h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** — RO. 03h = Audio Device

18.1.8 BCC—Base Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Bh Attribute: RO
Default Value: 04h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. 04h = Multimedia device

18.1.9 CLS—Cache Line Size Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Cache Line Size** — R/W. Implemented as R/W register, but has no functional impact to the ICH10

18.1.10 LT—Latency Timer Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Latency Timer — RO. Hardwired to 00

18.1.11 HEADTYP—Header Type Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Header Type — RO. Hardwired to 00.

18.1.12 HDBARL—Intel® High Definition Audio Lower Base Address Register (Intel® High Definition Audio—D27:F0)

Address Offset: 10h-13h
Default Value: 00000004h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:14	**Lower Base Address (LBA)** — R/W. Base address for the Intel® High Definition Audio controller's memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0s.
13:4	Reserved.
3	Prefetchable (PREF) — RO. Hardwired to 0 to indicate that this BAR is NOT prefetchable
2:1	**Address Range (ADDRNG)** — RO. Hardwired to 10b, indicating that this BAR can be located anywhere in 64-bit address space.
0	**Space Type (SPTYP)** — RO. Hardwired to 0. Indicates this BAR is located in memory space.

18.1.13 HDBARU—Intel® High Definition Audio Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 14h-17h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Upper Base Address (UBA)** — R/W. Upper 32 bits of the Base address for the Intel® High Definition Audio controller's memory mapped configuration registers.

18.1.14 SVID—Subsystem Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No		

The SVID register, in combination with the Subsystem ID register (D27:F0:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem Vendor ID** — R/WO.

18.1.15 SID—Subsystem Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No		

The SID register, in combination with the Subsystem Vendor ID register (D27:F0:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem ID** — R/WO.

18.1.16 CAPPTR—Capabilities Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

This register indicates the offset for the capability pointer.

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)** — RO. This field indicates that the first capability pointer offset is offset 50h (Power Management Capability)

18.1.17 INTLN—Interrupt Line Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — R/W. This data is not used by the Intel® ICH10. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

18.1.18 INTPN—Interrupt Pin Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 3Dh
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:4	Reserved.
3:0	**Interrupt Pin** — RO. This reflects the value of D27IP.ZIP (Chipset Config Registers:Offset 3110h:bits 3:0).

18.1.19 HDCTL—Intel® High Definition Audio Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 40h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**Intel® High Definition Signal Mode** — RO. This bit is hardwired to 1 (High Definition Audio mode)

18.1.20 TCSEL—Traffic Class Select Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Function Level Reset:	No		

This register assigned the value to be placed in the TC field. CORB and RIRB data will always be assigned TC0.

Bit	Description
7:3	Reserved.
2:0	**Intel® High Definition Audio Traffic Class Assignment (TCSEL)**— R/W. This register assigns the value to be placed in the Traffic Class field for input data, output data, and buffer descriptor transactions. 000 = TC0 001 = TC1 010 = TC2 011 = TC3 100 = TC4 101 = TC5 110 = TC6 111 = TC7 **NOTE:** These bits are not reset on $D3_{HOT}$ to D0 transition; however, they are reset by PLTRST#.

18.1.21 PID—PCI Power Management Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	50h-51h	Attribute:	R/WO, RO
Default Value:	6001h	Size:	16 bits
Function Level Reset:	No (Bits 7:0 only)		

Bit	Description
15:8	**Next Capability (Next)** — R/WO. Points to the next capability structure (MSI).
7:0	**Cap ID (CAP)** — RO. Hardwired to 01h. Indicates that this pointer is a PCI power management capability. These bits are not reset by Function Level Reset.

18.1.22 PC—Power Management Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 52h-53h
Default Value: C842h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME Support** — RO. Hardwired to 11001b. Indicates PME# can be generated from D3 and D0 states.
10	D2 Support — RO. Hardwired to 0. Indicates that D2 state is not supported.
9	D1 Support —RO. Hardwired to 0. Indicates that D1 state is not supported.
8:6	**Aux Current** — RO. Hardwired to 001b. Reports 55 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI) — RO. Hardwired to 0. Indicates that no device specific initialization is required.
4	Reserved
3	PME Clock (PMEC) — RO. Does not apply. Hardwired to 0.
2:0	**Version** — RO. Hardwired to 010b. Indicates support for version 1.1 of the PCI Power Management Specification.

18.1.23 PCS—Power Management Control and Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	54h-57h	Attribute:	RO, R/W, R/WC
Default Value:	00000000h	Size:	32 bits
Function Level Reset:	No		

Bit	Description
31:24	**Data** — RO. Does not apply. Hardwired to 0.
23	Bus Power/Clock Control Enable — RO. Does not apply. Hardwired to 0.
22	B2/B3 Support — RO. Does not apply. Hardwired to 0.
21:16	Reserved.
15	**PME Status (PMES)** — R/WC. 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the Intel® High Definition Audio controller would normally assert the PME# signal independent of the state of the PME_EN bit (bit 8 in this register). This bit is in the resume well and is cleared by a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	Reserved
8	**PME Enable (PMEE)** — R/W. 0 = Disable 1 = When set and if corresponding PMES also set, the Intel High Definition Audio controller sets the PME_B0_STS bit in the GPE0_STS register (PMBASE +28h). This bit in the resume well and is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:2	Reserved
1:0	**Power State (PS)** — R/W. This field is used both to determine the current power state of the Intel High Definition Audio controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state Others = reserved **NOTES:** 1. If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. 2. When in the $D3_{HOT}$ states, the Intel High Definition Audio controller's configuration space is available, but the IO and memory space are not. Additionally, interrupts are blocked. 3. When software changes this value from $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

18.1.24 MID—MSI Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 60h-61h
Default Value: 7005h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (Next)** — RO. Hardwired to 70h. Points to the PCI Express* capability structure.
7:0	**Cap ID (CAP)** — RO. Hardwired to 05h. Indicates that this pointer is a MSI capability

18.1.25 MMC—MSI Message Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 62h-63h
Default Value: 0080h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64b Address Capability (64ADD)** — RO. Hardwired to 1. Indicates the ability to generate a 64-bit message address
6:4	Multiple Message Enable (MME) — RO. Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	Multiple Message Capable (MMC) — RO. Hardwired to 0 indicating request for 1 message.
0	**MSI Enable (ME)** — R/W. 0 = an MSI may not be generated 1 = an MSI will be generated instead of an INTx signal.

18.1.26 MMLA—MSI Message Lower Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 64h-67h
Default Value: 00000000h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:2	**Message Lower Address (MLA)** — R/W. Lower address used for MSI message.
1:0	Reserved.

18.1.27 MMUA—MSI Message Upper Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 68h-6Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Message Upper Address (MUA)** — R/W. Upper 32-bits of address used for MSI message.

18.1.28 MMD—MSI Message Data Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 6Ch-6Dh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Message Data (MD)** — R/W. Data used for MSI message.

18.1.29 PXID—PCI Express* Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 70h-71h
Default Value: 0010h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (Next)** — RO. Hardwired to 0. Indicates that this is the last capability structure in the list.
7:0	**Cap ID (CAP)** — RO. Hardwired to 10h. Indicates that this pointer is a PCI Express* capability structure

18.1.30 PXC—PCI Express* Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 72h-73h
Default Value: 0091h
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved
13:9	Interrupt Message Number (IMN) — RO. Hardwired to 0.
8	Slot Implemented (SI) — RO. Hardwired to 0.
7:4	**Device/Port Type (DPT)** — RO. Hardwired to 1001b. Indicates that this is a Root Complex Integrated endpoint device.
3:0	**Capability Version (CV)** — RO. Hardwired to 0001b. Indicates version #1 PCI Express capability

18.1.31 DEVCAP—Device Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 74h-77h
Default Value: 10000000h
Function Level Reset: No
Attribute: R/WO, RO
Size: 32 bits

Bit	Description
31:29	Reserved
28	**Function Level Reset (FLR)** — R/WO. A 1 indicates that the ICH10 HD Audio Controller supports the Function Level Reset Capability.
27:26	Captured Slot Power Limit Scale (SPLS) — RO. Hardwired to 0.
25:18	Captured Slot Power Limit Value (SPLV) — RO. Hardwired to 0.
17:15	Reserved
14	Power Indicator Present — RO. Hardwired to 0.
13	Attention Indicator Present — RO. Hardwired to 0.
12	Attention Button Present — RO. Hardwired to 0.
11:9	Endpoint L1 Acceptable Latency — R/WO.
8:6	**Endpoint L0s Acceptable Latency** — R/WO.
5	**Extended Tag Field Support** — RO. Hardwired to 0. Indicates 5-bit tag field support
4:3	Phantom Functions Supported — RO. Hardwired to 0. Indicates that phantom functions not supported
2:0	**Max Payload Size Supported** — RO. Hardwired to 0. Indicates 128-B maximum payload size capability

18.1.32 DEVC—Device Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset:	78h-79h	Attribute:	R/W, RO
Default Value:	0800h	Size:	16 bits
Function Level Reset:	No (Bit 11 Only)		

Bit	Description
15	**Initiate FLR (IF)** — R/W. This bit is used to initiate FLR transition. 1 = A write of 1 initiates FLR transition. Since hardware does not respond to any cycles until FLR completion, the read value by software from this bit is 0.
14:12	Max Read Request Size — RO. Hardwired to 0 enabling 128B maximum read request size.
11	**No Snoop Enable (NSNPEN)** — R/W. 0 = The Intel® High Definition Audio controller will not set the No Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0. 1 = The Intel High Definition Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers. **NOTE:** This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#. This bit is not reset by Function Level Reset.
10	Auxiliary Power Enable — RO. Hardwired to 0, indicating that Intel High Definition Audio device does not draw AUX power
9	Phantom Function Enable — RO. Hardwired to 0 disabling phantom functions.
8	**Extended Tag Field Enable** — RO. Hardwired to 0 enabling 5-bit tag.
7:5	**Max Payload Size** — RO. Hardwired to 0 indicating 128B.
4	Enable Relaxed Ordering — RO. Hardwired to 0 disabling relaxed ordering.
3	Unsupported Request Reporting Enable — R/W. Not implemented.
2	Fatal Error Reporting Enable — R/W. Not implemented.
1	Non-Fatal Error Reporting Enable — R/W. Not implemented.
0	Correctable Error Reporting Enable — R/W. Not implemented.

18.1.33 DEVS—Device Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 7Ah-7Bh
Default Value: 0010h
Attribute: RO
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending** — RO. 0 = Indicates that completions for all non-posted requests have been received 1 = Indicates that Intel® High Definition Audio controller has issued non-posted requests which have not been completed.
4	**AUX Power Detected** — RO. Hardwired to 1 indicating the device is connected to resume power
3	Unsupported Request Detected — RO. Not implemented. Hardwired to 0.
2	Fatal Error Detected — RO. Not implemented. Hardwired to 0.
1	Non-Fatal Error Detected — RO. Not implemented. Hardwired to 0.
0	Correctable Error Detected — RO. Not implemented. Hardwired to 0.

18.1.34 VCCAP—Virtual Channel Enhanced Capability Header (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 100h-103h
Default Value: 13010002h
Attribute: R/WO
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset** — R/WO. Points to the next capability header. 130h = Root Complex Link Declaration Enhanced Capability Header 000h = Root Complex Link Declaration Enhanced Capability Header is not supported.
19:16	**Capability Version** — R/WO. 0h = PCI Express Virtual channel capability and the Root Complex Topology Capability structure are not supported. 1h = PCI Express Virtual channel capability and the Root Complex Topology Capability structure are supported.
15:0	**PCI Express* Extended Capability** — R/WO. 0000h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are not supported. 0002h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are supported.

18.1.35 PVCCAP1—Port VC Capability Register 1 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 104h-107h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:12	Reserved.
11:10	Port Arbitration Table Entry Size — RO. Hardwired to 0 since this is an endpoint device.
9:8	Reference Clock — RO. Hardwired to 0 since this is an endpoint device.
7	Reserved.
6:4	Low Priority Extended VC Count — RO. Hardwired to 0. Indicates that only VC0 belongs to the low priority VC group
3	Reserved.
2:0	**Extended VC Count** — RO. Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by the Intel® High Definition Audio controller.

18.1.36 PVCCAP2 — Port VC Capability Register 2 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 108h-10Bh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	VC Arbitration Table Offset — RO. Hardwired to 0 indicating that a VC arbitration table is not present.
23:8	Reserved.
7:0	VC Arbitration Capability — RO. Hardwired to 0. These bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register.

18.1.37 PVCCTL — Port VC Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Ch-10Dh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:4	Reserved.
3:1	VC Arbitration Select — RO. Hardwired to 0. Normally these bits are R/W. However, these bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register
0	Load VC Arbitration Table — RO. Hardwired to 0 since an arbitration table is not present.

18.1.38 PVCSTS—Port VC Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Eh-10Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:1	Reserved.
0	VC Arbitration Table Status — RO. Hardwired to 0 since an arbitration table is not present.

18.1.39 VC0CAP—VC0 Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 110h-113h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	Port Arbitration Table Offset — RO. Hardwired to 0 since this field is not valid for endpoint devices
23	Reserved.
22:16	Maximum Time Slots — RO. Hardwired to 0 since this field is not valid for endpoint devices
15	Reject Snoop Transactions — RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	Advanced Packet Switching — RO. Hardwired to 0 since this field is not valid for endpoint devices
13:8	Reserved.
7:0	Port Arbitration Capability — RO. Hardwired to 0 since this field is not valid for endpoint devices

18.1.40 VC0CTL—VC0 Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 114h-117h
Default Value: 800000FFh
Function Level Reset: No
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	VC0 Enable — RO. Hardwired to 1 for VC0.
30:27	Reserved.
26:24	VC0 ID — RO. Hardwired to 0 since the first VC is always assigned as VC0.
23:20	Reserved.
19:17	Port Arbitration Select — RO. Hardwired to 0 since this field is not valid for endpoint devices.
16	Load Port Arbitration Table — RO. Hardwired to 0 since this field is not valid for endpoint devices.
15:8	Reserved.
7:0	**TC/VC0 Map** — R/W, RO. Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits [7:1] are implemented as R/W bits.

18.1.41 VC0STS—VC0 Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ah-11Bh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	VC0 Negotiation Pending — RO. Hardwired to 0 since this bit does not apply to the integrated Intel® High Definition Audio device.
0	Port Arbitration Table Status — RO. Hardwired to 0 since this field is not valid for endpoint devices.

18.1.42 VCiCAP—VCi Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ch-11Fh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	Port Arbitration Table Offset — RO. Hardwired to 0 since this field is not valid for endpoint devices.
23	Reserved.
22:16	Maximum Time Slots — RO. Hardwired to 0 since this field is not valid for endpoint devices.
15	Reject Snoop Transactions — RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	Advanced Packet Switching — RO. Hardwired to 0 since this field is not valid for endpoint devices.
13:8	Reserved
7:0	Port Arbitration Capability — RO. Hardwired to 0 since this field is not valid for endpoint devices.

18.1.43 VCiCTL—VCi Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 120h-123h
Default Value: 00000000h
Function Level Reset: No
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**VCi Enable** — R/W. 0 = VCi is disabled 1 = VCi is enabled **NOTE:** This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#.
30:27	Reserved.
26:24	**VCi ID** — R/W. This field assigns a VC ID to the VCi resource. This field is not used by the ICH10 hardware, but it is R/W to avoid confusing software.
23:20	Reserved.
19:17	Port Arbitration Select — RO. Hardwired to 0 since this field is not valid for endpoint devices.
16	Load Port Arbitration Table — RO. Hardwired to 0 since this field is not valid for endpoint devices.
15:8	Reserved.
7:0	**TC/VCi Map** — R/W, RO. This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VCi. Bits [7:1] are implemented as R/W bits. This field is not used by the ICH10 hardware, but it is R/W to avoid confusing software.

18.1.44 VCiSTS—VCi Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 126h-127h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	VCi Negotiation Pending — RO. Does not apply. Hardwired to 0.
0	Port Arbitration Table Status — RO. Hardwired to 0 since this field is not valid for endpoint devices.

18.1.45 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 130h
Default Value: 00010005h
Attribute: RO
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset** — RO. Hardwired to 0 indicating this is the last capability.
19:16	**Capability Version** — RO. Hardwired to 1h.
15:0	**PCI Express* Extended Capability ID** — RO. Hardwired to 0005h.

18.1.46 ESD—Element Self Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 134h-137h
Default Value: 0F000100h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Number** — RO. Hardwired to 0Fh indicating that the Intel® High Definition Audio controller is assigned as Port #15d.
23:16	**Component ID** — RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:8	**Number of Link Entries** — RO. The Intel High Definition Audio only connects to one device, the ICH10 egress port. Therefore this field reports a value of 1h.
7:4	Reserved.
3:0	**Element Type (ELTYP**) — RO. The Intel High Definition Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.

18.1.47 L1DESC—Link 1 Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 140h-143h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Target Port Number** — RO. The Intel High Definition Audio controller targets the Intel® ICH10's Port 0.
23:16	**Target Component ID** — RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:2	Reserved.
1	**Link Type** — RO. Hardwired to 0 indicating Type 0.
0	**Link Valid** — RO. Hardwired to 1.

18.1.48 L1ADDL—Link 1 Lower Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 148h-14Bh
Default Value: See Register Description
Attribute: RO
Size: 32 bits

Bit	Description
31:14	**Link 1 Lower Address** — RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h).
13:0	Reserved.

18.1.49 L1ADDU—Link 1 Upper Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 14Ch-14Fh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	**Link 1 Upper Address** — RO. Hardwired to 00000000h.

18.2 Intel® High Definition Audio Memory Mapped Configuration Registers (Intel® High Definition Audio— D27:F0)

The base memory location for these memory mapped configuration registers is specified in the HDBAR register (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at HDBAR + Offset as indicated in Table 18.2.

These memory mapped registers must be accessed in byte, word, or dword quantities.

Table 18-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 1 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
00h–01h	GCAP	Global Capabilities	4401h	RO
02h	VMIN	Minor Version	00h	RO
03h	VMAJ	Major Version	01h	RO
04h–05h	OUTPAY	Output Payload Capability	003Ch	RO
06h–07h	INPAY	Input Payload Capability	001Dh	RO
08h–0Bh	GCTL	Global Control	00000000h	R/W
0Ch–0Dh	WAKEEN	Wake Enable	0000h	R/W
0Eh–0Fh	STATESTS	State Change Status	0000h	R/WC
10h–11h	GSTS	Global Status	0000h	R/WC
12h–13h	Rsv	Reserved	0000h	RO
18h–19h	OUTSTRMPAY	Output Stream Payload Capability	0030h	RO
1Ah–1Bh	INSTRMPAY	Input Stream Payload Capability	0018h	RO
1Ch–1Fh	Rsv	Reserved	00000000h	RO
20h–23h	INTCTL	Interrupt Control	00000000h	R/W
24h–27h	INTSTS	Interrupt Status	00000000h	RO
30h–33h	WALCLK	Wall Clock Counter	00000000h	RO
34h–37h	SSYNC	Stream Synchronization	00000000h	R/W
40h–43h	CORBLBASE	CORB Lower Base Address	00000000h	R/W, RO
44h–47h	CORBUBASE	CORB Upper Base Address	00000000h	R/W
48h–49h	CORBWP	CORB Write Pointer	0000h	R/W
4Ah–4Bh	CORBRP	CORB Read Pointer	0000h	R/W, RO
4Ch	CORBCTL	CORB Control	00h	R/W
4Dh	CORBST	CORB Status	00h	R/WC
4Eh	CORBSIZE	CORB Size	42h	RO
50h–53h	RIRBLBASE	RIRB Lower Base Address	00000000h	R/W, RO
54h–57h	RIRBUBASE	RIRB Upper Base Address	00000000h	R/W
58h–59h	RIRBWP	RIRB Write Pointer	0000h	R/W, RO
5Ah–5Bh	RINTCNT	Response Interrupt Count	0000h	R/W
5Ch	RIRBCTL	RIRB Control	00h	R/W

Table 18-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 2 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
5Dh	RIRBSTS	RIRB Status	00h	R/WC
5Eh	RIRBSIZE	RIRB Size	42h	RO
60h–63h	IC	Immediate Command	00000000h	R/W
64h–67h	IR	Immediate Response	00000000h	RO
68h–69h	IRS	Immediate Command Status	0000h	R/W, R/WC
70h–73h	DPLBASE	DMA Position Lower Base Address	00000000h	R/W, RO
74h–77h	DPUBASE	DMA Position Upper Base Address	00000000h	R/W
80–82h	ISD0CTL	Input Stream Descriptor 0 (ISD0) Control	040000h	R/W, RO
83h	ISD0STS	ISD0 Status	00h	R/WC, RO
84h–87h	ISD0LPIB	ISD0 Link Position in Buffer	00000000h	RO
88h–8Bh	ISD0CBL	ISD0 Cyclic Buffer Length	00000000h	R/W
8Ch–8Dh	ISD0LVI	ISD0 Last Valid Index	0000h	R/W
8Eh–8F	ISD0FIFOW	ISD0 FIFO Watermark	0004h	R/W
90h–91h	ISD0FIFOS	ISD0 FIFO Size	0077h	RO
92h–93h	ISD0FMT	ISD0 Format	0000h	R/W
98h–9Bh	ISD0BDPL	ISD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
9Ch–9Fh	ISD0BDPU	ISD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
A0h–A2h	ISD1CTL	Input Stream Descriptor 1(ISD01) Control	040000h	R/W, RO
A3h	ISD1STS	ISD1 Status	00h	R/WC, RO
A4h–A7h	ISD1LPIB	ISD1 Link Position in Buffer	00000000h	RO
A8h–ABh	ISD1CBL	ISD1 Cyclic Buffer Length	00000000h	R/W
ACh–ADh	ISD1LVI	ISD1 Last Valid Index	0000h	R/W
AEh–AFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
B0h–B1h	ISD1FIFOS	ISD1 FIFO Size	0077h	RO
B2h–B3h	ISD1FMT	ISD1 Format	0000h	R/W
B8h–BBh	ISD1BDPL	ISD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
BCh–BFh	ISD1BDPU	ISD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
C0h–C2h	ISD2CTL	Input Stream Descriptor 2 (ISD2) Control	040000h	R/W, RO
C3h	ISD2STS	ISD2 Status	00h	R/WC, RO
C4h–C7h	ISD2LPIB	ISD2 Link Position in Buffer	00000000h	RO
C8h–CBh	ISD2CBL	ISD2 Cyclic Buffer Length	00000000h	R/W

Table 18-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 3 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
CCh–CDh	ISD2LVI	ISD2 Last Valid Index	0000h	R/W
CEh–CFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
D0h–D1h	ISD2FIFOS	ISD2 FIFO Size	0077h	RO
D2h–D3h	ISD2FMT	ISD2 Format	0000h	R/W
D8h–DBh	ISD2BDPL	ISD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
DCh–DFh	ISD2BDPU	ISD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
E0h–E2h	ISD3CTL	Input Stream Descriptor 3 (ISD3) Control	040000h	R/W, RO
E3h	ISD3STS	ISD3 Status	00h	R/WC, RO
E4h–E7h	ISD3LPIB	ISD3 Link Position in Buffer	00000000h	RO
E8h–EBh	ISD3CBL	ISD3 Cyclic Buffer Length	00000000h	R/W
ECh–EDh	ISD3LVI	ISD3 Last Valid Index	0000h	R/W
EEh–EFh	ISD3FIFOW	ISD3 FIFO Watermark	0004h	R/W
F0h–F1h	ISD3FIFOS	ISD3 FIFO Size	0077h	RO
F2h–F3h	ISD3FMT	ISD3 Format	0000h	R/W
F8h–FBh	ISD3BDPL	ISD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
FCh–FFh	ISD3BDPU	ISD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
100h–102h	OSD0CTL	Output Stream Descriptor 0 (OSD0) Control	040000h	R/W, RO
103h	OSD0STS	OSD0 Status	00h	R/WC, RO
104h–107h	OSD0LPIB	OSD0 Link Position in Buffer	00000000h	RO
108h–10Bh	OSD0CBL	OSD0 Cyclic Buffer Length	00000000h	R/W
10Ch–10Dh	OSD0LVI	OSD0 Last Valid Index	0000h	R/W
10Eh–10Fh	OSD0FIFOW	OSD0 FIFO Watermark	0004h	R/W
110h–111h	OSD0FIFOS	OSD0 FIFO Size	00BFh	R/W
112–113h	OSD0FMT	OSD0 Format	0000h	R/W
118h–11Bh	OSD0BDPL	OSD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
11Ch–11Fh	OSD0BDPU	OSD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
120h–122h	OSD1CTL	Output Stream Descriptor 1 (OSD1) Control	040000h	R/W, RO
123h	OSD1STS	OSD1 Status	00h	R/WC, RO
124h–127h	OSD1LPIB	OSD1 Link Position in Buffer	00000000h	RO
128h–12Bh	OSD1CBL	OSD1 Cyclic Buffer Length	00000000h	R/W

Table 18-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 4 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
12Ch–12Dh	OSD1LVI	OSD1 Last Valid Index	0000h	R/W
12Eh–12Fh	OSD1FIFOW	OSD1 FIFO Watermark	0004h	R/W
130h–131h	OSD1FIFOS	OSD1 FIFO Size	00BFh	R/W
132h–133h	OSD1FMT	OSD1 Format	0000h	R/W
138h–13Bh	OSD1BDPL	OSD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
13Ch–13Fh	OSD1BDPU	OSD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
140h–142h	OSD2CTL	Output Stream Descriptor 2 (OSD2) Control	040000h	R/W, RO
143h	OSD2STS	OSD2 Status	00h	R/WC, RO
144h–147h	OSD2LPIB	OSD2 Link Position in Buffer	00000000h	RO
148h–14Bh	OSD2CBL	OSD2 Cyclic Buffer Length	00000000h	R/W
14Ch–14Dh	OSD2LVI	OSD2 Last Valid Index	0000h	R/W
14Eh–14Fh	OSD2FIFOW	OSD2 FIFO Watermark	0004h	R/W
150h–151h	OSD2FIFOS	OSD2 FIFO Size	00BFh	R/W
152h–153h	OSD2FMT	OSD2 Format	0000h	R/W
158h–15Bh	OSD2BDPL	OSD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
15Ch–15Fh	OSD2BDPU	OSD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
160h–162h	OSD3CTL	Output Stream Descriptor 3 (OSD3) Control	040000h	R/W, RO
163h	OSD3STS	OSD3 Status	00h	R/WC, RO
164h–167h	OSD3LPIB	OSD3 Link Position in Buffer	00000000h	RO
168h–16Bh	OSD3CBL	OSD3 Cyclic Buffer Length	00000000h	R/W
16Ch–16Dh	OSD3LVI	OSD3 Last Valid Index	0000h	R/W
16Eh–16Fh	OSD3FIFOW	OSD3 FIFO Watermark	0004h	R/W
170h–171h	OSD3FIFOS	OSD3 FIFO Size	00BFh	R/W
172h–173h	OSD3FMT	OSD3 Format	0000h	R/W
178h–17Bh	OSD3BDPL	OSD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
17Ch–17Fh	OSD3BDPU	OSD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W

18.2.1 GCAP—Global Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 00h
Default Value: 4401h
Attribute: RO
Size: 16 bits

Bit	Description
15:12	**Number of Output Stream Supported** — RO. Hardwired to 0100b indicating that the ICH10 Intel® High Definition Audio controller supports 4 output streams.
11:8	**Number of Input Stream Supported** — RO. Hardwired to 0100b indicating that the ICH10 Intel High Definition Audio controller supports 4 input streams.
7:3	**Number of Bidirectional Stream Supported** — RO. Hardwired to 0 indicating that the ICH10 Intel High Definition Audio controller supports 0 bidirectional stream.
2	Reserved.
1	**Number of Serial Data Out Signals** — RO. Hardwired to 0 indicating that the ICH10 Intel High Definition Audio controller supports 1 serial data output signal.
0	**64-bit Address Supported** — RO. Hardwired to 1b indicating that the ICH10 Intel High Definition Audio controller supports 64-bit addressing for BDL addresses, data buffer addressees, and command buffer addresses.

18.2.2 VMIN—Minor Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 02h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Minor Version** — RO. Hardwired to 0 indicating that the Intel® ICH10 supports minor revision number 00h of the Intel® High Definition Audio specification.

18.2.3 VMAJ—Major Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 03h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Major Version** — RO. Hardwired to 01h indicating that the Intel® ICH10 supports major revision number 1 of the Intel® High Definition Audio specification.

18.2.4 OUTPAY—Output Payload Capability Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 04h
Default Value: 003Ch
Attribute: RO
Size: 16 bits

Bit	Description
15:7	Reserved.
6:0	**Output Payload Capability** — RO. Hardwired to 3Ch indicating 60 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

18.2.5 INPAY—Input Payload Capability Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 06h
Default Value: 001Dh
Attribute: RO
Size: 16 bits

Bit	Description
15:7	Reserved.
6:0	**Input Payload Capability** — RO. Hardwired to 1Dh indicating 29 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

18.2.6 GCTL—Global Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 08h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:9	Reserved.
8	**Accept Unsolicited Response Enable** — R/W. 0 = Unsolicited responses from the codecs are not accepted. 1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.
7:2	Reserved.
1	**Flush Control** — R/W. Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush the pipelines to memory to ensure that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	**Controller Reset #** — R/W. 0 = Writing a 0 causes the Intel High Definition Audio controller to be reset. All state machines, FIFOs and non-resume well memory mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel High Definition Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset. 1 = Writing a 1 causes the controller to exit its reset state and deassert the Intel High Definition Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel High Definition Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset, therefore, software needs to write a 1 to this bit to begin operation. **NOTES:** 1. The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start. 2. When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. 3. When this bit is 0 indicating that the controller is in reset, writes to all Intel High Definition Audio memory mapped registers are ignored as if the device is not present. The only exception is this register itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# (this bit) is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel High Definition Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a $D3_{HOT}$ to D0 transition.

18.2.7 WAKEEN—Wake Enable Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 0Ch	Attribute:	R/W
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No		

Bit	Description
15:4	Reserved.
3:0	**SDIN Wake Enable Flags** — R/W. These bits control which SDI signal(s) may generate a wake event. A 1b in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. Bit 0 is used for SDI[0] Bit 1 is used for SDI[1] Bit 2 is used for SDI[2] Bit 3 is used for SDI[3] **NOTE:** These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

18.2.8 STATESTS—State Change Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 0Eh	Attribute:	R/WC
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No		

Bit	Description
15:4	Reserved.
3:0	**SDIN State Change Status Flags** — R/WC. Flag bits that indicate which SDI signal(s) received a state change event. The bits are cleared by writing 1s to them. Bit 0 = SDI[0] Bit 1 = SDI[1] Bit 2 = SDI[2] Bit 3 = SDI[3] **NOTE:** These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

18.2.9 GSTS—Global Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 10h	Attribute:	R/WC
Default Value:	0000h	Size:	16 bits

Bit	Description
15:4	Reserved.
3	Reserved
2	Reserved
1	**Flush Status** — R/WC. This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (HDBAR + 08h, bit 1) was set has completed. Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.
0	Reserved.

18.2.10 OUTSTRMPAY—Output Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 18h	Attribute:	RO
Default Value:	0030h	Size:	16 bits

Bit	Description
15:14	**Output FIFO Padding Type (OPADTYPE)**— RO: Indicates how the controller pads the samples in the controller's buffer (FIFO). Controllers may not pad at all or may pad to byte or memory container sizes. 0h =Controller pads all samples to bytes 1h = Reserved 2h = Controller pads to memory container size 3h = Controller does not pad and uses samples directly
13:0	**Output Stream Payload Capability (OUTSTRMPAY)**— RO**:** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. The value does not specify the number of words actually transmitted in the frame, but is the size of the data in the controller buffer (FIFO) after the samples are padded as specified by OPADTYPE. Thus to compute the supported streams, each sample is padded according to OPADTYPE and then multiplied by the number of channels and samples per frame. If this computed value is larger than OUTSTRMPAY then that stream is not supported. The value specified is not affected by striping. Software must ensure that a format which would cause more Words per frame than indicated is not programmed into the Output Stream Descriptor Register. The value may be larger than the OUTPAY register value in some cases.

18.2.11 INSTRMPAY—Input Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 1Ah
Default Value: 0018h
Attribute: RO
Size: 16 bits

Bit	Description
15:14	**Input FIFO Padding Type (IPADTYPE)**— RO. Indicates how the controller pads the samples in the controller's buffer (FIFO). Controllers may not pad at all or may pad to byte or memory container sizes. 0h = Controller pads all samples to bytes 1h = Reserved 2h = Controller pads to memory container size 3h = Controller does not pad and uses samples directly
13:0	**Input Stream Payload Capability (INSTRMPAY)**— RO. Indicates the maximum number of Words per frame for any single input stream. This measurement is in 16-bit Word quantities per 48-kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. The value does not specify the number of words actually transmitted in the frame, but is the size of the data as it will be placed into the controller's buffer (FIFO). Thus samples will be padded according to IPADTYPE before being stored into controller buffer. To compute the supported streams, each sample is padded according to IPADTYPE and then multiplied by the number of channels and samples per frame. If this computed value is larger than INSTRMPAY then that stream is not supported. As the inbound stream tag is not stored with the samples it is not included in the word count. The value may be larger than INPAY register value in some cases, although values less than INPAY may also be invalid due to overhead. Software must ensure that a format which would cause more Words per frame than indicated is not programmed into the Input Stream Descriptor Register.

18.2.12 INTCTL—Interrupt Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 20h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31	**Global Interrupt Enable (GIE)** — R/W. Global bit to enable device interrupt generation. 1 = When set to 1, the Intel® High Definition Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	**Controller Interrupt Enable (CIE)** — R/W. Enables the general interrupt for controller functions. 1 = When set to 1, the controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Enable (SIE)** — R/W. When set to 1, the individual streams are enabled to generate an interrupt when the corresponding status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

18.2.13 INTSTS—Interrupt Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 24h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31	**Global Interrupt Status (GIS)** — RO. This bit is an OR of all the interrupt status bits in this register. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	**Controller Interrupt Status (CIS)** — RO. Status of general controller interrupt. 1 = Interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. This bit is an OR of all of the stated interrupt status bits for this register. **NOTES:** 1. This bit is set regardless of the state of the corresponding interrupt enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. 2. This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Status (SIS)** — RO. 1 = Interrupt condition occurred on the corresponding stream. This bit is an OR of all of the stream's interrupt status bits. **NOTE:** These bits are set regardless of the state of the corresponding interrupt enable bits. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

18.2.14 WALCLK—Wall Clock Counter Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 30h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	**Wall Clock Counter** — RO. 32 bit counter that is incremented on each link Bit Clock period and rolls over from FFFF FFFFh to 0000 0000h. This counter will roll over to 0 with a period of approximately 179 seconds. This counter is enabled while the Bit Clock bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

18.2.15 SSYNC—Stream Synchronization Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 34h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	**Stream Synchronization (SSYNC)** — R/W. When set to 1, these bits block data from being sent on or received from the link. Each bit controls the associated stream descriptor (i.e. bit 0 corresponds to the first stream descriptor, etc.) To synchronously start a set of DMA engines, these bits are first set to 1. The RUN bits for the associated stream descriptors are then set to 1 to start the DMA engines. When all streams are ready (FIFORDY =1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop the streams, fist these bits are set, and then the individual RUN bits in the stream descriptor are cleared by software. If synchronization is not desired, these bits may be left as 0, and the stream will simply begin running normally when the stream's RUN bit is set. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1

18.2.16 CORBLBASE—CORB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 40h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	**CORB Lower Base Address** — R/W. Lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	**CORB Lower Base Unimplemented Bits** — RO. Hardwired to 0. This required the CORB to be allocated with 128B granularity to allow for cache line fetch optimizations.

18.2.17 CORBUBASE—CORB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 44h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**CORB Upper Base Address** — R/W. Upper 32 bits of the address of the Command Output Ring buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

18.2.18 CORBWP—CORB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 48h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**CORB Write Pointer** — R/W. Software writes the last valid CORB entry offset into this field in dword granularity. The DMA engine fetches commands from the CORB until the Read pointer matches the Write pointer. Supports 256 CORB entries (256x4B = 1 KB). This register field may be written when the DMA engine is running.

18.2.19 CORBRP—CORB Read Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ah
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	**CORB Read Pointer Reset** — R/W. Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the Intel® High Definition Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	Reserved.
7:0	**CORB Read Pointer (CORBRP)**— RO. Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

18.2.20 CORBCTL—CORB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ch — Attribute: R/W
Default Value: 00h — Size: 8 bits

Bit	Description
7:2	Reserved.
1	**Enable CORB DMA Engine** — R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**CORB Memory Error Interrupt Enable** — R/W. If this bit is set the controller will generate an interrupt if the CMEI status bit (HDBAR + 4Dh: bit 0) is set.

18.2.21 CORBST—CORB Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Dh — Attribute: R/WC
Default Value: 00h — Size: 8 bits

Bit	Description
7:1	Reserved.
0	**CORB Memory Error Indication (CMEI)** — R/WC. 1 = Controller detected an error in the path way between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an un-viable state and typically required a controller reset by writing a 0 to the Controller Reset # bit (HDBAR + 08h: bit 0).

18.2.22 CORBSIZE—CORB Size Register Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Eh — Attribute: RO
Default Value: 42h — Size: 8 bits

Bit	Description
7:4	**CORB Size Capability** — RO. Hardwired to 0100b indicating that the ICH10 only supports a CORB size of 256 CORB entries (1024B)
3:2	Reserved.
1:0	**CORB Size** — RO. Hardwired to 10b which sets the CORB size to 256 entries (1024B)

18.2.23 RIRBLBASE—RIRB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 50h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	**CORB Lower Base Address** — R/W. Lower address of the Response Input Ring Buffer, allowing the RIRB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RIRB Lower Base Unimplemented Bits — RO. Hardwired to 0. This required the RIRB to be allocated with 128-B granularity to allow for cache line fetch optimizations.

18.2.24 RIRBUBASE—RIRB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 54h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**RIRB Upper Base Address** — R/W. Upper 32 bits of the address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

18.2.25 RIRBWP—RIRB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 58h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	**RIRB Write Pointer Reset** — R/W. Software writes a 1 to this bit to reset the RIRB Write Pointer to 0. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	Reserved.
7:0	**RIRB Write Pointer (RIRBWP)** — RO. Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 dword RIRB entry units (since each RIRB entry is 2 dwords long). Supports up to 256 RIRB entries (256 x 8 B = 2 KB). This register field may be written when the DMA engine is running.

18.2.26 RINTCNT—Response Interrupt Count Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ah
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**N Response Interrupt Count** — R/W. 0000 0001b = 1 response sent to RIRB ..... 1111 1111b = 255 responses sent to RIRB 0000 0000b = 256 responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each response occupies 2 dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codecs responds in one frame, then the count is increased by the number of responses received in the frame.

18.2.27 RIRBCTL—RIRB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:3	Reserved.
2	**Response Overrun Interrupt Control** — R/W. If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (HDBAR + 5Dh: bit 2) is set.
1	**Enable RIRB DMA Engine** — R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**Response Interrupt Control** — R/W. 0 = Disable Interrupt 1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

18.2.28 RIRBSTS—RIRB Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Dh
Default Value: 00h
Attribute: R/WC
Size: 8 bits

Bit	Description
7:3	Reserved.
2	**Response Overrun Interrupt Status** — R/WC. 1 = Software sets this bit to 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.
1	Reserved.
0	**Response Interrupt** — R/WC. 1 = Hardware sets this bit to 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.

18.2.29 RIRBSIZE—RIRB Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Eh
Default Value: 42h
Attribute: RO
Size: 8 bits

Bit	Description
7:4	**RIRB Size Capability** — RO. Hardwired to 0100b indicating that the ICH10 only supports a RIRB size of 256 RIRB entries (2048B)
3:2	Reserved.
1:0	**RIRB Size** — RO. Hardwired to 10b which sets the CORB size to 256 entries (2048B)

18.2.30 IC—Immediate Command Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 60h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Immediate Command Write — R/W**. The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit (HDBAR + 68h: bit 0)

18.2.31 IR—Immediate Response Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 64h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:0	**Immediate Response Read (IRR)** — RO. This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same time, there is no assurance as to which response will be latched. Therefore, broadcast-type commands must not be issued via the Immediate Command mechanism.

18.2.32 IRS—Immediate Command Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 68h
Default Value: 0000h
Attribute: R/W, R/WC
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**Immediate Result Valid (IRV)** — R/WC. 1 = Set to 1 by hardware when a new response is latched into the Immediate Response register (HDBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.
0	**Immediate Command Busy (ICB)** — R/W. When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. **NOTE:** An Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

18.2.33 DPLBASE—DMA Position Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 70h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:7	**DMA Position Lower Base Address** — R/W. Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the Flush Control bit (HDBAR+08h:bit 1) is set.
6:1	DMA Position Lower Base Unimplemented bits — RO. Hardwired to 0 to force the 128-byte buffer alignment for cache line write optimizations.
0	**DMA Position Buffer Enable** — R/W. 1 = Controller will write the DMA positions of each of the DMA engines to the buffer in the main memory periodically (typically once per frame). Software can use this value to know what data in memory is valid data.

18.2.34 DPUBASE—DMA Position Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 74h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**DMA Position Upper Base Address** — R/W. Upper 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted.

18.2.35 SDCTL—Stream Descriptor Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 80h
Input Stream[1]: HDBAR + A0h
Input Stream[2]: HDBAR + C0h
Input Stream[3]: HDBAR + E0h
Output Stream[0]: HDBAR + 100h
Output Stream[1]: HDBAR + 120h
Output Stream[2]: HDBAR + 140h
Output Stream[3]: HDBAR + 160h

Attribute: R/W, RO

Default Value: 040000h

Size: 24 bits

Bit	Description
23:20	**Stream Number** — R/W. This value reflect the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the SYNC signal. When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor. Note that while a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number. 0000 = Reserved 0001 = Stream 1 ..... 1110 = Stream 14 1111 = Stream 15
19	Bidirectional Direction Control — RO. This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.
18	**Traffic Priority** — RO. Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express* registers.
17:16	Stripe Control — RO. This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.
15:5	Reserved
4	**Descriptor Error Interrupt Enable** — R/W. 0 = Disable 1 = An interrupt is generated when the Descriptor Error Status bit is set.
3	**FIFO Error Interrupt Enable** — R/W. This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	**Interrupt on Completion Enable** — R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.

Bit	Description
1	**Stream Run (RUN)** — R/W. 0 = DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine. 1 = DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
0	**Stream Reset (SRST)** — R/W. 0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. 1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.

18.2.36 SDSTS—Stream Descriptor Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 83h
Input Stream[1]: HDBAR + A3h
Input Stream[2]: HDBAR + C3h
Input Stream[3]: HDBAR + E3h
Output Stream[0]: HDBAR + 103h
Output Stream[1]: HDBAR + 123h
Output Stream[2]: HDBAR + 143h
Output Stream[3]: HDBAR + 163h
Attribute: R/WC, RO

Default Value: 00h
Size: 8 bits

Bit	Description
7:6	Reserved.
5	**FIFO Ready (FIFORDY)** — RO. For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
4	**Descriptor Error** — R/WC. 1 = A serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stopped. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	**FIFO Error** — R/WC. 1 = FIFO error occurred. This bit is set even if an interrupt is not enabled. The bit is cleared by writing a 1 to it. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	**Buffer Completion Interrupt Status** — R/WC. This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.
1:0	Reserved.

18.2.37 SDLPIB—Stream Descriptor Link Position in Buffer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 84h — Attribute: RO
Input Stream[1]: HDBAR + A4h
Input Stream[2]: HDBAR + C4h
Input Stream[3]: HDBAR + E4h
Output Stream[0]: HDBAR + 104h
Output Stream[1]: HDBAR + 124h
Output Stream[2]: HDBAR + 144h
Output Stream[3]: HDBAR + 164h

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:0	**Link Position in Buffer** — RO. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

18.2.38 SDCBL—Stream Descriptor Cyclic Buffer Length Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 88h — Attribute: R/W
Input Stream[1]: HDBAR + A8h
Input Stream[2]: HDBAR + C8h
Input Stream[3]: HDBAR + E8h
Output Stream[0]: HDBAR + 108h
Output Stream[1]: HDBAR + 128h
Output Stream[2]: HDBAR + 148h
Output Stream[3]: HDBAR + 168h

Default Value: 00000000h — Size: 32 bits

Bit	Description
31:0	**Cyclic Buffer Length** — R/W. Indicates the number of bytes in the complete cyclic buffer. This register represents an integer number of samples. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should be only modified when the RUN bit is 0. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfer may be corrupted.

18.2.39 SDLVI—Stream Descriptor Last Valid Index Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Ch — Attribute: R/W
Input Stream[1]: HDBAR + ACh
Input Stream[2]: HDBAR + CCh
Input Stream[3]: HDBAR + ECh
Output Stream[0]: HDBAR + 10Ch
Output Stream[1]: HDBAR + 12Ch
Output Stream[2]: HDBAR + 14Ch
Output Stream[3]: HDBAR + 16Ch

Default Value: 0000h — Size: 16 bits

Bit	Description
15:8	Reserved.
7:0	**Last Valid Index** — R/W. The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. This field must be at least 1, i.e. there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin. This value should only modified when the RUN bit is 0.

18.2.40 SDFIFOW—Stream Descriptor FIFO Watermark Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Eh — Attribute: R/W
Input Stream[1]: HDBAR + AEh
Input Stream[2]: HDBAR + CEh
Input Stream[3]: HDBAR + EEh
Output Stream[0]: HDBAR + 10Eh
Output Stream[1]: HDBAR + 12Eh
Output Stream[2]: HDBAR + 14Eh
Output Stream[3]: HDBAR + 16Eh

Default Value: 0004h — Size: 16 bits

Bit	Description
15:3	Reserved.
2:0	**FIFO Watermark (FIFOW)** — R/W. Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/eviction of data. 010 = 8B 011 = 16B 100 = 32B (Default) 101 = 64B Others = Unsupported **NOTE:** When the bit field is programmed to an unsupported size, the hardware sets itself to the default value. Software must read the bit field to test if the value is supported after setting the bit field.

18.2.41 SDFIFOS—Stream Descriptor FIFO Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 90h
Input Stream[1]: HDBAR + B0h
Input Stream[2]: HDBAR + D0h
Input Stream[3]: HDBAR + F0h
Output Stream[0]: HDBAR + 110h
Output Stream[1]: HDBAR + 130h
Output Stream[2]: HDBAR + 150h
Output Stream[3]: HDBAR + 170h
Attribute: Input: RO
Output: R/W

Default Value: Input Stream: 0077h
Output Stream: See Description.
Size: 16 bits

Bit	Description
15:10	Reserved.
9:0	**FIFO Size** — RO (Input stream), R/W (Output stream). Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. The value in this field is different for input and output streams. It is also dependent on the Bits per Samples setting for the corresponding stream. Following are the values read/written from/to this register for input and output streams, and for non-padded and padded bit formats: *Output Stream R/W value*: **Value** — **Output Streams** 0Fh = 16B — 8, 16, 20, 24, or 32 bit Output Streams 1Fh = 32B — 8, 16, 20, 24, or 32 bit Output Streams 3Fh = 64B — 8, 16, 20, 24, or 32 bit Output Streams 7Fh = 128B — 8, 16, 20, 24, or 32 bit Output Streams BFh = 192B — 8, 16, or 32 bit Output Streams (Default) FFh = 256B — 20 or 24 bit Output Streams (Default) 17Fh = 384B — 8, 16, or 32 bit Output Streams 1FFh = 512B — 20 or 24 bit Output Streams **NOTES:** 1. All other values not listed are not supported. 2. When the output stream is programmed to an unsupported size, the hardware sets itself to the default value (BFh). 3. Software must read the bit field to test if the value is supported after setting the bit field. *Input Stream RO value*: **Value** — **Input Streams** 77h = 120B — 8, 16, 32 bit Input Streams 9Fh = 160B — 20, 24 bit Input Streams **NOTE:** The default value is different for input and output streams, and reflects the default state of the BITS fields (in Stream Descriptor Format registers) for the corresponding stream.

18.2.42 SDFMT—Stream Descriptor Format Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 92h — Attribute: R/W
Input Stream[1]: HDBAR + B2h
Input Stream[2]: HDBAR + D2h
Input Stream[3]: HDBAR + F2h
Output Stream[0]: HDBAR + 112h
Output Stream[1]: HDBAR + 132h
Output Stream[2]: HDBAR + 152h
Output Stream[3]: HDBAR + 172h

Default Value: 0000h — Size: 16 bits

Bit	Description
15	Reserved.
14	**Sample Base Rate** — R/W 0 = 48 kHz 1 = 44.1 kHz
13:11	**Sample Base Rate Multiple** — R/W 000 = 48 kHz, 44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) Others = Reserved.
10:8	**Sample Base Rate Devisor** — R/W. 000 = Divide by 1(48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Reserved.
6:4	**Bits per Sample (BITS)** — R/W. 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries Others = Reserved.
3:0	Number of Channels (CHAN) — R/W. Indicates number of channels in each frame of the stream. 0000 =1 0001 =2 ..... 1111 =16

18.2.43 SDBDPL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 98h
Input Stream[1]: HDBAR + B8h
Input Stream[2]: HDBAR + D8h
Input Stream[3]: HDBAR + F8h
Output Stream[0]: HDBAR + 118h
Output Stream[1]: HDBAR + 138h
Output Stream[2]: HDBAR + 158h
Output Stream[3]: HDBAR + 178h

Attribute: R/W,RO

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:7	**Buffer Descriptor List Pointer Lower Base Address** — R/W. Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.
6:0	Hardwired to 0 forcing alignment on 128-B boundaries.

18.2.44 SDBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 9Ch
Input Stream[1]: HDBAR + BCh
Input Stream[2]: HDBAR + DCh
Input Stream[3]: HDBAR + FCh
Output Stream[0]: HDBAR + 11Ch
Output Stream[1]: HDBAR + 13Ch
Output Stream[2]: HDBAR + 15Ch
Output Stream[3]: HDBAR + 17Ch

Attribute: R/W

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Buffer Descriptor List Pointer Upper Base Address** — R/W. Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.

§ §

19 SMBus Controller Registers (D31:F3)

19.1 PCI Configuration Registers (SMBus—D31:F3)

Table 19-1. SMBus Controller PCI Register Address Map (SMBus—D31:F3)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0280h	RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	05h	RO
0Bh	BCC	Base Class Code	0Ch	RO
10h	SMBMBAR0	Memory Base Address Register 0 (Bit 31:0)	00000004h	R/W
14h	SMBMBAR1	Memory Based Address Register 1 (Bit 63:32)	00000000h	R/W
20h–23h	SMB_BASE	SMBus Base Address	00000001h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	RO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h	HOSTC	Host Configuration	00h	R/W

NOTE: Registers that are not shown should be treated as Reserved (See Section 9.2 for details).

19.1.1 VID—Vendor Identification Register (SMBus—D31:F3)

Address: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel

19.1.2 DID—Device Identification Register (SMBus—D31:F3)

Address: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 SMBus controller. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Device ID Register.

19.1.3 PCICMD—PCI Command Register (SMBus—D31:F3)

Address: 04h–05h Attributes: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. 0 = Enable 1 = Disables SMBus to assert its PIRQB# signal.
9	Fast Back to Back Enable (FBE) — RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)** — R/W. 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7	Wait Cycle Control (WCC) — RO. Hardwired to 0.
6	**Parity Error Response (PER)** — R/W. 0 = Disable 1 = Sets Detected Parity Error bit (D31:F3:06, bit 15) when a parity error is detected.
5	VGA Palette Snoop (VPS) — RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE) — RO. Hardwired to 0.
3	Special Cycle Enable (SCE) — RO. Hardwired to 0.
2	Bus Master Enable (BME) — RO. Hardwired to 0.
1	**Memory Space Enable (MSE)** — R/W. 0 = Disables memory mapped config space. 1 = Enables memory mapped config space.
0	**I/O Space Enable (IOSE)** — R/W. 0 = Disable 1 = Enables access to the SMBus I/O space registers as defined by the Base Address Register.

19.1.4 PCISTS—PCI Status Register (SMBus—D31:F3)

Address:	06h–07h	Attributes:	RO
Default Value:	0280h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected. 1 = Parity error detected.
14	**Signaled System Error (SSE)** — R/WC. 0 = No system error detected. 1 = System error detected.
13	Received Master Abort (RMA) — RO. Hardwired to 0.
12	Received Target Abort (RTA) — RO. Hardwired to 0.
11	**Signaled Target Abort (STA)** — RO. Hardwired to 0.
10:9	**DEVSEL# Timing Status** (DEVT) — RO. This 2-bit field defines the timing for DEVSEL# assertion for positive decode. 01 = Medium timing.
8	Data Parity Error Detected (DPED) — RO. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC) — RO. Hardwired to 1.
6	User Definable Features (UDF) — RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP) — RO. Hardwired to 0.
4	Capabilities List (CAP_LIST) — RO. Hardwired to 0 because there are no capability list structures in this function
3	**Interrupt Status (INTS)** — RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

19.1.5 RID—Revision Identification Register (SMBus—D31:F3)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register.

19.1.6 PI—Programming Interface Register (SMBus—D31:F3)

Offset Address: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Reserved

19.1.7 SCC—Sub Class Code Register (SMBus—D31:F3)

Address Offset: 0Ah
Default Value: 05h
Attributes: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code** (SCC) — RO. 05h = SMBus serial controller

19.1.8 BCC—Base Class Code Register (SMBus—D31:F3)

Address Offset: 0Bh
Default Value: 0Ch
Attributes: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code** (BCC) — RO. 0Ch = Serial controller.

19.1.9 SMBMBAR0—D31_F3_SMBus Memory Base Address 0 (SMBus—D31:F3)

Address Offset: 10-13h
Default Value: 00000004h
Attributes: R/W, RO
Size: 32 bits

Bit	Description
31:8	**Base Address** — R/W. Provides the 32 byte system memory base address for the Intel ICH10 SMB logic.
7:4	Reserved
3	Prefetchable (PREF) — RO. Hardwired to 0. Indicates that SMBMBAR is not pre-fetchable.
2:1	**Address Range (ADDRNG)** — RO. Indicates that this SMBMBAR can be located anywhere in 64 bit address space. Hardwired to 10b.
0	**Memory Space Indicator** — RO. This read-only bit always is 0, indicating that the SMB logic is Memory mapped.

19.1.10 SMBMBAR1—D31_F3_SMBus Memory Base Address 1 (SMBus—D31:F3)

Address Offset:	14h-17h	Attributes:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Base Address** — R/W. Provides bits 63-32 system memory base address for the Intel ICH10 SMB logic.

19.1.11 SMB_BASE—SMBus Base Address Register (SMBus—D31:F3)

Address Offset:	20–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32-bits

Bit	Description
31:16	Reserved — RO
15:5	**Base Address** — R/W. This field provides the 32-byte system I/O base address for the ICH10 SMB logic.
4:1	Reserved — RO
0	IO Space Indicator — RO. Hardwired to 1 indicating that the SMB logic is I/O mapped.

19.1.12 SVID—Subsystem Vendor Identification Register (SMBus—D31:F2/F4)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID)** — RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SVID register. **NOTE:** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

19.1.13 SID—Subsystem Identification Register (SMBus—D31:F2/F4)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID (SID)** — R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SID register. **NOTE:** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

19.1.14 INT_LN—Interrupt Line Register (SMBus—D31:F3)

Address Offset:	3Ch	Attributes:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)** — R/W. This data is not used by the ICH10. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

19.1.15 INT_PN—Interrupt Pin Register (SMBus—D31:F3)

Address Offset:	3Dh	Attributes:	RO
Default Value:	See description	Size:	8 bits

Bit	Description
7:0	**Interrupt PIN (INT_PN)** — RO. This reflects the value of D31IP.SMIP in chipset configuration space.

19.1.16 HOSTC—Host Configuration Register (SMBus—D31:F3)

Address Offset: 40h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved
3	**SSRESET - Soft SMBus Reset**— R/W. 0 = The HW will reset this bit to 0 when SMBus reset operation is completed. 1 = The SMBus state machine and logic in ICH10 is reset.
2	**I^{2}C_EN** — R/W. 0 = SMBus behavior. 1 = The ICH10 is enabled to communicate with I^{2}C devices. This will change the formatting of some commands.
1	**SMB_SMI_EN** — R/W. 0 = SMBus interrupts will not generate an SMI#. 1 = Any source of an SMB interrupt will instead be routed to generate an SMI#. Refer to Section 5.20.4 (Interrupts / SMI#). This bit needs to be set for SMBALERT# to be enabled.
0	**SMBus Host Enable (HST_EN)** — R/W. 0 = Disable the SMBus Host controller. 1 = Enable. The SMB Host controller interface is enabled to execute commands. The INTREN bit (offset SMBASE + 02h, bit 0) needs to be enabled for the SMB Host controller to interrupt or SMI#. Note that the SMB Host controller will not respond to any new requests until all interrupt requests have been cleared.

19.2 SMBus I/O and Memory Mapped I/O Registers

The following SMBus registers can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Table 19-2. SMBus I/O and Memory Mapped I/O Register Address Map

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W
07h	HOST_BLOCK_DB	Host Block Data Byte	00h	R/W
08h	PEC	Packet Error Check	00h	R/W
09h	RCV_SLVA	Receive Slave Address	44h	R/W
0Ah–0Bh	SLV_DATA	Receive Slave Data	0000h	RO
0Ch	AUX_STS	Auxiliary Status	00h	R/WC, RO
0Dh	AUX_CTL	Auxiliary Control	00h	R/W
0Eh	SMLINK_PIN_CTL	SMLink Pin Control (TCO Compatible Mode)	See register description	R/W, RO
0Fh	SMBus_PIN_CTL	SMBus Pin Control	See register description	R/W, RO
10h	SLV_STS	Slave Status	00h	R/WC
11h	SLV_CMD	Slave Command	00h	R/W
14h	NOTIFY_DADDR	Notify Device Address	00h	RO
16h	NOTIFY_DLOW	Notify Data Low Byte	00h	RO
17h	NOTIFY_DHIGH	Notify Data High Byte	00h	RO

19.2.1 HST_STS—Host Status Register (SMBus—D31:F3)

Register Offset: SMBASE + 00h
Default Value: 00h
Attribute: R/WC, RO
Size: 8-bits

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a 0 to any bit position has no effect.

Bit	Description
7	**Byte Done Status (DS)** — R/WC. 0 = Software can clear this by writing a 1 to it. 1 = Host controller received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. This bit is not set when transmission is due to the LAN interface heartbeat. This bit has no meaning for block transfers when the 32-byte buffer is enabled. **NOTE:** When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the DS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the ICH10 will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases. When not using the 32 Byte Buffer, hardware will drive the SMBCLK signal low when the DS bit is set until SW clears the bit. This includes the last byte of a transfer. Software must clear the DS bit before it can clear the BUSY bit.
6	**INUSE_STS** — R/W. This bit is used as semaphore among various independent software threads that may need to use the ICH10's SMBus logic, and has no other effect on hardware. 0 = After a full PCI reset, a read to this bit returns a 0. 1 = After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller.
5	**SMBALERT_STS** — R/WC. 0 = Interrupt or SMI# was not generated by SMBALERT#. Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was the SMBALERT# signal. This bit is only cleared by software writing a 1 to the bit position or by RSMRST# going low. If the signal is programmed as a GPIO, then this bit will never be set.
4	**FAILED** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction.
3	**BUS_ERR** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt of SMI# was a transaction collision.
2	**DEV_ERR** — R/WC. 0 = Software clears this bit by writing a 1 to it. The ICH10 will then deassert the interrupt or SMI#. 1 = The source of the interrupt or SMI# was due to one of the following: • Invalid Command Field, • Unclaimed Cycle (host initiated), • Host Device Time-out Error.

Bit	Description
1	**INTR** — R/WC. This bit can only be set by termination of a command. INTR is not dependent on the INTREN bit (offset SMBASE + 02h, bit 0) of the Host controller register (offset 02h). It is only dependent on the termination of the command. If the INTREN bit is not set, then the INTR bit will be set, although the interrupt will not be generated. Software can poll the INTR bit in this non-interrupt case. 0 = Software clears this bit by writing a 1 to it. The ICH10 then deasserts the interrupt or SMI#. 1 = The source of the interrupt or SMI# was the successful completion of its last command.
0	**HOST_BUSY** — R/WC. 0 = Cleared by the ICH10 when the current transaction is completed. 1 = Indicates that the ICH10 is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE Register. The BLOCK DATA BYTE Register can be accessed when this bit is set only when the SMB_CMD bits in the Host Control Register are programmed for Block command or I^2C Read command. This is necessary in order to check the DONE_STS bit.

19.2.2 HST_CNT—Host Control Register (SMBus—D31:F3)

Register Offset:	SMBASE + 02h	Attribute:	R/W, WO
Default Value:	00h	Size:	8-bits

Note: A read to this register will clear the byte pointer of the 32-byte buffer.

Bit	Description
7	**PEC_EN**. — R/W. 0 = SMBus host controller does not perform the transaction with the PEC phase appended. 1 = Causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. This bit must be written prior to the write in which the **START** bit is set.
6	**START** — WO. 0 = This bit will always return 0 on reads. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel® ICH10 has finished the command. 1 = Writing a 1 to this bit initiates the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position.
5	**LAST_BYTE** — WO. This bit is used for Block Read commands. 1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the ICH10 to send a NACK (instead of an ACK) after receiving the last byte. **NOTE:** Once the SECOND_TO_STS bit in TCO2_STS register (D31:F0, TCOBASE+6h, bit 1) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the ICH10 from running some of the SMBus commands (Block Read/Write, I^2C Read, Block I^2C Write).

Bit	Description
4:2	**SMB_CMD** — R/W. The bit encoding below indicates which command the ICH10 is to perform. If enabled, the ICH10 will generate an interrupt or SMI# when the command has completed If the value is for a non-supported or reserved command, the ICH10 will set the device error (DEV_ERR) status bit (offset SMBASE + 00h, bit 2) and generate an interrupt when the START bit is set. The ICH10 will perform no command, and will not operate until DEV_ERR is cleared. 000 = **Quick**: The slave address and read/write value (bit 0) are stored in the transmit slave address register. 001 = **Byte**: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 = **Byte Data**: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 = **Word Data**: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes, the DATA0 and DATA1 registers will contain the read data. 100 = **Process Call:** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 = **Block**: This command uses the transmit slave address, command, DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 = **I^2C Read**: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The ICH10 continues reading data until the NAK is received. 111 **=** **Block Process:** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **NOTE:** E32B bit in the Auxiliary Control register must be set for this command to work.
1	**KILL** — R/W. 0 = Normal SMBus host controller functionality. 1 = Kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus host controller to function normally.
0	**INTREN** — R/W. 0 = Disable. 1 = Enable the generation of an interrupt or SMI# upon the completion of the command.

19.2.3 HST_CMD—Host Command Register (SMBus—D31:F3)

Register Offset: SMBASE + 03h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	This 8-bit field is transmitted by the host controller in the command field of the SMBus protocol during the execution of any command.

19.2.4 XMIT_SLVA—Transmit Slave Address Register (SMBus—D31:F3)

Register Offset: SMBASE + 04h Attribute: R/W
Default Value: 00h Size: 8 bits

This register is transmitted by the host controller in the slave address field of the SMBus protocol.

Bit	Description
7:1	**Address** — R/W. This field provides a 7-bit address of the targeted slave.
0	**RW** — R/W. Direction of the host transfer. 0 = Write 1 = Read

19.2.5 HST_D0—Host Data 0 Register (SMBus—D31:F3)

Register Offset: SMBASE + 05h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Data0 / Count** — R/W. This field contains the 8-bit data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log invalid block counts.

19.2.6 HST_D1—Host Data 1 Register (SMBus—D31:F3)

Register Offset: SMBASE + 06h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Data1** — R/W. This 8-bit register is transmitted in the DATA1 field of the SMBus protocol during the execution of any command.

19.2.7 Host_BLOCK_DB—Host Block Data Byte Register (SMBus—D31:F3)

Register Offset: SMBASE + 07h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Block Data (BDTA)** — R/W. This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit (offset SMBASE + 0Dh, bit 1) is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the ICH3. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

19.2.8 PEC—Packet Error Check (PEC) Register (SMBus—D31:F3)

Register Offset: SMBASE + 08h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**PEC_DATA** — R/W. This 8-bit register is written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

19.2.9 RCV_SLVA—Receive Slave Address Register (SMBus—D31:F3)

Register Offset:	SMBASE + 09h	Attribute:	R/W
Default Value:	44h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7	Reserved
6:0	**SLAVE_ADDR** — R/W. This field is the slave address that the Intel® ICH10 decodes for read and write cycles. the default is not 0, so the SMBus Slave Interface can respond even before the processor comes up (or if the processor is dead). This register is cleared by RSMRST#, but not by PLTRST#.

19.2.10 SLV_DATA—Receive Slave Data Register (SMBus—D31:F3)

Register Offset:	SMBASE + 0Ah–0Bh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume

This register contains the 16-bit data value written by the external SMBus master. The processor can then read the value from this register. This register is reset by RSMRST#, but not PLTRST#

Bit	Description
15:8	**Data Message Byte 1 (DATA_MSG1)** — RO. See Section 5.20.7 for a discussion of this field.
7:0	**Data Message Byte 0 (DATA_MSG0)** — RO. See Section 5.20.7 for a discussion of this field.

19.2.11 AUX_STS—Auxiliary Status Register (SMBus—D31:F3)

Register Offset:	SMBASE + 0Ch	Attribute:	R/WC, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**SMBus TCO Mode (STCO)** — RO. This bit reflects the strap setting of TCO compatible mode vs. Advanced TCO mode. 0 = Intel® ICH10 is in the compatible TCO mode. 1 = ICH10 is in the advanced TCO mode.
0	**CRC Error (CRCE)** — R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after the ICH10 has received the final data bit transmitted by an external slave.

19.2.12 AUX_CTL—Auxiliary Control Register (SMBus—D31:F3)

Register Offset:	SMBASE + 0Dh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**Enable 32-Byte Buffer (E32B)** — R/W. 0 = Disable. 1 = Enable. When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the ICH10 generates an interrupt.
0	**Automatically Append CRC (AAC)** — R/W. 0 = ICH10 will Not automatically append the CRC. 1 = The ICH10 will automatically append the CRC. This bit must not be changed during SMBus transactions or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

19.2.13 SMLINK_PIN_CTL—SMLink Pin Control Register (SMBus—D31:F3)

Register Offset:	SMBASE + 0Eh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

This register is only applicable in the TCO compatible mode.

Bit	Description
7:3	Reserved
2	**SMLINK_CLK_CTL** — R/W. 0 = ICH10 will drive the SMLINK0 pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK0 pin. 1 = The SMLINK0 pin is **not** overdriven low. The other SMLINK logic controls the state of the pin. (Default)
1	**SMLINK1_CUR_STS** — RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK1 pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SMLINK0_CUR_STS** — RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK0 pin. This allows software to read the current state of the pin. 0 = Low 1 = High

19.2.14 SMBus_PIN_CTL—SMBus Pin Control Register (SMBus—D31:F3)

Register Offset:	SMBASE + 0Fh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved
2	**SMBCLK_CTL** — R/W. 1 = The SMBCLK pin is **not** overdriven low. The other SMBus logic controls the state of the pin. 0 = ICH10 drives the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. (Default)
1	**SMBDATA_CUR_STS** — RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBDATA pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SMBCLK_CUR_STS** — RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBCLK pin. This allows software to read the current state of the pin. 0 = Low 1 = High

19.2.15 SLV_STS—Slave Status Register (SMBus—D31:F3)

Register Offset:	SMBASE + 10h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll this register until a write takes effect before assuming that a write has completed internally.

Bit	Description
7:1	Reserved
0	**HOST_NOTIFY_STS** — R/WC. The ICH10 sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMlink (Consumer Only) or SMBus pins (Corporate Only). Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the ICH10 will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the ICH10 will NACK the first byte (host address) of any new “Host Notify” commands on the SMlink (Consumer Only) or SMBus pins (Corporate Only). Writing a 0 to this bit has no effect.

19.2.16 SLV_CMD—Slave Command Register (SMBus—D31:F3)

Register Offset: SMBASE + 11h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:2	Reserved
2	**SMBALERT_DIS** — R/W. 0 = Allows the generation of the interrupt or SMI#. 1 = Software sets this bit to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit (offset SMBASE + 00h, bit 5). The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	**HOST_NOTIFY_WKEN** — R/W. Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is “OR’d" in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register. 0 = Disable 1 = Enable
0	**HOST_NOTIFY_INTREN** — R/W. Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS (offset SMBASE + 10h, bit 0) is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB# or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31:F3:40h, bit 1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by AND’ing the STS and INTREN bits. 0 = Disable 1 = Enable

19.2.17 NOTIFY_DADDR—Notify Device Address Register (SMBus—D31:F3)

Register Offset: SMBASE + 14h
Default Value: 00h
Attribute: RO
Size: 8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:1	**DEVICE_ADDRESS** — RO. This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.
0	Reserved

19.2.18 NOTIFY_DLOW—Notify Data Low Byte Register (SMBus—D31:F3)

Register Offset:	SMBASE + 16h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_LOW_BYTE** — RO. This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.

19.2.19 NOTIFY_DHIGH—Notify Data High Byte Register (SMBus—D31:F3)

Register Offset:	SMBASE + 17h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_HIGH_BYTE** — RO. This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMBASE +10, bit 0) is set to 1.

§ §

20 PCI Express* Configuration Registers

20.1 PCI Express* Configuration Registers (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Note: Register address locations that are not shown in Table 20-1 and should be treated as Reserved.

Table 20-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Function 0–5 Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	04h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	81h	RO
18h–1Ah	BNUM	Bus Number	000000h	R/W
1Bh	SLT	Secondary Latency Timer	00h	RO
1Ch–1Dh	IOBL	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SSTS	Secondary Status Register	0000h	R/WC
20h–23h	MBL	Memory Base and Limit	00000000h	R/W
24h–27h	PMBL	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Base Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capabilities List Pointer	40h	RO
3Ch–3Dh	INTR	Interrupt Information	See bit description	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control Register	0000h	R/W
40h–41h	CLIST	Capabilities List	8010	RO

Table 20-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Function 0–5 Default	Type
42h–43h	XCAP	PCI Express* Capabilities	0041	R/WO, RO
44h–47h	DCAP	Device Capabilities	00000FE0h	RO
48h–49h	DCTL	Device Control	0000h	R/W, RO
4Ah–4Bh	DSTS	Device Status	0010h	R/WC, RO
4Ch–4Fh	LCAP	Link Capabilities	See bit description	R/W, RO, R/WO
50h–51h	LCTL	Link Control	0000h	R/W, WO, RO
52h–53h	LSTS	Link Status	See bit description	RO
54h–57h	SLCAP	Slot Capabilities Register	00000060h	R/WO, RO
58h–59h	SLCTL	Slot Control	0000h	R/W, RO
5Ah–5Bh	SLSTS	Slot Status	0000h	R/WC, RO
5Ch–5Dh	RCTL	Root Control	0000h	R/W
60h–63h	RSTS	Root Status	00000000h	R/WC, RO
64h-67h (Corporate Only)	DCAP2	Device Capabilities 2 Register	00000016h	RO
68h–69h (Corporate Only)	DCTL2	Device Control 2 Register	0000h	R/W, RO
70h–71h (Corporate Only)	LCTL2	Link Control 2 Register	0001h	RO
80h–81h	MID	Message Signaled Interrupt Identifiers	9005h	RO
82h–83h	MC	Message Signaled Interrupt Message Control	0000h	R/W, RO
84h–87h	MA	Message Signaled Interrupt Message Address	00000000h	R/W
88h–89h	MD	Message Signaled Interrupt Message Data	0000h	R/W
90h–91h	SVCAP	Subsystem Vendor Capability	A00Dh	RO
94h–97h	SVID	Subsystem Vendor Identification	00000000h	R/WO
A0h–A1h	PMCAP	Power Management Capability	0001h	RO
A2h–A3h	PMC	PCI Power Management Capability	C802h	RO
A4–A7h	PMCS	PCI Power Management Control and Status	00000000h	R/W, RO
D4-D7h	MPC2	Miscellaneous Port Configuration 2	00000000h	R/W, RO
D8–DBh	MPC	Miscellaneous Port Configuration	08110000h	R/W

Table 20-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Function 0–5 Default	Type
DC–DFh	SMSCS	SMI/SCI Status Register	00000000h	R/WC
E1h	RPDCGEN	Rort Port Dynamic Clock Gating Enable	00h	R/W
E8-EBh	PECR1	PCI Express Configuration Register 1	00000020h	R/W
100–103h	VCH	Virtual Channel Capability Header	18010002h	R/WO
104h–107h	—	Reserved	—	—
108h–10Bh	VCAP2	Virtual Channel Capability 2	00000001h	RO
10Ch–10Dh	PVC	Port Virtual Channel Control	0000h	R/W
10Eh–10Fh	PVS	Port Virtual Channel Status	0000h	RO
110h–113h	V0CAP	Virtual Channel 0 Resource Capability	00000001h	RO
114–117h	V0CTL	Virtual Channel 0 Resource Control	800000FFh	R/W, RO
11A–11Bh	V0STS	Virtual Channel 0 Resource Status	0000h	RO
11Ch–143h	—	Reserved	—	—
144h–147h	UES	Uncorrectable Error Status	See bit description	R/WC, RO
148h–14Bh	UEM	Uncorrectable Error Mask	00000000h	R/WO, RO
14Ch–14Fh	UEV	Uncorrectable Error Severity	00060011h	RO
150h–153h	CES	Correctable Error Status	00000000h	R/WC
154h–157h	CEM	Correctable Error Mask	00000000h	R/WO
158h–15Bh	AECC	Advanced Error Capabilities and Control	00000000h	RO
170h–173h	RES	Root Error Status	00000000h	R/WC, RO
180h–183h	RCTCL	Root Complex Topology Capability List	00010005h	RO
184h–187h	ESD	Element Self Description	See bit description	RO
190h–193h	ULD	Upstream Link Description	00000001h	RO
198h–19Fh	ULBA	Upstream Link Base Address	See bit description	RO
300-303h	PECR2	PCI Express Configuration Register 2	60005007h	R/W
318h	PEETM	PCI Express Extended Test Mode Register	See bit description	RO
324h–327h	PEC1	PCI Express Configuration Register 1	00000000h	RO, R/W

20.1.1 VID—Vendor Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel

20.1.2 DID—Device Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 02h–03h
Default Value: Port 1= Bit Description
Port 2= Bit Description
Port 3= Bit Description
Port 4= Bit Description
Port 5= Bit Description
Port 6= Bit Description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID** — RO. This is a 16-bit value assigned to the Intel® ICH10 PCI Express controller. Refer to the *Intel® I/O Controller Hub (ICH10) Family* for the value of the Device ID Register

20.1.3 PCICMD—PCI Command Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable** — R/W. This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE) — Reserved per the *PCI Express* Base Specification*.
8	**SERR# Enable (SEE)** — R/W. 0 = Disable. 1 = Enables the root port to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC) — Reserved per the *PCI Express Base Specification*.
6	**Parity Error Response (PER)** — R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	VGA Palette Snoop (VPS) — Reserved per the *PCI Express* Base Specification*.
4	Postable Memory Write Enable (PMWE) — Reserved per the *PCI Express* Base Specification*.
3	Special Cycle Enable (SCE) — Reserved per the *PCI Express* Base Specification*.
2	**Bus Master Enable (BME)** — R/W. 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a PCI Express* device.
1	**Memory Space Enable (MSE)** — R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express device.
0	**I/O Space Enable (IOSE)** — R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express device.

20.1.4 PCISTS—PCI Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 06h–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is not set.
14	**Signaled System Error (SSE)** — R/WC. 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	**Received Master Abort (RMA)** — R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the root port receives a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)** — R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the root port receives a completion with completer abort from the backbone.
11	**Signaled Target Abort (STA)** — R/WC. 0 = No target abort received. 1 = Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS) — Reserved per the *PCI Express* Base Specification*.
8	**Master Data Parity Error Detected (DPED)** — R/WC. 0 = No data parity error received. 1 = Set when the root port receives a completion with a data parity error on the backbone and PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is set.
7	Fast Back to Back Capable (FB2BC) — Reserved per the *PCI Express* Base Specification*.
6	Reserved
5	66 MHz Capable — Reserved per the *PCI Express* Base Specification*.
4	**Capabilities List** — RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status** — RO. Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D28:F0/F1/F2/F3/F4/F5:04h:bit 10).
2:0	Reserved

20.1.5 RID—Revision Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID** — RO. Refer to the *Intel® I/O Controller Hub (ICH10) Family Specification Update* for the value of the Revision ID Register

20.1.6 PI—Programming Interface Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface** — RO. 00h = No specific register level programming interface defined.

20.1.7 SCC—Sub Class Code Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Ah Attribute: RO
Default Value: 04h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** — RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 04h = PCI-to-PCI bridge. 00h = Host Bridge.

20.1.8 BCC—Base Class Code Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Bh Attribute: RO
Default Value: 06h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. 06h = Indicates the device is a bridge device.

20.1.9 CLS—Cache Line Size Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Cache Line Size (CLS)** — R/W. This is read/write but contains no functionality, per the *PCI Express* Base Specification*.

20.1.10 PLT—Primary Latency Timer Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:3	Latency Count. Reserved per the *PCI Express* Base Specification.*
2:0	Reserved

20.1.11 HEADTYP—Header Type Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Eh
Default Value: 81h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device** — RO. 0 = Single-function device. 1 = Multi-function device.
6:0	**Configuration Layout**— RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 00h = Indicates a Host Bridge. 01h = Indicates a PCI-to-PCI bridge.

20.1.12 BNUM—Bus Number Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 18–1Ah
Default Value: 000000h
Attribute: R/W
Size: 24 bits

Bit	Description
23:16	**Subordinate Bus Number (SBBN)** — R/W. Indicates the highest PCI bus number below the bridge.
15:8	**Secondary Bus Number (SCBN)** — R/W. Indicates the bus number the port.
7:0	**Primary Bus Number (PBN)** — R/W. Indicates the bus number of the backbone.

20.1.13 SLT—Secondary Latency Timer (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Bh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Secondary Latency Timer — Reserved for a Root Port per the *PCI Express* Base Specification*.

20.1.14 IOBL—I/O Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Ch–1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:12	**I/O Limit Address (IOLA)** — R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	**I/O Limit Address Capability (IOLC)** — R/O. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	**I/O Base Address (IOBA)** — R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Base Address Capability (IOBC)** — R/O. Indicates that the bridge does not support 32-bit I/O addressing.

20.1.15 SSTS—Secondary Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Eh–1Fh
Default Value: 0000h
Attribute: R/WC
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. 0 = No error. 1 = The port received a poisoned TLP.
14	**Received System Error (RSE)** — R/WC. 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	**Received Master Abort (RMA)** — R/WC. 0 = Unsupported Request not received. 1 = The port received a completion with “Unsupported Request” status from the device.
12	**Received Target Abort (RTA)** — R/WC. 0 = Completion Abort not received. 1 = The port received a completion with “Completion Abort” status from the device.
11	**Signaled Target Abort (STA)** — R/WC. 0 = Completion Abort not sent. 1 = The port generated a completion with “Completion Abort” status to the device.
10:9	Secondary DEVSEL# Timing Status (SDTS): Reserved per *PCI Express* Base Specification*.
8	**Data Parity Error Detected (DPD)** — R/WC. 0 = Conditions below did not occur. 1 = Set when the BCTRL.PERE (D28:FO/F1/F2/F3/F4/F5:3E: bit 0) is set, and either of the following two conditions occurs: • Port receives completion marked poisoned. • Port poisons a write request to the secondary side.
7	Secondary Fast Back to Back Capable (SFBC): Reserved per *PCI Express* Base Specification*.
6	Reserved
5	Secondary 66 MHz Capable (SC66): Reserved per *PCI Express* Base Specification*.
4:0	Reserved

20.1.16 MBL—Memory Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 20h–23h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5:04:bit 1) is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5:04:bit 2) is set. The comparison performed is MB ≥ AD[31:20] ≤ ML.

Bit	Description
31:20	**Memory Limit (ML)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
19:16	Reserved
15:4	**Memory Base (MB)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	Reserved

20.1.17 PMBL—Prefetchable Memory Base and Limit Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 24h–27h
Default Value: 00010001h
Attribute: R/W, RO
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5;04, bit 1) is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5;04, bit 2) is set. The comparison performed is PMBU32:PMB ≥ AD[63:32]:AD[31:20] ≤ PMLU32:PML.

Bit	Description
31:20	**Prefetchable Memory Limit (PML)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
19:16	**64-bit Indicator (I64L)** — RO. Indicates support for 64-bit addressing
15:4	**Prefetchable Memory Base (PMB)** — R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	**64-bit Indicator (I64B)** — RO. Indicates support for 64-bit addressing

20.1.18 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 28h–2Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)** — R/W. Upper 32-bits of the prefetchable address base.

20.1.19 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 2Ch–2Fh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)** — R/W. Upper 32-bits of the prefetchable address limit.

20.1.20 CAPP—Capabilities List Pointer Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 34h
Default Value: 40h
Attribute: R0
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)** — RO. Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

20.1.21 INTR—Interrupt Information Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 3Ch–3Dh
Default Value: See bit description
Function Level Reset: No (Bits 7:0 only)
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)** — RO. Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the D28IP register in chipset config space: **Port** — **Reset Value** 1 — D28IP.P1IP 2 — D28IP.P2IP 3 — D28IP.P3IP 4 — D28IP.P4IP 5 — D28IP.P5IP **NOTE:** The value that is programmed into D28IP is always reflected in this register.
7:0	**Interrupt Line (ILINE)** — R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.

20.1.22 BCTRL—Bridge Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 3Eh–3Fh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	Reserved
11	Discard Timer SERR# Enable (DTSE): Reserved per *PCI Express* Base Specification,* Revision 1.0a
10	Discard Timer Status (DTS): Reserved per *PCI Express* Base Specification,* Revision 1.0a.
9	Secondary Discard Timer (SDT): Reserved per *PCI Express* Base Specification,* Revision 1.0a.
8	Primary Discard Timer (PDT): Reserved per *PCI Express* Base Specification,* Revision 1.0a.
7	Fast Back to Back Enable (FBE): Reserved per *PCI Express* Base Specification,* Revision 1.0a.
6	**Secondary Bus Reset (SBR)** — R/W. Triggers a hot reset on the PCI Express* port.
5	Master Abort Mode (MAM): Reserved per Express specification.
4	**VGA 16-Bit Decode (V16)** — R/W. 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled, and only the base I/O ranges can be decoded
3	**VGA Enable (VE)**— R/W. 0 = The ranges below will not be claimed off the backbone by the root port. 1 = The following ranges will be claimed off the backbone by the root port: • Memory ranges A0000h-BFFFFh • I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1s
2	**ISA Enable (IE)** — R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = The root port will not block any forwarding from the backbone as described below. 1 = The root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SE)** — R/W. 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	**Parity Error Response Enable (PERE)** — R/W. 0 = Poisoned write TLPs and completions indicating poisoned TLPs will not set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5:1E, bit 8). 1 = Poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5:1E, bit 8).

20.1.23 CLIST—Capabilities List Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 40–41h
Default Value: 8010h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Value of 80h indicates the location of the next pointer.
7:0	**Capability ID (CID)** — RO. Indicates this is a PCI Express* capability.

20.1.24 XCAP—PCI Express* Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 42h–43h
Default Value: 0041h
Attribute: R/WO, RO
Size: 16 bits

Bit	Description
15:14	Reserved
13:9	**Interrupt Message Number (IMN)** — RO. The Intel® ICH10 does not have multiple MSI interrupt numbers.
8	**Slot Implemented (SI)** — R/WO. Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	**Device / Port Type (DT)** — RO. Indicates this is a PCI Express* root port.
3:0	**Capability Version (CV)** — RO. Indicates PCI Express 1.0.

20.1.25 DCAP—Device Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 44h–47h
Default Value: 00008FC0h
Attribute: RO
Size: 32 bits

Bit	Description
31:28	Reserved
27:26	Captured Slot Power Limit Scale (CSPS) — RO. Not supported.
25:18	Captured Slot Power Limit Value (CSPV) — RO. Not supported.
17:16	Reserved
15	**Role Based Error Reporting (RBER)** — RO. Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	Reserved
11:9	Endpoint L1 Acceptable Latency (E1AL) — RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 1.1 Spec.
8:6	Endpoint L0s Acceptable Latency (E0AL) — RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 1.1 Spec.
5	**Extended Tag Field Supported (ETFS)** — RO. Indicates that 8-bit tag fields are supported.
4:3	**Phantom Functions Supported (PFS)** — RO. No phantom functions supported.
2:0	**Max Payload Size Supported (MPS)** — RO. Indicates the maximum payload size supported is 128B.

20.1.26 DCTL—Device Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 48h–49h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15	Reserved
14:12	Max Read Request Size (MRRS) — RO. Hardwired to 0.
11	Enable No Snoop (ENS) — RO. Not supported. The root port will never issue non-snoop requests.
10	**Aux Power PM Enable (APME)** — R/W. The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	Phantom Functions Enable (PFE) — RO. Not supported.
8	Extended Tag Field Enable (ETFE) — RO. Not supported.
7:5	**Max Payload Size (MPS)** — R/W. The root port only supports 128-B payloads, regardless of the programming of this field.
4	Enable Relaxed Ordering (ERO) — RO. Not supported.
3	**Unsupported Request Reporting Enable (URE)** — R/W. 0 = The root port will ignore unsupported request errors. 1 = Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	**Fatal Error Reporting Enable (FEE)** — R/W. 0 = The root port will ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	**Non-Fatal Error Reporting Enable (NFE)** — R/W. 0 = The root port will ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	**Correctable Error Reporting Enable (CEE)** — R/W. 0 = The root port will ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

20.1.27 DSTS—Device Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 4Ah–4Bh
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending (TDP)** — RO. This bit has no meaning for the root port since only one transaction may be pending to the Intel® ICH10, so a read of this bit cannot occur until it has already returned to 0.
4	**AUX Power Detected (APD)** — RO. The root port contains AUX power for wakeup.
3	**Unsupported Request Detected (URD)** — R/WC. Indicates an unsupported request was detected.
2	**Fatal Error Detected (FED)** — R/WC. Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	**Non-Fatal Error Detected (NFED)** — R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	**Correctable Error Detected (CED)** — R/WC. Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

20.1.28 LCAP—Link Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 4Ch–4Fh
Default Value: See bit description
Attribute: R/WO, RO
Size: 32 bits

Bit	Description
31:24	**Port Number (PN)** — RO. Indicates the port number for the root port. This value is different for each implemented port: **Function** / **Port #** / **Value of PN Field** D28:F0 / 1 / 01h D28:F1 / 2 / 02h D28:F2 / 3 / 03h D28:F3 / 4 / 04h D28:F4 / 5 / 05h D28:F5 / 6 / 06h
23:22	Reserved
21 (Corporate Only)	**Link Bandwidth Notification Capability (LBNC) –** RO. 0 = Indicates root port can only support x1 link widths. 1 = Indicates root port can support link widths greater than x1. **NOTE:** Ports 1, 3, and 5 are required to set this bit. Ports 2, 4 and 6 can optionally set this bit.
21 (Consumer Only)	Reserved
20	**Link Active Reporting Capable (LARC)** — RO. Hardwired to 1 to indicate that this port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19:18	Reserved
17:15	**L1 Exit Latency (EL1)** — RO. Set to 010b to indicate an exit latency of 2 µs to 4 µs.
14:12	**L0s Exit Latency (EL0)** — RO. Indicates as exit latency based upon common-clock configuration. **LCLT.CCC** / **Value of EL0 (these bits)** 0 / MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18) 1 / MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15) **NOTE:** LCLT.CCC is at D28:F0/F1/F2/F3/F4/F5:50h:bit 6

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>11:10</td><td>Active State Link PM Support (APMS) — R/WO. Indicates what level of active state link power management is supported on the root port.

Bits — Definition
00b — Neither L0s nor L1 are supported
01b — L0s Entry Supported
10b — L1 Entry Supported
11b — Both L0s and L1 Entry Supported</td></tr>
<tr><td>9:4</td><td>Maximum Link Width (MLW) — RO. For the root ports, several values can be taken, based upon the value of the chipset config register field RPC.PC1 (Chipset Config Registers:Offset 0224h:bits1:0) for Ports 1-4 and RPC.PC2 (Chipset Config Registers:Offset 0224h:bits1:0) for Ports 5 and 6

Value of MLW Field
Port # — RPC.PC1=00b — RPC.PC1=11b
1 — 01h — 04h
2 — 01h — 01h
3 — 01h — 01h
4 — 01h — 01h
Port # — RPC.PC2=00b — RPC.PC2=11b
5 — 01h — N/A</td></tr>
<tr><td>3:0</td><td>Maximum Link Speed (MLS) — RO. Set to 1h to indicate the link speed is 2.5 Gb/s.</td></tr>
</table>

20.1.29 LCTL—Link Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 50h-51h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**Extended Synch (ES)** — R/W. 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	**Common Clock Configuration (CCC)** — R/W. 0 = The ICH10 and device are not using a common reference clock. 1 = The ICH10 and device are operating with a distributed common reference clock.
5	**Retrain Link (RL)** — R/W. 0 = This bit always returns 0 when read. 1 = The root port will train its downstream link. **NOTE:** Software uses LSTS.LT (D28:F0/F1/F2/F3/F4/F5:52, bit 11) to check the status of training. **NOTE:** It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that is already in progress.
4	**Link Disable (LD)** — R/W. 0 = Link enabled. 1 = The root port will disable the link.
3	**Read Completion Boundary Control (RCBC)** — RO. Indicates the read completion boundary is 64 bytes.
2	Reserved
1:0	**Active State Link PM Control (APMC)** — R/W. Indicates whether the root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled

20.1.30 LSTS—Link Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 52h–53h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:14	Reserved
13	**Data Link Layer Active (DLLA)** — RO. Default value is 0b. 0 = Data Link Control and Management State Machine is not in the DL_Active state 1 = Data Link Control and Management State Machine is in the DL_Active state
12	**Slot Clock Configuration (SCC)** — RO. Set to 1b to indicate that the Intel® ICH10 uses the same reference clock as on the platform and does not generate its own clock.
11	**Link Training (LT)** — RO. Default value is 0b. 0 = Link training completed. 1 = Link training is occurring.
10	Link Training Error (LTE) — RO. Not supported. Set value is 0b.
9:4	**Negotiated Link Width (NLW)** — RO. This field indicates the negotiated width of the given PCI Express* link. The contents of this NLW field is undefined if the link has not successfully trained. **Port #** — **Possible Values** 1 — 000001b, 000010b, 000100b 2 — 000001b 3 — 000001b 4 — 000001b 5 — 000001b, 000010b 6 — 000001b **NOTE:** 000001b = x1 link width, 000010b =x2 linkwidth, 000100b = x4 linkwidth
3:0	**Link Speed (LS)** — RO. This field indicates the negotiated Link speed of the given PCI Express* link. 01h = Link is 2.5 Gb/s.

20.1.31 SLCAP—Slot Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 54h–57h
Attribute: R/WO, RO
Default Value: 00000060h (Consumer Only)
00040060h (Corporate Only)
Size: 32 bits

Bit	Description
31:19	**Physical Slot Number (PSN)** — R/WO. This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	Reserved. Corporate Only 10h. Consumer Only 00h
16:15	**Slot Power Limit Scale (SLS)** — R/WO. Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	**Slot Power Limit Value (SLV)** — R/WO. Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	**Hot Plug Capable (HPC)** — R/WO. 1b = Indicates that Hot-Plug is supported.
5	**Hot Plug Surprise (HPS)** — R/WO. 1b = Indicates the device may be removed from the slot without prior notification.
4	**Power Indicator Present (PIP)** — RO. 0b = Indicates that a power indicator LED is not present for this slot.
3	**Attention Indicator Present (AIP)** — RO. 0b = Indicates that an attention indicator LED is not present for this slot.
2	**MRL Sensor Present (MSP)** — RO. 0b = Indicates that an MRL sensor is not present.
1	**Power Controller Present (PCP)** — RO. 0b = Indicates that a power controller is not implemented for this slot.
0	**Attention Button Present (ABP)** — RO. 0b = Indicates that an attention button is not implemented for this slot.

20.1.32 SLCTL—Slot Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 58h–59h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:13	Reserved
12	**Link Active Changed Enable (LACE)** — R/W. When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field (D28:F0/F1/F2/F3/F4/F5:52h:bit 13) is changed.
11	Reserved
10	**Power Controller Control (PCC)** — RO.This bit has no meaning for module based Hot-Plug.
9:6 (Corporate Only)	Reserved
9:8 (Consumer Only)	**Power Indicator Control (PIC)** — R/W. When read, the current state of the power indicator is returned. When written, the appropriate POWER_INDICATOR_* messages are sent. Defined encodings are: **Bits** **Definition** 00b Reserved 01b On 10b Blink 11b Off
7:6 (Consumer Only)	**Attention Indicator Control (AIC)** — R/W. When read, the current state of the attention indicator is returned. When written, the appropriate ATTENTION_INDICATOR_* messages are sent. Defined encodings are: **Bits** **Definition** 00b Reserved 01b On 10b Blink 11b Off
5	**Hot Plug Interrupt Enable (HPE)** — R/W. 0 = Hot plug interrupts based on Hot-Plug events is disabled. 1 = Enables generation of a Hot-Plug interrupt on enabled Hot-Plug events.
4 (Consumer Only)	**Command Completed Interrupt Enable (CCE)** — R/W. 0 = Hot plug interrupts based on command completions is disabled. 1 = Enables the generation of a Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
4 (Corporate Only)	Reserved
3	**Presence Detect Changed Enable (PDE)** — R/W. 0 = Hot plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a Hot-Plug interrupt or wake message when the presence detect logic changes state.

Bit	Description
2:1	Reserved.
0	**Attention Button Pressed Enable (ABE)** — R/W. When set, enables the generation of a Hot-Plug interrupt when the attention button is pressed. 0 = Hot plug interrupts based on the attention button being pressed is disabled. 1 = Enables the generation of a Hot-Plug interrupt when the attention button is pressed.

20.1.33 SLSTS—Slot Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 5Ah–5Bh
Default Value: 0000h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15:9	Reserved
8	**Link Active State Changed (LASC)** — R/WC. 1 = This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register (D28:F0/F1/F2/F3/F4/F5:52h:bit 13) is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	Reserved
6	**Presence Detect State (PDS)** — RO. If XCAP.SI (D28:F0/F1/F2/F3/F4/F5:42h:bit 8) is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if XCAP.SI is cleared, this bit is always set (1).
5	MRL Sensor State (MS) — Reserved as the MRL sensor is not implemented.
4 (Corporate Only)	Reserved
4 (Consumer Only)	**Command Completed (CC)** — R/WC. 0 = Issued command not completed. 1 = The Hot-Plug controller completed an issued command. This is set when the last message of a command is sent and indicates that software can write a new command to the slot controller.
3	**Presence Detect Changed (PDC)** — R/WC. 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	**MRL Sensor Changed (MSC)** — Reserved as the MRL sensor is not implemented.
1	**Power Fault Detected (PFD)** — Reserved as a power controller is not implemented.
0 (Corporate Only)	Reserved
0 (Consumer Only)	**Attention Button Pressed (ABP)** — R/WC. 0 = The attention button has not been pressed. 1 = The attention button is pressed.

20.1.34 RCTL—Root Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 5Ch–5Dh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:4	Reserved
3	**PME Interrupt Enable (PIE)** — R/W. 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when PCISTS.Inerrupt Status (D28:F0/F1/F2/F3/F4/F5:60h, bit 16) is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.IS already set).
2	**System Error on Fatal Error Enable (SFE)** — R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) is set, if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port.
1	**System Error on Non-Fatal Error Enable (SNE)** — R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) is set, if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port.
0	**System Error on Correctable Error Enable (SCE)** — R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port.

20.1.35 RSTS—Root Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 60h–63h
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

Bit	Description
31:18	Reserved
17	**PME Pending (PP)** — RO. 0 = When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. 1 = Indicates another PME is pending when the PME status bit is set.
16	**PME Status (PS)** — R/WC. 0 = PME was not asserted. 1 = Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	**PME Requestor ID (RID)** — RO. Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set.

20.1.36 DCAP2—Device Capabilities 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 64h–67h
Default Value: 00000016h
Attribute: RO
Size: 32 bits

Bit	Description
31:5	Reserved
4	**Completion Timeout Disable Supported (CTDS)** — RO. A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	**Completion Timeout Ranges Supported (CTRS) –** RO. This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is hardwired to support 10 ms to 250 ms and 250 ms to 4 s.

20.1.37 DCTL2—Device Control 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 68h–69h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:5	Reserved
4	**Completion Timeout Disable (CTD)** — RW. When set to 1b, this bit disables the Completion Timeout mechanism. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	**Completion Timeout Value (CTV)** — RW. This field allows system software to modify the Completion Timeout value. 0000b = 40–50 ms (Default) (specification range 50 us to 50 ms) 0101b = 40–50 ms (specification range is 16 ms to 55 ms) 0110b = 160–170 ms (specification range is 65 ms to 210 ms) 1001b = 400–500 ms (specification range is 260 ms to 900 ms) 1010b = 1.6–1.7 s (specification range is 1 s to 3.5 s) All other values are Reserved. **NOTE:** Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request w as issued.

20.1.38 LCTL2—Link Control 2 Register (Corporate Only) (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 70h–71h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bit	Description
15:4	Reserved
3:0	**Target Link Speed (TLS)**— RO. This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. 0001b = 2.5 GT/s Target Link Speed All other values reserved

20.1.39 MID—Message Signaled Interrupt Identifiers Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 80h–81h
Default Value: 9005h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Pointer (NEXT)** — RO. Indicates the location of the next pointer in the list.
7:0	**Capability ID (CID)** — RO. Capabilities ID indicates MSI.

20.1.40 MC—Message Signaled Interrupt Message Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 82–83h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)** — RO. Capable of generating a 32-bit message only.
6:4	**Multiple Message Enable (MME)** — R/W. These bits are R/W for software compatibility, but only one message is ever sent by the root port.
3:1	**Multiple Message Capable (MMC)** — RO. Only one message is required.
0	**MSI Enable (MSIE)** — R/W. 0 = MSI is disabled. 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts. **NOTE:** CMD.BME (D28:F0/F1/F2/F3/F4/F5:04h:bit 2) must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

20.1.41 MA—Message Signaled Interrupt Message Address Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 84h–87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:2	**Address (ADDR)** — R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

20.1.42 MD—Message Signaled Interrupt Message Data Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 88h–89h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:0	**Data (DATA)** — R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

20.1.43 SVCAP—Subsystem Vendor Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 90h–91h
Default Value: A00Dh
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Indicates the location of the next pointer in the list.
7:0	**Capability Identifier (CID)** — RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

20.1.44 SVID—Subsystem Vendor Identification Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 94h–97h
Default Value: 00000000h
Attribute: R/WO
Size: 32 bits

Bit	Description
31:16	**Subsystem Identifier (SID)** — R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID)** — R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

20.1.45 PMCAP—Power Management Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A0h–A1h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Indicates this is the last item in the list.
7:0	**Capability Identifier (CID)** — RO. Value of 01h indicates this is a PCI power management capability.

20.1.46 PMC—PCI Power Management Capabilities Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A2h–A3h
Default Value: C802h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support (PMES)** — RO. Indicates PME# is supported for states D0, $D3_{HOT}$ and $D3_{COLD}$. The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	D2_Support (D2S) — RO. The D2 state is not supported.
9	D1_Support (D1S) — RO The D1 state is not supported.
8:6	**Aux_Current (AC)** — RO. Reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	**Device Specific Initialization (DSI)** — RO. 1 = Indicates that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)** — RO. 1 = Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS)** — RO. Indicates support for *Revision 1.1 of the PCI Power Management Specification*.

20.1.47 PMCS—PCI Power Management Control and Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A4h–A7h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:24	Reserved
23	Bus Power / Clock Control Enable (BPCE) — Reserved per *PCI Express* Base Specification, Revision 1.0a*.
22	B2/B3 Support (B23S) — Reserved per *PCI Express* Base Specification, Revision 1.0a*.
21:16	Reserved
15	**PME Status (PMES)** — RO. 1 = Indicates a PME was received on the downstream link.
14:9	Reserved
8	**PME Enable (PMEE)** — R/W. 1 = Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	Reserved
1:0	**Power State (PS)** — R/W. This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state **NOTE:** When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into $D3_{HOT}$. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

20.1.48 MPC2—Miscellaneous Port Configuration Register 2 (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: D4h–D7h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:5	Reserved.
4 (Corporate Only)	**ASPM Control Override Enable (ASPMCOEN)** — RW. 1 = DMI will use the values in the ASPM Control Override registers 0 = DMI will use the ASPM Registers in the Link Control register. **NOTES:**This register allows BIOS to control the DMI ASPM settings instead of the OS.
4 (Consumer Only)	Reserved
3:2 (Corporate Only)	**ASPM Control Override (ASPMO)** — RW. Provides BIOS control of whether DMI should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
3:2 (Consumer Only)	Reserved
1	**EOI Forwarding Disable (EOIFD)** — R/W. When set, EOI messages are not claimed on the backbone by this port an will not be forwarded across the PCIe link. 0 = EOI forwarding is disabled. 1 = EOI forwarding is enabled.
0	**L1 Completion Timeout Mode (LICTM)** — R/W. 0 = PCI Express Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

20.1.49 MPC—Miscellaneous Port Configuration Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: D8h–DBh
Default Value: 08110000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**Power Management SCI Enable (PMCE)** — R/W. 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	**Hot Plug SCI Enable (HPCE)** — R/W. 0 = SCI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SCI whenever a Hot-Plug event is detected.
29	**Link Hold Off (LHO)** — R/W. 1 = Port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	**Address Translator Enable (ATE)** — R/W. This bit is used to enable address translation via the AT bits in this register during loopback mode. 0 = Disable 1 = Enable
27	**Lane Reversal (LR)** — R/O. Consumer Only: This register reads the setting of the SATALED# strap. Corporate Only: This register reads the setting of the PCIELR1 Soft Strap. 0 = PCI Express Lanes 0-3 are reversed. 1 = No Lane reversal (default). **NOTE:** The port configuration straps must be set such that Port 1 is configured as a x4 port using lanes 0-3 when Lane Reversal is enabled. x2 lane reversal is not supported. **NOTE:** This register is only valid on port 1.
26	**Invalid Receive Bus Number Check Enable (IRBNCE)** — R/W. When set, the receive transaction layer will signal an error if the bus number of a Memory request does not fall within the range between SCBN and SBBN. If this check is enabled and the request is a memory write, it is treated as an Unsupported Request. If this check is enabled and the request is a non-posted memory read request, the request is considered a Malformed TLP and a fatal error. Messages, I/O, Config, and Completions are never checked for valid bus number.
25	**Invalid Receive Range Check Enable (IRRCE)** — R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a Memory request does not outside the range between prefetchable and non-prefetchable base and limit. Messages, I/O, Configuration, and Completions are never checked for valid address ranges.
24	**BME Receive Check Enable (BMERCE)** — R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory read or write request is received and the Bus Master Enable bit is not set. Messages, IO, Config, and Completions are never checked for BME.
23	Reserved

Bit	Description
22	**Detect Override (FORCEDET)** — R/W. 0 = Normal operation. Detected output from AFE is sampled for presence detection. 1 = Override mode. Ignores AFE detect output and link training proceeds as if a device were detected.
21	**Flow Control During L1 Entry (FCDL1E)** — R/W. 0 = No flow control update DLLPs sent during L1 Ack transmission. 1 = Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30 µs periodic flow control update.
20:18	**Unique Clock Exit Latency (UCEL)** — R/W. This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = 0) (D28:F0/F1/F2/F3/F4/ F5:Offset 50h:bit 6). It defaults to 512 ns to less than 1 µs, but may be overridden by BIOS.
17:15	**Common Clock Exit Latency (CCEL)** — R/W. This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = 1) (D28:F0/F1/F2/F3/F4/ F5:Offset 50h:bit 6). It defaults to 128 ns to less than 256 ns, but may be overridden by BIOS.
14:8	Reserved
7	**Port I/OxApic Enable (PAE)** — R/W. 0 = Hole is disabled. 1 = A range is opened through the bridge for the following memory addresses: **Port # — Address** 1 — FEC1_0000h – FEC1_7FFFh 2 — FEC1_8000h – FEC1_FFFFh 3 — FEC2_0000h – FEC2_7FFFh 4 — FEC2_8000h – FEC2_FFFFh 5 — FEC3_0000h – FEC3_7FFFh 6 — FEC3_8000h – FEC3_FFFFh
6:3	Reserved
2	**Bridge Type (BT)** — RO. This register can be used to modify the Base Class and Header Type fields from the default P2P bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some server configurations. 0 = The root port bridge type is a P2P Bridge, Header Sub-Class = 04h, and Header Type = Type 1. 1 = The root port bridge type is a P2P Bridge, Header Sub-Class = 00h, and Header Type = Type 0.
1	**Hot Plug SMI Enable (HPME)** — R/W. 0 = SMI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SMI whenever a Hot-Plug event is detected.
0	**Power Management SMI Enable (PMME)** — R/W. 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

20.1.50 SMSCS—SMI/SCI Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: DCh–DFh
Default Value: 00000000h
Attribute: R/WC
Size: 32 bits

Bit	Description
31	**Power Management SCI Status (PMCS)** — R/WC. 1 = PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	**Hot Plug SCI Status (HPCS)** — R/WC. 1 = Hot-Plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	Reserved
4	**Hot Plug Link Active State Changed SMI Status (HPLAS)** — R/WC. 1 = SLSTS.LASC (D28:F0/F1/F2/F3/F4/F5:5A, bit 8) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
3	**Hot Plug Command Completed SMI Status (HPCCM)** — R/WC. 1 = SLSTS.CC (D28:F0/F1/F2/F3/F4/F5:5A, bit 4) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
2	**Hot Plug Attention Button SMI Status (HPABM)** — R/WC. 1 = SLSTS.ABP (D28:F0/F1/F2/F3/F4/F5:5A, bit 0) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
1	**Hot Plug Presence Detect SMI Status (HPPDM)** — R/WC. 1 = SLSTS.PDC (D28:F0/F1/F2/F3/F4/F5:5A, bit 3) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
0	**Power Management SMI Status (PMMS)** — R/WC. 1 = RSTS.PS (D28:F0/F1/F2/F3/F4/F5:60, bit 16) transitioned from 0-to-1, and MPC.PMME (D28:F0/F1/F2/F3/F4/F5:D8, bit 1) is set.

20.1.51 RPDCGEN—Root Port Dynamic Clock Gating Enable (PCI Express-D28:F0/F1/F2/F3/F4/F5)

Address Offset: E1h
Default Value: 00h
Attribute: R/W
Size: 8-bits

Bits	Description
7:4	Reserved. RO
3	**Shared Resource Dynamic Link Clock Gating Enable (SRDLCGEN) —** RW. 0 = Disables dynamic clock gating of the shared resource link clock domain. 1 = Enables dynamic clock gating on the root port shared resource link clock domain. Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5-6.
2	**Shared Resource Dynamic Backbone Clock Gate Enable (SRDBCGEN) —** RW. 0 = Disables dynamic clock gating of the shared resource backbone clock domain. 1 = Enables dynamic clock gating on the root port shared resource backbone clock domain. Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5-6.
1	**Root Port Dynamic Link Clock Gate Enable (RPDLCGEN) —** RW. 0 = Disables dynamic clock gating of the root port link clock domain. 1 = Enables dynamic clock gating on the root port link clock domain.
0	**Root Port Dynamic Backbone Clock Gate Enable (RPDBCGEN) —** RW. 0 = Disables dynamic clock gating of the root port backbone clock domain. 1 = Enables dynamic clock gating on the root port backbone clock domain.

20.1.52 PECR1—PCI Express* Configuration Register 1 (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: E8h–EBh
Default Value: 00000020h
Attribute: R/W
Size: 32 bits

Bit	Description
31:2	Reserved
1	**PECR1 Field 2** — R/W. BIOS may set this bit to 1.
0	Reserved.

20.1.53 VCH—Virtual Channel Capability Header Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 100h–103h
Default Value: 18010002h
Attribute: RWO
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset (NCO)** — R/WO. Indicates the next item in the list. 000h = Does not support Root Complex Topology Capability Structure. 180h = Supports Root Complex Topology Capability Structure.
19:16	**Capability Version (CV)** — R/WO. Indicates the version of the capability structure by the PCI SIG. 0h = Does not support PCI Express virtual Channel capability and the Root complex topology Capability Structure. 1h = Supports PCI Express virtual Channel capability and the Root complex topology Capability Structure.
15:0	**Capability ID (CID)** — R/WO. Indicates this is the Virtual Channel capability item. 0000h = Does not support PCI Express virtual Channel capability and the Root complex topology Capability Structure. 0002h = Supports PCI Express virtual Channel capability and the Root complex topology Capability Structure.

20.1.54 VCAP2—Virtual Channel Capability 2 Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 108h–10Bh
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**VC Arbitration Table Offset (ATO)** — RO. Indicates that no table is present for VC arbitration since it is fixed.
23:0	Reserved.

20.1.55 PVC—Port Virtual Channel Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 10Ch–10Dh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:4	Reserved.
3:1	**VC Arbitration Select (AS)** — R/W. Indicates which VC should be programmed in the VC arbitration table. The root port takes no action on the setting of this field since there is no arbitration table.
0	**Load VC Arbitration Table (LAT)** — R/W. Indicates that the table programmed should be loaded into the VC arbitration table. This bit always returns 0 when read.

20.1.56 PVS—Port Virtual Channel Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 10Eh–10Fh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:1	Reserved.
0	**VC Arbitration Table Status (VAS)** — RO. Indicates the coherency status of the VC Arbitration table when it is being updated. This field is always 0 in the root port since there is no VC arbitration table.

20.1.57 V0CAP—Virtual Channel 0 Resource Capability Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 110h–113h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Arbitration Table Offset (AT)** — RO. This VC implements no port arbitration table since the arbitration is fixed.
23	Reserved.
22:16	**Maximum Time Slots (MTS)** — RO. This VC implements fixed arbitration; therefore, this field is not used.
15	**Reject Snoop Transactions (RTS)** — RO. This VC must be able to take snoopable transactions.
14	**Advanced Packet Switching (APS)** — RO. This VC is capable of all transactions, not just advanced packet switching transactions.
13:8	Reserved.
7:0	**Port Arbitration Capability (PAC)** — RO. Indicates that this VC uses fixed port arbitration.

20.1.58 V0CTL—Virtual Channel 0 Resource Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 114h–117h
Default Value: 800000FFh
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31	**Virtual Channel Enable (EN)** — RO. Always set to 1. Virtual Channel 0 cannot be disabled.
30:27	Reserved.
26:24	**Virtual Channel Identifier (VCID)** — RO. Indicates the ID to use for this virtual channel.
23:20	Reserved.
19:17	**Port Arbitration Select (PAS)** — R/W. Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	**Load Port Arbitration Table (LAT)** — RO. The root port does not implement an arbitration table for this virtual channel.
15:8	Reserved.
7:1	**Transaction Class / Virtual Channel Map (TVM)** — R/W. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. **Bit** — **Transaction Class** 7 — Transaction Class 7 6 — Transaction Class 6 5 — Transaction Class 5 4 — Transaction Class 4 3 — Transaction Class 3 2 — Transaction Class 2 1 — Transaction Class 1
0	Reserved. Transaction class 0 must always mapped to VC0.

20.1.59 V0STS—Virtual Channel 0 Resource Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 11Ah–11Bh
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:2	Reserved.
1	**VC Negotiation Pending (NP)** — RO. 0 = Negotiation is not pending. 1 = Indicates the Virtual Channel is still being negotiated with ingress ports.
0	**Port Arbitration Tables Status (ATS)**. There is no port arbitration table for this VC, so this bit is reserved as 0.

20.1.60 UES—Uncorrectable Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 144h–147h
Default Value: 00000000000x0xxx0x0x0000000x0000b
Attribute: R/WC, RO
Size: 32 bits

This register maintains its state through a platform reset. It loses its state upon suspend.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status (URE)** — R/WC. Indicates an unsupported request was received.
19	ECRC Error Status (EE) — RO. ECRC is not supported.
18	**Malformed TLP Status (MT)** — R/WC. Indicates a malformed TLP was received.
17	**Receiver Overflow Status (RO)** — R/WC. Indicates a receiver overflow occurred.
16	**Unexpected Completion Status (UC)** — R/WC. Indicates an unexpected completion was received.
15	**Completion Abort Status (CA)** — R/WC. Indicates a completer abort was received.
14	**Completion Timeout Status (CT)** — R/WC. Indicates a completion timed out. This bit is set if Completion Timeout is enabled and a completion is not returned within the time specified by the Completion TImeout Value
13	Flow Control Protocol Error Status (FCPE) — RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Status (PT)** — R/WC. Indicates a poisoned TLP was received.
11:5	Reserved
4	**Data Link Protocol Error Status (DLPE)** — R/WC. Indicates a data link protocol error occurred.
3:1	Reserved
0	**Training Error Status (TE)** — RO. Training Errors not supported.

20.1.61 UEM—Uncorrectable Error Mask (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 148h–14Bh
Default Value: 00000000h
Attribute: R/WO, RO
Size: 32 bits

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Mask (URE)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
19	ECRC Error Mask (EE) — RO. ECRC is not supported.
18	**Malformed TLP Mask (MT)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
17	**Receiver Overflow Mask (RO)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
16	**Unexpected Completion Mask (UC)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
15	**Completion Abort Mask (CA)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
14	**Completion Timeout Mask (CT)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
13	**Flow Control Protocol Error Mask (FCPE)** — RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Mask (PT)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
11:5	Reserved

Bit	Description
4	**Data Link Protocol Error Mask (DLPE)** — R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
3:1	Reserved
0	**Training Error Mask (TE)** — RO. Training Errors not supported

20.1.62 UEV — Uncorrectable Error Severity (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 14Ch–14Fh
Default Value: 00060011h
Attribute: RO
Size: 32 bits

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Severity (URE)** — RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	ECRC Error Severity (EE) — RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)** — RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	**Receiver Overflow Severity (RO)** — RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	**Unexpected Completion Severity (UC)** — RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
15	**Completion Abort Severity (CA)** — RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	**Completion Timeout Severity (CT)** — RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
13	Flow Control Protocol Error Severity (FCPE) — RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Severity (PT)** — RO. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	Reserved
4	**Data Link Protocol Error Severity (DLPE)** — RO. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:1	Reserved
0	Training Error Severity (TE) — RO. TE is not supported.

20.1.63 CES — Correctable Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 150h–153h
Default Value: 00000000h
Attribute: R/WC
Size: 32 bits

Bit	Description
31:14	Reserved
13	**Advisory Non-Fatal Error Status (ANFES)** — R/WC. 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	**Replay Timer Timeout Status (RTT)** — R/WC. Indicates the replay timer timed out.
11:9	Reserved
8	**Replay Number Rollover Status (RNR)** — R/WC. Indicates the replay number rolled over.
7	**Bad DLLP Status (BD)** — R/WC. Indicates a bad DLLP was received.
6	**Bad TLP Status (BT)** — R/WC. Indicates a bad TLP was received.
5:1	Reserved
0	**Receiver Error Status (RE)** — R/WC. Indicates a receiver error occurred.

20.1.64 CEM — Correctable Error Mask Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 154h–157h
Default Value: 00000000h
Attribute: R/WO
Size: 32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:14	Reserved
13	**Advisory Non-Fatal Error Mask (ANFEM)** — R/WO. 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. **NOTE:** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	**Replay Timer Timeout Mask (RTT)** — R/WO. Mask for replay timer timeout.
11:9	Reserved
8	**Replay Number Rollover Mask (RNR)** — R/WO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)** — R/WO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT)** — R/WO. Mask for bad TLP reception.
5:1	Reserved
0	**Receiver Error Mask (RE)** — R/WO. Mask for receiver errors.

20.1.65 AECC — Advanced Error Capabilities and Control Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 158h–15Bh
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:9	Reserved
8	ECRC Check Enable (ECE) — RO. ECRC is not supported.
7	ECRC Check Capable (ECC) — RO. ECRC is not supported.
6	ECRC Generation Enable (EGE) — RO. ECRC is not supported.
5	ECRC Generation Capable (EGC) — RO. ECRC is not supported.
4:0	First Error Pointer (FEP) — RO.

20.1.66 RES — Root Error Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 170h–173h
Default Value: 00000000h
Attribute: R/WC, RO
Size: 32 bits

Bit	Description
31:27	**Advanced Error Interrupt Message Number (AEMN)** — RO. There is only one error interrupt allocated.
26:4	Reserved
3	**Multiple ERR_FATAL/NONFATAL Received (MENR)** — RO. For Intel® ICH10, only one error will be captured.
2	**ERR_FATAL/NONFATAL Received (ENR)** — R/WC. 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	**Multiple ERR_COR Received (MCR)** — RO. For ICH10, only one error will be captured.
0	**ERR_COR Received (CR)** — R/WC. 0 = No error message received. 1 = A correctable error message is received.

20.1.67 RCTCL — Root Complex Topology Capability List Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 180–183h
Default Value: 00010005h
Attribute: RO
Size: 32 bits

Bit	Description
31:20	**Next Capability (NEXT)** — RO. Indicates the next item in the list, in this case, end of list.
19:16	**Capability Version (CV)** — RO. Indicates the version of the capability structure.
15:0	**Capability ID (CID)** — RO. Indicates this is a root complex topology capability.

20.1.68 ESD—Element Self Description Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 184h–187h
Default Value: See Description
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Port Number (PN)** — RO. Indicate the ingress port number for the root port. There is a different value per port: **Port # / Value** 1 — 01h 2 — 02h 3 — 03h 4 — 04h 5 — 05h 6 — 06h
23:16	**Component ID (CID)** — RO. This field returns the value of the ESD.CID field (Chipset Config Space: Offset 0104h:bits 23:16) of the chip configuration section, that is programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:8	**Number of Link Entries (NLE)** — RO. The default value of 01h indicates one link entry (corresponding to the RCRB).
7:4	Reserved.
3:0	**Element Type (ET)** — RO. The default value of 0h indicates that the element type is a root port.

20.1.69 ULD — Upstream Link Description Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 190h–193h
Default Value: 00000001h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	**Target Port Number (PN)** — RO. Indicates the port number of the RCRB.
23:16	**Target Component ID (TCID)** — RO. This field returns the value of the ESD.CID field (Chipset Config Space: Offset 0104h:bits 23:16) of the chip configuration section, that is programmed by platform BIOS, since the root port is in the same component as the RCRB.
15:2	Reserved.
1	**Link Type (LT)** — RO. Indicates that the link points to the Intel® ICH10 RCRB.
0	**Link Valid (LV)** — RO. Indicates that this link entry is valid.

20.1.70 ULBA — Upstream Link Base Address Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 198h–19Fh
Default Value: See Description
Attribute: RO
Size: 64 bits

Bit	Description
63:32	**Base Address Upper (BAU)** — RO. The RCRB of the Intel® ICH10 lives in 32-bit space.
31:0	**Base Address Lower (BAL)** — RO. This field matches the RCBA register (D31:F0:Offset F0h) value in the LPC bridge.

20.1.71 PECR2 — PCI Express* Configuration Register 2 (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 300-303h
Default Value: 60005007h
Attribute: R/W
Size: 32 bits

Bit	Description
31:20	Reserved
21	**PECR2 Field 1** — R/W. BIOS must set this bit to 1b.
20:0	Reserved

20.1.72 PEETM — PCI Express* Extended Test Mode Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 318h
Default Value: See Description
Attribute: RO
Size: 8 bits

Bit	Description
7:3	Reserved
2	**Scrambler Bypass Mode (BAU)** — R/W. 0 = Normal operation. Scrambler and descrambler are used. 1 = Bypasses the data scrambler in the transmit direction and the data de-scrambler in the receive direction. **NOTE:** This functionality intended for debug/testing only. **NOTE:** If bypassing scrambler with ICH10 root port 1 in x4 configuration, each ICH10 root port must have this bit set.
1:0	Reserved

20.1.73 PEC1 — PCI Express* Configuration Register 1 (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 324h
Default Value: 14000016h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	**PEC1 Field 1** — R/W. BIOS must program this field to 40h.

§ §

21 High Precision Event Timer Registers

The timer registers are memory-mapped in a non-indexed scheme. This allows the processor to directly access each register without having to use an index register. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. There are four possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range will be selected by configuration bits in the High Precision Timer Configuration Register (Chipset Config Registers:Offset 3404h).

Behavioral Rules:

1. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

21.1 Memory Mapped Registers

Table 21-1. Memory-Mapped Registers (Sheet 1 of 2)

Offset	Mnemonic	Register	Default	Type
000–007h	GCAP_ID	General Capabilities and Identification	0429B17F8 086A201h	RO
008–00Fh	—	Reserved	—	—
010–017h	GEN_CONF	General Configuration	00000000 00000000h	R/W
018–01Fh	—	Reserved	—	—
020–027h	GINTR_STA	General Interrupt Status	00000000 00000000h	R/WC, R/W
028–0EFh	—	Reserved	—	—
0F0–0F7h	MAIN_CNT	Main Counter Value	N/A	R/W
0F8–0FFh	—	Reserved	—	—
100–107h	TIM0_CONF	Timer 0 Configuration and Capabilities	N/A	R/W, RO
108–10Fh	TIM0_COMP	Timer 0 Comparator Value	N/A	R/W
110–11Fh	—	Reserved	—	—
120–127h	TIM1_CONF	Timer 1 Configuration and Capabilities	N/A	R/W, RO

Table 21-1. Memory-Mapped Registers (Sheet 2 of 2)

Offset	Mnemonic	Register	Default	Type
128–12Fh	TIM1_COMP	Timer 1 Comparator Value	N/A	R/W
130–13Fh	—	Reserved	—	—
140–147h	TIM2_CONF	Timer 2 Configuration and Capabilities	N/A	R/W, RO
148–14Fh	TIM2_COMP	Timer 2 Comparator Value	N/A	R/W
150–15Fh	—	Reserved	—	—
160–167h	TIM3_CONG	Timer 3 Configuration and Capabilities	N/A	R/W, RO
168–16Fh	TIM3_COMP	Timer 3 Comparator Value	N/A	R/W
170–3FFh (Consumer Only)	—	Reserved	—	—
180–187h (Corporate Only)	TIM4_CONG	Timer 4 Configuration and Capabilities	N/A	R/W, RO
188–18Fh (Corporate Only)	TIM4_COMP	Timer 4 Comparator Value	N/A	R/W
190–19Fh (Corporate Only)	—	Reserved	—	—
1A0–1A7h (Corporate Only)	TIM5_CONG	Timer 5 Configuration and Capabilities	N/A	R/W, RO
1A8–1AFh (Corporate Only)	TIM5_COMP	Timer 5 Comparator Value	N/A	R/W
1B0–1BFh (Corporate Only)	—	Reserved	—	—
1C0–1C7h (Corporate Only)	TIM6_CONG	Timer 6 Configuration and Capabilities	N/A	R/W, RO
1C8–1CFh (Corporate Only)	TIM6_COMP	Timer 6 Comparator Value	N/A	R/W
1D0–1DFh (Corporate Only)	—	Reserved	—	—
1E0–1E7h (Corporate Only)	TIM7_CONG	Timer 7 Configuration and Capabilities	N/A	R/W, RO
1E8–1EFh (Corporate Only)	TIM7_COMP	Timer 7 Comparator Value	N/A	R/W
1F0–19Fh (Corporate Only)	—	Reserved	—	—
200–3FFh (Corporate Only)	—	Reserved	—	—

NOTES:
1. Reads to reserved registers or bits will return a value of 0.
2. Software must not attempt locks to the memory-mapped I/O ranges for High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

21.1.1 GCAP_ID—General Capabilities and Identification Register

Address Offset: 00h Attribute: RO
Default Value: 0429B17F8086A201h Size: 64 bits

Bit	Description
63:32	**Main Counter Tick Period (COUNTER_CLK_PER_CAP)** — RO. This field indicates the period at which the counter increments in femptoseconds (10^-15 seconds). This will return 0429B17F when read. This indicates a period of 69841279 fs (69.841279 ns).
31:16	**Vendor ID Capability (VENDOR_ID_CAP)** — RO. This is a 16-bit value assigned to Intel.
15	**Legacy Replacement Rout Capable (LEG_RT_CAP)** — RO. Hardwired to 1. Legacy Replacement Interrupt Rout option is supported.
14	Reserved. This bit returns 0 when read.
13	**Counter Size Capability (COUNT_SIZE_CAP)** — RO. Hardwired to 1. Counter is 64-bit wide.
12:8	**Number of Timer Capability (NUM_TIM_CAP)** — RO. This field indicates the number of timers in this block. 03h = Four timers. (Consumer Only) 07h = Eight timers. (Corporate Only)
7:0	**Revision Identification (REV_ID)** — RO. This indicates which revision of the function is implemented. Default value will be 01h.

21.1.2 GEN_CONF—General Configuration Register

Address Offset: 010h Attribute: R/W
Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:2	Reserved. These bits return 0 when read.
1	**Legacy Replacement Rout (LEG_RT_CNF)** — R/W. If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, then the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n config registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	**Overall Enable (ENABLE_CNF)** — R/W. This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. **NOTE:** This bit will default to 0. BIOS can set it to 1 or 0.

21.1.3 GINTR_STA—General Interrupt Status Register

Address Offset: 020h Attribute: R/W, R/WC
Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:8	Reserved. These bits will return 0 when read.
7 (Corporate Only)	**Timer 7Interrupt Active (T07_INT_STS)** — R/W. Same functionality as Timer 0.
6 (Corporate Only)	**Timer 6Interrupt Active (T06_INT_STS)** — R/W. Same functionality as Timer 0.
5 (Corporate Only)	**Timer 5Interrupt Active (T05_INT_STS)** — R/W. Same functionality as Timer 0.
4 (Corporate Only)	**Timer 4Interrupt Active (T04_INT_STS)** — R/W. Same functionality as Timer 0.
7:4 (Consumer Only)	Reserved. These bits will return 0 when read.
3	**Timer 3Interrupt Active (T03_INT_STS)** — R/W. Same functionality as Timer 0.

Bit	Description
2	**Timer 2 Interrupt Active (T02_INT_STS)** — R/W. Same functionality as Timer 0.
1	**Timer 1 Interrupt Active (T01_INT_STS)** — R/W. Same functionality as Timer 0.
0	**Timer 0 Interrupt Active (T00_INT_STS)** — R/WC. The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. **NOTE:** Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

21.1.4 MAIN_CNT—Main Counter Value Register

Address Offset: 0F0h
Default Value: N/A
Attribute: R/W
Size: 64 bits

Bit	Description
63:0	**Counter Value (COUNTER_VAL[63:0])** — R/W. Reads return the current value of the counter. Writes load the new value to the counter. **NOTES:** 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this delays the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads return the same value. The second of two reads always returns a larger value (unless the timer has rolled over to 0).

21.1.5 TIMn_CONF—Timer n Configuration and Capabilities Register

Address Offset:	Timer 0:	100–107h	Attribute:	RO, R/W
	Timer 1:	120–127h		
	Timer 2:	140–147h		
	Timer 3:	160–167h		
	Timer 4:	180–187h (Corporate Only)		
	Timer 5:	1A0–1A7h (Corporate Only)		
	Timer 6:	1C0–1C7h (Corporate Only)		
	Timer 7:	1E0–1E7h (Corporate Only)		
Default Value:	N/A		Size:	64 bit

Note: The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 (4, 5, 6, 7 Corporate Only) referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7(4,5,6,7 Corporate Only).

Bit	Description
63:56	Reserved. These bits will return 0 when read.
55:52, 43	**Timer Interrupt Rout Capability (TIMERn_INT_ROUT_CAP)** — RO. Timer 0, 1: Bits 52, 53, 54, and 55 in this field (corresponding to IRQ 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 2: Bits 43, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 3: Bits 44, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 4, 5, 6, 7 (Corporate Only). This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages. **NOTE:** If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET #2. **NOTE:** If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET #3.
51:45, 42:16	Reserved**.** These bits return 0 when read.
15 (Corporate Only)	**TIMERn_FSB_INT_DEL_CAP: FSB Interrupt Delivery:** (where n is the timer number: 00 to 07). If this read-only bit is 1, then the hardware supports a direct front-side bus delivery of this timer's interrupt. Intel Specific: This bit is always read as 1, since the Intel ICH10 HPET implementation supports the direct FSB interrupt delivery.
15 (Consumer Only)	Reserved**.** This bit returns 0 when read.
14 (Corporate Only)	**TIMERn_FSB_EN_CNF:** (where n is the timer number: 00 to 07). If the TIMERn_FSB_INT_DEL_CAP bit is set for this timer, then the software can set the TIMERn_FSB_EN_CNF bit to force the interrupts to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUT_CNF field in this register will be ignored. The TIMERn_FSB_ROUT register will be used instead. Intel and Timer 0, 1, 2, 3 Specific: This bit is a read/write bit. Intel and Timer 4, 5, 6, 7 Specific: This bit is always Read Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.
14 (Consumer Only)	Reserved**.** This bit returns 0 when read.

Bit	Description
13:9	**Interrupt Rout (TIMERn_INT_ROUT_CNF)** — R/W. This 5-bit field indicates the routing for the interrupt to the 8259 or I/O (x) APIC. Software writes to this field to select which interrupt in the 8259 or I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, then the value read back will not match what is written. The software must only write valid values. Timer 4, 5, 6, 7 (corporate Only): This field is Read-only and reads will return 0. **NOTES:** 1. If the interrupt is handled via the 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. 2. If the Legacy Replacement Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. 3. Timer 0,1: Software is responsible to make sure it programs a valid value (20, 21, 22, or 23) for this field. The ICH10 logic does not check the validity of the value written. 4. Timer 2: Software is responsible to make sure it programs a valid value (11, 20, 21, 22, or 23) for this field. The ICH10 logic does not check the validity of the value written. 5. Timer 3: Software is responsible to make sure it programs a valid value (12, 20, 21, 22, or 23) for this field. The ICH10 logic does not check the validity of the value written.
8	**Timer n 32-bit Mode (TIMERn_32MODE_CNF)** — R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. Timer 0: Bit is read/write (default to 0). 0 = 64 bit; 1 = 32 bit Timers 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only): Hardwired to 0. Writes have no effect (since these two timers are 32-bits). **NOTE:** When this bit is set to 1, the hardware counter will do a 32-bit operation on comparator match and rollovers, thus the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any rollover from lower 32-bit of the main counter and becomes all zeros.
7	Reserved**.** This bit returns 0 when read.
6	**Timer n Value Set (TIMERn_VAL_SET_CNF)** — R/W. Software uses this bit only for Timer 0 if it has been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timer's accumulator. Software does **not** have to write this bit back to 1 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode. **NOTE:** This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only).
5	**Timer n Size (TIMERn_SIZE_CAP)** — RO. This read only field indicates the size of the timer. Timer 0: Value is 1 (64-bits). Timers 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only): Value is 0 (32-bits).
4	**Periodic Interrupt Capable (TIMERn_PER_INT_CAP)** — RO. If this bit is 1, the hardware supports a periodic mode for this timer's interrupt. Timer 0: Hardwired to 1 (supports the periodic interrupt). Timers 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only): Hardwired to 0 (does not support periodic interrupt).

Bit	Description
3	**Timer n Type (TIMERn_TYPE_CNF)** — R/W or RO. Timer 0: Bit is read/write. 0 = Disable timer to generate periodic interrupt; 1 = Enable timer to generate a periodic interrupt. Timers 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only): Hardwired to 0. Writes have no affect.
2	**Timer n Interrupt Enable (TIMERn_INT_ENB_CNF)** — R/W. This bit must be set to enable timer n to cause an interrupt when it times out. 0 = Disable (Default). The timer can still count and generate appropriate status bits, but will not cause an interrupt. 1 = Enable.
1	**Timer Interrupt Type (TIMERn_INT_TYPE_CNF)** — R/W. 0 = The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1 = The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. Timer 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only): This bit is Read-Only, and will return 0 when read
0	Reserved. These bits will return 0 when read.

NOTE: Reads or writes to unimplemented timers should not be attempted. Read from any unimplemented registers will return an undetermined value.

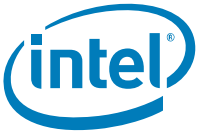
21.1.6 TIMn_COMP—Timer n Comparator Value Register

Address Offset: Timer 0: 108h–10Fh
Timer 1: 128h–12Fh
Timer 2: 148h–14Fh
Timer 3: 168h–16Fh
Timer 4: 188h – 18Fh (Corporate Only)
Timer 5: 1A8h – 1AFh (Corporate Only)
Timer 6: 1C8h – 1CFh (Corporate Only)
Timer 7: 1E8h – 1EFh (Corporate Only)

Attribute: R/W
Default Value: N/A Size: 64 bit

Bit	Description
63:0	**Timer Compare Value** — R/W. Reads to this register return the current value of the comparator Timers 0, 1, 2, 3, 4, 5, 6, 7 (4, 5, 6, 7 Corporate Only) are configured to non-periodic mode: Writes to this register load the value against which the main counter should be compared for this timer. • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • The value in this register does not change based on the interrupt being generated. Timer 0 is configured to periodic mode: • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • After the main counter equals the value in this register, the value in this register is increased by the value last written to the register. For example, if the value written to the register is 00000123h, then 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h 4. The value in this register will then be adjusted by the hardware to 00000369h • As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h Default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer has a default value of 00000000FFFFFFFFh. A 64-bit timer has a default value of FFFFFFFFFFFFFFFFh.

§ §



22 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface resides in memory mapped space. This function contains registers that allow for the setup and programming of devices that reside on the SPI interface.

Note: All registers in this function (including memory-mapped registers) must be addressable in byte, word, and dword quantities. The software must always make register accesses on natural boundaries (i.e., DWord accesses must be on dword boundaries; word accesses on word boundaries, etc.) In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the SPI memory-mapped space, the results are undefined.

22.1 Serial Peripheral Interface Memory Mapped Configuration Registers

The SPI Host Interface registers are memory-mapped in the RCRB (Root Complex Register Block) Chipset Register Space with a base address (SPIBAR) of 3800h and are located within the range of 3800h to 39FFh. The address for RCRB can be found in RCBA Register see Section 13.1.36. The individual registers are then accessible at SPIBAR + Offset as indicated Table 22-1.

These memory mapped registers must be accessed in byte, word, or dword quantities.

Table 22-1. Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) (Sheet 1 of 2)

SPIBAR + Offset	Mnemonic	Register Name	Default	Type
00h–03h	BFPR	BIOS Flash Primary Region	00000000h	RO
04h–05h	HSFSTS	Hardware Sequencing Flash Status	0000h	RO, R/WC, R/W
06h–07h	HSFCTL	Hardware Sequencing Flash Control	0000h	R/W, R/WS
08h–0Bh	FADDR	Flash Address	00000000h	R/W
0Ch–0Fh	Reserved	Reserved	00000000h	
10h–13h	FDATA0	Flash Data 0	00000000h	R/W
14h–4Fh	FDATAN	Flash Data N	00000000h	R/W
50h–53h	FRACC	Flash Region Access Permissions	00000202h	RO, R/W
54h–57h	FREG0	Flash Region 0	00000000h	RO
58h–5Bh	FREG1	Flash Region 1	00000000h	RO
5Ch–5F	FREG2	Flash Region 2	00000000h	RO
60h–63h	FREG3	Flash Region 3	00000000h	RO
64h–67h	FREG3	Flash Region 4	00000000h	RO
67h–73h	Reserved	Reserved for Future Flash Regions		

Table 22-1. Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) (Sheet 2 of 2)

SPIBAR + Offset	Mnemonic	Register Name	Default	Type
74h–77h	FPR0	Flash Protected Range 0	00000000h	R/W
78h–7Bh	FPR1	Flash Protected Range 1	00000000h	R/W
7Ch–7Fh	FPR2	Flash Protected Range 2	00000000h	R/W
80–83h	FPR3	Flash Protected Range 3	00000000h	R/W
84h–87h	FPR4	Flash Protected Range 4	00000000h	R/W
88h–8Fh	—	Reserved	—	
90h	SSFSTS	Software Sequencing Flash Status	00h	RO, R/WC
91h–93h	SSFCTL	Software Sequencing Flash Control	0000h	R/W
94h–95h	PREOP	Prefix Opcode Configuration	0000h	R/W
96h–97h	OPTYPE	Opcode Type Configuration	0000h	R/W
98h–9Fh	OPMENU	Opcode Menu Configuration	00000000 00000000h	R/W
A0h	BBAR	BIOS Base Address Configuration	00000000h	R/W, RO
B0h–B3h	FDOC	Flash Descriptor Observability Control	00000000h	R/W
B4h–B7h	FDOD	Flash Descriptor Observability Data	00000000h	RO
B8h–C3h	—	Reserved	—	
C0h–C3h	AFC	Additional Flash Control	00000000h	RO, R/W
C4–C7h	LVSCC	Host Lower Vendor Specific Component Capabilities	00000000h	RO, R/WL
C8–C11h	UVSCC	Host Upper Vendor Specific Component Capabilities	00000000h	RO, R/WL
D0–D3h	FPB	Flash Partition Boundary	00000000h	RO

22.1.1 BFPR –BIOS Flash Primary Region Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 00h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**BIOS Flash Primary Region Limit (PRL) —** RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	**BIOS Flash Primary Region Base (PRB)** — RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

22.1.2 HSFS—Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 04h	Attribute:	RO, R/WC, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15	**Flash Configuration Lock-Down (FLOCKDN)** — R/W/L. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel ME enabled system.
14	**Flash Descriptor Valid (FDV) —** RO. This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	**Flash Descriptor Override Pin-Strap Status (FDOPSS)** — RO: This register reflects the value the Flash Descriptor Override Pin-Strap. 0 = The Flash Descriptor Override strap is set 1 = No override
12:6	Reserved
5	**SPI Cycle In Progress (SCIP)—** RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0. **NOTE:** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.

Bit	Description
4:3	**Block/Sector Erase Size (BERASE)** — RO. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4 K Byte 10 = 8 K Byte 11 = 64 K Byte If the FLA is less than FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA is greater or equal to FPBA then this field reflects the value in the UVSCC.UBES register. **NOTE:** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
2	**Access Error Log (AEL)** — R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a 1. **NOTE:** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
1	**Flash Cycle Error (FCERR)** — R/W/C. Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs due to a global reset or host partition reset in an Intel ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register. **NOTE:** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
0	**Flash Cycle Done (FDONE)** — R/W/C. The ICH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. **NOTE:** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.

22.1.3 HSFC—Hardware Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 06h	Attribute:	R/W, R/WS
Default Value:	0000h	Size:	16 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
15	**Flash SPI SMI# Enable (FSMIE)** — R/W. When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	Reserved
13:8	**Flash Data Byte Count (FDBC) —** R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	**FLASH Cycle (FCYCLE)** — R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 64 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 64 bytes by setting FDBC) 11 = Block Erase
0	**Flash Cycle Go (FGO)** — R/W/S. A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

22.1.4 FADDR—Flash Address Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 08h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:25	Reserved
24:0	**Flash Linear Address (FLA) —** R/W. The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

22.1.5 FDATA0—Flash Data 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 10h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Flash Data 0 (FD0)** — R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

22.1.6 FDATAN—Flash Data [N] Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 14h SPIBAR + 18h SPIBAR + 1Ch SPIBAR + 20h SPIBAR + 24h SPIBAR + 28h SPIBAR + 2Ch SPIBAR + 30h SPIBAR + 34h SPIBAR + 38h SPIBAR + 3Ch SPIBAR + 40h SPIBAR + 44h SPIBAR + 48h SPIBAR + 4Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Flash Data N (FD[N])** — R/W. Similar definition as Flash Data 0. However, this register does not begin shifting until FD[N-1] has completely shifted in/out.— R/W.

22.1.7 FRAP—Flash Regions Access Permissions Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 50h	Attribute:	RO, R/W
Default Value:	00000202h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	**BIOS Master Write Access Grant (BMWAG)** — R/W. Each bit [31:29] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel Management Engine, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	**BIOS Master Read Access Grant (BMRAG) —** R/W. Each bit [28:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel Management Engine, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register are locked by the FLOCKDN bit
15:8	**BIOS Region Write Access (BRWA) —** RO. Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 1 Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register or the Flash Descriptor Security Override strap is set.
7:0	**BIOS Region Read Access (BRRA)** — RO. Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register or the Flash Descriptor Security Override strap is set.

22.1.8 FREG0—Flash Region 0 (Flash Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 54h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	Reserved
12:0	**Region Base (RB) / Flash Descriptor Base Address Region (FDBAR)** — RO. This specifies address bits 24:12 for the Region 0 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

22.1.9 FREG1—Flash Region 1 (BIOS Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 58h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

22.1.10 FREG2—Flash Region 2 (ME) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 5Ch	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 2 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

22.1.11 FREG3—Flash Region 3 (GbE) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 60h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 3 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

22.1.12 FREG4—Flash Region 4 (Platform Data) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 64h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 4 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base

22.1.13 PR0—Protected Range 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 74h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.1.14 PR1—Protected Range 1 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 78h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.1.15 PR2—Protected Range 2 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 7Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.1.16 PR3—Protected Range 3 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 80h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.1.17 PR4—Protected Range 4 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 84h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.1.18 SSFS—Software Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 90h	Attribute:	RO, R/WC
Default Value:	00h	Size:	8 bits

Note: The Software Sequencing control and status registers are reserved if the hardware sequencing control and status registers are used.

Bit	Description
7:5	Reserved
4	**Access Error Log (AEL) —** RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	**Flash Cycle Error (FCERR) —** R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system.
2	**Cycle Done Status** — R/WC. The ICH sets this bit to 1 when the SPI Cycle completes (i.e., SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	**SPI Cycle In Progress (SCIP)** — RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

22.1.19 SSFC—Software Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 91h Attribute: R/W
Default Value: 000000h Size: 24 bits

Bit	Description
23:19	Reserved
18:16	**SPI Cycle Frequency (SCF) —** R/W. This register sets frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, etc.) except for the read cycle which always run at 20 MHz. 000 = 20 MHz 001 = 33 MHz All other values reserved. This register is locked when the SPI Configuration Lock-Down bit is set.
15	**SPI SMI# Enable (SME)** — R/W. When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
14	**Data Cycle (DS)** — R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares
13:8	**Data Byte Count (DBC)** — R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
7	Reserved
6:4	**Cycle Opcode Pointer (COP)** — R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	**Sequence Prefix Opcode Pointer (SPOP)** — R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the ICH supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	**Atomic Cycle Sequence (ACS)** — R/W. When set to 1 along with the SCGO assertion, the ICH10 will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: • Atomic Sequence Prefix Command (8-bit opcode only) • Primary Command specified below by software (can include address and data) • Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	**SPI Cycle Go (SCGO)** — R/WS. This bit always returns 0 on reads. However, a write to this register with a 1 in this bit starts the SPI cycle defined by the other bits of this register. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	Reserved

22.1.20 PREOP—Prefix Opcode Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 94h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	**Prefix Opcode 1**— R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	**Prefix Opcode 0** — R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

NOTE: This register is not writable when the Flash Configuration Lock-Down bit (SPIBAR + 04h:15) is set.

22.1.21 OPTYPE—Opcode Type Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 96h Attribute: R/W
Default Value: 0000h Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

Note: The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, “Chip Erase” and “Auto-Address Increment Byte Program”)

Bit	Description
15:14	**Opcode Type 7** — R/W. See the description for bits 1:0
13:12	**Opcode Type 6** — R/W. See the description for bits 1:0
11:10	**Opcode Type 5** — R/W. See the description for bits 1:0
9:8	**Opcode Type 4** — R/W. See the description for bits 1:0
7:6	**Opcode Type 3** — R/W. See the description for bits 1:0
5:4	**Opcode Type 2** — R/W. See the description for bits 1:0
3:2	**Opcode Type 1** — R/W. See the description for bits 1:0
1:0	**Opcode Type 0** — R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

NOTE: This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

22.1.22 OPMENU—Opcode Menu Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 98h	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Note: It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	**Allowable Opcode 7** — R/W. See the description for bits 7:0
55:48	**Allowable Opcode 6** — R/W. See the description for bits 7:0
47:40	**Allowable Opcode 5** — R/W. See the description for bits 7:0
39:32	**Allowable Opcode 4** — R/W. See the description for bits 7:0
31:24	**Allowable Opcode 3** — R/W. See the description for bits 7:0
23:16	**Allowable Opcode 2** — R/W. See the description for bits 7:0
15:8	**Allowable Opcode 1** — R/W. See the description for bits 7:0
7:0	**Allowable Opcode 0** — R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

22.1.23 BBAR—BIOS Base Address Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + A0h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Bit	Description
31:24	Reserved
23:8	**Bottom of System Flash**— R/W. This field determines the bottom of the System BIOS. The ICH10 will not run programmed commands nor memory reads whose address field is less than this value. this field corresponds to bits 23:8 of the 3-byte address; bits 7:0 are assumed to be 00h for this vector when comparing to a potential SPI address. **NOTE:** The SPI host controller prevents any programmed cycle using the address register with an address less than the value in this register. Some flash devices specify that the Read ID command must have an address of 0000h or 0001h. If this command must be supported with these device, it must be performed with the BIOS Bar
7:0	Reserved

22.1.24 FDOC—Flash Descriptor Observability Control Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + B0h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register that can be used to observe the contents of the Flash Descriptor that is stored in the ICH10 Flash Controller. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:15	Reserved
14:12	**Flash Descriptor Section Select (FDSS)** — R/W. Selects which section within the loaded Flash Descriptor to observe. 000 = Flash Signature and Descriptor Map 001 = Component 010 = Region 011 = Master 111 = Reserved
11:2	**Flash Descriptor Section Index (FDSI) —** R/W. Selects the DW offset within the Flash Descriptor Section to observe.
1:0	Reserved

22.1.25 FDOD—Flash Descriptor Observability Data Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + B4h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register that can be used to observe the contents of the Flash Descriptor that is stored in the ICH10 Flash Controller.

Bit	Description
31:0	**Flash Descriptor Section Data (FDSD) —** RO. Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

22.1.26 AFC—Additional Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + C0h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits.

Bit	Description
31:3	Reserved.
2:1	**Flash Controller Interface Dynamic Clock Gating Enable** — R/W. 0 = Flash Controller Interface Dynamic Clock Gating is Disabled 1 = Flash Controller Interface Dynamic Clock Gating is Enabled Other configurations are Reserved.
0	**Flash Controller Core Dynamic Clock Gating Enable** — R/W. 0 = Flash Controller Core Dynamic Clock Gating is Disabled 1 = Flash Controller Core Dynamic Clock Gating is Enabled

22.1.27 LVSCC— Host Lower Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C4h Attribute: RO, RWL
Default Value: 00000000h Size: 32 bits

Note: All attributes described in LVSCC must apply to all flash space below the FPBA, even if it spans between two separate flash parts. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	Reserved.
23	**Vendor Component Lock (LVCL)** — RW. This register locks itself when set. 0 = The lock bit is not set 1 = The Vendor Component Lock bit is set.
22:16	Reserved
15:8	**Lower Erase Opcode (LEO)**— RW. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (LVCL) bit.
7:5	Reserved
4	**Write Enable on Write Status (LWEWS)** — RW. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to 1.
3	**Lower Write Status Required (LWSR)** — RW. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. This is not an atomic sequence. If the SPI component's status register is non-volatile, then an atomic software sequencing should be used to unlock the flash part. **NOTE:** This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. **NOTE:** Bit 3 and bit 4 should NOT be both set to 1.

Bit	Description
2	**Lower Write Granularity (LWG) —** RW**.** This register is locked by the Vendor Component Lock (LVCL) bit. 0 = 1 Byte 1 = 64 Byte **NOTES:** 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writeable SPI flash.
1:0	**Lower Block/Sector Erase Size (LBES)—** RW. This field identifies the erasable sector size for all Flash components. 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB This register is locked by the Vendor Component Lock (LVCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.

22.1.28 UVSCC— Host Upper Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + C8h	Attribute:	RO, RWL
Default Value:	00000000h	Size:	32 bits

Note: All attributes described in UVSCC must apply to all flash space equal to or above the FPBA, even if it spans between two separate flash parts. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	Reserved.
23	**Vendor Component Lock (UVCL)** — RW. 0 = The lock bit is not set 1 = The Vendor Component Lock bit is set. This register locks itself when set.
22:16	Reserved
15:8	**Upper Erase Opcode (UEO)**— RW. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (UVCL) bit.
7:5	Reserved

Bit	Description
4	**Write Enable on Write Status (UWEWS)** — RW.This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to 1.
3	**Upper Write Status Required (UWSR)** — RW. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. This is not an atomic sequence. If the SPI component's status register is non-volatile, then an atomic software sequencing should be used to unlock the flash part. 2. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to 1.
2	**Upper Write Granularity (UWG) —** RW. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = 1 Byte 1 = 64 Byte **NOTES:** 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writeable SPI flash.
1:0	**Upper Block / Sector Erase Size (UBES)—** RW. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB This register is locked by the Vendor Component Lock (UVCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is greater or equal to FPBA.

22.1.29 FPB — Flash Partition Boundary (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + D0h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:13	Reserved.
12:0	**Flash Partition Boundary Address (FPBA)** — RO. This register reflects the value of Flash Descriptor Component FPBA field.

22.2 Flash Descriptor Registers

The following sections describe the data structure of the Flash Descriptor on the SPI device. These are not registers within ICH10.

22.2.1 Flash Descriptor Content

22.2.1.1 FLVALSIG - Flash Valid Signature Register (Flash Descriptor Registers)

Memory Address: FDBAR + 000h Default Value: h
Size: 32 bits

Bits	Description
31:0	**Flash Valid Signature.** This field identifies the Flash Descriptor sector as valid. If the contents at this location contain 0FF0A55Ah, then the Flash Descriptor is considered valid and it will operate in Descriptor Mode, else it will operate in Non-Descriptor Mode.

22.2.1.2 FLMAP0 - Flash Map 0 Register (Flash Descriptor Registers)

Memory Address: FDBAR + 004h Default Value: h
Size: 32 bits

Bits	Description
31:27	Reserved
26:24	**Number Of Regions (NR).** This field identifies the total number of Flash Regions. This number is 0's based, so a setting of all 0's indicates that the only Flash region is region 0, the Flash Descriptor region.
23:16	**Flash Region Base Address (FRBA).** This identifies address bits [11:4] for the Region portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. A recommended FRBA is 04h.
15:10	Reserved
9:8	**Number Of Components (NC)**. This field identifies the total number of Flash Components. Each supported Flash Component requires a separate chip select. 00 = 1 Component. 01 = 2 Components. All other settings = Reserved
7:0	**Flash Component Base Address (FCBA)**. This identifies address bits [11:4] for the Component portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. A recommended FCBA is 01h.

22.2.1.3 FLMAP1—Flash Map 1 Register (Flash Descriptor Registers)

Memory Address: FDBAR + 008h Default Value: h
Size: 32 bits

Bits	Description
31:24	**ICH Strap Length (ISL).** Identifies the 1s based number of Dwords of ICH Straps to be read, up to 255 DWs (1KB) max. A setting of all 0's indicates there are no ICH DW straps.
23:16	**Flash ICH Strap Base Address (FISBA).** This identifies address bits [11:4] for the ICH Strap portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. For validation purposes, the recommended FISBA is 10h
15:11	Reserved
10:08	**Number Of Masters (NM).** This field identifies the total number of Flash Regions. This number is 0's based.
7:0	**Flash Master Base Address (FMBA).** This identifies address bits [11:4] for the Master portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. A recommended FMBA is 06h.

22.2.1.4 FLMAP2—Flash Map 2 Register (Flash Descriptor Registers)

Memory Address: FDBAR + 00Ch Default Value: h
Size: 32 bits

Bits	Description
31:16	Reserved
15:08	**MCH Strap Length (MSL).** Identifies the 1's based number of Dwords of (G)MCH Straps to be read, up to 255 DWs (1KB) max. A setting of all 0's indicates there are no (G)MCH DW straps.
7:0	**Flash (G)MCH Strap Base Address (FMSBA).** This identifies address bits [11:4] for the (G)MCH Strap portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. A recommended FMSBA is 20h.

22.2.2 Flash Descriptor Component Section

The following section of the Flash Descriptor is used to identify the different Flash Components and their capabilities.

22.2.2.1 FLCOMP—Flash Components Register (Flash Descriptor Registers)

Memory Address: FCBA + 000h Default Value: h
Size: 32 bits

Bits	Description
31:30	Reserved
29:27	**Read ID and Read Status Clock Frequency**. 000 = 20 MHz 001 = 33 MHz All other Settings = Reserved **NOTE:** If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components.
26:24	**Write and Erase Clock Frequency**. 000 = 20 MHz 001 = 33 MHz All other Settings = Reserved **NOTE:** If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components.
23:21	**Fast Read Clock Frequency**. This field identifies the frequency that can be used with the Fast Read instruction. This field is undefined if the Fast Read Support field is '0'. 000 = 20 MHz 001 = 33 MHz All other Settings = Reserved **NOTE:** If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components.
20	**Fast Read Support**. 0 = Fast Read is not Supported 1 = Fast Read is supported If the Fast Read Support bit is a '1' and a device issues a Direct Read or issues a read command from the Hardware Sequencer and the length is greater than 4 bytes, then the SPI Flash instruction should be "Fast Read". If the Fast Read Support is a '0' or the length is 1-4 bytes, then the SPI Flash instruction should be "Read". Reads to the Flash Descriptor always use the Read command independent of the setting of this bit. **NOTE:** If more than one Flash component exists, this field can only be set to '1' if both components support Fast Read.

Bits	Description
19:17	**Read Clock Frequency**. 000 = 20 MHz All other Settings = Reserved **NOTE:** If more than one Flash component exists, this field must be set to the lowest common frequency of the different Flash components.
16:6	Reserved
5:3	**Component 2 Density.** This field identifies the size of the 2nd Flash component. If there is not 2nd Flash component, the contents of this field are undefined. 000 = 512 KB 001 = 1 MB 010 = 2 MB 011 = 4 MB 100 = 8 MB 101 = 16 MB 111 = Reserved
2:0	**Component 1 Density.** This field identifies the size of the 1st or only Flash component. 000 = 512 KB 001 = 1 MB 010 = 2 MB 011 = 4 MB 100 = 8 MB 101 = 16 MB 111 = Reserved This field is defaulted to "101b" (16 MB) after reset. In non-descriptor mode, only one flash component is supported and all accesses to flash will be to this component.

22.2.2.2 FLILL—Flash Invalid Instructions Register (Flash Descriptor Registers)

Memory Address: FCBA + 004h Default Value: h
Size: 32 bits

Bits	Description
31:24	**Invalid Instruction 3**. See definition of Invalid Instruction 0
23:16	**Invalid Instruction 2**. See definition of Invalid Instruction 0
15:8	**Invalid Instruction 1**. See definition of Invalid Instruction 0
7:0	**Invalid Instruction 0**. Op-code for an invalid instruction in the that the Flash Controller should protect against such as Chip Erase. This byte should be set to 0 if there are no invalid instructions to protect against for this field. Op-codes programmed in the Software Sequencing Opcode Menu Configuration and Prefix-Opcode Configuration are not allowed o use any of the Invalid Instructions listed in this register.

22.2.2.3 FLPB—Flash Partition Boundary Register (Flash Descriptor Registers)

Memory Address: FCBA + 008h Default Value: h
Size: 32 bits

Bits	Description
31:13	Reserved
12:0	**Flash Partition Boundary Address (FPBA)**. This register specifies Flash Boundary Address bits[24:12] that logically divides the flash space into two partitions, a lower and an upper partition. The lower and upper partitions can support SPI flash parts with different attributes between partitions that are defined in the LVSCC and UVSCC. **NOTE:** All flash space in each partition must have the same in the VSCC attributes, even if it spans between different flash parts. **NOTE:** If this register is set to all 0s, then there is only one partition, the upper partition, and the entire address space has uniform erasable sector sizes, write granularity, and write state required settings. The FPBA must reside on an erasable sector boundary.

22.2.3 Flash Descriptor Region Section

The following section of the Flash Descriptor is used to identify the different Flash Regions

Flash Regions:

- If a particular region is not using SPI Flash, the particular region should be disabled by setting the Region Base to all 1's, and the Region Limit to all 0's (base is higher than the limit)
- For each region except FLREG0, the Flash Controller must have a default Region Base of FFFh and the Region Limit to 000h within the Flash Controller in case the Number of Regions specifies that a region is not used.

22.2.3.1 FLREG0—Flash Region 0 (Flash Descriptor) Register (Flash Descriptor Registers)

Memory Address: FRBA + 000h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved
28:16	**Region Limit.** This specifies address bits 24:12 for the Region Limit.
15:13	Reserved
12:0	**Region Base.** This specifies address bits 24:12 for the Region Base.

22.2.3.2 FLREG1—Flash Region 1 (BIOS) Register (Flash Descriptor Registers)

Memory Address: FRBA + 004h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved
28:16	**Region Limit.** This specifies address bits 24:12 for the Region Limit.
15:13	Reserved
12:0	**Region Base.** This specifies address bits 24:12 for the Region Base. **NOTE:** If the BIOS region is not used, the Region Base must be programmed to 1FFFh and the Region Limit to 0000h to disable the region.

22.2.3.3 FLREG2—Flash Region 2 (ME) Register (Flash Descriptor Registers)

Memory Address: FRBA + 008h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved
28:16	**Region Limit.** This specifies address bits 24:12 for the Region Limit.
15:13	Reserved
12:0	**Region Base.** This specifies address bits 24:12 for the Region Base. **NOTE:** If the Intel Management Engine region is not used, the Region Base must be programmed to 1FFFh and the Region Limit to 0000h to disable the region.

22.2.3.4 FLREG3—Flash Region 3 (GbE) Register (Flash Descriptor Registers)

Memory Address: FRBA + 00Ch Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved
28:16	**Region Limit.** This specifies address bits 24:12 for the Region Limit. **NOTE:** The maximum Region Limit is 128KB above the region base.
15:13	Reserved
12:0	**Region Base.** This specifies address bits 24:12 for the Region Base. **NOTE:** If the GbE region is not used, the Region Base must be programmed to 1FFFh and the Region Limit to 0000h to disable the region.

22.2.3.5 FLREG4—Flash Region 4 (Platform Data) Register (Flash Descriptor Registers)

Memory Address: FRBA + 010h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved
28:16	**Region Limit.** This specifies address bits 24:12 for the Region Limit. **NOTE:** The maximum Region Limit is 128KB above the region base.
15:13	Reserved
12:0	**Region Base.** This specifies address bits 24:12 for the Region Base. **NOTE:** If the Platform Data region is not used, the Region Base must be programmed to 1FFFh and the Region Limit to 0000h to disable the region.

22.2.4 Flash Descriptor Master Section

22.2.4.1 FLMSTR1—Flash Master 1 (Host CPU/ BIOS) (Flash Descriptor Registers)

Memory Address: FMBA + 000h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved, must be zero
28	**Platform Data Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
27	**GbE Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
26	**ME Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
25	**Host CPU/BIOS Master Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses. Bit 25 is a don't care as the primary master always has read/write permissions to it's primary region
24	**Flash Descriptor Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
23:21	Reserved, must be zero
20	**Platform Data Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
19	**GbE Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
18	**ME Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
17	**Host CPU/BIOS Master Region Read Access**. If the bit is set, this master can read that particular region through register accesses. Bit 17 is a don't care as the primary master always has read/write permissions to it's primary region
16	**Flash Descriptor Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
15:0	**Requester ID**. This is the Requester ID of the Host processor. This must be set to 0000h.

22.2.4.2 FLMSTR2—Flash Master 2 (ME) (Flash Descriptor Registers)

Memory Address: FMBA + 004h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved, must be zero
28	**Platform Data Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
27	**GbE Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
26	**ME Master Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses. Bit 26 is a don't care as the primary master always has read/write permissions to it's primary region
25	**Host CPU/BIOS Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
24	**Flash Descriptor Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
23:21	Reserved, must be zero
20	**Platform Data Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
19	**GbE Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
18	**ME Master Region Read Access**. If the bit is set, this master can read that particular region through register accesses. Bit 18 is a don't care as the primary master always has read/write permissions to it's primary region
17	**Host CPU/BIOS Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
16	**Flash Descriptor Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
15:0	**Requester ID**. This is the Requester ID of the Intel Management Engine. This must be set to 0000h.

22.2.4.3 FLMSTR3—Flash Master 3 (GbE) (Flash Descriptor Registers)

Memory Address: FMBA + 008h Default Value: h
Size: 32 bits

Bits	Description
31:29	Reserved, must be zero
28	**Platform Data Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
27	**GbE Master Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses. Bit 27 is a don't care as the primary master always has read/write permissions to it's primary region
26	**ME Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
25	**Host CPU/BIOS Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
24	**Flash Descriptor Region Write Access**. If the bit is set, this master can erase and write that particular region through register accesses.
23:21	Reserved, must be zero
20	**Platform Data Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
19	**GbE Master Region Read Access**. If the bit is set, this master can read that particular region through register accesses. Bit 19 is a don't care as the primary master always has read/write permissions to it's primary region
18	**ME Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
17	**Host CPU/BIOS Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
16	**Flash Descriptor Region Read Access**. If the bit is set, this master can read that particular region through register accesses.
15:0	**Requester ID**. This is the Requester ID of the GbE. This must be set to 0218h.

22.2.5 Descriptor Upper Map Section

22.2.5.1 FLUMAP1—Flash Upper Map 1 (Flash Descriptor Registers)

Memory Address: FDBAR + EFCh Default Value: 0000FFFFh
Size: 32 bits

Bits	Default	Description
31:16	0	Reserved
15:8	1	**ME VSCC Table Length (VTL).** Identifies the 1s based number of DWORDS contained in the VSCC Table. Each SPI component entry in the table is 2 DWORDS long.
7:0	1	**ME VSCC Table Base Address (VTBA).** This identifies address bits [11:4] for the VSCC Table portion of the Flash Descriptor. Bits [24:12] and bits [3:0] are 0. **NOTE:** VTBA should be above the offset for MCHSTRP0 and below FLUMAP1. It is recommended that this address is set based on the anticipated maximum number of different flash parts entries.

22.2.6 Intel ME Vendor Specific Component Capabilities Table

Entries in this table allow support for a SPI flash part for Intel® Quiet System Technology. BIOS will still need to set up the proper VSCC registers for BIOS and Integrated Gigabit Ethernet usage.

Each VSCC table entry is composed of two 32 bit fields: JEDEC ID and the corresponding VSCC value.

22.2.6.1 JID0—JEDEC-ID 0 Register (Flash Descriptor Registers)

Memory Address: VTBA + 000h Default Value:
Size: 32 bits

Bits	Description
31:24	Reserved
23:16	**SPI Component Device ID 1.** This field identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).
15:8	**SPI Component Device ID 0.** This field identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).
7:0	**SPI Component Vendor ID.** This field identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).

22.2.6.2 VSCC0—Vendor Specific Component Capabilities 0 (Flash Descriptor Registers)

Memory Address: VTBA + 004h Default Value:
Size: 32 bits

Note: In this table “Lower” applies to characteristics of all flash space below the Flash Partition Boundary Address (FPBA). “Upper” applies to characteristics of all flash space above the FPBA.

Bits	Description
31:16	**Lower Erase Opcode (LEO).** This register must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
23:21	Reserved
20	**Lower Write Enable on Write Status (LWEWS)**. 0 = No write to the SPI flash’s status register required prior to a write 1 = A write of 00h to the SPI flash’s status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 2. Bit 20 and bit 19 should NOT be both set to 1.
19	**Lower Write Status Required (LWSR)**. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash’s status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. Bit 20 and bit 19 should NOT be both set to 1. 2. Bit 19 should not be set if the flash part does not support the opcode 50h to unlock the status register.
18	**Lower Write Granularity (LWG)**. 0 = 1 Byte 1 = 64 Byte
17:16	**Lower Block/Sector Erase Size (LBES).** This field identifies the erasable sector size for all Flash space below the flash partition boundary address. 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB
15:8	**Upper Erase Opcode (UEO).** This register must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
7:5	Reserved

Bits	Description
4	**Upper Write Enable on Write Status (UWEWS).** 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 2. Bit 4 and bit 3 should NOT be both set to 1.
3	**Upper Write Status Required (UWSR).** 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. Bit 4 and bit 3 should NOT be both set to 1. 2. Bit 3 should not be set if the flash part does not support the opcode 50h to unlock the status register.
2	**Upper Write Granularity (UWG).** 0 = 1 Byte 1 = 64 Bytes
1:0	**Upper Block/Sector Erase Size (UBES).** This field identifies the erasable sector size for all Flash components. 00 = 256 Bytes 01 = 4 KB 10 = 8 KB 11 = 64 KB

22.2.6.3 JIDn—JEDEC-ID Register n (Flash Descriptor Registers)

Memory Address: VTBA + (n*8)h Default Value:
Size: 32 bits

Note: "n" is an integer denoting the index of the Intel ME VSCC table.

Bits	Description
31:24	Reserved
23:16	**SPI Component Device ID 1.** This field identifies the second byte of the Device ID of the SPI Flash Component. This is the third byte returned by the Read JEDEC-ID command (opcode 9Fh).
15:8	**SPI Component Device ID 0.** This field identifies the first byte of the Device ID of the SPI Flash Component. This is the second byte returned by the Read JEDEC-ID command (opcode 9Fh).
7:0	**SPI Component Vendor ID.** This field identifies the one byte Vendor ID of the SPI Flash Component. This is the first byte returned by the Read JEDEC-ID command (opcode 9Fh).

22.2.6.4 VSCCn—Vendor Specific Component Capabilities n (Flash Descriptor Registers)

Memory Address: VTBA + 004h + (n*8)h Default Value:
Size: 32 bits

Note: "n" is an integer denoting the index of the Intel ME VSCC table.

Note: In this table "Lower" applies to characteristics of all flash space below the Flash Partition Boundary Address (FPBA). "Upper" applies to characteristics of all flash space above the FPBA.

Bits	Description
31:16	**Lower Erase Opcode (LEO).** This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
23:21	Reserved
20	**Lower Write Enable on Write Status (LWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 2. Bit 20 and bit 19 should NOT be both set to 1.
19	**Lower Write Status Required (LWSR)**. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. Bit 20 and bit 19 should NOT be both set to1. 2. Bit 19 should not be set if the flash part does not support the opcode 50h to unlock the status register.
18	**Lower Write Granularity (LWG)**. 0 = 1 Byte 1 = 64 Byte
17:16	**Lower Block/Sector Erase Size (LBES)**. This field identifies the erasable sector size for all Flash space below the flash partition boundary address. Valid Bit Settings: 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB
15:8	**Upper Erase Opcode (UEO)**. This field must be programmed with the Flash erase instruction opcode that corresponds to the erase size that is in LBES.
7:5	Reserved

Bits	Description
4	**Upper Write Enable on Write Status (UWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. **NOTES:** 1. This bit should not be set to 1 if the SPI flash status register is non-volatile. This may lead to premature flash wear out. 2. Bit 4 and bit 3 should NOT be both set to 1.
3	**Upper Write Status Required (UWSR)**. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. **NOTES:** 1. Bit 4 and bit 3 should NOT be both set to 1. 2. Bit 3 should not be set if the flash part does not support the opcode 50h to unlock the status register.
2	**Upper Write Granularity (UWG)**. 0 = 1 Byte 1 = 64 Bytes
1:0	**Upper Block/Sector Erase Size (UBES)**. This field identifies the erasable sector size for all Flash components. 00 = 256 Bytes 01 = 4 KB 10 = 8 KB 11 = 64 KB

22.3 OEM Section

Memory Address: F00h Default Value:
Size: 256 Bytes

256 Bytes are reserved at the top of the Flash Descriptor for use by the OEM. The information stored by the OEM can only be written during the manufacturing process as the Flash Descriptor read/write permissions must be set to Read Only when the computer leaves the manufacturing floor. The ICH Flash controller does not read this information. FFh is suggested to reduce programming time.

22.4 GbE SPI Flash Program Registers

The GbE Flash registers are memory-mapped with a base address MBARB found in the GbE LAN register chapter Device 25: Function 0: Offset 14h. The individual registers are then accessible at MBARB + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

Note: These register are only applicable when SPI flash is used in descriptor mode.

Table 22-2. Gigabit LAN SPI Flash Program Register Address Map (GbE LAN Memory Mapped Configuration Registers)

MBARB + Offset	Mnemonic	Register Name	Default	Type
00h–03h	GLFPR	Gigabit LAN Flash Primary Region	00000000h	RO
04h–05h	HSFSTS	Hardware Sequencing Flash Status	0000h	RO, R/WC, R/W
06h–07h	HSFCTL	Hardware Sequencing Flash Control	0000H	R/W, R/WS
08h–0Bh	FADDR	Flash Address	00000000h	R/W
0Ch–0Fh	Reserved	Reserved	00000000h	
10h–13h	FDATA0	Flash Data 0	00000000h	R/W
14h–4Fh	Reserved	Reserved	00000000h	
50h–53h	FRAP	Flash Region Access Permissions	00000000h	RO, R/W
54h–57h	FREG0	Flash Region 0	00000000h	RO
58h–5Bh	FREG1	Flash Region 1	00000000h	RO
5Ch–5F	FREG2	Flash Region 2	00000000h	RO
60h–63h	FREG3	Flash Region 3	00000000h	RO
64h–73h	Reserved	Reserved for Future Flash Regions		
74h–77h	FPR0	Flash Protected Range 0	00000000h	R/W
78h–7Bh	FPR1	Flash Protected Range 1	00000000h	R/W
7Ch–8Fh	Reserved	Reserved		
90h	SSFSTS	Software Sequencing Flash Status	00h	RO, R/W
91h–93h	SSFCTL	Software Sequencing Flash Control	000000h	R/W
94h–95h	PREOP	Prefix Opcode Configuration	0000h	R/W
96h–97h	OPTYPE	Opcode Type Configuration	0000h	R/W
98h–9Fh	OPMENU	Opcode Menu Configuration	00000000 00000000h	R/W
A0h–DFh	Reserved	Reserved		

22.4.1 GLFPR –Gigabit LAN Flash Primary Region Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 00h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**GbE Flash Primary Region Limit (PRL)—** RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	Reserved
12:0	**GbE Flash Primary Region Base (PRB)** — RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

22.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 04h	Attribute:	RO, R/WC, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15	**Flash Configuration Lock-Down (FLOCKDN)**— R/W. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel ME enabled system.
14	**Flash Descriptor Valid (FDV)—** RO. This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not '1', software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—** RO. This bit reflects the value the Flash Descriptor Override Pin-Strap. 0 = No override 1 = The Flash Descriptor Override strap is set
12:6	Reserved
5	**SPI Cycle In Progress (SCIP)—** RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	**Block/Sector Erase Size (BERASE)** — RO. This field identifies the erasable sector size for all Flash components. 00 = 256 Byte 01 = 4 K Byte 10 = 8 K Byte 11 = 64 K Byte If the FLA is less than FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA is greater or equal to FPBA then this field reflects the value in the UVSCC.UBES register.
2	**Access Error Log (AEL)**— R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'
1	**Flash Cycle Error (FCERR)** — R/W/C. Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs due to a global reset or host partition reset in an Intel ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	**Flash Cycle Done (FDONE)** — R/W/C. The ICH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

22.4.3 HSFC—Hardware Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 06h
Default Value: 0000h
Attribute: R/W, R/WS
Size: 16 bits

Bit	Description
15:10	Reserved
9:8	**Flash Data Byte Count (FDBC) —** R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The content's of this register are 0s based with 0b representing 1 byte and 11b representing 4 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	**FLASH Cycle (FCYCLE)** — R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 4 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 4 bytes by setting FDBC) 11 = Block Erase
0	**Flash Cycle Go (FGO)** — R/W/S. A write to this register with a '1' in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

22.4.4 FADDR—Flash Address Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 08h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:25	Reserved
24:0	**Flash Linear Address (FLA) —** R/W. The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions.

22.4.5 FDATA0—Flash Data 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 10h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Flash Data 0 (FD0)** — R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…8-23-22-…16-31…24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

22.4.6 FRAP—Flash Regions Access Permissions Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 50h
Default Value: 00000808h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:28	Reserved
27:25	**GbE Master Write Access Grant (GMWAG)** — R/W. Each bit 27:25 corresponds to Master[3:1]. GbE can grant one or more masters write access to the GbE region 3 overriding the permissions in the Flash Descriptor. Master[1] is Host CPU/BIOS, Master[2] is Intel Management Engine, Master[3] is Host processor/GbE. The contents of this register are locked by the FLOCKDN bit.
24:20	Reserved
19:17	**GbE Master Read Access Grant (GMRAG) —** R/W. Each bit 19:17 corresponds to Master[3:1]. GbE can grant one or more masters read access to the GbE region 3 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel Management Engine, Master[3] is GbE. The contents of this register are locked by the FLOCKDN bit
16:12	Reserved
11:8	**GbE Region Write Access (GRWA) —** RO. Each bit 11:8 corresponds to Regions 3:0. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 3.Master Region Write Access OR a particular master has granted GbE write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set.
7:4	Reserved
3:0	**GbE Region Read Access (GRRA)** — RO. Each bit 3:0 corresponds to Regions 3:0. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 3.Master Region Write Access OR a particular master has granted GbE read permissions in their Master Read Access Grant register.

22.4.7 FREG0—Flash Region 0 (Flash Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 54h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 0 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

22.4.8 FREG1—Flash Region 1 (BIOS Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 58h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

22.4.9 FREG2—Flash Region 2 (ME) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 5Ch Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 2 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

22.4.10 FREG3—Flash Region 3 (GbE) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 60h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL) —** RO. This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)** — RO. This specifies address bits 24:12 for the Region 3 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

22.4.11 FPR0—Flash Protected Range 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 74h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.4.12 FPR1—Flash Protected Range 1 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 78h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit —** R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable** — R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base** — R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

22.4.13 SSFS—Software Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 90h	Attribute:	RO, R/WC
Default Value:	00h	Size:	8 bits

Note: The Software Sequencing control and status registers are reserved if the hardware sequencing control and status registers are used.

Bit	Description
7:5	Reserved
4	**Access Error Log (AEL) —** RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	**Flash Cycle Error (FCERR) —** R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system.
2	**Cycle Done Status** — R/WC. The ICH sets this bit to 1 when the SPI Cycle completes (i.e., SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	**SPI Cycle In Progress (SCIP)** — RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

22.4.14 SSFC—Software Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 91h
Default Value: 000000h
Attribute: R/W
Size: 24 bits

Bit	Description
23:19	Reserved
18:16	**SPI Cycle Frequency (SCF) —** R/W. This register sets frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, etc.) except for the read cycle which always run at 20MHz. 000 = 20 MHz 001 = 33 MHz All other values = Reserved. This register is locked when the SPI Configuration Lock-Down bit is set.
15	Reserved
14	**Data Cycle (DS)** — R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares
13:8	**Data Byte Count (DBC)** — R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 3. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00b, then there is 1 byte to transfer and that 11b means there are 4 bytes to transfer.
7	Reserved
6:4	**Cycle Opcode Pointer (COP)** — R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	**Sequence Prefix Opcode Pointer (SPOP)** — R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the ICH supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	**Atomic Cycle Sequence (ACS)** — R/W. When set to 1 along with the SCGO assertion, the ICH will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: • Atomic Sequence Prefix Command (8-bit opcode only) • Primary Command specified below by software (can include address and data) • Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	**SPI Cycle Go (SCGO)** — R/WS. This bit always returns 0 on reads. However, a write to this register with a '1' in this bit starts the SPI cycle defined by the other bits of this register. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	Reserved

22.4.15 PREOP—Prefix Opcode Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 94h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	**Prefix Opcode 1**— R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	**Prefix Opcode 0** — R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

NOTE: This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

22.4.16 OPTYPE—Opcode Type Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 96h Attribute: R/W
Default Value: 0000h Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

Note: The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, “Chip Erase” and “Auto-Address Increment Byte Program”).

Bit	Description
15:14	**Opcode Type 7** — R/W. See the description for bits 1:0
13:12	**Opcode Type 6** — R/W. See the description for bits 1:0
11:10	**Opcode Type 5** — R/W. See the description for bits 1:0
9:8	**Opcode Type 4** — R/W. See the description for bits 1:0
7:6	**Opcode Type 3** — R/W. See the description for bits 1:0
5:4	**Opcode Type 2** — R/W. See the description for bits 1:0
3:2	**Opcode Type 1** — R/W. See the description for bits 1:0
1:0	**Opcode Type 0** — R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

NOTE: This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

22.4.17 OPMENU—Opcode Menu Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 98h	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64 bits

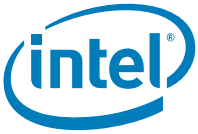
Eight entries are available in this register to give GbE a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Note: It is recommended that GbE avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	**Allowable Opcode 7** — R/W. See the description for bits 7:0
55:48	**Allowable Opcode 6** — R/W. See the description for bits 7:0
47:40	**Allowable Opcode 5** — R/W. See the description for bits 7:0
39:32	**Allowable Opcode 4** — R/W. See the description for bits 7:0
31:24	**Allowable Opcode 3** — R/W. See the description for bits 7:0
23:16	**Allowable Opcode 2** — R/W. See the description for bits 7:0
15:8	**Allowable Opcode 1** — R/W. See the description for bits 7:0
7:0	**Allowable Opcode 0** — R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

§ §



23 Thermal Sensor Registers (D31:F6)

23.1 PCI Bus Configuration Registers

Table 23-1. Thermal Sensor Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	TBD	RO
04h–05h	CMD	Command Register	0000h	R/W, RO
06h–07h	STS	Device Status	0010h	R/WC, RO
08h	RID	Revision ID	00h	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	80h	RO
0Bh	BCC	Base Class Code	11h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	LT	Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
0Fh	BIST	Built-in Self Test	00h	RO
10h–13h	TBAR	Thermal Base Address (Memory)	00000004h	R/W, RO
14h–17h	TBARH	Thermal Base Address High DWord	00000000h	RO
2Ch–2Dh	SVID	Subsystem Vendor Identifier	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identifier	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	RW
3Dh	INTPN	Interrupt Pin	TBD	RO
40h–43h	TBARB	BIOS Assigned Thermal Base Address	00000004h	R/W, RO
44h–47h	TBARBH	BIOS Assigned BA High DWord	00000000h	R/W
50h–51h	PID	Power Management Identifiers	0001h	RO
52h–53h	PC	Power Management Capabilities	0022h	RO
54h–57h	PCS	Power Management Control and Status	0000h	R/W, RO

23.1.1 VID—Vendor Identification

Offset Address: 00h–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:0	**Vendor ID** — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

23.1.2 DID—Device Identification

Offset Address: 02h–03h
Default Value: TBD
Attribute: RO
Size: 16 bit

Bit	Description
15:0	**Device ID (DID)** — RO. Indicates the device number assigned by the SIG.

23.1.3 CMD—Command

Address Offset: 04h–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)** — RW. Enables the device to assert an INTx#. 0 = When cleared, the INTx# signal may be asserted. 1 = When set, the Thermal logic's INTx# signal will be de-asserted.
9	FBE (Fast Back to Back Enable) — RO. Not implemented. Hardwired to 0.
8	SEN (SERR Enable) — RO. Not implemented. Hardwired to 0.
7	WCC (Wait Cycle Control) — RO. Not implemented. Hardwired to 0.
6	PER (Parity Error Response) — RO. Not implemented. Hardwired to 0.
5	VPS (VGA Palette Snoop) — RO. Not implemented. Hardwired to 0.
4	MWI (Memory Write and Invalidate Enable) — RO. Not implemented. Hardwired to 0.
3	SCE (Special Cycle Enable) — RO. Not implemented. Hardwired to 0.
2	BME (Bus Master Enable) — RO. Not implemented. Hardwired to 0.
1	**Memory Space Enable (MSE)** — RW. 0 = Disable 1 = Enable. Enables memory space accesses to the Thermal registers.
0	IOS (I/O Space) — RO. The Thermal logic does not implement IO Space; therefore, this bit is hardwired to 0.

23.1.4 STS—Status

Address Offset: 06h–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)** — R/WC. This bit is set whenever a parity error is seen on the internal interface for this function, regardless of the setting of bit 6 in the command register. Software clears this bit by writing a '1' to this bit location.
14	SERR# Status (SERRS) — RO. Not implemented. Hardwired to 0.
13	Received Master Abort (RMA) — RO. Not implemented. Hardwired to 0.
12	Received Target Abort (RTA) — RO. Not implemented. Hardwired to 0.
11	Signaled Target-Abort (STA) — RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEVT) — RO. Does not apply. Hardwired to 0.
8	Master Data Parity Error (MDPE) — RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FBC) — RO. Does not apply. Hardwired to 0.
6	Reserved
5	66 MHz Capable (C66) — RO. Does not apply. Hardwired to 0.
4	**Capabilities List Exists (CLIST)** — RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (IS)** — RO. Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).
2:0	Reserved

23.1.5 RID—Revision Identification

Address Offset: 08h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)** — RO. Indicates the device specific revision identifier.

23.1.6 PI— Programming Interface

Address Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Programming Interface (PI)** — RO. ICH Thermal logic has no standard programming interface.

23.1.7 SCC—Sub Class Code

Address Offset: 0Ah
Default Value: 80h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** — RO. Value assigned to ICH Thermal logic.

23.1.8 BCC—Base Class Code

Address Offset: 0Bh
Default Value: 11h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)** — RO. Value assigned to ICH Thermal logic.

23.1.9 CLS—Cache Line Size

Address Offset: 0Ch
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Cache Line Size (CLS)** — RO. Does not apply to PCI Bus Target-only devices.

23.1.10 LT—Latency Timer

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Latency Timer (LT)** — RO. Does not apply to PCI Bus Target-only devices.

23.1.10.1 HTYPE—Header Type

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD)** — RO. This bit is 0 because a multi-function device only needs to be marked as such in Function 0, and the Thermal registers are not in Function 0.
6:0	**Header Type (HTYPE)** — RO. Implements Type 0 Configuration header.

23.1.11 BIST—Built-in Self Test

Address Offset: 0Fh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Built-in Self Test (BIST)** — RO. Not implemented. Hardwired to 00h.

23.1.12 TBAR—Thermal Base

Address Offset: 10h–13h
Default Value: 00000004h
Attribute: RW, RO
Size: 32 bits

This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when the Command (CMD) register Memory Space Enable (MSE) bit is set and either TBAR[31:12] or TBARH are programmed to a non-zero address. This BAR is owned by the Operating System, and allows the OS to locate the Thermal registers in system memory space.

Bit	Description
31:12	**Thermal Base Address (TBA)** — RW. This field provides the base address for the Thermal logic memory mapped configuration registers. 4 KB bytes are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	**Prefetchable (PREF)** — RO. Indicates that this BAR is NOT pre-fetchable.
2:1	**Address Range (ADDRNG)** — RO. Indicates that this BAR can be located anywhere in 64 bit address space.
0	**Space Type (SPTYP)** — RO. Indicates that this BAR is located in memory space.

23.1.13 TBARH—Thermal Base High DWord

Address Offset: 14h–17h
Default Value: 00000000h
Attribute: RW, RO
Size: 32 bits

This BAR extension holds the high 32 bits of the 64 bit TBAR. In conjunction with TBAR, it creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers.

Bit	Description
31:0	**Thermal Base Address High (TBAH)** — RW. TBAR bits 61:32.

23.1.14 SVID—Subsystem Vendor ID

Address Offset: 2Ch–2Dh Attribute: R/WO
Default Value: 0000h Size: 16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by $D3_{HOT}$ to D0 reset.

Bit	Description
15:0	**SVID (SVID)** — R/WO. These RWO bits have no ICH10 functionality.

23.1.15 SID—Subsystem ID

Address Offset: 2Eh–2Fh Attribute: R/WO
Default Value: 0000h Size: 16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by $D3_{HOT}$ to D0 reset.

Bit	Description
15:0	**SID (SAID)** — R/WO. These RWO bits have no ICH10 functionality.

23.1.16 CAP_PTR —Capabilities Pointer

Address Offset: 34h Attribute: RO
Default Value: 50h Size: 8 bits

Bit	Description
7:0	**Capability Pointer (CP)** — RO. Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

23.1.17 Offset 3Ch – INTLN—Interrupt Line

Address Offset: 3Ch Attribute: RW
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Interrupt Line** — RW. ICH10 hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

23.1.18 INTPN—Interrupt Pin

Address Offset: 3Dh
Default Value: TBD
Attribute: RO
Size: 8 bits

Bit	Description
7:4	Reserved
3:0	**Interrupt Pin** — RO. This reflects the value of the Device 31 interrupt pin bits 27:24 (TTIP) in chipset configuration space.

23.1.19 TBARB—BIOS Assigned Thermal Base Address

Address Offset: 40h–43h
Default Value: 00000004h
Attribute: RW,RO
Size: 32 bits

This BAR creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space. If both TBAR and TBARB are programmed, then the OS and BIOS each have their own independent “view” of the Thermal registers, and must use the TSIU, TCIU, and TBIU registers to denote Thermal registers ownership/ availability.

Bit	Description
31:12	**Thermal Base Address (TBA)** — RW. This field provides the base address for the Thermal logic memory mapped configuration registers. 4K B bytes are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	**Prefetchable (PREF)** — RO. Indicates that this BAR is NOT pre-fetchable.
2:1	**Address Range (ADDRNG)** — RO. Indicates that this BAR can be located anywhere in 64 bit address space.
0	**Space Type Enable (SPTYPEN)** — RW. 0 = Disable. 1 = Enable. When set to 1b by software, enables the decode of this memory BAR.

23.1.20 TBARBH—BIOS Assigned Thermal Base High DWord

Address Offset: 44h–47h
Default Value: 00000000h
Attribute: RW
Size: 32 bits

This BAR extension holds the high 32 bits of the 64 bit TBARB.

Bit	Description
31:0	**Thermal Base Address High (TBAH)** — RW. TBAR bits 61:32.

23.1.21 PID—PCI Power Management Capability ID

Address Offset: 50h–51h
Default Value: 0001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Indicates that this is the last capability structure in the list.
7:0	**Cap ID (CAP)** — RO. Indicates that this pointer is a PCI power management capability

23.1.22 PC—Power Management Capabilities

Address Offset: 52h–53h
Default Value: 0022h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support** — RO. Indicates PME# is not supported
10	**D2_Support** — RO. The D2 state is not supported.
9	**D1_Support** — RO. The D1 state is not supported.
8:6	**Aux_Current** — RO. PME# from D3COLD state is not supported, therefore this field is 000b.
5	**Device Specific Initialization (DSI)** — RO. Indicates that device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)** — RO. Does not apply. Hardwired to 0.
2:0	**Version (VS)** — RO. Indicates support for Revision 1.2 of the *PCI Power Management Specification*.

23.1.23 PCS—Power Management Control And Status

Address Offset: 54h–57h
Default Value: 0000h
Attribute: RW, RO
Size: 32 bits

Bit	Description
31:24	**Data** — RO. Does not apply. Hardwired to 0s.
23	**Bus Power/Clock Control Enable (BPCCE)** — RO. Hardwired to 0.
22	**B2/B3 Support (B23)** — RO. Does not apply. Hardwired to 0.
21:16	Reserved
15	**PME Status (PMES)** — RO. This bit is always 0, since this PCI Function does not generate PME#
14:9	Reserved
8	**PME Enable (PMEE)** — RO. This bit is always zero, since this PCI Function does not generate PME#
7:4	Reserved
3	**No Soft Reset** — RO. When set (1), this bit indicates that devices transitioning from $D3_{HOT}$ to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from $D3_{HOT}$ to D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	Reserved
1:0	**Power State (PS)** — R/W. This field is used both to determine the current power state of the Thermal controller and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the $D3_{HOT}$ states, the Thermal controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the $D3_{HOT}$ state to the D0 state, no internal warm (soft) reset is generated.

23.2 Thermal Memory Mapped Configuration Registers (Thermal Sensor - D31:F26)

The base memory for these thermal memory mapped configuration registers is specified in the TBARB (D31:F6:Offset 40h). The individual registers are then accessible at TBARB + Offset.

There are two sensors in the ICH10. Each sensor has a separate configuration register set. Both sensors must be configured together.

Table 23-2. Thermal Memory Mapped Configuration Register Address Map

Offset	Mnemonic	Register Name	Default	Type
1h	TS0E	Thermal Sensor 0 Enable	00h	R/W
2h	TS0S	Thermal Sensor 0 Enable	00h	R/W
4h	TS0TTP	Thermal Sensor 0 Catastrophic Trip Point	00000000h	R/W
8h	TS0C0	Thermal Sensor 0 Catastrophic Lock Down	00h	R/W
0Eh	TS0PC	Thermal Sensor 0 Policy Control	00h	R/W
41h	TS1E	Thermal Sensor 1 Enable	00h	R/W
42h	TS1S	Thermal Sensor 1 Enable	00h	R/W
44h	TS1TTP	Thermal Sensor 1 Catastrophic Trip Point	00000000h	R/W
48h	TS1C0	Thermal Sensor 1 Catastrophic Lock Down	00h	R/W
4Eh	TS1PC	Thermal Sensor 1 Policy Control	00h	R/W
83h	TS0LOCK	Thermal Sensor 0 Register Lock Control	00h	R/W
C3h	TS1LOCK	Thermal Sensor 1 Register Lock Control	00h	R/W

23.2.1 TSxE—Thermal Sensor [1:0] Enable

Offset Address: Sensor 0: TBARB+01h / Sensor 1: TBARB+41h — Attribute: R/W
Default Value: 00h — Size: 8 bit

Bit	Description
7:0	**Thermal Sensor Enable (TSE)** — R/W. BIOS shall always program this register to the value BAh to enable the thermal sensor. All other values are reserved.

23.2.2 TSxS—Thermal Sensor[1:0] Status

Offset Address: Sensor 0: TBARB+02h
Sensor 1: TBARB+42h
Attribute: RO
Default Value: 00h
Size: 8 bit

Bit	Description
7	**Catastrophic Trip Indicator (CTI)** — RO. 0 = The temperature is below the catastrophic setting. 1 = The temperature is above the catastrophic setting.
6:0	Reserved

23.2.3 TSxTTP—Thermal Sensor [1:0] Catastrophic Trip Point

Offset Address: Sensor 0: TBARB+04h
Sensor 1: TBARB+44h
Attribute: R/W
Default Value: 00h
Size: 32 bit

Bit	Description
31:8	Reserved
7:0	**Catastrophic Trip Point Setting (CTPS)** — R/W. These bits set the catastrophic trip point. BIOS will program these bits. These bits are lockable via TSCO.bit 7.

23.2.4 TSxCO—Thermal Sensor [1:0] Catastrophic Lock-Down

Offset Address: Sensor 0: TBARB+08h
Sensor 1: TBARB+48h
Attribute: R/W
Default Value: 00h
Size: 8 bit

Bit	Description
7	**Lock bit for Catastrophic (LBC)** — R/W. 0 = Catastrophic programming interface is unlocked 1 = Locks the Catastrophic programming interface including TSTTP.bits[7:0]. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	Reserved

23.2.5 TSxPC—Thermal Sensor [1:0] Policy Control

Offset Address:	Sensor 0: TBARB+0Eh Sensor 1: TBARB+4Eh	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7	**Policy Lock-Down Bit** — R/W. 0 = This register can be programmed and modified. 1 = Prevents writes to this register. **NOTE:** TSCO.bit 7 and TSLOCK.bit2 must also be 1 when this bit is set to 1. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6	**Catastrophic Power-Down Enable — R/W.** 1 = When set to 1, the power management logic unconditionally transitions to the S5 state when a catastrophic temperature is detected by the sensor.
5:0	Reserved

23.2.6 TSxLOCK—Thermal Sensor [1:0] Register Lock Control

Offset Address:	Sensor 0: TBARB+83h Sensor 1: TBARB+C3h	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7:3	Reserved
2	**Lock Control — R/W.** This bit must be set to 1 when TSPC.bit7 is set to 1.
1:0	Reserved

§ §

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Intel:

AF82801JIB S LB8R AF82801JIR S LB8S