Intel® FPGA Programmable Acceleration Card D5005 Data Sheet


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DS-1058

ID: 683568

Version: 2019.11.04

Contents

1. Introduction

The Intel FPGA Programmable Acceleration Card D5005 (Intel® FPGA PAC D5005) is a PCI Express* Gen 3 x16 compliant card designed to accelerate data center applications.

This datasheet for the Intel FPGA PAC shows electrical, mechanical, compliance, and other key specifications. This datasheet assists data center operators and system integrators to properly deploy the Intel FPGA PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The Intel FPGA PAC is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Acceleration Stack provides a common developer interface to both application and accelerator function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA Interface Manager (FIM).

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-addition of their solution. Developers can use the Accelerator Functional Unit (AFU) Developer's User Guide to get started.

Intel validates each Intel FPGA PAC to support large scale deployments requiring FPGA acceleration.

This platform is targeted for market-specific acceleration in applications such as:

- Finance
- Data Analytics
- Video Transcoding
- Genomics
- Cyber-Security
- High-Performance Computing
- Artificial Intelligence

Note: Throughout this document, any mention of Intel FPGA PAC or Intel FPGA PAC D5005 shall specifically refer to the Intel FPGA Programmable Acceleration Card D5005.

2. Overview

This chapter provides an overview of the Intel FPGA PAC and describes the architecture and components.

2.1. Intel FPGA PAC D5005 Specifications

Figure 1. Conceptual Block Diagram

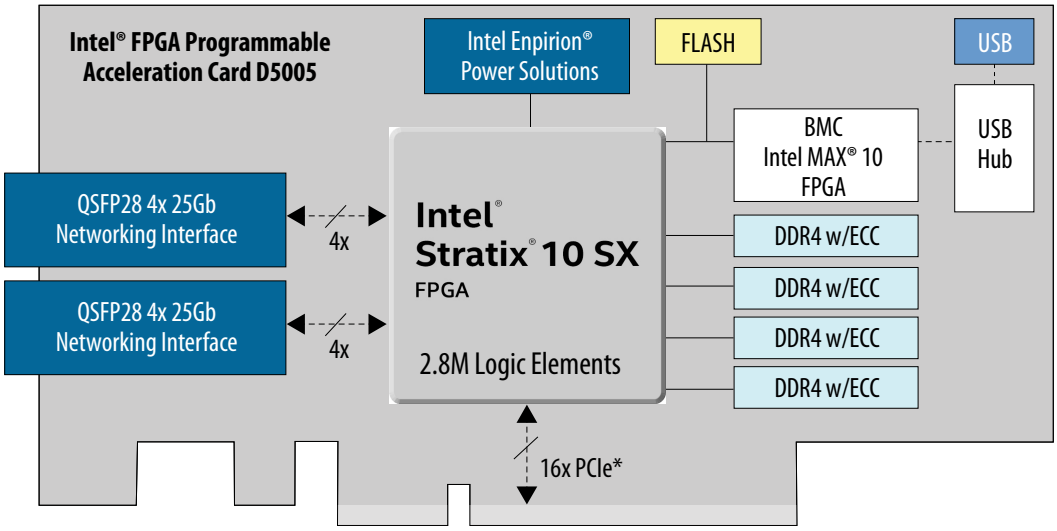


Table 1. Specifications Table

Specification	Value
Power	215 W (Under sufficient cooling capabilities) (1)
Cooling Requirement	Passively cooled. Requires server air flow.
Weight	1 Kilogram
Form Factor	¾ Length, Full height, Dual-slot PCIe* 3.0 CEM specification compliant
Networking Interfaces	Dual QSFP28 Ports: 2x100G
Memory Interfaces	4x 8GB DDR4-2400 with ECC
Management Port	Micro-USB
FPGA Device	1SX280HN2F43E2VG

(1) 65 W from the 12 V slot and 150 W from 12 V 2x4 pin auxiliary power connector. 10 W from the 3.3 V slot is not used.

Note: Initially 1x10G and 4x10G networking capability is supported on each QSFP28 port. Additional configurations will be supported in future releases.

2.2. Intel FPGA PAC Components

2.2.1. Intel Stratix® 10 FPGA

Intel Stratix® 10 FPGAs feature industry-leading programmable logic built on 14 nm process technology that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Intel Stratix 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build a versatile set of acceleration solutions.

When developing the accelerator function for the Intel FPGA PAC, select the 1SX280HN2F43E2VG device.

2.2.2. Power

Given a specific airflow, the Intel FPGA PAC D5005 can dissipate up to 189 W of power, of which up to 137 W can come from the FPGA. If the airflow is increased, the Intel FPGA PAC D5005 may be able to dissipate up to 215 W; however, you shall bear the responsibility of thermal validation of these conditions.

The Thermal Design Power (TDP) (215 W) is based on the maximum current, per the PCIe specification of 5.4 A from the 12 V-PCIe slot and 12.5 A from the 12 V-Auxiliary 2x4 PCIe power connector and requires optimized cooling conditions. The card TDP is limited to 189 W under the Thermal and Airflow requirement conditions.

As a developer or solution provider, you must design the AFU to stay within these power guidelines. If the AFU exceeds this limit or the limit provided by the qualified server vendor, Board Management Controller (BMC) safeguards will shut down the Intel FPGA PAC. Typical server BMC safeguards will likely shut down the server as well. Functionality and reliability of the server and the Intel FPGA PAC are not supported for AFUs that exceed the specification.

The Intel FPGA PAC source power must be provided from both the 12 V-PCIe slot and the 12V-Auxiliary 2x4 power connector.

The Intel FPGA PAC D5005 is designed to operate under the following conditions:

Table 2.

Operating Condition	Description
No 12 V PCIe slot power, No 12 V Auxiliary Connector Power	Intel FPGA PAC D5005 OFF
Only 12 V PCIe slot power, No 12 V Auxiliary Connector Power	Intel FPGA PAC D5005 OFF
No 12 V PCIe Slot Power, only 12 V Auxiliary Connector power available	Intel FPGA PAC D5005 ON, but limited by the total available power from 12V Aux power connector
12 V PCIe slot power and 12 V Auxiliary Power Connector available	Intel FPGA PAC D5005 ON, normal operation up to maximum power capabilities of the PAC card design

The 12 V-Auxiliary power connector pin assignment defined by the PCIe specification is shown below:

Figure 2. Power Connector

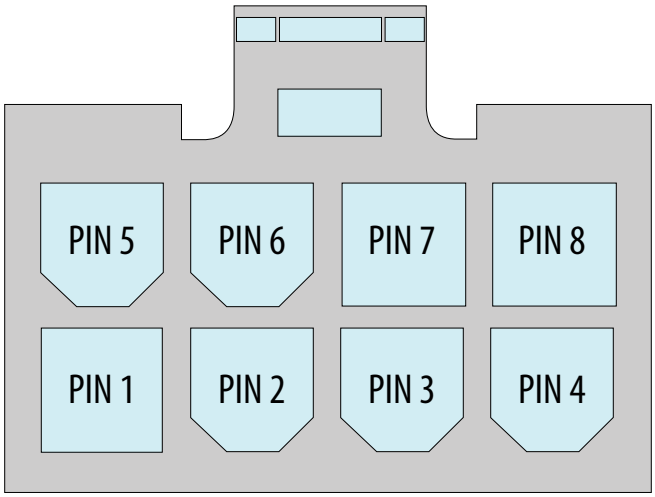


Table 3. 2x4 Auxiliary Power Connector Pin-Out Assignment

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Sense1
5	Ground
6	Sense0
7	Ground
8	Ground

2.2.3. PCIe Interface

The Intel FPGA PAC supports PCI Express Gen 3 data rates of 8 GT/s .

Table 4. PCIe ID and Power/Thermal Budget

Intel FPGA PAC	PCIe Vendor ID (VID)	PCIe Device ID (DID)	PCIe Subsystem Vendor ID (SVID)	PCIe Subsystem ID (SSID)
Intel FPGA Programmable Acceleration Card D5005	0x8086	0x0B2B	0x8086	0x0000

2.2.4. DDR4 SDRAM

The Intel FPGA PAC has four banks of Double Data Rate 4 Synchronous Dynamic Random-Access Memory (DDR4 SDRAM). Each bank is populated with 8 GB DDR4 RDIMM modules for a total of 32 GB. The banks are configured as single rank standard RDIMM modules arranged as 72-bit per bank. The memory width is organized as 64 data bits plus 8 ECC bits. Each DDR4 bank operates up to 1200 MHz (DDR4-2400).

Table 5. Memory Table

Supported Manufacturers	**Micron**
Manufacturer Part Number	MTA9ASF1G72PZ-2G9E1
Type	8 GB 288-pin DDR4 RDIMM
Configuration	1 Gb x 72
Rank	Single Rank
Error detection and correction (ECC)	Yes
Data rate	2400 MT/s

2.2.5. Network Interface

The Intel FPGA PAC has two QSFP28 cages on the I/O panel each of which supports up to 100G Ethernet. The Intel FPGA PAC supports Short Reach (SR) QSFP28 class 1-7 (up to 5 W) optical transceivers and Direct Attached Copper (DAC) cables up to 3 m in length.

Note: The current Intel Acceleration Stack release supports 1x10 Gbps and 4x10 Gbps operation. Other network interface support configurations will be enabled in a future release of the Intel Acceleration Stack.

2.2.6. Field Replaceable Unit Identification EEPROM

A Field Replaceable Unit Identification (FRUID) EEPROM (Microchip 24AA024-I/SN) located at SMBUS address `0xA0` is connected to the SMBUS of the PCIe interface. This FRUID EEPROM is powered by the host server's PCIe 3.3 V auxiliary power provided at the PCIe slot connector. This allows the FRUID EEPROM to be readable even when 12 V power to the slot is not provided by the host server.

Note: OEM-specific part numbers may use a different SMBus address. Check with your OEM for more information.

This FRUID contains board specific information that identifies the card installed into the PCIe slot. The FRUID contains the following information:

- Board Manufacturer
- Board Model Number
- Board Serial Number
- Location of Manufacture
- Date of Manufacture

2.2.7. MAC Address EEPROM

A secondary EEPROM (ST-Microelectronics M24128-BWMN6TP) is used to store the starting MAC address and the count (8) of total MAC addresses for the two network interface ports. Each port contains four unique MAC address information (total of eight MAC address for each Intel FPGA PAC). This information can be read by the BMC and FPGA device.

Note: The starting MAC Address for each board is also provided on the label on the back side of the PCB board. The eight MAC addresses are sequentially incremented from the starting MAC address provided.

2.2.8. Flash Memory

There are two QSPI flash memories: A BMC Firmware Flash (64 Mb) and a FPGA Configuration Flash (2 Gb) used to store the FPGA Interface Manager (FIM).

2.2.9. Control and Support

The following features are available on the Intel FPGA PAC for configuration, control and support:

- PCIe Gen 3 x16
- Board Management Controller (BMC)
- Intel FPGA Download Cable II

Note: Refer to Board Management Controller on page 9 for additional infromation.

3. Board Management Controller

A Board Management Controller (BMC) resides on the Intel FPGA PAC. The BMC is responsible for controlling, monitoring and granting access to board features. The Intel MAX® 10 BMC interfaces with on-board sensors, the FPGA and the flash, and it controls power-on/power-off sequences, FPGA configuration and telemetry data polling. The BMC communicates using the Platform Level Data Model (PLDM) version 1.1.1 protocol. The BMC firmware is field upgradeable over PCIe using the remote system update feature.

Features of the BMC

- Interfaces with sensors, FPGA, flash and QSFPs
- FPGA configuration and reconfiguration
- Controls BMC firmware and Intel Stratix 10 FPGA flash updates. Updates are provided over PCIe.
- Monitors telemetry data (board temperature, voltage and current) and provides protective action when readings are outside of critical threshold
- Reports telemetry data to host BMC via Platform Level Data Model (PLDM) over MCTP SMBus or Standard I^2C
- Supports PLDM over MCTP SMBus via PCIe SMBus. `0xCE` is a 8-bit slave address. Raw 7-bit slave address is `0x67`
- Supports Standard I^2C via PCIe SMBus. The I^2C slave address is `0xBC` (8-bit)
- Intel FPGA Download Cable functionality for the board
- Power up / down sequencing and fault detection with automatic shut-down protection
- Controls programmable FPGA and DDR4 SDRAM clocks for performance throttling if desired
- Controls power and resets on the board
- Acts as a Root of Trust (RoT) and enables the secure update features of the Intel FPGA PAC D5005. The RoT includes features that may help prevent the following:
  - Loading or executing of unauthorized code or designs.
  - Disruptive operations attempted by unprivileged software, privileged software, or the host BMC.
  - Unintended execution of older code or designs with known bugs or vulnerabilities by enabling the BMC to revoke authorization.
- Enforces several other security policies relating to access through various interfaces, as well as protecting the on-board flash through write rate limitation.

Refer to the Intel FPGA PAC D5005 Board Management Controller User Guide for more information.

Related Information

Intel FPGA PAC D5005 Board Management Controller User Guide

3.1. Health Monitoring Features

The Intel FPGA PAC incorporates sensors that allow the host server to read telemetry data from the board such as voltage, current, power, temperatures and network status information from various components on the board. This telemetry data is available via the PLDM interface or over PCIe using the **fpgainfo** tool available with the Intel Acceleration Stack. These sensors reside on the I^2C busses that are connected to the Board Management Controller (BMC) and FPGA device.

Note: The FPGA VCC Core power has a dedicated AVSbus that is separate from any of the I^2C busses.

Note: The QSFP Network ports reside behind the network port controller. See the controller datasheet (Texas Instruments FPC202RHUR) for more information.

Note: The FPGA design can read these sensors directly or through the Board Management Controller using standard PLDM commands and report their status to the host server.

Table 6. Thresholds with Sensor Information

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
12 V Aux Hot Swap Current	12.5 A max				12.5 A	13.2 A	14 A
12 V Aux Hot Swap Voltage	12 V +/-10%	9.6 V	10.2 V	10.5 V	13.2 V	13.5 V	14 V
12 V Aux Hot Swap Temperature	0 °C to 125 °C				118 °C	120 °C	125 °C
12 V PCIe Hot Swap Current	5.5 A max				5.5 A	5.8 A	6 A
12 V PCIe Hot Swap Voltage	12 V +/-10%	9.6 V	10.2 V	10.5 V	13.2 V	13.5 V	14 V
12 V PCIe Hot Swap Temperature	0 °C to 125 °C				118 °C	120 °C	125 °C
3.3 V Regulator Current	20 A max				20 A	22 A	23 A
3.3 V Regulator Voltage	3.3 V +/-5%				3.4 V	3.6 V	3.9 V

continued...

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
3.3 V Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
1.8 V Regulator Current	20 A max				20 A	22 A	23 A
1.8 V Regulator Voltage	1.8 V +/-5%	1.55 V	1.6 V	1.7 V	1.9 V	1.98 V	2.04 V
1.8 V Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCERAM Regulator Current	20 A max				20 A	22 A	23 A
VCCERAM Regulator Voltage	0.9 V +/-30mV	0.7 V	0.8 V	0.85 V	0.95 V	0.99 V	1.08 V
VCCERAM Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCR_GXB Regulator Current	20 A max				20 A	22 A	23 A
VCCR_GXB Regulator Voltage	1.12 V +/-3%	1 V	1.05 V	1.08 V	1.15 V	1.2 V	1.35 V
VCCR_GXB Regulator Temperature	125 °C max				118 °C	120 °C	125 °C
VCCT_GXB Regulator Current	20 A max				20 A	22 A	23 A
VCCT_GXB Regulator Voltage	1.12 V +/-2%	1 V	1.05 V	1.08 V	1.15 V	1.2 V	1.35 V
VCCT_GXB Regulator Temperature	125 °C max				118 °C	120 C	125 C
FPGA Core Regulator Voltage	0.80 V–0.94 V +/-30 mV				0.99 V	1.05 V	1.15 V
FPGA Core Regulator Current	150 A max				150 A	160 A	170 A
FPGA Core Regulator Temperature	-40 °C to 125 °C				115 °C	120 °C	125 °C

continued...

Name	Specification Values	Lower Non-Recoverable (LNR)	Lower Critical (LC)	Lower Non-Critical (LNC)	Upper Non-Critical (UNC)	Upper Critical (UC)	Upper Non-Recoverable (UNR)
Board Power Rail							
FPGA Core Die Temperature	0 °C to 100 °C				90 °C	95 °C	100 °C
FPGA Transceiver Die Temperature	0 °C to 100 °C				90 °C	95 °C	100 °C
QSFP Port 0 Temperature	0 °C to 70 °C max				70 °C	80 °C	90 °C
QSFP Port 1 Temperature	0 °C to 70 °C max				70 °C	80 °C	90 °C
DDR4 Module 0 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 1 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 2 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C
DDR4 Module 3 Temperature	0 °C to 95 °C				85 °C	90 °C	95 °C

3.2. Supported PLDM/MCTP Commands

Refer to the Intel FPGA PAC D5005 Board Management Controller User Guide for more information.

Related Information

Intel FPGA PAC D5005 Board Management Controller User Guide

4. FPGA Interface Manager

The FPGA Interface Manager (FIM) contains the FPGA logic to support the accelerators, including the PCIe IP core, the Core Cache Interface protocol (CCI-P) fabric, the on-board DDR memory interface and management engine. In addition, the FIM allows dynamic downloading of new accelerator functions and updates to the FIM. Specific features of the FIM are listed in the following documents:

- Intel Acceleration Stack Quick Start Guide for Intel FPGA Programmable Acceleration Card D5005
- OPAE Intel FPGA Linux Device Driver Architecture Guide

The 2 Gb flash memory stores the FPGA Interface Manager (FIM).

Related Information

- Intel Acceleration Stack Quick Start Guide: Intel FPGA Programmable Acceleration Card D5005
- OPAE Intel FPGA Linux Device Driver Architecture Guide

5. System Compatibility

This chapter describes the platforms and Linux distribution targeted for the Intel FPGA PAC validation.

Note: OEM partners validate server platforms.

Table 7. Operating System Compatibility

Operating System	Version
Red Hat Enterprise Linux (RHEL) 7.6	RHEL

Note: The above mentioned operating systems are Linux Kernel 3.10.

Table 8. Ordering Part Number (OPN) Table

OPN	Description
BD-ACD-1SX280H2DES	Engineering Sample
BD-ACD-D5005-1	Production Board

Note: Specific OEMs may have unique OPNs.

6. Power Requirements

The Intel FPGA PAC supports a total power of 215 W. Intel has conducted thermal validation up to 189 W. For any power levels above 189 W, you are responsible for conducting thermal validation at increased power levels.

For more information, refer to section Power on page 5.

7. Mechanical Information

Intel FPGA PAC D5005 Dimensions

- Dual-slot PCIe card
- PCIe x16 mechanical with hockey stick card retainer
- 3/4-length with optional full-length PCIe server extension mounting bracket (included)
- PCB thickness 0.062 inches
- Card Weight is 1 Kg.

Note: All dimensions in mm.

Figure 3. Intel FPGA PAC D5005 Dimensions

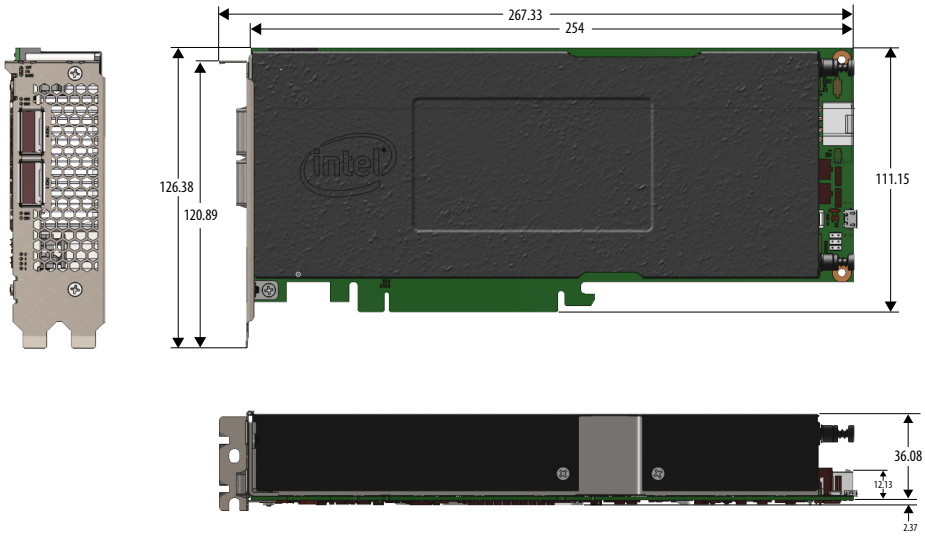
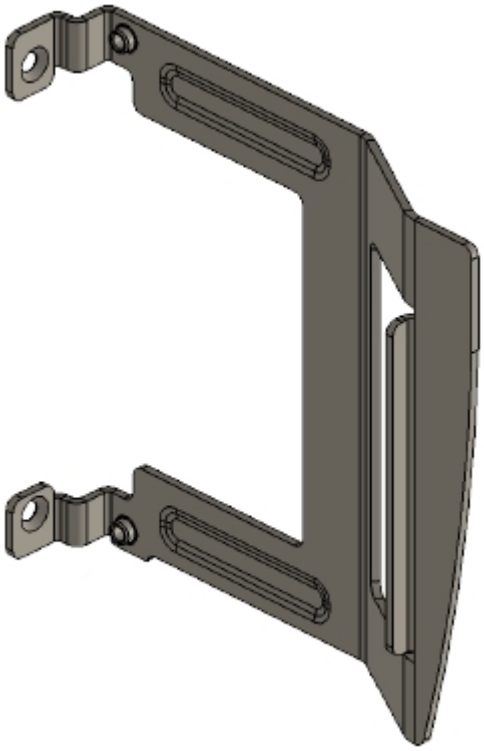


Figure 4. Extension Mounting Bracket

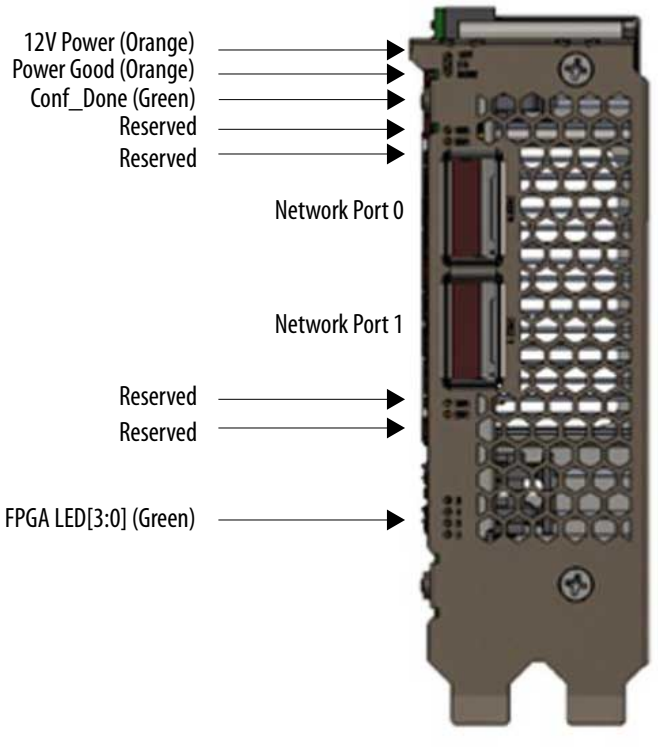
Figure 5. Non-coplanar Extension Bracket



7.1. Ports and LEDs

Various status LEDs are provided at the front panel to indicate the Intel FPGA PAC operating condition. The I/O panel status LED indicators are defined below.

Figure 6. Ports and LEDs



Port Description

- Network Port 0 – QSFP28 port capable of accepting 40 Gbps/100 Gbps SR optical module or 3 meter DAC cable
- Network Port 1 – QSFP28 port capable of accepting 40 Gbps/100 Gbps SR optical module or 3 meter DAC cable

Table 9. I/O Panel Definition

LED Name	Description
12V	Orange LED. On when 12 V power source is present. Off if 12V power source is not present.
PG	Orange LED. On when board power is present. Off if board power is not present.
DONE	Green LED. On indicates that the FPGA FIM is successfully loaded. This LED does not change states when AFUs are loaded.
FPGA LED 3	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.

continued...

LED Name	Description
FPGA LED 2	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.
FPGA LED 1	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.
FPGA LED 0	Green LED. Connected to FPGA for workload usage. State of LED is defined by the configured workload.

8. Thermal and Airflow Requirements

The Intel FPGA PAC D5005 has been thermally validated to 189 W for the entire card under provided flow characteristics. The FPGA junction temperature must not exceed 100 °C. The temperature of the QSFP28 modules must meet the module vendor's specification, typically 70 °C or 85 °C.

Table 10. Thermal Specifications

Parameter	Value
Operating Temperature	0 °C – 45 °C
Storage Temperature	-40 °C to 65 °C
Storage Humidity	5% to 85% RH with a 35 °C (95 °F) maximum dew point

Note: The BMC continuously monitors the FPGA junction temperature and will automatically shut down the Intel FPGA PAC D5005 when the FPGA junction temperature reaches 100 °C.

Note: AFU Developers should use the Intel Stratix 10 PowerPlay Early Power Estimator and the Quartus Prime Power Analyzer to estimate the FPGA power consumption.

Related Information

- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  The Intel Quartus Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition.
- Early Power Estimator for Intel Stratix 10 FPGAs User Guide
  This user guide describes the Early Power Estimator (EPE) for Intel Stratix 10 FPGA. This user guide provides guidelines for using the EPE, and details about thermal analysis and the factors contributing to FPGA power consumption.

8.1. Thermal Cooling Requirements

System airflow to the Intel FPGA PAC D5005 must be provided to keep the FPGA junction temperature below its 100 °C maximum specification. The temperature of the QSFP modules must also meet the module vendor's specification, typically 70 °C or 85 °C. The following table shows the airflow requirement for the Intel FPGA PAC D5005 during operation.

Table 11. Description of Terms

Term	Description
Linear Feet per Minute (LFM)	Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage.
T_{LA}	The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of the heatsink.

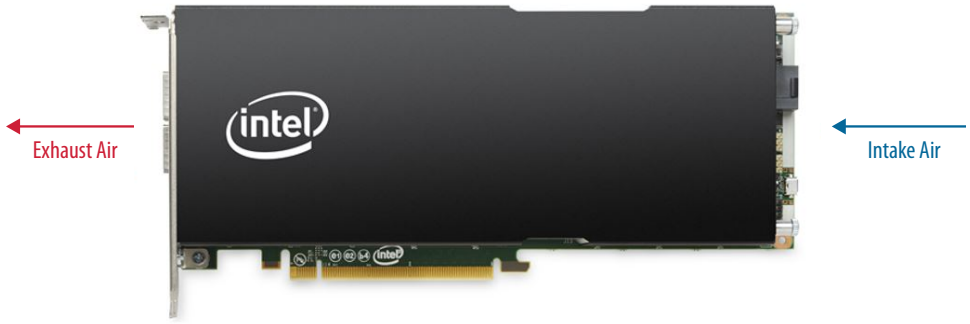
Table 12. Thermal Specifications

Local Air Inlet Temperature (°C)	Required Flow Rate (CFM)
30	14.2
35	16.7
40	20.0
45	25.0
50	33.3

8.2. Airflow Requirements

The recommended airflow direction is from the side of the 12 V auxiliary power connector (intake air side) to the I/O panel (exhaust air side).

Figure 7. Intel FPGA PAC D5005 Airflow Pattern



A. Safety and Regulatory Information

A.1. Regulatory Compliance

Regulatory Model Number: BD-ACD-D5005

United States Federal Communications Commission (FCC) Class A User Information

The Class A Product: Intel FPGA Programmable Acceleration Card D5005 complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept the interference received, including interference that may cause undesired operation.

Attention: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with other instrcutions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference is at his/her own expense.

Caution: If this device is changed or modified without permission from Intel, the user may void his or her authority to operate the equipment.

VCCI Class A Statement

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BSMI Class A Statement

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Canada EMC Compliance Statement

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

European Community Manufacturer Declaration

CE

Belgium (French)

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card D5005 est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante : https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Denmark

Intel Corporation erklærer hermed, at Intel FPGA Programmable Acceleration Card D5005 overholder direktiverne 2014/30/EU, 2014/35/EU og 2011/65/EU.

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Den fulde tekst for EUs overensstemmelseserklæring findes på engelsk på følgende adresse: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

The Netherlands

Intel Corporation verklaart hierbij dat Intel FPGA Programmable Acceleration Card D5005 in overeenstemming is met de richtlijnen 2014/30/EU, 2014/35/EU en 2011/65/EU.

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De volledige Engelse tekst van de EU-conformiteitsverklaring is hier beschikbaar: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Germany

Hiermit erklärt die Intel Corporation, dass die Intel FPGA Programmable Acceleration Card D5005 den Richtlinien 2014/30/EU, 2014/35/EU und 2011/65/EU entspricht.

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Die vollständige EU-Konformitätserklärung ist in englischer Sprache unter der folgenden URL einsehbar: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Sweden

Härmed intygar Intel Corporation att Intel FPGA Programmable Acceleration Card D5005 överensstämmer med direktiven 2014/30/EU, 2014/35/EU och 2011/65/EU.

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Den fullständiga engelska texten för EU-överensstämmelsen finns på följande internetadress: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Finland

Intel Corporation vakuuttaa täten, että Intel FPGA Programmable Acceleration Card D5005 on direktiivien 2014/30/EU, 2014/35/EU ja 2011/65/EU määräysten mukainen.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

EU-vaatimustenmukaisuusvakuutuksen koko englanninkielinen teksti on saatavilla osoitteessa: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Ireland

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card D5005 is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Portugal

A Intel Corporation declara, por este meio, que a Intel FPGA Programmable Acceleration Card D5005 cumpre as Diretivas 2014/30/UE, 2014/35/UE e 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Pode consultar o texto da declaração de conformidade da UE na íntegra, disponível em inglês através do seguinte URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Spain

Por la presente, Intel Corporation declara que Intel FPGA Programmable Acceleration Card D5005 cumple las directivas 2014/30/UE, 2014/35/UE y 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

El texto completo (en inglés) de la declaración de conformidad de la UE está disponible en la siguiente URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

France

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card D5005 est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante : https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Italy

Con il presente documento, Intel Corporation dichiara che la scheda di accelerazione programmabile Intel FPGA Programmable Acceleration Card D5005 è conforme alle direttive 2014/30/EU, 2014/35/EU e 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Il testo completo della dichiarazione di conformità UE in lingua inglese è disponibile al seguente indirizzo: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

United Kingdom

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card D5005 is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

Poland

Firma Intel Corporation niniejszym oświadcza, że karta Intel FPGA Programmable Acceleration Card D5005 jest zgodna z dyrektywami 2014/30/UE, 2014/35/UE i 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Pełny tekst deklaracji zgodności z wymogami UE w języku angielskim jest dostępny na stronie: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

End-of-Life/ Product Recycling

Product recycling and end-of-life take-back systems and requirements vary by country.

Contact the retailer or distributor of this product for information about product recycling and/or take-back.

Regulatory Markings

D33025
RoHS

R-R-CPU-BD-ACD-D5005

CAN ICES-3 (A)/NMB-3(A)

B. Revision History

Table 13. Revision History of the Intel FPGA Programmable Acceleration Card D5005 Data Sheet

Document Version	Changes
2019.11.04	Updated: • Intel Stratix® 10 FPGA on page 5 • Power on page 5 • Flash Memory on page 8 • Board Management Controller on page 9 • Mechanical Information on page 16 • Thermal Cooling Requirements on page 21
2019.09.12	Updated: • Power on page 5 • Power Requirements on page 15 • Mechanical Information on page 16
2019.05.13	Initial Release

Mouser Electronics

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Altera:

BD-ACD-1SX280H2DES BD-ACD-D5005-1