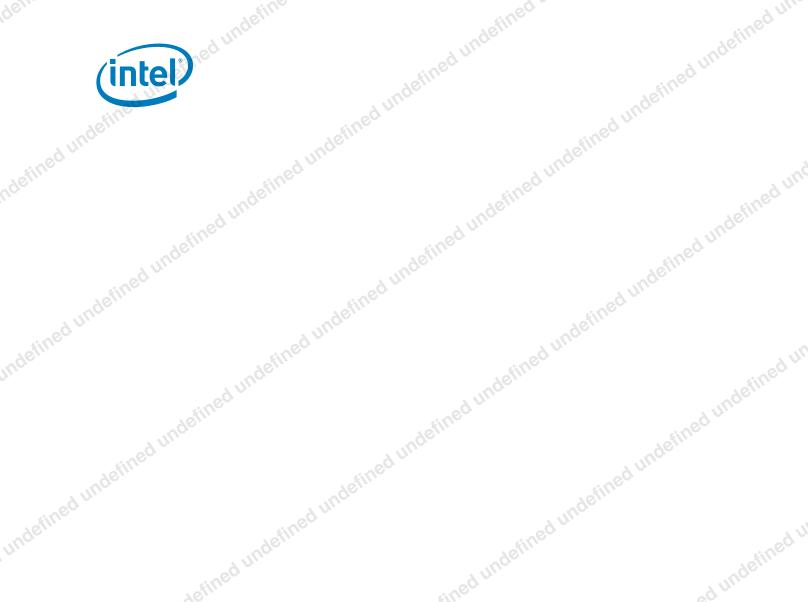


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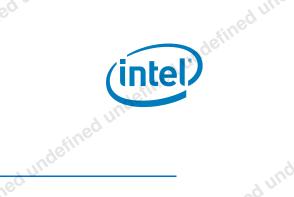
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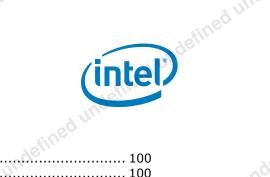
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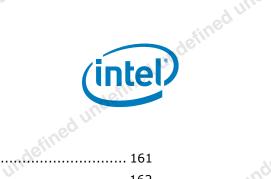
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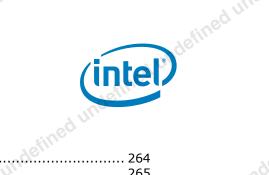
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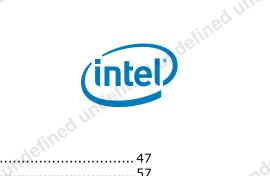
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Revision History

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	Document Number	Revision Number	Description	Revision Date
	332065	001	Initial release Added	March 2015
ined unde	332065	002	 Added Type3 SoC features and specifications included Updated Section 2.24, "Hardware Straps" strap pins updated. Max. Imaging video resolution updated for T4 to 1080p30. Table 124 VID values for all SKU's to match PRQ values. Section 12.1, "SoC Storage Overview" 	June 2015
		003	 Added Intel[®] Atom[™] processor X5-Z8350, Z8550, and Z8750. Updated Table 3, updated Table 124 	March 2016
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Introduction

The Intel[®] Atom™ Z8000 Processor Series Datasheet is the Intel Architecture (IA)
SoC that integrates the next generation Intel[®] processor core, Graphics, Memory
Controller, and I/O interfaces into a single system—on all.

The figures below shows the system level block diagram of the SoC. Refer the subsequent chapters for detailed information on the functionality of the different interface blocks.

Throughout this document Intel[®] Atom™ Z8000 Processor Series is referred as SoC. Note:

Section 1.3 lists the different features supported by the SoC packages.

References

Refer the following documents, which may be beneficial when reading this document or for additional information:

Document	Document Number
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/ products/processor/ manuals/index.htm
Intel [®] Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2)	332066
Intel [®] Atom™ Z8000 Processor Series Specification Update	332067

Terminology

90.	Term	Description
	ACPI	Advanced Configuration and Power Interface
dur	Cold Reset	Full reset is when PWROK is de-asserted and all system rails except VCCRTC are powered down
fines	DP	Display Port
inde	DTS	Digital Thermal Sensor
undefined undefined u	EMI	Electro Magnetic Interference
ie fine	eDP	embedded Display Port
ed und	adefined u	inder.
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hed unde	under	define
(intel)	Introduction	
	inder. define	
Sine	aed U.	
inge,	defilie	
Term	Description	
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-	20
defined und	definition video, plus multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available at http://www.hdmi.org/).	Indefined
Intel [®] TXE	Intel® Trusted Execution Engine	
LPDDR	Low Power Dual Data Rate memory technology.	
LPE	Low Power Engine	
MIPI CSI	MIPI Camera Interface Specification	
MIPI DSI	MIPI Display Interface Specification	
MP	Mega Pixel	60
MPEG	Moving Picture Experts Group	iefine
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.	unae
sined undefined U. MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64 bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR.	
PWM	Pulse Width Modulation	
POSM	Power on state machine	istine
SCI SDRAM SERR SMC	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading.	Inde
SCI	System Control Interrupt. SCI is used in the ACPI protocol.	
SDRAM	Synchronous Dynamic Random Access Memory	
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.	
SMC	System Management Controller or External Controller refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.	indefine
SMI	System Management Interrupt is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).	du
SIO	Serial I/O	
SIO TMDS Warm Reset	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in DVI and HDMI to send visual data to a display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing.	
Warm Reset	Warm reset is when both PMC_PLTRST# and PMC_CORE_PWROK are asserted.	
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Table 1.

	fined undefine		Lefined	
Introducti	on fined un	indefined undefil	led mod	(intel)
indefined		defined une		rined under
1.3	SoC Packages	ages	ndefined unde	
ed undefined un		Category	√60 T4	T3 A U
777	/ge	No. of Cores	4	4
	CPU	Burst Speed	2.4 GHz	1.84 GHz ^[4]
1.	GPU	Speed	Gen8-LP 12/16EU up to 600 MHz	Gen8-LP 12EU up to 500 MHz
		Туре	17x17mm Type 4	17x17mm Type 3
	Dark 18fil	IO count	628	378
	Package Mechanical	Ball count	1380	592
	~(O)	ball pitch	0.4mm	0.65mm
	delin	Z-height	0.937mm	1.002mm
ed u	Memory PCIe	Interface, Max transfer data rate	Dual Channel 2x64 bit, LPDDR3 - 1600MT/S	Single Channel 1x32/64 DDR3L-RS - 1600MT/s
<i>y</i>	Memory	Туре	BGA	BGA
		Capacity	2 - 8GB	1 - 2GB
	DCI o	Number of ports	2	1
	PCIe	Port Configuration	1x2, 2x1	x1
		Number of lanes	6	6
	Imaging	Lane configuration	4+2, 3+2, 2+2+2	4+2, 3+2, 2+2
	ind	Speed	1.5 GHz	1.5 GHz
6, 105		Still & Video	13MP ZSL, 1080p30	8MP, 1080p30
	Imaging Media Audio	Media decode rate	H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG	H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG
		Media encode rate	H.264, H.263, VP8, MVC, JPEG	H.264, H.263, VP8, MVC, JPEG
	Audio	LPE (Low Power Engine)	3 I2S ports	3 I2S ports
	and a	USB 3.0	3	Not Supported
	Achin.	USB 3.0 OTG	eines 1	1 6
_	USB devices	USB 2.0	<u> </u>	3
		USB SSIC	2	Not Supported
		USB HSIC	2	2
fined		USB 3.0 OTG USB 2.0 USB SSIC	1 - 2	1 3 Not Supported
Datasheet	d undefine	a undefined un	a defined undefined i	undefined undefine
		sine	60	~

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Jefined undefined undefined SoC Packages (Sheet 2 of 2) Table 1.

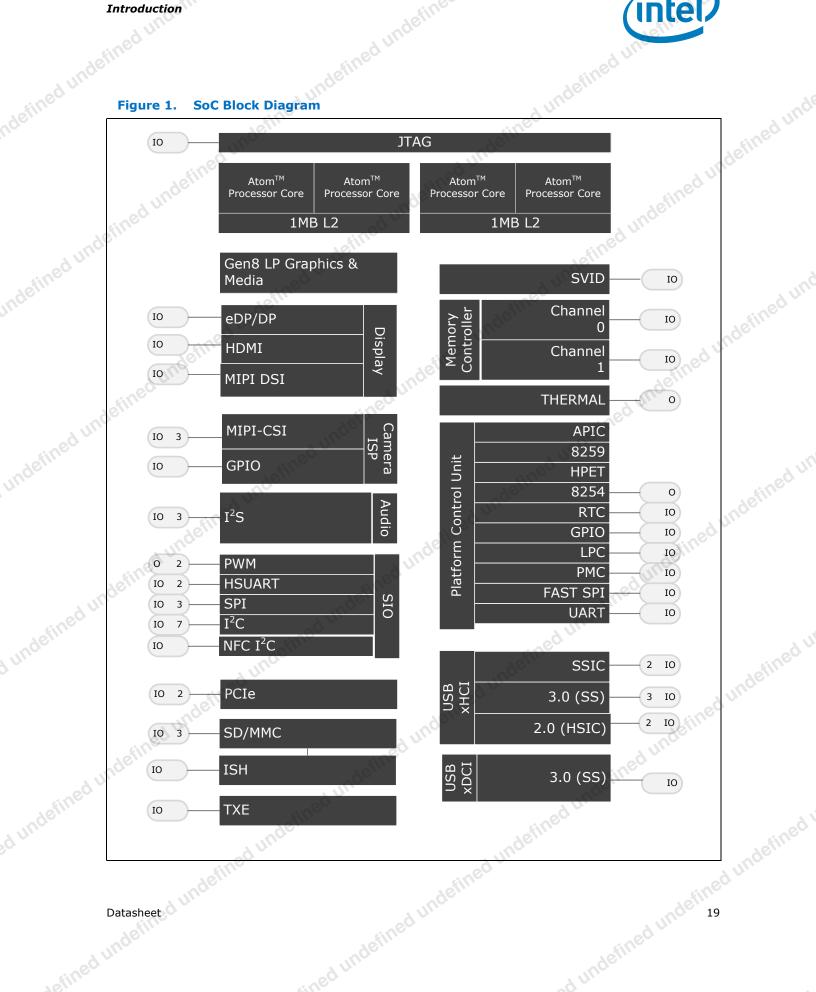
	Interface	Category	T4	Т3
	"luge"	LPC	YES	Not supported
	red o	I2C	7	6
A	efill	I2C Max Speed	1.7 MHz	1.7 MHz
4 line		I2C NFC	1	1
	SIO	I2C ISH	1	un'
nder.		SPI	3	Not supported ^[1]
Jefined undefined und		SPI Speed	Master Only up to 25 MHz	Master Only up to 25 MHz
	186	Fast SPI	Quad mode	Dual mode
	unde	SD Card	x1 SDR104	x1 SDR104 ^[2]
ndefined undefined uni	Storage	SDIO	x1 SDR104	x1 SDR104
	Seill.	eMMC	4.51	4.51
		DDI ports	x3	x2
adefinee		Max MIPI DSI Resolution	2560x1600 @60fps	1900x1200 @60fps
od uli.		MIPI-DSI ports	2x 4 Lanes @ 1Gbps	1x 4 Lanes @ 1Gbps
defines	Display	Max eDP Resolution	2560x1600 @ 24bbp	1920x1080 @60fps
Y	Display Unio	eDP ports	2 (2x4 @2.7Gbps)	2 (2x4 @2.7Gbps)
	defined un	Max DP 1.1a Resolution	2560x1600 @60fps	2560x1600 @60fps
isfined L		Max HDMI 1.4b Resolution	3840x2160 @30fps	1920x1080 @60fps
Indefined.	NOTES: 1. One SPI port is be dependent of 2. Is limited to DE 3. MPO available of 4. The Burst Spee	on the GPIO configurations DR50 due to PMIC power do on Display Pipe B only.		314
	· ven		4 UI	-

NOTES:

- 1. One SPI port is multiplexed with reference clock signal which is GPIO signal, and the usage will be dependent on the GPIO configurations on the platform.
- 2. Is limited to DDR50 due to PMIC power delivery limitation.
- 3. MPO available on Display Pipe B only.
- 4. The Burst Speed mentioned is for 2 Cores. This is PRE-SMT package height.



idefined undefined undefined SoC Block Diagram Figure 1.



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1.4 Feature Overview

1.4.1 Processor Core

- Up to four IA-compatible low power Intel[®] processor cores
 - One thread per core
- Two-wide instruction decode, out of order execution.
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core.
- On-die, 1 MB, 16-way L2 cache, shared per two cores.
- 36-bit physical address, 48-bit linear address size support.
- Supported C-states: C0, C1, C6C, C6, C7.
- Supports Intel[®] Virtualization Technology (Intel[®] VT-x2).

1.4.2 System Memory Controller

- Memory Controller supports dual-channel DDR3L-RS/LPDDR3.
- Up to two ranks per channel (4 ranks in total).
- 32 Bit or 64 Bit data bus.
- Supports DDR3L-RS/LPDDR3 with 1600 MT/s data rate.
- Supports x32 LPDDR3 DRAM device data widths.
- Supports x16 DDR3L-RS DRAM device data widths.
- Total memory bandwidth supported is 12.8GB/s (for 1600 MT/s single-channel) to 25.6GB/s (for 1600 MT/s dual-channel).
- Supports different physical mappings of bank addresses to optimize performance.
- Supports Dynamic Voltage and Frequency Scaling.
- Out-of-order request processing to increase performance.
- Aggressive power management to reduce power consumption.
- Proactive page closing policies to close unused pages.

1.4.3 Display Controller

- Supports up to 3 Display pipes.
- Supports 2 MIPI DSI ports.
- Supports 3 DDI ports to configure eDP 1.3/DP 1.1a/DVI/HDMI 1.4b.
- Supports 2 panel power sequence for 2 eDP ports.
- Supports Audio on DP/HDMI.
- Supports Intel[®] Display Power Saving Technology (DPST) 6.0, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS).

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1.4.4 Graphics and Media Engine

- Intel's 8th generation (Gen 8) LP graphics and media encode/decode engine.
- Supports 3D rendering, media compositing and video encoding.
- Graphics Burst enabled through energy counters.
- Supports DX*11.1, OpenGL 4.3, OGL ES 3.0, OpenCL 1.2.
- 4x anti-aliasing.
- Full HW acceleration for decode of H.263, MPEG4, H.264, H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG.
- Full HW acceleration for encode of H.264, H.263, VP8, MVC, JPEG.
- Supports Content protection using PAVP2.0, HDCP 1.4 (wired)/2.2 (wireless) and Media Vault DRM.

1.4.5 Image Signal Processor

- · Supports up to three MIPI CSI ports.
- Supports up to 13MP sensors.

1.4.6 Power Management

- Supports ACPI 5.0.
- Processor Core states: C0, C1, C1E, C6C, C6 and C7.
- Display and Graphics device states: D0, D3.
- System sleep states: S0, S0ix, S4, S5.
- Support CPU and GFx Burst for selected SKUs.
- Dynamic I/O power reductions (disabling sense amps on input buffers, tristating output buffers).
- Dynamic memory self-refresh.

1.4.7 PCI Express*

- Supports x2 PCIe 2.0 compliant controller.
- Supports both Gen1 and Gen2 data rates.
- The controller provides a max data payload of 128B with the capability of splitting the request at 64B granularity.
- Supports autonomous up-configuration and autonomous down-configuration as target.

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1.4.8 USB Controller

1.4.8.1 USB xHCI Controller

USB Host Controller supports:

- Two (2) Super Speed Inter-Chip (SSIC) port.
- Three (3) Super Speed (SS) ports [Backward Compatible of USB 2.0 HS/FS/LS].
- Two (2) High Speed Inter-Chip (HSIC) ports.

Note: SoC can support the 4th SS port when OTG port is in Host mode.

1.4.8.2 USB xDCI Controller

The SoC implements OTG block for device-mode functionality:

- Supports one USB 3.0 Super Speed port with backward compatibility of USB 2.0 High Speed and Low/Full Speed.
- Supports SuperSpeed OTG v3.0 device.
- Supports USB3 Debug Device Class Specification [USB3-debug].

1.4.9 Low Power Engine (LPE) Audio Controller

- Support 3 I2S ports.
- I2S and DDI with dedicated DMA.
- Supports MP3, AAC, AC3/DD+, WMA9, PCM (WAV).
- Provides HW acceleration for common audio and voice functions such as codecs, acoustic echo cancellation, noise cancellation.

1.4.10 Storage

1.4.10.1 Storage Control Cluster (eMMC, SDIO, SD)

- Supports one eMMC 4.51 controller
 - 200 MB/s Data rate
- Supports one SDIO 3.0 interface
 - 800 Mb/s Data rate
- Supports one SDXC controller
 - 800 Mb/s Data rate

1.4.11 Intel[®] Trusted Execution Engine (Intel[®] TXE)

Intel TXE is responsible for supporting and handling security related features.

- Supports MediaVault with OMA-DRM and One Time Password.
- Isolated execution environment for crypto operations.
- Supports secure boot with customer programmable keys to secure code.



Serial I/O (SIO) 1.4.12

- Controller for external devices via SPI, UART, I²C or PWM.
- Each port is multiplexed with general purpose I/O for configurations flexibility.
- Supports up to 7 I²C, NFC I²C, ISH I²C, 2 HSUART, 2 PWM, 3 SPI interface.

Platform Control Unit (PCU)

Platform controller unit is a collection of HW blocks, including UART, debug/boot SPI and Intel legacy block (iLB), that are critical to implement a Windows* compatible platform. Some of its key features are:

- Universal Asynchronous Receiver/Transmitter (UART) with COM1 interface.
- A Fast Serial Peripheral Interface (SPI) for Flash only stores boot FW and system configuration data.
- Intel Legacy Block (iLB) supports legacy PC platform features
 - RTC, Interrupts, Timers and Peripheral interface (LPC for TPM) blocks.

Intel®Sensor Hub

Intel® Sensor Hub Supports:

- Acquisition / sampling of sensor data.
- The ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS.
- Low power operation through clock gating and power gating of parts of the ISH together with the ability to turn sensors off.
- The ability to operate independently when the host platform is in low power state.

Package

Table 2. **Package Attributes**

ackage A		ico the package attrib	outes for different SoC	SkUs.
	Category	T4 [©]	Т3	definee
_	Туре	17x17mm Type 4	17x17mm Type 3	unde
Package _	IO count	628	378	So
Tuckage _	Ball count	1380	592	
	ball pitch	0.4mm	0.65mm	
	Z-height	0.937mm	1.002mm	-09
efined v		efined undefined	una	ned undefined undefine

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1.4.16

Table 3.

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defined un	1.4.16 Table 3		List KU List	ined un	deli				ned uni	gefined '		
	Processor Number	Stepping	Package Type	SDP(W)	Core LFM (MHz)/ HFM (GHz)	Core max Burst (GHz)	Tjmax (°C)	TDP/ SDP Tj(°C)	GFx Normal /Burst (MHz)	No. of Graphics EU	Memory Channel	Memory Speed (MT/s)
	Z8750	D-1	T4	2.0	480/1.6	2.56	90	70	400/600	16	2x64	LPDDR3- 1600
ed u	Z8550	D-1	T4	2.0	480/1.44	2.4	90	70	400/600	12	2x64	LPDDR3- 1600
Jefined u	Z8350	D-1	ТЗ	2.0	480/1.44	1.92	90	70	400/500	12	1x64	DDR3L/ LPDDR3 1600
	Z8700	C-0	T4	2.0	480/1.6	2.4	90	70	400/600	16	2x64	LPDDR3 1600
	Z8500	C-0	T4	2.0	480/1.44	2.24	90	70	400/600	12	2x64	LPDDR3 1600
	Z8300	C-0	Т3	2.0	480/1.44	1.84	90	70	400/500	12	1x32/64	DDR3L- 1600
	inge,		•		defin	0	1		•	Sine	0.	
		Issue		-9,	nue	XHCI	controll	er stuck	in reset du	uring warm	reboot cy	cles
idefined i		Step	oing	efines		BXT	Ax/Bx, A	PL Ax	eined t			
		Work	around	•						Controller g and clea		

Issue	XHCI controller stuck in reset during warm reboot cycles	
Stepping	BXT Ax/Bx, APL Ax	ed ni
Workaround	BIOS should program USB Host Controller Misc Reg 2 bit2 =1, set Bit5 for A0 stepping and clear for all other steppings	undefine
Impact of Workaround	define	D
Notes	USB	

	tine		steppir	ngs	unc
nu .	Impact of Workaround		96	Stil.	3
d undefined undefined un	Notes	e!	USB	, unde	
"ugei,		Tacilno		angeo.	_
red m.	Pad Name	GPI	0#	Net Name	
defill	GP187_DDI0_DDC_SDA	GPIO_18	7	HDMI_DDC_SDA	ال م
Uno	GP188_DDI0_DDC_SCL	GPIO_18	3	HDMI_DDC_SCL	- ineo
UP .	GP193_PNL0_VDDEN	GPIO_19	3	DISP0_VDDEN	J dell.
ed undefined undefined w	i efined		d uni	ined undefined undefil	
d undefined undefined was a serined was a serined undefined was a serined undefined was a serined was a serine a way a way a serine a way a serine a way a serine a way a way a serine a way a serine a way	undefined unde	undefin	ed ur	Net Name HDMI_DDC_SDA HDMI_DDC_SCL DISP0_VDDEN § Datashee	med undefineed



2 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, Some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

2.1 Pin States

This section describes the states of each signal before, during and directly after reset. Additionally, Some signals have internal pull-up/pull-down termination resistors, and their values are also provided. All signals with the "" symbol are muxed and may not be available without configuration.

Table 4. Platform Power Well Definitions

indefined undefines	Power Type	Voltage Range (V)	Power Well Description
ed u.	VCC0/1	Refer Table 118	Variable voltage rail for core
iefine	VGG	Refer Table 118	Variable voltage rail for Graphics Core
	VNN	Refer Table 118	Variable voltage rail for SoC.
	V1P15	1.15	Fixed voltage rail for SoC, Graphics, camera
	V1P05A	1.05	Fixed voltage rail for P-unit, LPE, TXE,I/O's, PLL's and ISH
ind	V1P2A	1.24	Fixed voltage rail for I/O's and PLL's.
ined uli	VDDQ	1.24/1.35	Fixed voltage rail for DDR PHY
4efill	VDDQG	1.24/1.35	Fixed voltage rail for DDR PHY
unde	V1P8A	1.8	Fixed voltage rail for I/O's.
ined	V3P3A	3.3	Fixed voltage rail for I/O's.
indefined undefined	V3P3A_V1P8A	1.8/3.3	Fixed voltage rail for SDIO.
Ulu	V3P3RTC	3.3	Voltage rai For RTC clock.
	-70,	1	100

Table 5. Buffer Type Definitions (Sheet 1 of 2)

Buffer Type	Buffer Description
MIPI-DPHY	1.24 V tolerant MIPI DPHY buffer type
USB3 PHY	1.0 V tolerant USB3 PHY buffer type
USB2 PHY	1.8 V tolerant USB3 PHY buffer type
SSIC PHY	1.2 V tolerant SSIC PHY buffer type
HSIC PHY	1.2 V tolerant HSIC PHY buffer type
GPIO	GPIO buffer type. This can be of the following types: 1.8/3.3 V.

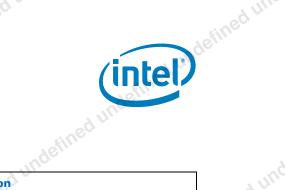


defined undefined undefined **Buffer Type Definitions (Sheet 2 of 2)** Table 5.

defill	Buffer Type	Buffer Description
	MODPHY	1.0 V tolerant MODPHY buffer type
	DDR3	1.5 V tolerant DDR3 buffer type
bni	Analog	Analog pins that do not have specific digital requirements. Often used for circuit calibration or monitoring.
	GPIOMV, HS	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz)
defille	GPIOMV, MS	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz)
ndefined undefined und	GPIOMV, MS, CLK	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz), Clock
ndefill	GPIOMV, HS, CLK	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz), Clock
	GPIOMV, HS, RCOMP	GPIO Buffer type, Medium Voltage(1.8V), High Speed (FMAX~208Mhz), RCOMP
m.	GPIOMV, MS, I2C	GPIO Buffer type, Medium Voltage(1.8V), Medium Speed (FMAX~60Mhz), I2C
	GPIOHV, HS	GPIO Buffer type, High Voltage(1.8V/3.3V), High Speed (FMAX~208Mhz)
indefine	GPIOHV, HS, RCOMP	GPIO Buffer type, High Voltage(1.8V/3.3V), High Speed (FMAX~208Mhz), RCOMP
undefined undefined un	NOTE: GPIO mode, wh functionally use	ere register controlled will not hit FMAX speeds. It only matters when d.
	Junden	indefine

Default Buffer State Definitions (Sheet 1 of 2) Table 6.

	Buffer State	Description
undefined undefined un	Z	The SoC places this output in a high-impedance state. For inputs, external drivers are not expected.
ad under	Do Not Care	The state of the input (driven or tristated) does not affect the processor. For outputs, it is assumed that the output buffer is in a high-impedance state.
fine	V _{OH}	The SoC drives this signal high with a termination of 50 Ω .
inde	V _{OL}	The SoC drives this signal low with a termination of 50 Ω .
900	Unknown	The processor drives or expects an indeterminate value.
	V _{IH}	The SoC expects/requires the signal to be driven high.
	VIL	The SoC expects/requires the signal to be driven low.
20	"P" 1.1V	USB low speed Single ended 1.
adefinee	Pull-up	This signal is pulled high by a pull-up resistor (internal or external — internal value specified in "Term" column).
d undefined undefine	Pull-down	This signal is pulled low by a pull-down resistor (internal or external — internal value specified in "Term" column).
deill	Running	The clock is toggling, or the signal is transitioning.
ed une	Off	The power plane for this signal is powered down. The processor does not drive outputs, and inputs should not be driven to the processor. (VSS on output)
26 undefined	undefine	Datasheet and undefined
76illi		ine and a



Default Buffer State Definitions (Sheet 2 of 2) Table 6.

Buffer State	Description
1 , ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Buffer drives V _{OH}
000	Buffer drives V _{OL}
Н	Buffer Hi Z, weak PU, default to 20K, unless explicitly specified otherwise
L	Buffer Hi Z, weak PD, default to 20K, unless explicitly specified otherwise
Input H	Input enable, weak PU
Output L	Output enable, weak PU
Pgm	Programmable
Retain	retain configuration/data prior to standby

System Memory Controller Interface Signals 2.2

DDR3L-RS

Table 7. DDR3L-RS System Memory Signals (Sheet 1 of 2)

ie fine			Default Buffer State					
undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	undefined un
	DDR3_M0_MA[15:0]	0	V1P35	DDR	Z	Z	Z	UM
	DDR3_M0_CK[1,0]_P	0	V1P35	DDR	Z	Z	Z	
ned i	DDR3_M0_CK[1,0]_N	0	V1P35	DDR	Z	Z	Z	
defill	DDR3_M0_CKE[3:0]	0	V1P35	DDR	Weak 0	0 0	0	
und	DDR3_M0_CS[1,0]_N	0	V1P35	DDR	Z	Z	Z	
eineo.	DDR3_M0_CAS_N	0	V1P35	DDR	Z	Z	Z	
d undefined undefined	DDR3_M0_RAS_N	0	V1P35	DDR	Z	Z	Z	undefined u
J Ulli	DDR3_M0_WE_N	0	V1P35	DDR	Z	Z	Z	sinec.
<i></i>	DDR3_M0_BS[2:0]	0	V1P35	DDR	Ull Z	Z	Z	inde"
	DDR3_M0_DRAMRST_N	0	V1P35	DDR	Weak 0	0	1 6	011
3	DDR3_M0_ODT[1,0]	0	V1P35	DDR	Z	Z	Z	
inec	DDR3_M0_DQ[63:0]	I/O	V1P35	DDR	Z	Z	Z	
deill	DDR3_M0_DM[7:0]	0	V1P35	DDR	Z	Z	Z	
dulle	DDR3_M0_DQSP[7:0]	I/O	V1P35	DDR	Z	Z	Z	
sine c	DDR3_M0_DQSN[7:0]	I/O	V1P35	DDR	Z	JI Z	Z	
"uge,	DDR3_M0_OCAVREF	0	V1P35	DDR	Z cine	Z	Z	9/1
ed undefined undefined	DDR3_M0_ODQVREF	0	V1P35	DDR	Z	Z	Z	iefine
	d undefined			4efine	d ui		eine	d unae
Datasheet	g or		4	ILO			27	,
Datasheet	ne ^d	und	efinec	DDR		d undefine	ed u.	d undefined i



DDR3L-RS System Memory Signals (Sheet 2 of 2) Table 7.

defills	sine c		Default Buffer State				
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
	DDR3_M0_RCOMPPD	I	V1P35	DDR	Z	Z	Z
defined undefined	DDR3_M1_MA[15:0]	0	V1P35	DDR	Z	Z	Z
rines	DDR3_M1_CK[1,0]_P	0	V1P35	DDR	Z	Z	Z
inde	DDR3_M1_CK[1,0]_N	0	V1P35	DDR	Z	Z	Z
ed a	DDR3_M1_CKE[3:0]	0	V1P35	DDR	Weak 0	0	0
16ting	DDR3_M1_CS[1,0]_N	0	V1P35	DDR	z	Z	Z
	DDR3_M1_CAS_N	0	V1P35	DDR	Z	Z	Z
	DDR3_M1_RAS_N	0	V1P35	DDR	Z	Z	Z
	DDR3_M1_WE_N	0	V1P35	DDR	Z	Z	Z
	DDR3_M1_BS[2:0]	0	V1P35	DDR	Z	Z	Z
defined undefined	DDR3_M1_DRAMRST_N	0	V1P35	DDR	Weak 0	0	OI
4efine	DDR3_M1_ODT[1,0]	0	V1P35	DDR	Z	Z	Z
unos	DDR3_M1_DQ[63:0]	I/O	V1P35	DDR	Z	Z	Z
	DDR3_M1_DM[7:0]	0	V1P35	DDR	Z	Z	Z
Heim	DDR3_M1_DQS[7:0]_P	I/O	V1P35	DDR	Z	Z	Z
	DDR3_M1_DQS[7:0]_N	I/O	V1P35	DDR	Z	Z	Z
	DDR3_M1_OCAVREF	0	V1P35	DDR	Z	Z	Z
	DDR3_M1_ODQVREF	0	V1P35	DDR	Z	Z	Z
	DDR3_M1_RCOMPPD	I	V1P35	DDR	Z	Z	Z
ine	DDR3_DRAM_PWROK	I	V1P35	DDR	Input	Input	Input
indefill	DDR3_CORE_PWROK	I	V1P35	DDR	Input	Input	Input
indefined undefine	LPDDR3				dundefine	d under.	

d undefined undefine

LPDDR3 System Memory Signals (Sheet 1 of 2) Table 8.

	duli		, UNO		Defa	ult Buffer 9	State	
defined undefine	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
fine	LPDDR3_M0_CA[9:0]	0	V1P24	DDR	Z	Z	Z	
nde	LPDDR3_M0_CK_P_A/B	0	V1P24	DDR	Z	Z	Z	ed '
	LPDDR3_M0_CK_N_A/B	0	V1P24	DDR	og z	Z	Z	4efine
28 undefin	ed undefinee	Jefin	ed unds	ifined L		undefin	Datasheet	led une



defined undefined undefined ndefined undefined Table 8. LPDDR3 System Memory Signals (Sheet 2 of 2)

Pnysicai 11	nterfaces		refile		(Intel)				
Table 8		$U_{U_{i}}$	define				611.		
define						eg ni.			
unde						ine			
Table 8	. LPDDR3 System Memory S	ignal	s (Sheet	2 of 2)	inge				
	Stine			45.5	Defa	ault Buffer S	State	d un	
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	ndefined un	
	LPDDR3_M0_CKE[1:0]_A/B	0	V1P24	DDR	Weak 0	0	0		
idefined undefined ut	LPDDR3_M0_CS[1:0]_N	0	V1P24	DDR	Z	Z	Z		
efine	LPDDR3_M0_ODT_A/B	0	V1P24	DDR	Z	Z	Z		
inoc	LPDDR3_M0_DQ[31:0]_A/B	I/O	V1P24	DDR	Z	Z	Z		
inced .	LPDDR3_M0_DM[3:0]_A/B	0	V1P24	DDR	Z	Z	Z		
defill	LPDDR3_M0_DQS[3:0]_P_A/B	I/O	V1P24	DDR	Z	Z	Z	, 0	
	LPDDR3_M0_DQS[3:0]_N_A/B	I/O	V1P24	DDR	Z	Z	Z	"ineo	
	LPDDR3_M0_OCAVREF	0	V1P24	DDR	Z	Z	Z	ndefined u	
	LPDDR3_M0_ODQVREF	0	V1P24	DDR	Z	Z	Z	7/1/2	
_ 1	LPDDR3_M0_RCOMPPD	I	V1P24	DDR	Z	Z	Z	1	
ed	LPDDR3_M1_CA[9:0]	0	V1P24	DDR	Z	Z	Z		
defille	LPDDR3_M1_CK_P_A/B	0	V1P24	DDR	Z	Z	Z		
ndefined undefined v	LPDDR3_M1_CK_N_A/B	0	V1P24	DDR	Z	Z	Z		
aneo.	LPDDR3_M1_CKE[1:0]_A/B	0	V1P24	DDR	Weak 0	0	0		
deill	LPDDR3_M0_CS[1:0]_N	0	V1P24	DDR	Z	Z	Z	A.	
	LPDDR3_M0_ODT_A/B	0	V1P24	DDR	Z	Z	Z	*inec.	
	LPDDR3_M1_DQ[31:0]_A/B	I/O	V1P24	DDR	Z	Z	Z	- uger	
	LPDDR3_M1_DM[3:0]_A/B	0	V1121	DDR	Z	Z	Z		
	LPDDR3_M1_DQS[3:0]_P_A/B	I/O	V1P24	DDR	Z	Z	Z		
ined	LPDDR3_M1_DQS[3:0]_N_A/B	I/O	V1P24	DDR	Z	Z	Z		
deill	LPDDR3 M1 OCAVREE	0	V/1P24	DDB	7	7	7		
dune	LPDDR3_M1_ODQVREF	0	V1P24	DDR	Z	Z	Z		
sinet.	LPDDR3_M1_RCOMPPD	ī	V11 24	DDD	7	7	7	_	
Indefined under	LPDDR3_DRAM_PWROK	т	V1F24	DDR	Input	Input	Input	6-	
31.	LPDDR3_DRAM_FWROK	T	V1P24	DDR	Input	Input	Input	- FINE	
	LPDDR3_CORE_PWROK	1	V1P24	DDR	Input	Input	Input	Tiuge,	
undefined undefined	LPDDR3_M1_ODQVREF LPDDR3_M1_RCOMPPD LPDDR3_DRAM_PWROK LPDDR3_CORE_PWROK		undefil			d	undefine		
defined una	sined under				edu	ndefine			
TIVE	fined under			ed un	define			undefine	
Datasheet	A under		d undef	luc			undefin	9	
Datasheet	dunde	fine				indefined			
16 [†] 11.	iner.				.60	O.			



2.3 USB Controller Interface Signals

2.3.1 USB2.0 Interface Signals

Table 9. USB2.0 Interface Signals

		, 0	UOL	Default Buffer State				
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix		
USB_DN[3:0]	I/O	V1P8	USB2 PHY	"P" 1.1V	"P" 1.1V	S0i3 ¹		
USB_DP[3:0]	I/O	V1P8	USB2 PHY	"P" 1.1V	"P" 1.1V	S0i3 ¹		
USB_OTG_ID	I/O	V1P8	USB2 PHY	Input, weak pull up	Input, weak pull up	Input		
USB_VBUSSNS	I/O	V1P8	USB2 PHY	Input	Input	Input		
USB_RCOMP	0	V1P8	USB2 PHY	Output	Output	Output		
USB_OC[1:0]_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)		

NOTES:

- 1. ¹Depends on USB2 Mode.
- 2. USB 2.0 Port 0 is the OTG port.

2.3.2 USB HSIC Interface Signals

Table 10. USB 2.0 HSIC Interface Signals

				Default Buffer State			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
USB_HSIC0_DATA	I/O	V1P2	HSIC Buffer	Weak 0	Weak 0	Weak 0	
USB_HSIC0_STROBE	I/O	V1P2	HSIC Buffer	Weak 1	Weak 1	Weak 1	
USB_HSIC1_DATA	I/O	V1P2	HSIC Buffer	Weak 0	Weak 0	Weak 0	
USB_HSIC1_STROBE	I/O	V1P2	HSIC Buffer	Weak 1	Weak 1	Weak 1	
USB_HSIC_RCOMP	J	V1P2	HSIC Buffer	Z	Zyen	Z	

NOTE: The HSIC should be reset after SoC.



USB3.0 Interface Signals 2.3.3

2.3.3.1 **USB 3.0 Interface Signals**

Table 11. USB 3.0 Interface Signals

lable	II. USB 3.0 Interrace Sign	gnais		" Jec			you.
, 0	nde	20	Gilli	Default Buffer State			
ndefined undefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
ined.	USB3_TXN[3:0]	0	V1P05A	USB3	Х	no z	Output
defill	USB3_TXP[3:0]	0	V1P05A	USB3	x	Z	Output
Tille	USB3_RXN[3:0]	I	V1P05A	USB3	X	Z	Input
	USB3_RXP[3:0]	I	V1P05A	USB3	X	Z	Input
	USB3_RCOMP_N	I	V1P05A	USB3	Х	Output	Off
2.1	USB3_RCOMP_P	I	V1P05A	USB3	Х	Output	Off

NOTE: USB3.0 Port 0 is the OTG port.

USB SSIC Interface Signals

Table 12. **USB SSIC Interface Signals**

	ed unoc			under Def	ate	undefinee		
2	Signal Name	Dir	Plat. Power	Type	Pwrgood Assert State	Resetout Deassert State	Soix	une
undefined.	USB_SSIC_RX_N[0,1]	I/O	V1P24	SSIC PHY	Input	Input	Input	
"uger.	USB_SSIC_RX_P[0,1]	I/O	V1P24	SSIC PHY	Input	Input	Input	
	USB_SSIC_TX_N[0,1]	I/O	V1P24	SSIC PHY	Z	Output	Output	
	USB_SSIC_TX_P[0,1]	I/O	V1P24	SSIC PHY	Z	Output	Output	
	USB_SSIC_RCOMP_N	0	V1P24	SSIC PHY	Output	Output	Output	ed o
	USB_SSIC_RCOMP_P	0	V1P24	SSIC PHY	Output	Output	Output	46111
undefii.	USB_SSIC_RCOMP_P	g un		define	d undefine	d undefine	ine.	Jundefined V
Datasheet				4 nue			31	-
Datasheet	2000	ed ur	ndefine			ad undefine	yd U	



Integrated Clock Interface Signals

Table 13. Integrated Clock Interface Signals

	fined			iuge,				
eined '	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
ige!!.	ICLK_OSCIN	I	V1P0	Crystal Oscillator	Input (Crystal)	Input (Crystal)	Input (Crystal)	
	ICLK_OSCOUT	0	V1P0	Crystal Oscillator	Output (Crystal)	Output (Crystal)	Output (Crystal)	, un
	ICLK_ICOMP	0	Analog	Analog	Input	Input	Input	ined
	ICLK_RCOMP	0	Analog	Analog	Input	Input	Input	deill
2.5	Display - Dig	gita	l Dis	olay In	terface (DDI) Si	ignals	
Table 1	4. Digital Display Inte	erfac	e Signal	s (Sheet 1		ult Buffer Stat		1
	ine.				Dela	art burier Stat	. c	, 11

		sq m.		Def	fault Buffer State	e
Signal Name	Power		Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
DDI0_TXP[3:0]	0	V1P24	DDI	ine z	Output	Output
DDI0_TXN[3:0]	0	V1P24	DDI	Z	Output	Output
DDI0_AUXP	I/O	V1P24	DDI	Z	Output	Output
DDI0_AUXN	I/O	V1P24	DDI	Z	Output	Output
DDI0_BKLTCTL	I/O	V1P8	GPIOMV, MS	0	0	0
DDI0_BKLTEN	I/O	V1P8	GPIOMV, MS	0	110	0
DDI0_DDC_CLK	I/O	V1P8	GPIOMV, MS, CLK	Input (20k PU)	Input (20k PU)	Input (20k PU)
DDI0_DDC_DATA	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)
DDI0_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)
DDI0_VDDEN	I/O	V1P8	GPIOMV, MS	0	0	0 11
DDI0_RCOMP_N	0	V1P24	DDI	Z	Output	Output
DDI0_RCOMP_P	0	V1P24	DDI	Z	Output	Output
DDI1_TXP[3:0]	0	V1P24	DDI	Z	Output	Output
DDI1_TXN[3:0]	0	V1P24	DDI	Z	Output	Output
DDI1_AUXP	I/O	V1P24	DDI	Z	Output	Output



Table 14. Digital Display Interface Signals (Sheet 2 of 2)

iefil'				Default Buffer State			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
DDI1_AUXN	I/O	V1P24	DDI	Z	Output	Output	
DDI1_BKLTCTL	I/O	V1P8	GPIOMV, MS	0	0	96,0	
DDI1_BKLTEN	I/O	V1P8	GPIOMV, MS	0	0 0	0	
DDI1_DDC_CLK	I/O	V1P8	GPIOMV, MS, CLK	Input (20k PU)	Input (20k PU)	Input (20k PU)	
DDI1_DDC_DATA	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
DDI1_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)	
DDI1_VDDEN	I/O	V1P8	GPIOMV, MS	0	0	0 0	
DDI1_RCOMP_N	0	V1P24	DDI	Z	Output	Output	
DDI1_RCOMP_P	0	V1P24	DDI	Z	Output	Output	
DDI2_DDC_CLK	I/O	V1P8	DDI	Z	Output	Output	
DDI2_DDC_DATA	I/O	V1P8	DDI	Z	Output	Output	
DDI2_TXP[3:0]	0	V1P24	DDI	Z	Output	Output	
DDI2_TXN[3:0]	0	V1P24	DDI	Z	Output	Output	
DDI2_AUXP	I/O	V1P24	DDI	Z	Output	Output	
DDI2_AUXN	I/O	V1P24	DDI	od ^U Z	Output	Output	
DDI2_HPD	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)	
	DDI1_AUXN DDI1_BKLTCTL DDI1_BKLTEN DDI1_DDC_CLK DDI1_DDC_DATA DDI1_HPD DDI1_VDDEN DDI1_RCOMP_N DDI1_RCOMP_P DDI2_DDC_CLK DDI2_DDC_DATA DDI2_TXP[3:0] DDI2_AUXP DDI2_AUXN	DDI1_AUXN I/O DDI1_BKLTCTL I/O DDI1_BKLTEN I/O DDI1_DDC_CLK I/O DDI1_DDC_DATA I/O DDI1_HPD I/O DDI1_VDDEN I/O DDI1_RCOMP_N O DDI1_RCOMP_P O DDI2_DDC_CLK I/O DDI2_TXP[3:0] O DDI2_AUXP I/O DDI2_AUXN I/O	Dir Power	DIT	Signal Name Dir Plat. Power Type Pwrgood Assert State DDI1_AUXN I/O V1P24 DDI Z DDI1_BKLTCTL I/O V1P8 GPIOMV, MS 0 DDI1_BKLTEN I/O V1P8 GPIOMV, MS 0 DDI1_DDC_CLK I/O V1P8 GPIOMV, MS Input (20k PU) DDI1_DDC_DATA I/O V1P8 GPIOMV, MS Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS 0 DDI1_VDDEN I/O V1P8 GPIOMV, MS 0 DDI1_RCOMP_N O V1P24 DDI Z DDI1_RCOMP_P O V1P24 DDI Z DDI2_DDC_CLK I/O V1P8 DDI Z DDI2_DDC_DATA I/O V1P8 DDI Z DDI2_TXP[3:0] O V1P24 DDI Z DDI2_AUXP I/O V1P24 DDI	Signal Name Dir Plat. Power Type Pwrgood Assert State Resetout Deassert State DDI1_AUXN I/O V1P24 DDI Z Output DDI1_BKLTCTL I/O V1P8 GPIOMV, MS 0 0 DDI1_BKLTEN I/O V1P8 GPIOMV, MS 0 0 DDI1_DDC_CLK I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_DDC_DATA I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS Input (20k PU) Input (20k PU) DDI1_HPD I/O V1P8 GPIOMV, MS	

MIPI DSI Interface Signals

MIPI DSI Interface Signals (Sheet 1 of 2) Table 15.

edu			Defa	dell			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	III.
MDSI_A_CLKN	0	V1P24	MIPI-DPHY	0	0	0	
MDSI_A_CLKP	0	V1P24	MIPI-DPHY	0	0,00	0	
MDSI_A_DN[3:0]	I/O	V1P24	MIPI-DPHY	0	1000	0	
MDSI_A_DP[3:0]	I/O	V1P24	MIPI-DPHY	0	0	0	
MDSI_C_CLKN	0	V1P24	MIPI-DPHY	0	0	0	ineo.
MDSI_C_CLKP	0	V1P24	MIPI-DPHY	1100	0	0	deill
d undefine			d undefine			undefine	d undefined f
	ned l	indefine	d undefine		d undefined		



Table 15. MIPI DSI Interface Signals (Sheet 2 of 2)

1efine			Default Buffer State			
Signal Name	Dir	Plat. Power Type		Pwrgood Assert State	Resetout Deassert State	S0ix
MDSI_C_DN[3:0]	I/O	V1P24	MIPI-DPHY	0	0	0
MDSI_C_DP[3:0]	I/O	V1P24	MIPI-DPHY	0	0	0
MDSI_RCOMP	I/O	V1P24	MIPI-DPHY	0	0.0	0

2.7 MIPI Camera Serial Interface (CSI) and ISP Interface Signals

Table 16. MIPI CSI Interface Signals

, Ull.		Default Buffer State				
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
MCSI_1_CLKN	O.I.	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_1_CLKP	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_1_DN[0:3]	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_1_DP[0:3]	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_2_CLKN	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_2_CLKP	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_2_DN[0:1]	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_2_DP[0:1]	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_3_CLKN	I	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_3_CLKP	O.I.	V1P24	MIPI-DPHY	Input	Input	Input
MCSI_RCOMP	I/O	V1P24	MIPI-DPHY	Input	Input	Input



PCI Express Signals

Table 17. PCIe Signals and Clocks

ineo.			Default Buffer State			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
PCIE_RXN[0:1]	Je i	V1P05	PCIe PHY	Х	Weak Pull Down	Input
PCIE_RXP[0:1]	I	V1P05	PCIe PHY	X	Weak Pull Down	Input
PCIE_TXN[0:1]	0	V1P05	PCIe PHY	X	Z	Output
PCIE_TXP[0:1]	0	V1P05	PCIe PHY	X	Z	Output
P_RCOMP_N	IO	Х	PCIe PHY	Х		Off
P_RCOMP_P	IO	Х	PCIe PHY	Х		Off
PCIE_CLKREQ[0:1]_N	IO	V1P8	GPIOMV, MS	Х	Input (20k PU)	Prg

Low Power Engine (LPE) for Audio (I²S) Interface

Table 18. LPE Interface Signals

	ndefill.			10:11	Def	Default Buffer State		
ndefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
	LPE_I2S[2:0]_CLK	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	0	
	LPE_I2S[2:0]_FRM	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	1	
	LPE_I2S[2:0]_DATAOUT	I/O	V1P8	GPIOM V, MS	0 (20k PD)	0 (20k PD)	0	
	LPE_I2S[2:0]_DATAIN	I/O	V1P8	GPIOM V, MS	Input (20k PD)	Input (20k PD)	Input	
ndefine	defin	ed u				led undefine		
	d undefined undefine			inde	Hined under	red undefined	4efi	
Datasheet			iefin	ed u.		ine	d undef	
71.			MOL			defill		



2.10

2.10.1

Table 19. Storage Controller (eMMC, SDIO, SD) Interface Signals

1 Storage	Con	trolle	r (eMMC, S	3D10, 3D)	ad undefined	A
19. Storage Co	ntroll	ier (emi	ic, sdio, sd		nais efault Buffer Sta	ite define
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
MMC1_D[7:0]	I/O	V1P8	GPIOMV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
MMC1_CMD	I/O	V1P8	GPIOMV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
MMC1_CLK	I/O	V1P8	GPIOMV, HS, CLK	0 (20k PD)	0 (20k PD)	0 (20k PD)
MMC1_RCLK	I/O	V1P8	GPIOMV, HS	Z (20k PD)	Z	Z
MMC1_RESET_N	I/O	V1P8	GPIOMV, HS	Z	Z	Z
MMC1_RCOMP	I/O	V1P8	GPIOMV, HS, RCOMP	Z	Z	d unz
SD2_D[2:0]	I/O	V1P8	GPIOMV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
SD2_D[3]_CD_N	I/O	V1P8	GPIOMV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
SD2_CMD	I/O	V1P8	GPIOMV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
SD2_CLK	I/O	V1P8	GPIOMV, HS, CLK	0 (20k PD)	0	0
SD3_D[3:0]	I/O	V1P8/ V3P3	GPIOHV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
SD3_CMD	I/O	V1P8/ V3P3	GPIOHV, HS	Z (20k PU)	Z (20k PU)	Z (20k PU)
SD3_PWREN_N	I/O	V1P8	GPIOMV, HS	1 (20k PD)	1	-
SD3_CLK	I/O	V1P8/ V3P3	GPIOHV, HS, CLK	0 (20k PD)	onde,	0
SD3_RCOMP	I/O	V1P8/ V3P3	GPIOHV, HS, RCOMP	Z	lue z	Z
SD3_1P8_EN	I/O	V1P8	GPIOMV, HS	0 (20k PD)	0	-
SD3_CD_N	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)



defined undefined undefined High Speed UART Interface Signals High Speed UART 5 2.11

Table 20.

	siln		_		ed un	ate UN	e, III.	
efined undefined	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
1 under	UART1_DATAIN	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
efineo	UART1_DATAOUT	I/O	V1P8	GPIOMV, MS	1 (20k PU)	d uno1	1	definer
	UART1_RTS_N	I/O	V1P8	GPIOMV, MS	1 (20k PU)	1	1	efine
	UART1_CTS_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
	UART2_DATAIN	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)	
indefine	UART2_DATAOUT	I/O	V1P8	GPIOMV, MS	1 (20k PU)	1 sined	1	
Jefined undefined	UART2_RTS_N	I/O	V1P8	GPIOMV, MS	1 (20k PU)	4 undein	1	
e.	UART2_CTS_N	I/O	V1P8	GPIOMV,	Input (20k PU)	Input (20k PU)	Input (20k PU)	:: 108
ined under		-81	undefil			indefine		
Lefined unde	.20	ned'	undefil			ed undefine		
defined unde	d under	ined '	undefil		.nde ^{fi}	ned undefine		defil?
defined unde	adefined undef	ined '	undefil		stined undefi	ned undefine	,o	_{Jindefir}
defined unde	ed undefined undef	ined '	undefil	od und	efined undefi	ned undefine	o undefined i	Indefin
idefined undefin	ed undefined undef	ined'	undefil	ned und	efined undefi	ned undefine	ed undefined i	_{JIP} defir
idefined undefin	ed undefined undef	ined ined	undefil	ned und	efined undefi	ned undefine	ed undefined i	Indefin
idefined undefin	ed undefined undef	ined ined	undefi	ned und	efined undefi	ned undefine	ed undefined i	_J ndefi ^r
idefined undefin	UART2_CTS_N Jefined undefined undef	ined ined	undefil	ned und	efined undefi	ned undefine	ed undefined i	undefin
defined undefin	ed undefined und	ined ined	undefil	ned und	efined undefi	ned undefine	ed undefined in a specific distribution of the specific distribution of th	undefin
defined undefin	UART2_CTS_N UART2_CTS_N	ined ined	undefil	ined und	efined undefi	ned undefine	ed undefined in ned undefined in a second contract to the second con	_{Jindefi} r



2.12

Table 21. I²C Interface Signals

	d und	Stille			ndefi	ned		ndefined
<u>(in</u>	tel) ed und			ind	efined undefi	Pi	hysical Interfaces	
ned undefine 2.12			76			ned undefine	d un	
Table		efin		igilais		ined un		ofined
					Ded Ully D	efault Buffer Sta	ite	inge
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
ined undefine	I2C0_DATA	I/O	V1P8	GPIOMV, MS, I2C	Z (1k PU, OD)	Z (1k PU, OD)	Z (1k PU, OD)	
ined une	I2C0_CLK	I/O	V1P8	GPIOMV, MS, I2C	Z (1k PU, OD)	Z (1k PU, OD)	Z (1k PU, OD)	
	I2C1_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	I2C1_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	undefil.
	I2C2_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
1efin	I2C2_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
afined undefin	I2C3_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
Aline	I2C3_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	4
	I2C4_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	odefin
	I2C4_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	Julia
	I2C5_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
4 nuger,	I2C5_CLK	I/O	V1P8	GPIOMV	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
Jefined undefil	I2C6_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	I2C6_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	aefil ⁱ
defined undef	ined undefined		41	Indefined	undefined	nde	Z (20k PU, OD) Z (20k PU, OD) Datasheet	id un
define	indefined	und	efineo		defined u	ndefined ur	7/3	ed undefi
38 ad unde	ilined D.			undefined	June		Datasheet	
efine			eined			ad une		



NFC I²C Interface Signals 2.13

Table 22. NFC I²C Interface Signals

				Default Buffer State					
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	Soix			
NFC_I2C_DATA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)			
NFC_I2C_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)			
GPIO_ALERT	I/O	V1P8	GPIOMV, MS	0 (20k PU)	0 0	0			

PCU- Fast Serial Peripheral Interface (SPI) Signals 2.14

Table 2	3. PCU- Fast Serial	Perip	oheral I	nterface	(SPI) Signals	ed	undefined
ed une		יוט ג	96.		De	fault Buffer Stat	
undefined unde Table 2	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
	FST_SPI_CLK	I/O	V1P8	GPIOMV, HS	0 (20k PU)	Output	Output
undefined undefined	FST_SPI_CS[0]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	Output	Output
indefine	FST_SPI_CS[1]_N	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Output	Output
fined by	FST_SPI_CS[2]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	Output	Output
nuge,	FST_SPI_D[3:0]	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)
Jundefined undefined	undefined undefi	ined '	undefin	ed unde	Fined undefi	ned undefine	d undefine
Datasheet	d undefinee			ed und	efined		undefin



2.15 PCU - Real Time Clock (RTC) Interface Signals

Table 24. PCU - Real Time Clock (RTC) Interface Signals

					Def	ault Buffer S	tate
ndefined undefined un	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
4 under	RTC_X1	I	V3P3	RTC PHY	Input (Crystal)	Input (Crystal)	Input (Crystal)
defined	RTC_X2	0	V3P3	RTC PHY	Output (Crystal)	Output (Crystal)	Output (Crystal)
Inc	RTC_RST_N	I	V3P3	RTC PHY	Input	Input	Input
	RTC_TEST_N	I	V3P3	RTC PHY	Input	Input	Input
	RTC_EXTPAD	0	V3P3	RTC PHY	Input	Input	Input

2.16 PCU - Low Pin Count (LPC) Bridge Interface Signals

Table 25. PCU - LPC Bridge Interface Signals

4 nuc				De	efault Buffer Sta	ite
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
LPC_AD[3:0]	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)
LPC_FRAME_N	I/O	V3P3/ V1P8	GPIOHV, HS	1 (20k PU)	1 defi	1
LPC_SERIRQ	I/O	V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)
LPC_CLKRUN_N	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PU)	Input (20k PU)	Input (20k PU)
LPC_CLKOUT[0]	I/O	V3P3/ V1P8	GPIOHV, HS	0 (20k PU)	Clock	0
LPC_CLKOUT[1]	I/O	V3P3/ V1P8	GPIOHV, HS	Input (20k PD)	Input	Input
LPC_RCOMP	I/O	V3P3/ V1P8	GPIOHV, HS	Z	Z	ine z

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PCU - Power Management Controller (PMC) 2.17 **Interface Signals**

PCU - Power Management Controller (PMC) Interface Signals Table 26.

1	uge.			4efil	De	efault Buffer Sta	ault Buffer State		
Jefined C	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	Jinden Soix		
	PMC_PLTRST_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	unden.	1		
	PMC_PWRBTN_N	I	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)		
I	PMC_RSTBTN_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)		
	PMC_SUSPWRDNACK	I/O	V1P8	GPIOMV, MS	0 (20k PD)	0 (20k PD)	0 (20k PD)		
,	PMC_SUS_STAT_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	1	nug ₀ 0		
Ī	PMC_SUSCLK[0]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	32 KHz Clock	32 KHz Clock		
ı	PMC_SLP_S4_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	ed 11	1		
	PMC_SLP_S0ix_N	I/O	V1P8	GPIOMV, MS	0 (20k PU)	1	0 at S0ix2		
	PMC_ACPRESENT	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Input (20k PD)	Input (20k PD)		
	PMC_BATLOW_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)		
-	PMC_WAKE_N	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Input (20k PU)	Input (20k PU)		
	PMC_CORE_PWROK	IQ.	V3P3	RTC PHY	Input	Input	Input		
		1.00			-		Input		
	PMC_RSMRST_N			20	afined under				



Serial Peripheral Interface (SPI) Signals 2.18

Table 27. Serial Peripheral Interface (SPI) Signals

				Default Buffer State					
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix			
SPI[1,2,3]_CLK	I/O	V1P8	GPIOMV, HS	0 (20k PU)	0	0			
SPI[1,2,3]_CS[0:1]_N	I/O	V1P8	GPIOMV, HS	1 (20k PU)	nuger.	1			
SPI[1,2,3]_MOSI	I/O	V1P8	GPIOMV, HS	0 (20k PU)	(SO 0	0			
SPI[1,2,3]_MISO	I/O	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PD)	Input			

Table 28. JTAG Interface Signals

1/0	V1P8	GPIOMV, HS	Input (20k PU)	Input (20k PD)	Input
		Signals	Hined Un		ad undefined
		e.	De	efault Buffer Sta	ite
Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
I/O	V1P8	GPIOMV, MS	Input (5k PD)	Input (5k PD)	Input (5k PD)
I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)
I/O	V1P8	GPIOMV, MS	Z Z	Z	Z
I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)
I/O	V1P8	GPIOMV, MS	Input (5k PU)	Input (5k PU)	Input (5k PU)
I/O	V1P8	GPIOMV, MS	Z (5k PU, OD)	Output (5k PU, OD)	Z (5k PU, OD)
I/O	V1P8	GPIOMV, MS	Input (5k PU, OD)	Input (5k PU, OD)	Input (5k PU, OD)
	Terestate Direct	terface Color	terface Signals Dir Plat. Power Type I/O V1P8 GPIOMV, MS I/O V1P8 GPIOMV, MS	Type	Terface Signals Default Buffer Sta Dir Plat. Power Type Pwrgood Assert State Resetout Deassert State I/O V1P8 GPIOMV, MS Input (5k PD) Input (5k PD) I/O V1P8 GPIOMV, MS Input (5k PU) Input (5k PU) I/O V1P8 GPIOMV, MS Z Z I/O V1P8 GPIOMV, MS Input (5k PU) Input (5k PU) I/O V1P8 GPIOMV, MS Input (5k PU) OD) I/O V1P8 GPIOMV, MS Input (5k PU, OD) Output (5k PU, OD) I/O V1P8 GPIOMV, MS Input (5k PU, Input (5k PU, OD)

Integrated Sensor Hub Interface Signals 2.20

Table 29. Integrated Sensor Hub Interface Signals (Sheet 1 of 2)

		6	efille	Default Buffer State			
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	
ISH_GPIO[7:0]	I/O	V1P8	GPIOMV, MS	Input (20k PD)	Z (20k PU)	Z (20k PU)	

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	ed undefine				ed undefined			refined un
Physical In				d undefin	edu	. 1	(intel)	
Table 29	9. Integrated Ser	nsor	Hub Int	erface Sig	_	of 2)	ite	dund
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix	idefinect
ad un	ISH_GPIO[8]	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
afines	ISH_GPIO[9]	I/O	V1P8	GPIOMV, MS	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	ISH_I2C1_SDA	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	
	ISH_I2C1_CLK	I/O	V1P8	GPIOMV, MS, I2C	Input (20k PU)	Z (20k PU, OD)	Z (20k PU, OD)	ined un

PWM Interface Signals 2.21

od u	nde .			undef			defined
Table 30). PWM Interface	Sig	nal 👯				Julie
			"uge"		De	efault Buffer Sta	te
	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
	PWM[0]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	0	0
40	PWM[1]	I/O	V1P8	GPIOMV, MS	0 (20k PU)	0	o fine

SVID Interface Signals

Table 31. SVID Interface Signal

ed un.				UNO De	efault Buffer Sta	te	defill
Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	Soix	, un
SVID_DATA	I/O	V1P8	GPIOMV, MS	0	0	1 or Z	
SVID_CLK	I/O	V1P8	GPIOMV, MS	0	1 or Z	1 or Z	
SVID_ALERT_N	I/O	V1P8	GPIOMV, MS	Input	Input	Input	sined!
undefined			.0	defined unit			d undefined
			afined un			ned under 43	}
		ed nuc			ed nuger		

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Miscellaneous Signals 2.23

Table 32. Miscellaneous Signals and Clocks

					ed un	efault Buffer Sta	ite
sined ur	Signal Name	Dir	Plat. Power	Туре	Pwrgood Assert State	Resetout Deassert State	S0ix
d nuder.	PLT_CLK[0:5]	I/O	V1P8	GPIOMV, MS	0 (20k PD)	Clock (20k PD)	01
adefinet	PROCHOT_N	I/O	V1P8	GPIOMV, MS	Z	edulz	Z
	NOTE: '0' in S0i2	or bel	ow.		defi		

2.24 **Hardware Straps**

All straps are sampled on the rising edge of PMC_RSMRST_N.

While PMC_RSMRST_N is low all strap pins are in input mode. Weak pull ups or downs keep straps from floating during this time. Strap values can be changed by driving the strap pins or using stronger pull resistors.

Table 33. Straps (Sheet 1 of 2)

	Signal Name	Purpose	Pull up/Pull Down	Strap Description
ined ur	GPIO_SUS[0] ¹	DDI0 Detect	Weak internal pull down of 20K	DDI0 Detect 0 = DDI0 not enabled 1 = DDI0 enabled
Jundefined undefined un	GPIO_SUS[1]	DDI1 Detect	Weak internal pull down of 20K	DDI1 Detect 0 = DDI1 not enabled 1 = DDI1 enabled
J under II	GPIO_SUS[2]	A16 swap overdrive	Weak internal pull up of 20K	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
ed V	GPIO_SUS[3]	DSI Display Detect	Weak internal pull down of 20K	MIPI DSI Detect 0 = DSI not enabled 1 = DSI enabled
ed undefill	GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull up of 20K	BIOS Boot Selection 0 = Default 1 = SPI
d undefined undefined v	GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull up of 20K	Security Flash Descriptors 0 = Override 1 = Normal Operation
44 44 Lefined undefined	Indefined	ned undefined ur	ndefined un	Datasheet



Jefined undefined undefined ndefined undefined Straps (Sheet 2 of 2) Table 33.

, nuc				fine	
Table 33.	Straps (Sheet 2 of Signal Name	Purpose	Pull up/Pull Down	Strap Description] , ,
	ned under		ad undefine	0 = Supply is 1.25V 1 = Supply is 1.35V	idefined u
Jefined undefined undef	GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull up of 20K	This strap also contains PLL LDO 0: supply is 1.25V 1: supply is 1.35V. Selects supply voltage for	
Jefine .	ndefined		lefined u	LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI	ined
ed unde	GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull down of 20K	Bypasses LDOs for ICLK 0 = Use LDOs 1 = Bypass LDOs (Supply1.05V on power pins)	nden.
defined undefined unde	GPIO_SUS[10]	POSM Select	Weak internal pull down of 20K	Selects which POSM (power on state machine) will be observed at time 0 0 = Fuse controller 1 = PMC	
	GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	define
ó	GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	and
fined ul.	GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull down of 20K	0 = No Bypass 1 = Bypass	
	NOTE: 1. Ignore this strap a can be used as a G		anism to detect the rel	evant DDI port. This signal	1
uge.	ed undefine		4 undefineo		ndefine

NOTE:

Datasheet dunde ined under ined u 1. Ignore this strap and use a software mechanism to detect the relevant DDI port. This signal ad as and and efined undefined undef

ashe Indefil



idefined undefined undefined **SoC RCOMP List** 2.25

Table 34. RCOMP's List (Sheet 1 of 2)

Table 34. RC Interface Name DDR3 D L MIPI DSI MIPI DSI	COMP's List (Sheet 1 RCOMP Name DDR3_M0_RCOMPPD/ PDDR3_M0_RCOMPPD DDR3_M1_RCOMPPD PDDR3_M1_RCOMPPD PDDR3_M1_RCOMPPD PDDR3_M1_RCOMPPD		Remarks RCOMP pins for DDR3
Interface Name DDR3 D L MIPI DSI M	RCOMP Name DDR3_M0_RCOMPPD/ PDDR3_M0_RCOMPPD DDR3_M1_RCOMPPD PDDR3_M1_RCOMPPD	Bias 182 Ohm ±1% to Ground 182 Ohm ±1% to	60
Name DDR3 L D L MIPI DSI M	DDR3_M0_RCOMPPD/ PDDR3_M0_RCOMPPD DDR3_M1_RCOMPPD PDDR3_M1_RCOMPPD	182 Ohm ±1% to Ground 182 Ohm ±1% to	60
MIPI DSI M	PDDR3_M0_RCOMPPD DR3_M1_RCOMPPD PDDR3_M1_RCOMPPD	Ground 182 Ohm ±1% to	RCOMP pins for DDR3
MIPI DSI M	PDDR3_M1_RCOMPPD		20
	IDSI_RCOMP		define
MIPI CSI M	46111	150 Ohm ±1% to Ground	RCOMP pin for MIPI DSI
	1CSI_RCOMP	150 Ohm ±1% to Ground	RCOMP pin for MIPI CSI
eMMC M	MC1_RCOMP	100 Ohm ±1% to Ground	eMMC, SDIO, FST_SPI RCOMP
SD Card S	D3_RCOMP	80.6 Ohm ±1% to Ground	SD Card contains its own RCOMP as it can be either 1.8V or 3.3V. Special care is needed to perform an RCOMP any time a card is inserted.
LPC L	PC_RCOMP	100 Ohm ±1% to Ground	LPC has its own RCOMP because it can operate at 1.8V or 3.3V.
iCLK I	CLK_ICOMP	2.5k Ohm ±1% to Ground	The calibration will be handled inside the iCLK.
4efined L	CLK_RCOMP	50 Ohm ±1% to Ground	ad under
USB2 U	ISB_RCOMP	113 Ohm ±1% to Ground	The calibration will be handled inside USB
HSIC U	SB_HSIC_RCOMP	45 Ohm ±1% to Ground	The calibration is handled inside the USB HSIC.
	SB_SSIC_RCOMP_P SB_SSIC_RCOMP_N	90 Ohm ±1% Between SSIC RCOMP pads	The calibration is handled inside the USB SSIC.
::08	JSB3_RCOMP_N JSB3_RCOMP_P	402 Ohm 1% between RCOMP pads	The calibration is handled inside the USB3.
GPIO G	GPIO0_RCOMP	100 Ohm to Ground	Will be shared across all GPIO buffers on the north side of the chip.
<u> </u>	CIE_RCOMP_N CIE_RCOMP_P	402 Ohm 1% between RCOMP pads	The Calibration is handled in PCIE.
46 undefined und	defili	defined und	Datasheet



Table 34. RCOMP's List (Sheet 2 of 2)

Interface Name	RCOMP Name	Bias	Remarks
DDI	DDI0_RCOMP_N	402 Ohm 1%	The calibration is handled in DDI
indef	DDI0_RCOMP_P	between RCOMP pads	sined u
eg u.	DDI1_RCOMP_N	402 Ohm 1%	nden
	DDI1_RCOMP_P	between RCOMP pads	ined un.

2.26 **GPIO Muxing**

Not all interfaces can be active at the same time. To provide flexibility, these shared interfaces are muxed with GPIOs.

All GPIOs default to function as GPIO name at boot. BIOS is responsible for enabling Note:

proper configuration.

GPIO Number= GPIO pin location

GPIO mode= GPIO mode in which the pin operates

Table 35. Multiplexed Functions - T4 SoC (Sheet 1 of 11)

	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	ISH_GPIO[8]/ ISH_SPI_CS[0]_N/ I2S5_CLK	BL9	E23		ISH_GPIO[8]	ISH_SPI _CS[0]_ N	I2S5_CLK		undefin	S _C
-9	LPC_AD[2]/ ISH_GPIO[14]/ ISH_I2C0_DATA	BP20	SE45	, und	LPC_AD[2]	ISH_GPI O[14]	ISH_I2C0_ DATA	ndefine		
d undefine	I2C4_CLK/ DDI0_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	BP34	SW52	ico.	I2C4_CLK	DDI0_D DC_CLK	DDI2_DDC _CLK	MDSI_DDC _CLK		26
	LPC_AD[3]/ ISH_GPIO[15]/ ISH_I2CO_CLK/ SPI2_MOSI	BR21	SE50		LPC_AD[3]	ISH_GPI O[15]	ISH_I2C0_ CLK	SPI2_MOSI	ndefi	ued nuc
φQ	PMC_PLT_CLK[4]/ ISH_GPIO[14]/ ISH_I2C0_DATA/ SPI2_MISO	BR7	SE3	od un	PMC_PLT_ CLK[4]	ISH_GPI O[14]	ISH_I2CO_ DATA	SPI2_MISO	sq on	
ed under	PMC_PLT_CLK[1]/ ISH_GPIO[11]/ ISH_UART_DATAIN /SPI2_CS[1]_N	BR9	SE2	ine	PMC_PLT_ CLK[1]	ISH_GPI O[11]	ISH_UART_ DATAIN	SPI2_CS[1]_N		2008
		indefill				ndefine	0		26	lived or
	Datasheet			ال 1	ndefined l	, ,			led under	47
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adefill.			996				4efined	unde		
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	T4 SoC (S	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	
I2C4_DATA/ DDI2_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	BT32	SW46		I2C4_DAT A	efined '	DDI2_DDC _DATA	MDSI_DDC _DATA	eiis	ed undef	1
PMC_PLT_CLK[5]/ ISH_GPIO[15]/ ISH_I2CO_CLK/ SPI2_MOSI	BT6	SE6	290	PMC_PLT_ CLK[5]	ISH_GPI O[15]	ISH_I2CO_ CLK	SPI2_MOSI	d nuger.		
MMC1_RCLK/ MMC1_RESET_N	BU13	SE69	ed uit	MMC1_RCL K	MMC1_R ESET_N	6-	NUGE			
PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	BU7	SE7		PMC_PLT_ CLK[2]	ISH_GPI O[12]	ISH_UART_ CTS_N	SPI2_CS[0]_N		d unde	
PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	BU9	SE4		PMC_PLT_ CLK[3]	ISH_GPI O[13]	ISH_UART_ RTS_N	SPI2_CLK	d undefi	Weg.	
DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E21	N67	ued uni	DDI2_DDC _CLK	DDI1_D DC_CLK	UARTO_DA TAOUT	MDSI_DDC _CLK	MDSI_A_ TE		
GPIO_N1/ C0_BPM3_TX/ C1_BPM3_TX	E39	N1			eine	Inde		C0_BPM3 _TX	C1_BPM3 _TX	6
DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	F20	N62		DDI2_DDC _DATA	DDI1_D DC_DAT A	UARTO_DA TAIN	MDSI_DDC _DATA	MDSI_C_ TE		
DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	F26	N71	ined ur	DDI0_DDC _CLK	DDI1_D DC_CLK	MDSI_DDC _CLK	od nuge,			
GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F38	N2			_0	d nudeil		C0_BPM2 _TX	C1_BPM2 _TX	96
GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	G39	N4		- 2	undefin			C0_BPM0 _TX	C1_BPM0 _TX	
DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	H26	N66	. 13	DDI0_DDC _DATA	DDI1_D DC_DAT A	MDSI_DDC _DATA	adefi	ned		
JTAG2_TMS	J37	N24	fined	JTAG2_TM S		2/2	ed un			
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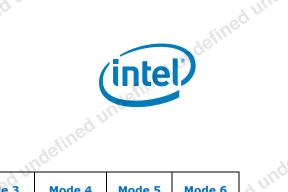
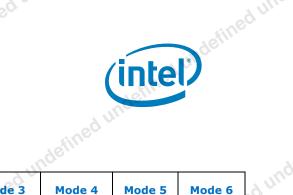


Table 35. Multiplexed Functions - T4 SoC (Sheet 3 of 11)

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				ned undef				ILISO.	
ndei			Jef!	Ue					
Table 35.	Multiple	xed Fur	nctions -	T4 SoC (S	heet 3 of	11)	uger.		
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode (
GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	J39	N6			tined un	0		C0_BPM3 _TX	C1_BPM _TX
GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	K40	N8		ned undi	0		2	C0_BPM1 _TX	C1_BPM _TX
GPIO_N3/ C0_BPM1_TX/ C1_BPM1_TX	B38	N3	d under				indefined	C0_BPM1 _TX	C1_BPM _TX
ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	C39	N7				ndefined	ISH_GPIO[13]	C0_BPM2 _TX	C1_BPM _TX
GPIO_NO/ CO_BPMO_TX/ C1_BPMO_TX	D40	NO NO		. 3	efined u			C0_BPM0 _TX	C1_BPM _TX
GPIO_CAMERASB0 3	B28	N51		GPIO_CAM ERASB03				nuger	
JTAG_TMS	B34	N34	26	JTAG_TMS		 	sine		
PMC_PWRBTN_N	BH10	E8	ed nuo	PMC_PWR BTN_N		6.0	under		
SD3_D[2]	BH18	SE33		SD3_D[2]		46/1/10			
PMC_RSTBTN_N	BH24	SE76		PMC_RSTB TN_N	fined'	Juga			ed und
UART2_RTS_N	BH26	SW19		UART2_RT S_N	De.			d undefi	
UART2_DATAIN LPE_I2S0_CLK	BH28	SW17	ed und	UART2_DA TAIN			undefine		
LPE_I2S0_CLK	BH32	SW31		LPE_I2S0_ CLK		define			
I2C6_CLK/NMI_N	BH34	SW53	1	I2C6_CLK	NMI_N	Ulla			0
I2C2_DATA	ВН36	SW62		I2C2_DAT A	ndefined			Ae ^{fi}	ned un
PMC_BATLOW_N	BH4	E1		PMC_BATL OW_N			i afiir	ed uno	
LPE_I2S2_FRM	BH40	SW96	ned un	LPE_I2S2_ FRM			d unde		
PMC_SUS_STAT_N	ВН6	E2 de		PMC_SUS_ STAT_N		undefin			.1
	ndefill				1efine	0			ined u
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			wed .				4 Uli		



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odefill.			nde	*			4efined	unde	
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	T4 SoC (S	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
MMC1_CMD	ВЈ15	SE23		MMC1_CM		ingelli			def
LPC_FRAME_N/ UARTO_DATAIN/ SPI2_MISO	BJ19	SE48		D LPC_FRAM E_N	UARTO_ DATAIN		SPI2_MISO	defin	Eq nin
GPIO_ALERT/ ISH_GPIO[11]/ ISH_UART_DATAIN	BJ21	SE77	und	GPIO_ALE RT	ISH_GPI O[11]	ISH_UART_ DATAIN	adefine	3. 3.1.1.1	
FST_SPI_D[2]	BJ25	SW0	(e _Q	FST_SPI_ D[2]		ed.	OIL.		
PMC_SLP_S3_N	ВЈЗ	E0		PMC_SLP_ S3_N	60	undefille			unde
LPE_I2S1_DATAIN	BJ30	SW37		LPE_I2S1_ DATAIN	define			, si	Veg
NFC_I2C_CLK	BJ33	SW54		NFC_I2C_ CLK				4 nuge,	
UARTO_DATAIN	BJ37	SW77	d uni	CER	UARTO_ DATAIN		indefine	O	
PMC_PLTRST_N	BJ5	E5	Vecr	PMC_PLTR ST_N		define	o. O.		
PMC_WAKE_N	BJ7	E10		PMC_WAK E_N		Julia			dund
PMC_SLP_S4_N	BJ9	E9		PMC_SLP_ S4_N	ndefill			inde	ined
ISH_GPIO[6]/ I2S4_DATAOUT	BK10	E25		ISH_GPIO[6]		I2S4_DATA OUT	717	SQ	
MMC1_D[3]	BK12	SE26	sed un	MMC1_D[3			4 nuge.		
MMC1_D[1]	BK14	SE24		MMC1_D[1		defin	0.		
SD3_D[0]	BK16	SE35		SD3_D[0]	_0	dun			un
SPI1_MOSI	BK18	SE64		SPI1_MOS I	adefilm			. (liveo
LPC_CLKOUT[0]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	BK20	SE51		LPC_CLKO UT[0]	ISH_GPI O[10]		ISH_UART _DATAOUT	veq nuo	
PMC_SUSPWRDNA CK	BK22	SE83	fined	PMC_SUSP WRDNACK		lefil)	ed una		
50 sined undefined	indefine	ed uli		WRDNACK	defin	led unde			ofined ur
50 indefined				defined	une			Data	sheet
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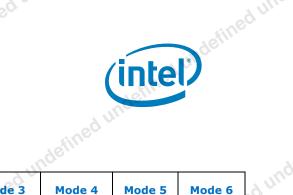


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Table 35. GPIO Pin Name FST_SPI_D[1] UART2_DATAOUT LPE_I2S0_FRM I2C5_CLK SPI3_MOSI LPE_I2S2_CLK	Multiple: Package Ball # BK26 BK28 BK32 BK34 BK36 BK36	SW51 SW55 SW21 SW50 SW82	Mode 0	T4 SoC (S Mode 1 FST_SPI_ D[1] UART2_DA TAOUT	Sheet 5 of Mode 2	11) Mode 3	Mode 4	Mode 5	Mode
GPIO Pin Name FST_SPI_D[1] UART2_DATAOUT LPE_I2S0_FRM I2C5_CLK SPI3_MOSI	Package Ball # BK26 BK28 BK32 BK34 BK36	GPIO # SW5 SW21 SW35 SW50		Mode 1 FST_SPI_ D[1] UART2_DA		-90	Mode 4	Mode 5	Mode
GPIO Pin Name FST_SPI_D[1] UART2_DATAOUT LPE_I2S0_FRM I2C5_CLK SPI3_MOSI	Package Ball # BK26 BK28 BK32 BK34 BK36	GPIO # SW5 SW21 SW35 SW50		Mode 1 FST_SPI_ D[1] UART2_DA		-90	Mode 4	Mode 5	Mode
Name FST_SPI_D[1] UART2_DATAOUT LPE_I2S0_FRM I2C5_CLK SPI3_MOSI	BAII # BK26 BK28 BK32 BK34 BK36	# SW5 SW21 SW35 SW50	Mode 0	FST_SPI_ D[1] UART2_DA	Mode 2	Mode 3	Mode 4	Mode 5	Mode
UART2_DATAOUT LPE_I2S0_FRM I2C5_CLK SPI3_MOSI	BK28 BK32 BK34 BK36	SW21 SW35 SW50	AG	D[1] UART2_DA	ined un	0		1	
LPE_I2S0_FRM I2C5_CLK SPI3_MOSI	BK32 BK34 BK36	SW35	ACE						unde
I2C5_CLK SPI3_MOSI	BK34 BK36	SW50	46		· ·			ndefine	J
SPI3_MOSI	BK36			LPE_I2S0_ FRM			ined		
SPI3_MOSI	BK36		, uno	I2C5_CLK			"geill		
LPE_I2S2_CLK	BK38	46,11	0	_	SPI3_MO SI	sined			
		SW92		LPE_I2S2_ CLK	ے ن	ugeili			nd'
PMC_ACPRESENT	BK4	E4		PMC_ACPR ESENT	efineo			define	d
LPE_I2S2_DATAOU T	BK40	SW97		LPE_I2S2_ DATAOUT			, aed	Ulur	
ISH_GPIO[9]/ ISH_SPI_MISO/ I2S5_FS	BK8	E20	ed unde	ISH_GPIO[9]	ISH_SPI _MISO	I2S5_FS	undefine		
SD2_CLK	BL11	SE19	<u> </u>	SD2_CLK		istine			
SD3_D[3]	BL15	SE32		SD3_D[3]		NO.			- (
SD3_CLK	BL17	SE31		SD3_CLK	. red				4 110
SPI1_MISO	BL19	SE60		SPI1_MIS O	defin.			defin	e.
LPC_CLKRUN_N/ UART0_DATAOUT/ SPI2_CLK	BL21	SE46		LPC_CLKR UN_N	UARTO_ DATAOU T		SPI2_CLK	d um	
FST_SPI_D[3]	BL25	SW3	red une	FST_SPI_ D[3]			y nuge,		
UART2_CTS_N	BL27	SW22		UART2_CT S_N	4	undefine			. 4
PMC_SLP_S0IX_N	BL3	E3		PMC_SLP_ S0IX_N	ndefined			Aefi	veq n
I2C6_DATA/ SD3_WP	BL33	SW49		I2C6_DAT A	SD3_WP		nije	sq nur	
I2C2_CLK	BL35	SW66	900	I2C2_CLK			"luge,		
UARTO_DATAOUT/ SPI3_CLK	BL37	SW79	ine		SPI3_CL K	UARTO_DA TAOUT	0.0		
UARTO_DATAOUT/ SPI3_CLK Datasheet	indefined	y Un.		ndefined l	define	dunas			ined '
Datasheet				defined	inc			ned undef	51
			ed u	Ur.			, under		



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defill			76	fined un.				unoc	
Table 35.	Multiple	xed Fun	ctions -	T4 SoC (S	heet 6 of	11)	inge,	_	_
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
LPE_I2S2_DATAIN	BL39	SW94		LPE_I2S2_ DATAIN	6	ino.			"Inde
MMC1_D[0]	BM12	SE17		MMC1_D[0	efine			defil	80
MMC1_D[2]	BM14	SE20		MMC1_D[2				June	
ISH_GPIO[7]/ I2S4_DATAIN	BM2	E16	4 und	ISH_GPIO[7]		I2S4_DATA IN	ndefine		
LPC_CLKOUT[1]/ ISH_GPIO[11]/ ISH_UART_DATAIN	BM20	SE49	C	LPC_CLKO UT[1]	ISH_GPI O[11]	16 fined	ISH_UART _DATAIN		
LPC_SERIRQ/ SPI2_CS[0]_N	BM24	SE79		LPC_SERIR Q	::ned	Unos	SPI2_CS[0]_N		dunde
LPE_I2S0_DATAOU	BM32	SW30		LPE_I2S0_ DATAOUT	defill			ie fi	New .
SPI3_CS[0]_N	BM38	SW76		Sineo		SPI3_CS[0]_N		ed unac	
ISH_GPIO[3]/ I2S3_DATAIN	BM4	E15	-d un	ISH_GPIO[3]		I2S3_DATA IN	indefill		
PMC_SUSCLK[0]	BM6	E6 eff	W.C.	PMC_SUSC LK[0]		adefine	3		
ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	BM8	E26		ISH_I2C1_ DATA	ISH_SPI _MOSI	I2S5_DATA OUT			ined unc
SD2_CMD	BN11	SE22		SD2_CMD				"uge	
MMC1_CLK	BN15	SE16		MMC1_CLK				69 0.	
SPI1_CLK FST_SPI_D[0]	BN19 BN25	SE62 SW1	ed ur	SPI1_CLK FST_SPI_ D[0]			4 undefil		
ISH_I2C1_CLK/ ISH_SPI_CLK/ I2S5_DATAIN	BN3	E17de		ISH_I2C1_ CLK	ISH_SPI _CLK	I2S5_DATA IN	30		
NFC_I2C_DATA	BN33	SW51		NFC_I2C_ DATA	4efine				sined un
SPI3_MISO	BN37	SW81		'sed'	SPI3_MI SO			a und	
ISH_GPIO[1]/ I2S3_FS	BN5	E18	. 1	ISH_GPIO[1]		I2S3_FS	Jefi	heo	
SD2_D[3]_CD_N	BP12	SE15	fined	SD2_D[3] _CD_N			ed nue		
MMC1_D[6]	BP14	SE63		MMC1_D[6		indefin			
52 tined undefined	undefine			undefined	undefin	ed	a	Data	sheet
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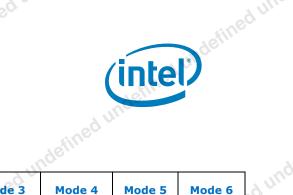


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Physical Inter	faces			10	ille		4	(Inte	リ
eined un.				ned undef				infeiti.	
nden			96,				lefined'		
Table 35. GPIO Pin Name	Package	GPIO	Mode 0	T4 SoC (S	Sheet 7 of Mode 2	f 11) Mode 3	Mode 4	Mode 5	Mode
	Ball #	# CE30	indue 0		1.1046 2	46 June 3	- Inde 4	- Tode J	Mode
SD3_D[1] USB_OC[0]_N	BP16 BP22	SE30 SE80	<u> </u>	SD3_D[1] USB_OC[0	SQ ni				unde
	DI 22	5200	<u></u>]_N	ine			eine	
FST_SPI_CLK	BP24	SW2		FST_SPI_C LK				udell	
LPE_I2S1_DATAOU	BP28	SW34		LPE_I2S1_		1	1,760	n.	
Ţ	BDC 6	011165	unde	DATAOUT		1	defill		
I2C1_CLK GPIO_SW93	BP36 BP38	SW63 SW93	0	I2C1_CLK		201			
ISH_GPIO[5]/	BP38	E19	 	ISH_GPIO[_	I2S4_FS	+	+	1
I2S4_FS	eq u			5]	. 0	NO.			50.
PMC_PLT_CLK[0]/ ISH_GPIO[10]/	BP8	SE0		PMC_PLT_ CLK[0]	ISH_GPI O[10]	ISH_UART_ DATAOUT			ad un.
ISH_UART_DATAO UT				ind	,			defin	
SD2_D[1]	BR11	SE18	+	SD2_D[1]		+	- 2	1000	
MMC1_D[4]	BR13	SE67	200	MMC1_D[4		†	- ine		†
SD3_CMD	BR15	SE34	Sq 01.	SD3_CMD			anor		
SD3_CMD SPI1_CS[1]_N	BR15	SE34 SE66	 	SPI1_CS[1	+	*inec	<u> </u>	+	1
	AV	lu-]_N		"uger.			
LPC_AD[1]/ ISH_GPIO[13]/ ISH_UART_RTS_N	BR19	SE52		LPC_AD[1]	ISH_GPI O[13]		ISH_UART _RTS_N	21.72	ed un
FST_SPI_CS[1]_N	BR23	SW4		FST_SPI_C S[1]_N				Junden	
UART1_RTS_N	BR25	SW15	a und	UART1_RT S_N			ndefine		
UART1_CTS_N	BR27	SW18	Ven.				d. William		+
		nuge.		UART1_CT S_N		defill			
ISH_GPIO[0]/ I2S3_CLK	BR3	E21		ISH_GPIO[0]	sined	I2S3_CLK			ed u
LPE_I2S1_CLK	BR30	SW32		LPE_I2S1_ CLK	uge.			4efi	
I2C5_DATA	BR33	SW45	 	CLIC		+		4000	
unde				I2C5_DAT A			Nije.	C.	
I2C1_DATA	BR35	SW60	eg ur			+	" nuge,	1	
		Aei	IUS	I2C1_DAT A		2013	50		
	<u>ــــــــــــــــــــــــــــــــــــ</u>	Union	1			I woell			
Datasheet	defined			A ndefined i		'g n.			ined i
Datachast	W.				inger.			ned undef	53
Datasileet								ed num	JJ
16.1.									
Datasheet				geil.			196	, no	



GPIO Pin Name ISH_GPIO[12]/ ISH_UART_CTS_N	Multiplex Package Ball #			ined und	afine c		Phy	sical Interf	aces
Table 35. I GPIO Pin Name ISH_GPIO[12]/ ISH_UART_CTS_N	Multiplex Package Ball #	ced Fun		ined und					
Table 35. I GPIO Pin Name ISH_GPIO[12]/ ISH_UART_CTS_N	Multiplex Package Ball #	ced Fun		ined				geill	
ISH_GPIO[12]/ ISH_UART_CTS_N	Package Ball #	GPIO					60	Ullia	
ISH_GPIO[12]/ ISH_UART_CTS_N	Package Ball #	GPIO	ictions -				define		
ISH_GPIO[12]/ ISH_UART_CTS_N	- 4		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	- 00	SW75			ISH_GPI	ISH_UART_			96
PUTE (TRRECTO)	DD20	CIMOO		DOTE OU	O[12]	CTS_N			90,011,0
N [BR39	SW90		PCIE_CLK REQ[0]_N	e,,,			niisi	
SD2_D[0]	BT10	SE25		SD2_D[0]				Inde	
MMC1_D[7]	BT14	SE68	60	MMC1_D[7			Sine		
SPI1_CS[0]_N	BT18	SE61	ed un	SPI1_CS[0]_N		2	nuge		
ISH_GPIO[2]/ I2S3_DATAOUT	BT2	E24	•	ISH_GPIO[2]		I2S3_DATA OUT	•		
	BT22	SE85		SD3_1P8_ EN	red	71.40			-d und
UART1_DATAIN/ UART0_DATAIN	BT26	SW16		UART1_DA	UARTO_ DATAIN			indefi	.00
I2C0_CLK	BT36	SW65		I2C0_CLK			09	,	
	BT4	E22	ed un	ISH_GPIO[4]		I2S4_CLK	nugetii		
	BT40	SW95	0		SD3_WP	sine.	<u> </u>		
_	BU11	SE21		SD2_D[2]		96,			
	BU15	SE65		MMC1_D[5	.: ned	, ville			dun
SD3_CD_N	BU17	SE81		SD3_CD_N	deill				Wes
LPC_AD[0]/ ISH_GPIO[12]/ ISH_UART_CTS_N	BU19	SE47		LPC_AD[0]	ISH_GPI O[12]		ISH_UART _CTS_N	ed nuge	
USB_OC[1]_N	BU21	SE75	ed ur	USB_OC[1]_N			undein		
SD3_PWREN_N	BU23	SE78		SD3_PWR EN_N		4efine	,		
FST_SPI_CS[0]_N	BU25	SW6		FST_SPI_C S[0]_N	_0	d und			d un
	BU27	SW20		UART1_DA TAOUT	UARTO_ DATAOU T			inde	livec
	,							A V	-
UARTO_DATAOUT	BU30	SW33		LPE_I2S0_ DATAIN				Vec.	



defined undefined undefineed Table 35. Multiplexed Functions - T4 SoC (Sheet 9 of 11)

	rfaces			26				(Inte	
ined by				ned undef				Uselli.	
defil.			130	Ver			ined "		
Table 35.	Multiple	xed Fur	nctions -	T4 SoC (S	Sheet 9 of	F 11)	defille		
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
I2C0_DATA	BU35	SW61		I2C0_DAT	ined un	20			unde
GPIO_SW78	BU37	SW78		09				Stills	
PCIE_CLKREQ[1]_ N	BU39	SW91		PCIE_CLK REQ[1]_N			ed	unde	
PWM[1]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	BU5	SE1	d unde	PWM[1]	ISH_GPI O[10]	ISH_UART_ DATAOUT	Indefill		
FST_SPI_CS[2]_N	BV24	SW7		FST_SPI_C S[2]_N	. 13	ndefill			ò
LPE_I2S1_FRM	BV28	SW36		LPE_I2S1_ FRM	efineo			ei O	d un
2C3_CLK	BV34	SW67		I2C3_CLK				gen	
MMC1_RESET_N/ SPI3_CS[1]_N	BV38	SW80		liveo	MMC1_R ESET_N	SPI3_CS[1]_N	ined	n,	
PWM[0]	BV4	SE5	4 nuch	PWM[0]			"uge,		
DDI2_HPD	C21	N68	Sa	DDI2_HPD		65	n,		
GPIO_CAMERASB0 7	C27	N54		GPIO_CAM ERASB07		define			
GPIO_CAMERASB0 1	C30	N56		GPIO_CAM ERASB04	ined!	nu.			A Ur
SVID_ALERT_N	C33	N38		SVID_ALE RT_N	deill			defin	
GPIO_SUS5/ PMC_SUSCLK[1]	C35	N20	À	PMC_SUSC LK[1]			*100	g ni.	
GPIO_SUS3/ ITAG2_TDI	C37	N17	leg nur	JTAG2_TDI GPIO CAM			nuger.		
GPIO_CAMERASB1)	D26	N50		ERASB10		istine'			
SVID_DATA	D32	N33	SVID_D ATA		60	nuge			
GPIO_SUS6/ PMC_SUSCLK[2]	D36	N25		PMC_SUSC LK[2]	define			ne ^{fi}	Ueo
DDI1_HPD	E25	N64		DDI1_HPD				June	
GPIO_CAMERASB0	E27	N49	.0	GPIO_CAM ERASB06			defin	e	
GPIO_CAMERASB0 2	E30	N46	ined n.	GPIO_CAM ERASB02			d undefil		
ITAG_TDI	E33	N41	1	JTAG_TDI		i efili			



	A UIT	ge,			. 4	ndefine			aefi
intel	®*			fined und	efined u		Phy	sical Inter	aces
undefil			296				4efined	unde	
Table 35. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	T4 SoC (S	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
JTAG_TRST_N	E35	N30		JTAG_TRS T_N	4 /	luge,			nde
GPIO_SUS0	E37	N15		1_1	fineo				Sq n.
DDI0_VDDEN	F22	N72		DDI0_VDD EN	8			undefin	
GPIO_CAMERASB1	F28	N55	500	GPIO_CAM ERASB11			iefine	d .	
SVID_CLK	F32	N40	900	SVID_CLK			unde		
JTAG_TCK	F34	N31		JTAG_TCK		ined			
GPIO_SUS8	F36	N23		GPIO_SUS 8		nuge,,			.,,,,
GPIO_CAMERASB0 5	G27	N45		GPIO_CAM ERASB05	refined			٠	led mi.
JTAG_PRDY_N	G33	N37		JTAG_PRD Y_N	O			, nuger	
GPIO_SUS4/ JTAG2_TDO	G37	N22		JTAG2_TD O			18110	30	
DDI1_VDDEN/ MDSI_DDC_DATA	H22	N69	ued n.	DDI1_VDD EN	MDSI_D DC_DAT A	00	d uno		
PROCHOT_N	H32	N32		PROCHOT_ N		undeilli			ó
JTAG_PREQ_N	H34	N26		JTAG_PRE Q_N	define				ned ul
GPIO_DFX4	H38	N5		40				"uge	
DDI1_BKLTEN/ MDSI_DDC_CLK	J21	N70		DDI1_BKL TEN	MDSI_D DC_CLK			ed	
GPIO_CAMERASB0 9	J27	N52	ned ur	GPIO_CAM ERASB09			4 nuge.		
GPIO_CAMERASB0 0	J30	N48		GPIO_CAM ERASB00		defin			
JTAG_TDO	J33	N39		JTAG_TDO		Julia			
GPIO_SUS9	J35	N27		GPIO_SUS 9	define				tined by
DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	K20	N63		DDI1_BKL TCTL		MDSI_A_T E	MDSI_C_T E	sed und	
DDI0_BKLTCTL	K22	N65	-40	DDI0_BKL TCTL			indef		
DDI0_HPD	K26	N61	files.	DDI0_HPD			ed		
GPIO_CAMERASB0 8	K28	N47		GPIO_CAM ERASB08		Indefil			
56 mile (in)	undefin			ERASB08	undefin			Data	sheet
ined un.			60	nuor			, unde	lived m.	

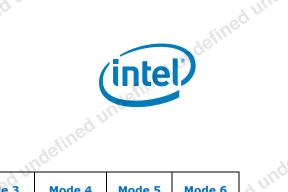


Table 35. Multiplexed Functions - T4 SoC (Sheet 11 of 11)

	Physical Inte	riaces			del				unte	
ned	undefined by Table 35.	Multiple	xed Fur	adefil	ned under		f 11)	ndefined i	Mess	
ndefill	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	GPIO_CAMERASB0	K32	N53		GPIO_CAM ERASB01	ed un	0.0			nuger
	GPIO_SUS10	K34	N16		GPIO_SUS 10				define!	·
	GPIO_SUS7/ PMC_SUSCLK[3]	K36	N18	4	PMC_SUSC LK[3]			ed	und	
ed	GPIO_SUS1/ JTAG2_TCK	K38	N19	4 nuge	JTAG2_TC K			ndefille		
indefill.	DDI0_BKLTEN	L21	N60		DDI0_BKL TEN		stined.			
			12							

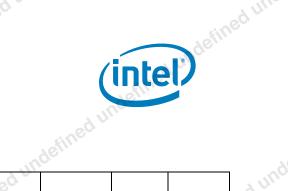
Table 36. Multiplexed Functions - T3 SoC (Sheet 1 of 9)

		 	1			1	1		- 411		7
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	
defined	DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	A10	N71	nuge	DDI0_DD C_CLK	DDI1_DD C_CLK	MDSI_D DC_CLK	indelli.			, un
uno	GPIO_SE79	AA13	SE79			711	define			2	fined
	I2C4_CLK/ DDI1_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	AB17	SW52		I2C4_CLK	DDI1_DD C_CLK	DDI2_D DC_CLK	MDSI_DDC _CLK	ndefi'	led nuo	_
	I2C4_DATA/ DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	AB18	SW46	undefi	I2C4_DA TA	DDI1_DD C_DATA	DDI2_D DC_DATA	MDSI_DDC _DATA	101.		
d undefit.	PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	AB4	SE4		PMC_PLT _CLK[3]	ISH_GPI O[13]	ISH_UAR T_RTS_N	SPI2_CLK			efined u
	PMC_PLT_CLK[4]/ ISH_GPIO[14]/ ISH_I2C0_DATA/ SPI2_MISO	AC3	SE3		PMC_PLT _CLK[4]	ISH_GPI O[14]	ISH_I2C 0_DATA	SPI2_MIS O	indef	lued m.	
213	PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	AC4	SE7	d undef	PMC_PLT _CLK[2]	ISH_GPI O[12]	ISH_UAR T_CTS_N	SPI2_CS[0]_N	Ò		
ed under	PMC_PLT_CLK[5]/ ISH_GPIO[15]/ ISH_I2CO_CLK/ SPI2_MOSI	AE3	SE6		PMC_PLT _CLK[5]	ISH_GPI O[15]	ISH_I2C 0_CLK	SPI2_MOS I		71.	defined
,		ndefi	•	•	-0	definer	•	<u>'</u>	26	fined 3	_
	Datasheet			inde	fined un			d undefin	ed unor	57	
4efil	ver.		es (led n.				9 nuga			A



Idefined undefined undefined Table 36. Multiplexed Functions - T3 SoC (Sheet 2 of 9)

6,11,1			-0					1			- C)
udeili	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	lived nue
	MMC1_RCLK/ MMC1_RESET_N	AE8	SE69		MMC1_R CLK	MMC1_R ESET_N				ed unas	
	PMC_SUSCLK[3]	B12	N18		PMC_SUS CLK[3]				undefil		
-	JTAG2_TDI	B14	N17	indefil	JTAG2_T DI			defined			
undefine	DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	C10	N66		DDI0_DD C_DATA	DDI1_DD C_DATA	MDSI_D DC_DATA	71.17			ined und
	PMC_SUSCLK[2]	C14	N25		PMC_SUS CLK[2]	red un	O			dund	elii.
	JTAG2_TCK	C15	N19		JTAG2_TC K	STILL			adefi	ive.	
	GPIO_N3/ C0_BPM1_TX/ C1_BPM1_TX	C17	N3	indefi	UEO			define	C0_BPM 1_TX	C1_BPM1 _TX	
undefin	DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	C9	N62	0	DDI2_DD C_DATA	DDI1_DD C_DATA	UARTO_D ATAIN	MDSI_DDC _DATA	MDSI_C _TE	.0	defined un
	JTAG2_TDO	D14	N22		JTAG2_T DO	efined				ined on	-
	JTAG2_TMS	D15	N24		JTAG2_T MS				ed unde		
i efil	DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	D8	N63	ed unde	DDI1_BK LTCTL		MDSI_A_ TE	MDSI_C_T E			
d unde	DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E10	N67		DDI2_DD C_CLK	DDI1_DD C_CLK	UARTO_D ATAOUT	MDSI_DDC _CLK	MDSI_A _TE	ed ur	defined
	GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	E16	N4		ined un	90,			C0_BPM 0_TX	4417	
ci	GPIO_N0/ C0_BPM0_TX/ C1_BPM0_TX	E17	N0	ed und	3/11			undefil	CO_BPM O_TX	C1_BPM0 _TX	
ed under	GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F16	N2				indefin	0	C0_BPM 2_TX	C1_BPM2 _TX	defined
	58	undefine			Jefined V	ndefined			Data	asheet	Nuc.
	dundefing			.ini	sefine a			, undef	ined un		
76	inec		e i	ued n.				ad und			

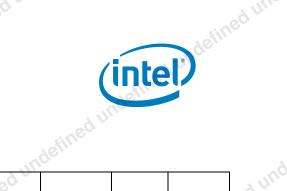


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indefinec							refined n	U	
GPIO Pin	Package Ball #	GPIO#	Mode 0	SoC (She	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Name GPIO_N1/ C0_BPM3_TX/ C1_BPM3_TX	F17	N1		4641	ved nuo			C0_BPM 3_TX	C1_BPM3 _TX
UARTO_DATAIN	V13	SE48	cine	d una	UARTO_D ATAIN		od'	Ingelli	
PMC_SLP_S0IX_N	W4	E3	undeili	PMC_SLP _S0IX_N			define		
UARTO_DATAOUT	Y12	SE46			UARTO_D ATAOUT	stined of	*		
GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	C16	N6		į.	ined und			C0_BPM 3_TX	C1_BPM3 _TX
GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	D16	N8		ed nuge			4	CO_BPM 1_TX	C1_BPM: _TX
ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	D17	N7	undefin				ISH_GPIO[13]	C0_BPM 2_TX	C1_BPM2 _TX
GPIO_SUS9	A13	N27		GPIO_SU S9		lefined.	pr.		
GPIO_SUS0	A14	N15			ined un				ad und
DDI0_VDDEN	A9	N72		DDI0_VD DEN				.ndefi	No.
SD3_CMD	AA10	SE34	Jeff'	SD3_CM D			eine!	30.	
FST_SPI_CS[0]_N	AA12	SW6	d nuc	FST_SPI_ CS[0]_N		-3	nugerr		
LPE_I2S1_FRM	AA14	SW36		LPE_I2S1 _FRM	-4	defined			
LPE_I2SO_DATAOU T	AA15	SW30		LPE_I2S0 _DATAOU T	efined u			۵	ined un
LPE_I2SO_CLK	AA16	SW31		LPE_I2S0 _CLK				dunde	
I2C2_CLK	AA17	SW66	4 under	I2C2_CLK			ndefini		
ISH_I2C1_CLK/ ISH_SPI_CLK/ I2S5_DATAIN	AA3	E17		ISH_I2C1 _CLK	ISH_SPI_ CLK	I2S5_DA TAIN			
.1	ndefined				defined i), <u> </u>			sined u
Datasheet				efined un			4 undefin	ed unde	59
Butasileet			d und	3*			indefil		



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GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	ilUe
ISH_GPIO[9]/ ISH_SPI_MISO/ I2S5_FS	AA4	E20		ISH_GPI O[9]	ISH_SPI_ MISO	I2S5_FS		Viin .	led nuo	
ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	AA5	E26	10/11/	ISH_I2C1 _DATA	ISH_SPI_ MOSI	I2S5_DA TAOUT	ined	unde		
MMC1_CMD	AA6	SE23	nuo	MMC1_C MD			indelli			
MMC1_D[7]	AA7	SE68		MMC1_D[7]		refined				ei V
MMC1_D[0]	AA8	SE17		MMC1_D[0]	ed un	O.			und	3//,
SD3_PWREN_N	AA9	SE78		SD3_PWR EN_N	Stille			461	ueo.	
SD3_D[2]	AB10	SE33	e i	SD3_D[2]				o nuc		
FST_SPI_D[0]	AB11	SW1	d nuger	FST_SPI_ D[0]			undefine			
FST_SPI_CLK	AB12	SW2		FST_SPI_ CLK		"ined)			
UART2_DATAOUT	AB13	SW21		UART2_D ATAOUT	ad v	hoe.			, uni	Je f
LPE_I2S1_CLK	AB14	SW32		LPE_I2S1 _CLK	efine			76	lined	
LPE_I2SO_DATAIN	AB15	SW33	20	LPE_I2S0 _DATAIN			4:10	ed unu]
I2C5_CLK	AB16	SW50	ed unac	I2C5_CLK			unden			
LPE_I2S2_CLK	AB19	SW92		LPE_I2S2 _CLK		ndefine				76
ISH_GPIO[0]/ I2S3_CLK	AB2	E21		ISH_GPI O[0]	Fined	I2S3_CL K			sed un	VO.
PCIE_CLKREQ[0]_ N	AB20	SW90		PCIE_CLK REQ[0]_ N	O.S.			4 und		
ISH_GPIO[2]/ I2S3_DATAOUT	AB3	E24	, und	ISH_GPI O[2]		I2S3_DA TAOUT	adefil	67		
SD2_CMD	AB5	SE22	Jea .	SD2_CM D			ed un			
MMC1_D[2]	AB6	SE20		MMC1_D["ugetit	1			nd'
60 andefined	undefined			Jefined U	ndefined	,	4.5	Data	sheet	, CO
Hined u.			red nu				ad undef			

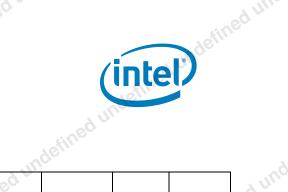


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ined ur.				d undefin			110	Uselli	
Table 36.	Multiplexe	nd Funct	ge,			ı	defined "		
Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
MMC1_D[6]	AB7	SE63		MMC1_D[6]	red rivo.				d unde
SD3_1P8_EN	AB8	SE85		SD3_1P8 _EN				ndefine	
SD3_D[1]	AB9	SE30	define	SD3_D[1			fined		
ISH_GPIO[7]/ I2S4_DATAIN	AC1	E16	VIII.	ISH_GPI O[7]		I2S4_DA TAIN	Vqe.		
SD3_D[0]	AC10	SE35		SD3_D[0]	م	efines			
FST_SPI_D[1]	AC11	SW5		FST_SPI_ D[1]	wed m.				ed und
UART2_RTS_N	AC12	SW19		UART2_R TS_N			Δ.	undefir	
UART1_CTS_N	AC13	SW18	undefir	UART1_C TS_N			ndefined		
UART1_DATAOUT/ UART0_DATAOUT	AC14	SW20	3	UART1_D ATAOUT	UARTO_D ATAOUT	efined	70.0		
NFC_I2C_DATA	AC15	SW51		NFC_I2C _DATA	red un				4 un
NFC_I2C_CLK	AC16	SW54		NFC_I2C _CLK				indefi'	Nev.
I2C2_DATA	AC17	SW62	indefi	I2C2_DA TA			define		
GPIO_SW78	AC18	SW78	, D.	1.0	+	eined.	nu nu		
LPE_I2S2_FRM	AC19	SW96		LPE_I2S2 _FRM	-A U	ige _{III} .			
ISH_GPIO[4]/ I2S4_CLK	AC2	E22		ISH_GPI O[4]	Stillen	I2S4_CL K		105	lued n
GPIO_SW93	AC20	SW93	- K	ined m.				d unos	
MMC1_D[3]	AC6	SE26	ed nuge	MMC1_D[3]			nugetin		
MMC1_D[4]	AC7	SE67		MMC1_D[Jefine!			
Datasheet	defined	0	_	4]	efined i	Inc			stined u
Datasheet	Inc			ed un	96,		dundefin	unde	61
d under.			nde	fine			16. J.	'eo	
		4	led m.				4 unos		



intel	ed unc			ed undef	und	e.			ndef
(intel				i est	iuso,		Phys	sical Inter	faces
100 UIV	I			4 huge				indefill.	
			iefin				ined		
Table 36.	Multiplex	ed Funct					ndefill		
Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
MMC1_D[5]	AC8	SE65		MMC1_D[5]	ined un				ed nuci
SD3_CLK	AC9	SE31		SD3_CLK				46811	
SD3_D[3]	AD10	SE32		SD3_D[3				UNG	
UART2_CTS_N	AD12	SW22	undefi	UART2_C TS_N			indefine		
UART1_DATAIN/ UART0_DATAIN	AD14	SW16		UART1_D ATAIN	UARTO_D ATAIN	defined			
I2C6_DATA/ SD3_WP	AD16	SW49		I2C6_DA TA	SD3_WP	P			ned uno
MMC1_RESET_N	AD18	SW80		ed und	MMC1_R ESET_N			undef	
PWM[1]/ ISH_GPIO[10]/ ISH_UART_DATAO UT	AD2	SE1	d under	PWM[1]	ISH_GPI O[10]	ISH_UAR T_DATAO UT	undefine		
SD3_WP	AD20	SW95			SD3_WP	ndefine			
PWM[0]	AD3	SE5		PWM[0]	ed '				יוט ו
SD2_D[0]	AD4	SE25		SD2_D[0	etino				ineo
SD2_CLK	AD5	SE19		SD2_CLK				11196	
SD2_D[3]_CD_N	AD6	SE15	76	SD2_D[3			27/2	69	
MMC1_CLK	AD8	SE16	sq nuc]_CD_N MMC1_CL			1 nuger.		
UART2_DATAIN	AE12	SW17		K UART2_D ATAIN	2	undefine			
UART1_RTS_N	AE13	SW15		UART1_R TS_N	defined			6.	efined W
I2C6_CLK/NMI_N	AE16	SW53	2	I2C6_CLK	NMI_N		£ N	ned une	
I2C5_DATA	AE17	SW45	ned uno	I2C5_DA TA			d under		
UARTO_DATAIN	AE18	SW77			UARTO_D ATAIN	indefin			
	ndefine!		•	•	lefined		•	•	ined!
62 ined undefined	n.			defined u	inois			Data	asheet
ed uno			, un	Jer.				ine	



adefined undefined undefineu Table 36. Multiplexed Functions - T3 SoC (Sheet 7 of 9)

	Physical Inter	faces			717			(inte	17
	red nue				d undefin				Or Elly	
	ndefille			define				ined u		
sd L	Table 36.	Multiplexe	ed Funct	ions - T3	SoC (She	eet 7 of 9)		gel.		
	Table 36. GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	SD2_D[1]	AE4	SE18		SD2_D[1	ved m				d unas
	SD2_D[2]	AE5	SE21		SD2_D[2				ndefine	
	SD3_CD_N	AE9	SE81	define	SD3_CD_ N			stined.		
Ò	GPIO_CAMERASB1	B10	N50		GPIO_CA MERASB1 0		ined u	196		
	DDI0_BKLTCTL	B8 UIT	N65		DDI0_BK LTCTL	und	81111			.00
	GPIO_CAMERASB1	C11	N55		GPIO_CA MERASB1 1	ineo			defin	Sqriii
	JTAG_TDI	C12	N41		JTAG_TDI			۸	nuc	
6	GPIO_SUS8	C13	N23	undefin	GPIO_SU S8			adefined		
	DDI0_BKLTEN	C8	N60		DDI0_BK LTEN		stined !			
	GPIO_CAMERASB0 9	D10 climed un	N52		GPIO_CA MERASB0 9	ined un	96.			od uni
	GPIO_CAMERASB0 8	D11	N47		GPIO_CA MERASB0 8				undefi	
0	DDI0_HPD	D9	N61	undefi	DDI0_HP D			define		
10	SVID_ALERT_N	E12	N38	<u> </u>	SVID_AL ERT_N		sined	Oil		
	JTAG_TRST_N	E13	N30		JTAG_TR ST_N	4 11	19e,			
	JTAG_TCK	E14	N31		JTAG_TC K	efinec			e e	ued n.
	DDI2_HPD	E9	N68		DDI2_HP D				4 nuge	
	SVID_CLK	F11	N40	, unde	SVID_CL K			adefin	3	
10	SVID_DATA	F12	N33	SVID_D ATA			eine e	1011		
	JTAG_TDO	F13	N39		JTAG_TD O		uger.			
		ndefill.				defined				eined u
	Datasheet				fined un			d undefil	ed unde	63
	Datasheet			inde					le.	
				ed				4 nuc		



adefined undefined undefineu Table 36. Multiplexed Functions - T3 SoC (Sheet 8 of 9)

(Intel				defi	iu _c		Phys	sical Inter	faces
defined			2113	ed undefi			6.0	nuge.	
Table 36.	Multiplexe	ed Functi	ions - T3	SoC (She	et 8 of 9))	ndefine		
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
JTAG_TMS	F14	N34		JTAG_TM S	ined vin				ed unde
GPIO_DFX4	F18	N5		od nude				undefil	
PROCHOT_N	F9	N32	adefil	PROCHOT _N			iefine		
LPE_I2S2_DATAIN	U17	SW94	1011	LPE_I2S2 _DATAIN		ed	nuge		
PMC_SUSPWRDNA CK	V12	SE83		PMC_SUS PWRDNA CK	-d ur	defill			ind
LPE_I2S2_DATAOU T	V18	SW97		LPE_I2S2 _DATAOU T	stine			adefi	ueq n
PMC_SUS_STAT_N	V5	E2	10 ^k	PMC_SUS _STAT_N			eine	of the	
I2C1_DATA	W15	SW60	d nuor	I2C1_DA		eined.	nugein		
I2C1_CLK	W16	SW63		I2C1_CLK	ofined u	1081			ined un
PMC_PWRBTN_N	W3	E8		PMC_PW RBTN_N				dunde	
ISH_GPIO[3]/ I2S3_DATAIN	Y1	E15	Inde	ISH_GPI O[3]		I2S3_DA TAIN	defin		
LPE_I2S1_DATAIN	Y13	SW37	80.	LPE_I2S1 _DATAIN		fine	dun		
LPE_I2S1_DATAOU T	Y14	SW34		LPE_I2S1 _DATAOU T	, ed'	Iuqe,			م ن
LPE_I2S0_FRM	Y16	SW35		LPE_I2S0 _FRM	define			200	HINEO
I2C0_CLK	Y17	SW65	red und	I2C0_CLK			ed undefi	ued m.	
		undefil				defin	0		
	defined				fined	Ulli			sheet
64 undefined	nuc			defined u	uge.			Data	sheet
ined una			ed uni	Aer.			dunder	ine	
		e d	in o				29		

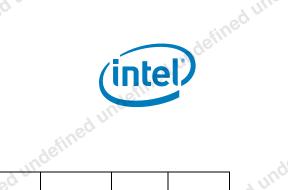


Table 36. Multiplexed Functions - T3 SoC (Sheet 9 of 9)

deill	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	ued un
	I2C0_DATA	Y18	SW61		I2C0_DA TA	led		27	ndefine	d und	
-9	ISH_GPIO[1]/ I2S3_FS	Y2	E18	ingelii.	ISH_GPI O[1]		I2S3_FS	define			
definec	PMC_WAKE_N	Y3	E10		PMC_WA KE_N		sined u				ed u
	PMC_SUSCLK[0]	Y4 JIM	E6		PMC_SUS CLK[0]	ned und	Ø.			d under	Inc
	PMC_PLTRST_N	Y5	E5		PMC_PLT RST_N				indefin	3	
9	MMC1_D[1]	Y8	SE24	adefil	MMC1_D[1]			lefined			
odefines	USB_OC[0]_N	Y9	SE80		USB_OC[1]_N		ned "	inoe			-9,
	Table 37.	Multiplexe	ed Functi	ions - T3	SoC (She	et 1 of 9)	Jeilli			unds	finec

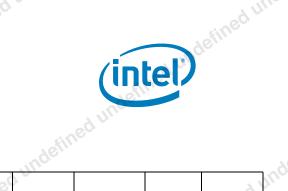
Table 37. Multiplexed Functions - T3 SoC (Sheet 1 of 9)

	ACC.				CILI					
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
undefined un	DDI0_DDC_CLK/ DDI1_DDC_CLK/ MDSI_DDC_CLK	A10	N71	elli	DDI0_DD C_CLK	DDI1_DD C_CLK	MDSI_D DC_CLK	fine		
I nuger,	GPIO_SE79	AA13	SE79			defil	Jeo.			Fine
	I2C4_CLK/ DDI1_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	AB17	SW52		I2C4_CLK	DDI1_DD C_CLK	DDI2_D DC_CLK	MDSI_DDC _CLK	efined	nuge.
رم نا	I2C4_DATA/ DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	AB18	SW46	defined	I2C4_DA TA	DDI1_DD C_DATA	DDI2_D DC_DATA	MDSI_DDC _DATA	0	
id undefines	PMC_PLT_CLK[3]/ ISH_GPIO[13]/ ISH_UART_RTS_N/ SPI2_CLK	AB4	SE4		PMC_PLT _CLK[3]	ISH_GPI O[13]	ISH_UAR T_RTS_N	SPI2_CLK		1efin
	undef	Inec			defin	ed u.			fined	uno
	Datasheet				June			efined u	65	
sined !	Inde.		90	indefiner			71.	defined		
16/11/			anov.				29 01.			



adefined undefined undefineu Table 37. Multiplexed Functions - T3 SoC (Sheet 2 of 9)

(intel)				defines			Physical I	nterfaces	
Table 37. Mult			fined u	ndefinec		A	ined una		
Table 37. Mult	iplexed Fu	nctions -	- T3 SoC	(Sheet 2	of 9)	undef		T	
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode
PMC_PLT_CLK[4]/ ISH_GPIO[14]/ ISH_I2C0_DATA/ SPI2_MISO	AC3	SE3		PMC_PLT _CLK[4]	ISH_GPI O[14]	ISH_I2C 0_DATA	SPI2_MIS O	efined) (no
PMC_PLT_CLK[2]/ ISH_GPIO[12]/ ISH_UART_CTS_N/ SPI2_CS[0]_N	AC4	SE7	efined	PMC_PLT _CLK[2]	ISH_GPI O[12]	ISH_UAR T_CTS_N	SPI2_CS[0]_N		
PMC_PLT_CLK[5]/ ISH_GPIO[15]/ ISH_I2C0_CLK/ SPI2_MOSI	AE3	SE6		PMC_PLT _CLK[5]	ISH_GPI O[15]	ISH_I2C 0_CLK	SPI2_MOS I		dei
MMC1_RCLK/ MMC1_RESET_N	AE8	SE69		MMC1_R CLK	MMC1_R ESET_N			ined.	
PMC_SUSCLK[3]	B12	N18	6.0	PMC_SUS CLK[3]			nu .	defille	
JTAG2_TDI	B14	N17	delines	JTAG2_T DI		29	efined		
DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	C10	N66		DDI0_DD C_DATA	DDI1_DD C_DATA	MDSI_D DC_DATA			
PMC_SUSCLK[2]	C14	N25		PMC_SUS CLK[2]	ed une				unde
JTAG2_TCK	C15	N19	4	JTAG2_TC K				adefine)·
GPIO_N3/ CO_BPM1_TX/ C1_BPM1_TX	C17	N3	ndefine				Jefined D	C0_BPM 1_TX	C1_BF _TX
CO_BPM1_TX/ C1_BPM1_TX DDI2_DDC_DATA/ DDI1_DDC_DATA/ UARTO_DATAIN/ MDSI_DDC_DATA/ MDSI_C_TE	c9	N62		DDI2_DD C_DATA	DDI1_DD C_DATA	UARTO_D ATAIN	MDSI_DDC _DATA	MDSI_C _TE	ind
JTAG2_TDO	D14	N22		JTAG2_T DO				<i>Aefine</i>	Ó
JTAG2_TMS	D15	N24	iefine	JTAG2_T MS			"ned"	3/10	
DDI1_BKLTCTL/ MDSI_A_TE/ MDSI_C_TE	D8	N63	Jugg	DDI1_BK LTCTL		MDSI_A_ TE	MDSI_C_T E		
	fined und				ned und	efii			ed un
MDSI_C_TE				ed Undef			6-	Datasheet	
d unac		do	undefili			. 1	Indefined		

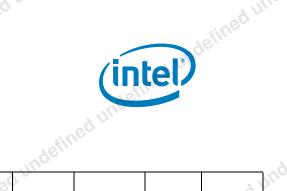


ger		indefine				defined				Jefined um
	Physical Interfaces				lefined u	ndefined		(in	tel	26.
idefined undef	ined L		اکی ا	lued nu				led nuger		
ined un.	Table 37. Mult	iplexed Fu	nctions -	T3 SoC	(Sheet 3	of 9)	indefil	, v		- 6
nder.	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	DDI2_DDC_CLK/ DDI1_DDC_CLK/ UART0_DATAOUT/ MDSI_DDC_CLK/ MDSI_A_TE	E10	N67	ed un	DDI2_DD C_CLK	DDI1_DD C_CLK	UARTO_D ATAOUT	MDSI_DDC _CLK	MDSI_A _TE	
ed unde	GPIO_N4/ C0_BPM0_TX/ C1_BPM0_TX	E16	N4	line			ndefi	ueg	C0_BPM 0_TX	C1_BPM0 _TX
Indefine	GPIO_N0/ C0_BPM0_TX/ C1_BPM0_TX	E17	N0			define	9 77		C0_BPM 0_TX	C1_BPM0 _TX
	GPIO_N2/ C0_BPM2_TX/ C1_BPM2_TX	F16	N2		stined	nuc			C0_BPM 2_TX	C1_BPM2 _TX
	GPIO_N1/ CO_BPM3_TX/ C1_BPM3_TX	F17	N1	ined u	196.			ed und	C0_BPM 3_TX	C1_BPM3 _TX
ined une	UARTO_DATAIN	V13	SE48	3		UARTO_D ATAIN	unde	III		
nuge,,	PMC_SLP_S0IX_N	W4	E3		PMC_SLP _S0IX_N	iefil?	s _o			ined u
	UARTO_DATAOUT	Y12	SE46		0	UARTO_D ATAOUT				hugell.
	GPIO_N6/ C0_BPM3_TX/ C1_BPM3_TX	C16	N6	-97	Indefine			ind	C0_BPM 3_TX	C1_BPM3 _TX
ed un	GPIO_N8/ C0_BPM1_TX/ C1_BPM1_TX	D16	N8	efines			290	tined t	C0_BPM 1_TX	C1_BPM1 _TX
undefinedu	ISH_GPIO[13]/ C0_BPM2_TX/ C1_BPM2_TX	D17	N7			Aefi'	ned un	ISH_GPIO[13]	C0_BPM 2_TX	C1_BPM2 _TX
	GPIO_SUS9	A13	N27		GPIO_SU S9	dune			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	nuge.
	GPIO_SUS0	A14	N15	2	nugetill			200	defined	
	DDI0_VDDEN	A9	N72	defined	DDI0_VD DEN			sined b		
isfined "	SD3_CMD	AA10	SE34		SD3_CM D		od nuc			
d undefined u	FST_SPI_CS[0]_N	AA12	SW6		FST_SPI_ CS[0]_N	adef	lues			lefined.
	ndefi				18fil	led m.				g nuger.
I	Datasheet				d undefin			defined u	67	
ofined "			red u	iuger.			a Ur	define		



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Name	(intel)				defines			Physical 1	nterfaces	
Package Pin Package Package	defined			fined u				sed und		
LPE_IZS1_FRM	Table 37. Mul	tiplexed Fu				of 9)				
FRM	GPIO Pin Name			Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Мо
T	LPE_I2S1_FRM	AA14	SW36						ined "	UOL
CLK		AA15	SW30	sined i	_DATAOU			ed und	Sim	
ISH_IZC1_CLK ISH_IZC1_CLK ISH_IZC1_ISH_SPI_L ISH_SPI_L ISH_SPI_L ISH_SPI_L ISH_SPI_L ISH_SPI_L ISH_SPI_L ISS_DATAIN ISH_GPIO[9] ISH_SPI_MISO ISH_SPI_MISO ISH_SPI_MISO ISH_SPI_MISO ISH_IZC1_DATA ISH_SPI_MOSI ISH_IZC1_DATA ISH_SPI_MOSI ISH_IZC3_DATAOUT ISH_SPI_MOSI ISH_IZC3_DATAIN ISH_	LPE_I2SO_CLK	AA16	SW31	e.			unde	line		
SH_SPL_CLK/ 12S5_DATAIN	I2C2_CLK	AA17	SW66		I2C2_CLK	defil	leg .			
SH_ SPI_MISO/ I2S5_FS	ISH_SPI_CLK/	AA3	E17						ned	und
ISH_SPI_MOSI/ IZSS_DATAOUT	ISH_SPI_MISO/	AA4	E20	eined			I2S5_FS	ed un	GELL	
MMC1_D[7] AA7 SE68 MMC1_D[T] MMC1_D[0] AA8 SE17 MMC1_D[T] SD3_PWREN_N AA9 SE78 SD3_PWR EN_N SD3_D[2] AB10 SE33 SD3_D[2] FST_SPI_D[0] AB11 SW1 FST_SPI_D[0] FST_SPI_CLK AB12 SW2 FST_SPI_CLK UART2_DATAOUT AB13 SW21 UART2_D ATAOUT LPE_I2S1_CLK AB14 SW32 LPE_I2S1_CLK LPE_I2S0_DATAIN AB15 SW33 LPE_I2S0_DATAIN I2C5_CLK AB16 SW50 I2C5_CLK	ISH_SPI_MOSI/	AA5	E26	9err				efine		
7] MMC1_D[0] AA8 SE17 MMC1_D[0]	MMC1_CMD	AA6	SE23			16	Weo.			
MMC1_D[0] AA8 SE17 MMC1_D[0] SD3_PWREN_N AA9 SE78 SD3_PWR EN_N SD3_D[2] AB10 SE33 SD3_D[2] FST_SPI_D[0] AB11 SW1 FST_SPI_D[0] FST_SPI_CLK AB12 SW2 FST_SPI_CLK UART2_DATAOUT AB13 SW21 UART2_D ATAOUT LPE_I2S1_CLK AB14 SW32 LPE_I2S1_CLK LPE_I2S0_DATAIN AB15 SW33 LPE_I2S0_DATAIN I2C5_CLK AB16 SW50 I2C5_CLK	MMC1_D[7]	AA7	SE68			ed unos				UN
EN_N SD3_D[2]	MMC1_D[0]	AA8	SE17						defined	
UART2_DATAOUT	Yej,	AA9	SE78	Fine				ed u	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
CLK	SD3_D[2]	AB10	SE33	Voe,			.0	Jefino		
CLK	FST_SPI_D[0]	AB11	SW1			76	lined			
LPE_I2S1_CLK AB14 SW32 LPE_I2S1 _ CLK LPE_I2S1 _ CLK LPE_I2S1 _ CLK LPE_I2S0 _ DATAIN LPE_I2SO _ DATAIN <t< td=""><td>FST_SPI_CLK</td><td>AB12</td><td>SW2</td><td></td><td>FST_SPI_ CLK</td><td>ed une</td><td></td><td></td><td></td><td>4 U</td></t<>	FST_SPI_CLK	AB12	SW2		FST_SPI_ CLK	ed une				4 U
CLK	-9 ni.	AB13	SW21		UART2_D ATAOUT				define	
LPE_I2S0_DATAIN AB15 SW33 LPE_I2S0 _ DATAIN I2C5_CLK AB16 SW50 I2C5_CLK	"del"	AB14	SW32	4efine				eined'		
I2C5_CLK AB16 SW50 I2C5_CLK	LPE_I2S0_DATAIN	AB15	SW33	and			ال الم	<i>lgerr</i>		
		100	SW50		I2C5_CLK	nd	efines			
	68 aned und				od under	· ·			Datasheet	
Datasheet	4 nugeri.			indefin				defined		
68 Datasheet			red	OI.			AV	IUO		

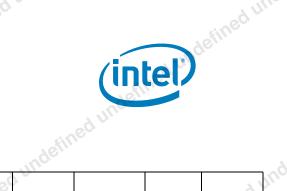


9e,,		undefine				adefined				efined u
	Physical Interfaces			, ind	Jefined U	ndefined		(in	tel	
defined under	lives		ae ^s	lued n.				ied nue		
eined u.	Table 37. Mult	iplexed Fu	nctions -	- T3 SoC	(Sheet 5	of 9)	"uge,,			
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	LPE_I2S2_CLK	AB19	SW92		LPE_I2S2 _CLK	<i>P</i>			ned un	
	ISH_GPIO[0]/ I2S3_CLK	AB2	E21	ed un	ISH_GPI O[0]		I2S3_CL K	unde		
ined und	PCIE_CLKREQ[0]_ N	AB20	SW90	in	PCIE_CLK REQ[0]_ N		indefi	veo		
	ISH_GPIO[2]/ I2S3_DATAOUT	AB3	E24		ISH_GPI O[2]	EINE	I2S3_DA TAOUT			6.0
	SD2_CMD	AB5	SE22		SD2_CM D	nuger				define
	MMC1_D[2]	AB6	SE20		MMC1_D[2]				tined w	
	MMC1_D[6]	AB7	SE63	red u	MMC1_D[6]			4 und		
ned uni	SD3_1P8_EN	AB8	SE85	Siling	SD3_1P8 _EN		34	Inec		
Ver	SD3_D[1]	AB9	SE30		SD3_D[1		ed una			
	1254_DATAIN	AC1	E16		ISH_GPI O[7]	undefin	I2S4_DA TAIN			adefine
	SD3_D[0]	AC10	SE35		SD3_D[0]				"ned"	
	FST_SPI_D[1]	AC11	SW5	ed'	FST_SPI_ D[1]			d und	em	
ined un	UART2_RTS_N	AC12	SW19	Je _{ll} II.	UART2_R TS_N		und	Fine		
	UART1_CTS_N	AC13	SW18		UART1_C TS_N	ndefi	ned			efine
	UART1_DATAOUT/ UART0_DATAOUT	AC14	SW20		UART1_D ATAOUT	UARTO_D ATAOUT			. red	nuos
	NFC_I2C_DATA	AC15	SW51	ced	NFC_I2C _DATA			4 UT	ge _{ff.}	
adv	NFC_I2C_CLK	AC16	SW54	defile	NFC_I2C _CLK		- 2	efinea		
ined v	I2C2_DATA	AC17	SW62		I2C2_DA TA	le f	lued nu			.::0
	a undef	ined m.	ı	I		led unde	I	<u>I</u>	1	Indetil
					d undefin			defined v	ndefine	
retined,	indefine			define				eined u		
			ed u	inor			nu ,	ge,,		
76///			ine				99			



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GPI LPE ISH I2S GPI MM	Name Ball		GPIO # SW78	- T3 SoC Mode 0	(Sheet 6 Mode 1	of 9) Mode 2	Mode 3	Mode 4		
GPI LPE ISH I2S GPI MMI	GPIO Pin Name IO_SW78 E_I2S2_FRM H_GPIO[4]/ 64_CLK IO_SW93	Package Ball # AC18 AC19	GPIO # SW78				Mode 3	Mode 4		2
GPI LPE ISH I2S GPI MMI	Pin Name IO_SW78 E_I2S2_FRM H_GPIO[4]/ 64_CLK IO_SW93	AC18 AC19	# SW78	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4		
ISH I2S GPI	E_I2S2_FRM H_GPIO[4]/ H_CLK IO_SW93	AC19				1 2 2 2			Mode 5	Mode 6
ISH I2S GPI MM	H_GPIO[4]/ H_CLK IO_SW93		SW96		1efinec	0.			ined v	Vo-
I2S GPI MM	64_CLK IO_SW93	AC2		ened "	LPE_I2S2 _FRM			-d und	S	
MM ¹	IO_SW93	ĺ	E22	Sill.	ISH_GPI O[4]		I2S4_CL K	line		
MM	IC1 D[3]	AC20	SW93			410	ed una			
		eq	SE26		MMC1_D[3]	3 nuges,			4 1	indelin.
BABA.	IC1_D[4]	AC7	SE67		MMC1_D[4]				sined.	
- 6	in		SE65	aned.	MMC1_D[5]			ad un'	ge.	
. 13			SE31	9611.	SD3_CLK			tines		
sineo SD3	3_D[3]	AD10	SE32		SD3_D[3]		4 UNO			
UAF	RT2_CTS_N	AD12	SW22		UART2_C TS_N	indefi	Vec			defin
		AD14	SW16		UART1_D ATAIN	UARTO_D ATAIN			dined	nuc
SD3		AD16	SW49	i of the d	I2C6_DA TA	SD3_WP		red ur	96.	
MM	IC1_RESET_N	AD18	SW80	VOICE		MMC1_R ESET_N		Silli		
ISH ISH	H_GPIO[10]/ H_UART_DATAO	AD2	SE1		PWM[1]	ISH_GPI O[10]	ISH_UAR T_DATAO UT			.ndefil
SD3	3_WP	AD20	SW95		adefil	SD3_WP			iefine	3 011
	Cit I	AD3	SE5		PWM[0]				Nois	
	2_D[0]	AD4	SE25	define	SD2_D[0]					
SD2	2_CLK	AD5	SE19		SD2_CLK		711	'ge,		
SD2			SE15		SD2_D[3]_CD_N		fined			
	46	stined ur.				hed uno				ed undef
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ined un.	Table 37. Mult	iplexed Fu	nctions -	- T3 SoC	(Sheet 7	of 9)	"Wqe _{ill} "			
	GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
	MMC1_CLK	AD8	SE16		MMC1_CL	<i>P</i>			ad un	<i>-</i>
	UART2_DATAIN	AE12	SW17	sed un	UART2_D ATAIN			unde	III.	
Indefined und	UART1_RTS_N	AE13	SW15		UART1_R TS_N		indefi	veo.		
Indett.	I2C6_CLK/NMI_N	AE16	SW53		I2C6_CLK	NMI_N	Ò			fined
	I2C5_DATA	AE17	SW45		I2C5_DA TA	Oll .			od u	Juge.
	UARTO_DATAIN	AE18	SW77	ي ن	Joe 1	UARTO_D ATAIN		ndi	file	
in.	SD2_D[1]	AE4	SE18	efinea	SD2_D[1]		٥	ined with		
fined u	SD2_D[2]	AE5	SE21		SD2_D[2]		4 nuge,			
undefined uni	SD3_CD_N	AE9	SE81		SD3_CD_ N	indefin	80			lefined
	GPIO_CAMERASB1 0	B10	N50		GPIO_CA MERASB1 0	3 0.			sined l	Inos
	DDI0_BKLTCTL	B8	N65	_ed1	DDIO_BK LTCTL			4 und	e i	
Jundefined un	GPIO_CAMERASB1	C11	N55	Selius	GPIO_CA MERASB1 1		inde	fineo		
4 undein	GPIO_SUS8	C13	N23		GPIO_SU S8	Aefi ^l	ned th			eine.
	DDI0_BKLTEN	C8	N60		DDIO_BK LTEN	d une			- 6-	nuger
	GPIO_CAMERASB0 9	D10	N52	6.0	GPIO_CA MERASB0 9			, un	defines	
edu	GPIO_CAMERASB0 8	D11	N47	definit	GPIO_CA MERASB0 8			efineo		
ed undefined u	DDI0_HPD	D9	N61		DDI0_HP	46	ined all			2002
	Datasheet	Ined or			Jundefin	led nuc			od	undefin
	Datasheet				I nuger.			defined u	ndefine	
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Table 37. Mult	tiplexed Fu	nctions -				undef	Inc		_
GPIO Pin Name	Package Ball #	GPIO #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	N
SVID_ALERT_N	E12	N38		SVID_AL ERT_N	0			ed u	i.C.
DDI2_HPD	E9	N68	ed '	DDI2_HP D			, und	Still	
SVID_CLK SVID_DATA GPIO_DFX4	F11	N40	efine	SVID_CL K			ineo.		
SVID_DATA	F12	N33	SVID_D ATA	, c		od unde			
GPIO_DFX4	F18	N5			indefil				
PROCHOT_N	F9	N32		PROCHOT _N	9.			ed	U
LPE_I2S2_DATAIN	U17	SW94	ed	LPE_I2S2 _DATAIN			, un	lge _{ll} i,	
PMC_SUSPWRDNA CK	V12	SE83	deline	PMC_SUS PWRDNA CK		60.	efined		
CK LPE_I2S2_DATAOU T	V18	SW97		LPE_I2S2 _DATAOU T	46	ueg m.			
PMC_SUS_STAT_N	V5	E2		PMC_SUS _STAT_N	ed nuo				
I2C1_DATA	W15	SW60	ne	I2C1_DA TA			الم	ndefine	
I2C1_CLK	W16	SW63	nde ^{fill}	I2C1_CLK		dun	Je jinec		
I2C1_CLK PMC_PWRBTN_N	M3 71/10	E8		PMC_PW RBTN_N	unde	inec			
ISH_GPIO[3]/ I2S3_DATAIN	Y1	E15		ISH_GPI O[3]	ieg .	I2S3_DA TAIN		#ine	0
LPE_I2S1_DATAIN	Y13	SW37	:: 108	LPE_I2S1 _DATAIN			-9,	nuger.	
LPE_I2S1_DATAOU T	Y14	SW34	Indei	LPE_I2S1 _DATAOU T			define		
LPE_I2SO_FRM	Y16	SW35		LPE_I2S0 FRM	6.	efined			
LPE_I2S1_DATAOU T LPE_I2S0_FRM	.00			LPE_I2S0	ned und	stined b		Datasheet	
ned undefil.		o.d	undefin			21/2	Indefined	n,	



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I2CO_CLK				4 un				in eith	
I2CO_CLK	defill			inec			. 40	ed m.	
I2CO_CLK	Table 37.	Multiplexed Fu	ınctions	- T3 SoC	(Sheet 9	of 9)	undefil	*	
I2CO_DATA	GPIO Pin Name			Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
ISH_GPT IZS3_FS	I2C0_CLK	Y17	SW65		I2C0_CLK				ned un
ISH_GPI IZS3_FS	fined un.			ed un	ge.			unde	
ISH_GPIO[1]/ 12	I2C0_DATA	Y18	SW61				defi	Ve _o	
ISH_GPT IZS3_FS		defir	eq.			sine	dune		
	130_GP10[1]/	Y2	E18			nuger	I2S3_FS		
PMC_SUS CLK[0]	PMC_WAKE_N	Y3	E10	4				20	fined
		0] Y4	E6	efined v				ined una	
	PMC_PLTRST_N	V Y5	E5 \\		PMC_PLT		ed nuge,		
USB_OC[0]_N	MMC1_D[1]	Y8	SE24		MMC1_D[undefin			
undefined undefi	USB_OC[0]_N	Y9	SE80		USB_OC[ined'
	undefine	ade	iined un		§		ned und	Fined un	
	d undefined un	defined un.		ndefined	undefine	id undefi		efined un	defined
ed undefined un.	d undefined un	defined un	afined u	ndefined	undefine	d undefi	ined und	efined un	defined
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3 Processor Core

Up to four out-of-order execution processor cores are supported, each dual core module supports up to 1 MB of L2 cache.

3.1 Features

- 14nm Process technology.
- Quad Out-of-Order Execution (OOE) processor cores.
- Primary 32 KB, 8-way L1 instruction cache and 24 KiB, 6-way L1 write-back data cache.
- Cores are grouped into dual-core modules: modules share a 1 MB, 16-way L2 cache (2 MB total for Quad Core)Intel[®] Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2), which include new instructions for media and for fast XML parsing.
- Intel[®] 64 Bit architecture
- Supports IA 32-bit.
- Supports Intel[®] VT-x2.
- Supports Intel[®] Advanced Encryption Standard (AES) New instructions (AES-NI).
- Supports Intel[®] Carry-Less Multiplication Instruction (PCLMULQDQ).
- Supports Digital Random Number Generator (DRNG).
- Supports C0, C1, C1E, C6C, C6 and C7 states.
- Thermal management support via Intel[®] Thermal Monitor (TM1 & TM2).
- Uses Power Aware Interrupt Routing (PAIR).

Note: Intel[®] Hyper-Threading Technology is not supported.

3.1.1 Intel[®] Virtualization Technology (Intel[®] VT)

Intel[®] Virtualization Technology (Intel[®] VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel[®] VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel[®] Virtualization Technology for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-x2) added hardware support in the processor to improve the virtualization performance and robustness.

Intel® VT-x2 specifications and functional descriptions are included in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at: http://www.intel.com/products/processor/manuals/index.htm.



Other Intel® VT-x2 documents can be referenced at: http://www.intel.com/technology/virtualization/index.htm

3.1.1.1 Intel® VT-x2 Objectives

- Robust: VMMs no longer need to use paravirtualization or binary translation. This
 means that they will be able to run off-the-shelf OSs and applications without any
 special steps.
- Enhanced: Intel[®] VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation
 of VMs and further prevents corruption of one VM from affecting others on the
 same system. Intel[®] VT-x2 provides hardware acceleration for virtualization of IA
 platforms. Virtual Machine Monitor (VMM) can use Intel[®] VT-x2 features to provide
 improved reliable virtualized platform.

3.1.1.1.1 Intel® VT-x2 Features

- Extended Page Tables (EPT)
 - EPT is hardware assisted page table physical memory virtualization.
 - Support guest VM execution in unpaged protected mode or in real-address mode.
 - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance.
- Virtual Processor IDs (VPID)
 - A VM Virtual Processor ID is used to tag processor core hardware structures (such as TLBs) to allow a logic processor to cache information (such as TLBs) for multiple linear address spaces.
 - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
 - Mechanism for a VMM to preempt the execution of a guest OS VM after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
 - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees flexibility in guest VM scheduling and building Quality of Service (QoS) schemes.
- Descriptor-Table Exiting
 - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data



structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).

 A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

VM Functions

- VM function is an operation provided by the processor that can be invoked using the VMFUNC instruction from quest VM without a VM exit.
- VM function to perform EPTP switching is supported and allows guest VM to load a new value for the EPT pointer, thereby establishing a different EPT paging structure hierarchy.

3.1.2 Security and Cryptography Technologies

3.1.2.1 Advanced Encryption Standard New Instructions (AES-NI)

The processor supports Advanced Encryption Standard New Instructions (AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). AES-NI are valuable for a wide range of cryptographic applications, for example: applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

AES-NI consists of six Intel® SSE instructions. Four instructions, namely AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for support AES, offering security, high performance, and a great deal of flexibility.

3.1.2.2 PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.1.2.3 Digital Random Number Generator

The processor introduces a software visible digital random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the new RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards (ANSI X9.82 and NIST SP 800-90).



Some possible uses of the new RDRAND instruction include cryptographic key generation as used in a variety of applications including communication, digital signatures, secure storage, and so on.

3.1.3 Power Aware Interrupt Routing

PAIR is an improvement in H/W routing of "redirectable" interrupts. Each core power-state is considered in the routing selection to reduce the power or performance impact of interrupts. System BIOS configures the routing algorithm, e.g. fixed-priority, rotating, hash, or PAIR, during setup via non-architectural register. The PAIR algorithm can be biased to optimize for power or performance and the largest gains will be seen in systems with high interrupt rates.

3.2 Platform Identification and CPUID

In addition to verifying the processor signature, the intended processor platform type must be determined to properly target the microcode update. The intended processor platform type is determined by reading bits [52:50] of the IA32_PLATFORM_ID register, (MSR 17h) within the processor. This is a 64-bit register that must be read using the RDMSR instruction. The 3 Platform Id bits, when read as a binary coded decimal (BCD) number, indicate the bit position in the microcode update header's Processor Flags field that is asSoCiated with the installed processor.

Executing the CPUID instruction with EAX=1 will provide the following information.

EAX	Field Description
[31:28]	Reserved
[27:20]	Extended Family value
[19:16]	Extended Model value
[15:13]	Reserved
[12]	Processor Type Bit
[11:8]	Family value
[7:4]	Model value
[3:0]	Stepping ID Value

3.3 References

For further details on Intel[®] 64 and IA-32 architectures refer Intel[®] 64 and IA-32 Architectures Software Developer's Manual Combined Volumes:1, 2A, 2B, 2C, 3A, 3B, and 3C:

 http://www.intel.com/content/www/µs/en/processors/architectures-softwaredeveloper-manuals.html

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For more details on AES-NI refer:

- For more details on using the RDRAND instruction refer Intel® Advanced Vector Extensions Programming Reference.

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Integrated Clock

Clocks are integrated, consisting of multiple variable frequency clock domains, across different voltage domains. This architecture achieves a low power clocking solution is supports the various clocking requirements of the SaG' clocking is provided integrated. clocking is provided internally by the iClock block and does not require external devices for clocking. All the required platform clocks are provided by only two inputs: a 19.2 MHz primary reference for the integrated clock block and a 32.768 kHz reference for the Real Time Clock (RTC) block. Both of these would likely be implemented as crystal references.

The different inputs and outputs are listed below.

Table 38. **SoC Clock Inputs**

	Clock Domain	Signal Name	Frequency	Usage/Description
ined un	Main	ICLK_OSCIN ICLK_OSCOUT	19.2 MHz	Reference crystal for the iCLK PLL
1 under	RTC	RTC_X1 RTC_X2	32.768 kHz	RTC crystal I/O for RTC block
indefined	LPC	LPC_CLKOUT	19.2 MHz	Can be configured as an input to compensate for board routing delays through Soft Strap.

Table 39. SoC Clock Outputs (Sheet 1 of 2) Jundefined undefined un

Ind	Clock Domain	Signal Name	Frequency	Usage/Description	
indefined undefined une	DDR	LPDDR3_M0_CK_P_A/B LPDDR3_M0_CK_N_A/B LPDDR3_M1_CK_P_A/B LPDDR3_M1_CK_N_A/B	800 MHz	Drives the Memory ranks 0-1. Data rate (MT/s) is 2x the clock rate.	
Jundefine	SDXC	MMC1_CLK SD2_CLK SD3_CLK	200 MHz	Clock for Storage Devices	offined u
	SPI	SPI1_CLK FST_SPI_CLK	20 MHz, 33 MHz, 50 MHz	Clock for SPI flash	d nuge.
sined un	PMIC/COMMS	PMC_SUSCLK[0]	32.768 kHz	Pass through clock from RTC oscillator	
d under	LPC	LPC_CLKOUT[0:1]	19.2 MHz	Provided to devices requiring LPC clock	
ndefined undefined s	Display Port	DDI[0]_TXP[3] DDI[0]_TXN[3]	162 or 270 MHz	Differential clock for DP devices	
ed und	HDMI	DDI[2]_TXP[3] DDI[2]_TXN[3]	25-297 MHz	Differential clock for HDMI devices	defined
	ndefine		Jefined -	ni:	ed une
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	define		
ble 39. SoC Clock Outp	outs (Sheet 2 of 2)		indeti.
Clock Domain	Signal Name	Frequency	Usage/Description
HDMI DDC	DDI[2:0]_DDCCLK	100 kHz	Clock for HDMI DDC devices
MIPI DSI	MDSI_A_CLKP MDSI_A_CLKN MDSI_C_CLKP MDSI_C_CLKN	1000 MHz	Differential clock for MIPI DSI Devices
MIPI CSI	MCSI1_CLKP MCSI1_CLKN MCSI2_CLKP MCSI2_CLKN MCSI3_CLKP MCSI3_CLKN	200-400 MHz	Clocks for front and rear cameras
SVID	SVID_CLK	20 MHz	Clock used by voltage regulator
I ² S	LPE_I2S[2:0]_CLK	9.6 MHz	Continuous serial clock for I ² S interfaces
Platform Clocks	PLT_CLK [5:0]	19.2MHz	Platform clocks.
SIO SPI	SPI_CLK	15 MHz	SPI clock output
Platform Clocks SIO SPI I ² C NFC	I2C[6:0]_CLK	1.7MHz	I ² C clocks
NFC	NFC_I2C_CLK	100 kHz	Clock for NFC device
sed unos	<u> </u>	dein	adefines
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5 Power Up and Reset Sequence

This chapter provides information on the following topics:

- "Power Up Sequences"
- "Power Down Sequences"
- "Reset Behavior"

5.1 SoC System States

5.1.1 System Sleeping States Control (S-states)

The SoC supports the S0, S0i1, S0i2, S0i3, S4, and S5 sleep states. S4 and S5 states are identical from a hardware and power perspective. The differentiation is software determined (S4 = Suspend to Disk).

The SoC platform architecture assumes the usage of an external power management controller e.g., CPLD or PMIC. Some flows in this section refer the power management controller for support of the S-states transitions.

The SoC sleep states are described in Chapter 7, "Power Management".

5.2 Power Up Sequences

5.2.1 RTC Power Well Transition (G5 to G3 States Transition)

When RTC_VCC (Real Time Clock power) is applied via RTC battery, the following occurs (refer Figure 2 for timing):

- 1. RTC_VCC ramps. RTC_RST_N should be low.
- 2. The system starts the real time clock oscillator.
- 3. A minimum of t1 units after RTC_VCC ramps, the external RTC RC circuit de-asserts RTC_RST_N. The system is now in the G3 state. RTC oscillator is unlikely to be stable at this point.

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Figure 2. **RTC Power Well Timing Diagrams**

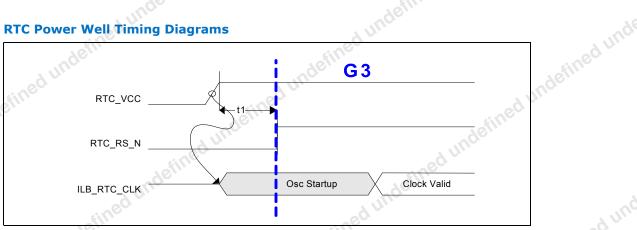


Table 40. **RTC Power Well Timing Parameters**

Parameter	Description	Min	Max	Units
t1	RTC_VCC to RTC_RST_N de-assertion	9	ı	ms

NOTES:

- 1. This delay is typically created from an RC circuit.
- 2. The oscillator startup times are component and design specific. A crystal oscillator can take several second to reach a large enough voltage swing. A silicon oscillator can have startups times <10 ms.
- 3. All VCC measurements points are at 90% nominal VCC voltage.

5.2.2 G3 to S4/S5

The timings shown in Figure 3 occurs when a board event such as AC power or power button is pressed. The following occurs:

- 1. Suspend well ramp in the order given.
- 2. The external power management controller de-asserts PMC_RSMRST_N after the suspend rails become stable.
- 3. PMC_SUSCLK will begin toggling after the de-assertion of PMC_RSMRST_N.
- 4. The system is now in S4/S5 state. Depending on policy bits, the system either waits for a wake event, or continues to S0 states.

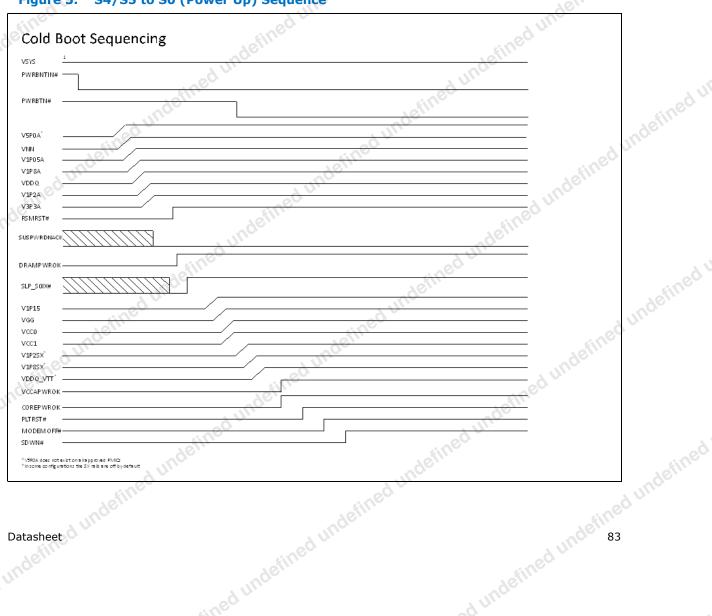
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5.2.3 **S4/S5 to S0**

- 1. The external power management controller detects an event (i.e., power button) to
- 2. VCC, VNN and other S0 core voltage power rails may be enabled after the initiation of the S4/S5 to S0 event. The VCC and VNN voltage rails must be driven to the default values.
- 3. After the DRAM power rail ramp, the external power management controller drives DRAM PWROK high.
- 4. After all of the S0 core voltage power rails are stable, external power management controller drives PMC_CORE_PWROK and VCCA_PWROK to HIGH.
- 5. The processor de-asserts PMC_PLTRST_N after PMC_CORE_PWROK is stable. The PMC_PLTRST_N is the main platform reset to other components.
- 6. The processor will begin fetching code from either the PCU-located SPI interface or the LPC interface.

S4/S5 to S0 (Power Up) Sequence





NOTES:

- 1. RTC and SUS power rails may come up at the same time if no RTC battery is used.
- 2. RTC clock should be oscillating, but may not be at 32.768 KHz yet.
- 3. Wake events show in figure are optional and depending on platform configuration.

5.3 Power Down Sequences

5.3.1 S0 to S4/S5 Sequence

Entry to Sleep states (S4, S5) is initiated by any of the following methods:

- Setting the desired sleep type in PM1_CNT.SLP_TYP and setting PM1_CNT.SLP_EN.
- Detection of an external catastrophic temperature event may cause a transition to G3, if the system is designed to do so.

The following sequence applies to S0-S4/S5 transitions.

- The Operating System Power Management (OSPM) will handle the enabling or disabling of interrupt generation after S4 resume. The Operating System Power Management (OSPM) will need to read and clear Wake status information and the processing of the clearing wake status which will include enabling interrupts (both at the core level and platform level).
- 2. All interrupts in the processor need to be disabled before the S4 sequence is started (and re-enabled on exit). The CPU APIC must be disabled.
- 3. When the desired sleep state is set in the PM1_CNT.TYP and PM1_CNT.SLP_EN registers, a sleep state request is sent to the PMC.
- 4. The PMC flushes all the internal buffers to main memory.

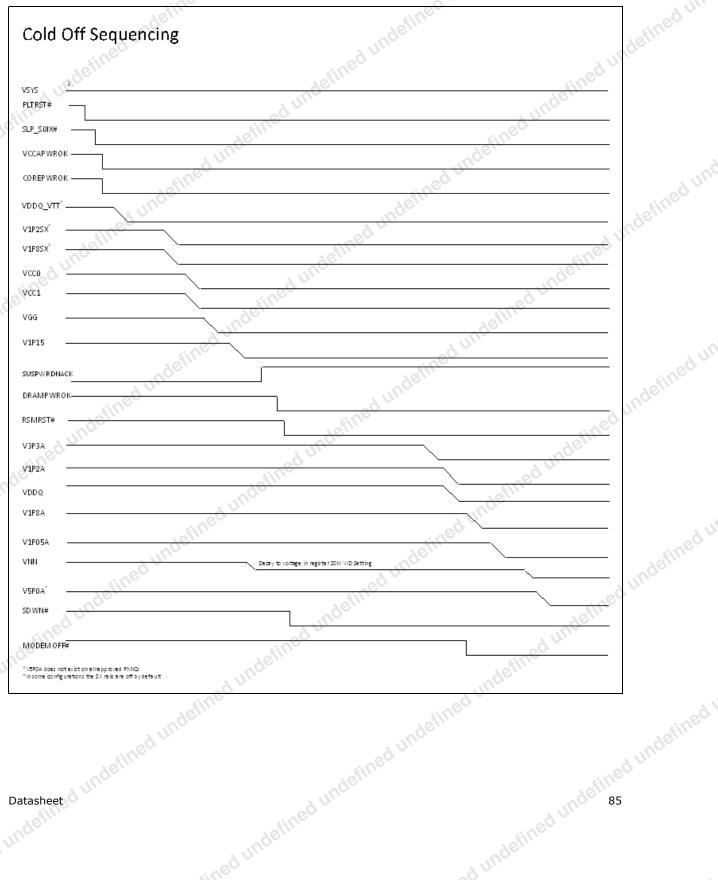
The Power Down Sequence is shown in Figure 4 below.

Other Assumptions:

- Entry to a Cx state is mutually exclusive with software-initiated entry to a Sleep state. This is because the processor(s) can only perform one register access at a time. This requirement is enforced by the CPU as well as the OS. The system may hang if it attempts to do a C-state and S-state at the same time.
- The G3 system state cannot be entered via any software mechanism. The G3 state
 indicates a complete loss of power. In this state, the RTC well may or may not be
 powered by an external coin cell battery.
- An external Power Management Controller (PMIC/EC) can be used to put the
 processor in G3 when the S4/S5 state is requested by the SoC. This is done to save
 power in S4/S5 state. This G3 like state is enabled by removing SUS rails via the
 SUSPWRDNACK pin. Doing so prevents the use of any of SUS wake events
 including USB, RTC, and GPIOs including the power button. The external Power
 Management Controller (or re-application of power) is required to return to S0.









5.3.2 S4/S5 to S0 (Exit Sleep States)

Sleep states (S5) are exited based on Wake events. The Wake events will force the system to a full on state (S0), although some non-critical subsystems might still be powered down and have to be brought back manually. For example, the hard disk may be powered down during a sleep state, and have to be enabled via an I/O pin before it can be used. Upon exit from software-entered Sleep states (i.e., those initiated via the PM1_CNT.SLP_EN bit), the PM1_STS_EN.WAK_STS bit will be set.

To enable Wake Events, the possible causes of wake events (and their restrictions) are shown in Table 41.

Table 41. S4/S5 to S0 Cause of Wake Events

Туре	How Enabled
Internal	Set PM1_STS_EN.RTC_EN register bit
External	Default enabled as Wake event
External	GPE0a_EN register (after having gone to S5 via PM1_CNT.SLP_EN, but not after a power failure.)
ndefille	Note: GPIOs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.
External	Southeast GPIO can (optionally) be used as Wake sources based on GPIO register programming.
Internal	GPEOa_EN.PME_B0_EN register bit. This wake status bit includes multiple internal agents: EHCI (USB2)
Internal	No enable bits. The PMC can wake the host independent of other wake events listed, if desired. A bit is provided in PRSTS for reporting this wake event to BIOS. Note that this wake event may be used as a wake trigger on behalf of some other wake source.
	Internal External External External Internal

5.3.3 Enter S0ix

The S0IX state is entered when the SoC is in a shallow sleep state. This state is entered when the SoC asserts the PMC_SLP_S0IX_N (LOW) pin to the PMIC. VDDQ_VTT and SX rails are turned off. The VCC rail is turned off by SVID commands (not by PMC_SLP_S0IX_N signal). The VNN rail is set to a voltage set in SVID address 39h. The rest of the VRs remain on but enters into PFM/power save mode.

5.3.4 Exit S0ix

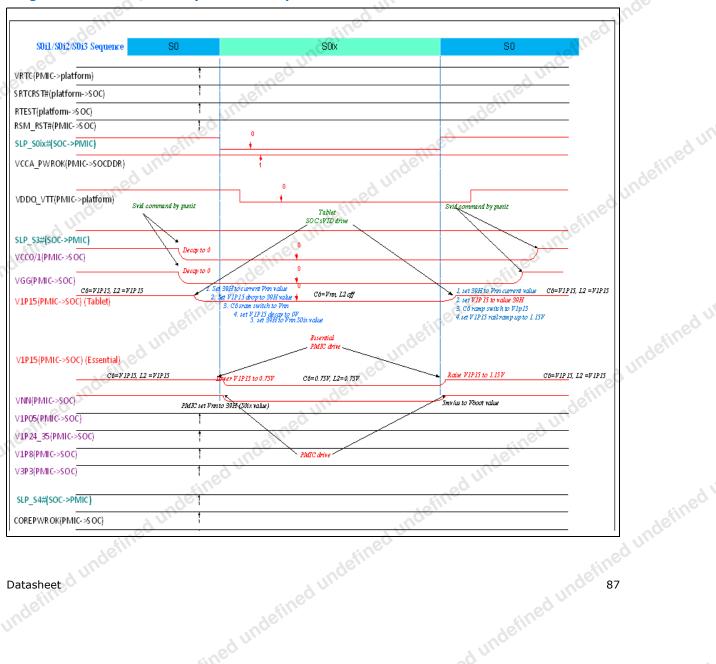
The S0IX state is exited when the SoC de-asserts the PMC_SLP_S0IX_Npin (HIGH). VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by PMC_SLP_S0IX_N). The rest of the rails will come out of PFM/power save mode. All SMI/SCI events wake SoC from the S0ix states. The following table lists the addition events that wake the SoC from S0ix states.



undefined undefined undefined Table 42. S0ix Cause of Wake Events

undefined un	de	fined unc	ofined underlin	
Table 42.	S0ix Cause of Wake Ev	vents	ad under	inde
V _O	Cause	Туре	How Enabled	
, unde	Any GPIO	External	IO-APIC forwards the interrupt, resulting in S0 (as configured by BIOS). Alternatively use S0ix Wake Register (S0IX_WAKE_EN and S0IX_WAKE_STS) in PMC	
18 fined	LPC CLKRUN	External	Wake from S0i2/3 only when the signal is asserted, moves the SoC to S0i1.	
unoc	ISH	External	From External Sensors	
ined	USB	External	USB Port connected device / host	
Figure 5.	S0 to S0ix Entry and E	xit Seque	nce ndefined b	lefined une

S0 to S0ix Entry and Exit Sequence Figure 5.



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5.3.5 **Handling Power Failures**

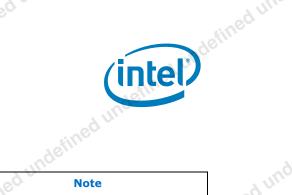
adefined undefined undefined unde The power failures can occur if the AC power or battery is removed. In this case, when the system was originally in a S0 state, power failure bit (GEN_PMCON1.PWR_FLR) is set after a power failure. Software can clear the bit.

Reset Behavior

There are several ways to reset the processor.

Table 43. Types of Resets (Sheet 1 of 2)

	Trigger	Description	Note	111
	Write of 0Eh to CF9 Register	Write of 0Eh to the CF9 register	TYPE 2: Host Reset with Power Cycle: Cold	ined s
	PMC_RSTBTN_N & CF9h bit 3= 1	User presses the reset button, causing the PMC_RSTBTN_N signal to go active (after the debounce logic)	reset. PMC will lose all the information. All the functionality in SoC gets reset.	Indeff.
	defined	ofined une	The host system automatically is powered back up and brought out of reset to S0 state.	
efined u	defined und	ined under	SoC must not drop this type of reset request if received while the system is in a software-entered S4/5 state. However, SoC is allowed to perform the reset without executing the RESET_WARN protocol in these states.	sined u
	indefined	4efinet	If the system is in S5 due to a reset type #8 event, SoC is allowed to drop this type of reset request.	nuger
. 9	PMC_RSTBTN_N & CF9h bit 3= 0	User presses the reset button, causing the PMC_RSTBTN_N signal to go active (after the debounce logic)	TYPE 1:Host Reset with Power Cycle: Warm Reset 1. Host-Only functionality in SoC gets reset	
ed (Write of 06h to CF9 Register	Write of 06h to the CF9 register	2. Any functionality that needs to remain	
3efile	TCO watchdog timer	TCO timer reaches zero two times	operational during a host reset must not get reset. 3. PMC does not get reset. 4. RTC remain information. 5. Suspend well remain information 6. S4/S5 drop the warm reset request.	Jundefined '
	S4/S5	The processor is reset when going to S4 or S5 state	TYPE 4: Sx Entry (host stays there) 1. All the Vnn reset by external power Good. Except:	
defined		efined unc	PMC remain information. RTC remain information. Suspend well remain information	693
	88 Jundefined undefined uni	ined undefined undefin	Datasheet	ed undefille
	88 sined ulli	ed under	Datasheet	
	under	Indefine	defined &	
Silver			dune	



defined undefined undefined Table 43. Types of Resets (Sheet 2 of 2)

Power Up and Reset Sequence	define	(intel)
ined III	ed unde	July City
ndefin	4efines	
Table 43. Types of Reset	s (Sheet 2 of 2)	indelli
Trigger	Description	Note
Power Failure	PMC_CORE_PWROK signal goes inactive in S0/S1	TYPE 7: Global, Power Cycle Reset: S0->S4/S5->S0
Write of 06h or 0Eh to CF9 Register	CF9h global Reset bit = 1b	1. All the Vnn reset by external power
Host Partition Reset Entry Timeout	Host partition reset entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	Good. 2. All power wells that are controlled by the PMC_SLP_S0iX_N pins are turned off. 3. PMC get reset. 4. External Dram-unchanged Except: 1. RTC retain information. 2. Suspend well retain information.
Processor Thermal Trip	The internal thermal sensor signals a catastrophic temperature condition – transition to S5 and reset asserts	SOC_G3: Straight-to-S5 (thermal trip->SOC_G3) SOC power cycle: S0->SOC_G3 SOC lost all the info Except: RTC retain info
PMC_PWRBTN_N	10-second press causes transition	TYPE 8: Straight-to-S5 (Host stays there)
PMC_PWRBTN_N Power Button Override	to S5 (and reset asserts)	SOC power cycle: S0->S4->S5 1. All the Vnn reset by external power
S4/S5 Entry Timeout	S4, or S5 entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	Good. 2. All power wells that are controlled by the PMC_SLP_S0iX_N pins are turned off. 3. External Dram-unchanged Except:
PMC Watchdog Timer	Firmware hang and Watchdog Timeout detected in the PMC platform	PMC retain information. RTC retain information. Suspend well retain information
CPU Shutdown with Policy to assert PMC_PLTRST_N	Shutdown special cycle from CPU can cause either INIT or Reset Control-style PMC_PLTRST_N	Type 7:Global, Power Cycle Reset (if CF9h Global Reset bit = 1b) Type 2:Host Reset with Power Cycle (if CF9h Register bit 3 = 1b) Type 1:Hest Poset without Power Cycle
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d unde.	ed undefin	i undefined
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6 Thermal Management

The SoC's thermal management system helps in managing the overall thermal profile of the system to prevent overheating and system breakdown. The architecture implements various proven methods of maintaining maximum performance while remaining within the thermal spec. Throttling mechanisms are used to reduce power consumption when thermal limits of the device are exceeded and the system is notified of critical conditions via interrupts or thermal signalling pins. SoC thermal management differs from legacy implementations primarily by replacing dedicated thermal management hardware with firmware.

The thermal management features are:

- Eight digital thermal sensors (DTS).
- Supports hardware trip point and four programmable trip points based on the temperature indicated by thermal sensors.
- Supports different thermal throttling mechanisms.

6.1 Thermal Sensors

SoC Sensors are based on DTS (Digital Thermal Sensor) to provide more accurate measure of system thermals.

The SoC has 8 DTS's. DTS provides as wires the current temperature around the real estate it occupies on SoC. These are driven to PM unit, which in turn monitor the temperature from DTS on the SoC.

DTS output are adjusted for silicon variations. For a given temperature the output from DTS is always the same irrespective of silicon.

Table 44. Temperature Reading Based on DTS (Sheet 1 of 2)

idefined u	Temperature Reading (If T _{J-MAX} =100°C) Thermal Read Register [7:0]	Temperature Reading (If T _{J-MAX} =110°C)	Temperature Reading (If T _{J-MAX} =100°C)	Temperature Reading (If T _{J-MAX} =90°C)	DTS Counter Value [8:0]	Jundefille
	100°C	110°C	100°C	90°C	127	20
	90°C	100°C	90°C	80°C	137	*inec
	80°C	90°C	80°C	70°C	147	nder
	70°C	80°C	70°C	60°C	157	ad uli
	60°C	70°C	60°C	50°C	167	istine
ed'	50°C	60°C	50°C	40°C	177	Inde
defile	40°C	50°C	40°C	30°C	187	30
	90°C 80°C 70°C 60°C 50°C	100°C 90°C 80°C 70°C 60°C	90°C 80°C 70°C 60°C 50°C	80°C 70°C 60°C 50°C 40°C	137 147 157 167 177	ed undefined undefined be

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Table 44. Temperature Reading Based on DTS (Sheet 2 of 2)

ndefined undefined undef	DTS Counter Value [8:0]	Temperature Reading (If T _{J-MAX} =90°C)	Temperature Reading (If T _{J-MAX} =100°C)	Temperature Reading (If T _{J-MAX} =110°C)	Temperature Reading (If T _{J-MAX} =100°C) Thermal Read Register [7:0]
ed u.	197	20°C	30°C	40°C	30°C
istine	207	10°C	20°C	30°C	20°C
Inde	217	0°C	10°C	20°C	10°C
· · · · · · · · · · · · · · · · · · ·	227	-10°C	0°C	10°C	0°C
defill	237	-20°C	-10°C	0°C	-10°C
TUC.	247	-30°C	-20°C	-10°C	-20°C
	257	-40°C	-30°C	-20°C	-28°C [255]
	247	-50°C	-40°C	-30°C	-28°C [255]

Note:

DTS encoding of 127 always represents Tjmax. If Tjmax is at 100°C instead of 90°C then the encoding 127 from DTS indicates 100°C, 137 indicates 90°C and so forth.

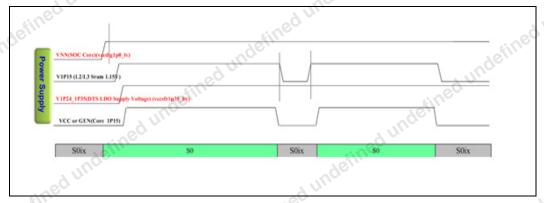
Thermal trip points are of two types:

- **Hard Trip**: The Catastrophic trip points generated by DTS's based on predefined temperature setting defined in fuses.
- **Programmable Trips**: SoC provides four programmable trip settings (Hot, Aux2, Aux1, Aux0) that can be set by firmware/software. Default value for Hot Trip is from Fuses.

6.1.1 DTS Timing

DTS should be enabled only after setting up SoC and system to prevent spurious counts from DTS to trigger thermal events. P-Unit determines when DTS is enabled. The figure below shows the various control signals needed for DTS operations.

Figure 6. DTS Operation Mode





6.2 Hardware Trips

6.2.1 Catastrophic Trip (THERMTRIP)

Catastrophic trip is generated by DTS whenever the ambient temperature around it reaches (or extends) beyond the max value (indicated by a fuse). Catastrophic trip will not trip unless enabled (DTS are enabled only after HFPLL is locked). Within each DTS Catastrophic trips are flopped to prevent any glitches on Catastrophic signals from affecting the SoC behavior. Catastrophic trips are reset, once set, during power cycles.

Catastrophic trip signals from all DTS in the SoC are combined to generate THERMTRIP function which will in turn shut off all the PLL's and power rails to prevent SoC breakdown. To prevent glitches from triggering shutdown events, Catastrophic trip's from DTS's are registered before being sent out.

6.3 SoC Programmable Trips

Programmable trips can be programmed to cause different actions when triggered to reduce temperature of the die.

6.3.1 Aux3 Trip

By default, the Aux 3 (Hot Trip) point is set by software/firmware has an option to set these to a different value.

This trip point is enabled by firmware to monitor and control the system temperature while the rest of the system is being set up.

6.3.2 Aux2, Aux1, Aux0 Trip

These are fully programmable trip points for general hardware protection mechanisms. The programmable trips are only active after software/firmware enables the trip.

Note:

Unlike Aux3, the Aux[2:0] trip registers are defaulted to zero. To prevent spurious results, software/firmware should program the trip values prior to enabling the trip point.

6.4 Platform Trips

6.4.1 PROCHOT#

The platform components use the signal PROCHOT# to indicate thermal events to SoC. Assertion of the PROCHOT# input will trigger Thermal Monitor 1 or Thermal Monitor 2 throttling mechanisms if they are enabled.



6.4.2 **EXTTS**

SoC does not support external thermal sensors and the corresponding bits in the P-Unit registers will be reserved for future use if needed.

For SoC, PROCHOT is the only mechanism for a platform component to indicate Thermal events to P-Unit.

6.4.3 sVID

When the Voltage Regulator (VR) reaches it's threshold (VR_Icc_Max, VR_Hot), status bits in sVID are set. sVID sends SVID Status message to PUnit.

6.5 Dynamic Platform Thermal Framework (DPTF)

SoC is required to support interface for OS level thermal drivers and Intel's DPTF (Dynamic Platform and Thermal Framework) drivers to control thermal management. This interface provides high-level system drivers a mechanism to manage thermal events within the SoC with respect to events outside SoC. These events could potentially be triggered before PM Unit firmware performs active management as DPTF/OS level drivers respond to events on platform outside of SoC.In addition, these interfaces also respond to interrupts from within the SoC.

Platform level thermal management layout is shown in the figure below.

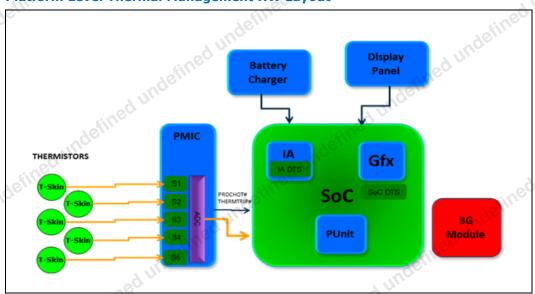


Figure 7. Platform Level Thermal Management HW Layout

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The thermal events happen outside of SoC on platform level are reported as interrupts from PMIC. PMIC monitors a number of catastrophic and critical thermal events, such as PMIC over-temperature, system over-temperature (reported by skin sensors), and

Thermal Status

The firmware captures to trigger them actions The firmware captures Thermal Trip events (other than THERMTRIP) in status registers of price of price of the control of d undertreed undertreed undertreed undertreed undertreed undertreed under treed under tree to trigger thermal actions. Associated with each event is a set of programmable

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7 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- Integrated Graphics Controller

7.1 Features

- ACPI System States support (S0, S0i1, S0i2, S0i3, S4, S5).
- Processor Core/Package States support (C0 C7).
- SoC Graphics Adapter States support D0 D3.
- Supports CPU and GFx Burst.
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers).
- Active power down of display links.

7.2 States Supported

The Power Management states supported by the processor are described in this section.

7.2.1 System States

Table 45. General Power States for System (Sheet 1 of 2)

Indefine	States/Sub- states	Legacy Name / Description
30	G0/S0/C0	FULL ON: CPU operating. Individual devices may be shut down to save power. The different CPU operating levels are defined by Cx states.
	G0/S0/Cx	Cx State: CPU manages C-state itself.
stined ur	G0/S0i1	S0i1 State: Low power platform active state. All DRAM and IOSF traffic are halted. PLL are configured to be off. This state allows MP3 playing using ISH/LPE engine
inde.	G0/S0i2	S0i2 State: The SoC clocks and oscillators are parked
ed u.	G0/S0i3	S0i3 State: All SoC clocks and oscillators are turned off
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Table 45. General Power States for System (Sheet 2 of 2)

nden	States/Sub- states	Legacy Name / Description
6	G1/S4	Suspend-To-Disk (STD): The context of the system is maintained on the disk. All of the power is shut down except power for the logic to resume. The S4 and S5 states are treated the same.
indefined une	G2/S5	Soft-Off: System context is not maintained. All of the power is shut down except power for the logic to restart. A full boot is required to restart. A full boot is required when waking. The S4 and S5 states are treated the same.
Indefined b	G3	Mechanical OFF. System content is not maintained. All power shutdown except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3.

Table 48 shows the transitions rules among the various states.

Note:

Transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.

Table 46. Cause of Sx Wake Events

	Cause	How Enabled
	RTC Alarm	Set RTC_EN bit in PM1_EN Register
	Power Button	Always enabled as Wake event from Sx
ed u	PMC_SLP_S4_N	None
18 fine	PMC_BATLOW_N	None
INOG	PMC_SUS_STAT_N	None
ined or	PMC_SLP_S0IX_N	None
define	PMC_ACPRESENT	None
Unit	PMC_PLTRST_N	None
	PMC_SUSCLK[0]	None

The following shows the differences in the sleep states with regards to the processor's output signals.

Table 47. SoC Sx-States to SLP_S*# (Sheet 1 of 2)

State	SO 117	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	No	OFF
PMC_SLP_S4_N	HIGH	LOW	LOW	HIGH	LOW



SoC Sx-States to SLP S*# (Sheet 2 of 2)

SoC Sx-States to S	SLP_S*#	# (Sheet	t 2 of 2)	ind	eji	
State	S0	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle	ined und
S0 Power Rails	ON	OFF	OFF	ON	OFF	deill
PMC_PLTRST_N	0	1	100	1	1	dulli
PMC_SUS_STAT_N	HIGH	LOW	LOW	HIGH	LOW	S.

NOTE: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S4_N. PMC_SUS_STAT_N is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT_N also warns of upcoming reset.

ACPI PM State Transition Rules

nae e	Present State	Transition Trigger	Next State	lefined b
	G0/S0/C0	IA Code MWAIT or LVL Rd	C0/S0/Cx	VOC
4 unde		PM1_CNT.SLP_EN bit set	G1/Sx or G2/S5 state (specified by PM1_CNT.SLP_TYP)	
		Power Button Override	G2/S5	
adeil.		Mechanical Off/Power Failure	G3	
ndefined undefined unde	G0/S0/Cx	Cx break events which include: CPU snoop, MSI, Legacy Interrupt, AONT timer	G0/S0/C0	
UOC	200	Power Button Override	G2/S5	red
	d ull	Resume Well Power Failure	G3	46fill.
b _n .	G1/S4	Any Enabled Wake Event	G0/S0/C0	nuc.
	8,	Power button Override	G2/S5	
ed u.		Resume Well Power Failure	G3	
	G2/S5	Any Enabled Wake Event	G0/S0/C0	
unos		Resume Well Power Failure	G3	
undefined undefined un	G3	Power Returns	Option to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other enabled wake event) or G1/S4 (if system state was S4 prior to the power failure). Some wake events are preserved through a power failure.	undefined
iefineo		State Combinations tate Combinations (Sheet 1 of 2	2) sined undefined	
tined b	Global S	leep Processor Processor	System Clocks Description	

	4in			- 200	preserved tillough a	power failure.	- UI.
7.2.2 Table 49.			e Combin	ations (Sheet 1 of 2)		rined undefin	
undefined L	Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description	ed
d	G0	S0	CO	Full On	On	Full On	4efilne
	undefined			indefined	o.	46/11	led nug
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Table 49. G, S and C State Combinations (Sheet 2 of 2)

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ndein.	Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
	G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
الم الم	G0	S0	C6	Deep Power Down	On	Deep Power Down
defined	G0	S0ix	C7	Deep Power Down	On	Deep Power Down
ndefined undefined ur	G1	S4	Power off		Off except RTC & internal ring OSC	Suspend to Disk
indefil.	G2	S5	Power off		Off except RTC & internal ring OSC	Soft Off
₽	G3	NA	Power Off		Power off	Hard Off

7.2.3 Integrated Graphics Display States

Table 50. SoC Graphics Adapter State Control

State		Description	
D0	rueq s	Full on, Display active	77
D3	4e _{lll}	Power off display	"I'Ueo

7.2.4 Integrated Memory Controller States

Table 51. Main Memory States

States	Description
Powerup	CKE asserted. Active mode.
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed.
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active.
Self-Refresh	CKE de-asserted using device self-refresh

Table 52. D, S and C State Combinations (Sheet 1 of 2)

Graphics Adapter (D) State	Sleep (S) State	(C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C6	Deep Sleep, Display Off



Table 52. D, S and C State Combinations (Sheet 2 of 2)

Graphics Adapter (D) State	Sleep (S) State	(C) State	Description
D0	S0ix	C7	Deep Sleep, Display Off
D3	S0/S0ix	Any	Not Displaying
D3	S4 unde	100	Not Displaying Suspend to disk Core power off

Not Displa Suspend Core power Management

While executing code, Enhanced Intel SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

7.3.1 Enhanced Intel SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep[®] Technology:

- Applicable to Processor Core Voltage and Graphic Core Voltage
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
 - If the target frequency is higher than the current frequency, Core_VCC is ramped up slowly to an optimized voltage. This voltage is signaled by the SVID signals to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
 - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID signals.
- The processor controls voltage ramp rates by requesting appropriate ramp rates from an external SVID controller.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.
- Thermal Monitor mode.
 - Refer Chapter 6, "Thermal Management"

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7.3.2 Dynamic Cache Sizing*

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

7.3.3 Low-Power Idle States

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-state. However, higher C-states have longer exit and entry latencies. Resolution of C-state occur at the thread, processor core, and processor core level.

7.3.3.1 Clock Control and Low-Power States*

The processor core supports low power states at core level. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done by initiating a P_LVLx (P_LVL4 & P_LVL6) I/O read to all of the cores. States that require external intervention and typically map back to processor core power states. States for processor core include Normal (C0, C1), and Stop Grant.

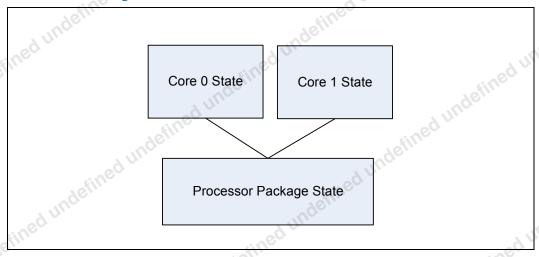
The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state specifies and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state specifications used for each P_LVLx read can be configured in a software programmable MSR by BIOS.

The Cx state ends due to a break event. Based on the break event, the processor returns the system to C0. The following are examples of such break events:

- Any unmasked interrupt goes active
- Any internal event that will cause an NMI or SMI_B
- CPU Pending Break Event (PBE_B)
- MSI



Idle Power Management Breakdown of Processor Cores



Processor Core C-States Description

Table 53. **Processor Core/ States Support**

Hine	State	Description
unde	C0	Active mode, processor executing code
	C1	AutoHALT state
	C1E	AutoHALT State with lowest frequency and voltage operating point.
rzed undefined und	C6	Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on a different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage is completely shut off.
efinec	C7 aned	Execution cores in this state behave similarly to the C6 state. Voltage is removed from the system agent domain

The following state descriptions assume that both threads are in common low power state.

Core CO State 7.3.4.1

The normal operating state of a core where code is being executed.

7.3.4.2 Core C1/C1E State

C1/C1E is a low power state entered when a core execute a HLT or MWAIT(C1/C1E) instruction.



A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. Refer $Intel^{\circledR}$ 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, refer Section 7.3.8.2, "Package C1/C1E".

7.3.4.3 Core C6 State

Individual core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM.Once complete, a core will have its voltage reduced. During exit, the core is powered on and its architectural state is restored.

7.3.4.4 Core C7 State

Individual core can enter the C7 state by initiating a P_LVL7 I/O read or an MWAIT(C7) instruction. The core C7 state exhibits the same behavior as core C6 state, but in addition gives permission to the internal Power Management logic to enter a package S0ix state if possible.

7.3.4.5 C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore incorrect or inefficient usage of deeper C-states has a negative impact on battery life. In order to increase residency and improve battery life in deeper C-states, the processor supports C-state auto-demotion.

This is the C-State auto-demotion option:

• C7/C6 to C1

The decision to demote a core from C7/C6 to C1 is based on each core's immediate residency history. Upon each core C7/C6 request, the core C-state is demoted to C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C6 or C7.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.



7.3.5 **Module C-states**

Table 54. **Module C-states**

sined u.	7.3.5	Module C-	Module C-states		
S,	Table 54.	Module C-state	ies	indefined	
	10.	C-states	Core Status	Cache status	d une
	INOC	C0	At least one core in C0	Normal Operation	
_	efined	C1	Both cores HALTed. Most clocks OFF	No Cache flushed; Snoops wake up cores	
, uno			Both cores in C6 (powered off)	Core DL1s flushed	<u> </u>
ined.			CPLL bypassed (powered off)	L2 flushed	
defill		. 4 4	CPU Refclk OFF BIU domain powered off	L2 domain powered off C2 popup NOT required	ed un

Module C6 7.3.6

There are two module C-states the Punit can put a CPU module into depending on the type of C-state entry sub-state hint and remaining size of L2. In this module C-state, both cores are power gated and all ways of L2 cache can be flushed. In this state, the Punit can power gate the BIU/L2 Vcc domain as well as the VCCSRAM_GT domain.

7.3.7 **S0i1**

Once the core has entered package C6 or C7, the SoC can transition to S0i1. S0i1 transitions from a PC6 means that L2 state will be preserved through S0i1. Transitions from C7 no longer have state retention. These two paths are quite different due to the requirements on the L2 power rails and the need to snoop the core.

Package C-States*

The processor supports C0, C1/C1E,C6 and C7 power states. The following is a summary of the general rules for package C-state entry. These apply to all package Cstates unless specified otherwise:

- Package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
- Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
- The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected.



7.3.8.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

7.3.8.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E via MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.

7.3.8.3 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C7 state but has allowed a package C6 state.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts.

7.3.8.4 Package C7 State

A processor enters the package C7 low power state when all cores are in the C7 state. In package C7, the processor will take action to remove power from portions of the system agent.

Core break events are handled the same way as in package C6.



7.3.9 Graphics, Video and Display Power Management

7.3.9.1 Graphics and video decoder C-State

GFX C-State (GC6) are designed to optimize the average power to the graphics and video decoder engines during times of idleness. GFX C-state is entered when the graphics engine, has no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the processor will power gate the Graphics and video decoder engines.

7.3.9.2 Intel® Display Power Saving Technology (Intel® DPST)

The Intel DPST technique achieves backlight power savings while maintaining visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user image quality at a decreased backlight power level.

- 1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel[®] DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
- 2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
- 3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image. Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

7.3.9.3 Intel[®] Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the back light setting.

7.3.9.4 Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel[®] Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/

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enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the design application is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel SDRRS—static and seamless. The static Intel SDRRS method uses a mode change to assign the new refresh rate. The seamless Intel SDRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

7.4 Memory Power Management

The main memory is power managed during normal operation and in low-power states.

7.4.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as unpopulated, or single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

7.4.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

7.4.2.1 Initialization Role of CKE*

During power-up, CKE is the only input to the SDRAM that is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power- up.

CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.



Conditional Self-Refresh 7.4.2.2

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package low-power states. RMPM functionality depends on graphics/ display state (relevant only when internal graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then places all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package low-power states as long as there are no memory requests to service.

7.4.2.3 **Dynamic Power Down Operation**

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The processor core controller can be configured to put the devices in active power down (CKE deassertion with open pages) or precharge power down (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

DRAM I/O Power Management 7.4.2.4

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled Sed underined underined underined underined under ined automatically when input receiver is disabled).

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8 System Memory Controller

The system memory controller supports DDR3L-RS/LPDDR3 protocol with up to two 64-bit wide dual rank channels at data rates up to 1600 MT/s with ECC is also available on a single DDR3L-RS channel.

8.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

8.1.1 DDR3L-RS Interface Signals

Table 55. Memory Channel 0 DDR3L-RS Signals (Sheet 1 of 2)

	Signal Name	Direction Type	Description
adv	DDR3_M0_CK[1,0]_P DDR3_M0_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.
ndefine	DDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.
ndefined undefine	DDR3_M0_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.
unde.	DDR3_M0_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.
	DDR3_M0_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.
ined!	DDR3_M0_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands
indefined undefin	DDR3_M0_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands
d undefines	DDR3_M0_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
	ined	•	40,



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Table 55. Memory Channel C) DDR3L-RS Sign	nals (Sheet 2 of 2)
Signal Name	Direction Type	Description
DDR3_M0_DQ[63:0	I/O DDR3	Data Lines: Bidirectional signals between DRAM/PHY
DDR3_M0_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DDR3_M0_DQS[7:0 DDR3_M0_DQS[7:0		Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DDR3_M0_ODT[1,0	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
DDR3_M0_RCOMPD	I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board. This signal is driven from external clock source.
DDR3_M0_OCAVRE	F O DDR	Reference Voltage: DDR3 CA interface Reference Voltage
DDR3_M0_ODQVRE	F O DDR	Reference Voltage: DDR3 DQ interface Reference Voltage
DDR3_CORE_PWR0	DK I DDR	Core Power OK: This signal indicates the status of the DRAM Core power supply (power on in S0). Active high signal indicates that DDR PHY voltage(1.5v) is good.
DDR3_VDD_S4_PW	YROK I DDR	VDD Power OK: Asserted once the VRM is settled.
DDR3_M0_DRAMRS	ST_N 0	DRAM Reset: This signal is used to reset DRAM devices.
DDR3_VDD_S4_PW DDR3_M0_DRAMRS ble 56. Memory Channel 1	L DDR3L-RS Sig	nals (Sheet 1 of 2)
Signal Name	Direction Type	Description
DDR3_M1_CK[1,0]_ P 0	Clock PAD: (1 pair per Rank) Driven by PHY to

Table 56. Memory Channel 1 DDR3L-RS Signals (Sheet 1 of 2)

Juna	Signal Name	Direction Type	Description	defined
	DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.	d linds
ined un	DDR3_M1_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.	
d under.	DDR3_M1_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.	
defined	DDR3_M1_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.	41
ed un	DDR3_M1_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.	adefined
	ndefine		defined	led min
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sed unoc	۵ لا	Indeill.	ndefine	
4. Efilt	ineo.		od n.	



defined undefined undefined Table 56. Memory Channel 1 DDR3L-RS Signals (Sheet 2 of 2)

nden	Signal Name	Direction Type	Description
	DDR3_M1_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands
ined uno	DDR3_M1_CAS_N	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands
adefined undefined und	DDR3_M1_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
	DDR3_M1_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/PHY
, un	DDR3_M1_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
indefined undefined	DDR3_M1_DQS[7:0]_P DDR3_M1_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of DDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
	DDR3_M1_ODT[1,0]	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
	DDR3_M1_DRAMRST_N	0	Reset DRAM: This signal can be used to reset DRAM devices.

DDR3L-RS Interface Signals

Table 57. Memory Channel 0 DDR3L-RS Signals (Sheet 1 of 2)

Signal Name	Direction Type	Description			
DDR3_M0_CK[1,0]_P DDR3_M0_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.			
DDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.			
DDR3_M0_CKE[3,0] O DDR3		Clock Enable: (power management) Driven by PHY to DRAM.			
DDR3_M0_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.			
DDR3_M0_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.			
DDR3_M0_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands			

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ODDR3 I/O DDR3	Description Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
O DDR3 O DDR3 I/O	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
O DDR3 O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
O DDR3	DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
DDR3	DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
	B. I. Burner I Committee C
	Data Lines: Bidirectional signals between DRAM/PHY
O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS
I/O DDR3	Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
O DDR3	On Die Termination: ODT signal going to DRAM ir order to turn ON the DRAM ODT during Write.
I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board. This signal is driven from external clock source.
O DDR	Reference Voltage: DDR3 CA interface Reference Voltage
O DDR	Reference Voltage: DDR3 DQ interface Reference Voltage
I DDR	Core Power OK: This signal indicates the status of the DRAM Core power supply (power on in S0). Active high signal indicates that DDR PHY voltage(1.5v) is good.
I DDR	VDD Power OK: Asserted once the VRM is settled.
	DRAM Reset: This signal is used to reset DRAM devices.
	I/O DDR3 O DDR3 I DDR O DDR O DDR I DDR I DDR

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ned Ur	eined und	indefin.
''',	efinec	ined II.
Table 58. Memory Channel 1 DDI	R3L-RS Sign	als inde ^{itr}
Signal Name	Direction Type	Description
DDR3_M1_CK[1,0]_P DDR3_M1_CK[1,0]_N	O DDR3	Clock PAD: (1 pair per Rank) Driven by PHY to DRAM.
DDR3_M1_CS[1,0]_N DDR3_M1_CKE[3,0] DDR3_M1_MA[15:0] DDR3_M1_BS[2:0]	O DDR3	Chip Select: (1 per Rank). Driven by PHY to DRAM.
DDR3_M1_CKE[3,0]	O DDR3	Clock Enable: (power management) Driven by PHY to DRAM.
DDR3_M1_MA[15:0]	O DDR3	Memory Address: Driven by PHY to DRAM.
DDR3_M1_BS[2:0]	O DDR3	Bank Select: Driven by PHY to DRAM.
DDR3_M1_RAS_N	O DDR3	Row Address Select: Used with DDR3_M0_CAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the DRAM Commands
DDR3_M1_CAS_N DDR3_M1_WE_N DDR3_M1_DQ[63:0]	O DDR3	Column Address Select: Used with DDR3_M0_RAS# and DDR3_M0_WE# (along with DDR3_M0_CS#) to define the SRAM Commands
DDR3_M1_WE_N	O DDR3	Write Enable Control Signal: Used with DDR3_M0_WE# and DDR3_M0_CAS# (along with control signal, DDR3_M0_CS#) to define the DRAM Commands.
DDR3_M1_DQ[63:0]	I/O DDR3	Data Lines: Bidirectional signals between DRAM/PHY
DDR3_M1_DM[7:0]	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DDR3_M1_DQS[7:0]_P DDR3_M1_DQS[7:0]_N	I/O DDR3	Data Strobes: The data is captured at the crossing point of DDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DDR3_M1_ODT[1,0]	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
DDR3_M1_DRAMRST_N		

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defined undefined undefineu ndefined undefined **LPDDR3 Interface Signals** 8.1.3

Table 59. Memory Channel 0 LPDDR3 Signals

Table 39.	Memory Channel 0 LPDI	DK3 Signal	5	46,111
	Signal Name	Direction Type	Description	unde
defined undefined une	LPDDR3_M0_CK_P_A/B LPDDR3_M0_CK_N_A/B	O DDR3	SDRAM and inverted Differential Clock: (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.	
defines	LPDDR3_M0_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Used to qualify the command on the command bus for a particular rank.	ed u
ined unde	LPDDR3_M0_CKE[1,0]_ A/B	O DDR3	Clock Enable: (power management) It is used during DRAM power up/power down and Self refresh. NOTE: LPDDR3 uses only LPDDR3_M0_CKE[2,0]. LPDDR3_M0_CKE[1,3] are not being used for LPDDR3.	undefil.
ndefined undefined unde	LPDDR3_M0_CA[9:0]	O DDR3	Memory Address: Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol w.r.t. LPDDR3_M0_CKN, LPDDR3_M0_CKP pairs	Α'
	LPDDR3_M0_DQ[31:0]_ A/B	I/O DDR3	Data Lines: Data signal interface to the DRAM data bus	defines
i afined und	LPDDR3_M0_DM[3:0]_A /B	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.	d une
undefined undefined und	LPDDR3_M0_DQS[3:0]_ P_A/B LPDDR3_M0_DQS[3:0]_ N_A/B	I/O DDR3	Data Strobes: The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	sined.
	LPDDR3_M0_ODT_A/B	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	d nuge,
sined un	LPDDR3_M0_RCOMPD	I DDR	Resistor Compensation: This signal needs to be terminated to VSS on board. This signal is driven from external clock source.	
ed under	LPDDR3_M0_OCAVREF	O DDR	Reference Voltage: LPLPDDR3 CA interface Reference Voltage	
undefined undefined un	LPDDR3_M0_ODQVREF	O DDR	Reference Voltage: LPLPDDR3 DQ interface Reference Voltage	
Datasheet	ndefined uno		Reference Voltage: LPLPDDR3 DQ interface Reference Voltage	ned undefine
Datasheet		ed'	iur, iudei.	113
Datasheet	ر ر	ndefine	adefineo	
Jefill .	ined		ad un.	



idefined undefined undefined Table 60. Memory Channel 1 LPDDR3 Signals

	Signal Name	Direction Type	Description
ndefined undefined u	LPDDR3_M1_CK_P_A/B LPDDR3_M1_CK_N_A/B	O DDR3	SDRAM and inverted Differential Clock: (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.
ed unde.	LPDDR3_M1_CS[1,0]_N	O DDR3	Chip Select: (1 per Rank). Used to qualify the command on the command bus for a particular rank.
ndefine	LPDDR3_M1_CKE[1,0]_ A/B	O DDR3	Clock Enable: (power management) It is used during DRAM power up/power down and Self refresh. NOTE: LPDDR3 uses only LPDDR3_M1_CKE[0,2]. LPDDR3_M1_CKE[1,3] are not being used for LPDDR3.
undefined undefined h	LPDDR3_M1_CA[9:0]	O DDR3	Memory Address: Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol relative to LPDDR3_M1_CKN, LPDDR3_M1_CKP pairs
eined um	LPDDR3_M1_DQ[31:0]_ A/B	I/O DDR3	Data Lines: Data signal interface to the DRAM data bus.
Indeir	LPDDR3_M1_DM[3:0]_A /B	O DDR3	Data Mask: DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
undefined undefined	LPDDR3_M1_DQS[3:0]_ P_A/B LPDDR3_M1_DQS[3:0]_ N_A/B	I/O DDR3	Data Strobes: The data is captured at the crossing point of LPDDR3_M1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
fined U.	LPDDR3_M1_ODT_A/B	O DDR3	On Die Termination: ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
nuge.	LPDDR3_M1_OCAVREF	O DDR	Reference Voltage: LPDDR3 CA interface Reference Voltage
	LPDDR3_M1_ODQVREF	O DDR	Reference Voltage: LPDDR3 DQ interface Reference Voltage

ECC Support

The system memory controller supports ECC. When ECC is enabled, only Memory Channel 0 will be active. Memory Channel 1 will be disabled and used for the ECC data pins. The table below shows the details on the muxing relationship between the ECC Signals and the Memory Channel 1 signals.

Note: ECC SO-DIMMs are not backwards compatible with non-ECC SO-DIMMs.



Table 62. ECC Signals

Vo.	Signal Name	Direction Type	Description
¢.	DDR3_M0_ECC_DQ[7:0]	I/O	ECC Check Data Bits
"de		DDR3	These are muxed with channel 1.
defined undefined un	DDR3_M0_ECC_DM	O DDR3	ECC Data Mask: DM is an optional output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of ECC_DQS. This signal is muxed with channel 1 and may not be needed.
ined unde	DDR3_M0_ECC_DQSP DDR3_M0_ECC_DQSN	I/O DDR3	ECC Data Strobes: The data is captured at the crossing point the 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window. These are muxed with channel 1.

8.2 Features

8.2.1 System Memory Technology Supported

The system memory controller supports the following DDR3L-RS/LPDDR3 Data Transfer Rates, DRAM Device Technologies:

- DDR3L-RS/LPDDR3 Data Transfer Rates: 1600MT/s (12.8 GB/s per channel).
- LPDDR3 (1.2V DRAM VDDQ)
- DDR3L-RS (1.35V DRAM interface I/Os)
- DDR3L-RS DRAM Device Technology
 - Standard 2 Gb technologies and addressing
 - Read latency 5, 6, 7, 8, 9, 10, 11, 12, 13
 - Write latency 3, 4, 5, 6, 7, 8
- LPDDR3 DRAM Device Technology
 - x64, 253 ball LPDDR3 DRAM package
 - 8 GB (2 rank per channel) package density
 - Standard 2 Gb, 4 Gb and 8 Gb DRAM technologies and addressing
 - Read latency 5, 6, 7, 8, 9, 10, 11, 12, 13
 - Write latency 3, 4, 5, 6, 7, 8
- Supports Trunk Clock Gating
- ECC supports 64-bit data bus on DDR3L-RS single channel
- Supports early SR exit
- Supports slow power down
- Supports CA tri-state when not driving a valid command



Table 63. Supported LPDDR3 DRAM Devices

DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size	
2Gb	x32	8	BA[2:0]	A[13:0]	A[8:0]	2KB	
4Gb	x32	8	BA[2:0]	A[13:0]	A[9:0]	4KB	
8Gb	x32	8	BA[2:0]	A[14:0]	A[9:0]	4KB	

Table 64. Supported DDR3L-RS DRAM Devices

	DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
Ī	2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB

Table 65. Supported DDR3L-RS DRAM Devices

DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB

Table 66. Supported LPDDR3 Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
512MB	2	2Gb	x32	4KB = 2KB * 2 chips
1GB	2	4Gb	x32	8KB = 4KB * 2 chips
2GB	2	8Gb	x32	8KB = 4KB * 2 chips

Table 67. Supported DDR3L-RS Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
1GB	4	2Gb	x16	8KB = 2KB * 4 chips

8.3 Register Map

For more information on System Memory Controller registers, refer $Intel^{\circledR}$ Atom $^{\intercal M}$ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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9 Graphics, Video and Display

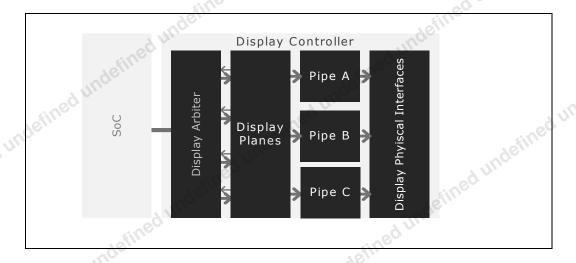
This chapter provides an overview of Graphics, Video and Display features of the SoC.

9.1 Features

The key features of the individual blocks are as follows:

- Refreshed eight generation Intel graphics core with sixteen Execution Units (EUs)
 - 3D graphics hardware acceleration including support for DirectX*11.1, OpenGL
 4.3, OGL ES 3.0, OpenCL 1.2.
 - Video decode hardware acceleration including support for H.263, MPEG4, H.264,
 H.265 (HEVC), VP8, VP9, MVC, MPEG2, VC1, JPEG.
 - Video encode hardware acceleration including support for H.264, H.263, VP8, MVC, JPEG.
 - Display controller, incorporating the display planes, pipes and physical interfaces.
 - Four planes available per pipe 1x Primary, 2x Video Sprite & 1x Cursor.
 - Three multi-purpose Digital Display Interface (DDI) PHYs implementing HDMI,
 DVI, DisplayPort (DP) or Embedded DisplayPort (eDP) support.
 - Two dedicated digital Display Serial Interface PHYs implementing MIPI-DSI support.

9.2 SoC Graphics Display



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The Processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Display Physical Interfaces

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on a display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

9.2.1 Primary Planes A, B and C

Planes A, B and C are the main display planes and are associated with Pipes A, B and C respectively. Each plane supports per-pixel alpha blending.

9.2.2 Video Sprite Planes A, B, C, D, E and F

Video Sprite Planes A, B, C, D, E and F are planes optimized for video decode.

- Pipe A Primary planeA, VSpriteA, VSpriteB, CusrorA
- Pipe B Primary planeB, VSpriteC, VSpriteD, CursorB
- Pipe C Primary planeC, VSpriteE, VSpriteF, CursorC

9.2.3 Cursors A, B and C

Cursors A, B and C are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A, B and C respectively.

9.3 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed.

The display pipes A, B and C operate independently of each other at the rate of one pixel per clock. They can attach to any of the display interfaces.

9.4 Display Physical Interfaces

The display physical interfaces consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device. These interfaces are digital (MIPI-DSI, DisplayPort*, Embedded DisplayPort*, DVI and HDMI*) interfaces.



Figure 9. Display Pipe to Port Mapping

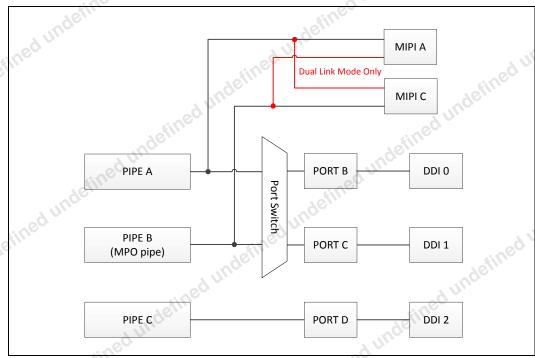
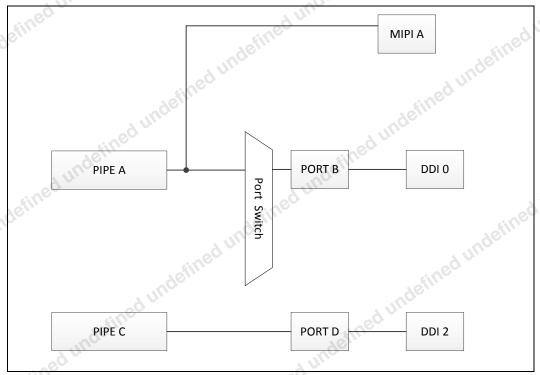


Figure 10. Display Pipe to Port Mapping [T3]





PIPE A

PORT B

DDI 0

PIPE C

PORT D

DDI 2

Figure 11. Display Pipe to Port Mapping [T3]

9.4.1 Digital Display Interfaces

Table 68. SoC Display Configuration (Sheet 1 of 2)

Feature	MIPI DSI	eDP	DP nde	HDMI/DVI
Number of Ports	2	2	2	2
deill	(x4 @ 1Gbps)	(x4 @2.7Gbps)	(x4 @2.7GHz)	(x4 @2.97GHz)
Max Resolution	2560x1600	2560x1600	2560x1600	1920x1080
ndefined	24bpp @60Hz	24bpp @60Hz	24bpp @60Hz	24bpp @120Hz/ 3840x2160 24bpp @ 30Hz
Standard	DSI1.01/ DPHY1.00	eDP1.3	DP1.1a	HDMI1.4b
Power gated during S0ix w/display off	Yes	Yes	Yes	Yes
DRRS (Refresh reduction)	Yes (M/N pair)	Yes (Panel command)	N/A	N/A
Self-Refresh with Frame buffer in Panel	Yes (Command Mode)	Yes (PSR)	No	No



defined undefined undefined **SoC Display Configuration (Sheet 2 of 2)** Table 68.

	Feature	MIPI DSI	eDP	DP DP	HDMI/DVI		
	Content-Based backlight control	DPST6.0/CABC	DPST6/CABC	N/A	N/A		
sined undef	HDCP wired display	N/A	N/A(ASSR support)	1.4	1.4		
	HDCP wireless display	N/A	N/A(ASSR support)	2.2	2.2		
nder.	PAVP	AVP AES-encrypted buffer, plane control, panic attack					
od uli	SEC	All display registers can be accessed by CEC					
indefined undefined un	LPE Audio	N/A	N/A	Yes	Yes		
	Compressed Audio	N/A	N/A	Yes	Yes		
	4 Ulive		inde				

Table 69. SoC Display supported Resolutions

ed ui		1 Dis	splay uno	2 Dis	splays	3 Displays	
undefined undefined un.		1 Internal	1 External	1 Internal +1 External	2 External	1 Internal +2 External	
	Internal #1	eDP* 2560x1600 @ 60Hz or MIPI DSI* 2560x1600 @60Hz	N/A	eDP* 2560x1600 @ 60Hz or MIPI DSI* 2560x1600 @60Hz	N/A	eDP* 2560x1600 @ 60Hz or MIPI DSI* 2560x1600 @60Hz	undefined u
undefined undefined uni	External #1	N/A	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz	N/A	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz	.zed ^v
	sined un	N/A	N/A	N/A	HDMI/DP* 3840×2160 @ 30Hz 2560×1600 @ 60Hz	HDMI/DP* 3840x2160 @ 30Hz 2560x1600 @ 60Hz	d undefin.
ed undefined undefined un	NOTES: 1. SoC is supprextended m 2. Experience	nodes.		. ,	External display , and work loads	in both clone and	adefined

NOTES:

- 1. SoC is supported maximum of 3 simultaneous displays. External display in both clone and extended modes.
- , and undefined undefined undefined 2. Experience may differ based on configuration, resolution, and work loads.

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9.4.1.1 **Signal Descriptions**

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 71. Display Physical Interfaces Signal Names (2 of 2)

Signal names	Direction Type	Description	fined un.
MDSI_A_CLKP	0	MIPI Clock output for port A	"uge,
MDSI_A_CLKN	0	MIPI Clock complement output for port A	90.
MDSI_A_DP[3:0]	I/O	MIPI Data Lane 3:0 for port A	
MDSI_A_DN[3:0]	I/O	MIPI Data Lane 3:0 complement for port A	
MDSI_C_CLKP	0	MIPI Clock output for port C	
MDSI_C_CLKN	0,00	MIPI Clock complement output for port C	
MDSI_C_DP[3:0]	I/O	MIPI Data Lane 3:0 for port C	.,0
MDSI_C_DN[3:0]	I/O	MIPI Data Lane 3:0 complement for port C	ed ui
MDSI_A_TE	I/O	Tearing Effect Signal from x4 port A display	iefine
MDSI_C_TE	I	Tearing Effect Signal from x4 port C display	INOC
MDSI_DDC_DATA	I/O	DDC Data	9
MDSI_DDC_CLK	I/O	DDC Clock	
MDSI_RCOMP	I/O	MDSI_RCOMP: This is for pre-driver slew rate compensation for the MIPI DSI Interface. An external precision resistor of 150 Ω ±1% should be connected from this pin to ground.	
	MDSI_A_CLKP MDSI_A_CLKN MDSI_A_DP[3:0] MDSI_A_DN[3:0] MDSI_C_CLKP MDSI_C_CLKN MDSI_C_DP[3:0] MDSI_C_DN[3:0] MDSI_C_DN[3:0] MDSI_A_TE MDSI_C_TE MDSI_DDC_DATA MDSI_DDC_CLK	MDSI_A_CLKP	Signal namesTypeDescriptionMDSI_A_CLKP0MIPI Clock output for port AMDSI_A_CLKN0MIPI Clock complement output for port AMDSI_A_DP[3:0]I/OMIPI Data Lane 3:0 for port AMDSI_A_DN[3:0]I/OMIPI Data Lane 3:0 complement for port AMDSI_C_CLKP0MIPI Clock output for port CMDSI_C_CLKN0MIPI Clock complement output for port CMDSI_C_DP[3:0]I/OMIPI Data Lane 3:0 for port CMDSI_C_DN[3:0]I/OMIPI Data Lane 3:0 complement for port CMDSI_A_TEI/OTearing Effect Signal from x4 port A displayMDSI_C_TEITearing Effect Signal from x4 port C displayMDSI_DDC_DATAI/ODDC DataMDSI_DDC_CLKI/ODDC ClockMDSI_RCOMP: This is for pre-driver slew rate compensation for the MIPI DSI Interface. An external precision resistor of 150 Ω ±1% should be

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9.4.1.2.1

Dual Link interface supports display resolution up to 2560 x 1600p @ 60 Hz with 24b per pixel.

Interface supports maximum of 1Gbps per land



Full Frame Buffer Panel

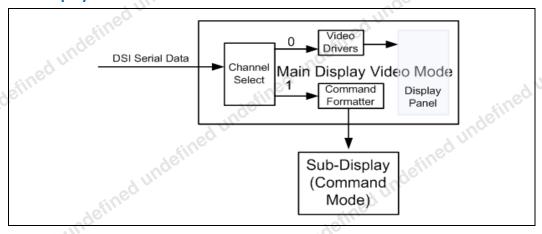
The display controller supports full frame buffer display (also called command-mode display) with optimizations for both SoC power consumption and system power consumption. Full frame buffer panel does not need to be refreshed regularly by a frame buffer in system memory so the path between panel and system memory can be power-managed as much as possible until a new request occurs to update one or more planes that are active in the display pipe.

Sub-Display Support

The display controller supports a sub-display panel that uses a different virtual channel and shares the same interface with the main panel. The pixel data for this sub-display can come from a direct system memory read or it can come from the output at the pipe as described. Sub-display allows, for example, the pixel stream to be updated more frequently or presented in a format and/or resolution that would require software to convert or scale the panel resolution.

One example usage of sub-display is as a view finder for camera. The camera interface unit may output images in a format and resolution that are not read by the sub-display itself or must be blended with camera application graphics.

Figure 12. Sub-Display Connection



Partial Display Mode Support

The display controller supports a partial display mode that utilizes the MIPI command set to transition the panel from normal mode to partial display mode, so a small part of the display panel can be kept active for pixel data. The same panel can switch from full screen mode to a sub-display mode with a handful of scan lines to show time, date, signal strength indicator, etc., to save power for the host processor and display panel.

There are two scenarios:

 Type 1 display panel—both full display and partial display operates in command mode.



Type 2 display panel—full display (normal mode) operate in video mode; partial
display operates in command mode. This requires the host processor and display
panel to be in sync in transition from normal mode to partial mode after 2 frames
from the enter_partial_mode command.

The software driver must implement most of the protocols of transition and send the correct commands to the display panel to start the transition. The software driver must program the display controller to select the buffer for partial display (display pipe output or system memory) and follow the protocol to be in sync with the display panel.

When the display transitions from partial mode to normal mode, it is recommended to turn the display off to avoid tearing effect as in a flow chart in DCS specification.

MIPI DSI Dual-link Mode

The SoC supports MIPI DSI dual-link mode, so that a single display can transmit a single stream of video data across two independent MIPI DSI interfaces. The packetization and timing of each link follows MIPI DSI 1.00 and DPHY 1.00 precisely, but the receiving device, which is a panel or a bridge, can combine the streaming data from two interfaces and display it in a single panel.

There are two types of dual-link panels that the SoC can support:

- Front-back type of panel, the first half of columns of pixels is always transmitted by port A and the second half of columns of pixels is always transmitted by port B.
- Pixel alternative type of panel, odd columns of pixels are always transmitted by port A and even columns of pixels are always transmitted by port B. So the 1st, 3rd, 5th, 7th, etc., pixels are separated at the source and sent in the first interface; the 2nd, 4th, 6th, 8th, etc., pixels are sent in the second interface. When the platform requires a dual-link interface for a large MIPI DSI panel or bridge (usually with resolution larger than 1920x1080 in which a 4-lane interface does not have enough bandwidth), the driver treats dual-link a special port configuration, with special handling of DSI controller but the operation of dual-link mode is consistent with single-link mode for planes and pipe operations. The system interface with upper level of SW does not need to change, like flip mechanism, interrupt, and so on.

LVDS Panel Support

An external MIPI DSI-to-LVDS bridge device is required to connect the display controller to a LVDS panel. A bridge device is used for larger panels.

9.4.1.3 High Definition Multimedia Interface

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multichannel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the SoC and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.



HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the SoC). As shown in Figure 13, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the SoC are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

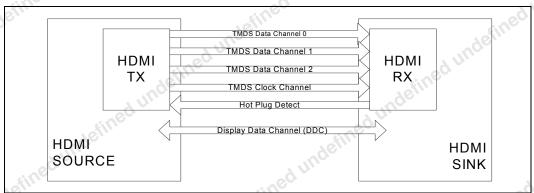
The SoC HDMI interface is designed as per the High-Definition Multimedia Interface Specification 1.4. The SoC supports High-Definition Multimedia Interface Compliance Test Specification 1.4.

9.4.1.3.1 Stereoscopic Support on HDMI

SoC display supports HDMI 1.4 3D video formats. If the HDMI panel is detected to support 3D video format then the SW driver will program Pipe2dB for the correct pipe timing parameters.

The left and right frames can be loaded from independent frame buffers in the main memory. Depending on the input S3D format, the display controller can be enabled do perform frame repositioning, image scaling, line interleaving.

Figure 13. HDMI Overview



9.4.1.4 Display Port

Display Port is a digital communication interface that utilizes differential signalling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

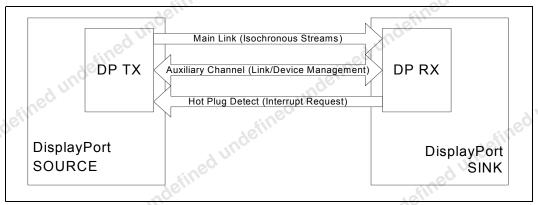
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A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The SoC supports DisplayPort Standard Version 1.2.

Figure 14. DisplayPort* Overview



9.4.1.5 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is a embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. eDP is supported only on Digital Display Interfaces 0 and/or 1. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

Each eDP port can be configured for up-to 4 lanes.

The SoC supports Embedded DisplayPort Standard Version 1.3.

9.4.1.5.1 DisplayPort Auxiliary Channel

A bidirectional AC coupled AUX channel interface replaces the $\rm I^2C$ for EDID read, link management and device control. $\rm I^2C$ -to-Aux bridges are required to connect legacy display devices.

9.4.1.5.2 Hot-Plug Detect (HPD)

SoC supports HPD for Hot-Plug sink events on the HDMI and DisplayPort interfaces.

9.4.1.5.3 Integrated Audio over HDMI and DisplayPort

SoC can support two audio streams on DP/HDMI ports. Each stream can be programmable to either DDI port. HDMI/DP audio streams can be sent with video streams as follows.



LPE mode: In this mode the uncompressed or compressed audio sample buffers are generated either by OS the audio stack or by audio Lower Power Engine (LPE) and stored in system memory. The display controller fetches audio samples from these buffers, forms an SPDIF frame with VUCP and preamble (if needed), then sends out with video packets.

High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TV). The SoC supports HDCP 1.4(wired)/2.2(wireless) for content protection over wired displays (HDMI, DisplayPort and Embedded DisplayPort).

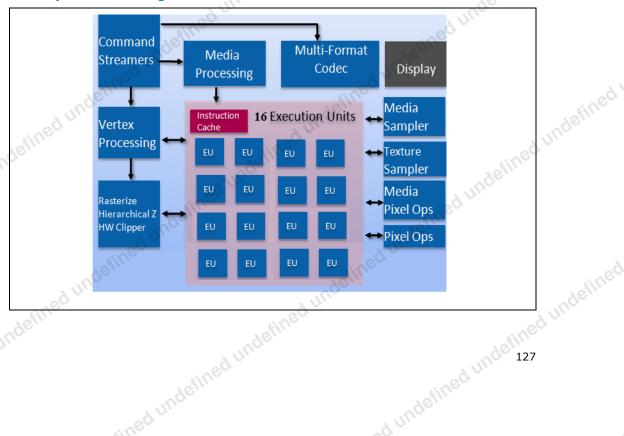
9.5 References

- High-Definition Multimedia Interface Specification, Version 1.4b
- High-bandwidth Digital Content Protection System, Revision 1.4
- VESA DisplayPort Standard, Version 1.2
- VESA Embedded DisplayPort Standard, Version 1.3

3D Graphics and Video

The SoC implements a derivative of the Generation 8 LP graphics engine which consists of rendering engine and bit stream encoder/decoder engine. The rendering engine is used for 3D rendering, media compositing and video encoding. The Graphics engine is built around sixteen execution units (EUs).

Figure 15. 3D Graphics Block Diagram





9.7 Features

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 8.0 LP 3D engine provides the following performance and power-management enhancements:

- Hierarchal-Z
- Video quality enhancements

9.7.1 3D Engine Execution Units

- The EUs perform 128-bit wide execution per clock
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing

9.7.2 3D Pipeline

9.7.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

9.7.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

9.7.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

9.7.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.



9.7.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

9.7.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

9.7.3 Video Engine

The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content. This engine supports Full HW acceleration for decode of AVC/H.264, VC-1 and MPEG -2 contents along with encode of MPEG-2 and AVC/H.264 apart from various video processing features. The new Processor Graphics Video engine adds support for processing features such as frame rate conversion, image stabilization and gamut conversion.

9.8 VED (Video Encode/Decode)

The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content.

9.8.1 Features

The features for the Video decode hardware accelerator in SoC are:

- VED core can be configured on a time division multiplex basis to handle single, dual and multi-stream HD decoding/encoding.
- VED provides full hardware acceleration Decode/Encode support below Media formats.

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undefined undefined undefined Table 72. Hardware Accelerated Video Decode/Encode Codec Support

AO						
uc	Encode Format	Profile	Level	Resolution	Bitrate (Mbps)	Frame Rate
	H.263			480p		30
ed uni	H.264	HP/BP/CBP	L5.1	4kx2k 1080p	100-130	30 120
ighthe	VP8		veg.	4kx2k		30
Inde	MVC	HP/BP/CBP	L4.2	1080p	File	60
ed to	JPEG	4 Un	1067Mpps (4	20), 800Mpps (42	22) @400Mhz	
Indefined undefined un	,nde	Hines		4efin	30,00	
1	D-A 2			100	Dituata	Fueres

	Decode Format	Profile	Level	Resolution	Bitrate (Mbps)	Frame Rate
lu ,	H.263		age,	480p		30
	MPEG4	SP	4011	480p		30
undefined undefined ur	H.264	НР,МР,СВР	L5.2	4Kx2K	200-250	60
4 Ullie		inde		1080P	16/11	240
	H.265(HEVC)	MP	L5	4Kx2K	uno	30
delli	VP8	Silve		4kx2k	160	30
n,	VP9			1080p		30
	MVC			4Kx2K		30
	MPEG2	MP	HL	1080p		60
ال ا	VC1	AP	L4	1080P		60
	JPEG		1067Mpps (4	20), 800Mpps (4	22) @400Mhz	unos

Register Map

For more information on Graphics, Video and Display registers refer Intel[®] Atom™ s of 2),

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Setting to the street with the st Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.



PCI Express 2.0

There are up to two PCI Express root ports, each supporting the PCI Express* Base Specification, Rev. 2.0 at a maximum 5 GT/s signaling rate. The root ports can be configured to support a diverse set of lane assignments.

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

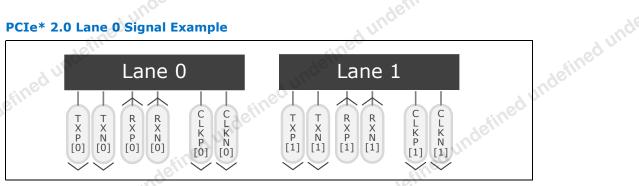
- **Signal Name:** The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Signals

undefined u	Signal Name	Direction /Type	Description
unos	PCIE_TXP[1:0] PCIE_TXN[1:0]	O PCIe	PCI Express* Transmit PCI Express* Ports 1:0 transmit pair (P and N) signals. Each pair makes up the transmit half of a lane.
aduni	PCIE_RXP[1:0] PCIE_RXN[1:0]	I PCIe	PCI Express* Receive: PCI Express* Ports 1:0 receive pair (P and N) signals. Each pair makes up the receive half of lane.
Jundefined undefined und	PCIE_CLKREQ[1:0]_N	IO	PCI Express* Clock Request Used for devices that need to request one of the output clocks. Each clock request maps to the matching PCIe Root Port (e.g. PCIE_CLKREQ#[0] maps to PCIE Root Port [0] and so on) NOTE: These signals are muxed and may be used by other functions.
	I P RCOMP P	I/O	These pins connected with 402 Ohm 1% between RCOMP pads.
d undefined undefined un	P_RCOMP_N	Indefined	RCOMP pads.
Datasheet	ndefine	undefiner	Jundefined undefined undefined



Figure 16. PCIe* 2.0 Lane 0 Signal Example



Features

- Conforms to PCI Express* Base Specification, Rev. 2.0.
- 5.0 or 2.5 GT/s operation per root port.
- Virtual Channel support for VC0 only.
- x1, x2 link widths (auto negotiated).
- Spread Spectrum Clocking (SSC) is supported for PCIe Gen1 components.
- Flexible Root Port configuration options
 - -(1) x2's
 - (2) x1
- Interrupts and Events
 - Legacy (INTx) and MSI Interrupts
 - General Purpose Events
 - Express Card Hot Plug Events
 - System Error Events
- Power Management
 - Link State support for ASPM(LOs, L1), L1 sub states (L1.SNOOZ,L1.OFF), L23_RDY,L2 and L3.
 - Powered down in ACPI S3 state L3.

Intel recommends disabling Spread Spectrum Clocking (SSC), if PCIe Gen2 based Note: component is used.

10.2.1 **Root Port Configurations**

Depending on SKU, there are up to two possible lane assignments for root ports 1-2.

Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(2) x1". Links for each root port will train automatically to the maximum ii. - A undefined undefined possible for each port.

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x2 link widths are not common. Most devices will only train to x1 Note:

PCI functions in PCI configuration space are disabled for root ports not available. Note:

Interrupts and Events 10.2.2

A root port is capable of handling interrupts and events from an end point device. A root port can also generate its own interrupts for some events, including power management and hot plug events, but also including error events.

There are two interrupt types a root port will receive from an end point device: INTx (legacy), and MSI. MSI's are automatically passed upstream by the root port, just as other memory writes would be. INTx messages are delivered to the Legacy block's interrupt router/controller by the root port.

Events and interrupts that are handled by the root port are shown with the possible interrupts they can deliver to the interrupt decoder/router.

Table 74. **Possible Interrupts Generated From Events/Packets**

indefined undefinee	Packet/Event	Туре	INTx	MSI	SERR	SCI	SMI	GPE
inde	INTx	Packet	Х	Х		717	0	
ined c	PM_PME	Packet	Х	Х		"UQe,		
defill	Power Management (PM)	Event	Х	Х	60	Х	Х	
	Hot Plug (HP)	Event	Х	Х		Х	Х	
	ERR_CORR	Packet		, uno	Х			
	ERR_NONFATAL	Packet	-::0	30	Х			
uno	ERR_FATAL	Packet	geilli		Х			Silve
ned to	Internal Error	Event			Х			90
defill	VDM	Packet					69 0	Х
undefines	NOTE: Above table lists the posor events generated in the different interrupts as a When INTx interrupts are resistent upts and sent to the interrupts are sent to the interrupts and sent to the interrupts are sent to the interrupts and sent to the interrupts are s	the root p pplicable. eceived b	ort. Confi	guration	needed by	y software mapped	e to enabl	e the

When INTx interrupts are received by an end point, they are mapped to the following interrupts and sent to the interrupt decoder/router in the iLB.

Interrupt Generated for INT[A-D] Interrupts

	INTA	INTB	INTC	INTD
Root Port 1	INTA#	INTB#	INTC#	INTD#
Root Port 2	INTD#	INTA#	INTB#	INTC#

NOTE: Interrupts generated from events within the root port are not swizzled.

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10.2.2.1 Express Card Hot Plug Events

Express Card Hot Plug is available based on Presence Detection for each root port.

Note: A full Hot Plug Controller is not implemented.

Presence detection occurs when a PCI Express* device is plugged in and power is supplied. The physical layer will detect the presence of the device, and the root port will set the SLSTS.PDS and SLSTS.PDC bits.

When a device is removed and detected by the physical layer, the root port will clear the SLSTS.PDS bit, and set the SLSTS.PDC bit.

Interrupts can be generated by the root port when a hot plug event occurs. A hot plug event is defined as the transition of the SLSTS.PDC bit from 0 to 1. Software can set the SLCTL.PDE and SLTCTL.HPE bits to allow hot plug events to generate an interrupt.

If SLCTL.PDE and SLTCTL.HPE are both set, and STSTS.PDC transitions from 0 to 1, an interrupt will be generated.

10.2.2.2 System Error (SERR)

System Error events are support by both internal and external sources. Refer the PCI Express* Base Specification, Rev. 2.0 for details.

10.2.3 Power Management

Each root port's link supports L0s, L1, and L2/3 link states per PCI Express* Base Specification, Rev. 2.0. L2/3 is entered on entry to S3.

10.3 References

PCI Express* Base Specification, Rev. 2.0

10.4 Register Map

For more information on PCI Express* 2.0 registers refer Intel[®] Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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11 MIPI-Camera Serial Interface (CSI) and ISP

MIPI CSI and controller front end interfaces with three sensors and is capable of simultaneously acquiring three streams, one from each sensor. These three streams are presented to the ISP.

11.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- Signal Name: The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 76. CSI Signals

Signal Name	Direction	Description
MCSI1_CLKP/N	I	Clock Lane: MIPI CSI input clock lane 0 for port 1.
MCSI1_DP/N[3:0]	I	Data Lanes: Four MIPI CSI Data Lanes (0-3) for port 1. Lanes 2 and 3 can optionally used as data lanes for port 3.
MCSI2_CLKP/N	I	Clock Lane: MIPI CSI input clock lane 0 for port 2.
MCSI2_DP/N[1:0]	I	Data Lane: Two MIPI CSI Data Lanes for port 2.
MCSI3_CLKP/N	I	Clock Lane: MIPI CSI input clock lane 0 for port 3.
MCSI_RCOMP	I/O	Resistor Compensation: This is for pre-driver slew rate compensation for the MIPI CSI Interface.

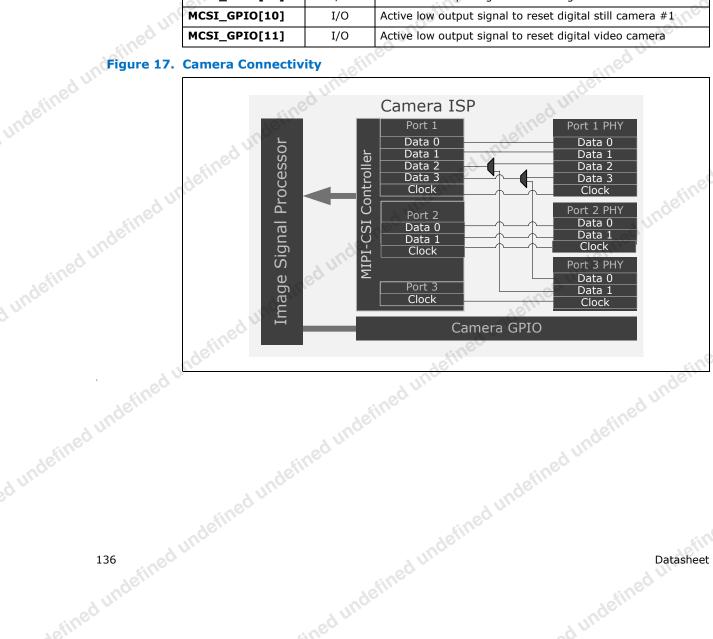
..../N ISI2_DP/N[1:0] I MCSI3_CLKP/N I MCSI_RCOMP I/O Table 77. GPIO Signals (Sheet 1 of 2)

ofined undefined un	Signal Name	Direction /Type	Description
	MCSI_GPIO[00]	I/O	Output from shutter switch when its pressed halfway. This switch state is used to trigger the Auto focus LED for Xenon Flash or Torch mode for LED Flash
	MCSI_GPIO[01]	I/O	Output from shutter switch when its pressed full way. This switch state is used to trigger Xenon flash or LED Flash
	MCSI_GPIO[02]	I/O	Active high control signal to Xenon Flash to start charging the Capacitor
d unde	MCSI_GPIO[03]	I/O	Active low output from Xenon Flash to indicate that the capacitor is fully charged and is ready to be triggered
	ined to		- A Unit



GPIO Signals (Sheet 2 of 2) Table 77.

IIILEI			under indefinition and similar	
Table 77.	GPIO Signals (She	eet 2 of 2)	indefined un	
ndefil.	Signal Name	Direction /Type	Description	ined une
	MCSI_GPIO[04]	I/O	Active high Xenon Flash trigger / Enables Torch Mode on LED Flash IC	indefil.
d uni	MCSI_GPIO[05]	I/O	Enables Red Eye Reduction LED for Xenon / Triggers STROBE on LED Flash IC /	
indefined	MCSI_GPIO[06]	I/O	Camera Sensor 0 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.	
adefined L	MCSI_GPIO[07]	I/O	Camera Sensor 1 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.	d un
71.	MCSI_GPIO[08]	I/O	Active high signal to video camera to power down the device.	definect
	MCSI_GPIO[09]	I/O	Active low output signal to reset digital still camera #0.	nue
7).	MCSI_GPIO[10]	I/O	Active low output signal to reset digital still camera #1	1
ined th	MCSI_GPIO[11]	I/O	Active low output signal to reset digital video camera]





11.2 **Features**

- Integrated MIPI-CSI 2.0 interface.
- Image Signal Processor (ISP) with DMA and local SRAM.
- Imaging data is received by the MIPI-CSI interface and is relayed to the ISP for processing.
- Up to six MIPI-CSI 2.0 data lanes.
 - Each lane can operate at up to 1.5Gbp/s. resulting in roughly 1.2 Gbp/s of actual pixels.
- The MIPI-CSI interface supports lossless compressed image streams to increases the effective bandwidth without losing data.
- Up to 13MP sensors supported, and full HD 1080p30
 - Can also support Stereo HD 1080p30.

Imaging Capabilities 11.2.1

The following table summarizes imaging capabilities.

Table 78. **Imaging Capabilities**

inde	Feature	Capabilities
ined b	Sensor interface	Configurable MIPI-CSI2 interfaces.
under.	adefine	3 sensors: x2, x2, x2 or x1 x2, x3 2 sensors: x4, x2
fined und	Simultaneous sensors	Up to 3 simultaneous sensors
	2D Image capture	13MP ZSL @ 18fps
	2D video capture	Up to 1080p30
	Input formats	RAW 8, 10, 12, 14, RGB444, 565, 888, YUV420, 422, JPEG.
inde.	Output formats)	YUV422, YUV420, RAW
Jundefined under	Special Features	Image and video stabilization Low light noise reduction Burst mode capture
	ined under	Memory to memory processing 3A (Auto Exposure (AE), Auto White Balance (AWB) and Auto Focus (AF)) High Dynamic Range (HDR)
dun	Perr.	Multi-focus Zero shutter lag

11.2.2 Simultaneous Acquisition

SoC will support on-the-fly processing for only one image at a time. While this image is . A . indefined undefined undefined being processed on-the-fly, images from the other two cameras are saved to DRAM for later processing.

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11.2.3 Primary Camera Still Image Resolution

Maximum still image resolution for the primary camera in post-processing mode is limited by the resolution of the sensors. Currently 13Mpixel sensors are supported.

Higher resolution, or higher frame rates are supported as long as the product of resolution and frame rate does not exceed 235 Mpixels/s (= 13 Mpixels * 18 fps).

Maximum primary camera on-the-fly stereoscopic still image resolution for primary camera is 8 Mpixel for each of the left and right images at 18 fps. The number of Mpixels can be increased by decreasing the frame rate.

11.2.4 Burst Mode Support

The SoC supports capturing multiple images back to back at maximum sensor resolution. At least 5 images must be captured in burst mode. The maximum number of images that can be so captured is limited only by available system memory. These images need not be processed on-the-fly.

11.2.5 Continuous Mode Capture

SoC supports capturing images and saving them to DRAM in a ring of frame buffers continuously at maximum sensor resolution. This adds a round trip to memory for every frame and increases the bandwidth requirements.

11.2.6 Secondary Camera Still Image Resolution

Maximum secondary camera still image resolution is 4 Mpixel at 15 fps.

11.2.7 Primary Camera Video Resolution

Maximum primary camera video resolution is 1080p60.

Maximum primary camera dual video resolution is 1080p30.

11.2.8 Secondary Camera Video Resolution

Maximum secondary camera video resolution is 1080p30.

11.2.9 Bit Depth

Capable of processing 14-bit images at the stated performance levels.

Capable of processing 18-bit images at half the performance levels, i.e. process onthe-fly 13 Mpixel 18-bit images at 7 fps instead of 15 fps.

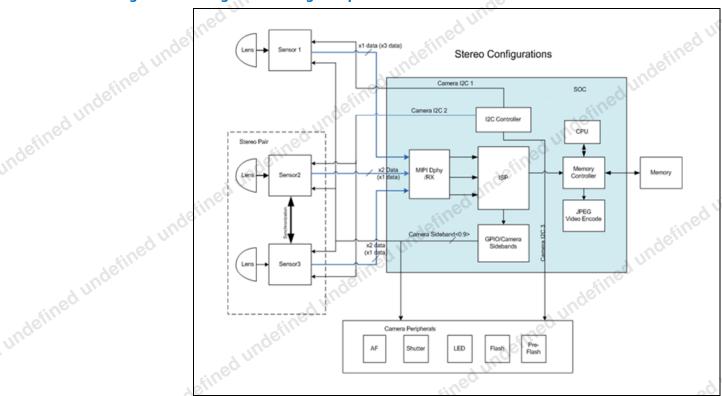
Capable of processing up to 18-bit precision.

The higher precision processing will be employed mainly for high dynamic range imaging (HDR).



Imaging Subsystem Integration 11.3

Figure 18. Image Processing Components



11.3.1 **CPU Core**

The CPU core augments the signal processing capabilities of the hardware to perform post-processing on images such as auto focus, auto white balance, and auto exposure. The CPU also runs the drivers that control the GPIOs and I²C for sensor control.

11.3.2 **Imaging Signal Processor (ISP)**

The ISP (Imaging Signal Processor) includes a 64-way vector processor enabling high quality camera functionality. Key features include support of three camera sensors.

MIPI-CSI-2 Ports 11.3.2.1

The SoC has three MIPI clock lanes and six MIPI data lanes. The Analog Front End (AFE) and Digital Physical Layer (DPHY) take these lanes and connects them to three virtual ports. Two data lanes are dedicated to each of the rear facing cameras and the . A undefined undefined remaining data lane is connected to the front facing camera. The MIPI interfaces follow the MIPI-CSI-2 specifications as defined by the MIPI Alliance. They support YUV420, YUV422, RGB444, RGB555, RGB565, and RAW 8b/10b/12b. Both MIPI ports support



compression settings specified in MIPI-CSI-2 draft specification 1.01.00 Annex E. The compression is implemented in Hardware with support for Predictor 1 and Predictor 2. Supported compression schemes:

- 12-8-12
- 12-7-12
- 12-6-12
- 10-8-10
- 10-7-10
- 10-6-10

The data compression schemes above use an X-Y-Z naming convention where X is the number of bits per pixel in the original image, Y is the encoded (compressed) bits per pixel and Z is the decoded (uncompressed) bits per pixel.

11.3.2.2 I²C for Camera Interface

The platform supports three (3) I^2C ports for the camera interface. These ports are used to control the camera sensors and the camera peripherals such as flash LED and lens motor.

11.3.2.3 Camera Sideband for Camera Interface

Twelve (12) GPIO signals are allocated for camera functions, refer Table 77 for signal names. These GPIOs are multiplexed and are available for other usages without powering on the ISP. The ISP provides a timing control block through which the GPIOs can be controlled to support assertion, de-assertion, pulse widths and delay. The configuration below of camera GPIOs is just an example of how the GPIOs can be used. Several of these functions could be implemented using $\rm I^2C$, depending on the sensor implementation for the platform.

- Sensor Reset signals
 - -Force hardware reset on one or more of the sensors.
- · Sensor Single Shot Trigger signal
 - —Indicate that the target sensor needs to send a full frame in a single shot mode, or to capture the full frame for flash synchronization.
- PreLight Trigger signal
 - —Light up a pilot lamp prior to firing the flash for preventing red-eye.
- Flash Trigger signal
 - Indicate that a full frame is about to be captured. The Flash fires when it detects an assertion of the signal.
- Sensor Strobe Trigger signal
 - —Asserted by the target sensor to indicate the start of a full frame, when it is configured in the single shot mode, or to indicate a flash exposed frame for flash synchronization.



11.4 Functional Description

At a high level, the Camera Subsystem supports the following modes:

- Preview
- Image capture
- Video capture

11.4.1 Preview

Once the ISP and the camera subsystem is enabled, the ISP goes into the preview mode where very low resolution frames, such as VGA/480p (programmable), are being processed.

11.4.2 Image Capture

During the image capture mode, the camera subsystem can acquire at a peak throughput of 13 Mpixels @ 18fps. While doing this, it continues to output preview frames simultaneously.

- The ISP can output RAW, RGB or YUV formats. The ISP can capture one full frame at a time or perform burst mode capture, where up to five full back-to-back frames are recorded.
- The ISP will not limit the number of back-to-back full frames captured, but the number is programmable and determined on how much memory can be allocated dynamically.
- The ISP can process all the frames on the fly and writes to memory only after fully
 processing the frames, without requiring download of any part of the frame for
 further processing.
 - —The exceptions to this approach are image stabilization and some other advanced functions requiring temporal information over multiple frames.

The ISP can support image stabilization in image capture model.

- The ISP initially outputs preview frames.
- When the user decides to capture the picture, image stabilization is enabled. The ISP checks the previous frame for motion and compensates for it appropriately.

Auto Exposure (AE), Auto Focus (AF), and Auto White Balance (AWB), together known as 3A, are implemented in the CPU to provide flexibility.

11.4.3 Video Capture

During video recording, the ISP can capture video up to 1080p @ 60 fps and output preview frames concurrently. The ISP output video frames to memory in YUV420 or YUV422 format.

11.4.4 ISP

The Camera subsystem consists of 2 parts, the hardware subsystem and a software stack that implements the ISP functionality on top of this hardware.

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The core of the ISP is a vector processor. The vector processor is supported by the following components:

- · Interfaces for data and control
- A small input formatter that parallelizes the data
- A scalar (RISC) processor, for system control and low-rate processing
- An accelerator for scaling, digital zoom, and lens distortion correction
- A DMA engine transfers large amounts of data such as input and output image data or large parameter sets between LPDDR2 and the ISP block.

11.4.5 Memory Management Unit (MMU)

The camera subsystem has capabilities to deal with a virtual address space, since a contiguous memory range in the order of 16–32MB cannot be guaranteed by the OS.

11.4.5.1 Interface

The MMU performs the lookup required for address translation from a 32-bit virtual address to 36-bit physical address. The lookup tables are stored external to the system. The MMU performs the lookup through a master interface without burst support that is connected to the Open Core Protocol (OCP) master of the subsystem. The MMU configuration registers can be accessed through a 32-bit Core I/O (CIO) slave interface. Additionally there is a 32-bit CIO slave interface connected to the address translator.

11.5 MIPI-CSI-2 Receiver

MIPI-CSI-2 devices are camera serial interface devices. They are categorized into two types, a CSI transmitter device with Camera Control Interface (CCI) slave and CSI receiver device with CCI master.

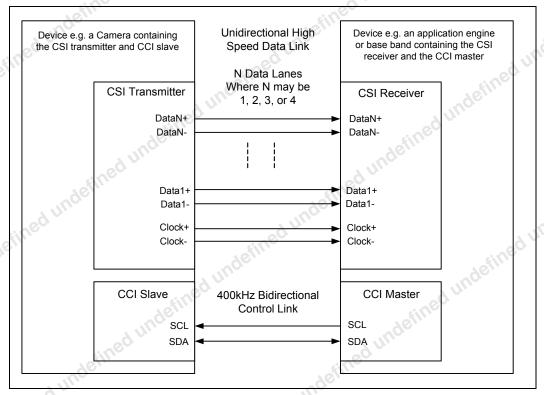
Data transfer by means of MIPI-CSI is unidirectional that is, from transmitter to receiver. CCI data transfer is bidirectional between the CCI slave and master.

Camera Serial Interface Bus (CSI) is a type of serial bus that enables transfer of data between a Transmitter device and a receiver device. The CSI device has a point-to-point connections with another CSI device by means of D-PHYs and as shown in Figure 19.

Similarly, CCI (Camera Control Interface bus) is a type of serial bus that enables transfer back and forth between the master CCI and a Slave CCI Unit.



Figure 19. MIPI-CSI Bus Block Diagram



D-PHY data lane signals are transferred point-to-point differentially using two signal lines and a clock lane. There are two signaling modes, a high speed mode that operates up-to 1500Mbs and a low power mode that works at 10Mbs. The mode is set to low power mode and a stop state at start up/power up. Depending on the desired data transfer type, the lanes switch between high and low power modes.

The CCI interface consists of an ${\rm I}^2{\rm C}$ bus which has a clock line and a bidirectional data line

The MIPI-CSI-2 devices operate in a layered fashion. There are 5 layers identified at the receiver and transmitter ends.

MIPI-CSI-2 Functional Layers:

PHY Layer

 An embedded electrical layer sends and detects start of packet signalling and end of packet signalling on the data lanes. It contains a serializer and deserializer unit to interface with the PPI / lane management unit. There is also a clock divider unit to source and receive the clock during different modes of operation.

• PPI/Lane Management Unit

 This layer does the lane buffering and distributes the data in the lanes as programmed in a round robin manner and also merges them for the PLI/Low Level Protocol unit.



PLI/Low Level Protocol Unit

 This layer packetizes as well as de-packetizes the data with respect to channels, frames, colors and line formats. There is also a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protection.

Pixel/Byte to Byte/Pixel Packing Formats

 Conversion of pixel formats to data bytes in the payload data is done depending on the type of image data supported by the application. It also re-converts the raw data bytes to pixel format understandable to the application layer.

Application

 Depending on the type of formats, camera types, capability of the camera used by the transmitter, the application layer recovers the image formats and reproduces the image in the display unit. It also works on de-framing the data into pixel-to-packing formats. High level encoding and decoding of image data is handled in the application unit.

11.5.1 MIPI-CSI-2 Receiver Features

CSI Features:

- Compliant to CSI-2 MIPI specification for Camera Serial Interface (Version 1.00).
- Supports standard D-PHY receiver compliant to the MIPI Specification.
- Supports PHY data programmability up to four lanes.
- Supports PHY data time-out programming.
- Has controls to start and re-start the CSI-2 data transmission for synchronization failures and to support recovery.
- The ISP may not support all the data formats that the CSI-2 receiver can handle.
- Refer Table 78 for formats supported by the ISP
- Supports all generic short packet data types
- Single Image Signal Processor interface for pixel transfers to support multiple image streams for all virtual channel numbers

D-PHY Features:

- Supports synchronous transfer in high speed mode with a bit rate of 80-1500Mb/s.
- Supports asynchronous transfer in low power mode with a bit rate of 10Mb/s.
- Differential signalling for HS data.
- Spaced one-hot encoding for Low Power [LP] data.
- Data lanes support transfer of data in high speed as well as low power modes.
- Supports ultra low power mode, escape mode, and high speed mode.
- Hasa clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.
- Activates and disconnects high speed terminators for reception and control mode.
- Activates and disconnects low power terminators for reception and transmission.

11.6 Register Map

For more information on MIPI- Camera Serial Interface (CSI) and ISP registers refer Intel[®] Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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12 SoC Storage

12.1 SoC Storage Overview

12.1.1 Storage Control Cluster (eMMC, SDIO, SD)

The SCC consists of SDIO, SD and eMMC controllers to support mass storage and IO devices.

- One eMMC 4.51 interface
- One SD 3.0 interface
- One SDIO 3.0 interface

12.2 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- Direction: The buffer direction can be either input, output, or I/O (bidirectional)
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- Description: A brief explanation of the signal's function.

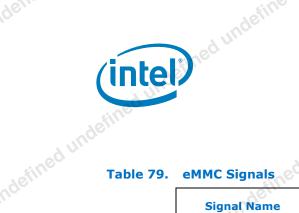
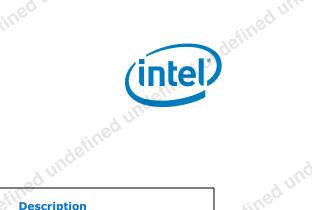


Table 79. eMMC Signals Signal Name Direction Type Description The frequency may vary between 25 and 200MHz.	indefine		defined	fined u
Table 79. eMMC Signals Signal Name Direction /Type MMC1_CLK I/O/GPIO I/O/GPIO I/O/GPIO MMC1_D[7:0] I/O/GPIO MMC1_CMD I/O/GPIO	(intel)		SoC Storag	unde. ge
MMC1_CLK I/O/GPIO eMMC Clock The frequency may vary between 25 and 200MHz.	afined	. red	July 4 Hude.	
MMC1_CLK I/O/GPIO eMMC Clock The frequency may vary between 25 and 200MHz.	unde	ndefills	i efinec	
MMC1_CLK I/O/GPIO eMMC Clock The frequency may vary between 25 and 200MHz.	Table 79. eMMC Signals	4 m.	4 unde	
The frequency may vary between 25 and 200MHz. MMC1_D[7:0] I/O/GPIO eMMC Port Data bits 0 to 7 Bidirectional port used to transfer data to and from eMMC device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull-ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7]. MMC1_CMD I/O/GPIO I/O/GPIO MMC1_RCOMP I/O/GPIO I/O/GPIO EMMC RCOMP This signal is used for pre-driver slew rate compensation.	48/11/1		Description	defined '
MMC1_D[7:0] I/O/GPIO BMMC Port Data bits 0 to 7 Bidirectional port used to transfer data to and from eMMC device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7]. MMC1_CMD I/O/GPIO EMMC Port Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer. MMC1_RCOMP I/O/GPIO EMMC RCOMP This signal is used for pre-driver slew rate compensation.	MMC1_CLK	I/O/GPIO		Une
data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7]. MMC1_CMD I/O/GPIO EMMC Port Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer. MMC1_RCOMP I/O/GPIO EMMC RCOMP This signal is used for pre-driver slew rate compensation.	MMC1_D[7:0]	I/O/GPIO	eMMC Port Data bits 0 to 7 Bidirectional port used to transfer data to and from eMMC device.	
This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer. MMC1_RCOMP I/O/GPIO EMMC RCOMP This signal is used for pre-driver slew rate compensation.	June Indefined undefine	ed under.	data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the	d undefined
This signal is used for pre-driver slew rate compensation.	MMC1_CMD	I/O/GPIO	This signal is used for card initialization and transfer of commands. It has two modes—open-drain for	
	MMC1_RCOMP	I/O/GPIO		
MMC1_RCLK I/GPIO eMMC Return Clock Signals	MMC1_RST_N	I/O/GPIO		Stine
nde ined unde in	MMC1_RCLK	I/GPIO	eMMC Return Clock Signals	' nuge,
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tined I. anden.	ned underined underined under	ined under	Datashe	ined undefil
	ined u	sed unos	4 undett.	



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SoC Storage	ine		de l'intel	
adefined undefined unu		ndefined i	defined une	
Table 80.	SDIO Signals		ad uno	ind
no.	Signal Name	Direction /Type	Description	defined
ade	SD2_CLK	I/O/GPIO	SDIO Clock The frequency may vary between 25 and 200MHz.	TUC
sined undefined un	SD2_D[2:0]	I/O/GPIO	SDIO Port Data bits 0 to 2 Bidirectional port used to transfer data to and from SDIO device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].	ne ne
Inde.	SD2_D[3]_CD_N	I/O/GPIO	SDIO Port Data bit 3 Bidirectional port used to transfer data to and from the SDIO device. Also, Card Detect. Active low when device is present.	undefined u.
undefined une	SD2_CMD	I/O/GPIO	SDIO Port Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.	
Table 81.	SD Signals (Sheet	1 of 2)	ed unde	٧٧ ،
unc	Signal Name	Direction /Type	Description	adefined

Table 81. SD Signals (Sheet 1 of 2)

S	Signal Name	Direction /Type	Description	defines
s	SD3_CLK	I/O/GPIO		
		-, 0, 00	SD Card Clock	Ulli
			The frequency may vary between 25 and 200 MHz.	
s	SD3_D[3:0]	I/O/GPIO	SD Card Data bits 0 to 3	
indefined undefined un	eò	undefine	Bidirectional port used to transfer data to and from SD/MMC card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].	. 19
Junde	SD3_CD_N	I/O/GPIO	SD Card Detect Active low when a card is present. Floating (pulled high with internal PU) when a card is not present.	adefined b
ined und	GD3_CMD	I/O/GPIO	SD Card Command This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.	d uli
sined under.	SD3_1P8EN	I/O/GPIO	SD Card 1.8V Enable Controls the voltage of the SD Card, the default is low (3.3V). The voltage is 1.8V when this signal is high.	
d under.	defined undefine		defined undefined	ed undefined l
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Table 81. SD Signals (Sheet 2 of 2)

Signal Name	Direction /Type	Description
SD3_RCOMP	I/O/GPIO	SD Card RCOMP
Silves		This signal is used for pre-driver slew rate compensation.
SD3_PWREN_N	I/O/GPIO	SD Card Power Enable This signal is used to enable power on a SD device.
SD3_WP	I/O/GPIO	SD Card Write Protect Active high to protect from write.

SD3_WP 12.3 Features

12.3.1 Memory Capacity

- Standard Capacity SD Memory Card (SDSC): Up to and including 2 GB.
- High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB.
- Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB.

12.3.2 SDIO/SD Interface Features

- Host clock rate variable between 0 and 200 MHz.
- Up to 800 Mbits per second data rate using 4 parallel data lines (SDR104 mode).
- Transfers the data in 1 bit and 4 bit SD modes.
- Transfers the data in following UHS-I modes (SDR12/25/50/104 and DDR50).
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Designed to work with I/O cards, Read-only cards and Read/Write cards.
- Supports Read wait Control, Suspend/Resume operation.

12.3.3 eMMC Interface Features

- Supports eMMC v4.51.
- Host clock rate variable between 0 and 200 MHz.
- Supports HS400 mode.
- Up to 1600 Mbits per second data rate using 8 bit parallel data lines (High Speed DDR mode).
- Up to 3200 Mbits per second data rate using 8 bit parallel data lines (HS400 mode).
- Transfers the data in 1 bit, 4 bit and 8 bit modes.
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Supports MMC Plus and MMC mobile.



12.3.4 **Storage Interfaces**

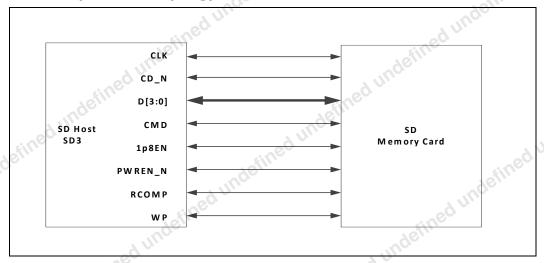
This section provides a very high level overview of the SD, SDIO, eMMC 4.51 specification.

SD 3.0 Bus Interface 12.3.4.1

The SD Card bus has a single master, single slaves (card), synchronous topology (refer Figure 20). During initialization process commands are sent to the card, allowing the application to detect the card and assign logical addresses to the physical slot. All data communication in the Card Identification Mode uses the command line (CMD) only.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Card will use only SD3_D[0] for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between hardware cost and system performance. Note that while DAT1-SD3 D[3:1] are not in use, the SoC will tri-state those signals.

Figure 20. SD Memory Card Bus Topology



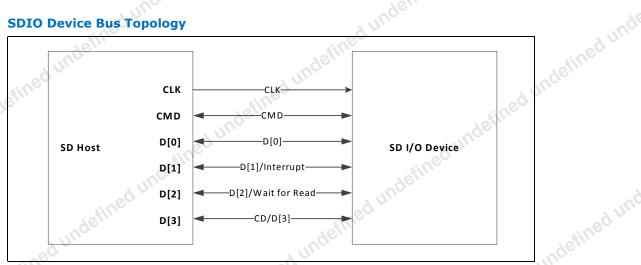
12.3.4.2 SDIO 3.0 Interface

The SDIO interface is the very much like the SD card interface. The SoC supports one SDIO device.

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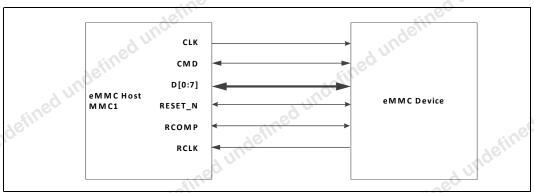


Figure 21. SDIO Device Bus Topology



12.3.4.3 eMMC 4.51 Interface

Figure 22. eMMC Interface



The standard offers performance enhancement features, including HS400 support and has an interface bandwidth of 400 MByte/sec.

The command protocol is significantly improved with Packed Commands (the ability to group a series of commands in a single data transaction), Context ID (grouping different memory transactions under a single ID so the device can understand that they are related), and Data Tag (tagging specific write transactions so they can be prioritized and targeted to a memory region with higher performance and better reliability).

The v4.51 standard also adds provision for volatile data cache, which can greatly reduce the latency between data transactions to improve performance.



12.4 References

The controller is configured to comply with:

- SD Specification Part 01 Physical Layer Specification version 3.00, April 16, 2009.
- SD Specification Part E1 SDIO Specification version 3.00, December 16, 2010.
- SD Specification Part A2 SD Host Controller Standard Specification version 3.00, February 18, 2010.
- SD Specification Part 03 security Specification version 1.01, April 15, 2001.
- Embedded MultiMedia Card (eMMC) Product Standard v4.51, JESD84-A5.

12.5 Register Map

For more information on SoC Storage registers refer Intel[®] Atom[™] Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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13 USB Controller Interfaces

USB Controller contains xHCI host controller that supports xHCI framework and USB1/2/3 specifications. And it has xDCI controller block for device only mode functionality. These 2 controllers will use an integrated mux to select between the 2 modes. All of this functionality is located in xDCI Controller.

13.1 SoC Supports

- Two (2) Super Speed Inter-Chip (SSIC) ports
- Three (3) Super Speed (SS) ports [Backward Compatible of USB 2.0 HS/FS/LS]
- One (1) Super Speed (SS) OTG port
- Two (2) High Speed Inter-Chip (HSIC) ports

Note: SoC can support the 4th SS port when OTG port is in Host mode.

13.2 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 82. USB SSIC Signals

Signal Name	Direction /Type	Description
USB_SSIC_RX_P/ N[0,1]	I/O/ SSIC PHY	Receiver serial data inputs: High-speed serialized data inputs.
USB_SSIC_TX_P/ N[0,1]	I/O/ SSIC PHY	Transmitter serial data outputs: High-Speed Serialized data outputs.
USB_SSIC_RCOMP _P/N	I / SSIC PHY	Resistor Compensation: An external resistor of 90 Ohm ±1% must be connected between the RCOMP pads.



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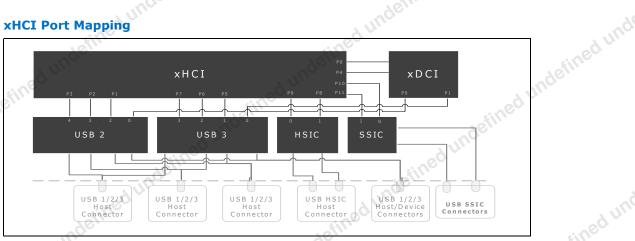
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USB Controll	er Interfaces		intel
Table 83.		undefine	d undefined undefined unterined undefined unterined undefined unde
Table 83.	USB Signals		ed une
	Signal Name	Direction /Type	Description
	USB3_TXP/ N[0:3]	O USB3 PHY	Transmitter serial data outputs: High-Speed Serialized data outputs.
sined un.	USB3_RXP/ N[0:3]	I USB3 PHY	Receiver serial data inputs: High-speed serialized data inputs.
d under.	USB3_RCOMP_P /N	I USB3 PHY	Resistor Compensation: An external resistor of 402 Ohm ±1% must be connected between the RCOMP pads.
ndefined undefined un	USB_DP/N[0:3]	I/O USB2 PHY	USB2 Data: High speed serialized data I/O.
	USB_RCOMP	O USB2 PHY	Resistor Compensation: An external resistor of 113 Ohm ±1% must be connected between pin and GND.
	USB_OTG_ID	I/O USB2 PHY	OTG ID: Pin out to detect the OTG ID.
ofined U.	USB_PLL_MON	O USB2 PHY	USB High Speed Observation
ed under	USB_VBUSSNS	I/O USB2 PHY	OTG Interface: VBUS_Sense
undefined undefined und	HSIC Signals	30	afined un
	Signal Nam	Di Di	Description

Table 84. HSIC Signals

ineo.	USB2 P	HY		
undefined Table 84.	HSIC Signals		Jefined U.	undefined un
	Signal Name	Direction /Type	Description	nugen.
ined uni	USB_HSIC[0:1]_DATA	I/O HSIC Buffer	HSIC Data.	
ined under	USB_HSIC[0:1]_STROBE	I/O HSIC Buffer	HSIC Strobe	
d undefined undefined uni	USB_HSIC_RCOMP	I/O HSIC Buffer	Resistor Compensation: RCOMP for HSIC buffer. Resistor: 450hm +/-1% connected between USB_HSIC_RCOMP and ground.	defined u
ad undefined undefined un	define	defined v	ndefined to	une
ed undefined	defined undefined un		Resistor Compensation: RCOMP for HSIC buffer. Resistor: 450hm +/-1% connected between USB_HSIC_RCOMP and ground.	d undefined i
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Figure 23. xHCI Port Mapping



USB 3.0 xHCI (Extensible Host Controller 13.3 Interface)

The xHCI compliant host controller can control up to 2 SSIC, 3 USB3.0 ports. USB3.0 being backward compatible to support USB2.0. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

13.3.1 **USB 3.0 Host Features**

The USB 3.0 Super Speed data interface is a four wire differential (TX and RX pairs) interface that supports simultaneous bi-directional data transmission. The interface supports a bit rate of 5 Gbps with a maximum theoretical data throughput over 3.2 Gbps due to 8b/10b symbol encoding scheme and protocol overhead (link flow control, packet framing and protocol overhead).

Low Frequency Periodic signaling (LFPS) is used to communicate initialization, training and power management information across a link that is in low power link state without using Super Speed signaling. This reduces power consumption.

13.3.1.1 **USB SSIC**

- Supports the SuperSpeed protocol only as defined in [USB 3.0].
- Optimized for Power, Area, Cost and EMI robustness.
- Supports 2 ports of 1 lane each.

13.3.1.2 **USB 3.0**

- Supported by xHCI software host controller interface.
- USB3 port disable.
- Supports local dynamic clock gating and trunk clock gating.
- Supports USB 3.0 LPM (U0, U1, U2, and U3) and also a SS Disabled low power

.ate Datasheet



- Supports USB3 Debug Device.
- Supports IVCAM(USB PC Camera).

13.3.2 USB HSIC Features

HSIC is a 2-signal (strobe and data) source synchronous serial interface for on board inter-chip USB communication. The interface uses 240 MHz DDR signaling to provide High-Speed 480 Mb/s USB transfers which are 100% host driver compatible with traditional USB cable connected topologies. Full Speed (FS) and Low Speed (LS) USB transfers are not directly supported by the HSIC interface.

Major feature and performance highlights are as follows:

- Supported by xHCI software host controller interface
- High-Speed 480 Mb/s data rate only.
- Source-synchronous serial interface.
- · Power is only consumed when a transfer is in progress.
- No Plug and Play support.
- No hot plug removal/attach.
- Signals driven at 1.2V standard LVCMOS levels.
- Designed for low power applications.
- Support for two host ports compliant to High Speed Inter-Chip Supplement (HSIC) to the USB 2.0 Specification. (USB 2.0).
- Clock request/ack mechanism.

13.4 USB 3.0 xDCI (Extensible Device Controller Interface)

The xDCI compliant Device controller can control up to 1 USB3.0 OTG port. USB3 being backward compatible to support USB2.0. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

13.5 References

USB 3.0 Specification

USB 2.0 Specification (Includes High-Speed Inter-Chip USB Electrical Specification)

13.5.1 Host Controller Specifications

Extensible Host Controller Interface (xHCI) Specification for USB 3.0 version 1.0.

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Low Power Engine (LPE) for Audio (I²S)

Low Power Engine for Audio provides acceleration for common audio and voice functions. The voice and audio engine provides a mechanism for rendering audio and voice streams and tones from the operating system, applications to an audio or voice codec, and ultimately to the speaker, headphones, or Bluetooth* headsets.

Audio streams in the SoC can be encoded and decoded by the Low Power Engine (LPE) in the Audio subsystem.

LPE Audio provides three external I²S audio interfaces.

Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 85. LPE Signals

• Direction : The buffer of	lirection car	i be either input, output, or I/O (bidirectiona	II).
• Type: The buffer type f	ound in Cha	apter 19, "Electrical Specifications".	
• Description : A brief ex	planation o	f the signal's function.	adeill
LPE Signals		efineo	led mi.
Signal Name	Direction /Type	Description	
LPE_I2S[2:0]_CLK	I/O	Clock signal for I ² S	
LPE_I2S[2:0]_FRM	I/O	Frame select signal for I ² S	
LPE_I2S[2:0]_DATAIN	I/O	RX data for I ² S	
LPE_I2S[2:0]_DATAOUT	I/O	TX data for I ² S	eineo

NOTE: All LPE signals are muxed and may be used by other functions.

Features

The LPE Audio Subsystem consists of the following:

- Integrated, power-efficient 32-bit architecture core with 24-bit audio processing instructions.
- Core processing speeds up to 343 MHz.
- Closely Coupled Memories (CCMs)
 - 80 KB Instruction RAM



- 160 KB Data RAM
- 48 KB Instruction Cache
- 96 KB Data Cache
- Very low-power consumption coupled with high-fidelity 24-bit audio.
- Dual-issue, static, super-scalar VLIW processing engine.
- Mode-less switching between 16-, 24-, and 64-bit dual-issue instructions.
- Dual MACs which can operate with 32 x 16-bit and/or 24 x 24-bit operands.
- Inter-Process Communication (IPC) mechanism to communicate with the SoC Processor Core including 4 KB mailbox memory.
- Flexible audio interfaces include three SSPs with I²S port functionality for BI-directional audio transfers.
 - I²S mode supports PCM payloads
 - Frame counters for all I²S ports
- High Performance DMA
 - DMA IP to support multiple outstanding transactions
 - Interleaved scatter-gather support for Audio DMA transfers
- Clock switching logic including new frequency increments.
- External timer function with an always running clock.

The LPE core runs at a peak clock frequency of 343 MHz and has dedicated on-chip program and data memories and caches. The LPE core can access shared SRAM blocks, and external DRAM through OCP fabric. It communicates with audio peripherals using the audio sub-fabric, and employs Inter-Processor Communication (IPC) mechanism to communicate with the SoC Processor Core.

The Audio subsystem includes two OCP-based DMA engines. These DMA engines support single and multi-block transfers. They can be configured to transfer data between DRAM and audio CCMs or transfer data between CCMs and the audio peripheral interfaces.

All these interfaces are peripherals in the Audio subsystem. LPE, LPE DMA, or the SoC processor core may access the peripherals during normal operation. The PMC may access all peripherals during specific tasks such as at boot time or during power state changes. A complete audio solution based on an internal audio processing engine which includes several I²S-based output ports.

The audio core used is a dedicated audio DSP core designed specifically for audio processing (decoding, post-processing, mixing, etc.)

Note:

LPE requires systems with more than 512 MB memory. This is required since the LPE firmware must reside at a stolen memory location on 512 MB boundaries below 3 GiB. The LPE firmware itself is \sim 1 MB, and is reserved by BIOS for LPE use.



Audio Capabilities 14.2.1

14.2.1.1 **Audio Decode**

Audio core supports decoding of the following formats:

- AAC-LC
- HE-AAC v1/2
- WMA9,10, PRO, Lossless, Voice
- MPEG layer 2
- RealAudio
- OggVorbis
- FLAC
- DD/DD+

Audio Encode

Audio core supports encoding of the following formats:

- MP3
- AAC-LC
- WMA
- DD-2channel

Clocks

14.3.1 **Clock Frequencies**

Table 86 shows the clock frequency options for the Audio functional blocks.

Table 86. **Clock Frequencies**

	Clock	Frequency	Notes
indefined un	Audio core	343/250/200 MHz/100/ 50 MHz/2x Osc/Osc 50(RO)/100(RO)	Audio input clock trunk. CCU drives one of several frequencies as noted.
defill.	DMA 0	50/OSC	DMA clock
UINC.	DMA1	50/OSC	DMA clock
	Audio fabric clock	50/OSC	Fabric clock derived from audio core clock
. •	ndefined under	defined un	ine ine
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INOC		deilli	Hineca



Table 86. Clock Frequencies

Clock	Frequency	Notes
SSP0 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP0 clock domains
SSP1 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP1 clock domains
SSP2 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP2 clock domains

14.3.2 38.4 MHz Clock for LPE

38.4 MHz, the 2X OSC clock, is added to increase MIPS for low power MP3 mode. This frequency will be supplied by the clock doubler internal to the SoC's Clock Control Unit.

14.3.3 Calibrated Ring Osc (50/100 MHz) Clock for LPE

A calibrated Ring Oscillator in the CCU_SUS provides a 50Mhz or an 100Mhz clock as another option for higher MIPS for low power MP3 mode. It is expected that this will be required to support decode of HE-AAC streams in the low power mode.

14.3.4 Cache and CCM Clocking

Data CCM, Data cache, Instruction CCM, and Instruction Cache run off of the LPE clock. These memories are in a single clock domain.

Note: All Data CCM and Instruction CCM run in the same clock domain.

14.4 SSP (I²S)

The SoC audio subsystem consists of the LPE Audio Engine and three Synchronous Serial Protocol (SSP) ports. These ports are used in PCM mode and enable simultaneous support of voice and audio streams over I²S. The SoC audio subsystem also includes two DMA controllers dedicated to the LPE. The LPE DMA controllers are used for transferring data between external memory and CCMs, between CCMs and the SSP ports, and between CCMs. All peripheral ports can operate simultaneously.

The Enhanced SSP Serial Ports are full-duplex synchronous serial interfaces. They can connect to a variety of external analog-to-digital (A/D) converters, audio, and telecommunication codecs, and many other devices which use serial protocols for transferring data. Formats supported include National* Microwire, Texas Instruments* Synchronous Serial Protocol (SSP), Motorola* Serial Peripheral Interface (SPI) protocol and a flexible Programmable Serial Port protocol (PSP).



The Enhanced SSPs operate in master mode (the attached peripheral functions as a slave) or slave mode (the attached peripheral functions as a master), and support serial bit rates from 0 to 6.5 Mbps, dependent on the input clock. Serial data formats range from 4 to 32-bits in length. Two on-chip register blocks function as independent FIFOs for transmit and receive data.

FIFOs may be loaded or emptied by the system processor using single transfers or DMA burst transfers of up to the FIFO depth. Each 32-bit word from the bus fills one entry in a FIFO using the lower significant bits of a 32-bit word.

Features

The SSP port features are:

- Inter-IC Sound (I²S) protocols, are supported by programming the Programmable Serial Protocol (PSP).
- One FIFO for transmit data (TXFIFO) and a second, independent, FIFO for receive data (RXFIFO), where each FIFO is 16 samples deep x 32 bits wide.
- Data sample sizes from 8, 16, 18, or 32 bits.
- 6.5 Mbps maximum serial bit-rate in both modes: master and slave.
- Clock master or slave mode operations.
- Receive-without-transmit operation.
- Network mode with up to eight time slots for PSP formats, and independent transmit/receive in any/all/none of the time slots.
- After updating SSP configuration, for example active slot count, the SSP will need to be disabled and enabled again. In other words, a SSP will not function correctly if a user changes the configuration setting on the fly.

Register Map

For more information on Low Power Engine (LPE) for Audio (I2S) registers refer Intel® Atom™ Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.



15 Intel[®] Trusted Execution Engine (Intel[®] TXE)

This chapter describes the security components and capabilities. The security system contains an $Intel^{\circledR}$ TXE and additional hardware security feature that enable a secure and robust platform.

15.1 Features

15.1.1 Security Features

Intel $^{\circledR}$ TXE in the SoC is responsible for supporting and handling security related features.

- 32-bit RISC processor.
- 256KB Data/Code RAM accessible only to the Intel[®] TXE.
- 128KB On Chip Mask ROM for storage of Intel[®] TXE code.
- Inter-Processor Communication for message passing between the Host CPU and Intel® TXE.
- 64 byte input and output command buffers.
- 256 byte shared payload (enables 2048-bit keys to be exchanged as part of the command).
- Multiple context DMA engine to transfer data between Host CPU address domain (System memory) and the Intel[®] TXE; programmable by the Intel[®] TXE CPU only.
- Secure I²C interface to NFC using master I²C block integrated into the Intel TXE -IP. Secure GPIOs to support input alert and two GP Outputs.

15.1.1.1 HW Accelerators

- DES/3DES (ECB, CBC) 128b ABA key for 3DES Key Ladder Operations.
- Three AES engines Two fast -128 and one slow- 128/256.
- Exponentiation Acceleration Unit (EAU) for modular exponentiation, modular reduction, large number addition, subtraction, and multiplication.
- SHA1, SHA256/384/512, MD5.

15.1.1.2 FW Utilities and Ciphers

- RSA (with EAU acceleration).
- Flash Write Enable/Disable.
- Comprehensive IPC Command Set.
- Chip Unique Key encryption key wrapping of other platform keys (Flash).



Downloadable FW Utilities and Ciphers 15.1.1.3

- Integrated Theft Deterrence Technology Intel[®] Anti-Theft Technology (Intel[®] AT).
- One Time Programmable (OTP).
- Firmware TPM (fTPM) measured boot.

TXE Interaction with NFC

- The NFC device requests attention from the TXE from GPIO ALERT pin to a SoC input interrupt pin (GPIO_SUS[8] pin).
- The GPIO block sends the pin value to TXE over a dedicated wire.
- The wire is connected to the TXE clock request mechanism in order to get a clock for sampling the wire. The TXE bridge includes a configuration register which includes an enable bit to qualify the clock request (which allows masking the clock request, in case the GPIO_SUS[8] is not used by NFC), and a polarity bit (which allows selecting whether the a clock request would be set on a high or low value in the wire).)
- The same qualified & polarity configured clock request input is also sent to PMU. In S0ix PMU uses it as a wake request.
- When a clock is available, the wire value is updated to an ICR (SICR31) in TXE bridge.
- TXE Bridge configuration register also includes two bits that allow detection of falling and/or rising edge on the alert pin. They cause an ISR (SISR[31]) to be set. When both ISR and IER bits for the alert are set an interrupt is generated.
- When the TXE is interrupted it parses the interrupt status registers in the TXE Bridge and figures the cause is the NFC device.
- TXE clears the Bridge ISR and sets configuration to detect the next edge on the alert pin.
- In order to use the I2C master, the TXE sets an I2C clock request register in the Bridge.
- The firmware then uses the I2C master to communicate with the NFC device. The firmware configures the I2C master to read up to 33Bytes of data (up to 36 bytes are supported by HW for read/write).
- When the I2C read is completed, the firmware is interrupted. The TXE may then read the data/status and clear the interrupt.
- The firmware repeats read/write sequence's as many times as it needs.
- When firmware is done with the I2C master, it must poll the controller to check that the I2C bus is idle before writing to the register to remove the I2C clock request, and before any reset of the I2C controller or power gating sequence. Shutting off clock or I2C master before the completion all activity on the bus will hang the I2C .d undefined undefined undefined device.



16 Intel[®] Sensor Hub

This chapter describes Intel[®] Sensor Hub.

16.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- Description: A brief explanation of the signal's function.

Table 87. ISH Signals

Signal Name	Direction	Description
ISH_I2C1_CLK	I/O	Clock Lane: ISH input clock
ISH_I2C1_SDA	I/O	Data Lane: ISH Data Lane
ISH_GPIO	I/O	ISH GPIO

16.2 Features

- Acquisition / sampling of sensor data.
- The ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS.
- Low power operation through clock gating of the ISH together with the ability to turn sensors off under control of host SW.
- The ability to operate independently when the host platform is in a low power state(S0-S0i3).
- Power saving features.
- Clock gating and power gating of functional blocks depending on current workloads.

16.2.1 Hardware

- Minute IA microprocessor.
- 384KB on chip Data/Code SRAM accessible only to the ISH.
- 8KB on chip ROM for ISH boot code.



- Inter-Processor Communication for message passing between the Host CPU and Intel[®] ISH.
 - Single Command/Doorbell DWORD register and 32 DWORD data registers each direction.
- Inter-Processor Communication for message passing between the Intel[®] ISH and Intel[®] TXE for ISH FW load.
 - Single Command/Doorbell DWORD register and 32 DWORD data registers each direction.
- Inter-Processor Communication for message passing between the Intel[®] ISH and PMC for ISH power management and ISH TXE communication assistance by PMC.
 - Single Command/Doorbell DWORD register each direction.
- DMA engine to transfer data between Host CPU address domain (System memory) and the Intel[®] ISH; programmable by the Intel[®] ISH CPU only.
- Two I2C interfaces and up to 15 GPIO lines for connecting sensors to ISH.

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17 Serial IO (SIO) Overview

The Serial I/O (SIO) is a collection of hardware blocks that implement simple but key serial I/O interfaces for platform usage. These hardware blocks include:

- "SIO I2C Interface"
- "SIO High Speed UART"
- "SIO Serial Peripheral Interface (SPI)"
- "SIO Pulse Width Modulation (PWM)"



SIO - Serial Peripheral Interface (SPI) 17.1

The Serial I/O implements three SPI controllers that supports master mode.

17.1.1 **Signal Descriptions**

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 88. **SPI Interface Signals**

Signal Name	Direction /Type	Description
SPI[1,2,3]_CLK	O GPIO	SPI Clock: When the bus is idle, the owner will drive the clock signal low.
SPI[1,2,3]_CS[0]_N	O GPIO	SPI Chip Select 0: Used as the SPI Chip select 0.
SPI[1,2,3]_CS[1]_N	O GPIO	SPI Chip Select 1: Used as the SPI Chip select 1.
SPI[1,2,3]_MISO	I GPIO	SPI Master IN Slave OUT: Data input pin for the SoC.
SPI[1,2,3]_MOSI	O GPIO	SPI Master OUT Slave IN: Data output pin for the SoC. Operates as a second data input pin for the SoC when in Single Input, Dual Output Fast Read mode.

Features

The following is list of SPI features:

- Single interrupt line.
 - Could be assigned to interrupt PCI INT [A] or ACPISIO INT[1].
- Configurable frame format, clock polarity and clock phase.
- · Supports three SPI peripherals only.
- Two Chip selects are supported for each of the 3 SPI controllers.
- Supports master mode only.
- Receive and transit buffers are both 256x32 Bits.
 - The receive buffer has only 1 water mark.
 - The transmit buffer has 2 water marks.

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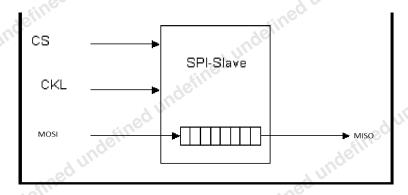
Supports up to 20 Mbps.

17.1.2.1 General

The Serial Peripheral Interface is used primarily for a synchronous serial communication of host processor and peripherals.

In the standard configuration for a slave device, two control and two data lines are used. The data output MISO serves on the one hand the reading back of data, offers however also the possibility to cascade several devices. The data output of the preceding device then forms the data input for the next IC.

Figure 24. SPI Slave



There is a MASTER and a SLAVE mode. The MASTER device provides the clock signal and determines the state of the chip select lines, i.e. it activates the SLAVE it wants to communicate with. CS and CKL are therefore outputs. The SLAVE device receives the clock and chip select from the MASTER, CS and CKL are therefore inputs. This means there is one master, while the number of slaves is only limited by the number of chip selects.

A SPI device can be a simple shift register up to an independent subsystem. The basic principle of a shift register is always present. Command codes as well as data values are serially transferred, pumped into a shift register and are then internally available for parallel processing.

The SPI requires two control lines (CS and CLK) and two data lines MOSI (Master-Out-Slave-In) and MISO (Master-In-Slave-Out).

17.1.2.2 Data and Control lines for SPI

With CS (Chip-Select) the corresponding peripheral device is selected. This pin is mostly active-low. In the un-selected state the MISO lines are hi-Z and therefore inactive. The master decides with which peripheral device it wants to communicate. The clock line CLK is brought to the device whether it is selected or not. The clock serves as synchronization of the data communication. The majority of SPI devices provide these four lines. Sometimes it happens that MOSI and MISO are multiplexed.



SPI Configuration: Clock Phase and Polarity 17.1.2.3

SPI clock phase and clock polarity overview.

- The SSCR1.SPO polarity setting bit determines whether the serial transfer occurs on the rising edge of the clock or the falling edge of the clock.
 - When SSCR1.SPO = 0, the inactive or idle state of SPI1 CLK is low.
 - When SSCR1.SPO = 1, the inactive or idle state of SPI1_CLK is high.
- The SSCR1.SPH phase setting bit selects the relationship of the serial clock with the slave select signal.
 - When SSCR1.SPH = 0, SPI1 CLK is inactive until one cycle after the start of a frame and active until 1/2 cycle after the end of a frame.
 - When SSCR1.SPH = 1, SPI1_CLK is inactive until 1/2 cycle after the start of a frame and active until one cycle after the end of a frame.

Below figure shows an 8-bit data transfer with different phase and polarity settings.

SSCR1.SPO=0 CLK SSCR1.SPO=1 CLK SS# DO SSCR1.SPH=0 Data out Di7 D₀ D2 Di3 Dİ4 D₅ DĠ Dİ7 D:4 Di0 Ď1 D3 D5 SSCR1.SPH=1 Data out Data in Dj0 D2 D3 D4 D5

Figure 25. Clock Phase and Polarity

In a single frame transfer, the SPI controller supports all four possible combinations for the serial clock phase and polarity.

The combinations of polarity and phases are referred to as modes which are commonly numbered according to the following convention, with SSCR1.SPO as the high order bit and SSCR1.SPH as the low order bit.

Table 89. **SPI** Modes

Mode	SSCR1.SPO	SSCR1.SPH
0	0	0 60
1	0	76.1
2	1	0
3	1 00	1

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17.2 SIO - I²C Interface

The SoC supports 7 instances of I^2C controller. Both 7-bit and 10-bit addressing modes are supported. These controllers operate in master mode only.

17.2.1 Signal Descriptions

 $\rm I^2C$ is a two-wire bus for inter-IC communication. Data and clock signals carry information between the connected devices. The following is the $\rm I^2C$ Interface. The SoC supports 7 $\rm I^2C$ interfaces for general purpose to control external devices. The $\rm I^2C$ signals are muxed over GPIOs.

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 90. I²C[6:0] Signals

Signal Name	Direction /Type	Description	
I2C[6:0]_DATA	I/O/	I ² C Serial Data	
defined.	GPIOMV, MS, I2C	These signals are muxed and may be used by other functions.	
I2C[6:0]_CLK	I/O/	I ² C Serial Clock	
	GPIOMV, MS, I2C	These signals are muxed and may be used by other functions.	

17.2.2 NFC I²C Interface Signals

Table 91. NFC I²C Interface Signals

	Signal Name	Direction/ Type	Description
ofined v	NFC_I2C_DATA	I/O/ GPIOMV, MS, I2C	NFC I²C Serial Data These signals are muxed and may be used by other functions.
sined under	NFC_I2C_CLK	I/O/ GPIOMV, MS, I2C	NFC I ² C Serial Clock These signals are muxed and may be used by other functions.
under	GPIO_ALERT	I/O/ GPIOMV, MS	ALERT pin for NFC These signals are muxed and may be used by other functions.



17.2.3 Features

17.2.3.1 I²C Protocol

The I²C bus is a two-wire serial interface, consisting of a serial data line and a serial clock. These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a "transmitter" or "receiver," depending on the function of the device. Devices are considered slaves when performing data transfers, as the SoC will always be a Master. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

- The SoC is always the I²C master; and it supports multi-master mode.
- The SoC can support clock stretching by slave devices.
- The I2Cx_DATA line is a bidirectional signal and changes only while the I2Cx_CLK line is low, except for STOP, START, and RESTART conditions.
- The output drivers are open-drain or open-collector to perform wire-AND functions on the bus.
- The maximum number of devices on the bus is limited by the maximum capacitance specification of 400 pF. Refer Chapter 19, "Electrical Specifications" for more details.
- · Data is transmitted in byte packages.

17.2.3.2 I²C Modes of Operation

The I²C module can operate in the following modes:

- Standard mode (with a bit rate up to 100 Kb/s).
- Fast mode (with a bit rate up to 400 Kb/s).
- Fast Mode plus mode (with a bit rate up to 1 Mb/s).
- High-speed mode (with a bit rate up to 1.7 Mb/s).

The I^2C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, high speed mode, fast mode plus and fast mode devices are downward compatible.

- High-speed mode devices can communicate with fast mode and standard mode devices in a mixed speed bus system.
- \bullet Fast mode devices can communicate with standard mode devices in a 0–100 Kb/s I^2C bus system.

However, according to the I²C specification, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system since they cannot follow the higher transfer rate and unpredictable states would occur.

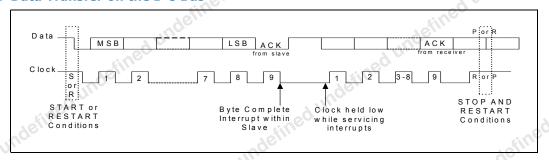
Refer Table 1 for more information on the I2C interface speed for different Sku's.



17.2.3.3 Functional Description

- The I²C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to/from the master.
- The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer:
 - When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.
 - The slave then sends an acknowledge (ACK) pulse after the address.
- If the master (master-transmitter) is writing to the slave (slave-receiver)
 - The receiver gets one byte of data.
 - This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver)
 - The slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
 - This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in below figure.

Figure 26. Data Transfer on the I²C Bus



17.2.3.3.1 START and STOP Conditions

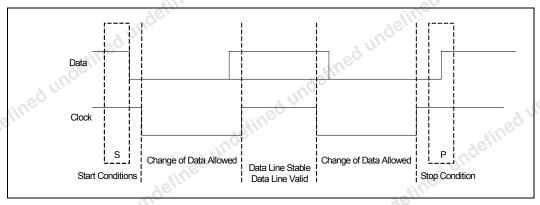
When the bus is idle, both the clock and data signals are pulled high through external pull-up resistors on the bus.

When the master wants to start a transmission on the bus, the master issues a START condition.



- This is defined to be a high-to-low transition of the data signal while the clock is high.
- When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the data line while the clock is high. Figure 27 shows the timing of the START and STOP conditions.
- When data is being transmitted on the bus, the data line must be stable when the clock is high.

Figure 27. START and STOP Conditions



The signal transitions for the START/STOP conditions, as depicted above, reflect those observed at the output of the master driving the I^2C bus. Care should be taken when observing the data/clock signals at the input of the slave(s), because unequal line delays may result in an incorrect data/clock timing relationship.

17.3 NFC I²C

NFC device requires 1.8V I/Os.

For more information refer "TXE Interaction with NFC"

17.3.1 References

 $\rm I^2C ext{-}Bus$ Specification and User Manual, Revision 03: http://ics.nxp.com/support/documents/interface/pdf/i2c.bus.specification.pdf

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SIO - High Speed UART 17.4

The SoC implements two instances of high speed UART controller that support baud rates between 300 and 3686400. Hardware flow control is also supported.

Signal Descriptions 17.4.1

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 92. UART 1 Interface Signals

ne name of th	e signal/pin.	
uffer directior	n can be either input, output, or I/O (bidirectional).	Ind
type found in	Chapter 19, "Electrical Specifications".	ined to
rief explanati	on of the signal's function.	indein
ignals	defined sined	
Direction/ Type	Description	
I/O/ GPIOMV, MS	High-speed UART receive data input: This signal is muxed and may be used by other functions.	.0
I/O/ GPIOMV, MS	High-speed UART transmit data: This signal is muxed and may be used by other functions.	defined un
I/O/ GPIOMV, MS	High-speed UART request to send: This signal is muxed and may be used by other functions.	d une
I/O/ GPIOMV, MS	High-speed UART clear to send: This signal is muxed and may be used by other functions.	
	uffer direction type found in rief explanati ignals Direction/ Type I/O/ GPIOMV, MS I/O/ GPIOMV, MS I/O/ GPIOMV, MS	Direction/ Type I/O/ GPIOMV, MS I/O/ G

Jundefined undefined ur **UART 2 Interface Signals**

Signal Name	Direction/ Type	Description
JART2_DATAIN	I/O/ GPIOMV, MS	High-speed UART receive data input: This signal is muxed and may be used by other functions.
JART2_DATAOUT	I/O/ GPIOMV, MS	High-speed UART transmit data: This signal is muxed and may be used by other functions.
JART2_RTS_N	I/O/ GPIOMV, MS	High-speed UART request to send: This signal is muxed and may be used by other functions.
JART2_CTS_N	I/O/ GPIOMV, MS	High-speed UART clear to send: This signal is muxed and may be used by other functions.
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J	JART2_DATAIN JART2_DATAOUT JART2_RTS_N	IART2_DATAIN



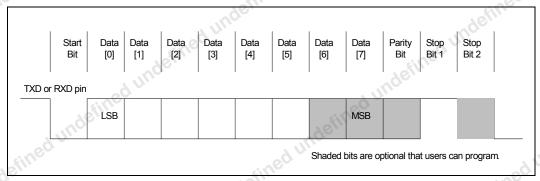
17.4.2 **Features**

17.4.2.1 **UART Function**

The UART transmits and receives data in bit frames as shown in Figure 29.

- Each data frame is between 7 and 12 bits long, depending on the size of data programmed and if parity and stop bits are enabled.
- The frame begins with a start bit that is represented by a high-to-low transition.
- Next, 5 to 8 bits of data are transmitted, beginning with the least significant bit. An optional parity bit follows, which is set if even parity is enabled and an odd number of ones exist within the data byte; or, if odd parity is enabled and the data byte contains an even number of ones.
- The data frame ends with one, one-and-one-half, or two stop bits (as programmed by users), which is represented by one or two successive bit periods of a logic one.

Figure 29. UART Data Transfer Flow



Each UART has a Transmit FIFO and a Receive FIFO and each holds 64 characters of data. There are two separate methods for moving data into/out of the FIFOs— Interrupts and Polling.

17.4.2.2 **Clock and Reset**

The BAUD rate generates from base frequency of 50 MHz.

17.4.2.3 **Baud Rate Generator**

The baud rates for the UARTs are generated with from the base frequency (Fbase) indicated in Table 94 by programming the DLH and DLL registers as divisor. The hexadecimal value of the divisor is (IER_DLH[7:0]<<8) | RBR_THR_DLL[7:0].

Fbase 44236800 Hz can be achieved by programming the DDS Multiplier as 44,236,800 (in decimal), and DDS Divisor as the system clock frequency in Hz. (50,000,000 in decimal when the system clock frequency is 50 MHz.) indefined undefined undefine



hed undefined undefined und The output baud rate 3686400 is equal to the base frequency divided by thirteen times the value of the divisor, as follows: baud rate = (Fbase) / (13 * divisor). The output baud rate for all other baud rates is equal to the base frequency divided by sixteen times the value of the divisor, as follows: baud rate = (Fbase) / (16 * divisor).

Baud Rates Achievable with Different DLAB Settings

indefined undefined uni	DLH,DLL Divisor	DLH,DLL Divisor Hexadecimal	Baud Rate	ned undefined &
*inec.		Fbase 1: 47923200 Hz		unc
dell	1	0001	3686400	eo
d ull		Fbase 2: 44236800 Hz	Aeil	
einec	1	0001	2764800	ed undefined undefined uni
deli	3	0003	921600	4 UIII
7/1/2	6	0006	460800	inec
	9	0009	307200	deili
	12	000C	230400	, unc
	15	000F	184320	ineo.
الله لم	18	0012	153600	defill.
eine c	24	0018	115200	IInos
delli	48	0030	57600	eq.
4 Une	72	0048	38400	
ineo	144	0090	19200	
defill	288	0120	9600	111
undefined undefined un	384	0180	7200	ea
	576	0240	4800	defil.
	768	0300	3600	IIIO
	1152	0480	2400	ed
ر ۱	1536	0600	1800	ed undefined undefined un
ineo	2304	0900	1200	inoc
defill	4608	1200	600	ed
undefined u	9216	2400	300	line

Use

Each UART has a transmit FIFO and a receive FIFO, each FIFO holding 64 characters of data. Three separate methods move data into and out of the FIFOs: interrupts, DMA, and polled.

17.4.3.1 **DMA Mode Operation**

17.4.3.1.1 **Receiver DMA**

The data transfer from the HSUART to host memory is controlled by the DMA write channel. To configure the channel in write mode, channel direction in the channel control register needs to be programmed to "1". The software need to program the



descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

17.4.3.1.2 Transmit DMA

The data transfer from host memory to HSUART is controlled by DMA read channel. To configure the channel in read mode, channel direction in the channel control register needs to be programmed to "0". The software need to program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

17.4.3.1.3 Removing Trailing Bytes in DMA Mode

When the number of entries in the Receive FIFO is less than its trigger level, and no additional data is received, the remaining bytes are called Trailing bytes. These are DMAed out by the DMA as it has visibility into the FIFO Occupancy register.

17.4.3.2 FIFO Polled-Mode Operation

With the FIFOs enabled (IIR_FCR.IID0_FIFOE bit set to 1), clearing IER_DLH[7] and IER_DLH[4:0] puts the serial port in the FIFO Polled Operation mode. Because the receiver and the transmitter are controlled separately, either one or both can be in Polled Operation mode. In this mode, software checks Receiver and Transmitter status using the Line Status Register (LSR). The processor polls the following bits for Receive and Transmit Data Service.

17.4.3.2.1 Receive Data Service

The processor checks data ready (LSR.DR) bit which is set when 1 or more bytes remains in the Receive FIFO or Receive Buffer Register (RBR_THR_DLL).

17.4.3.2.2 Transmit Data Service

The processor checks transmit data request LSR.THRE bit, which is set when the transmitter needs data.

The processor can also check transmitter empty LSR.TEMT, which is set when the Transmit FIFO or Holding register is empty.

17.4.3.2.3 Autoflow Control

Autoflow Control uses Clear-to-Send (nCTS) and Request-to-Send (nRTS) signals to automatically control the flow of data between the UART and external modem. When autoflow is enabled, the remote device is not allowed to send data unless the UART asserts nRTS low. If the UART de-asserts nRTS while the remote device is sending data, the remote device is allowed to send one additional byte after nRTS is deasserted. An overflow could occur if the remote device violates this rule. Likewise, the UART is not



allowed to transmit data unless the remote device asserts nCTS low. This feature increases system efficiency and eliminates the possibility of a Receive FIFO Overflow error due to long interrupt latency.

Autoflow mode can be used in two ways: Full autoflow, automating both nCTS and nRTS, and half autoflow, automating only nCTS. Full Autoflow is enabled by writing a 1 to bits 1 and 5 of the Modem Control Register (MCR). Auto-nCTS-Only mode is enabled by writing a 1 to bit 5 and a 0 to bit 1 of the MCR register.

17.4.3.2.4 RTS (UART Output)

When in full autoflow mode, nRTS is asserted when the UART FIFO is ready to receive data from the remote transmitter. This occurs when the amount of data in the Receive FIFO is below the programmable threshold value. When the amount of data in the Receive FIFO reaches the programmable threshold, nRTS is de-asserted. It will be asserted once again when enough bytes are removed from the FIFO to lower the data level below the threshold.

17.4.3.2.5 CTS (UART Input)

When in Full or Half-Autoflow mode, nCTS is asserted by the remote receiver when the receiver is ready to receive data from the UART. The UART checks nCTS before sending the next byte of data and will not transmit the byte until nCTS is low. If nCTS goes high while the transfer of a byte is in progress, the transmitter will complete this byte.



SIO - Pulse Width Modulation (PWM) 17.5

The Pulse Width Modulation block allows control the frequency and duty cycle of an output signal. The SoC has 2 instances of the PWM interface.

17.5.1 A Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- Jundefined undefined un **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- **Type:** The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

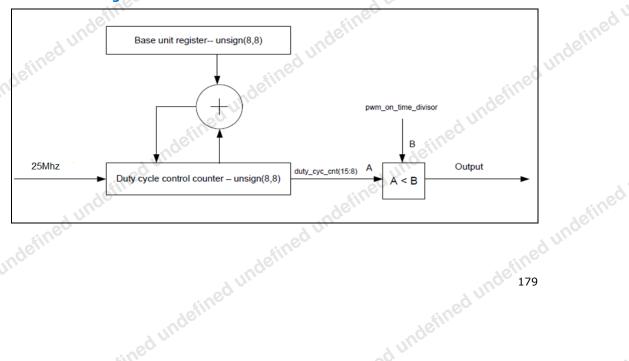
Figure 30. PWM Signals

Signal Name	Direction/ Type	Description	
PWM[0]	I/O/ GPIOMV, MS	Pulse Width Modulation output 0.	
PWM[1]	I/O/ GPIOMV, MS	Pulse Width Modulation output 1.	

17.5.2 **Features**

The software controls the PWM block by updating the PWMCTRL register and setting the PWMCTRL.PWM SW UPDATE bit whenever a change in frequency or duty cycle of the PWM output signal is required. The PWM block applies the new settings at the start of the next output cycle and resets the PWMCTRL.PWM SW UPDATE bit. The SoC uses 25 MHz for the counter. Refer Figure 31 for PWM block diagram.

Figure 31. PWM Block Diagram





There are two controls of the PWM output:

- Frequency is controlled by the PWMCTRL.PWM_BASE_UNIT bits. The PWMCTRL.PWM_BASE_UNIT value is added to a 16 bit counter every clock cycle and the counter roll-over marks the start of a new cycle.
- **Duty cycle** is controlled by the PWMCTRL.PWM_ON_TIME_DIVISOR setting (0 to 255). When the counter rolls-over it is reset and a new cycle starts with the output signal being 0, once the counter reaches the PWMCTRL.PWM_ON_TIME_DIVISOR value the output toggles to 1 and stays high until the counter rolls over.

The PWM block is clocked by the 25 MHz oscillator clock. The output frequency can be estimated with the equation:

• Target frequency = 25MHz * base_unit value/256.

NOTE: The larger the value of base_unit, the larger the error that the PWM output frequency will have with respect to the equation above. For example any Base_unit_value > 128 will result in 12.5 MHz max frequency. Any value between 86 and 128 will result in 8.33 MHz output frequency. And accordingly the larger the base_unit value the smaller duty cycle resolution. Maximum duty cycle resolution is 8 bits.

Table 95 illustrates the output frequency and duty-cycle resolution for different settings of the base_unit_value (when using 25 MHz oscillator clock).

Table 95. Example PWM Output Free	quency and Resolution
-----------------------------------	-----------------------

Target Frequency	Base Unit Value	CLK Cycle Count	Duty Cycle Resolution	ined
12.5 MHz	>=128	1 1100	no resolution	deill
1.07 MHz	11	23	<8 bit resolution	d une
488 kHz	5	51	<8 bit resolution	
97.6 kHz	1	256	8 resolution	
48.8 kHz	0.5	Theoretically 512 but only 255 available since On Time Divisor is only 8b	>8bit	
0	0 0	0	Flat 0 output	

97.6 kHz 48.8 kHz 0 17.6 Register Map

For more information on Serial IO registers refer Intel[®] Atom[™] Z8000 Processor Series Datasheet (Volume 2 of 2), Doc ID:332066.

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18 Platform Controller Unit (PCU) Overview

Platform Controller Unit (PCU) is a collection of HW blocks that are critical for implementing a Windows* compatible platform. These HW blocks include:

- "PCU Power Management Controller (PMC)"
- "PCU Fast Serial Peripheral Interface (SPI)"
 - For boot FW and system configuration data Flash storage
- "PCU Universal Asynchronous Receiver/Transmitter (UART)"
- "PCU Intel Legacy Block (iLB) Overview"

The PCU also implements some high level configuration features for BIOS/EFI boot.

18.1 Features

The key features of the individual blocks are as follows:

- Universal Asynchronous Receiver/Transmitter (UART)
 - 16550 controller compliant.
 - Reduced Signal Count: TX and RX only.
 - COM1 interface.
- Fast Serial Peripheral Interface (FST SPI)
 - For SPI Flash, of up to 16MB size per chip select is supported. No other SPI peripherals are supported.
 - Stores boot FW and system configuration data.
 - Supports frequencies of 20 MHz, 33 MHz and 50 MHz.
- Power Management Controller (PMC)
 - Controls many of the power management features present in the SoC.
- Intel Legacy Block (iLB)
 - Supports legacy PC platform features.
 - Sub-blocks include LPC, GPIO, 8259 PIC, IO-APIC, 8254 timers, HPET timers and the RTC.

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PCU - Power Management Controller (PMC) 18.2

Power Management Controller (PMC) controls many of the power management features present in the SoC.

Signal Descriptions 18.2.1

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 96. PMC Signals (Sheet 1 of 2)

isfined u.	Signal Name	Direction /Type	Description
undefined undefined un	PMC_ACPRESENT	I/O/ GPIOMV, MS	AC Present: This input pin indicates when the platform is plugged into AC power.
	PMC_BATLOW_N	I/O/ GPIOMV, MS	Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from the S4/S5 state. This signal can also be enabled to cause an SMI_N when asserted. In desktop configurations without a battery, this signal should be tied high to V1P8_S5.
Jundefined undefined un	iefined L	I/GPIOMV, MS	Core Power OK: When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for 10 ms. It can be driven asynchronously. When it is negated, the SoC asserts PMC_PLTRST_N. NOTE: It is required that the power rails associated with PCI Express (typically the 3.3V, 5V, and 12V core well rails) have been valid for 99 ms prior to PMC_CORE_PWROK assertion in order to comply with the 100 ms T _{PVPERL} PCI Express 2.0 specification on PMC_PLTRST_N deassertion. NOTE: PMC_CORE_PWROK must not glitch, even if PMC_RSMRST_N is low.
d undefined undefined u	PMC_PLTRST_N	I/O/ GPIOMV, MS	Platform Reset: The SoC asserts this signal to reset devices on the platform. The SoC asserts the signal during power-up and when software initiates a hard reset sequence through the Reset Control (RST_CNT) register.
182 undefined	undefined under	undefin	Datashee
4efine	ine'	0	ad ulli



defined undefined undefined ndefined undefined Table 96. PMC Signals (Sheet 2 of 2)

	Tito bigitals (blicet 2		
	Signal Name	Direction /Type	Description
indefined undefined undef	PMC_PWRBTN_N	I/O/ GPIOMV, MS	Power Button: The signal will cause SMI_N or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If the signal is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
Indefine	PMC_RSMRST_N	I/GPIOMV, MS	Resume Well Reset: Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.
undefined undefined und	PMC_RSTBTN_N	I/O/ GPIOMV, MS	System Reset: This signal forces an internal reset after being debounced. This signal is muxed and may be used by other functions.
d undefine	PMC_SLP_SOIX_N	I/O/ GPIOMV, MS	S0ix Sleep Control: This signal is for power plane control. It can be used to control system power when it is in a S0ix state.
undefinec	PMC_SLP_S4_N	I/O/ GPIOMV, MS	S4 Sleep Control: This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.
undefined undefined und	PMC_SUS_STAT_N	I/O/ GPIOMV, MS	Suspend Status: This signal is asserted by the SoC to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is muxed and may be used by other functions.
	ined to	I/O/ GPIOMV, MS	Suspend Clock: This 32 kHz clock is an output of the RTC generator circuit for use by other chips for refresh clock. This signal is muxed and may be used by other functions.
ed undefined undefined un	PMC_SUSPWRDNACK	I/O/ GPIOMV, MS	Suspend Power Down Acknowledge: Asserted by the SoC when it does not require its Suspend well to be powered. This pin requires a pull-up to UNCORE_V1P8_G3. This signal is muxed and may be used by other functions.
ed undefine	ndefined undefined		Jundefined undefined undef
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indefil.		Aefine C	sined un
Datasheet	ine ^d	und	Jundefined undefined undefined

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18.2.2 Features

18.2.2.1 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The GEN_PMCON1.AG3E bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only two possible events that will wake the system after a power failure.

- PMC_PWRBTN_N: PMC_PWRBTN_N is always enabled as a wake event. When RSMRST_N is low (G3 state), the PM1_STS_EN.PWRBTN_STS bit is reset. When the SoC exits G3 after power returns (PMC_RSMRST_N goes high), the PMC_PWRBTN_N signal is already high (because the suspend plane goes high before PMC_RSMRST_N goes high) and the PM1_STS_EN.PWRBTN_STS bit is 0b.
- RTC Alarm: The PM1_STS_EN.RTC_EN bit is in the RTC well and is preserved after a power loss. Like PM1_STS_EN.PWRBTN_STS the PM1_STS_EN.RTC_STS bit is cleared when PMC_RSMRST_N goes low.

The SoC monitors both PMC_CORE_PWROK and PMC_RSMRST_N to detect for power failures. If PMC_CORE_PWROK goes low, the GEN_PMCON1.PWR_FLR bit is set. If PMC_RSMRST_N goes low, GEN_PMCON1.SUS_PWR_FLR is set.

Table 97. Transitions Due to Power Failure

State at Power Failure	GEN_PMCON1.AG3E bit	Transition When Power Returns		
S0	1 0 define	S5 S0		
S4	0	S4 S0		
S5	inderin 1	S5 S0		

The SoC has various input signals that trigger specific events. This section describes those signals and how they should be used.

18.2.2.2.1 PMC_PWRBTN_N (Power Button)

The PMC_PWRBTN_N signal operates as a "Fixed Power Button" as described in the Advanced Configuration and Power Interface specification. The signal has a 16 ms debounce on the input. The state transition descriptions are included in Table 98.

Note: The transitions start as soon as the PMC_PWRBTN_N is pressed (but after the debounce logic), and does not depend on when the power button is released.



Note:

During the time that the PMC SLP S4 N signal is stretched for the minimum assertion width (if enabled), the power button is not a wake event. Refer note below for more

Transitions Due to Power Button

ed unde	Present State	Event	Transition/Action	Comment
defined undefinee	S0/Cx	PMC_PWRBTN_N goes low	SMI_N or SCI generated (depending on PM1_CNT.SCI_EN, PM1_STS_EN.PWRBTN_EN and SMI_EN.GBL_SMI_EN)	Software typically initiates a Sleep state
	S4/S5	PMC_PWRBTN_N goes low	Wake Event. Transitions to S0 state	Standard wakeup
A ^Q	G3	PMC_PWRBTN_N pressed	None	No effect since no power Not latched nor detected
adefined une	S0, S4	PMC_PWRBTN_N held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor or any other subsystem
defined undefined	S0ix	PMC_PWRBTN_N goes low	Wake Event. Transitions to S0 state	PM1_STS_EN.PWRBTN_EN should be set since a SMI/SCI event is required.

Power Button Override Function

If PMC_PWRBTN_N is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the S5 state, regardless of present state (S0-S4), even if the PMC_CORE_PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor nor any similar dependency from any other subsystem.

The PMC_ PWRBTN_N status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the GEN_PMCON2.PWRBTN_LVL bit.

Note:

The 4 seconds PMC_PWRBTN_N assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the SoC is in a S0 state. If the PMC_PWRBTN_N signal is asserted and held active when the system is in a suspend state (S4), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

During the time that the SLP S4 N signal is stretched for the minimum assertion width (if enabled by GEN PMCON1.S4ASE), the power button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the power button waiting for the system to awake. Since a 4 seconds press of the power button is already defined as an unconditional power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has



expired, the power button awakes the system. Once the minimum PMC_SLP_S4_N power cycle expires, the power button must be pressed for another 4 to 5 seconds to create the override condition to S5.

18.2.2.2. Sleep Button

The Advanced Configuration and Power Interface specification defines an optional sleep button. It differs from the power button in that it only is a request to go from S0 to S4 (not S5). Also, in an S5 state, the power button can wake the system, but the sleep button cannot.

Although the SoC does not include a specific signal designated as a sleep button, one of the GPIO signals can be used to create a "Control Method" sleep button. Refer Advanced Configuration and Power Interface specification for implementation details.

18.2.2.2.3 PME_B0 (PCI Power Management Event Bus 0)

The GPE0a_STS.PME_B0_STS bit exists to implement PME_N-like functionality for any internal device on Bus 0 with PCI power management capabilities.

18.2.2.2.4 PMC_RSTBTN_N Signal

When the PMC_RSTBTN_N pin is detected as active after the 16 ms debounce logic, the SoC attempts to perform a "graceful" reset, by waiting for the relevant internal devices to signal their idleness. If all devices are idle when the pin is detected active, the reset occurs immediately; otherwise, a counter starts. If at any point during the count all devices go idle the reset occurs. If the counter expires and any device is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the PMC_RSTBTN_N input remains asserted or not. It cannot occur again until PMC_RSTBTN_N has been detected inactive after the debounce logic, and the system is back to a full S0 state with PMC_PLTRST_N inactive. Note that if RST_CNT.FULL_RST is set then PMC_RSTBTN_N will result in a full power cycle reset.

18.2.2.3 System Power Planes

The system has several independent power planes, as described in Table 99.

Note: When a particular power plane is shut off, it should go to a 0 V level.



Table 99. System Power Planes

U.O.	Plane	Controlled By	Description
adefined undef	Devices and Memory	PMC_SLP_S4_N	When PMC_SLP_S4_N goes active, power can be shut off to any circuit not required to wake the system from the S4/S5. Since the memory context does not need to be preserved in the S4/S5 state, the power to the memory can also be shut down. S4 and S5 requests are treated the same so no PMC_SLP_S5_N signal is implemented.
indefined un.	Devices	Implementation Specific	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.
	Suspend	PMC_SUSPWRDNACK	The suspend power planes are generally left on whenever the system has a charged main battery or is plugged in to AC power.
adefined unde		efiner	In some cases, it may be preferable to disable the suspend power planes in S4/S5 states to save additional power. This requires some external logic (such as an embedded controller) to ensure that a wake event is still possible (such as the power button).
undefined un	.,70	defined under	When the SeC is enabled it is advised that the suspend power planes not be removed. Doing so may result in extremely long Sx exit times since the SeC if forced to consider it a cold boot which may, in turn, cause exit latency violations for software using the TXE.
	29 0	1	11/10

18.2.2.3.1 Power Plane Control with PMC_SLP_SOIX_N and PMC_SLP_S4_N

The PMC_SLP_S0IX_N output signal can be used to cut power to any systems supplies that are not required during a S0ix system state.

Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The PMC_SLP_S4_N output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

18.2.2.3.2 PMC_SLP_S4_N and Suspend-To-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The PMC_SLP_S4_N signal should be used to remove power to system memory. The PMC_SLP_S4_N logic in the SoC provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note:

To use the minimum DRAM power-down feature that is enabled by the GEN_PMCON1.S4ASE bit, the DRAM power must be controlled by the PMC_SLP_S4_N signal.



18.2.2.3.3 PMC_CORE_PWROK Signal

When asserted, PMC_CORE_PWROK is an indication to the SoC that its core well power rails are powered and stable. PMC_CORE_PWROK can be driven asynchronously. When PMC_CORE_PWROK is low, the SoC asynchronously asserts PMC_PLTRST_N. PMC_CORE_PWROK must not glitch, even if PMC_RSMRST_N is low.

It is required that the power rails associated with PCI Express have been valid for 99 ms prior to PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST_N deassertion.

Note:

PMC_RSTBTN_N is recommended for implementing the system reset button. This saves external logic that is needed if the PMC_CORE_PWROK input is used. Additionally, it allows for better handling of the processor resets and avoids improperly reporting power failures.

18.2.2.3.4 PMC_BATLOW_N (Battery Low)

The PMC_BATLOW_N input can inhibit waking from S4, and S5 states if there is not sufficient power. It also causes an SMI if the system is already in an S0 state.

18.2.2.4 SMI_N/SCI Generation

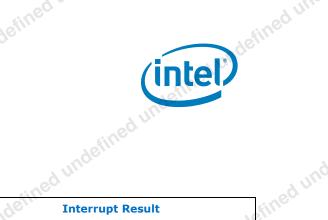
Upon any enabled SMI event taking place while the SMI_EN.EOS bit is set, the SoC will clear the EOS bit and assert SMI to the CPU core, which will cause it to enter SMM space. SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI_N pin.

Once the SMI message has been delivered, the SoC takes no action on behalf of active SMI events until Host software sets the End of SMI (EOS) bit. At that point, if any SMI events are still active, the SoC will send another SMI message.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts IRQs[11:9] or IRQs[23:20]. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not. The interrupt remains asserted until all SCI sources are removed.

Table 100 shows which events can cause an SMI and SCI. Note that some events can be programmed to cause either an SMI or SCI. The usage of the event for SCI (instead of SMI) is typically associated with an ACPI-based system. Each SMI or SCI source has a corresponding enable and status bit.



ed undefined undefined undefineu Table 100. Causes of SMI and SCI (Sheet 1 of 2)

Table 100.	4 under		indefil	Interru	pt Result	
Event	Status Indication ¹	Enable Condition		_EN. I_EN=1b		_EN. I_EN=0b
defined un	Indication	fined unde	PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= 0b	PM1_CNT, SCI_EN= 1b	PM1_CNT. SCI_EN=0 b
Power Button Override ³	PM1_STS_EN. PWRBTNOR_STS	None	SCI	None	SCI	None
RTC Alarm	PM1_STS_EN. RTC_STS	PM1_STS_EN_EN. RTC_EN=1b	SCI	SMI	SCI	None
Power Button Press	PM1_STS_EN. PWRBTN_STS	PM1_STS_EN_EN. PWRBTN_EN=1b	SCI	SMI	SCI	None
SMI_EN.BIOS_RLS bit written to 1b ⁴	PM1_STS_EN. GBL_STS	PM1_STS_EN_EN. GBL_EN=1b	0	S	SCI .	fined w
ACPI Timer overflow (2.34 seconds)	PM1_STS_EN. TMROF_STS	PM1_STS_EN_EN. TMROF_EN =1b	SCI	SMI	SCI	None
GPI[n] ⁹	GPE0a_STS. CORE_GPIO_STS[n] ² or GPE0a_STS. SUS_GPIO_STS[n] ²	GPIO_ROUT[n] = 10b & GPE0a_EN. CORE_GPIO_EN[n] ² = 1b or	SCI	None	SCI	None
bnu	elinea	GPE0a_EN. SUS_GPIO_EN[n] ² =1 b	ued nur			sined u
Internal, Bus 0, PME-Capable Agents (PME_B0)	GPE0a_STS. PME_B0_STS	GPE0_EN. PME_B0_EN=1b	SCI	SMI	SCI	None
BATLOW_N pin goes low	GPE0a_STS. BATLOW_STS_N	GPE0_EN. BATLOW_EN=1b	SCI	SMI	SCI	None
Software Generated GPE	GPE0a_STS. SWGPE_STS	GPE0_EN. SWGPE_EN=1b	SCI	SMI	SCI	None
DOSCI message from GUNIT ⁵	GPE0a_STS. GUNIT_STS	None (enabled by G-Unit ⁸)	SCI	None	SCI	None
ASSERT_SMI message from SPI ⁵	SMI_STS. SPI_SMI_STS	None (enabled by SPI controller)	S	MI	N	one inco
ASSERT_IS_SMI message from USB	SMI_STS. USB_IS_STS	SMI_EN. USB_IS_SMI_EN=1b	S	MI	No.	one
ASSERT_SMI message from USB	SMI_STS.USB_STS	SMI_EN. USB_SMI_EN=1b	S	MI	define N	one
ASSERT_SMI message from iLB ⁵	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	S	MI WI	No	one
Periodic timer expires	SMI_STS. PERIODIC_STS	SMI_EN. PERIODIC_EN=1b		MI	N	one
Datasheet	defi	ed undefined und	efinec		indefined '	indefined



Table 100. Causes of SMI and SCI (Sheet 2 of 2)

	Mineo				Interru	pt Result		dun	
	Event	Status Indication ¹	Enable Condition		_EN. [_EN=1b		_EN. I_EN=0b	definec	
	ed unde	Indication-	4 undefi	PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= Ob	PM1_CNT. SCI_EN= 1b	PM1_CNT. SCI_EN=0 b		
	WDT first expiration	SMI_STS.TCO_STS	SMI_EN.TCO_EN=1b	SI	MI	No	ne		
	64 ms timer expires	SMI_STS. SWSMI_TMR_STS	SMI_EN. SWSMI_TMR_EN=1b	SI	MI	No.	one		
idefine	PM1_CNT.SLP_EN bit written to 1b	SMI_STS. SMI_ON_SLP_EN_S TS	SMI_EN. SMI_ON_SLP_EN =1b	Sync SMI ⁶		Sync SMI ⁶ None		one	sined u
	PM1_CNT.GBL_RLS written to 1b	SMI_STS.BIOS_STS	SMI_EN. BIOS_EN=1b	Sync	SMI ⁶	No	one	ige,,	
	DOSMI message from GUNIT ⁵	SMI_STS. GUNIT_SMI_STS	None (enabled by G-Unit ⁸)	SI	MI	No	one in Co		
	ASSERT_IS_SMI message from iLB ⁵	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	Sync	SMI ⁷	No.	one		
ndefine	GPI[n] ¹⁰	ALT_GPIO_SMI. CORE_GPIO_SMI_S TS[n] ² or ALT_GPIO_SMI. SUS_GPIO_SMI_ST S[n] ²	GPIO_ROUT[n]=01b & ALT_GPIO_SMI. CORE_GPIO_SMI_EN [n] ² =1b or ALT_GPIO_SMI. SUS_GPIO_SMI_EN[n] ² =1b	fined und	MI efined un	No.	one	ndefined	
, stin	USB Per-Port Registers Write Enable bit is changed from 0b to 1b	UPRWC.WE_STS & SMI_STS. USB_IS_STS	UPRWC. WE_SMI_E=1b & SMI_EN. USB_IS_SMI_EN=1b	Sync	SMI ⁶	defined	one		

NOTES:

- 1. Most of the status bits (except otherwise is noted) are set according to event occurrence regardless to the enable bit.
- 2. GPIO status bits are set only if enable criteria is true. GPIO_ROUT[n]=10b & GPE0a EN.x GPIO EN[n] for GPE0a STS.x GPIO STS[n] (SCI). GPIO ROUT[n]=01b & ALT_GPIO_SMI. x_GPIO_SMI_EN[n]=1b for ALT_GPIO_SMI.x_GPIO_SMI_STS[n] (SMI).
- 3. When power button override occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PM1 STS EN.PWRBTNOR STS) is not cleared prior to setting PM1 CNT.SCI EN.
- 4. PM1_STS_EN.GBL_STS being set will cause an SCI, even if the PM1_CNT.SCI_EN bit is not set. Software must take great care not to set the SMI_ENBIOS_RLS bit (which causes PM1_STS_EN.GBL_STS to be set) if the SCI handler is not in place.
- 5. No enable bits for these SCI/SMI messages in the PMC. Enable capability should be implemented in the source unit.
- 6. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding completion to host till SYNC_SMI_ACK message is received from T-Unit.

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- 7. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding the SSMI ACK message to iLB till SYNC SMI ACK message is received from T-
- 8. The G-Unit is an internal functional sub-block which forms part of the graphics functional block.
- 9. The GPE0a_STS.CORE_GPIO_STS[31:24] & GPE0a_EN.CORE_GPIO_EN[31:24] register bits correspond to GPIO S0 SC[7:0]. GPE0a STS.SUS GPIO STS[23:16] & GPE0a_EN.SUS_GPIO_EN[23:16] correspond to GPIO_S5[7:0].
- 10. The ALT_GPIO_SMI.CORE_GPIO_SMI_STS[31:24] & ALT GPIO SMI.CORE GPIO SMI EN[15:8] register bits correspond to GPIO S0 SC[7:0]. ALT_GPIO_SMI.SUS_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI.SUS_GPIO_SMI_EN[7:0] correspond to GPIO_S5[7:0].

18.2.2.5 **Platform Clock Support**

The SoC supports up to 6 clocks (PMC_PLT_CLK[5:0]) with a frequency of 19.2 MHz. These clocks are available for general system use, where appropriate and each have Control and Frequency register fields associated with them.

18.2.2.6 INIT_N (Initialization) Generation

The INIT_N functionality is implemented as a 'virtual wire' internal to the SoC rather than a discrete signal. This virtual wire is asserted based on any one of the events described in below table. When any of these events occur, INIT N is asserted for 16 PCI clocks and then driven high.

INIT_N, when asserted, resets integer registers inside the CPU cores without affecting its internal caches or floating-point registers. The cores then begin execution at the power on Reset vector configured during power on configuration.

Table 101. INIT_N Assertion Causes

Cause
PORT92.INIT_NOW transitions from 0b to1b.
RST_CNT.SYS_RST = 0b and RST_CNT.RST_CPU transitions from 0b to 1b

18.2.3 References

Advanced Configuration and Power Interface Specification, Revision 3.0: http:// Datasheet dundering dunder www.acpi.info/

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18.3 PCU - Fast Serial Peripheral Interface (SPI)

The SoC implements a SPI controller as the interface for BIOS Flash storage. This SPI Flash device is also required to support configuration storage for the firmware for the Trusted Execution Engine. The controller supports a maximum of two SPI Flash devices, using two chip select signals, with speeds of 14.28 MHz, 20 MHz, 25 MHz, 40 MHz or 50 MHz and both have to be Fast SPI. SoC Supports FAST SPI mode.

Note: The default interface speed is 20 MHz.

SPI 'Fast mode' is quad mode.

18.3.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

• Signal Name: The name of the signal/pin.

• **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).

• Type: The buffer type found in Chapter 19, "Electrical Specifications".

• **Description**: A brief explanation of the signal's function.

Table 102. SPI Signals

	Signal Name	Direction /Type	Description
. 1/	FST_SPI_CLK	I/O GPIO	Fast SPI Clock: When the bus is idle, the owner will drive the clock signal low.
defined	FST_SPI_CS[0]_N	I/O GPIO	Fast SPI Chip Select 0: Used as the SPI bus request signal for the first SPI Flash device.
raed und	FST_SPI_CS[1]_N	I/O GPIO	Fast SPI Chip Select 1: Used as the SPI bus request signal for the second SPI Flash devices.
undefil	FST_SPI_CS[2]_N	I/O GPIO	Fast SPI Chip Select 2: Used as the SPI bus request signal for the second SPI Flash devices.
	FST_SPI_D[3:0]	I/O GPIO	Fast SPI Data Pad: Data Input/output pin for the SoC.

Note:

All SPI signals are tri-stated when PMC_RSMRST_N and PMC_CORE_PWROK are asserted. FST_SPI_CS[0:2] and FST_SPI_CLK are not tri-stated.

18.3.2 Features

1) Descriptor Mode Capabilities

a)Two modes of operation

i)Descriptor mode with security access restrictions

Platform Controller Unit (PCU) Overview



- ii)Non-Descriptor mode, no access security restrictions (ICH7 style)
 - (1)BIOS Only
 - (2) If the SPI Flash Signature is invalid, the SPI flash operates in nondescriptor mode
- a. Supports Flash that is divided into 5 regions and accessible by 3 masters
 - i)Regions (5)
 - (1) Flash Descriptor and Chipset Soft Straps
 - (2) BIOS
 - (3) TXE
 - (4) Platform Data
 - ii)Masters (3)
 - (1) Host CPU (for BIOS)
 - (2) TXE
 - iii)Regions are allowed to extend across multiple Flash components
 - iv)Regions are aligned to 4K blocks/sectors
- b. Chipset Soft Strap region provides the ability to use Flash NVM as an alternative to hardware pullup/pulldown resistors for both SoC and the processor Complex
 - i)Each Unit that pulls Soft straps from SPI should have a default value that is used if the Flash Signature is invalid.
- c. The top of the Flash Descriptor contains the Flash Upper Map
- ii)This is used by software to define Flash vendor specific capabilities
- d. The top 256B of the flash descriptor is reserved for use by the OEM

2) Security Capabilities

- a. Descriptor based Region Restriction: Hardware enforced security restricting master accesses to different regions
 - i)Flash Descriptor region settings define separate read/write access to each region per master.
 - ii)Uses SAI for master accesses security checking
 - (1)Soft Strap+fuse to disable sourceID and SAI checks
 - iii)Flash Security Override Pin Strap
 - (1)Removes all descriptor based security
 - (2) Disables the write protection to the BIOS Protected Range 4 (PR4).
 - iv)Each master can grant other masters read/write access to its region
- b. Protected Range Registers.
 - i)3 sets (one for each master) of Lockable Protected Range registers that can restrict program register accesses from the same master.
 - ii)Can span multiple regions

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- iii)Separate read and write protection
- iv)Special case: BIOS PR4 write protect values are received from Soft Strap and affect all masters.
- c. SMI Write Protection for BIOS
 - i)If enabled, will cause an SMI if a program register access occurs. The primary purpose of this requirement is to support SMI based BIOS update utilities.
- d. Illegal Instruction protection for instructions such as Chip Erase
- e. Lockable software sequencing opcodes

3)SPI Flash Access

- a. Direct Read Access
- b. Program Register Access
 - i)Hardware Sequencing
 - (1)Software Sequencing uses HW to provide the basic instructions of read, write, and erase.
 - ii)Software Sequencing
 - (1) Allows SW to use any legal Opcode
- c. Support for Boot BIOS on SPI.
 - i)Non-boot BIOS that is accessible through program register only can be used on SPI when boot BIOS is located on some other interface.
- d. Pre-fetching/Caching to improve performance
 - i)Separate 64B pre-fetch/cache each for HOST and SEC direct read accesses
- 4)SFDP Parameter Discoverability 1
- 5) Flash Component Capabilities
 - a. In Descriptor mode, supports two SPI Flash components using two separate chip select pins, CS0# and CS1#. Only one component supported in non-descriptor mode.
 - i)Components must have the same erasable block/sector size
 - ii)Each component can be up to 16MB (32MB total addressable) using 24-bit addressing.
 - b. 1.8V SPI I/O buffer VCC
 - c. Supports the SPI Fast Read/Write instruction and frequencies of 20MHz, 33MHz and 50 MHz. Supports the SPI Dual Output Fast Read/Write instruction with frequencies of 20 MHz, 33 MHz and 50 MHz
 - d. Supports the SPI Quad Output Fast Read/Write instruction with frequencies of 20 MHz, 33 MHz and 50 MHz
 - e. Uses standardized Flash Instruction Set.
 - f. Supports non-power of 2 flash sizes, with the following restrictions:



- i)Only supported in Descriptor Mode.
- ii)BIOS accesses in non-descriptor mode to a non-binary flash size will not function properly.
- iii)The Flash Regions must be programmed to the actual size of the Flash Component(s).
- iv) If using two flash components, the 1st flash component (the one with the Flash Descriptor) must be of binary size. The 2nd flash component can be a non-binary size. If using only one flash component, it can be of non-binary size.
- v)The value programmed in the Flash Descriptor Component Density must be set to the next power of 2 value larger than the non-binary size.

8) Reset Capabilities

- a. RSMRST#
 - i)When RSMRST# is asserted, SoC will tri-state with a weak pull-up all SPI pins
 - i)The SPI Controller will implement a sideband handshake((handshake is reset warn message)) with PMC when a host reset is requested to allow the SPI Flash controller to complete any outstanding atomic sequences and quiescence the SPI Bus

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18.4 PCU - Universal Asynchronous Receiver/ Transmitter (UART)

This section describes the Universal Asynchronous Receiver/Transmitter (UART) serial port integrated into the PCU. The UART may be controlled through programmed IO.

Note:

Only a minimal ball-count, comprising receive & transmit signals, UART port is implemented. Further, a maximum baud rate of only 115,200 bps is supported. For this reason, it is recommended that the UART port be used for debug purposes only.

18.4.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 103. UART Signals

Signal Name	Direction /Type	Description
UARTO_DATAIN	I/GPIOHV, HS	COM1 Receive: Serial data input from device pin to the receive port. This signal is muxed and may be used by other functions.
UARTO_DATAOU T	O/GPIOHV, HS	COM1 Transmit: Serial data output from transmit port to the device pin. This signal is muxed and may be used by other functions.

18.4.2 Features

The serial port consists of a UART which supports a subset of the functions of the 16550 industry standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor may read the complete status of the UART at any time during the functional operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions.

The serial port may operate in either FIFO or non-FIFO mode. In FIFO mode, a 16-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 16-byte Receive FIFO buffers data from the serial link until read by the processor.



The UART includes a programmable baud rate generator which is capable of generating a baud rate of between 50 bps and 115,200 bps from a fixed baud clock input of 1.8432 MHz. The baud rate is calculated as follows:

Baud Rate Calculation:

BaudRate =
$$\frac{1.8432 \times 10^6}{16 \times \text{Divisor}}$$

The divisor is defined by the Divisor Latch LSB and Divisor Latch MSB registers. Some common values are shown in Table 104.

Table 104. Baud Rate Examples

		A Oriental Control of the Control of		
Desired Baud Rate	Divisor	Divisor Latch LSB Register	Divisor Latch MSB Register	
115,200	1	1h	0h	
57,600	2	2h	0h	
38,400	3	3h	0h	
19,200	6	6h	0h	
9,600	12	Ch	0h	
4,800	24	18h	0h	
2,400	48	30h	0h	
1,200	96	60h	0h	
300	384	80h	1h	
50	2,304	0h	9h	
	115,200 57,600 38,400 19,200 9,600 4,800 2,400 1,200 300	115,200 1 57,600 2 38,400 3 19,200 6 9,600 12 4,800 24 2,400 48 1,200 96 300 384	Desired Baud Rate Divisor Register 115,200 1 1h 57,600 2 2h 38,400 3 3h 19,200 6 6h 9,600 12 Ch 4,800 24 18h 2,400 48 30h 1,200 96 60h 300 384 80h	

The UART has interrupt support and those interrupts may be programmed to the user's requirements, minimizing the computing required to handle the communications link. Each UART may operate in a polled or an interrupt driven environment as configured by software.

18.4.2.1 FIFO Operation

18.4.2.1.1 FIFO Interrupt Mode Operation

Receiver Interrupt

When the Receive FIFO and receiver interrupts are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register (IIR), bit 0 = 1b), receiver interrupts occur as follows:

• The receive data available interrupt is invoked when the FIFO has reached its programmed trigger level. The interrupt is cleared when the FIFO drops below the programmed trigger level.

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- The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, the bits are cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = C6h), as before, has the highest priority. The receiver data available interrupt (IIR = C4h) is lower. The line status interrupt occurs only when the character at the top of the FIFO has errors.
- The COM1_LSR.DR bit is set to 1b as soon as a character is transferred from the shift register to the Receive FIFO. This bit is reset to 0b when the FIFO is empty.

Character Time Out Interrupt

When the receiver FIFO and receiver time out interrupt are enabled, a character time out interrupt occurs when all of the following conditions exist:

- At least one character is in the FIFO.
- The last received character was longer than four continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- The most recent processor read of the FIFO was longer than four continuous character times ago.
- The receiver FIFO trigger level is greater than one.

The maximum time between a received character and a timeout interrupt is 160 ms at 300 baud with a 12-bit receive character (i.e., 1 start, 8 data, 1 parity, and 2 stop bits).

When a time out interrupt occurs, it is cleared and the timer is reset when the processor reads one character from the receiver FIFO. If a time out interrupt has not occurred, the time out timer is reset after a new character is received or after the processor reads the receiver FIFO.

Transmit Interrupt

When the transmitter FIFO and transmitter interrupt are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register, bit 0 = 1b), transmit interrupts occur as follows:

The Transmit Data Request interrupt occurs when the transmit FIFO is half empty or more than half empty. The interrupt is cleared as soon as the Transmit Holding Register is written (1 to 16 characters may be written to the transmit FIFO while servicing the interrupt) or the Interrupt Identification Register is read.

18.4.2.1.2 FIFO Polled Mode Operation

With the FIFOs enabled (FIFO Control register, bit 0=1b), setting Interrupt Enable register (IER), bits 3:0=000b puts the serial port in the FIFO polled mode of operation. Since the receiver and the transmitter are controlled separately, either one or both may be in the polled mode of operation. In this mode, software checks receiver and transmitter status through the Line Status Register (LSR). As stated in the register description:



- LSR[0] is set as long as there is one byte in the receiver FIFO
- LSR[1] through LSR[4] specify which error(s) has occurred for the character at the top of the FIFO. Character error status is handled the same way as interrupt mode. The Interrupt Identification Register is not affected since IER[2] = 0b.
- LSR[5] indicates when the transmitter FIFO needs data.
- LSR[6] indicates that both the transmitter FIFO and shift register are empty.
- LSR[7] indicates whether there are any errors in the receiver FIFO.

18.4.3 Use

18.4.3.1 Base I/O Address

COM1

The base I/O address for the COM1 UART is fixed to 3F8h.

18.4.3.2 Legacy Interrupt

COM₁

The legacy interrupt assigned to the COM1 UART is fixed to IRQ4.

18.4.4 UART Enable/Disable

The COM1 UART may be enabled or disabled using the UART_CONT.COM1EN register bit. By default, the UART is disabled.

Note:

It is recommended that the UART be disabled during normal platform operation. An enabled UART can interfere with platform power management.

18.4.5 IO Mapped Registers

There are 12 registers associated with the UART. These registers share eight address locations in the IO address space. Table 105 shows the registers and their addresses as offsets of a base address. Note that the state of the COM1_LCR.DLAB register bit, which is the most significant bit (MSB) of the Serial Line Control register, affects the selection of certain of the UART registers. The COM1_LCR.DLAB register bit must be set high by the system software to access the Baud Rate Generator Divisor Latches.

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Table 105. Register Access List

gerr		indefine			defined	sined une
(intel	i hed undefine	65	undefin	Platform Controller Unit (PCU) Overvio	ew
defined under	8.5	Register Ma	ap undefine		, undefined	
nde''	Table 105.	Register Access	s List		rined	ed un.
		Register Address (Offset to Base IO Address)	COM1_LCR.DLA B Value	Register Access Type	Register Accessed	undefine
	ind	0h	0b	RO	Receiver Buffer ¹	
sined unde		0h	0b	wo	Transmitter Holding ¹	
		0h	1b	RW	Divisor Latch LSB (Lowest Significant Bit) ¹	
inuo		1h	0b	RW	Interrupt Enable ²	
ined.		1h	1b	RW	Divisor Latch MSB (Most Significant Bit) ²	
defill.		2h	xb	RO	Interrupt Identification ³	, u'
		2h	xb	WO	FIFO Control ³	"Neo
		3h	xb	RW	Line Control	46illi
		4h	xb	RW	Modem Control ⁴	Unc
		5h	xb	RO	Line Status	3
	eg m.	6h	xb	RO	Modem Status ⁴	
		7h	xb	RW	Scratchpad	
undefined und		NOTES: 1. These registers (COM1_RX_TX_2. These registers 3. These registers (COM1_IIR).	_BUFFER). are consolidated i	n the Inter	rupt Enable Register (COM1_IER) rupt Identification / FIFO Control Register	-fined V

NOTES:

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PCU - Intel Legacy Block (iLB) Overview 18.6

The Intel Legacy Block (iLB) is a collection of disparate functional blocks that are critical for implementing the legacy PC platform features. These blocks include:

- "PCU iLB Low Pin Count (LPC) Bridge"
- "PCU iLB Real Time Clock (RTC)"
- "PCU iLB 8254 Timers"
- "PCU iLB High Precision Event Timer (HPET)"
- "PCU iLB GPIO"
- "PCU iLB IO APIC"
- "PCU iLB 8259 Programmable Interrupt Controllers (PIC)"

The iLB also implements a register range for configuration of some of those blocks along with support for Non-Maskable Interrupts (NMI).

18.6.1 **Signal Descriptions**

Refer Chapter 2, "Physical Interfaces" for additional details as well as the subsequent sections.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 106. iLB Signals

Signal Name	Direction /Type	Description
NMI_N undefi	I/GPIOMV, MS	Non-Maskable Interrupt: This is an NMI event indication into the SoC. This signal is muxed and may be used by other functions.

18.6.2 **Features**

18.6.2.1 **Key Features**

The key features of various blocks are as follows:

- LPC Interface
 - Supports Low Pin Count (LPC) 1.1 Specification
 - No support for DMA or bus mastering
 - Supports Trusted Platform Module (TPM) 1.2

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Platform Controller Unit (PCU) Overview



- General Purpose Input Output
 - Legacy control interface for SoC GPIOs
 - I/O mapped registers
- 8259 Programmable Interrupt Controller
 - Supports Legacy interrupt
 - 15 total interrupts through two cascaded controllers
 - I/O mapped registers
- I/O Advanced Programmable Interrupt Controller
 - Supports Legacy-free interrupt
 - 115 total interrupts
 - Memory mapped registers
- 8254
 - Legacy timer support
 - Three timers with fixed uses: System Timer, Refresh Request Signal and Speaker Tone
 - I/O mapped registers
- HPET High Performance Event Timers
 - Supports Legacy-free timer
 - Three timers and one counter
 - Memory mapped registers
- Real-Time Clock (RTC)
 - 242 byte RAM backed by battery (aka CMOS RAM)
 - Can generate wake/interrupt when time matches programmed value
 - I/O and indexed registers

18.6.2.2 Non-Maskable Interrupt

NMI support is enabled by setting the NMI Enable (NMI_EN) bit, at IO Port 70h, Bit 7, to 1b.

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 107.



Table 107. NMI Sources

.no.	NMI Source	NMI Source Enabler/ Disabler	NMI Source Status	Alternate Configuration
d undefined under	SERR# goes active NOTE: A SERR# is only generated internally in the SoC)	NSC.SNE	NSC.SNS	All NMI sources may, alternatively, generate a SMI by setting
	IOCHK# goes active NOTE: A IOCHK# is only generated as a SERIRQ# frame	NSC.INE	NSC.INS	The SoC uses
Indefined	NMI goes active NOTE: Active can be defined as being on the positive or negative edge of the signal using the GNMI.GNMIED register bit.	GNMI.GNMIED	GNMI.GNMIS	GNMI.NMI2SMIST for observing SMI status
ad und	Software sets the GNMI.NMIN register bit	GNMI.NMIN	GNMI.NMINS	defined

18.6.2.3 **S0ix Support**

There is no requirement to set "HPET_GCFG.EN" to 0b. Basically turn off HPET during S0i2/3. RTD3hot status is not a key requirement for OS anymore.

The S1 state described in the HPET spec is a "CPU Stop Grant" condition. This condition is met during the S0i2/3 states, (although entry into S0i2/3 is performed in a different way).

18.6.3 Use

18.6.3.1 **S0ix Support**

Prior to entry into S0i2 or S0i3 state, the driver/OS must set HPET_GCFG.EN to 0b to Datasheet d undefined unde indicate RTD3hot status.



18.7 PCU - iLB - Low Pin Count (LPC) Bridge

The SoC implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the SoC resides in PCI Device 31, Function 0.

Note:

In addition to the LPC bridge interface function, D31:F0 contains other functional units including interrupt controllers, timers, power management, system management, GPIO, and RTC.

18.7.1 **Signal Descriptions**

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 108. LPC Signals

GPIOHV, HS LPC_CLKOUT[0] I/O/ GPIOHV, HS LPC_CLKOUT[1] I/O/ GPIOHV, HS LPC_CLKRUN_N I/O/ GPIOHV, HS I/O/ GPIOHV, H						
GPIOHV, HS Drovided for these signals. These signals are muxed and may be used by other for these signals are muxed and may be used by other for these signals are muxed and may be used by other for these signals are muxed and may be used by other for these signals are muxed and may be used by other for the configured as an input to compensate for board rou soft Strap. LPC_CLKRUN_N	defined	Signal Name		Description		
LPC_CLKOUT[0] I/O/ GPIOHV, HS LPC_CLKOUT[1] I/O/ GPIOHV, HS LPC_CLKRUN_N I/O/ GPIOHV, HS LPC_CLKRUN_N I/O/ GPIOHV, HS LPC_CLKRUN_N I/O/ GPIOHV, HS I/	nuc	LPC_AD[3:0]				
be configured as an input to compensate for board rou Soft Strap. These signals are muxed and may be used by other for drain output used to request starting or speeding up to sustained tri-state signal used by the central resource permission to stop or slow LPC_CLK. The central		LPC_CLKOUT[0]	I JO/ GPIOHV, HS I/O/			
drain output used to request starting or speeding up to sustained tri-state signal used by the central resource permission to stop or slow LPC_CLK. The central resource permission to stop or slow LPC_CLK. The central resource permission to stop or slow LPC_CLK. The central resource permission to stop or slow LPC_CLK. The central resource permission to stop for maintaining the signal in the asserted state when and deasserts the signal to request permission to stop An internal pull-up is provided for this signal. This signal is muxed and may be used by other function for the signal indicates the start of an LPC of This signal is muxed and may be used by other function for the signal is muxed and may be u	ed V	LPC_CLKOUT[1]		be configured as an input to compensate for board routing delays through Soft Strap.		
LPC_SERIRQ I/O/ GPIOHV, HS I/O/ GPIOHV, HS Serial Interrupt Request: This signal implements the protocol. This signal is muxed and may be used by other function NOTE: A level shifter needs to be implemented on this	d undefine	LPC_CLKRUN_N		drain output used to request starting or speeding up LPC_CLK. This is a sustained tri-state signal used by the central resource to request permission to stop or slow LPC_CLK. The central resource is responsible for maintaining the signal in the asserted state when LPC_CLK is running and deasserts the signal to request permission to stop or slow LPC_CLK. An internal pull-up is provided for this signal.		
GPIOHV, HS protocol. This signal is muxed and may be used by other function NOTE: A level shifter needs to be implemented on this		LPC_FRAME_N				
	undefined	LPC_SERIRQ		protocol. This signal is muxed and may be used by other functions.		
ined undefine		204 undefined undef	ined une	Datasheet undefined undefined undefined undefined		

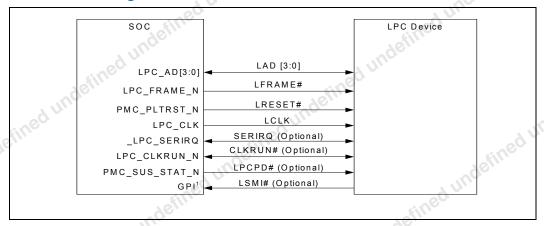


18.7.2 Features

The LPC interface to the SoC is shown in Figure 32. Note that the SoC implements all of the signals that are shown as optional, but peripherals are not required to do so.

Note: The LPC controller does not implement bus mastering cycles or DMA.

Figure 32. LPC Interface Diagram



NOTE: The General Purpose Input (GPI) must use a SMI capable GPIO: GPIO_S0_SC[7:0].

18.7.2.1 Memory Cycle Notes

For cycles below 16M, the LPC Controller will perform standard LPC memory cycles. For cycles targeting firmware (BIOS/EFI code only), firmware memory cycles are used. Only 8-bit transfers are performed. If a larger transfer appears, the LPC controller will break it into multiple 8-bit transfers until the request is satisfied.

If the cycle is not claimed by any peripheral (and subsequently aborted), the LPC Controller will return a value of all 1's to the CPU.

18.7.2.2 Trusted Platform Module (TPM) 1.2 Support

The LPC interface supports accessing Trusted Platform Module (TPM) 1.2 devices via the LPC TPM START encoding. Memory addresses within the range FED00000h to FED40FFFh will be accepted by the LPC Bridge and sent on LPC as TPM special cycles. No additional checking of the memory cycle is performed.

This is different to the FED00000h to FED4BFFFh range implemented on some other Intel components since no Intel[®] Trusted Execution Technology (Intel[®] TXT) transactions are supported.

18.7.2.3 FWH Cycle Notes

If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.



BIOS/EFI boot from LPC is not supported when Secure Boot is enabled.

18.7.2.4 **Subtractive Decode**

All cycles that are not decoded internally, and are not targeted for LPC (i.e., configuration cycles, IO cycles above 64KB and memory cycles above 16MB), will be sent to LPC with LPC FRAME N not asserted.

18.7.2.5 **POST Code Redirection**

Writes to addresses 80h - 8Fh in IO register space will also be passed to the LPC bus.

Note: Reads of these addresses do not result in any LPC transactions.

18.7.2.6 **Power Management**

18.7.2.6.1 LPCPD_N Protocol

Same timings as for PMC SUS STAT N. After driving PMC SUS STAT N active, the SoC drives LPC_FRAME_N low, and tri-states (or drives low) LPC_AD[3:0].

Note:

The Low Pin Count Interface Specification, Revision 1.1 defines the LPCPD_N protocol where there is at least 30 µs from LPCPD_N assertion to LRST_N assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The SoC asserts both PMC_SUS_STAT_N (connects to LPCPD_N) and PLTRST_N (connects to LRST_N) at the same time during a global reset. This is not inconsistent with the LPC LPCPD_N protocol.

Clock Run (CLKRUN) 18.7.2.6.2

When there are no pending LPC cycles, and SERIRQ is in quiet mode, the SoC can shut down the LPC clock. The SoC indicates that the LPC clock is going to shut down by deasserting the LPC_CLKRUN_N signal. LPC devices that require the clock to stay running should drive LPC CLKRUN N N low within 4 clocks of its de-assertion. If no device drives the signal low within 4 clocks, the LPC clock will stop. If a device asserts LPC_CLKRUN_N, the SoC will start the LPC clock and assert LPC_CLKRUN_N.

Note:

The CLKRUN protocol is disabled by default. Refer Section 18.7.3.2.2, "Clock Run Enable" for further details.

Serialized IRQ (SERIRQ)

The interrupt controller supports a serial IRQ scheme. The signal used to transmit this information is shared between the interrupt controller and all peripherals that support serial interrupts. The signal line, LPC_SERIRQ, is synchronous to LPC clock, and follows the sustained tri-state protocol that is used by LPC signals. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

S - Sample Phase: Signal driven low.

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- R Recovery Phase: Signal driven high.
- T Turn-around Phase: Signal released.

The interrupt controller supports 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0- 1, 3-15), the four PCI interrupts, and the control signals SMI_N and IOCHK_N. Serial interrupt information is transferred using three types of frames:

- Start Frame: LPC_SERIRQ line driven low by the interrupt controller to indicate the start of IRQ transmission.
- Data Frames: IRQ information transmitted by peripherals. The interrupt controller supports 21 data frames.
- Stop Frame: LPC_SERIRQ line driven low by the interrupt controller to indicate end of transmission and next mode of operation.

18.7.2.7.1 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame:

- Continuous Mode: The interrupt controller is solely responsible for generating the start frame.
- Quiet Mode: Peripheral initiates the start frame, and the interrupt controller completes it.

These modes are entered via the length of the stop frame.

Continuous mode must be entered first, to start the first frame. This start frame width is 8 LPC clocks. This is a polling mode.

In Quiet mode, the LPC_SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives LPC_SERIRQ low. The interrupt controller senses the line low and drives it low for the remainder of the Start Frame. Since the first LPC clock of the start frame was driven by the peripheral, the interrupt controller drives LPC_SERIRQ low for 1 LPC clock less than in continuous mode. This mode of operation allows for lower power operation.

18.7.2.7.2 Data Frames

Once the Start frame has been initiated, the LPC_SERIRQ peripherals start counting frames based on the rising edge of LPC_SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- Sample Phase: During this phase, a device drives LPC_SERIRQ low if its
 corresponding interrupt signal is low. If its corresponding interrupt is high, then the
 LPC_SERIRQ devices tri-state LPC_SERIRQ. LPC_SERIRQ remains high due to pullup resistors.
- Recovery Phase: During this phase, a device drives LPC_SERIRQ high if it was
 driven low during the Sample Phase. If it was not driven during the sample phase,
 it remains tri-stated in this phase.
- Turn-around Phase: The device tri-states LPC_SERIRQ.

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18.7.2.7.3 **Stop Frame**

After the data frames, a Stop Frame will be driven by the interrupt controller. LPC_SERIRQ will be driven low for two or three LPC clocks. The number of clocks is determined by the SCNT.MD register bit. The number of clocks determines the next mode, as indicated in Table 109.

Table 109. SERIRQ, Stop Frame Width to Operation Mode Mapping

Stop Frame Width	Next Mode
Two LPC clocks	Quiet Mode: Any SERIRQ device initiates a Start Frame
Three LPC clocks	Continuous Mode: Only the interrupt controller initiates a Start Frame

18.7.2.7.4 **Serial Interrupts Not Supported**

There are four interrupts on the serial stream which are not supported by the interrupt controller. These interrupts are:

- IRQ0: Heartbeat interrupt generated off of the internal 8254 counter 0
- IRQ8: RTC interrupt can only be generated internally.
- IRQ13: This interrupt (floating point error) is not supported.

The interrupt controller will ignore the state of these interrupts in the stream.

18.7.2.7.5 **Data Frame Format and Issues**

Table below shows the format of the data frames. The decoded INT[A:D]_N values are ANDed with the corresponding PCI-express input signals (PIRQ[A:D]_N). This way, the interrupt can be shared.

The other interrupts decoded via SERIRQ are also ANDed with the corresponding internal interrupts. For example, if IRQ10 is set to be used as the SCI, then it is ANDed with the decoded value for IRQ10 from the SERIRQ stream.

Table 110. SERIRO Interrupt Mapping

undefine Table 110.				I from the SERIRQ stream.	ined v
	Data Frame #	Interrupt	Clocks Past Start Frame	Comment	ed undeim
ad v	1	IRQ0	2	Ignored. Can only be generated via the internal 8524	
istines	2	IRQ1	5	Before port 60h latch	
indefined undefined	3	SMI_N	8 10	Causes SMI_N if low. Sets SMI_STS.ILB_SMI_STS register bit.	
Sine	4	IRQ3	e ^O 11	4 Unit	
inde	5	IRQ4	14	sine	ed.
d	6	IRQ5	17	index	18fills
2.1	undefine			ndefined b	ned uno
208 ad undefined			indef	Datashee	t
4efine		ć.	ned a	ad une	



Table 110. SERIRQ Interrupt Mapping

11.10				
ndeitt	Data Frame #	Interrupt	Clocks Past Start Frame	Comment
g e	7	IRQ6	20	ed of ut
ndefined undefined undef	8	IRQ7	23	16 tine
ad uli	9	IRQ8	26	Ignored. IRQ8_N can only be generated internally
Stille	10	IRQ9	29	d un
inde	11	IRQ10	32	fine
inged to	12	IRQ11	35	inde
defill	13	IRQ12	38	Before port 60h latch
nuc.	14	IRQ13	41	Ignored.
	15	IRQ14	44	Ignored
	16	IRQ15	47	ineo d'
IInde	17	IOCHCK_N	50	Same as ISA IOCHCK_N going active.
Stined	18	PCI INTA_N	53	nu.
ad unde	19	PCI INTB_N	56	definee
undefined undefined unde	20	PCI INTC_N	59	ined un
n.	21	PCI INTD_N	62	undelli

18.7.2.7.6 S0ix Support

During S0i2 and S0i3, the LPC and SERIRQ interfaces are disabled.

18.7.3 Usage

18.7.3.1 LPC Clock Delay Compensation

In order to meet LPC interface AC timing requirements, a LPC clock loop back is required. The operation of this loop back can be configured in two ways:

- 1. On the SOC: In this configuration, LPC_CLK[0] is looped back on itself on the SOC pad.
 - a. Benefit:

LPC_CLK[0] and LPC_CLK[1] are both available for system clocking

b. Drawback:

Clock delay compensation is less effective at compensating for mainboard delay

c. Soft Strap & Register Requirements:

Soft Strap LPCCLK_SLC = 0b



Configuration is reflected by register bit LPCC.LPCCLK_SLC=0b

Soft Strap LPCCLK1_ENB = 0b (LPC_CLK[1] disabled) or 1b (LPC_CLK[1] enabled)

- 2. Configuration is reflected by register bit LPCC.LPCCLK1EN=0b (LPC_CLK[1] disabled) or 1b (LPC_CLK[1] enabled)
- 3. On the main board: In this configuration, LPC_CLK[0] is looped back to LPC_CLK[1] on the main board.
 - a. Benefit:

Clock delay compensating in more effective at compensating for main board delay

b. Drawback:

Only LPC_CLK[0] is available for system clocking. LPC_CLK[1] must be disabled.

c. Soft Strap & Register Requirements:

Soft Strap LPCCLK_SLC = 1b

Configuration is reflected by register bit LPCC.LPCCLK_SLC=1b

Soft Strap LPCCLK1_ENB = 0b (LPC_CLK[1] disabled)

Configuration is reflected by register bit LPCC.LPCCLK1EN=0b

18.7.3.2 LPC Power Management

18.7.3.2.1 Clock Enabling

The LPC clocks can be enabled or disabled by setting or clearing, respectively, the LPCC.LPCCLK[1:0]EN bits.

18.7.3.2.2 Clock Run Enable

The Clock Run protocol is disabled by default and should only be enabled during operating system run-time, once all LPC devices have been initialized. The Clock Run protocol is enabled by setting the LPCC.CLKRUN_EN register bit.

18.7.3.3 SERIRQ Disable

Serialized IRQ support may be disabled by setting the OIC.SIRQEN bit to 0b.

18.7.4 References

- Low Pin Count Interface Specification, Revision 1.1 (LPC): http://www.intel.com/design/chipsets/industry/lpc.htm.
- Serialized IRQ Support for PCI Systems, Revision 6.0: http://www.smsc.com/media/Downloads_Public/papers/serirq60.doc.
- Implementing Industry Standard Architecture (ISA) with Intel[®] Express Chipsets (318244): http://www.intel.com/assets/pdf/whitepaper/318244.pdf.



18.8 PCU - iLB - Real Time Clock (RTC)

The SoC contains a real-time clock with 242 bytes of battery-backed RAM. The real-time clock performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 kHz crystal and a 3.3 V battery.

The RTC supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC supports a date alarm that allows for scheduling a wake up event up to 30 days in advance.

18.8.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- **Description**: A brief explanation of the signal's function.

Table 111. RTC Signals

, _n d	Signal Name	Direction /Type	Description
adefined U.	RTC_X1	I Analog	Crystal Input 1: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal can be driven with the desired clock rate.
Jefined un	RTC_X2	I Analog	Crystal Input 2: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal should be left floating.
Junos un	RTC_RST_N	I	RTC Reset: When asserted, this signal resets register bits in the RTC well. NOTE: Unless CMOS is being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. NOTE: In the case where the RTC battery is dead or missing on the platform, the signal should be deasserted before the PMC_RSMRST_N signal is deasserted.
ed undefined under	RTC_TEST_N	ed nugeri	RTC Battery Test: An external RC circuit creates a time delay for the signal such that it will go high (to ILB_RTC_3P3_G3) sometime after the battery voltage is valid. The RC time delay should be in the 10-20 ms range. This signal will be asserted just after suspend power is up if the coin cell battery is weak. NOTE: This signal may also be used for debug purposes, as part of a XDP port.

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18.8.2 Features

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 ms to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola* MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

18.8.2.1 Update Cycles

An update cycle occurs once a second, if the B.SET bit is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle starts at least 488 ms after A.UIP is asserted, and the entire cycle does not take more than 1984 ms to complete. The time and date RAM locations (00h to 09h) are disconnected from the external bus during this time.

18.8.3 Interrupts

The real-time clock interrupt is internally routed within the SoC both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the SoC, nor is it shared with any other interrupt. IRQ8# from the ILB_LPC_SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

18.8.3.1 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked: the RC.UL and RC.LL register bits. When the locking bits are set, the corresponding range in the RAM is not readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to re-lock the RAM range.

18.8.3.2 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an SoC-based platform can be done by using a jumper on RTC_RST_N or a GPI. Implementations should not attempt to clear CMOS by using a jumper to pull RTC_VCC low.



Using RTC RST N to Clear CMOS 18.8.3.2.1

A jumper on RTC RST N can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTC_RST_N is strapped to ground, the GEN_PMCON1.RPS register bit will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTC_RST_N to be pulled up through a weak pull-up resistor. Table 112 shows which bits are set to their default state when RTC_RST_N is asserted. This RTC_RST_N jumper technique allows the jumper to be moved and then replaced—all while the system is powered off. Then, once booted, the sfined undefined undefined uni GEN_PMCON1.RPS bit can be detected in the set state.

Table 112. Register Bits Reset by RTC RST N Assertion

			_ 4 / 1 / 2
	Register Bit	Bit(s)	Default State
	RCRB_GENERAL_CONTROL.TS		xb
	GEN_PMCON1.PME_B0_S5_DIS	15	0b
edu	GEN_PMCON1.WOL_EN_OVRD	13	0b
tefine	GEN_PMCON1.DIS_SLP_X_STRCH_SUS_UP	12	0b
Illinois	GEN_PMCON1.RTC Reserved	8	0b
undefined undefined und	GEN_PMCON1.SWSMI_RATESEL	7:6	00b
defill	GEN_PMCON1.S4MAW	5:4	00b
Ulu	GEN_PMCON1.S4ASE	3	0b
	GEN_PMCON1.RPS	2	1b
	GEN_PMCON1.AG3E	0	0b
nu ,	PM1_STS_EN.RTC_EN	26	0b
	PM1_STS_EN.PWRBTNOR_STS	11	0b
	PM1_CNT.SLP_TYP	12:10	0b
ined undefined un	GPE0a_EN.PME_B0_EN	13	0b
	GPE0a_EN.BATLOW_EN	10	0b Jin

undefined undefined und **Using GPI to Clear CMOS**

A jumper on a GPI can also be used to clear CMOS values. BIOS should detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note:

The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

Warning: Do not implement a jumper on RTC_VCC to clear CMOS.

18.8.3.4 **S0ix Support**

During S0i3, the RTC interface is active.



18.8.4 References

Accessing the Real Time Clock Registers and the NMI Enable Bit: http://download.intel.com/design/intarch/PAPERS/321088.pdf.

18.8.5 IO Mapped Registers

The RTC internal registers and RAM is organized as two banks of 128 bytes each, called the standard and extended banks.

Note: It is not possible to disable the extended bank.

The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/O space.

Note: Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank. Registers reg_RTC_RIR_type and reg_RTC_RTR_type are used for data movement to and from the extended bank. All of these registers have alias I/O

locations, as indicated in Table 113.

Table 113. I/O Registers Alias Locations

Register	Original I/O Location	Alias I/O Location
reg_RTC_IR_type	70h	74h
reg_RTC_TR_type	71h	75h
reg_RTC_RIR_type	72h	76h
reg_RTC_RTR_type	73h	77h

18.8.6 Indexed Registers

The RTC contains indexed registers that are accessed via the reg_RTC_IR_type and reg_RTC_TR_type registers.

Table 114. RTC Indexed Registers (Sheet 1 of 2)

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week



Table 114. RTC Indexed Registers (Sheet 2 of 2)

ino	ler Unit (PCU) Overview	46 ill	(inte	
lefined L	ine	dunc	ed uneer	
Table 114. R	ler Unit (PCU) Overview CC Indexed Registers (Si	neet 2 of 2)	undefined under	
	Start	End	Name	define
	07h	07h	Day of Month	FILE
	08h	08h	Month	"Vge,
46/11/	09h	09h	Year	9,0
4 une	0Ah	0Ah	Register A	
eineo.	0Bh	0Bh	Register B	
delli	0Ch	0Ch	Register C	
-dull	0Dh	0Dh	Register D	
Vec	UEN	7FN	114 Bytes of User RAM	
hed undefined undefined	defill			
	4 unc			48/11/
		ed u.		undi
nder.		efine		
od un.		Inoc	defi	
Sine			4 une	
inde	Aefill		sineu.	
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18.9 **PCU - iLB - 8254 Timers**

The 8254 contains three counters which have fixed uses including system timer and speaker tone. All registers are clocked by a 14.31818 MHz clock.

18.9.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- Description: A brief explanation of the signal's function.

18.9.2 Features

18.9.2.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

18.9.2.2 Counter 1, Refresh Request Signal

This counter is programmed for Mode 2 operation and impacts the period of the NSC.RTS register bit. Programming the counter to anything other than Mode 2 results in undefined behavior.

18.9.2.3 Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to the NSC.SDE register bit.

18.9.2.4 **SOix Support**

During S0i2 and S0i3, the 8254 timer is halted. A platform that requires the 8254 timer to be always active, should disable S0i2/3 using the S0ix_Enable register.



18.9.3 **Usage**

18.9.3.1 **Timer Programming**

The counter/timers are programmed in the following fashion:

- 1. Write a control word to select a counter.
- 2. Write an initial count for that counter.
- 3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
- 4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- Control Word Command. Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- Counter Latch Command. Latches the current count so that it can be read by the system. The countdown process continues.
- Read Back Command. Reads the count value, programmed mode, the current Fined undefined state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 115 lists the six operating modes for the interval counters.

Table 115. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware re-triggerable one- shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.



Table 115. Counter Operating Modes

Mode	Function	Description
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

18.9.3.2 Reading from Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

18.9.3.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through Port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

Note:

Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing 0b to the NSC.TC2E register bit.

18.9.3.2.2 Counter Latch Command

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.



18.9.3.2.3 **Read Back Command**

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/ O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

Datasheet dunderined underined under underined under underined under u If both count and status of a counter are latched, the first read operation from that



18.10 PCU - iLB - High Precision Event Timer (HPET)

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and three timers.

18.10.1 Features

18.10.1.1 Non-Periodic Mode - All Timers

This mode can be thought of as creating a one-shot. When a timer is set up for non-periodic mode, it generates an interrupt when the value in the main counter matches the value in the timer's comparator register. As timers 1 and 2 are 32-bit, they will generate another interrupt when the main counter wraps.

TOCV cannot be programmed reliably by a single 64-bit write in a 32-bit environment unless only the periodic rate is being changed. If TOCV needs to be re-initialized, the following algorithm is performed:

- 1. Set T0C.TVS
- 2. Set T0CV[31:0]
- 3. Set T0C.TVS
- 4. Set T0CV[63:32]

Every timer is required to support the non-periodic mode of operation.

18.10.1.2 Periodic Mode - Timer 0 Only

When set up for periodic mode, when the main counter value matches the value in TOCV, an interrupt is generated (if enabled). Hardware then increases TOCV by the last value written to TOCV. During run-time, TOCV can be read to find out when the next periodic interrupt will be generated. Software is expected to remember the last value written to TOCV.

Example: if the value written to TOCV is 00000123h, then

- An interrupt will be generated when the main counter reaches 00000123h.
- TOCV will then be adjusted to 00000246h.
- Another interrupt will be generated when the main counter reaches 00000246h.
- T0CV will then be adjusted to 00000369h.

When the incremented value is greater than the maximum value possible for ToCV, the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h.



If software wants to change the periodic rate, it writes a new value to TOCV. When the timer's comparator matches, the new value is added to derive the next matching point. If software resets the main counter, the value in the comparator's value register must also be reset by setting TOC.TVS. To avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

- 1. Software clears GCFG.EN to prevent any interrupts.
- 2. Software clears the main counter by writing a value of 00h to it.
- 3. Software sets T0C.TVS.
- 4. Software writes the new value in TOCV.
- 5. Software sets GCFG.EN to enable interrupts.

18.10.1.2.1 Interrupts

If each timer has a unique interrupt and the timer has been configured for edgetriggered mode, then there are no specific steps required. If configured to leveltriggered mode, then its interrupt must be cleared by software by writing a '1' back to the bit position for the interrupt to be cleared.

Interrupts associated with the various timers have several interrupt mapping options. Software should mask GCFG.LRE when reprogramming HPET interrupt routing to avoid spurious interrupts.

18.10.1.2.2 Mapping Option #1: Legacy Option (GCFG.LRE set)

Table 116, 8254 Interrupt Mapping

Mappir	ng Option #1	: Legacy Opti	on (GCFG.LRE set)	ined u
efine	ces the followi		defined unoe	d under.
Timer	8259 Mapping	APIC Mapping	Comment	
0	IRQ0	IRQ2	The 8254 timer will not cause any interrupts	
1	IRQ8	IRQ8	RTC will not cause any interrupts.	
2	T2C.IR	T2C.IRC	1260	2,1

18.10.1.2.3 Mapping Option #2: Standard Option (GCFG.LRE cleared)

Each timer has its own routing control. The interrupts can be routed to various interrupts in the I/O APIC. T[2:0]C.IRC indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any other interrupts.

S0ix Support

During S0i1, the HPET is kept running. During S0i2 & S0i3, the HPET is halted.



18.10.1.4 S0ix Support

Prior to entry into S0i2 or S0i3 state, the driver/OS must set HPET_GCFG.EN to 0b to indicate RTD3 $_{
m hot}$ status.

18.10.2 References

IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a: http://www.intel.com/hardware design/hpetspec_1.pdf.

18.10.3 Memory Mapped Registers

The register space is memory mapped to a 1K block at address FED00000h. All registers are in the core well. Accesses that cross register boundaries result in undefined behavior.



18.11 PCU - iLB - GPIO

187 GPIOs are available for use. Most of these GPIOs can be used as legacy GPIOs. This chapter describes their use as legacy GPIOs.

18.11.1 Signal Descriptions

Refer Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin.
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional).
- Type: The buffer type found in Chapter 19, "Electrical Specifications".
- Description: A brief explanation of the signal's function.

18.11.2 Features

GPIOs can generate general purpose events (GPEs) on rising and/or falling edges.

18.11.2.1 GPIO Controller

The GPIO controllers handle all GPIO interface to SoC,

- GPIO NORTH used for Camera sensors, DFX, SVID, and Display Pins.
- GPIO SOUTHEAST Defines the pads/Pins for MMC/SD host controller, LPC pins, FAST SPI pins and Platform Clock.
- GPIO SOUTHWEST Defines the Pads/Pins for HS UART, I2S HS, LPE, PCIe and SPI pins.
- GPIO EAST Defines the Pads/Pins for SoC power state related signals of PMU and ISH pins.

18.11.3 Usage

Each GPIO has six registers that control how it is used, or report its status:

- Use Select
- I/O Select
- GPIO Level
- Trigger Positive Edge
- Trigger Negative Edge
- Trigger Status

The Use Select register selects a GPIO pin as a GPIO, or leaves it as its programmed function. This register must be set for all other registers to affect the GPIO.

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The I/O Select register determines the direction of the GPIO.

The Trigger Positive Edge and Trigger Negative Edge registers enable general purpose events on a rising and falling edge respectively. This only applies to GPIOs set as input.

The Trigger Status register is used by software to determine if the GPIO triggered a GPE. This only applies to GPIOs set as input and with one or both of the Trigger modes enabled.

Additionally, there is one additional register for each S5 GPIO:

• Wake Enable

This register allows S5 GPIOs to trigger a wake event based on the Trigger registers' settings.

18.11.4 GPIO Registers

18.11.4.1 SD Card and LPC Pins (3.3V versus 1.8V Modes)

The CFIO cells for both the SD Card Pins (SDMMC3_*) and LPC (LPC_*) are 3.3V capable.

To use as 1.8V IOs:

- Set power supply to 1.8V for the pads.
- Set v1p8mode in family configuration register.
- Trigger a RCOMP cycle using Family RCOMP register
- Copy RCOMP value to Family p and n strength values.

Note: All GPIO registers must be accessed as double words. Unpredictable results will occur

otherwise.

Note: All MMIO GPIO *_PAD_VAL's must set Ienenb = 0 in order to read the pad_val of the

GPIO. This applies to RO GPIO's as well.

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18.12 PCU - iLB - Interrupt Decoding and Routing

The interrupt decoder is responsible for receiving interrupt messages from other devices in the SoC and decoding them for consumption by the interrupt router, the "PCU - iLB - 8259 Programmable Interrupt Controllers (PIC)" and/or the "PCU - iLB - IO APIC".

The interrupt router is responsible for mapping each incoming interrupt to the appropriate PIRQx, for consumption by the "PCU - iLB - 8259 Programmable Interrupt Controllers (PIC)" and/or the "PCU - iLB - IO APIC".

18.12.1 Features

18.12.1.1 Interrupt Decoder

The interrupt decoder receives interrupt messages from devices in the SoC. These interrupts can be split into two primary groups:

- For consumption by the interrupt router
- For consumption by the 8259 PIC

For Consumption by Interrupt Router

When a PCI-mapped device in the SoC asserts or de-asserts an INT[A:D] interrupt, an interrupt message is sent to the decoder. This message is decoded to indicate to the interrupt router which specific interrupt is asserted or de-asserted and which device the INT[A:D] interrupt originated from.

For Consumption by the 8259 PIC

When a device in the SoC asserts or de-asserts a legacy interrupt (IRQ), an interrupt message is sent to the decoder. This message is decoded to indicate to the 8259 PIC, which specific interrupt (IRQ[3, 4, 14 or 15]) was asserted or de-asserted.

18.12.1.2 Interrupt Router

The interrupt router aggregates the INT[A:D] interrupts for each PCI-mapped device in the SoC, received from the interrupt decoder, and the INT[A:D] interrupts direct from the Serialized IRQ controller. It then maps these aggregated interrupts to 8 PCI based interrupts: PIRQ[A:H]. This mapping is configured using the IR[31:0] registers.

PCI based interrupts PIRQ[A:H] are then available for consumption by either the 8259 PICs or the IO-APIC, depending on the configuration of the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH.



Routing PCI Based Interrupts to 8259 PIC

The interrupt router can be programmed to allow PIRQA-PIRQH to be routed internally to the 8259 as ISA compatible interrupts IRQ 3–7, 9–12 & 14–15. The assignment is programmable through the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH. One or more PIRQs can be routed to the same IRQ input. If ISA Compatible Interrupts are not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The SoC internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.



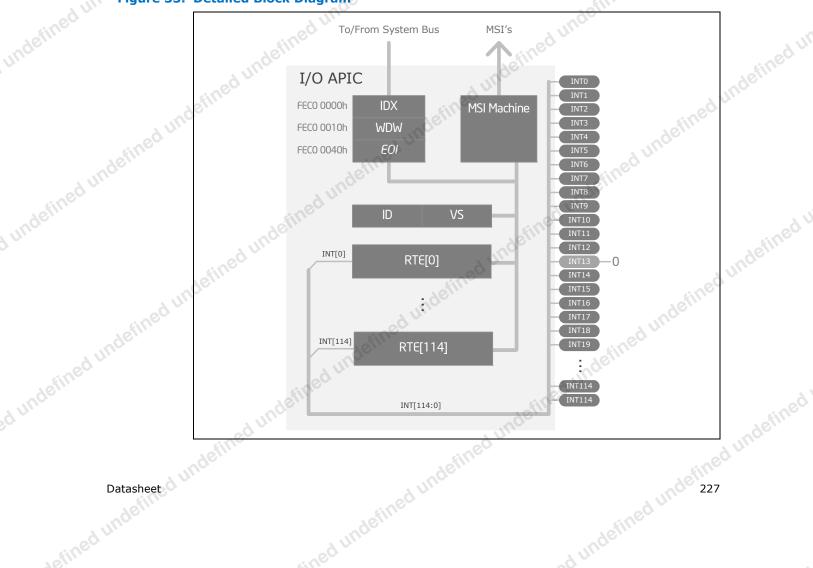
PCU - iLB - IO APIC 18.13

The IO Advanced Programmable Interrupt Controller (APIC) is used to support line interrupts more flexibly than the 8259 PIC. Line interrupts are routed to it from multiple sources, including legacy devices, via the interrupt decoder and serial IRQs, or they are routed to it from the interrupt router in the iLB. These line based interrupts are then used to generate interrupt messages targeting the local APIC in the processor.

18.13.1 **Features**

- 115 interrupt lines
 - IRQ0-114
- Edge or level trigger mode per interrupt
- Active low or high polarity per interrupt
- Works with local APIC in processor via MSIs
- MSIs can target specific processor core
- Established APIC programming model

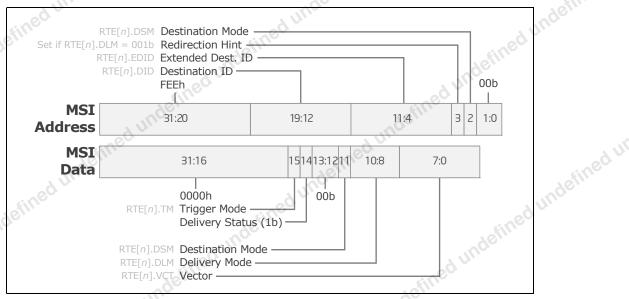
Figure 33. Detailed Block Diagram





MSIs generated by the I/O APIC are sent as 32-bit memory writes to the Local APIC. The address and data of the write transaction are used as follows.

Figure 34. MSI Address and Data



Destination ID (DID) and Extended Destination ID (EDID) are used to target a specific processor core's local APIC.

18.13.2 Usage

The I/O APIC contains indirectly accessed I/O APIC registers and normal memory mapped registers. There are three memory mapped registers:

- Index Register (IDX)
- Window Register (WDW)
- End Of Interrupt Register (EOI)

The Index register selects an indirect I/O APIC register (ID/VS/RTE[n]) to appear in the Window register.

The Window register is used to read or write the indirect register selected by the Index register.

The EOI register is written to by the Local APIC in the processor. The I/O APIC compares the lower eight bits written to the EOI register to the Vector set for each interrupt (RTE.VCT). All interrupts that match this vector will have their RTE.RIRR register cleared. All other EOI register bits are ignored.



Indirect I/O APIC Registers 18.13.3

These registers are selected with the IDX register, and read/written through the WDW register. Accessing these registers must be done as DW requests, otherwise unspecified behavior will result. Software should not attempt to write to reserved registers. Reserved registers may return non-zero values when read.

Note: There is one pair of redirection (RTE) registers per interrupt line. Each pair forms a 64-

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18.14 PCU - iLB - 8259 Programmable Interrupt Controllers (PIC)

SoC provides an ISA-compatible programmable interrupt controller (PIC) that incorporates the functionality of two, cascaded 8259 interrupt controllers.

18.14.1 Features

In addition to providing support for ISA compatible interrupts, this interrupt controller can also support PCI based interrupts (PIRQs) by mapping the PCI interrupt onto a compatible ISA interrupt line. Each 8259 controller supports eight interrupts, numbered 0-7. Table 117 shows how the controllers are connected.

Note:

SoC does not implement any external PIRQ# signals. The PIRQs referred to in this chapter originate from the interrupt routing unit.

Table 117. Interrupt Controller Connections

undefined undefined	8259	8259 Input	Connected Pin / Function
ined une	Master	0	Internal Timer / Counter 0 output or HPET #0; determined by GCFG.LRE register bit
defill		1	IRQ1 using SERIRQ, Keyboard Emulation
UNG		2	Slave controller INTR output
	60	3	IRQ3 via SERIRQ, PIRQx or PCU UART 1
	efine	4	IRQ4 via SERIRQ or PIRQx
1100		5	IRQ5 via SERIRQ or PIRQx
ined "		6	IRQ6 via SERIRQ or PIRQx
undefined undefined und		7	IRQ7 via SERIRQ or PIRQx
d line	Slave	0	Inverted IRQ8# from internal RTC or HPET
<i>sined</i>		1	IRQ9 via SERIRQ, SCI or PIRQx
nder.		2	IRQ10 via SERIRQ, SCI or PIRQx
d un		3	IRQ11 via SERIRQ, SCI, HPET or PIRQx
	· ve	4	IRQ12 via SERIRQ, PIRQx or mouse emulation
	46fill.	5	None
A 1/2		6	PIRQx
fineu		7	IRQ15 via SERIRQ or PIRQx o

The SoC cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the SoC PIC.

Interrupts can be programmed individually to be edge or level, except for IRQ0, IRQ2 and IRQ8#.



Note:

Active-low interrupt sources (such as a PIRQ#) are inverted inside the SoC. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term "high" indicates "active," which means "low" on an originating PIRO#.

18.14.1.1 **Interrupt Handling**

Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 118 defines the IRR, ISR, and IMR.

Table 118. Interrupt Status Registers

	Bit	Description
ad und	IRR	Interrupt Request Register. This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode.
undefines	ISR	Interrupt Service Register. This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
1efineo	IMR	Interrupt Mask Register. This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.
nuge	Ackno	wledging Interrupts

Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated into a Interrupt Acknowledge Cycle to the SoC. The PIC translates this command into two internal INTA# pulses expected by the 8259 controllers. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon the ICW2.IVBA bits, combined with the ICW2.IRL bits representing the interrupt within that controller.

Note:

References to ICWx and OCWx registers are relevant to both the master and slave 8259 controllers.

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Table 119. Content of Interrupt Vector Byte

UOC	Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
	IRQ7,15	, una	111
	IRQ6,14	eineo.	110
	IRQ5,13	dein	101
ined	IRQ4,12	TCM/2 TVPA	100
adefills	IRQ3,11	ICW2.IVBA	011
	IRQ2,10	-	010
afined by	IRQ1,9	-	001
	IRQ0,8	cini	000
7.	11/10	dett	

Hardware/Software Interrupt Sequence

- 1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
- 2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
- 3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle.
- 4. Upon observing the special cycle, the SoC converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
- 5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
- 6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
- 7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

18.14.1.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the SoC, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.



ICW₁

A write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

- 1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
- 2. The Interrupt Mask Register is cleared.
- 3. IRQ7 input is assigned priority 7.
- 4. The slave mode address is set to 7.
- 5. Special mask mode is cleared and Status Read is set to IRR.

ICW₂

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the SoC, IRQ2 is used. Therefore, MICW3.CCC is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an
 interrupt acknowledge cycle. On interrupt acknowledge cycles, the master
 controller broadcasts a code to the slave controller if the cascaded interrupt won
 arbitration on the master controller. The slave controller compares this
 identification code to the value stored in its ICW3, and if it matches, the slave
 controller assumes responsibility for broadcasting the interrupt vector.

ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, ICW4.MM must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

18.14.1.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

OCW1 masks and unmasks interrupt lines



- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

18.14.1.4 Modes of Operation

Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked
 out from the master's priority logic and further interrupt requests from higher
 priority interrupts within the slave are recognized by the master and initiate
 interrupts to the processor. In the normal-nested mode, a slave is masked out
 when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the
 interrupt serviced was the only one from that slave. This is done by sending a NonSpecific EOI command to the slave and then reading its ISR. If it is 0, a non-specific
 EOI can also be sent to the master.

Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2.REOI; the Rotation on Non-Specific EOI Command (OCW2.REOI=101b) and the rotate in automatic EOI mode which is set by (OCW2.REOI=100b).



Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: OCW2.REOI=11xb, and OCW2.ILS is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (OCW2.REOI=111b) and OCW2.ILS=IRQ level to receive bottom priority.

Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting OCW3.PMC. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in Bit 7 if there is an interrupt, and the binary code of the highest priority level in Bits 2:0.

Edge and Level Triggered Mode

In ISA systems this mode is programmed using ICW1.LTIM, which sets level or edge for the entire controller. In the SoC, this bit is disabled and a register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

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18.14.1.5 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when the ICW4.AEOI bit is set to 1.

Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the SoC, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI.

An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

Note:

Both the master and slave PICs have an AEOI bit: MICW4.AEOI and SICW4.AEOI respectively. Only the MICW4.AEOI bit should be set by software. The SICW4.AEOI bit should not be set by software.

18.14.1.6 Masking Interrupts

Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.



The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern.

The special mask mode is set by OCW3.ESMM=1b & OCW3.SMM=1b, and cleared where OCW3.ESMM=1b & OCW3.SMM=0b.

18.14.1.7 **S0ix Support**

During S0i2 & S0i3, the 8259 PICs are disabled. A platform that requires the 8259 PICs to be always active, should disable S0i2/3 using the S0ix_Enable register.

18.14.2 **IO Mapped Registers**

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions, depending upon the data written to them. Table 120 is a description of the different register possibilities for each address.

Note: The register descriptions after Table 120 represent one register possibility.

Table 120. I/O Registers Alias Locations

	A D. V		
nuc	Registers	Original I/O Location	Alias I/O Locations
	eineo	od ui	24h
	MICW1	ight	28h
ed ull	MICWI	Inde	2Ch
undefined undefined un	MOCW2	20h	30h
inde	MOCW3		34h
	1100W3		38h
defille	"ineo		3Ch
	ode,	Nil.	25h
	MICW2	inde	29h
	MICW3	raed to	2Dh
71.	A. C.	21h	31h
edu	MICW4	4 Unit	35h
defille	MOCW1	efined undefin	39h
unde	60	E //	3Dh
d undefined undefined ut	indefined undefined und	defined undefined undefil	led unot
	ined unit	ad under	
Datasheet	Indell	indefine	ndefine
Bacasilect		ined	d ullie 23,
Datasneet		Jefii.	defined under 237

. A . indefined undefined undefined



I/O Registers Alias Locations **Table 120.**

Registers	Original I/O Location	Alias I/O Locations
Illian	delli	A4h
CICWI	dune	A8h
SICWI	sinec	ACh
SOCW2	A0h	B0h
SOCW3	ed ui	B4h
Soews		B8h
unoc		BCh
ineo.		A5h
SICW2	7117	A9h
SICW3	inde.	ADh
einec.	A1h	B1h
SICW4	ie fine	B5h
SOCW1	Inoc	B9h
	ned to	BDh
ELCR1	4D0h	N/A
ELCR2	4D1h	N/A
	SICW1 SOCW2 SOCW3 SICW2 SICW3 SICW4 SOCW1 ELCR1	SICW1 SOCW2 A0h SOCW3 SICW2 SICW3 SICW4 SOCW1 ELCR1 4D0h

undefined undefined und



19 Electrical Specifications

This chapter is categorized into the following sections:

- "Absolute Maximum and Minimum Specifications"
- "Thermal Specifications"
- "Storage Conditions"
- "Voltage and Current Specifications"
- "Crystal Specifications"
- "DC Specifications"

19.1 Absolute Maximum and Minimum Specifications

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the SoC, but with possible reduced life expectancy once returned to function limits.

At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Although the processor contains protective circuitry to resist damage from Electrostatic discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

19.2 Thermal Specifications

These specifications define the operating thermal limits of the SoC. Thermal solutions not designed to provide the following level of thermal capability may affect the long-term reliability of the processor and system, but more likely result in performance throttling to ensure silicon junction temperatures within specification.

This section specifies the thermal specifications for all SKUs. Some definitions are needed, however. "Tj Max" defines the maximum operating silicon junction temperature. Unless otherwise specified, all specifications in this document assume Tj Max as the worse case junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed CPU and graphics frequencies. "TDP" defines the thermal dissipated power for a worse case estimated real world thermal scenario. "SDP", or scenario dissipated power, defines the thermal dissipated power under a lighter workload specific to a user scenario and at a lower thermal junction temperature than Tj Max. Note that turbo frequencies are opportunistically selected when thermal headroom exists. Automatic throttling along with a proper thermal solution ensure Tj Max will not be exceeded.

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Table 121. Thermal Specifications

Thermal Specifications		ad undern	und
"uge,	T4	Т3	ined .
T _j Max	90 °C	90 °C	deir
T _j Min	0 °C	0 °C	ed mi.
T _j @ Max. Steady State Power (SDP)	70 °C	70 °C	No.
SDP	2W	2.2 W]

Storage Conditions

This section specifies absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 122. Storage Conditions Prior to Board Attach

raed or	Symbol	Parameter	Min	Max	
Indefil.	Tabsolute storage	Device storage temperature when exceeded for any length of time.	-25 °C	125 °C	ed!
	Tshort term storage	The ambient storage temperature and time for up to 72 hours.	-25 °C	85 °C	indefille
	Tsustained storage	The ambient storage temperature and time for up to 30 months.	5 °C	40 °C	edu
lefined s	RHsustained storage	The maximum device storage relative humidity for up to 30 months.		60% @ 24 °C	
od unac	NOTES:	Indeili	76	fine	-
undefines	Exceptions for su	ratures are not to exceed values based urface mount re-flow are specified by th dherence may affect processor reliabilit	ne applical		fined
	• Component proc	luct device storage temperature qualific	ation mot	hode may follow	76,

NOTES:

- Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount re-flow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
- Component product device storage temperature qualification methods may follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards when applicable for volatile memory.
- Component stress testing is conducted in conformance with JESD22-A104.
- The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.



19.3.1 Post Board-Attach

The storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component-level certification assessments post board-attach given the multitude of attach methods, socket types, and board types used by customers.

Provided as general guidance only, board-level Intel-branded products are specified and certified to meet the following temperature and humidity limits:

- Non-Operating Temperature Limit: -40 °C to 70 °C
- Humidity: 50% to 90%, non-condensing with a maximum wet-bulb of 28 °C

19.4 Voltage and Current Specifications

The I/O buffer supply voltages are specified at the SoC package balls. The tolerances shown in Table 138 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 124 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Note:

The SoC is a pre-launch product. Voltage and current specifications are subject to change.

Table 123. SoC Power Rail DC Specs and Max Current

defined undefined	Platform Rail	4efined L	Voltage Tolerances	Max Icc	June .
ad un	V1P05A	UNCORE1_V1P05A_G3		oge,,	
Sine		UNCORE2_V1P05A_G3	Α'		
inde	defil	DDR_V1P05A_G3	1.05 V		edv
3	4 une	USB3_V1P05A_G3	DC: ±2%	1700 mA	define
	eiu _{eo}	USBSSIC_V1P05A_G3	AC: ±2%		, uno
.0	ger.	F_V1P05A_G3			ineo .
od un		PCIECLK_V1P05A_G3			deili
Stine	V1P15	CORE_V1P15_S0iX	1.15 V	8	Ulli
inde		DDI_V1P15_S0iX	DC: ±2%	2100 mA	
raeq t		UNCORE_V1P15_S0iX	AC: ±3%	2100 IIIA	
defill.	¢.	F_V1P15_S0iX	69	O.	
ed univ	red under		d undefine	•	indefined

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adefined undefined undefineu Table 123. SoC Power Rail DC Specs and Max Current

(Intel)	lefined undefine		Electrical Specifications	5
fine	red m.		4 unot	
inde,	defin			
Table 123. SoC Power	Rail DC Specs and Max Curre	ent	ade.	
Table 123. SoC Power	ail	Voltage Tolerances	Max Icc 67 mA	ined
V1P2A	USBSSIC_V1P2A_G3	1.24 V		
i efine	MIPI_V1P2A_G3	DC: ±2%	67 mA	n,
IIno	USBHSIC_V1P2A_G3	AC: ±2%	fines	
V1P8A	USB_V1P8A_G3		ude.	
defill	UNCORE_V1P8A_G3	1.8 V	ed	
d Unit	GPIOSE_V1P8A_G3	DC: ±2%	971 mA	
eo.	GPION_V1P8A_G3	AC: ±2%	More	
V1P8A V3P3A	F_V1P8A_G3	ined,		
V3P3A	USB_V3P3A_G3	3.3 V		
aed b	F_V3P3A_G3	DC: ±2%	196 mA	"uge,
define.	RTC_V3P3A_G5	AC: ±2%	S	J. Ur.
V3P3A_V1P8A	A SDIO_V3P3A_V1P8A_G3	1.8 V/3.3 V	stine	
V3P3A_V1P8A VSFR	LPC_V3P3A_V1P8A_S4	DC: ±2% AC: ±2%	196 mA	
VSFR	ICLK_VSFR_G3	1.05 V/1.24 V/	Activity.	
Ver a la company de la company	COREO_VSFR_G3	1.35 V	und	
	CORE1_VSFR_G3	DC: ±2%	-	
	UNCORE_VSFR_G3	AC: ±3%		ring
VCC0	CORE_VCC0_S0iX	Refer	2200 1	d undefing
defin	CORE_VCC0_SENSE	Table 124	3200 mA	
VCC1	CORE_VCC1_S0iX	Refer	and defill	
diller.	CORE_VCC1_SENSE	Table 124	3200 mA	
VNN	LINCORE VNN SA	Refer	2500 mA	
ed u.	UNCORE_VNN_SENSE	Table 124	2500 mA	
VGG	DDI_VGG_S0iX	Refer	Olli	
	DDI VGG SENSE	Table 124	8000 mA	
voci vnn vgg vgg vgg vgg vgg vgg vgg	UNCORE_VNN_SENSE DDI_VGG_S0iX DDI_VGG_SENSE	"uqei"		4efil
		ed u.		, uno
"Ide".		in		
ad uli	· unde		dein	
i efine			dune	
Inde	defill			
raed v	4 unc.		inger.	
Kill.			d u	
	aden.	infine		
-41	71.	Inde		defi
		sed w		4 nuc
"uge,	10	Silv.		
242	· uno		Datashee	t.
Stine	ined to		Datasiice	· -
Inde	defill.		Finer	
	" Une		nder.	
Him	ineo .		4 m.	



Table 123. SoC Power Rail DC Specs and Max Current

ndefill	Platform Rail		Voltage Tolerances	Max Icc
	VDDQ	DDI1_VDDQ_G3	1.24 V/1.35 V	
10	ine	DDI2_VDDQ_G3	DC: ±2%	
Inde		USB_VDDQ_G3	AC: ±2%	
ined to	VDDQG	DDR_VDDQG_S4		1900 -
defill		DDRCH0_VDDQG_S4	1.24 V/1.35 V	2500mA
d Unit		DDRCH1_VDDQG_S4	DC: ±2%	efile
efined undefine		DDRSFRCH0_VDDQG_S4	AC: ±2%	0.0
adeili	isting	DDRSFRCH1_VDDQG_S4	ined s	
71,	V3P3RTC	RTC_V3P3RTC_G5	G5: 2-3 V at battery	
und	Hines	adefined "	Otherwise V3P3A (pre diode drop)	-

NOTE:

- 1. RTC_VCC average current draw (G5) is specified at 27°C under battery conditions
- 2. This value is applicable only for Z8350 and Z8300 SKUs.

VCC and VNN Voltage Specifications

Table 124 and Table 138 list the DC specifications for the SoC power rails. They are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 124. VCC and VNN DC Voltage Specifications

	Symbol	Parameter	Min	Тур	Max	Unit	Note
4 U	CORE_VCC VID [Z8700, Z8750]	Core VID Target Range	0.6	.0.	1.30	V	
undefined ut	CORE_VCC VID [Z8500, Z8550]	Core VID Target Range	0.6	, nuo	1.28	V	
adelli	CORE_VCC VID [Z8300, Z8350]	Core VID Target Range	0.6	80	1.13	V	
y min	CORE_VCC0_S0iX	V _{CC0} for SoC Core 0	Re	efer VCC VID)	V	2
	CORE_VCC1_S0iX	V _{CC1} for SoC Core 1	Re	efer VCC VID)	V	2
	UNCORE_VNN VID [Z8700]	Uncore VID Target Range	0.4		1.28	V	eq,
	UNCORE_VNN VID [Z8500]	Uncore VID Target Range	0.4		1.28	V	
	UNCORE_VNN VID [Z8300, Z8350]	Uncore VID Target Range	0.4		1.1	V	
20	UNCORE_VNN_S4	V _{NN} for SoC Uncore	Re	efer VNN VIC)	V	2
sined	DDI_VGG_S0iX [Z8700]	V _{GG} for SoC Display	0.4	uno	0.9	V	
dell	DDI_VGG_S0iX [Z8500]	V _{GG} for SoC Display	0.4	Ve _Q	0.9	V	
d uii	DDI_VGG_S0iX [Z8300, Z8350]	V _{GG} for SoC Display	0.4		1.1	V	
sined.	Datasheet	d undefined undefine	A Ult	b _n .	efined	unde	243
16/11/10				900			



Table 124. VCC and VNN DC Voltage Specifications

Symbol	Parameter	Min	Тур	Max	Unit	Note
CORE_VCC/UNCORE_VNN V _{BOOT}	Default target V_{CC}/V_{NN} voltage for initial power up.	ugen	1.0 or 1.1		V	3
VCC0/1 Tolerance	Tolerance of VCC0/1 voltage at VID target.	DC: ±2%	AC: ±3%		%	eq ₁
VNN Tolerance	Tolerance of VNN voltage at VID target.	DC: ±2%	AC: ±2%	ال ا	%	1
VGG Tolerance	Tolerance of VGG voltage at VID target.	DC: ±2%	AC: ±3%	Inec	%	1

NOTES:

- 1. Contact local Intel representative for load line and tolerance details.
- 2. Each SoC is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two SoCs at the same frequency may have different settings within the VID range. Note this differs from the VID employed by the SoC during a power management event.
- 3. Refer VR12/IMVP7 Pulse Width Modulation specification for additional details. Either value is

Table 125. CPU ESD level details

CPU Type	CDM	НВМ
T4/T3	±250v	±1000v

CDM HBM

1.15 ±250v ±1000v

Crystal Specifications

There are two crystal oscillators of timing reference for power covers clocking of the covers clocking of th There are two crystal oscillators. One for RTC which maintains time and provides initial timing reference for power sequencing. The other is for the Integrated Clock, which

Table 126. ILB RTC Crystal Specification

Symbol	Parameter	Min	Тур	Max	Units	Notes
F _{RTC}	Frequency	- 100	32.768	-	kHz	1
T _{PPM}	Crystal frequency tolerance (refer notes)	ugein	-	+/-20	ppm	1 in
P _{DRIVE}	Crystal drive load	-	0.1	0.5	uW	1
C _{LOAD}	Crystal load capacitance		12.5		pF	
C _{SHUNT}	Crystal shunt capacitance	-	1.3	09	pF	1
C ₁ /C ₂	Load Capacitance tolerance			+/-10	%	

NOTES:

1. These are the specifications needed to select a crystal oscillator for the RTC circuit.



2. Crystal tolerance impacts RTC time. A 10 ppm crystal is recommended for 1.7 s tolerance per day, RTC circuit itself contributes addition 10 ppm for a total of 20 ppm in this example.

Table 127. Integrated Clock Crystal Specification

	4//						
	Symbol	Parameter	Min	Тур	Max	Units	Notes
26	F _{ICLK}	Frequency	ine -	19.2	-	MHz	10
sed unc	T _{PPM}	Crystal frequency tolerance & stability	-	-	+/-30	ppm	1
defille	P _{DRIVE}	Crystal drive load	-	-	100	uW	1
undefil	R _{ESR}	ESR	-	-	80	Ohm	1
ineo.	C _{LOAD}	Crystal load capacitance		12	Inos	pF	
adefined L	C _{SHUNT}	Crystal shunt capacitance	-	0.75	-	pF	1
TIL.	C ₁ /C ₂	Load Capacitance tolerance		eill	+/-10	%	
4		T			1		

NOTE:

1. These are the specifications required to select a crystal oscillator for the Integrated Clock circuit. Crystal must be AT cut, fundamental, parallel resonance.

19.6 DC Specifications

Platform reference voltages are specified at DC only. V_{REF} measurements should be made with respect to the supply voltages specified in "Voltage and Current Specifications".

Note: V_{IH/OH} Max and V_{IL/OL} Min values are bounded by reference voltages.

The following DC Specifications are explained in this section:

- "Display DC Specification"
- "MIPI-Camera Serial Interface (CSI) DC Specification"
- "SDIO DC Specification"
- "SD Card DC Specification"
- "eMMC 4.51 DC Specification"
- "JTAG DC Specification"
- "LPDDR3 Memory Controller DC Specification"
- "USB 2.0 Host DC Specification"
- "USB 3.0 DC Specification"
- "SSIC DC Specification"
- "SPI and FST_SPI DC Specification"
- "Power Management/Thermal (PMC) and RTC DC Specification"
- "SVID DC Specification"
- "GPIO DC Specification"



- "SIO I2C DC Specification"
- "SIO UART DC Specification"
- "I2S (Audio) DC Specification"
- "PCI Express DC Specification"

Note: Care should be taken to read all notes associated with each parameter.

19.6.1 **Display DC Specification**

DC specifications for display interfaces:

- "Display Port DC Specification"
- "HDMI DC Specification"
- "Embedded Display Port DC Specification"
- "Display Port AUX Channel DC Specification"
- "Embedded Display Port AUX Channel DC Specification"
- "DDC Signal DC Specification"
- "MIPI DSI DC Specification"

Display Port DC Specification

Table 128. Display Port DC specification

19.6.1.1	Dienlay Bo	rt DC Specification				e,		
indeir		DC specification		indefil	ned uni			ned undefined ur
	Symbol	Parameter	Min	Тур	Max	Units	Notes	dunos
Jundefined undefined un	V _{TX-DIFFp-p-} Level0	Differential Peak-to-peak Output Voltage Level 0	0.34	0.4	0.46	V	defi	IIIec
indefine	V _{TX-DIFFp-p-} Level1	Differential Peak-to-peak Output Voltage Level 1	0.51	0.6	0.68	V	g m.	
is fined b	V _{TX-DIFFp-p-} Level2	Differential Peak-to-peak Output Voltage Level 2	0.69	0.8	0.92	V		
J unde	VT _{X-DIFFp-p-} Level3	Differential Peak-to-peak Output Voltage Level 3	0.85	1.2	1.38	V		ined undefined u
	::UEQ	No Pre-emphasis	0.0	0.0	0.0	dB		inde
	V _{TX-PREEMP-}	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB		ned o
A ^U	RATIO	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	76	
finect		9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	4 UNG	
ed unde.	V _{TX-DC-CM}	Tx DC Common Mode Voltage	0		2.0	Vin	S _O .	
efined undefined waterined water ined to the state of the	indefined i	Indefined undefined u	define	d unde	fined v			stined undefined
246	O.	sined u	inor				Datas	heet
defined unit		ined under			رن.	undefil		



Table 128. Display Port DC specification

	Symbol	Parameter	Min	Тур	Max	Units	Notes
	RL _{TX-DIFF}	Differential Return Loss at 0.675GHz at Tx Package pins	12	e,,		dB	4
ned unde	IX DIT	Differential Return Loss at 1.35 GHz at Tx Package pins	9			dB	ndefineo
defill	C _{TX}	TX Output Capacitance			1.5	pF	2
ed une	NOTES:	4 nuge.			ndefi		
	 Straight loss 	line between 0.675 GHz and	1.35 GHz		Oli.		
iuge,	2. Represents termination.	only the effective lump capaci	tance see	n at the So	C interfa	ce that s	hunts the T〉

NOTES:

- 1. Straight loss line between 0.675 GHz and 1.35 GHz.
- ndefined undefined und 2. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination.

19.6.1.2 **HDMI DC Specification**

Table 129. HDMI DC specification

Parameter	Min	Тур	Max	Units	Notes	
Single Ended Standby (off), output voltage	-10		10	mV	1 @ AVcc	
Single Ended output swing voltage	400	sine.	600	mV		
Single Ended high level, output voltage	-10	uger	10	mv	1 @ AVcc	undefin
Single Ended high level, output voltage	-200		10	mV	1 @ AVcc	ed u.
Single Ended low level, output voltage	-600		-400	mV	1 @ AVcc	
Single Ended low level, output voltage	-700		-400	mV	1 @ AVcc	
	Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level,	Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level, -600 output voltage Single Ended low level, -700	Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level, output voltage Single Ended low level, -700	Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level, output voltage Single Ended low level, -700 -400	Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level, output voltage Single Ended low level, -700 Single Ended Standby (off), output voltage Single Ended output swing voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended high level, output voltage Single Ended low level, output voltage Single Ended low level, output voltage Single Ended low level, output voltage Single Ended low level, -700 -400 mV 1 @ AVcc	

Jundefined undefined und **Embedded Display Port DC Specification**

Table 130. Embedded Display Port DC Specification

-/	output voltage			0			
mbedded	Display Port DC Specifications	fication		g Voltage	level) =	3.3V ±5%	ed undefiner
Symbol	Parameter	Min	Тур	Max	Units	Notes	
V _{TX-DIFFp-p-} Level0	Differential Peak-to-peak Output Voltage Level 0	0.18	0.2	0.22	Vefine	1,2	
V _{TX-DIFFp-p-} Level1	Differential Peak-to-peak Output Voltage Level 1	0.2	0.25	0.275	V	1,2	1
V _{TX-DIFFp-p-} Level2	Differential Peak-to-peak Output Voltage Level 2	0.27	0.3	0.33	V	1,2	define
efined	ned undefined un	defined		.e	idefine	d undef	247
	ined to			ad ur			



Table 130. Embedded Display Port DC Specification

					4/1/		
defill	Symbol	Parameter	Min	Тур	Max	Units	Notes
	VT _{X-DIFFp-p-} Level3	Differential Peak-to-peak Output Voltage Level 3	0.315	0.35	0.385	V	1,2
, _{in} d	VT _{X-DIFFp-p-} Level4	Differential Peak-to-peak Output Voltage Level 4	0.36	0.4	0.44	V	1,2
is fined by	VT _{X-DIFFp-p-} Level5	Differential Peak-to-peak Output Voltage Level 5	0.405	0.45	0.495	V	1,2
indefined undefined unde	VT _{X-DIFFp-p-} MAX	Maximum Allowed Differential Peak-to-peak Output Voltage			1.380		3
Inge.	V _{TX-DC-CM}	Tx DC Common Mode Voltage	0	defin	2.0	V	1,2,3
	rueq.	No Pre-emphasis	0.0	0.0	0.0	dB	1,2,3
2	V _{TX-PREEMP-}	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB	1,2,3
un	RATIO	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	1,2,3
eineo.		9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	1,2,3
undefined undefined uni	RL _{TX-DIFF}	Differential Return Loss at 0.675GHz at Tx Package pins	12		.nd	dB	4
undefine	17-0111	Differential Return Loss at 1.35 GHz at Tx Package pins	9	defil	led pr	dB	4
	C_TX	TX Output Capacitance	٨	Ulus	1.5	pF	5

NOTES:

- 1. Steps between VTX-DIFFP-P voltages must be monotonic. The actual VTX-DIFFP-P-1 voltage must be equal to or greater than the actual VTX-DIFFP-P-0 voltage; the actual VTX-DIFFP-P-2 voltage must be greater than the actual VTX-DIFFP-P-1 voltage; etc.
- 2. The recommended minimum VTX-DIFFP-P delta between adjacent voltages is mV.
- 3. Allows eDP Source devices to support differential signal voltages compatible with eDP v1.3 (and lower) devices and designs.
- 4. Straight loss line between 0.675 GHz and 1.35 GHz.
- 5. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX



Display Port AUX Channel DC Specification 19.6.1.4

Table 131. DDI AUX Channel DC Specification

	4 / // /						
	Symbol	Parameter	Min	Тур	Max	Units	Notes
d unde	V _{AUX-DIFFp-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	V	4efineo
ndefined undefined unde	V _{AUXTERM_R}	AUX CH termination DC resistance		100		Ω	(0
eined une	V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0		2.0	V	2
Indei.	V _{AUX-TURN-CM}	AUX turn around common mode voltage		efineo	0.3	V	3
	I _{AUX_SHORT}	AUX Short Circuit Current Limit	ed un	5	90	mA	4
ind	C _{AUX}	AC Coupling Capacitor	75		200	nF	5

NOTES:

- 1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} V_{AUXM}|$
- Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
 Steady state common mode voltage shift between transmit and receive modes of operation.
- 4. Total drive current of the transmitter when it is shorted to its ground.
- 5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.

Embedded Display Port AUX Channel DC Specification 19.6.1.5

Table 132. Embedded Display Port AUX Channel DC Specification

Symbol	Parameter	Min	Тур	Max	Units	Notes	
V _{AUX-DIFFp-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	V	1	
V _{AUXTERM_R}	AUX CH termination DC resistance		100	,0	Ω		fined u
V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0		1.2	V	2	d under
V _{AUX-TURN-CM}	AUX turn around common mode voltage	8///		0.3	V	3	
I _{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	4	
C_{AUX}	AC Coupling Capacitor	75		200	nF	5	
1. V _{AUX-DIFFp-p} = 2. Common mo	= 2* V _{AUXP} – V _{AUXM} de voltage is equal to V _{bias_Tx} common mode voltage shift h	(or V _{bias_I}	_{Rx}) voltage	e. d receive	modes o	of operation.	adefined
	VAUX-DIFFP-P VAUX-TERM_R VAUX-DC-CM VAUX-TURN-CM IAUX_SHORT CAUX NOTES: 1. VAUX-DIFFP-P= 2. Common mo	V _{AUX-DIFFp-p} AUX Peak-to-peak Voltage at a transmitting Device V _{AUX-TERM_R} AUX CH termination DC resistance V _{AUX-DC-CM} AUX DC Common Mode Voltage V _{AUX-TURN-CM} AUX turn around common mode voltage I _{AUX_SHORT} AUX Short Circuit Current Limit C _{AUX} AC Coupling Capacitor NOTES: 1. V _{AUX-DIFFp-p} = 2* V _{AUXP} - V _{AUXM} 2. Common mode voltage is equal to V _{bias Tx}	V _{AUX-DIFFP-P} AUX Peak-to-peak Voltage at a transmitting Device V _{AUX-TERM_R} AUX CH termination DC resistance V _{AUX-DC-CM} AUX DC Common Mode Voltage V _{AUX-TURN-CM} AUX turn around common mode voltage I _{AUX_SHORT} AUX Short Circuit Current Limit C _{AUX} AC Coupling Capacitor 75 NOTES: 1. V _{AUX-DIFFP-P} = 2* V _{AUXP} - V _{AUXM} 2. Common mode voltage is equal to V _{bias_Tx} (or V _{bias_Tx}	V _{AUX-DIFFP-P} AUX Peak-to-peak Voltage at a transmitting Device V _{AUX-TERM_R} AUX CH termination DC resistance V _{AUX-DC-CM} AUX DC Common Mode Voltage V _{AUX-TURN-CM} AUX turn around common mode voltage I _{AUX_SHORT} AUX Short Circuit Current Limit C _{AUX} AC Coupling Capacitor 75 NOTES: 1. V _{AUX-DIFFP-P} = 2* V _{AUXP} - V _{AUXM} 2. Common mode voltage is equal to V _{bias_Tx} (or V _{bias_Rx}) voltage	$V_{AUX-DIFFp-p} \text{AUX Peak-to-peak Voltage} \\ \text{at a transmitting Device} \qquad 0.29 \\ \text{at a transmitting Device} \qquad 1.38 \\ \\ V_{AUX-TERM_R} \text{AUX CH termination DC} \\ \text{resistance} \qquad 0 \\ \\ V_{AUX-DC-CM} \text{AUX DC Common Mode} \\ \text{Voltage} \qquad 0 \\ \\ V_{AUX-TURN-CM} \text{AUX turn around common} \\ \text{mode voltage} \qquad 0.3 \\ \\ \\ I_{AUX_SHORT} \text{AUX Short Circuit Current} \\ \text{Limit} \qquad 90 \\ \\ \\ C_{AUX} \text{AC Coupling Capacitor} \qquad 75 \qquad 200 \\ \\ \textbf{NOTES:} \\ 1. V_{AUX-DIFFp-p} = 2* V_{AUXP} - V_{AUXM} \\ 2. \text{Common mode voltage is equal to } V_{bias} \text{ Tx} \text{ (or } V_{bias} \text{ Rx)} \text{ voltage.} \\ \\ \end{cases}$	$V_{AUX-DIFFP-P}$ AUX Peak-to-peak Voltage at a transmitting Device 0.29 1.38 V $V_{AUX-TERM_R}$ AUX CH termination DC resistance 100 Ω $V_{AUX-DC-CM}$ AUX DC Common Mode Voltage 0 1.2 V $V_{AUX-TURN-CM}$ AUX turn around common mode voltage 0.3 V I_{AUX_SHORT} AUX Short Circuit Current Limit 90 mA C_{AUX} AC Coupling Capacitor 75 200 nF NOTES: 1. $V_{AUX-DIFFP-P} = 2* V_{AUXP} - V_{AUXM} $ 2. Common mode voltage is equal to V_{bias} Tx (or V_{bias} Rx) voltage.	VAUX-DIFFP-P at a transmitting Device 0.29 1.38 V 1 VAUXTERM_R at a transmitting Device 100 Ω Ω VAUXTERM_R resistance AUX CH termination DC resistance 100 Ω VAUX-DC-CM Voltage AUX DC Common Mode Voltage 0 1.2 V 2 VAUX-TURN-CM mode voltage AUX turn around common mode voltage 0.3 V 3 IAUX_SHORT Limit AUX Short Circuit Current Limit 90 mA 4 CAUX AC Coupling Capacitor 75 200 nF 5

NOTES:

- 1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} V_{AUXM}|$
- Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
 Steady state common mode voltage shift between transmit and receive modes of operation.

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- 4. Total drive current of the transmitter when it is shorted to its ground.
- All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors
 must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver
 side is optional.

19.6.1.6 DDC Signal DC Specification

Table 133. DDC Signal DC Specification (DCC_DATA, DDC_CLK)

Symbol	Parameter	Min	Тур	Max	Units	Notes
V_{REF}	I/O Voltage	GP	V			
V_{IH}	Input High Voltage	0.75*V _{REF}		900	V	1
V _{IL}	Input Low Voltage		ilos	0.35*V _{REF}	V	2
V _{OL}	Output Low Voltage		1100	0.45	V	3
$\mathbf{I_i}$	Input Pin Leakage	-10	20	10	μΑ	4

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 2. $V_{\rm IL}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. This buffer reaches VOH/VOL with 3mA load.
- 4. For VIN between 0V and CORE_VCC_S0iX. Measured when driver is tri-stated.

Table 134. DDC Misc Signal DC Specification (HPD, BKLTCTL, VDDEN, BKLTEN)

Symbol	Parameter	Min	Тур	Max	Units	Notes
V _{REF}	I/O Voltage	GP	V	gell		
V _{IH}	Input High Voltage	0.75*V _{REF}			V	UN 1
V _{IL}	Input Low Voltage			0.35*V _{REF}	V	2
Z _{pu}	Pull up Impedance	40	50	60	Ω	3
Z _{pd}	Pull down Impedance	40	50	60	Ω	3
Ii	Input Pin Leakage	-10	2	10	μΑ	4

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. $V_{\rm IL}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at CORE_VCC0_S0iX and CORE_VCC1_S0iX.
- For VIN between 0V and CORE_VCC0_S0iX and CORE_VCC1_S0iX. Measured when driver is tri-stated.
- 5. This buffer reaches VOH/VOL with 3mA load.



Figure 35. Definition of Differential Voltage and Differential Voltage Peak-to-Peak

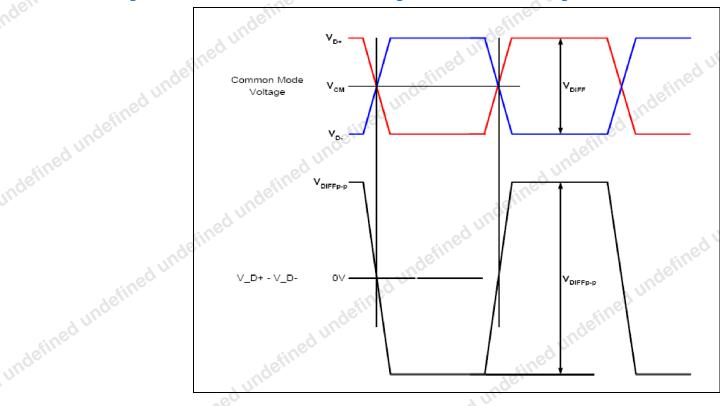
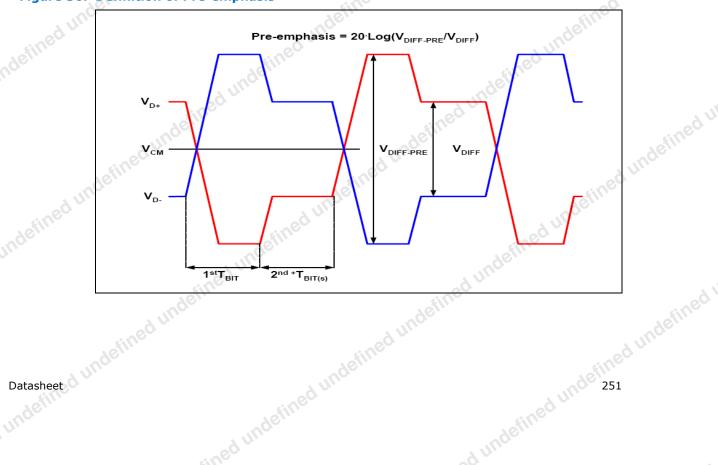


Figure 36. Definition of Pre-emphasis



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defined undefined undefined **MIPI DSI DC Specification**

Table 135. MIPI DSI DC Specification

	Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
A Pit	EAK	Pin Leakage current	-10	_	10	μA	· veg
y All	IIPI DSI HS	-TX Mode				296	
V	СМТХ	HS transmit static common-mode voltage	150	200	250	mV	
II. M V IV	V _{CMTX(1,0)}	V _{CMTX} mismatch when output is differential-1 or differential-0	-	- ed'	5	mV	
1/	V _{OD}	HS transmit differential voltage	140	200	270	mV	
unde I	∆V _{OD}	V _{OD} mismatch when output is Differential-1 or Differential-0	efined th	-	14	mV	ofined !
V Z	OHHS	HS output high voltage	-	-	360	mV	0,
Z	os	Single-ended output impedance	40	50	62.5	Ω	
Δ	Z _{OS}	Single-ended output impedance mismatch	_	8	10	%	
M	IIPI DSI LP	-TX Mode		iefine			
V	ОН	Thevenin output high level	1.1	1.2	1.3	V	
V	OL	Thevenin output low level	-50	-	50	mV	- 8
Z	OLP	Output impedance of LP transmitter	50	_	_	Ω	1 in
M	IIPI DSI LP	-RX Mode				-9 ni.	
V	IH	Logic 1 input voltage	880	_	- 6	mV	
Z	IL	Logic 0 input voltage, not in ULP state	_	-	550	mV	
V	HYST	Input hysteresis	25	- Sine	-	mV	
V	IHCD	Logic 1 Contention threshold	450	NU OF	_	mV	
V	ILCD	Logic 0 Contention threshold	define	_	200	mV	Stine

NOTE: Deviates from MIPI D-PHY specification Rev 1.0, which has minimum ZOLP of 110 Ω .



19.6.2 MIPI-Camera Serial Interface (CSI) DC Specification

Table 136. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters

	Parameters	nu .					
46	Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
4 unos	I _{LEAK}	Pin Leakage current	-10	-	10	μΑ	100
fined	MIPI-CSI H	S-RX Mode			د	nuo	
indefined undefined undef	V _{CMRX(DC)}	Common-mode voltage HS receive mode	70	-	330	mV	1
Stines	$V_{\rm IDTH}$	Differential input high threshold	-	Y ALL	70	mV	
inde	V _{IDTL}	Differential input low threshold	-70	_	-	mV	
	V _{IHHS}	Single-ended input high voltage	196,	-	460	mV	
	V _{ILHS}	Single-ended input low voltage	-40	-	-	mV	4.1
undefined undefined unde	V _{TERM-EN}	Single-ended threshold for HS termination enable	-	_	450	mV	inec
Hinec	Z _{ID}	Differential input impedance	80	100	125	Ω	
unde,	MIPI-CSI LI	P-RX Mode			Sine	, O	
ined to	V _{IH}	Logic 1 input voltage	880	0	967	mV	
defili	V _{IL}	Logic 0 input voltage, not in ULP state	-	eq-	550	mV	
nu	V _{IL-ULPS}	Logic 0 input voltage, ULP state	1135	_	300	mV	
•	V _{HYST}	Input hysteresis	25	-	-	mV	
	6777	AO-			11		

NOTE: 1. Setup/hold violation will be seen for a VCM higher than 250mv.

19.6.3 SDIO DC Specification

Table 137 provides the SDIO DC Specification, for all other DC Specifications not listed in this table, refer to Table 160.

Table 137. SDIO DC Specification

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
V _{OH}	Output High Voltage	1.4	uea	-	V	Measured at I _{OH} maximum.
$I_{OH/}I_{OL}$	Current at VoL/Voh	11-2	-	-	mA	indelli

19.6.4 SD Card DC Specification

Table 138 provides the SD Card DC Specification, for all other DC Specifications not listed in in this table, refer to Table 160.

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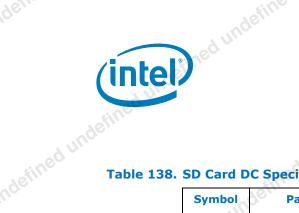


Table 138. SD Card DC Specification

,,,	ind	efine	define			defined u
intel	ned L		undefined undefine	Electrical Speci	ifications	
ed unde		OC Specification		, undefined unde		
	Symbol	Parameter	Min.	Max.	Unit	idefined l
	V _{REF}	I/O Voltage	SDIO_V3P3A	A_V1P8A_G3		defil.
. 8	V _{OH(3.3)}	Output High Voltage	0.75*V _{REF}	-	V	
sfined undefined und	V _{OL(3.3)}	Output Low Voltage	nuger.	0.125*V _{REF}	V	
4 under	V _{IH (3.3)}	Input High Voltage (3.3 V)	0.625*V _{REF}	V _{REF} +0.3	V	
Hineco	V _{IL (3.3)}	Input Low Voltage (3.3 V)	VSS-0.3	0.25*V _{REF}	V	ndefined
	V _{OH(1.8)}	Output High Voltage	1.40	_	V	
	V _{OL(1.8)}	Output Low Voltage	ined unit	0.45	V	iuge,
efined undefined uni	V _{IH (1.8)}	Input High Voltage (1.8 V)	1.27	2.00	V	
indefine	V _{IL (1.8)}	Input Low Voltage (1.8 V)	VSS-0.3	0.58	V	
ined u.	$I_{OH/}I_{OL}$	Current at VoL/Voh	-2	2	mA	
efill,	C _{LOAD}	total Load Capacitance	-	40	pF	
defined undefined un	defines	undefined undefine	ed undefined by	ined undefined ut	ndefined	undefine
defined undefined unadefined unadefined undefined undefi	ndefiner	Jundefined undefin	ned undefined unde	afined undefined l	Datasheet	dundefin
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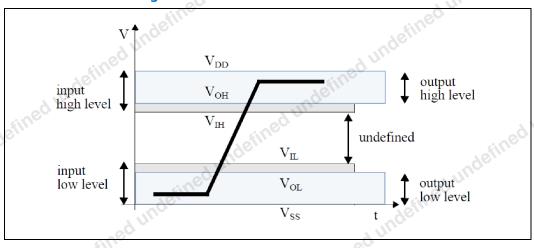
19.6.5 eMMC 4.51 DC Specification

Table 139. eMMC 4.51 DC Electrical Specifications

٥	Symbol	Parameter	Min	Max	Units
nde	V _{REF}	I/O Voltage	GPIOSE_V1P	8A_G3	USQ.
raed un.	V _{OH}	Output HIGH voltage	V _{REF} - 0.45	- del	V
Stines	V _{OI}	Output LOW voltage	-	0.45	V
inde	V _{IH}	Input HIGH voltage	0.65 * V _{REF}	V _{REF} + 0.3	V
edt	V _{IL}	Input LOW voltage	-0.3	0.35 * V _{REF}	V
indefined undefined	C _L	Bus Signal Line capacitance	*ined	30	pF
<u></u>	IIL	Input Leakage Current	-10	10	μΑ
	I _{OL}	Output Leakage Current	-10	10	μΑ

NOTE: This buffer reaches VOH/VOL with 3mA load.

Figure 37. eMMC 4.51 DC Bus Signal Level



19.6.6 JTAG DC Specification

Table 140. JTAG Signal Group DC Specification (JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TRST_N) (Sheet 1 of 2)

Symbol	Parameter	Min	Тур	Max	Units	Notes
V_{REF}	I/O Voltage	GP	ION_V1P8A_	_G3		
V _{IH}	Input High Voltage	0.75*V _{REF}		uno	V	1
V _{IL}	Input Low Voltage			0.35*V _{REF}	V	2
R _{wpu}	Weak Pull Up Impedance	2.5	5	7.5	kΩ	3



Table 140. JTAG Signal Group DC Specification (JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TRST_N) (Sheet 2 of 2)

hoe	Symbol	Parameter	Min	Тур	Max	Units	Notes
	R _{wpd}	Weak Pull Down Impedance	2.5	J175	7.5	kΩ	3
dunk	R _{wpu-20K}	Weak Pull Up Impedance 20K	12		28	kΩ	16 1460
defined	R _{wpd-40K}	Weak Pull Down Impedance 40K	20		70	kΩ	4
ed une	NOTES:	i IInde.			defi		
defined un		lefined as the minimum voll high value.	tage level at a	receiving ag	gent that will	be interp	eted as a
NUT.		efined as the minimum volt low value.	age level at a	receiving ag	ent that will	be interpr	eted as a

- 1. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO V1P8A G3.
- 4. Rwpu_40k and Rwpd_40k are only used for JTAG_TRST#.
- 5. This buffer reaches VOH/VOL with 3mA load.

Table 141. JTAG Signal Group DC Specification (JTAG_TDO)

indell.	Symbol	Parameter	Min	Тур	Max	Units	Notes
ed u.	V _{REF}	I/O Voltage	GI	PION_V1P8A	_G3	8//	
ndefined undefil.	V _{IH}	Input High Voltage	0.75*V _{RE}		eined mi	V	1
	V _{IL}	Input Low Voltage		260	0.45*V _{REF}	V	2
	Z _{pd}	Pull down Impedance	17.5	dun	35	Ω	3
	R _{wpu}	Weak Pull Up Impedance	12	Ver	28	kΩ	3
ined ur	R _{wpd}	Weak Pull Down Impedance	20		70	kΩ	3
inde ^{it}	NOTES:						
adefined under		lefined as the minimum vol high value.	tage level at	a receiving	agent that wi	ll be inter	preted as a
defili		efined as the minimum volt low value.	tage level at	a receiving	agent that wil	I be interp	oreted as a
UII.		ed at GPIO_V1P8A_G3.			Cilli		
	4. This bu	ffer reaches VOH/VOL with	3mA load.	100			

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. $V_{
 m IL}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO_V1P8A_G3.
- 4. This buffer reaches VOH/VOL with 3mA load.

Table 142. JTAG Signal Group DC Specification (JTAG_PRDY#, JTAG_PREQ#)

60	Symbol	Parameter	Min	Тур	Max	Units	Notes
ndefined undefined	V _{REF}	I/O Voltage	GPI	ON_V1P8A_	G3		7011
, unou	V _{IH}	Input High Voltage	0.75*V _{REF}			V	1
	V _{IL}	Input Low Voltage			0.45*V _{REF}	O V	2
defin	Z _{pd}	Pull down Impedance	17.5		35	Ω	3
	R _{wpu}	Weak Pull Up Impedance	2.5	5	7.5	kΩ	3
	d undefi		29	efined			2.4
256			ed ulli				Datash
sined undefine		in.	defined und			ndefin	
1efines		sined b			ad V	iue.	

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- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. Measured at GPIO V1P8A G3.
- 4. This buffer reaches VOH/VOL with 3mA load.

19.6.7 **DDR3L-RS Memory Controller DC Specification**

Table 143. DDR3L-RS Signal Group DC Specifications

Lefined W. Table 14.	Symbol	Parameter	Min	Туре	Max	Units	Notes	
	V _{IL}	Input Low Voltage		ndefine	DDR_VREF - 200mV	V	1	is fined to
	V _{IH}	Input High Voltage	DDR_VREF + 200mV	tined ut		V	2, 3	More
ofined un	V _{OL}	Output Low Voltage	wed "	(DDR_VDDQG_S4 / 2)* (RON / (RON+RVTT_TERM))		d ur	3,4	
ndefined undefined un	V _{OH}	Output High Voltage	defin	DDR_VDDQG_S4 - ((DDR_VDDQG_S4 / 2)* (RON/ (RON+RVTT_TERM))	ed undefi	V	3,4	ed l'
	IIL	Input Leakage Current		ed under	5	μA	For all DDR Signals	undefine
ined u	R _{ON}	DDR3L-RS Clock Buffer strength	26	undefilt	40	Ω	nde fine o	
ndefined undefined	C _{IO}	DQ/DQS/DQS# DDR3L-RS IO Pin Capacitance	ndefine	3.0	adef	pF		
undefine	logic	s defined as the mall low value. DDR	_VREF is norn	age level at the receiving nally DDR_VDDQG_S4				defined

NOTES:

- 1. V_{IL} is defined as the maximum voltage level at the receiving agent that will be received as a logical low value. DDR VREF is normally DDR VDDQG S4
- VIH is defined as the minimum voltage level at the receiving agent that will be received as a logical high value. DDR_VREF is normally DDR_VDDQG_S4
- 3. V_{IH} and V_{OH} may experience excursions above DDR_VDDQG_S4. However, input signal drivers must comply with the signal quality specifications.
- RON is DDR driver resistance whereas RTT TERM is DDR ODT resistance which is controlled by DDR.
- 5. DDR3L-1333 CLK buffer Ron is 260hm and SR target is 4V/ns; DQ-DQS buffer Ron is 300hms arget undefined and SR target is 4V/ns; CMD/CTL buffer Ron is 200hms and SR target is 1.8V/ns.

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LPDDR3 Memory Controller DC Specification 19.6.8

Table 144. LPDDR3 Signal Group DC Specifications

				~U'			
	Symbol	Parameter	Min	Тур	Max	Units	Notes
	DDR_VDDQG_S4	I/O Supply Voltage	1.14	1.24	1.26	V	" Deg
defined undefined un	V _{IL}	Input Low Voltage	ande		DDR_VRE F - 200 mV	d unde	
raed und	V _{IH}	Input High Voltage	DDR_VREF + 200 mV		ndefine	V	
defill	V _{OL}	Output Low Voltage	-	0.260	O	V	1,2
	V _{OH}	Output High Voltage	-	0.960	-	V	1,2
	III	Input Leakage Current	- 0	Jn0-5	-	μΑ	3,4
	R _{ON}	Clock Buffer strength	26		40	Ω	· Dec
9/1	C _{IO}	IO Pin Capacitance	11000	3.0		pF	S.III
adefines	NOTES:	is determined with 100	Ohan haiffe a stage		COOk	ed um	/1 T al.al.
undefined undefine	test load. 2. LPDDR3-10 40Ohms an 3. Applies to t	H is determined with 400 H66 CLK buffer Ron is 35 Hd SR target is 2V/ns; Cl He pin to VCC or VSS lea He pin to pin leakage cu	Ohm and SR tar MD/CTL buffer R akage current.	get is 2.5V/ns	s; DQ-DQS b	uffer Ro	n is
		_		11/10			

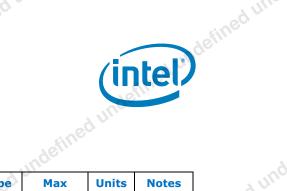
NOTES:

- 1. V_{OL} and V_{OH} is determined with 400hm buffer strength setting into a 600hm to 0.5x V1p5_ddr test load.
- 2. LPDDR3-1066 CLK buffer Ron is 350hm and SR target is 2.5V/ns; DQ-DQS buffer Ron is 400hms and SR target is 2V/ns; CMD/CTL buffer Ron is 300hms and SR target is 1.5V/ns.
- 3. Applies to the pin to VCC or VSS leakage current.
- 4. Applies to the pin to pin leakage current.

19.6.9 **USB 2.0 Host DC Specification**

Table 145. USB 2.0 Host DC Specification (Sheet 1 of 3)

4 nhos	Symbol	Parameter	Min	Туре	Max	Units	Notes	
undefined unde	Supply Vo	oltage	•	•	4 nuo		•	
"uge.	VBUS	High-power Port	4.75	4	5.25	V	2	ed u
90.	VBUS	Low-power Port	4.20	"Uges	5.25	V		undefined u
	Supply Cu	irrent	-6	70.	•		•	4 unos
	ICCPRT	High-power Hub Port (out)	500			mA	1775	SC
de	ICCUPT	Low-power Hub Port (out)	100			mA	der	
4e fine	ICCHPF	High-power Function (in)			500	mA	O.,	
, unos	ICCLPF	Low-power Function (in)			100	mA		
d undefined undefineo	ICCINIT	Unconfigured Function/Hub (in)			100	mA		
unas	ICCSH	Suspended High-power Device			2.5	mA	15	ed
go -	ICCSL	Suspended Low-power Device		inge	500	μΑ		defill
	indefil	16-	define	jd			2/2	red unc
258			I UNO				Datashee	t
258 undefine		od undefined				Jefiner		
16fine		sined "			od um			



defined undefined undefineu ndefined undefined Table 145. USB 2.0 Host DC Specification (Sheet 2 of 3)

Symbol	Parameter	Min	Туре	Max	Units	Note
Input Le	vels for Low-/full-speed		Clino			
VIH	High (driven)	2.0			V	4
VIHZ	High (floating)	2.7		3.6	V	4
VIL	Low			0.8	V	4
VDI	Differential Input Sensitivity	0.2	_	undefin	ed uno	(D+)- (D-) ;Figu ; Note
VCM	Differential Common Mode Range	0.8	define	2.5	V	Include VDI range; Figure; Note 4
Input Lev	vels for High-speed				חנט ,	
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100		150	mV	
Input Lev VHSSQ VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525	ndefine	625	mV	
defines	High-speed differential input signaling levels	fined c				16
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50		500	mV	defin
Output L	evels for Low-/full-speed	1	1	30.	luer	
VOL	Low	0.0		0.8	V	4,5
VOH	High (Driven)	2.8		3.6	V	4,6
VOSE1	SE1	0.8	delitt	-	V	
VCRS	Output Signal Crossover Voltage	1.3	30.	2.0	V	10
Output L	evels for High-speed:	deilli			1	defin
VHSOI	High-speed idle level	-10		10	mV	UOF
VHSOH	High-speed data signaling high	360		440	mV	
VHSOL	High-speed data signaling low	-10		10	mV	
	Chirp J level (differential	700	Ni sa	1100	mV	
VCHIRPJ	voltage)	undefined	unde	1100		undefi



Jefined undefined undefined **USB 2.0 Host DC Specification (Sheet 3 of 3) Table 145.**

(Inte	17	4	sined undefine Elec			ectrical Specifications			
eined On		ad uno				. "Ind	Jel.		
Jer.		defines			27.2	led n			
Table 145.	USB 2.0	Host DC Specification (Sh	heet 3 of 3))	"hyge"		T	1	
	Symbol	Parameter	Min	Туре	Max	Units	Notes		
	VCHIRPK	Chirp K level (differential voltage)	-900	961	-500	mV		indefil	
	Decouplin	g Capacitance:	is fines				red	0.	
Jefined ur	СНРВ	Downstream Facing Port Bypass Capacitance (per hub)	120			μF	defill		
3/,	CRPB	Upstream Facing Port Bypass Capacitance	1.0		10.0	μF	9		
	Input Cap	pacitance for Low-/full-speed:			4 Uno	_			
	CIND	Downstream Facing Port		Sing	150	pF	2	46	
	CINUB	Upstream Facing Port (w/o cable)	-0.0	vge.	100	pF	3	undef	
ال الم	CEDGE	Transceiver edge rate control capacitance	define		75	pF	4efiner		
ineu	Input Imp	pedance for High-speed:	•			الالم	'UC		
		TDR spec for high-speed termination			de	ined			
	Terminati	ons:		· · · · · · · · · · · · · · · · · · ·	ad Ulive	<u> </u>	•		
efined	RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425	indefin	1.575	kΩ	1.5 kΩ ±5%	76	
	RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25	-	15.75	kΩ	1.5 kΩ ±5%	dunos	
fined	ZINP	Input impedance exclusive of pull-up/pull-down (for low-/full speed)	300			kΩ	Indetil	-	
	VTERM	Termination voltage for upstream facing port pull-up (RPU)	3.0	.61	3.6	V		ed und	
Ē	Terminati	ons in High-speed:		"Iuge,					
-	VHSTERM	Termination voltage in high speed	-10		10	mV	-:-	ed uno	
60	RTERM	High Speed Termination	40	45	50	Ω	gen		
define	VBUSD	VBUS Voltage drop for detachable cables	-	-	1	mV	n.		
undefined	 Measu Measu Measu 	detachable cables ured at A plug. ured at A receptacle. ured at B receptacle. ured at A or B connector. ured with RL of 1.425 kΩ to 3.6 V.		d undef	ined uni	Je.,	_	ned uni	
	indeili		<i>Aefine</i>					ued n	
io stined	70.	. ned	Juna					et .	
260 undefined		.ndefine				idefined			
		ed ui			4 UL	10			

- 1. Measured at A plug.
- 2. Measured at A receptacle.
- 3. Measured at B receptacle.
- 4. Measured at A or B connector.
- 5. Measured with RL of 1.425 $k\Omega$ to 3.6 V.



- 6. Measured with RL of 14.25 $k\Omega$ to GND.
- 7. Timing difference between the differential data signals.
- 8. Measured at crossover point of differential data signals.
- 9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330 mV.
- 10. Excluding the first transition from the Idle state.
- 11. The two transitions should be a (nominal) bit time apart.
- 12. For both transitions of differential signaling.
- 13. Must accept as valid EOP.
- 14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors .
- 15. For high power devices (non-hubs) when enabled for remote wakeup.
- 16. Specified by eye pattern templates.

USB HSIC DC Specification 19.6.10

Table 146. USB HSIC DC Electrical Specifications

Symbol	Parameter	Min	Max	Units
V_{REF}	I/O Voltage	USBHSIC_V1	P2A_G3	
V _{OH}	Output HIGH voltage	0.75 * V _{REF}	4efill-	V
V _{OI}	Output LOW voltage	- 3	0.25 * V _{REF}	V
V _{IH}	Input HIGH voltage	0.65 * V _{REF}	V _{REF} + 0.3	V
V _{IL}	Input LOW voltage	-0.3	0.35 * V _{REF}	V
O _D	I/O Pad Drive Strength	40	60	Ω
CL	Load capacitance	sine 1	5	pF
Z _I	I/O input impedance	240	- 40	kΩ
T _I	Characteristic Trace Impedance	45	55 und	Ω

Jundefined undefined und **USB 3.0 DC Specification**

Table 147. USB 3.0 DC transmitter specifications

	Symbol	Parameter	Min	Max	Units	Notes	"Inge.
~	UI	Unit Interval	199.94	200.06	ps	4	
undefined undefined un	V _{TX-DIFF-PP}	Differential peak-peak Tx voltage swing	0.8	1.2	V	ige,	
4 unden	V _{TX-DIFF-PP-LOW}	Low-Power Differential peak- peak Tx voltage swing	0.4	1.2	luev.	1	
eineo.	R _{TX-DIFF-DC}	DC differential impedance	72	92	Ω		
ed under	V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection	.ndefil	0.6	V	2	defined !
David vi d uli	ndefinec	indefine	,d U			define	d und
Datasheet						261	
ined undefil.		d undefined under		ind	efineo		
16/11		einet.		9,0,			



intel	ohed undering	indefined	Electrical Specifica				
defined undefine		undefined un					
	Symbol	Parameter	Min	Max	Units	Notes	
	C _{AC-COUPLING}	AC Coupling Capacitor	75	200	nF	3	
	T _{CDR-SLEW-MAX}	Maximum slew rate	agen	10	ms/s		
	C _{TX-PARASITIC}	Tx input capacitance for return loss	7),, -	1.25	pf	5	
lefined undefined und		Eye Height	100	1200	mV	7,9	
	Dj	Deterministic Jitter	=	0.43	UI	7,8,9	
defill	Rj	Random Jitter	-	0.23	UI	6,7,8,10	
	Tj	Total Jitter		0.66	UI	7,8,9	

- 1. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
- 2. Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below output.
- 3. All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
- 4. The specified UI is equivalent to a tolerance of +-300 ppm for each device. period does not account for SSC induced variations.
- 5. parasitic capacitance to ground.
- 6. Measured over 10⁶ consecutive UI and extrapolated to 10⁻¹² BER.
- 7. Measured after receiver equalization function.
- 8. Measured at the end of reference channel and cables at TP1.
- 9. The eye height is measured at the maximum opening.
- 10. The Rj spec is calculated at 14.069 times the RMS random jitter for 10^{-12} BER.

Table 148. USB 3.0 DC LFPS specifications

od u'	Symbol	Parameter	Min	Max	Units	Notes
afinee	T _{PERIOD}	· veg	20	100	ns	0
inge	V _{CM-AC-LFPS}	delli	-	10	mV	
defined undefined u	V _{CM-AC-LFPS-} ACTIVE	zed une	-	10,00	mV	
	V _{TX-DIFF-PP-LFPS}	peak-peak Differential amplitude	0.8	1.2	V	
	V _{TX-DIFF-PP-LFPS-LP}	Low power peak-peak Differential amplitude	0.4	0.6	V	
	T _{RISEFALL2080}	defin	-	4	ns	Silve
	Duty cycle	4 Une	40	60	%	uge.
indefille	C _{TX-PARASITIC}	Tx input capacitance for return loss	-	1.25	pf	0.
ndefined undefined a sefined undefined	adefined und	loss sined undefined undefin	ed undefi	ined und		
262 undefined	une	d undefined under		771.	defined	Datasheet
16111		cine		99 2		



Table 149. USB 3.0 DC Receiver specifications

NOO	Symbol	Parameter	Min	Max	Units	Notes
	UI	Unit Interval	199.94	200.06	ps	1
	R _{RX-DC}	Receiver DC common mode impedance	18	30	Ω	2 11
od III.	R _{RX-DIFF-DC}	DC differential impedance	72	120	Ω	3
adefines	Z _{RX-HIGH-IMP-} DCPOS	DC input CM input for V>0 during reset or power down	25	-	kΩ	4
Indefined undefined undef	V _{RX-LFPS-DETDIFFp-}	LFPS detect threshold	100	300	mV	
adelli	f1	tolerance corner	- 200	4.9	MHz	
71.	J_{RJ}	Random Jitter	46 ₇ //	0.0121	UI rms	1
	J _{RJP-P}	Random Jitter peak-peak at 10 ⁻¹	,	0.17	UI p-p	1,4
inde	Sj @0.5MHz	Sinusoidal Jitter	-	2	UI p-p	1,2,3
	Sj @1MHz	Sinusoidal Jitter	-	1	UI p-p	1,2,3
defill defilled	Sj @2MHz	Sinusoidal Jitter	-	0.5	UI p-p	1,2,3
Linds	Sj @f1MHz	Sinusoidal Jitter	-	0.2	UI p-p	1,2,3
	Sj @50MHz	Sinusoidal Jitter	-	0.2	UI p-p	1,2,3
undefined undefined unde	V_full_swing	transition bit differential voltage swing	- fine	0.75	V p-p	1
	V_EQ_level	Non transition bit voltage (equalization)	nuo-	-3	db	1

- 1. All parameters are measured at TP1.
- 2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. however, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
- 3. During the Rx tolerance test, SSC is generated by test equipment and present all the time.

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defined undefined undefineu **SSIC DC Specification** 19.6.12

Table 150. SSIC DC Specification

(intel	7	def	adefinee			Electrical Specifications			
undefine		adefined une			efined	nuge.			
19.6.12	SSIC DC Spe	ecification		ed u	uge.		, un		
Table 150.	SSIC DC Specific	cation		Jefine			fined		
	Symbol	Parameter	Min.	Nom.	Max.	Unit	, unde.		
ned und	R _{REF_RT}	Reference load for when the Transmitter is terminated.	iin	100		D			
Indefined undefined und	R _{REF_NT}	Reference load for when the Transmitter is not terminated.	10	21	Indefined	kΩ			
inder.	Z _R	Reference impedance.		100		Ω	raed ul		
	V _{DIFF_DC_LA_RT_TX}	Large Amplitude differential TX DC voltage when the Transmitter is terminated. Defined for $R_{REF_RT}^{-1}$ and test pattern ²	160	36	240	mV	ined undefile		
undefined undefined uni	V _{DIFF_DC_LA_NT_TX}	Large Amplitude differential TX DC voltage when the Transmitter is not terminated. Defined for R _{REF_NT} ³ and test pattern ²	320	ndefined	480	mV	fined undefined u		
ed undefined un	V _{DIFF_DC_SA_RT_TX}	Small Amplitude differential TX DC voltage when the Transmitter is terminated. Defined for $R_{REF_RT}^{-1}$ and test pattern ²	100		130	mV	Z [*]		
d undefined undefined u	V _{DIFF_DC_SA_NT_TX}	R _{REF_RT} ¹ and test pattern ² Small Amplitude differential TX DC voltage when the Transmitter is not terminated. Defined for R _{REF_NT} ³ and test pattern ²	200	Indefiner	260	mV	ofined undefined		
ad undefined undefined vindefined		ned undefined un			d undefil	led line			
ed unde	defined unde	Au.	oni:	undefine			ed undefined		
264	Tur	defined L	Inder.			Dat Ined III	asheet		
lefined L		ined uni			ad under	•			



Table 150. SSIC DC Specification

defin	Symbol	Parameter	Min.	Nom.	Max.	Unit
ned under	V _{CM_LA_TX}	Large Amplitude common-mode TX voltage. Defined R _{REF_RT} ¹ and test pattern ²	160		260	mV
indefined undefine	V _{CM_SA_TX}	Small Amplitude common-mode TX voltage. Defined R _{REF_RT} ¹ and test pattern ²	80	fined un	190	mV
	C _{PIN_RX}	PIN Capacitance	4 uno	0	1.5	pF

- 1. External reference load R_{REF_RT} and a reference impedance Z_{REF_RT} that conform to SRL_{REF_RT} (return loss of Z_{REF_RT}).
- 2. Defined when driving both a DIF-N and a DIF-P LINE state.
- 3. External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN_RX} .

19.6.13 LPC DC Specification

Table 151. LPC 1.8V Signal Group DC Specification

Symbol	Parameter	Min	Тур	Max	Units	Notes
V _{IH}	Input High Voltage	1.5	1.8	1.8 +0.5	V	3)
V _{IL}	Input Low Voltage	-0.5	0	0.8	O V	
V _{OH}	Output High Voltage	0.9 x 1.8		18/11/1	V	
V _{OL}	Output Low Voltage			0.1 x 1.8	V	
I _{OH}	Output High Current		0.5	"UEO	mA	
I _{OL}	Output Low Current		-1.5		mA	
I _{LEAK}	Input Leakage Current	-10	d un	10	μΑ	-6
C _{IN}	Input Capacitance	gelli		10	pF	Silve

Table 152. LPC 3.3V Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Min	Тур	Max	Units	Notes
V _{IH}	Input High Voltage	2.0	3.3	3.3 +0.5	V	1
V _{IL}	Input Low Voltage	-0.5	0	0.8	V	2
V _{OH}	Output High Voltage	2.5	11000		V	3

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defined in		fined unoc				ed under			
Table 152		Signal Group DC Spe	1	Sheet 2 of	7 111,	<u> </u>			
	Symbol	Parameter	Min	Тур	Max	Units	Notes		
	V _{OL}	Output Low Voltage		gelli	0.4	V	3		
	I _{OH}	Output High Current	2	0.5		mA	3		
	I _{OL}	Output Low Current	"ine"	-1.5		mA	3		
4 UIV	I _{LEAK}	Input Leakage Current	-10		10	μΑ	16/11/1		
	C_IN	Input Capacitance	O.		10	pF	0-		
ndefined under	logical 2. V _{IL} is d logical	lefined as the minimum vol high value, Applies to LPC_ efined as the minimum voll low value. Applies to LPC_A tested with Iout=500uA, V _C	AD[3:0], LPC_ age level at a lD[3:0], ILB_l	_CLKRUN_N receiving a _PC_CLKRUN	gent that will J_N.	·			

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a defined undefined undefined un logical high value, Applies to LPC_AD[3:0], LPC_CLKRUN_N.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. Applies to LPC_AD[3:0], ILB_LPC_CLKRUN_N.
- 3. V_{OH} is tested with Iout=500uA, V_{OL} is tested with Iout=1500uA.
- 4. Applies to LPC AD[3:0], LPC CLKRUN N and LPC FRAME N.
- 5. LPC_SERIRQ is always a 1.8V I/O irrespective of the value of LPC_V1P8V3P3_S4.

SPI and FST_SPI DC Specification

Table 153. SPI and FST_SPI Signal Group DC Specification

-O			•		70			
istinee	Symbol	Parameter	Min	Тур	Max	Units	Notes	<u></u>
inde	V _{REF}	I/O Voltage	GI	PIOSE_1P8A_0	G3	V	3	
	V _{IH}	Input High Voltage	0.65 * V _{REF}	"Vge.		V	2	ie film
	VIL	Input Low Voltage	-0.5	900	0.35 * V _{REF}	V	2	IIIO
	V _{OH}	Output High Voltage	V _{REF} - 0.45		1.8V	V	1	
A UIT	V _{OL}	Output Low Voltage	1000		0.45	V	1	
eineu	I _{OH}	Output High Current	9 0		2	mA	1	
age,	I _{OL}	Output Low Current	-2			mA	1	
ndefine	 Applies The I/C 	to SPI1_CS[1:0], SPI1_CL to SPI1_MISO and SPI1_M b buffer supply voltage is more to of all noise from DC up to	OSI. easured at the	SoC packag	•			

NOTES:

- 1. Applies to SPI1_CS[1:0], SPI1_CLK, SPI1_MOSI.
- 2. Applies to SPI1_MISO and SPI1_MOSI.
- The I/O buffer supply voltage is measured at the SoC package pins. The tolerances shown are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.
- 4. This buffer reaches VOH/VOL with 3mA load.



Power Management/Thermal (PMC) and RTC DC 19.6.15 **Specification**

Table 154. Power Management Signal Group DC Specification indefined undefined unde

Symbol	Parameter	Min	Тур	Max	Units	Notes	
V_{REF}	I/O Voltage	GI	GPIOSE_1P8A_G3				
V_{IH}	Input High Voltage	0.65 * V _{REF}			V	2	
V _{IL}	Input Low Voltage	-0.5		0.35 * V _{REF}	V	2,3	
V _{OH}	Output High Voltage	V _{REF} - 0.45		1.8V	V	1	
V _{OL}	Output Low Voltage			0.45	V	1	
I _{OH}	Output High Current		2013	2	mA	1	
I _{OL}	Output Low Current	-2	gen		mA	1	

NOTES:

- 1. The data in this table apply to signals PMC ACPRESENT, PMC BATLOW N, PMC PLTRST N, PMC_PWRBTN_N,PMC_SLP_S4_N, PMC_SUS_STAT_N, PMC_SUSCLK[3:0], PMC_SUSPWRDNACK
- 2. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 3. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 4. This buffer reaches VOH/VOL with 3mA load.

Table 155. PMC_RSTBTN# 1.8V Core Well Signal Group DC Specification

	Symbol	Parameter	Min	Тур	Max	Units	Notes
60.	VREF	I/O Voltage	UN	CORE_V1P8	_G3	V	ineo
ad uli.	V _{IH}	Input High Voltage	0.65* VREF			V) e 1
Stines	V _{IL}	Input Low Voltage			0.35* VREF	V	2
	NOTES:	indefin			46/1	lues	
defineo	411	lefined as the minimum volt high value.	age level at a	receiving a	gent that will	be interp	reted as a
unde		efined as the minimum volt low value.	age level at a	receiving a	gent that will l	oe interpr	eted as a
	_						

NOTES:

- 1. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{II} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 156. Power Management and RTC Well Signal Group DC Specification

Symbol	Parameter	Min	Тур	Max	Units	Notes
VREF	I/O Voltage	RTC_	V3P3R	ΓC_G5		oge,
V _{IH}	Input High Voltage	2.0	-	-	V	1
V_{IL}	Input Low Voltage	-	-	0.78	V	2

NOTES:

- 1. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. $V_{\rm IL}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

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Table 157. RTC Well DC Specification

Symbol	Parameter	Min	Тур	Max	Units	Notes
V _{IH}	Input High Voltage	2.3	U-C	-	V	1
V _{IL}	Input Low Voltage	- sine	-	0.78	V	2

NOTES:

- 1. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 158. PROCHOT# Signal Group DC Specification

31.	Symbol	Parameter	Min	Туре	Max	Units	Notes
	V _{REF}	I/O Voltage	GP:	ION_V1P8	A_G3		
	V _{IH}	Input High Voltage	0.75*V _{REF}		V_{REF}	V	1
dul	V_{IL}	Input Low Voltage	inos		0.45*V _{REF}	V	2
fines	V _{OL}	Output Low Voltage	30		0.35 * V _{REF}	V	
"ude"	I _{OL}	Output Low Current			-5	mA	
undefined undefine	logica 2. V _{IL} is	defined as the minimum volling to the defined as the minimum volling to the minimum volling	J		(ine	·	

NOTES:

- 1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
- 2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
- 3. This buffer reaches VOH/VOL with 3mA load.

19.6.16 SVID DC Specification

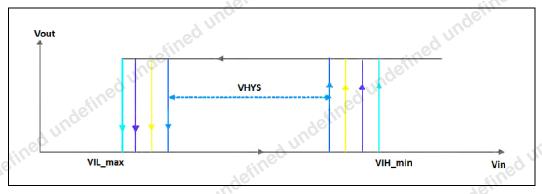
Table 159. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT_N)

V _{REF} V _{IH} V _{IL}	I/O Voltage Input High Voltage Input Low Voltage	GPIO 0.65*V _{REF}	N_V1P8	A_G3		
VIL		0.65*V _{REF}		1767	-	
- 41	Input Low Voltage			O	V	1
V	Input Low Voltage		900,	0.35*V _{REF}	V	1
V_{OH}	Output High Voltage	V _{REF} - 0.45	10	V _{REF}	V	1
V _{OL}	Output Low Voltage	INOS		0.45	V	4
V_{HYS}	Hysteresis Voltage	0.1			V	4 Um
R _{ON}	BUffer on Resistance	40		60	Ω	2
I_{L}	Leakage Current	-10		10	μA	3
C _{PAD}	Pad Capacitance			9	pF	4
V_{PIN}	Pin Capacitance			10	pF	
Z _{pd}	Pull down Impedance	35	50	70	Ω	
ndefin	od undefi	ned undef	inea.		indefin	Datash
	V _{OL} V _{HYS} R _{ON} I _L C _{PAD} V _{PIN}	V _{OL} Output Low Voltage V _{HYS} Hysteresis Voltage R _{ON} BUffer on Resistance I _L Leakage Current C _{PAD} Pad Capacitance V _{PIN} Pin Capacitance Z _{pd} Pull down Impedance	V _{OL} Output Low Voltage V _{HYS} Hysteresis Voltage 0.1 R _{ON} BUffer on Resistance 40 I _L Leakage Current -10 C _{PAD} Pad Capacitance V _{PIN} Pin Capacitance Z _{pd} Pull down Impedance 35	V _{OL} Output Low Voltage V _{HYS} Hysteresis Voltage 0.1 R _{ON} BUffer on Resistance 40 I _L Leakage Current -10 C _{PAD} Pad Capacitance V _{PIN} Pin Capacitance Z _{pd} Pull down Impedance 35 50	VOL Output Low Voltage 0.45 VHYS Hysteresis Voltage 0.1 RON BUffer on Resistance 40 60 IL Leakage Current -10 10 CPAD Pad Capacitance 9 VPIN Pin Capacitance 10 Zpd Pull down Impedance 35 50 70	V_{OL} Output Low Voltage 0.45 V V_{HYS} Hysteresis Voltage 0.1 V R_{ON} BUffer on Resistance 40 60 Ω I_L Leakage Current -10 10 μA C_{PAD} Pad Capacitance 9 pF V_{PIN} Pin Capacitance 10 pF Z_{pd} Pull down Impedance 35 50 70 Ω



- 1. GPIO_V1P8A_G3 refers to instantaneous voltage VSS_SENSE.
- 2. Measured at 0.31 * GPIO V1P8A G3.
- 3. V_{IN} between 0V and GPIO_V1P8A_G3.
- 4. CPAD includes die capacitance only. No package parasitic included.
- 5. This buffer reaches VOH/VOL with 3mA load.

Figure 38. Definition of VHYS



19.6.17 **GPIO DC Specification**

GPIO Buffer DC specifications.

Table 160. GPIO 1.8V Core Well Signal Group DC Specification

nuc.	Symbol	Parameter	Min	Тур	Max	Units	Notes	eineo.
d undefined undefined und	Vacc	I/O Voltage	GPI	ON_V1P8A OSE_V1P8 <i>A</i>	_G3		65	undefined
· IIUC	V _{IH}	Input High Voltage	0.65*V _{REF}			V	ight	
ined	V _{IL}	Input Low Voltage	U		0.35 * V _{REF}	V	100	
defin	V _{OH}	Output High Voltage	V _{REF} - 0.45		V _{REF}	V		
dune	V _{OL}	Output Low Voltage			0.45	V		
sinec	V _{Hys}	Input Hysteresis	0.1		uno	V		
inde,	IL	Leakage Current	-10	c'i	10	mA		69 V
y m.	C _{LOAD}	Load Capacitance	2	"Ye,	75	pF		stine
ed undefined undefined uni	,defined	Output Low Voltage Input Hysteresis Leakage Current Load Capacitance s buffer reaches VOH/VOL v	, stin	ed unde	ined unde			d undefined
Datasheet		undefin	ed under			efined	269)



SIO - I²C DC Specification 19.6.18

Table 161. I²C Signal Electrical Specifications

	Symbol	Parameter	Min	Тур	Max	Units	Notes
200	V _{REF}	I/O Voltage	GPI	OSE_V1P8A	_G3	V	· ne
od uli.	V _{IH}	Input High Voltage	0.7 * V _{REF}			V	4eill
fine	V _{IL}	Input Low Voltage			0.3 * V _{REF}	V	
inde	V _{OL}	Output Low Voltage			0.2 * V _{REF}	V	
	V _{Hys}	Input Hysteresis	0.1		"Uge.	V	
	C _{PIN}	Pin Capacitance	2		5	pF	

SIO - UART DC Specification 19.6.19

Refer to GPIO Buffer (1.8V) DC Specification, mentioned Section 19.6.17, "GPIO DC Specification"

I²S (Audio) DC Specification 19.6.20

Refer to the GPIO Buffer (1.8V) DC Specification, mentioned Section 19.6.17, "GPIO DC Specification"

PCI Express DC Specification 19.6.21

Table 162. PCI Express DC Receive Signal Characteristics

Symbol	Parameter	Min	Туре	Max	Unit	Notes
V _{RXDIFF Gen1}	Differential RX Peak to Peak	175		1200	mV	1
V _{RXDIFF Gen2}	Differential RX Peak to Peak	100		1200	mV	1

NOTE:

1. PCI Express differential peak to peak = 2*|RXp[x] - RXn[x]|

Table 163. PCI Express DC Transmit Characteristics (Sheet 1 of 3)

ed	Symbol	Parameter	Ul ^{no} Ge	n 1	Ge	n 2	Unit	Notes
defill	Symbol	i di dinetei	Min	Max	Min	Max	SQ	Hotes
od uli	UI	Unit Interval	399.88	400.12	199.94	200.06	ps	1
odefined undefined	V _{TX-DIFF-}	Differential p-p Tx voltage swing	800	1200	800	1200	mV	
	V _{TX-DIFF-LP}	Differential TX Peak to Peak (low power mode)	400	1200	400	1200	mV	
270	undefine		indef	inea			г)atashee
ined undefines		, undefine					ined '	Jacasneed
1efine		sined o				9 nue		



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gen	indi	file		define	d				defined un
Electrical Spe	cifications		Jefined u	no.			in	tel	gen
Table 163.	PCI Expr	ess DC Transmit Charac	cteristics	(Sheet 2	2 of 3)	afined "	Inc		
ndefine	Symbol	Parameter	Ge		4777	n 2	Unit	Notes	ed und
	V _{TX-DE-}	Tx de-emphasis level	Min 3	Max 4	Min 3	Max 4	db	ed v	ndefine
ined une	3.5DB V _{TX-DE-} RATIO-6DB	Tx de-emphasis	-	-	5.5	6.5	db		
ed under	T _{MIN-PULSE}	Instantaneous pulse width	-	-	0.9	efineo	UI		
Indefined undefined unde	T _{TX-EYE}	Transmitter Eye including all jitter sources	0.75	defi	0.75	-	UI		ofined uni
und	T _{TX-EYE} - MEDIAN-to MAX-JITTER	Maximum time between the jitter median and max deviation from the median	ndefined	0.125	-	-	unde	ined i	Inde
efined undefined	T _{TX-HF-DJ-}	Tx deterministic jitter > 1.5 MHz	-	-	-	0.15	UI	3	
ndefine	T _{RF-} MISMATCH	Tx rise/fall mismatch	-	-	neā ur	0.1	UI		ad un
O.	T _{TX-RISE} -	Transmitter rise and fall time	-	inuge,	0.15	-	UI		ndefine
ed un	V _{TX-CM-AC-} PP	Tx AC peak-peak common mode voltage	INGE ING	-	-	150	mVp p	efined	0,
ed underine	V _{TX-DC-CM}	Transmitter DC common-mode voltage	0	3.6	0	3.6	V	4	
d undefined undefined un	V _{TX-CM-DC-} LINEDELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	000	25	mV		undefined u
ad ul	Z _{TX-DIFF} -	DC differential Tx impedance	80	120	-	120	Ω	define	•
ed undefine	I _{TX-SHORT}	Transmitter short-circuit current limit	-	90	-	90	mA	5	
Datasheet	2	current limit	•	bn.	efined	7111			ed undefined t
. 1	ndefined		defin	led m.				nin.	ed uno
Datasheet		definer	J nuc			undefil	ned u	de 27:	1
Jefined L		ined unt			ò	nuge,			



Table 163. PCI E	xpress DC Transmit Charac	cteristics	(Sheet 3	3 of 3)	defili		
Samele	ol Aefille Parameter	Ge	n 1	ed Ge	en 2	Unit	Notes
Symb	oi Parameter	Min	Max	Min	Max	Unit	notes
V _{TX-CM-} ACTIVEI -DELT. V _{TX-IDI} DIFF-AC	of DC Common	o o o	100	0	100	mV	Hined
V _{TX-IDI}		0	20	0	20	mV	
V _{TX-IDI}		-	4 unde	0	5	mV	
T _{TX-D}	Tx deterministic jitter	<u>=</u> 100	-	-	57	ps	.0.
T _{TX-R}	Tx Random jitter	V96,	-	-	3.41	ps	efile
T _{TX-R} T _{TX-} MEDIAN MAX-JIT T _{TX-T}	-to Medium-to-max jitter	_	77	-	-	ps	
T _{TX-T}	Total Jitter @ BER 1E-12	-	-	-	105	ps	

- 1. The specified UI is equivalent to a tolerance of +-300 ppm for each RefClk source. period does not account for SSC induced variations. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
- 2. Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function
- 3. Deterministic jitter only
- The allowed DC common-mode voltage at a transmitter pin under any conditions.
- 5. The total single-ended current a transmitter can supply when shorted to ground.

Table 164. PCI Express DC Clock Request Input Signal Characteristics

Symbol	Parameter	Min	Туре	Max	Unit	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S4				
V_{IL}	Input Low Voltage	٨	nu	0.3*V _{REF}	V	1
V_{IH}	Input High Voltage	0.65*V _{REF}			V	1

NOTE:

1. 3.3 V refers to UNCORE_3P3_S0 for signals in the core well. Refer Chapter 2, "Physical Interfaces" for signal and power well association.

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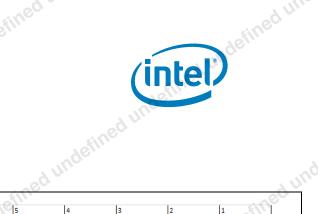


20 Ballout and Ball Map

20.1 Ballout

Figure 39. Ballout - DDR3L-RS (T3) Top View Part A

					_0	7					Y A.		
	25	24	23	22	21	20	19	18	17	16	15	14	13
AE	PWR_RSVD_0 BS	PWR_RSVD_0 BS	DDR3_M0_DQ3 5	DDR3_M0_ODQ VREF	DDR3_M0_OCA	DDR3_M0_RCO MPPD		UARTO_DATAI N	I2C5_DATA	I2C6_CLK/NMI_ N		SD3_RCOMP	UART1_RTS_I
AD	VSS	DDR3_M0_DQ3	DDR3_M0_DQ3 8	vss	DDR3_M0_DQ5			MMC1_RESET_ N	VSS	I2C6_DATA/SD 3_WP		UART1_DATAI N/UART0_DAT	VSS
AC	DDR3_M0_DQS 4_P	DDR3_M0_DM4	DDR3_M0_DQ3 7	DDR3_M0_DQ4 9	RESERVED	GPIO_SW93	LPE_I2S2_FRM	GPIO_SW78	I2C2_DATA	NFC_I2C_CLK	NFC_I2C_DATA	UART1_DATAO UT/UART0_DAT	UART1_CTS_I
AB	DDR3_M0_DQ3 3	DDR3_M0_DQS 4_N	DDR3_M0_DQS 6_P	DDR3_M0_DQ4 8	RESERVED	PCIE_CLKREQ[0]_N	LPE_I2S2_CLK	1_DDC_DATA/	I2C4_CLK/DDI1 _DDC_CLK/DDI	12C5_CLK	LPE_I2S0_DAT AIN	LPE_I2S1_CLK	UART2_DATA UT
AA	DDR3_M0_DQ3	VSS	DDR3_M0_DQS 6_N	DDR3_M0_DQ5 2	VSS	DDR3_CORE_P WROK	DDR3_DRAM_P WROK	VSS	12C2_CLK	LPE_I2SO_CLK	LPE_I2S0_DAT AOUT	LPE_I2S1_FRM	GPIO_SE79
Υ	DDR3_M0_DQ3 9	DDR3_M0_DQ3 4	DDR3_M0_DQ5 3	DDR3_M0_DM6	DDR3_M0_DQ5 5	DDR3_M0_DQ5	DDR3_M0_DQ5 0	I2C0_DATA	12C0_CLK	LPE_I2SO_FRM	DDI_VGG_S0iX	LPE_I2S1_DAT AOUT	LPE_I2S1_DA AIN
W	20		DDR3_M0_DQ4	DDR3_M0_DQ4 2	DDR3_M0_DQ6	DDR3_M0_DQ5 8	VSS	VSS	VSS	I2C1_CLK	I2C1_DATA	DDI_VGG_S0iX	SDIO_V3P3A V1P8A_G3
V	DDR3_M0_DQS 5_P	DDR3_M0_DM5	DDR3_M0_DQ4 0	DDR3_M0_DQ4 6	VSS	DDR3_M0_DQ5 9	DDR_VDDQG_ S4	LPE_I2S2_DAT AOUT	DDI_VGG_S0iX	UNCORE_V1P8 A_G3	UNCORE_V1P8 A_G3	DDI_VGG_S0iX	UARTO_DATA
U	DDR3_M0_DQS 5_N	VSS	DDR3_M0_DQS 7_N	DDR3_M0_DQS 7_P	DDR3_M0_DQ6	DDR3_M0_DQ6	DDR3_M0_DRA MRST_N	DDR_V1P05A_ G3	LPE_I2S2_DAT	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_S0
Т	DDR3_M0_DQ4 7	DDR3_M0_DQ4 1	DDR3_M0_DM7	DDR3_M0_DQ5	DDR3_M0_DQ6	DDR3_M0_DQ5 7	DDR_VDDQG_ S4	VSS	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_S0iX	DDI_VGG_S0
R			DDR3_M0_DQ4	DDR3_M0_DQ4 5	VSS	VSS	VSS	DDR_V1P05A_ G3	DDI_V1p05A_S 0iX	DDI_V1p05A_S 0iX	VSS	DDI_VGG_S0iX	DDI_VGG_S0
Р	DDR3_M0_ODT 1	DDR3_M0_ODT 0	DDR3_M0_CS1 _N	DDR3_M0_CS0 _N	DDR3_M0_WE_ N	DDR3_M0_CAS	DDRSFR_VDDQ G_S4	VSS	VSS	VSS	VSS	VSS	RESERVED
N	DDR3_M0_MA7	VSS	DDR3_M0_MA2	DDR3_M0_RAS _N	VSS	DDR3_M0_MA1	DDR3_M0_BS1	VSS	VSS	VSS	CORE_VCC_S0	CORE_VCC_S0i	VSS
M	DDR3_M0_MA1	DDR3_M0_MA0	DDR3_M0_MA1	DDR3_M0_MA4	DDR3_M0_BS0	DDR3_M0_MA3	VSS	DDR_VDDQG_ S4	VSS	VSS	CORE_VCC_S0	CORE_VCC_S0i	VSS
L			DDR3_M0_MA1	DDR3_M0_MA5	VSS	DDR_VDDQG_ S4	DDR_VDDQG_ S4	DDR_VDDQG_ S4	CORE_V1p05A _S0iX	F_V1p05A_S0i X	CORE_VCC_S0	i CORE_VCC_S0i	UNCORE2_V 05A_G3
K	DDR3_M0_MA1	DDR3_M0_MA6	DDR3_M0_MA1	DDR3_M0_BS2	DDR3_M0_CK1	DDR3_M0_CK1	VSS	DDR_VDDQG_ S4	CORE_V1p05A _S0iX	F_V1p05A_S0i	CORE_VCC_S0	i VSS	VSS
J	DDR3_M0_MA8	VSS	DDR3_M0_CK0	DDR3_M0_CK0	DDR3_M0_DQ2	DDR3_M0_DQ3	VSS	VSS	VSS	VSS	CORE_VCC_S0	i CORE_VCC_S0i	VSS
Н	DDR3_M0_MA1	DDR3_M0_MA0	DDR3_M0_DQ2 7	DDR3_M0_DQ3	VSS	DDR3_M0_DQS 3_P	DDR3_M0_DQS 3_N	DDR_V1P05A_ G3	VSS	VSS	CORE_VCC_S0	i CORE0_VSFR_ G3	UNCORE_V1
G			DDR3_M0_CKE	DDR3_M0_CKE 0	DDR3_M0_DQ2 8	DDR3_M0_DQ2		CORE_V1p05A _S0iX	CORE_V1p05A _S0iX	VSS	CORE_VCC_S0	i CORE_VCC_S0i	
F	DDR3_M0_DQ1 9	DDR3_M0_DQ2	DDR3_M0_CKE 2	DDR3_M0_CKE 3	DDR3_M0_DQ2 5	DDR3_M0_DQ2 4	DDR3_M0_DM3		GPIO_N1/C0_B PM3_TX/C1_BP	GPIO_N2/C0_B PM2_TX/C1_BP	VSS	JTAG_TMS	JTAG_TD0
E	DDR3_M0_DQ1 6	VSS	DDR3_M0_DQ1	DDR3_M0_DQ1	VSS	DDR3_M0_DQ1	DDR3_M0_DQ1	VSS	M3 TV GPIO_N0/C0_B PM0_TX/C1_BP	GPIO_N4/C0_B	VSS	JTAG_TCK	JTAG_TRST_
D	DDR3_M0_DM2	DDR3_M0_DQ2 1	DDR3_M0_DQ9	DDR3_M0_DQ1 2	DDR3_M0_DM1	DDR3_M0_DQ1	DDR3_M0_DQS 0_P	DDR3_M0_DQ0	ISH_GPIO[13]/C 0_BPM2_TX/C1	MO TV	JTAG2_TMS	JTAG2_TDO	JTAG_PRDY_
С	DDR3_M0_DQS 2_N	DDR3_M0_DQS 2_P	DDR3_M0_DQ1	DDR3_M0_DQS 1_P	DDR3_M0_DQS 1_N	DDR3_M0_DQ8	DDR3_M0_DQS 0_N	DDR3_M0_DQ3	GPIO_N3/C0_B PM1_TX/C1_BP	M1 TV GPIO_N6/C0_B PM3_TX/C1_BP	JTAG2_TCK	PMC_SUSCLK[2	GPIO_SUS8
В	PWR_RSVD_0 BS	DDR3_M0_DQ2 0	DDR3_M0_DQ2 2	DDR3_M0_DQ7	VSS	DDR3_M0_DQ5		DDR3_M0_DQ1	M1 TV	GPIO0_RCOMP	-	JTAG2_TDI	VSS
A		VSS	DDR3_M0_DQ1	DDR3_M0_DQ4	DDR3_M0_DQ2	DDR3_M0_DM0	-	DDR3_M0_DQ6	DDR_VDDQG_ S4	CORE_V1p05A		GPIO_SUS0	GPIO_SUS9

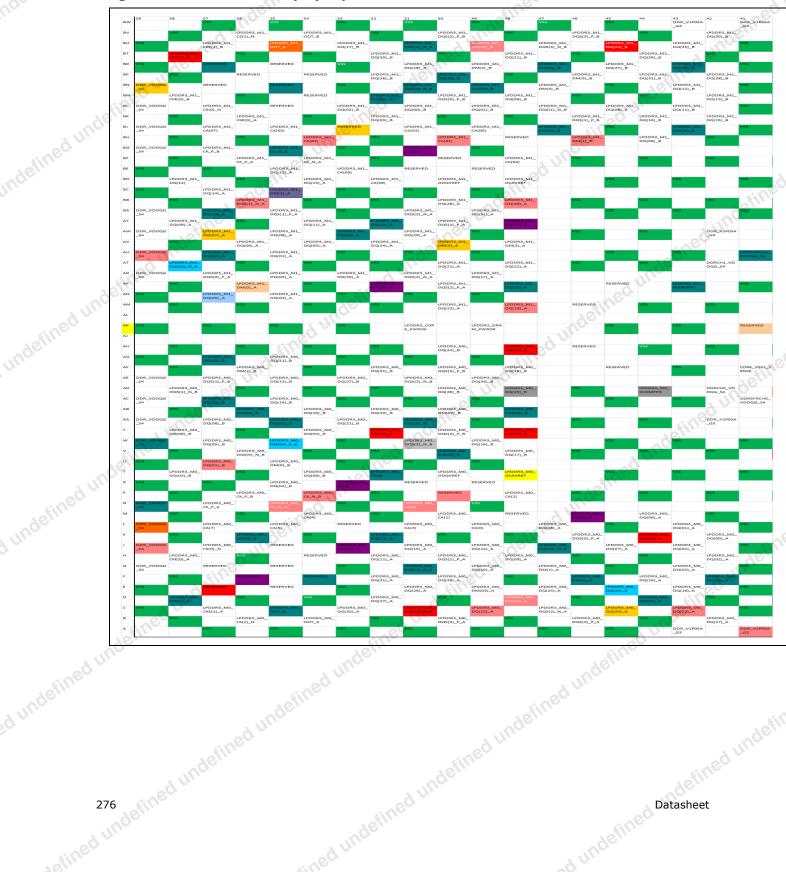


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				76///					:196					-0-
		12	11	10	9	8	7	6	5	4	3	2	1	1
	A	UART2_DATAI	ned	MMC1_RCOMP	SD3_CD_N	MMC1_RCLK/M MC1_RESET_N		DDI_VGG_S0iX	SD2_D[2]	SD2_D[1]	PMC_PLT_CLK[5]/ISH_GPIO[15]	RESERVED	RESERVED	
	A	D UART2_CTS_N		SD3_D[3]	VSS	MMC1_CLK	defilm	SD2_D[3]_CD_ N	SD2_CLK		PWM[0]	PWM[1]/ISH_GPI O[10]/ISH_UAR		
		C_UART2_RTS_N		SD3_D[0]	SD3_CLK	MMC1_D[5]	MMC1_D[4]	MMC1_D[3]	VSS	2]/ISH_GPI0[12]	PMC_PLT_CLK[4]/ISH_GPIO[14]	4_CLK	4_DATAIN	
a under	A	B FST_SPI_CLK	FST_SPI_D[0]	SD3_D[2]	SD3_D[1]	SD3_1P8_EN	MMC1_D[6]	MMC1_D[2]	SD2_CMD	PMC_PLT_CLK[3]/ISH_GPIO[13]		ISH_GPIO[0]/I2S 3_CLK	ICLK_ICOMP	
Indefined undef	A	A FST_SPI_CS[0] _N		SD3_CMD	SD3_PWREN_N		MMC1_D[7]	MMC1_CMD	MIDSS DATAOL	ISH_GPIO[9]/ISH S_SPI_MISO/I2S5	SH_SPI_CLK/I2		ICLK_RCOMP	
Inde	_	UARTO_DATAC		RESERVED	USB_OC[0]_N	MMC1_D[1]	VSS	VSSA	PMC_PLTRST_ N]		ISH_GPI0[1]/I2S 3_FS	ISH_GPIO[3]/I2S 3_DATAIN	leg,
	_	VSS	VSS	RESERVED	UNCORE_V1P8 A_G3		ICLK_OSCIN	ICLK_OSCOUT		PMC_SLP_SOIX _N	N		"uge,	
		PMC_SUSPWR DNACK	N	UNCORE_V1P8 A_G3		RTC_V3P3RTC _G5	46/11	VSS	PMC_SUS_STA T_N		_P	_N	S4	
4		DDI_VGG_S0iX				RTC_V3P3A_G 5		RTC_TEST_N	RTC_RST_N	RTC_X2	RTC_X1	VSS	RTC_EXTPAD	
inde	T	DDI_VGG_S0iX		05A_G3	2	Silli		ROK	N	PCIE_RCOMP_N	Jec.	PCIE_RXN0	PCIE_RXP0	
undefined unde	R	VSS	DDI_VGG_S0iX		VSS	ICLK_VSFR_G3			VSS	PCIE_TXP0	PCIE_TXN0			
ingeli	P	VSS		DDI_VGG_S0iX	S4		PCIeCLK_V1P0 5A_G3		USB3_RXN0	N	USB3_RCOMP_ P		USB3_TXP0	ed
		DDI_VGG_S0iX	69,	S4		MPHY_1P05A_ G3	MPHY_1P05A_ G3	, un	USB3_RXP0	ATA	USB_HSIC_1_S TROBE		USB_HSIC_RC OMP	
		UNCORE_VSFR _G3	S4	S4	S4		USBSSIC_V1P0 5A_G3	Ve	USB_DP2	USB_DP3	USB_DN3	USB_HSIC_0_D ATA	USB_HSIC_0_S TROBE	
	_	UNCORE_VNN_ S4	S4	S4	S4	3	nu.	UNCORE_VSFR _G3		USB_DP1	USB_DN1	geill		
76		UNCORE_VNN_ S4	S4	S4	S4	A_G3	Q_G3		DDI2_TXP3	DDI2_TXP1	DDI2_TXN1	USB_VBUSSNS		
med un	_	VSS	VSS	S4	S4	USBHSIC_V1P2 A_G3	Q_G3		DDI2_AUXN	DDI2_TXN0	DDI2_TXP0	VSS	USB_RCOMP	
Jundefined und	H	USB_V1P8A_G	3	113	3	DDI_USB_VDD Q_G3			DDI2_AUXP	0	DDI0_RCOMP_P	DDI2_TXP2	DDI2_TXN2	
y or.	_	RESERVED	VSS	VSS	3	UNCORE_VSFR _G3		VSS	VSS	DDI0_TXN0	DDI0_TXP0	DDIO TOUR		line
		SVID_DATA	SVID_CLK	RESERVED	PROCHOT_N		MCSI_1_CLKP	veo.	DDI0_TXP2		DDI0_TXP3		DDIO_AUXN	
	_	SVID_ALERT_N		DDI2_DDC_CLK /DDI1_DDC_CL K/IIAPTO_DAT GPI0_CAMERA		MCSI_1_DP0 DDI1_BKLTCTL/	VSS	VSS MCSI_1_DP3	MCSI 2 CLKP	MDSI_A_DP3 MDSI_A_CLKN		DDH_RCOMP_P	DDI0_AUXP	
2		JTAG_TDI	GPIO_CAMERA SB08 GPIO_CAMERA	SB09	DDI2_DDC_DAT	MDSI_A_TE/MD	MCSI_1_DN2	MCSI_1_DP3	MCSI_2_CLKP		MDSI_A_DP0	MDSI_A_DP1	MDSI_A_DN1	
ed un	-	PMC SUSCLK(3	SB11	A/DDI1_DDC_D ATA/MDSL_DDC GPI0_CAMERA	A/DDI1_DDC_D	DDIO_BKLTCTL	INCSI_1_DF2	MCSI_1_DN1	VSS	MCSI_2_DN0	MCSI_2_DN1	MDSI_A_DN0	RESERVED	-
adefine	<u> </u>] CORE_VCC_S0		SB10 DDI0_DDC_CLK	Uer.	MCSI_RCOMP		MCSI_1_DP1	MDSI_RCOMP	MCSI_2_DP0	MCSI_2_DP1	RESERVED		
id undefined und	_	Х		/DDI1_DDC_CL		_			76//					file
_		heet	ndefine	<i>J</i>		ndefine	-nde	fined o	*		efined '	4efil?	ied nuo	
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Da Lefined un					.1	ndeill					efines			
iefine.					aned v					ad uno	,			



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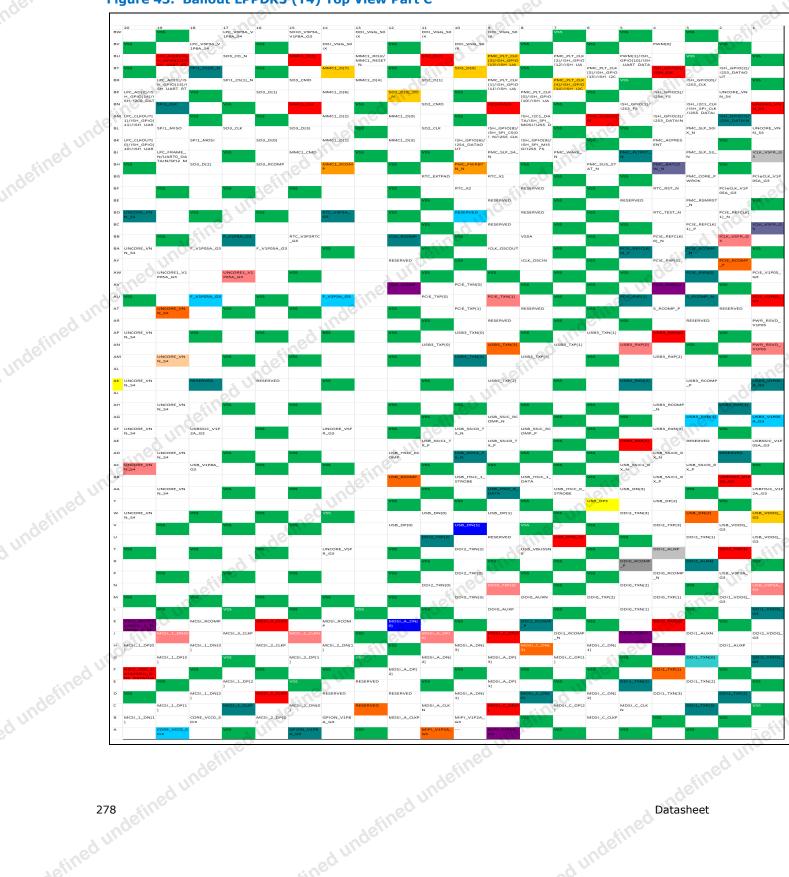
undefined undefined undefineu (T Figure 42. Ballout LPPDR3 (T4) Top View Part B



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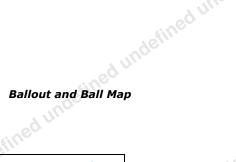


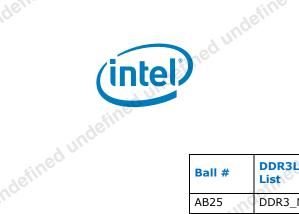
Ballout and Ball Map **SoC T3 Pin List Location** 20.2

Ball #	DDR3L-RS Customer Pin List	Ball AA2
A10	DDI0_DDC_CLK/	AA2
	MDSI_DDC_CLK	AA2
A12	CORE_VCC_S0iX	AA2
A13	GPIO_SUS9	AA2
A14	GPIO_SUS0	AA3
A16	CORE_V1p05A_S0iX	0.04
A17	DDR_VDDQG_S4	AA4
A18	DDR3_M0_DQ6	AA5
A2	RESERVED	UEO.
A20	DDR3_M0_DM0	200
A21	DDR3_M0_DQ2	AA6
A22	DDR3_M0_DQ4	AA7
A23	DDR3_M0_DQ17	AA8
A24	VSS	AA9
A25	PWR_RSVD_OBS	AB1
A3	MCSI_2_DP1	AB1
A4	MCSI_2_DP0	AB1
A5	MDSI_RCOMP	AB1
A6	MCSI_1_DP1	AB1
A8	MCSI_RCOMP	AB1
A9	DDI0_VDDEN	AB1
AA1	ICLK_RCOMP	AB1
AA10	SD3_CMD	AB1
AA11	VSS	
AA12	FST_SPI_CS0_N	AB1
AA13	GPIO_SE79	69 m
AA14	LPE_I2S1_FRM	eline
AA15	LPE_I2SO_DATAOUT	AB1
AA16	LPE_I2S0_CLK	AB2
-		l L
AA17	I2C2_CLK	AB2
	I2C2_CLK VSS	AB2
AA17		
AA17 AA18	VSS	AB2
	A12 A13 A14 A16 A17 A18 A2 A20 A21 A22 A23 A24 A25 A3 A4 A5 A6 A8 A9 AA1 AA10 AA11 AA12 AA13 AA14 AA15	A10

		4 011
Ball #	DDR3L-RS Customer Pin List	ndefined une
AA21	VSS	U.C.
AA22	DDR3_M0_DQ52	
AA23	DDR3_M0_DQS6_N	
AA24	VSS	
AA25	DDR3_M0_DQ36	
AA3	ISH_I2C1_CLK/ISH_SPI_CLK/ I2S5_DATAIN	ind
AA4	ISH_GPIO9/ISH_SPI_MISO/ I2S5_FS	undefined und
AA5	ISH_I2C1_DATA/ ISH_SPI_MOSI/ I2S5_DATAOUT	unde
AA6	MMC1_CMD	
AA7	MMC1_D7	
AA8	MMC1_D0	
AA9	SD3_PWREN_N	
AB1	ICLK_ICOMP	undefined un
AB10	SD3_D2	"ineo
AB11	FST_SPI_D0	delli
AB12	FST_SPI_CLK	n,
AB13	UART2_DATAOUT	
AB14	LPE_I2S1_CLK	
AB15	LPE_I2S0_DATAIN	
AB16	I2C5_CLK	
AB17	I2C4_CLK/DDI1_DDC_CLK/ DDI2_DDC_CLK/ MDSI_DDC_CLK	d undefined u
AB18	I2C4_DATA/	iefine
30 011	DDI1_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	dunae
AB19	LPE_I2S2_CLK	
AB2	ISH_GPIO0/I2S3_CLK	1
AB20	PCIE_CLKREQ0_N	1
AB21	RESERVED	1
AB22	DDR3_M0_DQ48	
AB23	DDR3_M0_DQS6_P	ined '
AB24	DDR3_M0_DQS4_N	defill
(ea	DDR3_M0_DQ48 DDR3_M0_DQS6_P DDR3_M0_DQS4_N	ed une
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idefined undefine		adefined u.			
	Ball #	DDR3L-RS Customer Pin List		Ball #	DD Lis
10.	AB25	DDR3 M0 DQ33		AD1	RES
	AB3	ISH_GPIO2/I2S3_DATAOUT		AD10	SD3
indefined undefined un	AB4	PMC_PLT_CLK3/ISH_GPIO13/	:0e0	AD12	UAF
777	9.0	ISH_UART_RTS_N/SPI2_CLK		AD13	VSS
raed or	AB5	SD2_CMD		AD14	UAF
4efill.	AB6	MMC1_D2			UAF
4 uno	AB7	MMC1_D6		AD16	I2C
	AB8	SD3_1P8_EN		AD17	VSS
	AB9	SD3_D1		AD18	MM
	AC1	ISH_GPIO7/I2S4_DATAIN		AD2	PWI
	AC10	SD3_D0		AD20	ISH
	AC11	FST_SPI_D1	Sine		SD3
Jefined ur	AC12	UART2_RTS_N	8,,	AD22	DDI
	AC13	UART1_CTS_N		AD22 AD23	VSS
/	AC14	UART1_DATAOUT/			
	AC1 F	UARTO_DATAOUT		AD25	DDI
	AC15 AC16	NFC_I2C_DATA		AD25 AD3	VSS
	AC17	NFC_I2C_CLK			76
	AC17	I2C2_DATA		AD5	SD2
	ACIO	GPIO_SW78	4	AD5	SD2
	AC19	LPE_I2S2_FRM	afin'	AD8	SD2
-d1	AC2	ISH_GPIO4/I2S4_CLK	10.	AD0	MM
	AC20	GPIO_SW93		AD9	VSS
	AC21	RESERVED		AE10	RES
	AC22	DDR3_M0_DQ49		AE10	MM
	AC24	DDR3_M0_DQ37		AE12	UAF
	AC24	DDR3_M0_DM4		AE13	UAF
efined v	AC25	DDR3_M0_DQS4_P		AE14 AE16	SD3
		PMC_PLT_CLK4/ISH_GPIO14/ ISH_I2C0_DATA/SPI2_MISO		AE16 AE17	I2C
	AC4	PMC_PLT_CLK2/ISH_GPIO12/	4efil	AE17	UAF
ed	0.	ISH_UART_CTS_N/ SPI2_CS0_N		AE18	RES
elin	AC5	VSS		AE20	DDI
	AC5	MMC1 D3		AE20 AE21	DDI
	AC6	MMC1_D3		AE21 AE22	DDI
	AC7	410		AE22 AE23	DDI
	AC0	MMC1_D5		ΛΕ24	77.
defined undefined	AC9	SD3_CLK	ndefi	AE24	PW
fined una		ed unden.			
76/.		City			

		Ballout and Ball Map
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		istine
	Ball #	DDR3L-RS Customer Pin List RESERVED SD3_D3 UART2_CTS_N
	AD1	RESERVED
_	AD10	SD3_D3
UEO	AD12	UART2_CTS_N
	AD13	VSS
	AD14	UART1_DATAIN/ UART0_DATAIN
	AD16	I2C6_DATA/SD3_WP
	AD17	VSS
	AD18	MMC1_RESET_N
	AD2	VSS MMC1_RESET_N PWM1/ISH_GPIO10/ ISH_UART_DATAOUT SD3_WP
e	AD20	SD3_WP
	AD21	DDR3_M0_DQ51
	AD22	VSS
	AD23	DDR3_M0_DQ38
	AD24	DDR3_M0_DQ32
	AD25	VSS
	AD3	PWM0
	AD4	PWM0 SD2_D0 SD2_CLK SD2_D3_CD_N
	AD5	SD2_CLK
.:.08	AD6	SD2_D3_CD_N
S.L.I.	AD8	MMC1_CLK
	AD9	VSS
	AE1	RESERVED
	AE10	MMC1_RCOMP
	AE12	UART2_DATAIN
	AE13	UART1_RTS_N
	AE14	SD3_RCOMP
	AE16	UART2_DATAIN UART1_RTS_N SD3_RCOMP I2C6_CLK/NMI_N I2C5_DATA UART0_DATAIN
113	AE17	I2C5_DATA
6,.	AE18	UARTO_DATAIN
	AE2	RESERVED
	AE20	DDR3_M0_RCOMPPD
	AE21	DDR3_M0_OCAVREF
	AE22	DDR3_M0_ODQVREF
	AE23	DDR3_M0_DQ35
	AE24	PWR_RSVD_OBS
defi	ued u	DDR3_M0_ODQVREF DDR3_M0_DQ35 PWR_RSVD_OBS
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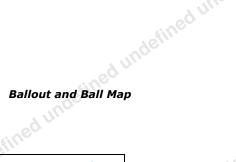
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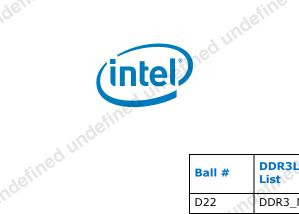


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	ndefin			
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	deill			
Ball #	DDR3L-RS Customer Pin List		Ball #	D
AE25	PWR_RSVD_OBS		C16	G
AE3	PMC_PLT_CLK5/ISH_GPIO15/ ISH_I2C0_CLK/SPI2_MOSI	ed u	C17	G
AE4	SD2_D1			С
AE5	SD2_D2			D
AE6	DDI_VGG_S0iX			D
AE8	MMC1_RCLK/MMC1_RESET_N		C2	М
AE9	SD3_CD_N		C20	D
B1	RESERVED		C21	D
B10	GPIO_CAMERASB10		C22	D
DIZ	PMC_SUSCLK3	. 4	C23	D
	VSS	red	C24	D
B14	JTAG2_TDI	11.	C25	D
B16			C3	М
B17	VSS		C4	М
B18	10		C5	М
B2	-		C6	М
B20			C7	М
B21			C8	D
חרים			C9	D
B23		ined		D U
B24				М
B25			D1	D
B3			D10	G
B4	AU'		D11	G
B5	A Vi		D12	V
B6	440		D13	J
B8	0		D14	J٦
	_		D15	J٦
C1		SING	D16	G
C10	-	S.		С
	DDI1_DDC_DATA/ MDSI_DDC_DATA		D17	C
C11	GPIO_CAMERASB11		D18	D
C12	JTAG_TDI		D19	D
C13	GPIO_SUS8		D2	D
	760.		D20	D
C14	PMC_SUSCLK2		D20	
	Ball # AE25 AE3 AE4 AE5 AE6 AE8 AE9 B1 B10 B12 B13 B14 B16 B17 B18 B2 B20 B21 B22 B23 B24 B25 B3 B4 B5 B6 B8 B9 C1 C10	Ball # DDR3L-RS Customer Pin List AE25 PWR_RSVD_OBS AE3 PMC_PLT_CLK5/ISH_GPIO15/ISH_I2CO_CLK/SPI2_MOSI AE4 SD2_D1 AE5 SD2_D2 AE6 DDI_VGG_S0IX AE8 MMC1_RCLK/MMC1_RESET_N AE9 SD3_CD_N B1 RESERVED B10 GPIO_CAMERASB10 B12 PMC_SUSCLK3 B13 VSS B14 JTAG2_TDI B16 GPIO0_RCOMP B17 VSS B18 DDR3_M0_DQ1 B2 MDSI_A_DNO B20 DDR3_M0_DQ5 B21 VSS B22 DDR3_M0_DQ7 B23 DDR3_M0_DQ20 B24 DDR3_M0_DQ20 B25 PWR_RSVD_OBS B3 MCSI_2_DN1 B4 MCSI_2_DN0 B5 VSS B6 MCSI_1_DN1 B8 DDIO_BKLTCTL B9 VSS	Map	

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Ball #	DDR3L-RS Customer Pin List	ndefined und
C16	GPIO_N6/C0_BPM3_TX/ C1_BPM3_TX	defined
C17	GPIO_N3/C0_BPM1_TX/ C1_BPM1_TX	inc.
C18	DDR3_M0_DQ3	
C19	DDR3_M0_DQS0_N	
C2	MDSI_A_DP1	
C20	DDR3_M0_DQ8	
C21	DDR3_M0_DQS1_N	undefined und
C22	DDR3_M0_DQS1_P	ed o
C23	DDR3_M0_DQ18	defille
C24	DDR3_M0_DQS2_P	und
C25	DDR3_M0_DQS2_N	
C3	MDSI_A_DP0	
C4	MDSI_A_CLKP	
C5	MCSI_2_CLKN	
C6	MCSI_1_DN3	
C7	MCSI_1_DP2	710
C8	DDI0_BKLTEN	ined
C9	DDI2_DDC_DATA/ DDI1_DDC_DATA/ UART0_DATAIN/ MDSI_DDC_DATA/MDSI_C_TE	undefinedun
D1	DDI1_RCOMP_N	
D10	GPIO_CAMERASB09	
D11	GPIO_CAMERASB08	
D12	VSS	
D13	JTAG_PRDY_N	defined u
D14	JTAG2_TDO	sinet.
D15	JTAG2_TMS	"uger
D16	GPIO_N8/C0_BPM1_TX/ C1_BPM1_TX	d undefine
D17	ISH_GPIO13/C0_BPM2_TX/ C1_BPM2_TX	
D18	DDR3_M0_DQ0	1
D19	DDR3_M0_DQS0_P	1
D2	DDI1_RCOMP_P	
D20	DDR3_M0_DQ15	ined.
D21	DDR3_M0_DM1	defin
	DDI1_RCOMP_P DDR3_M0_DQ15 DDR3_M0_DM1	ed un.
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Ball #	ndefinee	_		
Ball #	DDR3L-RS Customer Pin List		Ball #	DD Lis
D22	DDR3_M0_DQ12		E7	VSS
D23	DDR3_M0_DQ9		E8	MC
D24	DDR3_M0_DQ21	"Vec	E9	DD
D25	DDR3_M0_DM2		F1	DD1
D3	MDSI_A_DP2		F10	RES
D4	MDSI_A_CLKN		F11	SVI
D5	MCSI_2_CLKP		F12	SVI
D6	MCSI_1_DP3		F13	JTA
D7	MCSI_1_DN2		F14	JTA
D24 D25 D3 D4 D5 D6 D7 D8	DDI1_BKLTCTL/MDSI_A_TE/ MDSI_C_TE		F15	VSS
D9	DDI0_HPD	ane	0, 10	C1_
und E1	DDIO_AUXP	Silli	F17	GPI
E1 E10 E11 E12 E13	DDI2_DDC_CLK/ DDI1_DDC_CLK/		F18	C1_ GPI
unoc	UARTO_DATAOUT/ MDSI_DDC_CLK/MDSI_A_TE		F19	DDI
E11	VSS		F2	DD
E12	SVID ALERT N		F20	DDI
E13	JTAG_TRST_N		F21	DDI
E14	JTAG_TCK		F22	DDI
	VSS	440	F23	DDI
E16	GPIO_N4/C0_BPM0_TX/	etil.	F24	DDI
ned a large	C1_BPM0_TX		F25	DDI
E15 E16 E17 E18 E19 E2 E20	GPIO_N0/C0_BPM0_TX/ C1_BPM0_TX		F3	DD1
E18	VSS		F5	DDI
E19	DDR3_M0_DQ10		F6	DD
E2	VSS		F7 20	MCS
E20	DDR3_M0_DQ14		F8	MCS
E21	VSS	20.00	F9	PRO
E22	DDR3_M0_DQ13	deill	G10	VSS
E23	DDR3_M0_DQ11		G11	VSS
E24	VSS		G12	RES
E25	DDR3_M0_DQ16		G12	UNG
E3	MDSI_A_DN2		G14	COF
E4	MDSI_A_DP3		G15	COF
E5	MDSI_A_DN3		C1C	VSS
E6	VSS		-4000	1
E5	MDSI_A_DN3	Indef	C1C	-

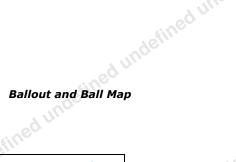
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F1 DDI0_AUXN F10 RESERVED F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDI0_TXN3 F2 DDI0_TXN3 F2 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE2 F24 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDI0_TXP3 F4 RESERVED F5 DDI0_TXP2 F6 DDI0_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_VIDOSA_SOIX <		_{{\\\}}	
F1 DDI0_AUXN F10 RESERVED F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDI0_TXN3 F2 DDI0_TXN3 F2 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE2 F24 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDI0_TXP3 F4 RESERVED F5 DDI0_TXP2 F6 DDI0_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_VIDOSA_SOIX <	Ball #	DDR3L-RS Customer Pin List	ndi
F1 DDIO_AUXN F10 RESERVED F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDIO_TXN3 F2 DDIO_TXN3 F2 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE2 F24 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_VIDO5A_SOIX G14 CORE_VCC_SOIX	E7	VSS	
F1 DDIO_AUXN F10 RESERVED F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDIO_TXN3 F2 DDIO_TXN3 F2 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE2 F24 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_VIDO5A_SOIX G14 CORE_VCC_SOIX	E8	MCSI_1_DP0	
F10 RESERVED F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDIO_TXN3 F2 DDIO_TXN3 F20 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE3 F23 DDR3_MO_CKE2 F24 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0IX G14 CORE_VCC_S0IX G16 VSS	E9	DDI2_HPD	
F11 SVID_CLK F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_MO_DM3 F2 DDIO_TXN3 F2 DDIO_TXN3 F20 DDR3_MO_DQ24 F21 DDR3_MO_DQ25 F22 DDR3_MO_CKE3 F23 DDR3_MO_CKE3 F23 DDR3_MO_DQ23 F25 DDR3_MO_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0IX G16 VSS	F1	DDI0_AUXN	
F12 SVID_DATA F13 JTAG_TDO F14 JTAG_TMS F15 VSS F16 GPIO_N2/CO_BPM2_TX/ C1_BPM2_TX F17 GPIO_N1/CO_BPM3_TX/ C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_M0_DM3 F2 DDIO_TXN3 F20 DDR3_M0_DQ24 F21 DDR3_M0_DQ25 F22 DDR3_M0_CKE3 F23 DDR3_M0_CKE2 F24 DDR3_M0_DQ23 F25 DDR3_M0_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F10	RESERVED	
F13	F11	SVID_CLK	
F17	F12	SVID_DATA	
F17 GPIO_N1/CO_BPM3_TX/C1_BPM3_TX F18 GPIO_DFX4 F19 DDR3_M0_DM3 F2 DDIO_TXN3 F20 DDR3_M0_DQ24 F21 DDR3_M0_DQ25 F22 DDR3_M0_CKE3 F23 DDR3_M0_CKE2 F24 DDR3_M0_DQ23 F25 DDR3_M0_DQ19 F3 DDIO_TXP3 F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F13	JTAG_TDO	
F17	F14	JTAG_TMS	
F17	F15	VSS	
F17	F16	GPIO_N2/C0_BPM2_TX/ C1_BPM2_TX	
F19	F17	GPIO_N1/C0_BPM3_TX/	
F2 DDI0_TXN3 F20 DDR3_M0_DQ24 F21 DDR3_M0_DQ25 F22 DDR3_M0_CKE3 F23 DDR3_M0_CKE2 F24 DDR3_M0_DQ23 F25 DDR3_M0_DQ19 F3 DDI0_TXP3 F4 RESERVED F5 DDI0_TXP2 F6 DDI0_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F18	GPIO_DFX4	
F20 DDR3_M0_DQ24 F21 DDR3_M0_DQ25 F22 DDR3_M0_CKE3 F23 DDR3_M0_CKE2 F24 DDR3_M0_DQ23 F25 DDR3_M0_DQ19 F3 DDI0_TXP3 F4 RESERVED F5 DDI0_TXP2 F6 DDI0_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F19	DDR3_M0_DM3	
F25	F2	DDI0_TXN3	
F25	F20	DDR3_M0_DQ24	UL
F25	F21	DDR3_M0_DQ25	Þ.
F25	F22	DDR3_M0_CKE3	
F25	F23	DDR3_M0_CKE2	
F3	F24	DDR3_M0_DQ23	
F4 RESERVED F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DN0 F9 PROCHOT_N G10 VSS G11 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F25	DDR3_M0_DQ19	
F5 DDIO_TXP2 F6 DDIO_TXN2 F7 MCSI_1_CLKP F8 MCSI_1_DNO F9 PROCHOT_N G10 VSS G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F3	DDI0_TXP3	
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F4	RESERVED	
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F5	DDI0_TXP2	
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F6	DDI0_TXN2	90
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F7 00	MCSI_1_CLKP	
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F8	MCSI_1_DN0	
G11 VSS G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	F9	PROCHOT_N	
G12 RESERVED G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	G10	VSS	
G13 UNCORE_V1p05A_S0iX G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS	G11	VSS	
G14	G12	RESERVED	
G14 CORE_VCC_S0iX G15 CORE_VCC_S0iX G16 VSS Datasheet	G13	UNCORE_V1p05A_S0iX	
G15 CORE_VCC_S0iX G16 VSS Datasheet	G14	CORE_VCC_S0iX	
G16 VSS Datasheet	G15	CORE_VCC_S0iX	6
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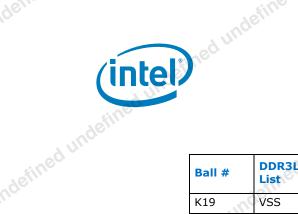
-82 Indefined under



DR3L-RS Customer Pin ist ORE_V1p05A_S0iX ORE_V1p05A_S0iX DR_V1P05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXP0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3 DI2_TXN2	led.	H8 H9 J1 J10 J11 J12 J13 J14 J15 J16 J17	D M U U V V V V C C
DR3L-RS Customer Pin ist ORE_V1p05A_S0iX ORE_V1p05A_S0iX DR_V1P05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3		H8 H9 J1 J10 J11 J12 J13 J14 J15 J16 J17	
ORE_V1p05A_S0iX ORE_V1p05A_S0iX ORE_V1p05A_S0iX DR_V1p05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	,ed 1	H8 H9 J1 J10 J11 J12 J13 J14 J15 J16 J17	
ORE_V1p05A_S0iX DR_V1p05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	,ed 1	H9 J1 J10 J11 J12 J13 J14 J15 J16 J17	M U V V
ORE_V1p05A_S0iX DR_V1p05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	, ed 1	J1 J10 J11 J12 J13 J14 J15 J16	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DR_V1P05A_G3 DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	ed'	J10 J11 J12 J13 J14 J15 J16 J17	V V
DR3_M0_DQ26 DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	(ed)	J11 J12 J13 J14 J15 J16	V V
DR3_M0_DQ28 DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	(ed)	J12 J13 J14 J15 J16 J17	V V C
DR3_M0_CKE0 DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	(ed	J12 J13 J14 J15 J16 J17	V C
DR3_M0_CKE1 DI0_TXP0 DI0_TXN0 SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	(ed	J14 J15 J16 J17	V C
DIO_TXPO DIO_TXNO SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	led!	J14 J15 J16 J17	С
DIO_TXNO SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	(ed	J15 J16 J17	
SS SS CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	ed.	J16 J17	
CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	ed'	J17	V
CSI_1_CLKN NCORE_VSFR_G3 IPI_V1P2A_G3	eo.		V
NCORE_VSFR_G3 IPI_V1P2A_G3		J18	V
IPI_V1P2A_G3		J19	V
		J2	V
		J20	D
SS		J20 J21	D
SB_V1P8A_G3		J21 J22	D
			٧
		10//	D
	د	111.	۷
	Uec		D
-04	, **		D
SS		J4 	D
SS		J5	D
		J6	D
DR3_M0_DQS3_N		J7	D
DI2_TXP2		J8	U
DR3_M0_DQS3_P		J9	U
SS		K1	U
DR3_M0_DQ31	ine	K10	U
DR3_M0_DQ27		K11	U
DR3_M0_MA09		K12	U
DR3_M0_MA14		K13	٧
DI0_RCOMP_P		K14	٧
DIO_RCOMP_N		K15	С
DI2_AUXP		K16	F
DIO_TXP1		K17	С
SB_VDDQ_G3		K18	D
	SB_V1P8A_G3 NCORE_V1p05A_S0iX DREO_VSFR_G3 DRE_VCC_S0iX SS DR_V1P05A_G3 DR3_M0_DQS3_N D12_TXP2 DR3_M0_DQS3_P SS DR3_M0_DQ31 DR3_M0_DQ27 DR3_M0_DQ27 DR3_M0_MA09 DR3_M0_MA14 D10_RCOMP_P D10_RCOMP_N D12_AUXP D10_TXP1 SB_VDDO_G3	SB_V1P8A_G3 NCORE_V1p05A_S0iX DRE0_VSFR_G3 DRE_VCC_S0iX SS DR_V1P05A_G3 DR3_M0_DQS3_N D12_TXP2 DR3_M0_DQS3_P SS DR3_M0_DQ31 DR3_M0_DQ27 DR3_M0_DQ27 DR3_M0_MA09 DR3_M0_MA09 DR3_M0_MA14 D10_RCOMP_P D10_RCOMP_N D12_AUXP D10_TXP1	J23 J24 J24 J24 J25 J24 J25
	efine		
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Ball #	DDR3L-RS Customer Pin List	defined unde	
H8	DDI_USB_VDDQ_G3		
H9	MIPI_V1P2A_G3		
J1	USB_RCOMP		
J10	UNCORE_VNN_S4		
J11	VSS		
J12	VSS		
J13	VSS		
J14	CORE_VCC_S0iX		
J15	CORE_VCC_S0iX	ndefined und	
J16	VSS		
J17	VSS		
J18	VSS		
J19	VSS		
J2	VSS		
J20	DDR3_M0_DQ30		
J21	DDR3_M0_DQ29		
J22	DDR3_M0_CK0_P		
J23	DDR3_M0_CK0_N		
J24	VSS	defille	
J25	DDR3_M0_MA8	indefined un	
J3	DDI2_TXP0		
J4	DDI2_TXN0		
J5	DDI2_AUXN		
J6	DDI0_TXN1		
J7	DDI_USB_VDDQ_G3		
J8	USBHSIC_V1P2A_G3	, 11	
J9	UNCORE_VNN_S4	"ineo	
K1	USB_OTG_ID	geili	
K10	UNCORE_VNN_S4	undefinedu	
K11	UNCORE_VNN_S4		
K12	UNCORE_VNN_S4		
K13	VSS		
K14	VSS		
K15			
K16	F_V1p05A_S0iX	-61	
K17	CORE_V1p05A_S0iX	Fines	
K18	DDR_VDDQG_S4	"uge"	
	CORE_VCC_S0iX F_V1p05A_S0iX CORE_V1p05A_S0iX DDR_VDDQG_S4		
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Ball #	Indefine	\neg		
Ball #	DDR3L-RS Customer Pin List		Ball #	DD Lis
K19	VSS		M10	UN
K2	USB_VBUSSNS		M11	UNG
K20	DDR3_M0_CK1_P	ined	M12	UNG
K21	DDR3_M0_CK1_N	76///	M13	VSS
K22	DDR3_M0_BS2		M14	COF
K23	DDR3_M0_MA15		M15	COI
K20 K21 K22 K23 K24 K25 K3	DDR3_M0_MA6		M16	VSS
K25	DDR3_M0_MA11		M17	VSS
K3	DDI2_TXN1		M18	DDI
K4	DDI2_TXP1		M19	VSS
K5	DDI2_TXP3		M2	USE
K6	DDI2_TXN3	SINE	M20	DDI
K7	DDI_USB_VDDQ_G3	10,5//	M21	DDI
K6 K7 K8 K9 L10 L11 L12 L13	USBSSIC_V1P2A_G3		M22	DDI
К9	UNCORE_VNN_S4		M23	DDI
L10	UNCORE_VNN_S4		M24	DDI
L11	UNCORE_VNN_S4	\dashv	M25	DDI
L12	UNCORE_VNN_S4	\dashv	M3	USE
L13	UNCORE2_V1P05A_G3	\dashv	M4	USE
1140	CORE_VCC_S0iX	=	M5	USE
L15	CORE_VCC_S0iX	ning	M6	USE
L16	F_V1p05A_S0iX	Wale	M7	USE
L17	CORE_V1p05A_S0iX	P.	M8	VSS
L14 L15 L16 L17 L18 L19 L20 L21	DDR_VDDQG_S4	\dashv	M9	UNG
L19	DDR_VDDQG_S4	\dashv	N1	USE
L20	DDR_VDDQG_S4		N10	UNG
L21	VSS	\dashv	N11	DDI
L22	DDR3_M0_MA5		N12	DD1
123	DDR3_M0_MA1		N13	VSS
L3	USB_DN1	Aefil	N14	COF
L4	USB_DP1	UI	N15	COF
L5	VSS		N16	VSS
L6	UNCORE_VSFR_G3		N17	VSS
L7	VSS		N18	VSS
L8	USB_V3P3A_G3		N19	DDI
L3 L4 L5 L6 L7 L8 L9	UNCORE_VNN_S4		N2	VSS
M1 Andefined undefin	USB_HSIC_0_STROBE		N20	DDI

	Ballout and Ball Map
	raed und
Ball #	UNCORE_VNN_S4 UNCORE_VNN_S4 UNCORE_VSFR_G3
M10	UNCORE_VNN_S4
M11	UNCORE_VNN_S4
M12	UNCORE_VSFR_G3
M13	VSS
M14	CORE_VCC_S0iX
M15	CORE_VCC_S0iX
M16	VSS
M17	VSS DDR_VDDQG_S4 VSS USB_HSIC_0_DATA DDR3 M0 MA3
M18	DDR_VDDQG_S4
M19	VSS
M2	USB_HSIC_0_DATA
M20	DDR3_M0_MA3
M21	DDR3_M0_BS0
M22	DDR3_M0_MA4
M23	DDR3_M0_MA13
M24	DDR3_M0_MA0
M25	DDR3_M0_MA12
M3	USB_DN3
M4	USB_DP3
M5	DDR3_M0_MA12 USB_DN3 USB_DP3 USB_DP2 USB_DN2
M6	USB_DN2
M7	USBSSIC_V1P05A_G3
M8	VSS
M9	UNCORE_VNN_S4
N1	USB_HSIC_RCOMP
N10	UNCORE_VNN_S4 DDI_VGG_S0iX DDI_VGG_S0iX VSS CORE_VCC_S0iX
N11	DDI_VGG_S0iX
N12	DDI_VGG_S0iX
N13	VSS
N14	CORE_VCC_S0iX
N15	CORE_VCC_S0iX
N16	VSS
N17	VSS
N18	VSS
N19	DDR3_M0_BS1
N2	VSS
N20	DDR3_M0_MA10
160	DDR3_M0_BS1 VSS DDR3_M0_MA10
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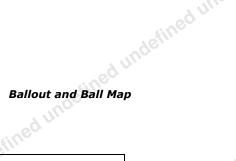
-84 undefined undefin

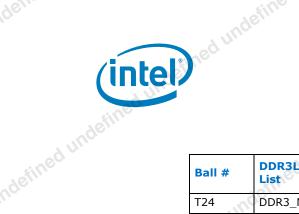


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		ine adefined undefin	led m	*	
indefine		defined			
Ballout and Bal	Ball #	DDR3L-RS Customer Pin List		Ball #	E
	N21	VSS	_	R10	V
	N22	DDR3_M0_RAS_N		R11	Е
ile	N23	DDR3_M0_MA2	hed,	R12	ν
Inde	N24	VSS	-	R13	D
ined to	N25	DDR3_M0_MA7	_	R14	D
fined undefined undefi	N3	USB_HSIC_1_STROBE		R15	V
4 uno	N4	USB_HSIC_1_DATA		R16	D
	N5	USB3_RXP0	1	R17	D
	N6	USB_DP0	1	R18	D
	N7	MPHY_1P05A_G3		R19	V
	N8	MPHY_1P05A_G3	٨	R20	V
Aei	N9	VSS	Uen	R21	V
4 Uno	P1	USB3_TXP0	1	R22	D
	P10	DDI_VGG_S0iX	1	R23	D
defined undef	P11	DDI_VGG_S0iX		R3	Р
	P12	VSS	1	R4	Р
	P13	RESERVED		R5	٧
	P14	VSS		R6	V
	P15	VSS		R7	F
		VSS	00	R8	I
29	P17	VSS	line	R9	V
ed ni.	P18	VSS		T1	Р
	P19	DDRSFR_VDDQG_S4		T10	U
defined und	P2	USB3_TXN0		T11	D
	P20	DDR3_M0_CAS_N		T12	D
	P21	DDR3_M0_WE_N		T13	D
	P22	DDR3_M0_CS0_N		T14	D
	P23	DDR3_M0_CS1_N		T15	D
	P24	DDR3_M0_ODT0		T16	D
100	P25	DDR3_M0_ODT1	efill	T17	D
ned u	P3	USB3_RCOMP_P		T18	V
defills	P4	USB3_RCOMP_N		T19	D
	P5	USB3_RXN0		T2	Р
	P6	USB_DN0		T20	D
	P7	PCIeCLK_V1P05A_G3		T21	D
	P8	VSS		T22	D
undefined und		UNCORE_VNN_S4	4	T23	D

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Ball #	DDR3L-RS Customer Pin List VSS DDI_VGG_S0iX	6
R10	VSS	
R11	DDI_VGG_S0iX	
R12	VSS	
R13	DDI_VGG_S0iX	
R14	DDI_VGG_S0iX	
R15	VSS	
R16	DDI_V1p05A_S0iX	
R17	DDI_V1p05A_S0iX	
R18	DDI_V1p05A_S0iX DDR_V1P05A_G3 VSS VSS	
R19	VSS	
R20	VSS	
R21	VSS	
R22	DDR3_M0_DQ45	
R23	DDR3_M0_DQ44	
R3	PCIE_TXN0	
R4	PCIE_TXP0	
R5	VSS	
R6	VSS	
R7	F_V1P05A_G3	
R8	VSS VSS F_V1P05A_G3 ICLK_VSFR_G3	
R9	VSS	
T1	PCIE_RXP0	
T10	UNCORE1_V1P05A_G3	
T11	DDI_VGG_S0iX	
T12	DDI_VGG_S0iX	
T13	DDI_VGG_S0iX	V
T14	DDI_VGG_S0iX	
T15	DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX	
T16	DDI_VGG_S0iX	
T17	DDI_VGG_S0iX	
T18	VSS	
T19	DDR_VDDQG_S4	
T2	PCIE_RXN0	
T20	DDR3_M0_DQ57	
T21	DDR3_M0_DQ63	
T22	DDR3_M0_DQ56	
T23	DDR3_M0_DM7	
	DDR3_M0_DQ63 DDR3_M0_DQ56 DDR3_M0_DM7	
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Ball #	indefine			
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T24	DDR3_M0_DQ41		V12	PMO
T25	DDR3_M0_DQ47		V13	UAF
T3	PCIE_RCOMP_P	inec	V14	DD
T3 T4 T5 T6 T7 T8 T9 U1	PCIE_RCOMP_N	46/11	V15	UNG
T5	PMC_RSMRST_N		V16	UNG
T6	PMC_CORE_PWROK		V17	DD
und T7	F_V1P05A_G3		V18	LPE
T8	VSS		V19	DDI
Т9	F_V1P05A_G3		V2	PCI
U1	RTC_EXTPAD		V20	DDI
U10	DDI_VGG_S0iX		V21	VSS
U11	DDI_VGG_S0iX	Sine	V22	DDI
U12	DDI_VGG_S0iX	10 _{5/.}	V23	DDI
U11 U12 U13 U14 U15 U16 U17	DDI_VGG_S0iX		V24	DDI
U14	DDI_VGG_S0iX		V25	DDI
U15	DDI_VGG_S0iX		V3	PCI
U16	DDI_VGG_S0iX		V4	RES
U17	LPE_I2S2_DATAIN		V5	PMC
U18	DDR_V1P05A_G3		V6	VSS
1119	DDR3_M0_DRAMRST_N		V7	VSS
U2	VSS	efin	V8	RTC
U20	DDR3_M0_DQ62	10	V9	VSS
U21	DDR3_M0_DQ60	<i></i>	W10	RES
U22	DDR3_M0_DQS7_P		W11	VSS
U23	DDR3_M0_DQS7_N		W12	VSS
U24	VSS		W13	SDI
U2 U20 U21 U22 U23 U24 U25 U3	DDR3_M0_DQS5_N		W14	DDI
U3	RTC_X1		W15	I2C
U4	RTC_X2		W16	I2C
U5	RTC_RST_N	Aefill	W17	VSS
U6	RTC_TEST_N	UIT	W18	VSS
U7	F_V3P3A_G3		W19	VSS
U8	RTC_V3P3A_G5		W20	DDI
U9	F_V1P8A_G3		W21	DDI
U5 U6 U7 U8 U9 V1 V10 V11	UNCORE_VNN_S4		W22	DDI
	UNCORE_V1P8A_G3		W23	DDI
V10		undef		PMC

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	lefine
Ball #	DDR3L-RS Customer Pin List
V12	PMC_SUSPWRDNACK
/13	UARTO_DATAIN
V14	DDI_VGG_S0iX
V15	UNCORE_V1P8A_G3
V16	UNCORE_V1P8A_G3
/17	DDI_VGG_S0iX
V18	LPE_I2S2_DATAOUT
V19	DDR_VDDQG_S4
/2	PCIE_REFCLK0_N
/20	DDR3_M0_DQ59
/ 21	VSS
/22	DDR_VDDQG_S4 PCIE_REFCLK0_N DDR3_M0_DQ59 VSS DDR3_M0_DQ46
V23	DDR3_M0_DQ40
/24	DDR3_M0_DM5
V25	DDR3_M0_DQS5_P
V3	PCIE REFCLKO P
/4	RESERVED
/5	PMC_SUS_STAT_N
V6	VSS
V7	RESERVED PMC_SUS_STAT_N VSS VSS RTC_V3P3RTC_G5
/8	RTC V3P3RTC G5
/9	VSS
W10	RESERVED
W11	VSS
W12	VCC
V12	SDIO V3P3A V1P8A G3
W14	DDI_VGG_S0iX
V14	I2C1_DATA
V15	SDIO_V3P3A_V1P8A_G3 DDI_VGG_S0iX I2C1_DATA I2C1_CLK VSS
V10 V17	VSS (A)
V17 V18	VSS
V19	VSS
N20	DDR3_M0_DQ58
N21	DDR3_M0_DQ61
N22	DDR3_M0_DQ42 DDR3_M0_DQ43 PMC_PWRBTN_N
	DDR3_M0_DQ43
W23 W3	PMC PWRBTN N

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gen		indef	ine		defined	
		ll Map	ine lefined undefi	ned ur		
ndefined l	Indefine		adefined			
		Ball #	DDR3L-RS Customer Pin List		Ball #	E
		W4	PMC_SLP_S0IX_N		Y2	I
		W5	VSS	_	Y20	D
	undefined undef	W6	ICLK_OSCOUT	ned u	Y21	D
	Unoc	W7	ICLK_OSCIN		Y22	D
	ined.	W8	VSS		Y23	D
	defill	W9	UNCORE_V1P8A_G3		Y24	D
2	Um	Y1	ISH_GPIO3/I2S3_DATAIN		Y25	D
		Y10	RESERVED		Y3	Р
		Y11	VSS		Y4	Р
		Y12	UARTO_DATAOUT		Y5	Р
			LPE_I2S1_DATAIN	6	Y6	٧
	ade	Y14	LPE_I2S1_DATAOUT	SILVER	Y7	٧
	ad une	Y15	DDI_VGG_S0iX	7	Y8	М
		Y16	LPE_I2S0_FRM		Y9	U
	inge.	Y17	I2C0_CLK			
	3 0.	Y18	I2C0_DATA			
4efille		Y19	DDR3_M0_DQ50			
nuor	d undefined under	sed un	4er.		undefin	

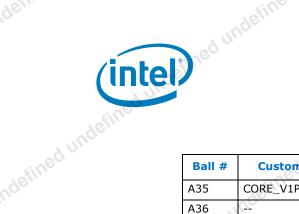
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DDR3L-RS Customer Pin List	ndefined unde
ISH_GPIO1/I2S3_FS	sinec
DDR3_M0_DQ54	uger.
DDR3_M0_DQ55	
DDR3_M0_DM6	
DDR3_M0_DQ53	
DDR3_M0_DQ34	
DDR3_M0_DQ39	
PMC_WAKE_N	6
PMC_SUSCLK0	ndefined und
PMC_PLTRST_N	istine
VSSA	inge
VSS	0.
MMC1_D1	
USB_OC0_N	
	ISH_GPIO1/I2S3_FS DDR3_M0_DQ54 DDR3_M0_DQ55 DDR3_M0_DM6 DDR3_M0_DQ53 DDR3_M0_DQ34 DDR3_M0_DQ39 PMC_WAKE_N PMC_SUSCLK0 PMC_PLTRST_N VSSA VSS MMC1_D1

	Y13	LPE_I2S1_DATAIN	-8	Y6	VSSA
-8	Y14	LPE_I2S1_DATAOUT	FILES	Y7	VSS
undefined undefined und	Y15	DDI_VGG_S0iX	3	Y8	MMC1_D1
	Y16	LPE_I2S0_FRM		Y9	USB_OCO_N
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lu ,	A15	GPION_V1P8A_G3	96//	A29	
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A30	CORE_V1P15_S0iX	
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ige,	A35	CORE_V1P15_S0iX		AA15	VSS
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	A38		Ue	AA18	
dulle	A39	VSS		AA19	UNCO
indefined undefined und	A4	Loed	1	AA2	
"uge"	A40	Yellus		AA20	
ed u.	A41	DDR_V1P05A_G3		AA21	UNCO
18fins	A42	cineo		AA22	6
	A43	DDR_V1P05A_G3]	AA23	UNCO
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	A45	VSS	-6	AA25	UNCO
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ed u.	A47	VSS		AA27	UNCO
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	A5	VSS		AA3	VSS
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	A58			AA38	VSS
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AA25	UNCORE_V1P15_S0iX	
AA26	"1060	
AA27	UNCORE_VNN_S4	
AA28	June	
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AA32	VSS	
AA33	uni	
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AA35		
AA36	UNCORE VNN S4	
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-0	VSS	
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AA42	DDR_VIPUSA_G3	
AA43		
AA44	VSS	
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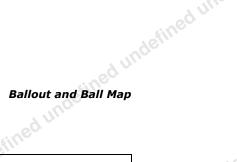
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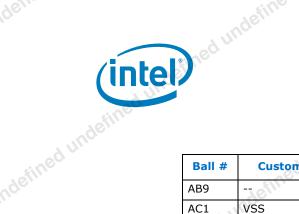


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AA51	LPDDR3_M0_DQ[18]_B	AB31	
AA52	"1000	AB32	
AA53	LPDDR3_M0_DQ[21]_B	AB33	
AA54	defill	AB34	
AA55	LPDDR3_M0_DQ[07]_B	AB35	
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AA57	LPDDR3_M0_DQ[08]_B	AB37	
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AA6	4611	AB4	USB
AA7	USB_HSIC_0_STROBE	AB40	
AA8	sinec	AB41	
AA9	USB_HSIC_0_DATA	AB42	
AB1	ad u	AB43	
AB10	USB_HSIC_1_STROBE	AB44	-E0
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AB20	USBHSIC_VIPZA_G3	AB53	
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AB36	-4 m	adefined uni
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AB4	USB_SSIC1_RX_P	
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AB42	- fine	
AB43	110/6	
AB44	-69	, un
AB45		undefined un
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AB48	LPDDR3_M0_DM[03]_B	
AB49	"udge,	
AB5	89	
AB50	LPDDR3_M0_DM[02]_B	
AB51	Indo	
AB52	LPDDR3_M0_DQ[23]_B	90
AB53		edefined v
AB54	LPDDR3_M0_DQ[10]_B	"uge.
AB55		
AB56	LPDDR3_M0_DQ[09]_B	
AB57	und	
AB58	VSS	
AB59	gen	
AB6	VSS	
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AB8	USB_HSIC_1_DATA	defille
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ger.	AB9	-18/100		AC42	450
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	AC11	VSS	Ue,	AC45	VSS
4 nu	AC12	1706		AC46	
	AC13	69		AC47	
ndefined undefined un	AC14	VSS		AC48	
ed u.	AC15	UNO		AC49	VSS
16fin	AC16	VSS		AC5	USB_S
	AC17	96 ₁₁		AC50	1400
	AC18	USB_V1P8A_G3		AC51	VSS
	AC19			AC52	
	AC2	46		AC53	VSS
Indefined undefined un	AC20	UNCORE_VNN_S4		AC54	
efine	AC21	:100		AC55	LPDDR
uno	AC22	VSS		AC56	
	AC23	dun		AC57	LPDDR
defili	AC24	UNCORE_VSS_SENSE		AC58	69
	AC25	-inde		AC59	DDR_\
	AC26	UNCORE_VNN_SENSE		AC6	
	AC27			AC7	VSS
	AC28	RESERVED		AC8	
	AC29	duli		AC9	VSS
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dune	AC30	Inde		AD10	USB_S
	AC31	UNCORE_VNN_S4		AD11	
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Α'	AC36		e,	AD16	
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lefine	AC4			AD2	RESER
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	AC41	DDRSFRCH0_VDDQG_S4		AD21	UNCOF

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AC46 AC47 AC48 AC49 AC5 AC50 AC51 AC52 AC53	VSS VSS USB_SSIC1_RX_N VSS VSS	
AC47 AC48 AC49 AC5 AC50 AC51 AC52 AC53	VSS USB_SSIC1_RX_N VSS VSS	
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AC56	Sine	
AC57	LPDDR3_M0_DQ[13]_B	
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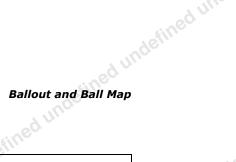
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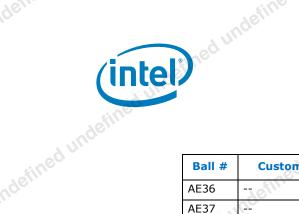


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	AD26	Inde		AD6	VSS
	AD27	UNCORE_VNN_S4		AD7	
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	AD32	CORE_VCC1_S0iX	ed	AE12	
	AD32 AD33 AD34 AD35 AD36 AD37 AD38 AD39	461		AE13	
	AD34	CORE_VCC1_S0iX		AE14	
	AD35	sineo		AE15	
	AD36	CORE_VCC1_S0iX		AE16	
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age III.	AD38	CORE_VCC1_S0iX		AE18	69
	AD39	Tuge.		AE19	122
	AD4	USB_SSIC0_RX_N		AE2	
	AD40	F_V1P15_S0iX	We	AE20	
	AD41			AE21	
	AD42	DDRCH0_VDDQG_S4		AE22	
	AD43	Sine	1	AE23	
	AD44	LPDDR3_M0_RCOMPPD	1	AE24	
Sine	AD45	- ned	1	AE25	
"IUGIE"	AD46	VSS	1	AE26	06
	AD40 AD41 AD42 AD43 AD44 AD45 AD46 AD47 AD48	1700	1	AE27	
	***	LPDDR3_M0_DQ[25]_B		AE28	
	AD49		110	AE29	
	AD5	mo	Ĭ	AE3	RESI
	AD50	LPDDR3_M0_DQ[26]_B	1	AE30	
	AD51	- defill	1	AE31	
	AD52	VSS	4	AE32	
defill	AD53		-	AE33	
Unc	AD49 AD5 AD50 AD51 AD52 AD53 AD54 AD55	VSS	-	AE34	27/1/3
	AD55	- J J. - J.]	AE35	P

Ball #	Customer Name - LPDDR3	defined un
AD56	VSS	ad ul
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AD58	LPDDR3_M0_DQS[1]_N_B	yge.
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AE27	2	- Lefined
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AE3	RESERVED	1
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Ball #	Customer Name - LPDDR3		Ball #	Cus
AE36	- efine	-	AF16	VSS
AE37	1100	-	AF17	
AE38		1	AF18	USBSS
AE39	&	ue,	AF19	
AE4	ndei	-	AF2	VSS
AE40	20 1111	-	AF20	UNCO
AE41	Sine	=	AF21	
AE39 AE4 AE40 AE41 AE42 AE43 AE44 AE45	inge,		AF22	UNCO
AE43	280		AF23	\
AE44	28410		AF24	UNCO
AE45	1200		AF25	
AE46		-	AF26	UNCO
		iu_6	AF27	
AE47 AE48 AE49 AE5 AE50 AE51 AE52	Inde	*	AF28	RESER
AE49	LPDDR3_M0_DQ[30]_B		AF29	
AE49	USB3_RXP[3]		AF3	
AE50	USB3_KXP[3]		AF30	
AE51	20	-		
AESI	LPDDR3_M0_DQS[3]_N_B	-	AF31	VSS
AE52		-	AF32	
ALSS	LPDDR3_M0_DQ[27]_B		AF33	CORE_
AE54		410	AF34	
AE55	LPDDR3_M0_DQ[12]_B	8,	AF35	CORE_
AE56	edu''	-	AF36	
AE55 AE56 AE57 AE58 AE59 AE6 AE7 AE8	LPDDR3_M0_DQS[1]_P_B		AF37	CORE_
AE58	unde		AF38	
AE59	DDR_VDDQG_S4		AF39	CORE_
AE6	Jefine		AF4	USB3_
AE7	VSS		AF40	G-
AE8	(e) ² -		AF41	CORE_
AE9	USB_SSICO_TX_P	130	AF42	
AF1		70.	AF43	VSS
AF10	USB_SSICO_TX_N		AF44	
AF11	Lefin		AF45	RESER
AF12	VSS		AF46	
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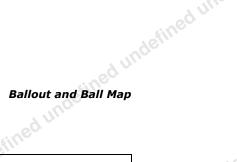
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AF19	ned	
AF2	VSS	1
AF20	UNCORE_VNN_S4	1
AF21	sine	1
AF22	UNCORE_VNN_S4	
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AF24	UNCORE2_V1P05A_G3	, sed
AF25		defills
AF26	UNCORE2_V1P05A_G3	undefined
AF27	cine	
AF28	RESERVED	1
AF29	3011	1
AF3	sine	
AF30	"uge,	
AF31	VSS	
AF32	£712	ine
AF33	CORE_VCC1_S0iX	defill
AF34		d undefine
AF35	CORE_VCC1_S0iX	
AF36	inde	
AF37	CORE_VCC1_S0iX	
AF38	isline	†
AF39	CORE_VCC1_SENSE	†
AF4	USB3_RXN[3]	-
AF40	Cili	2013
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AF43	VSS	
AF44	Inde	1
AF45	RESERVED	1
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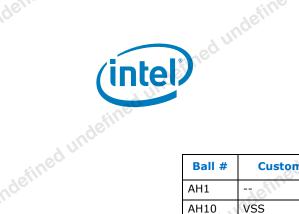
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A	F50	LPDDR3_M0_DQS[3]_P_B	_	AG30	
	F51		-	AG31	
A	F52	LPDDR3_M0_DQ[31]_B		AG32	
LINOS A	F53			AG33	
A A	F54	VSS		4G34	
defill.	F55	Sinec		4G35	
4 Unit	F56	76,	_	4G36	
	F56 F57	LPDDR3_M0_DM[1]_B		4G36 4G37	
della					<u> </u>
A	F58	VSS		AG38	
	F59			AG39	
10	F6	VSS		AG4	
, uno A	F7			AG40	
A	F8	USB_SSIC_RCOMP_P		AG41	
A	F9			AG42	
AUNT	G1	USB3_V1P05A_G3		4G43	
A	G10	89 1111		4G44	
A	G11	VSS	1	4G45	0
А	G12	TO OF THE PERSON	1	AG46	12.
' '	G13	Y	,	4G47	
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A	G17	%1000	7	4G50	
A	G18	"Jger	,	4G51	VSS
A	G19	3d 711,		AG52	
A	G2	Aines	_	AG53	VSS
A	G20	wye,	_	AG54	
	G21		_	AG55	LPDI
	G22		- 1	AG56	
A	G23	006		AG57	LPDI
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4 une	G25 G26	"uqeji,	_	4G6	
ineo A	G20 G27	60 nn		4G7	VSS
deil.	G27 G28	lejine	_	4G7 4G8	V33
A	G28 G29	,no	-	100	USB
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	Ball #	Customer Name - LPDDR3	defined und
	AG3	USB3_RXN[1]	ed ui.
	AG30		efine
6	AG31		100
6	AG32		
	AG33	defin	
	AG34	4 Uni	
	AG35	EINEG	
	AG36	Sqe	
	AG37	-d m	ndefined uni
	AG38	12	red to
	AG39		defill
eg	AG4		iuo.
	AG40	sine	
	AG41		
	AG42	ad un	
	AG43	Silve	
	AG44	illique	
	AG45	-ed	الله لم
	AG46		adefined un
	AG47		dell
100	AG48		71.
	AG49	VSS	
	AG5	VSS	
	AG50		
	AG51	VSS	
	AG52	- une	
	AG53	VSS	ed u
	AG54	77.	istine
	AG55	LPDDR3_M0_DQ[11]_B	nuqeir.
	AG56		
9	AG57	LPDDR3_M0_DQ[15]_B	
	AG58	un	
]	AG59	VSS	
	AG6	ye,	
]	AG7	VSS	
	AG8	Time	ined.
	AG9	USB_SSIC_RCOMP_N	deilli
efir			4 nuc
e,		fine	
		"luge"	
		293	
		48 fine	
		VSS USB_SSIC_RCOMP_N 293	
		20	_





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	Ball #	Customer Name - LPDDR3		Ball #	Cus
der.	AH1	Chine		AH43	10°0
	AH10	VSS		AH44	VSS
	AH11			AH45	
	AH12	VSS		AH46	RESER
4 nu	AH13			AH47	
	AH14			AH48	LPDDR
indefined undefined und	AH15	VSS		AH49	
ed u.	AH16	Inde		AH5	
18 fine	AH17	VSS		AH50	LPDDR
	AH18	9e,,		AH51	140
	AH19	UNCORE_VNN_S4		AH52	VSS
	AH2	USB3_RXP[1]		AH53	
	AH20	20		AH54	VSS
ed u.	AH21	UNCORE_VNN_S4		AH55	
Indefined undefined un	AH22	sinea		AH56	VSS
, nuor	AH23	UNCORE_VNN_S4		AH57	
	AH24	dui		AH58	VSS
defill	AH25	UNCORE_VNN_S4		AH59	69
	AH26	-1096		AH6	VSS
	AH27	RESERVED		AH7	
	AH28			AH8	VSS
. 1	AH29	VSS		AH9	
	АН3	3011		АЈ1	
defill	AH30	fine		AJ10	
4 un	AH31	Inde		AJ11	
	AH32	CORE_VCC1_S0iX		AJ12	
undefined undefined u	AH33	- Lefine		AJ13	-ine
	AH34	CORE_VCC1_S0iX		AJ14	6-1
	AH35	O		AJ15	
	AH36	CORE_VCC1_S0iX		AJ16	
A1	AH37		e.	AJ17	
	AH38	CORE_VCC1_S0iX		AJ18	
"udei"	AH39	lefine		AJ19	
ed un	AH4	USB3_RCOMP_N		AJ2	
iefine	AH40	VSS		AJ20	
undefined undefined	AH41	delli		AJ21	610
	AH42	VSS		AJ22	Ge.

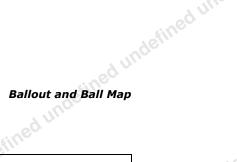
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	Ball #	Customer Name - LPDDR3	indefined und
	AH43	Co.	od un.
	AH44	VSS	istine
	AH45		nde
No.	AH46	RESERVED	
1	AH47	4ellin	
	AH48	LPDDR3_M0_DQ[28]_B	
	AH49	inco	
-	AH5	- deff	-
	AH50	LPDDR3_M0_DQ[24]_B	undefined uni
	AH51	(A)	ed u.
-	AH52	VSS	ie fine
	AH53		INOG
	AH54	VSS	
	AH55	36111	1
	AH56	VSS	1
	AH57	£ineo	1
-	AH58	VSS	-
1	AH59		21.
	AH6	VSS	ed t
	AH7	g* 	undefined un
	AH8	VSS	und
	AH9	sine)·
2	AJ1	"ndeli	-
	AJ10	30 31	-
	AJ11	- Sine	1
	AJ12	Inde	1
1	AJ13		od v
	AJ14	Cill	d undefined
	AJ15		"uge"
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	AJ18	unde	-
-	AJ19		-
	AJ2	Zejin	†
	AJ20	1 Unio	1
	AJ21	:: neo	ر 6ء
	AJ22	Geim	stines
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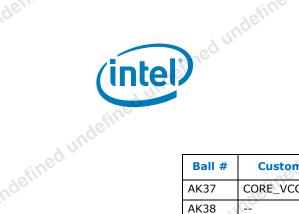
-94 Indefined undefine 122 Indefined undefined



gen	led Uni	Jefine		adefine	30
		Jefine	,d \	ili.	
Ballout and Ballou		defined			
sined b	Ball #	Customer Name - LPDDR3		Ball #	C
ger	AJ23	- fine		AJ57	So.
	AJ24	0		AJ58	
	AJ25		A	AJ59	
ndefined undefined undef	AJ26	7/2		АЈ6	
uno	AJ27	:\deli		AJ7	
ineo -	AJ28			AJ8	
deilli	AJ29			AJ9	
4 une	AJ3	1/096,		AK1	USB
sine .	AJ30	60		AK10	
'961,	AJ31	+811		AK11	VSS
	AJ32			AK12	
<u> </u>				4777	
28	AJ33			AK13	
und	AJ34	dell		AK14	VSS
	AJ35	Julia		AK15	
defili	AJ36	sinet		AK16	RES
4 Une	AJ37	'9'E'		AK17	
inec.	AJ38	du'		AK18	RES
der	AJ39	file		AK19	0
	AJ4	in de		AK2	12-
	, 13 . 0	Y		AK20	UNC
	AJ41			AK21	
, IIIO	AJ42	de		AK22	DDI
::ned	AJ43	d un		AK23	
defill	AJ44	sine		AK24	DDI
Unc	AJ45	"Jer		AK25	
iineo	AJ46	09/07		AK26	VSS
odein	AJ47	61108		AK27	. - -e
	AJ48	-700		AK28	COR
_	AJ49			AK29	
	AJ5			AK3	USB
110	AJ50			AK30	
ined w	AJ51	100		AK31	COR
4efill.	AJ52	4100		AK31	
, unc	AJ53	"uqe,,		AK33	COR
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AJ8	Juna	
AJ9	«ined	
AK1	USB3_V1P05A_G3	
AK10	d U/A	
AK11	VSS	ed
AK12		ndefined u
AK13		UC
AK14	VSS	
AK15	defini	
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AK17	files	
AK18	RESERVED	
AK19	-eq.m.	indefined '
AK2		"Ted
AK20	UNCORE_VNN_S4	defili
AK21	3	and
AK22	DDI_VGG_S0iX	
AK23	ndeli	
AK24	DDI_VGG_S0iX	
AK25	Isline	
AK26	VSS	
AK27	eq	1efined
AK28	CORE1_VSFR_G3	*ineo
AK29		nuqei.
AK3	USB3_RCOMP_P	O.
AK30	lefine	
AK31	CORE1_VSFR_G3	
AK32		
AK33	CORE_VCC1_S0iX	
AK34	4 nuo	
AK35	CORE_VCC1_S0iX	
AK36	2-	iefine
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ined by	CORE_VCC1_S0iX	
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idefined undefine		adefine			
	Ball #	Customer Name - LPDDR3		Ball #	Cus
	AK37	CORE_VCC1_S0iX		AL17	1450.
	AK38	00		AL18	
	AK39	RESERVED		AL19	
60.	AK4		Up	AL2	
ad ull	AK40	Inde		AL20	
Stines	AK41	RESERVED		AL21	
Indefined undefined und	AK42	Lefin		AL22	
ed a	AK43	VSS		AL23	
defilin	AK44	sineo		AL24	6
	AK45	VSS		AL25	100
	AK46	277		AL26	
	AK47		6	AL27	
	AK48			AL28	
ed u.	AK49	LPDDR3_DRAM_PWROK		AL29	
undefined undefined un	AK5	USB3_RXN[2]		AL3	
uno	AK50	gen		AL30	
	AK51	LPDDR3_CORE_PWROK		AL31	
defill	AK52	fine		AL32	69
	AK53	VSS		AL33	6/7//
	AK54	2.		AL34	
	AK55	VSS	21.55	AL35	
111.	AK56		S _{II} ,	AL36	
	AK57	VSS		AL37	
defin	AK58	sine		AL38	
dun	AK59	VSS		AL39	
	AK6	69		AL4	
undefined undefined u	AK7	VSS		AL40	-ine
	AK8	-Inos		AL41	6-1
	AK9	USB3_TXP[2]		AL42	
	AL1		41	AL43	
A V	AL10	'''	Je,	AL44	
Jundefined undefined t	AL11	ed w		AL45	
aden	AL12	Jefine		AL46	
ed m.	AL13	una		AL47	
iefine	AL14			AL48	
Inde	AL15	defil		AL49	(10)
	AL16	T UNC		AL5	90,

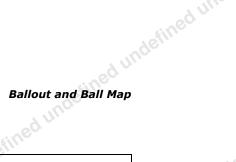
Ball #	Customer Name - LPDDR3	undefined un
AL17	CSO.	ed uli
AL18		Filher
AL19		"uge,
AL2	80	-
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AL21	, , , , , , ,	1
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AL24	4 0/10	undefined ur
AL25	(TO)	eg u
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AL28		
AL29	461100	-
AL29	uno	-
AL30	:: Cod v	-
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		d undefined v
AL32	ELIVEO .	- ad 13
AL33		Sine
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AL42		unos
AL43		0.0
AL44	indefin	
AL45	uno	
AL46	sineo	
AL47	"96 _{11,}	
AL48	dule	
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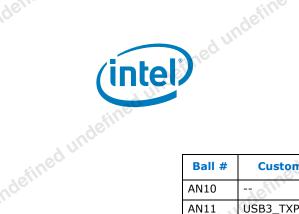
-96 Indefined undefine 15 Lindefined undefined



91,	ined uni	Jefine	ndefine	5Q
		Jefined undefined	, UII.	
Ballout and B		defined		
	Ball #	Customer Name - LPDDR3	Ball #	C
le,	AL50	- Alle	AM30	So.
	AL51	0	AM31	
	AL52		AM32	VSS
	AL53	27/3	AM33	
, unc	AL54	2061	AM34	PWR
	AL55		AM35	
deill	AL56	Fine	AM36	DDI
A Ullia	AL57	1/1/26	AM37	
Jefined undefined unde	AL58	60	AM38	DDI
	AL59	±8/1/0	AM39	
	AL6	N	AM4	USB:
			AM40	DDI
ed undefined und	AL7		AM41	
4 Une	ALO	ye.		
	AL9 AM1	co um	AM42 AM43	VSS
delli	AM10			
	AM10	USB3_TXN[2]	AM44	VSS
	AM11	NCC	AM45	
	AM12	VSS	AM46	RESI
	AM13	und C	AM47	
	1111-00		AM48	LPDI
	AM15	VSS	AM49	
4 010	AM16	de	AM5	
	AM17	VSS	AM50	LPDI
indefined un	AM18		AM51	
	AM19	UNCORE_VNN_S4	AM52	VSS
	AM2	VSS	AM53	
	AM20	18/11/2	AM54	VSS
	AM21	DDI_VGG_S0iX	AM55	3/77
			AM56	VSS
	AM23	VSS	AM57	
4 U	AM24	inde	AM58	VSS
	AM25	DDI_VGG_S0iX	AM59	
delli	AM26	infine	AM6	VSS
4 Ulli	AM27	DDI_VGG_S0iX	AM7	
ed undefined u	AM28		AM8	USB
	AM29	VSS	AM9	7075
	AM3	tined undefined unde		PWR

Ball #	Customer Name - LPDDR3]
	Customer Name - LPDDR3	define
AM30	U	4.08
AM31	VCC	96,111
AM32 AM33	VSS	
		-
AM34	PWR_RSVD_OBS	
AM35		
AM36	DDI_VGG_S0iX	
AM37		
AM38	DDI_VGG_S0iX	ndefil
AM39		27/3
AM4	USB3_RXP[2]	uge,,
AM40	DDI_VGG_S0iX	
AM41		-
AM42	VSS	
AM43		
AM44	VSS	
AM45	uno	
AM46	RESERVED	ındefi
AM47		130
AM48	LPDDR3_M1_DQ[19]_A	"uge,
AM49	0	0.
AM5	define	
AM50	LPDDR3_M1_DQ[23]_A	
AM51		
AM52	VSS	
AM53	Unc	
AM54	VSS	76
AM55	<u>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</u>	10
AM56	VSS	nuge
AM57		
AM58	VSS	
AM59	uno	
AM6	VSS	
AM7	461	
AM8	USB3_TXP[3]	
AM9	- Tine	
AN1	PWR_RSVD_V1P05	76
ed		4 nuo
	eine	
	USB3_TXP[3] PWR_RSVD_V1P05	
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ndefined undefine		1100	7		1
efine	Ball #	Customer Name - LPDDR3		Ball #	Cus
	AN10	- <u>J</u> eff!!		AN44	450
	AN11	USB3_TXP[0]		AN45	
	AN12		0	AN46	
	AN13			AN47	
ed u.	AN14	- und	_	AN48	
indefined undefined uni	AN15		1	AN49	VSS
, nuor	AN16	deili	-	AN5	USB3_
	AN17	- dull		AN50	
deill	AN18	41000		AN51	VSS
	AN19	96.		AN52	
	AN2	()77.		AN53	VSS
	AN20		100	AN54	
nu,	AN21			AN55	LPDDR
	AN22	d ull		AN56	
deili	AN23			AN57	LPDDR
undefined undefined un	AN24	"V96",		AN58	
	AN25	69 n.	_	AN59	VSS
	AN26	- define		AN6	
	AN27	Those		AN7	USB3_
	AN28)		AN8	
	AN29		117	AN9	USB3_
-du	AN3	VSS		AP10	USB3
	AN30	12eg 11,		AP10	
	AN31	Zefine		AP11	 VCC
ed u	AN32 AN33	Junge	1	AP12	VSS
defiling	ANSA	4/10.0	1	AP13	VSS O
unos	AN34	defil'	1	AP14	4.1
Jundefined undefined v	AN35 AN36	2-	1	AP15 AP16	VSS
	AN37			AP16 AP17	V55
	AN38		(eff	AP17	VSS
ed	AN39	4 AU		AP16 AP19	V55
d undefined undefined i	AN4	"!!/60		AP19	VSS
1 Unas	AN40	indelli		AP20	UNCO
	AN41	60 MI,		AP21	
detri	AN42	lefine	1	AP21	DDI_V
dulli	AN43	nuge.	1	AP23	
	TINTS.	9	J	71. 23	

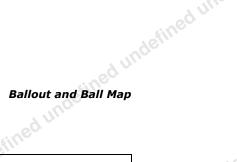
Ball #	Customer Name PDDP2
N44	Customer Name - LPDDR3
51	
N45 N46	
N47	
N48	
N49	VSS
AN5	USB3_RXP[0]
AN50	
N51	VSS
N52	
N53	VSS
N54	NDDD2 M1 DO[04] A
AN55 AN56	LPDDR3_M1_DQ[04]_A
N56 N57	
	LPDDR3_M1_DQ[00]_A
AN58	
AN59	VSS
AN6	
AN7	USB3_TXP[1]
AN8	
AN9	USB3_TXN[3]
AP1	
AP10	USB3_TXN[0]
\P11	
AP12	VSS
\P13	- Julie
\P14	VSS
NP15	<i>e</i> ¹
\P16	VSS
AP17	
NP18	VSS
P19	und
NP2	VSS
\P20	UNCORE_VNN_S4
\P21	dui,
\P22	DDI_VGG_S0iX
P23	3°
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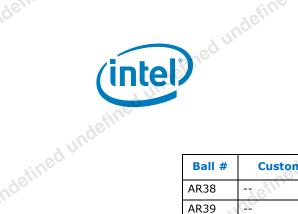
-98 undefined undefiner 123 undefined undefined



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		Jefine defined undefined	'nı,	
Ballout and Ba		defined b		
	Ball #	Customer Name - LPDDR3	Ball #	C
	AP24	DDI_VGG_S0iX	AP58	VSS
	AP25		AP59	
	AP26	DDI_VGG_S0iX	AP6	USB
	AP27	372	AP7	
4 uno	AP28	DDI_VGG_S0iX	AP8	VSS
	AP29		AP9	
deill	AP3	fine	AR1	PWR
dung	AP30	1/1/96,	AR10	
	AP31	DDI_VGG_S0iX	AR11	VSS
efined undefined unde	AP32		AR12	
	AP33	DDI_VGG_S0iX	AR13	
	AP34		AR14	
ed undefined und	AP35	DDI_VGG_S0iX	AR15	
4 nuc	AP36	DDI_VGG_SUIX	AR16	
	AP36	DDI_VGG_S0iX	AR16	
inder.				
ni.	AP38		AR18	
	AP39	DDI_VGG_S0iX	AR19	
	AP4	USB3_RXN[0]	AR2	e0
	AP40	(CO)	AR20	
	AP41	VSS	AR21	
	AP42		AR22	
4 nu	AP43	LPDDR3_M1_RCOMPPD	AR23	
undefined uni	AP44	4 111.	AR24	
dein	AP45	RESERVED	AR25	
	AP46	"uge"	AR26	
	AP47		AR27	
	AP48	LPDDR3_M1_DQ[18]_A	AR28	e
	AP49	7.00	AR29	
			AR3	RESI
	AP50	LPDDR3_M1_DQS[2]_P_A	AR30	
4 UI	AP51	,nde	AR31	
	AP52	LPDDR3_M1_DQ[16]_A	AR32	
gen	AP53	: ::	AR33	
Ull	AP54	VSS	AR34	
ed undefined ur	AP55	080	AR35	
	AP56	LPDDR3_M1_DM[0]_A	AR36	77.73
	AP57	tined undefined under		5

	16	•
Ball #	Customer Name - LPDDR3	defined und
AP58	VSS	od un.
AP59		stine
AP6	USB3_TXN[1]	196
AP7	200	
AP8	VSS	
AP9	Uni	
AR1	PWR_RSVD_V1P05	
AR10	2961	1
AR11	VSS	ndefined uni
AR12	<u> </u>	red to
AR13		defille
AR14		UC
AR15	sineo	
AR16	adeti	1
AR17	duin	1
AR18	stines	1
AR19	'''0'e,	
AR2	-69	, 117
AR20	(22)	indefined un
AR21		delli
AR22		
AR23	sine	
AR24	Inde	
AR25		
AR26	defin	
AR27	Und	
AR28	-Leo	90
AR29	7-	lefined u
AR3	RESERVED	"WO'C
AR30		
AR31	Lefille	
AR32	LING	
AR33	singo	
AR34	delli	
AR35	4 n	
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der	.4	define		4891	ueq.
intel	shed u	ndefine	led	unas	
ndefined undefine		adefine			
	Ball #	Customer Name - LPDDR3		Ball #	Cus
	AR38	-Ichine		AT18	Web.
	AR39	00		AT19	UNCO
	AR4			AT2	RESER
	AR40		Up	AT20	
od uli.	AR41	inoc		AT21	UNCO
fine	AR42			AT22	
Indefined undefined uni	AR43	Aefin		AT23	DDI_V
edu	AR44	June		AT24	
4efiline	AR45	sinec		AT25	VSS
	AR46	-dell.		AT26	
	AR47	77,		AT27	VSS
	AR48		6	AT28	
	AR49	LPDDR3_M1_DQ[17]_A		AT29	DDI_V
undefined undefined un	AR5	VSS		AT3	
48film	AR50	sined		AT30	
una	AR51	LPDDR3_M1_DQS[2]_N_A		AT31	
	AR52	dui		AT32	PWR_F
defill	AR53	LPDDR3_M1_DQ[20]_A		AT33	69
nue -	AR54	-nde		AT34	VSS
	AR55	LPDDR3_M1_DQ[03]_A		AT35	
	AR56		27.55	AT36	VSS
. \(\sigma\)	AR57	LPDDR3_M1_DQS[0]_P_A	Sur	AT37	
	AR58	30		AT38	DDI_V
defili	AR59	DDR_VDDQG_S4		AT39	
dung	AR6	inde		AT4	S_RCC
	AR7	VSS		AT40	DDI_V
"uge,	AR8	18/1/11		AT41	ne
undefined undefined u	AR9	RESERVED		AT42	DDRCI
	AT1	27.		AT43	
	AT10	PCIE_TXP[1]	132	AT44	VSS
A ¹	AT11		No.	AT45	
	AT12	VSS		AT46	VSS
	AT13	lefin		AT47	
ed u.	AT14	uno		AT48	LPDDR
18 fine	AT15	VSS		AT49	
d undefined undefined	AT16	delli		AT5	
	AT17	VSS		AT50	LPDDR

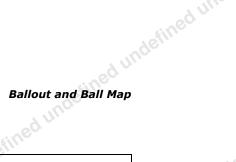
Ball #	Customer Name - LPDDR3	Indefined un
AT18	45°	ed un
AT19	UNCORE_VNN_S4	FILE
AT2	RESERVED	uge.
AT20		
AT21	UNCORE_VNN_S4	
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AT23	DDI_VGG_S0iX	
AT24	38	
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AT27	VSS	4efine
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AT29	DDI_VGG_S0iX	
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AT32	PWR_RSVD_OBS	
AT33	69 311	undefined v
AT34	VSS	
AT35		dein
AT36	VSS	Ulli
AT37	fine	
AT38	DDI_VGG_S0iX	
AT39	600	
AT4	S_RCOMP_P	
AT40	DDI_VGG_S0iX	
AT41		-8
AT42	DDRCH1_VDDQG_S4	
AT43		d undefined
AT44	VSS	9 0.
AT45	 V/CC	
AT46	VSS	
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AT48	LPDDR3_M1_DQ[22]_A	
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AT50	LPDDR3_M1_DQ[21]_A	4efine
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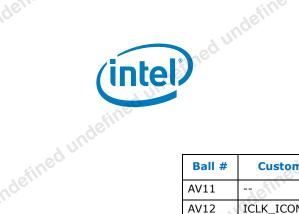
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# Customer Name - LPDDR3 VSS VSS LPDDR3_M1_DQS[0]_N_A VSS	AU31 AU32 AU33 AU34 AU35 AU36 AU37 AU38	
Customer Name - LPDDR3 VSS VSS VSS LPDDR3_M1_DQS[0]_N_A	AU31 AU32 AU33 AU34 AU35 AU36 AU37	DDI DDI DDI
Customer Name - LPDDR3 VSS VSS VSS LPDDR3_M1_DQS[0]_N_A	AU31 AU32 AU33 AU34 AU35 AU36 AU37	DDI DDI_ DDI_
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VSS VSS LPDDR3_M1_DQS[0]_N_A	AU34 AU35 AU36 AU37	 DDI
VSS LPDDR3_M1_DQS[0]_N_A	AU35 AU36 AU37	DDI_
VSS LPDDR3_M1_DQS[0]_N_A	AU36 AU37	
 LPDDR3_M1_DQS[0]_N_A 	AU37	
LPDDR3_M1_DQS[0]_N_A	-	1
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W	AU40	
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76.	-	VSS
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VSS		PCIE
de	AU50	
F_V1P05A_G3	AU51	VSS
	AU52	
	AU53	VSS
VSS	AU54	
Etimo	AU55	LPDE
UNCORE_VNN_S4	AU56	76 ₇₇
,o	AU57	LPDE
DDI_VGG_S0iX	AU58	
	AU59	DDR
DDI_VGG_S0iX	AU6	
Sine	AU7	VSS
DDI_VGG_S0iX	AU8	
	AU9	PCIE
S RCOMP N	-	27.07
100		PCIE
	F_V1P05A_G3 VSS UNCORE_VNN_S4 DDI_VGG_S0iX DDI_VGG_S0iX DDI_VGG_S0iX S_RCOMP_N	PCIE_V1P05_G3

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	Ball #	Customer Name - LPDDR3	defined unde
	AU31	DDI_VGG_S0iX	od uli
	AU32		fine
1 2	AU33	DDI_VGG_S0iX	96.
100	AU34		
	AU35	DDI_VGG_S0iX	
	AU36	Una	
	AU37	DDI_VGG_S0iX	
	AU38	deill	
	AU39	DDI_VGG_S0iX	ndefined und
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	AU40		4efille
60	AU41	DDRSFRCH1_VDDQG_S4	70.0
11/0	AU42	inec	
1	AU43	VSS	
	AU44	4011	
	AU45	VSS	
	AU46	'uge,	
	AU47	-69	, ur
	AU48	(22	ndefined un
	AU49	VSS	delli
ne	AU5	PCIE_RXP[1]	
	AU50	Stine	
	AU51	VSS	
	AU52		
	AU53	VSS	
	AU54	uno	
	AU55	LPDDR3_M1_DQ[01]_A	ed n
	AU56	77.	undefined u
	AU57	LPDDR3_M1_DQ[02]_A	
(10)	AU58	ed	
	AU59	DDR_VDDQG_S4	
	AU6	June	
	AU7	VSS	
	AU8	Ye,	
	AU9	PCIE_TXN[1]	
	AV1	Tine	
	AV10	PCIE_TXN[0]	deill
			June
Jefil		PCIE_TXN[1] PCIE_TXN[0] 301	
		Jude 301	
		301	
		defili	
		d Unit	
		OU.	





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	Ball #	Customer Name - LPDDR3		Ball #	Cus
uge,	AV11	-Jeffitt		AV45	USO.
	AV12	ICLK_ICOMP		AV46	
	AV13			AV47	
60	AV14		100	AV48	LPDDR
od uli.	AV15			AV49	
stines	AV16			AV5	
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edu	AV18	une		AV51	
46 film	AV19	sined		AV52	LPDDR
	AV2	VSS		AV53	100
	AV20	277		AV54	LPDDR
	AV21		6	AV55	
undefined undefined un	AV22	26		AV56	LPDDR
and U.	AV23	unc		AV57	
46 fills	AV24	sineo		AV58	VSS
, uno	AV25	den		AV59	
	AV26	dun		AV6	VSS
defil	AV27	fine		AV7	69
	AV28	-nde		AV8	VSS
	AV29	2.		AV9	
	AV3		245	AW1	PCIE_\
14.	AV30		8,11.	AW10	
	AV31	dun		AW11	VSS
defili	AV32	sinet		AW12	
4 un	AV33	"uger		AW13	
	AV34	'eq a.		AW14	
undefined undefined ut	AV35	Lefine		AW15	VSS
O.	AV36	-inos		AW16	6-1
	AV37	2.		AW17	UNCO
	AV38		413	AW18	
AV	AV39		76,,	AW19	UNCO
	AV4	PCIE_RXN[1]	1	AW2	
nden	AV40	18/11/8	1	AW20	
ed m.	AV41	unos	1	AW21	UNCO
efine	AV42		1	AW22	
d undefined undefined t	AV43	defill	1	AW23	DDI_V
	AV44	T OWN		AW24	90,

	Ballout and Ball Map	
	ined unac	
Ball #		
AV45	Customer Name - LPDDR3 LPDDR3 M1 DM[2] A	Un
	sine	
AV46	dein	
AV47	LEDDRA MI DMIALA	
AV48	LI DDRS_MI_DM[2]_A	
AV49	inden	
AV5	A V	
AV50	LPDDR3_M1_DM[3]_A	
AV51	LDDDD2 M1 DO[24] A	
AV52	LPDDR3_M1_DQ[24]_A	y ur
AV53	LDDDD3 M1 DOIGET A	
AV54	LPDDR3_M1_DQ[24]_A LPDDR3_M1_DQ[05]_A	
AV55	LDDDD3 M1 DOIGGI A	
AV56	LPDDR3_M1_DQ[06]_A	
AV57	VCC	
AV58	VSS	
AV59	VCC	
AV6	VSS	
AV/2	Wee	eg u
AV8	VSS	
AV4	100	
AW1		
AW10	VCC	
AW11	VSS	
AW12		
AW13	dell'	
AW14	Vec	
AW15	VSS UNCORE1_V1P05A_G3 UNCORE1_V1P05A_G3	
AW16	LINCORE1 VIDOEA C3	
AW17	UNCORE1_V1P05A_G3	
AW18	LINCODE1 VIDOEA C3	
AW19	UNCORE1_V1P05A_G3	
AW20	- ch ///.	
AW20 AW21	LINCODE VAIN CA	
	UNCORE_VNN_S4	
AW22	DDI VCC 50:X	_
AW23	DDI_VGG_S0iX	
AW24	- Agei	
	DDI_VGG_S0iX Datasheet	
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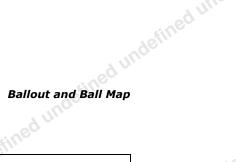
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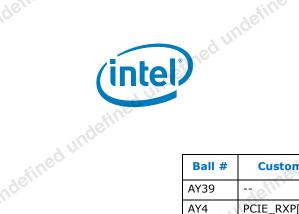


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Ba	II # Customer Name - LPDDR3		C
AW	DDI_VGG_SENSE	AW59	DDR
AW		AW6	
AW	DDI_VGG_S0iX	AW7	VSS
AW:		AW8	
AW:	29 DDI_VGG_S0iX	AW9	VSS
AW:		AY1	
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AW4			F/17:
AW4		AY21	,
/ ***		AY22	
AW-		AY23	
AW		AY24	
AW		AY25	
AW		AY26	
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AWA AWA AWA AWA AWA AWA AWA AWA AWA	7 D.	AY3	S/
the state of the s		AY30	
AW:		AY31	
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AW:	33 LPDDR3_M1_DQ[26]_A	AY33	
AW!	76,	AY34	
AW!	55 LPDDR3_M1_DQ[08]_A	AY35	
AW:	56	AY36	
AWS AWS AWS AWS AWS AWS AWS	57 LPDDR3_M1_DQ[07]_A	AY37	77
0.107	ined undefined i	AY38	96-

		efill	
	Ball #	Customer Name - LPDDR3	defined unde
	AW59	DDR_VDDQG_S4	od un.
	AW6		Sine
-6	AW7	VSS	Ige.
700	AW8		
	AW9	VSS	
	AY1	June	
	AY10	VSS	
	AY11	de	
	AY12	RESERVED	ndefined und
	AY13	12	red to
	AY14		defill.
eg	AY15	4 1	luc.
	AY16	sined	
	AY17	inder	
	AY18	od on	
	AY19	Gine	
	AY2	PCIE_RCOMP_P	
	AY20	-ed 2	undefined un
	AY21	(Z)	eineo.
	AY22		delli
SUL	AY23		
	AY24	sfine	
	AY25	Indie	
	AY26		
	AY27	- defill	
	AY28	- un	.4
	AY29	-ne ⁰	ed m
	AY3	77.	undefined
	AY30		INGE
110	AY31		
	AY32	define	
	AY33	unc	
	AY34	sine	
	AY35	ger	
	AY36	dun	
	AY37	TIME	ined.
	AY38	<u> </u>	defill
Jefil ^r		d undefined undefine	d une
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intel	hedin	idefine	ed	nuo	
ndefined undefine					
18 fine	Ball #	Customer Name - LPDDR3		Ball #	Cus
nac	AY39	-geim		B19	US.
	AY4	PCIE_RXP[0]		B2	VSS
	AY40		~e	B20	MCSI_
ind	AY41			B21	
	AY42	uno		B22	CORE_
define	AY43			B23	
4 Uno	AY44 AY45	"uqe _{ili} "		B24 B25	CORE_
	AY45 AY46	°69 ni.		B25	CORE
deir	AY47	16/1/0		B27	CORE_
ndefined undefined und	AY48	LPDDR3_M1_DQ[27]_A		B27	GPIO_
	AY49			B29	GF10_
	AY5		IU_{ϵ}	B3	
4 nu	AY50	LPDDR3_M1_DQS[3]_P_A		B30	
	AY51			B31	
inge.	AY52	LPDDR3_M1_DQ[25]_A		B32	VSS
undefined undefined un	AY53	10/03-		B33	
4efine	AY54	LPDDR3_M1_DQ[11]_A		B34	JTAG_
	AY55	-dejli		B35	EIN
	AY56	VSS		B36	CORE
	AY57		0	B37	
	AY58	LPDDR3_M1_DQ[09]_A	3/11	B38	GPIO_
ed v	AY59	4 1/100			C1_BP
defill	AY6	VSS		B39	
4 unc	AY7	index		B4	VSS
	AY8	ICLK_OSCIN		B40	DDR_\
undefined undefined ur	AY9	Lefin		B41	
	B1	-ino		B42	LPDDR
	B10	MIPI_V1P2A_G3		B43	
	B11		130	B44	VSS
40	B12	MDSI_A_CLKP	10.	B45	
Jundefined undefined u	B13	eq 0.		B46	LPDDR
"ude"	B14	GPION_V1P8A_G3		B47	
ed u.	B15	uno		B48 B49	VSS
define	B16	MCSI_2_DP[0]		B5	0
uno	B17	9e ₁₁ ,		B50	LPDDR
	B18	CORE_VCC0_S0iX		550	LUDDIN

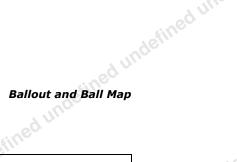
Ball #	Customer Name - LPDDR3	
319	(S)	ındefi
32	VSS	130
320	MCSI_1_DN[1]	
B21		
B22	CORE_VCC0_S0iX	
323	4 Unc	
324	CORE_VCC1_S0iX	
325	ade	
326	CORE_VCC1_S0iX	
327	1420	
328	GPIO_CAMERASB03	76
B29	2	unde
В3	sineo	
330	adem	
B31	od um	
332	VSS	
B33	11006	
334	JTAG_TMS	und
335	471	
336	CORE_V1P15_S0iX	
B37		1011.
B38	GPIO_N3/C0_BPM1_TX/ C1_BPM1_TX	
B39	ad ul.	
34	VSS	
340	DDR_V1P05A_G3	
341	eq.	
B42	LPDDR3_M0_DQ[17]_A	
343	P	d uni
344	VSS	9 ni.
345	101	
B46	LPDDR3_M0_DQS[2]_P_A	
347	ed	
B48	VSS	
B49	und	
B5	:: CO	
B50	LPDDR3_M0_DQS[3]_P_A Datasheet	

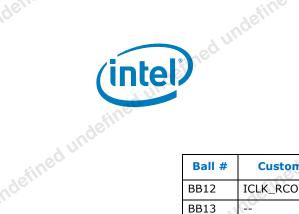
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ined L	Ball #	Customer Name - LPDDR3	Ball #	C
	B52	VSS	BA32	50
	B53		BA33	DDI
	B54	LPDDR3_M0_ODT_A	BA34	
46/	B55		BA35	VSS
4 Uno	B56	LPDDR3_M0_CS[1]_N	BA36	
eineo -	B57	20 11	BA37	VSS
adem.	B58	VSS	BA38	
-duli.	B59	'Iuge'	BA39	DDI
	B6	MDSI_C_CLKP	BA4	\
3°	B7	+0/1	BA40	150
 	B8 V	VSS	BA41	VSS
_	B9		BA42	
	BA1	VSS	BA43	VSS
	BA10	''''de''	BA44	
*inec	BA11	VSS	BA45	VSS
inder.	BA12	46110	BA46	
d ur.	BA13	Unac	BA47	
_	BA14	VSS	BA48	0
-	BA14 BA15	V55	BA49	LPDI
<u> </u>		F_V1P05A_G3	- 300	
	BA16 BA17	-	BA5 BA50	PCIE
200	2	F VIDOEA C3		
dun	BA18	F_V1P05A_G3	BA51	LPDI
Sine	BA19		BA52	
"uge,	BA20		BA53	VSS
O.	BA20	UNCORE_VNN_S4	BA54	
	BA21		BA55	LPDI
	BA22	DDI_VGG_S0iX	BA56	-76
<u> </u>	BA23	7.5	BA57	LPDI
	BA24	DDI_VSS_SENSE	BA58	
200	BA25		BA59	DDR
ad un	BA26	VSS	BA6	
istines	BA27	ed V	BA7	VSS
inge	BA28	VSS	BA8	
d	BA29	uno	BA9	ICLK
	BA3	PCIE_RCOMP_N	BB1	
ined undefined un	BA30	46 ₁₁₁	BB10	VSS
	BA31	DDI_VGG_S0iX	BB11	<u>o</u>

Ball #	Customer Name - LPDDR3	defined u
BA32	20	A U
BA33	DDI_VGG_S0iX	
BA34		
BA35	VSS	•
BA36		
BA37	VSS	
BA38		
BA39	DDI_VGG_S0iX	
BA4	07	
BA40	(C)	691
BA41	VSS	ndefined '
BA42		
BA43	VSS	
BA44	de _i ,,	
BA45	VSS	
BA46	sinec	
BA47	ingeli	
BA48	0	indefined
BA49	LPDDR3_M1_DQ[31]_A	"ned
BA5	PCIE_REFCLK[0]_P	geil.
BA50		71110
BA51	LPDDR3_M1_DQS[3]_N_A	
BA52	"1000"	
BA53	VSS	
BA54	defill	
BA55	LPDDR3_M1_DQS[1]_P_A	
BA56	::U60	
BA57	LPDDR3_M1_DQ[10]_A	undefine
BA58		Inde
BA59	DDR_VDDQG_S4	
BA6	defill	
BA7	VSS	
BA8	tineo	
BA9	ICLK_OSCOUT	
BB1	eq 1/1'	
BB10	VSS	***
BB11	<u> </u>	defill
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	d undefil.	





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	Ball #	Customer Name - LPDDR3		Ball #	Cus
deir	BB12	ICLK_RCOMP		BB46	VSS
	BB13	(22		BB47	
	BB14			BB48	LPDDR
	BB15	RTC_V3P3RTC_G5	100	BB49	
od uli.	BB16	Inde		BB5	
indefined undefined undefi	BB17	F_V1P8A_G3		BB50	LPDDR
Inde	BB18	defill		BB51	
rued to	BB19	VSS		BB52	VSS
defill	BB2	ICLK_VSFR_G3		BB53	60
U.C.	BB20	-96,		BB54	VSS
	BB21	UNCORE_VNN_S4		BB55	
	BB22		0	BB56	LPDDR
nin i	BB23	DDI_VGG_S0iX		BB57	
undefined undefined unf	BB24	June		BB58	VSS
defill	BB25	DDI_VGG_S0iX		BB59	
4 unc	BB26	yoder		BB6	VSS
	BB27	DDI_VGG_S0iX		BB7	
adeir	BB28	Sine		BB8	VSSA
	BB29	DDI_VGG_S0iX		BB9	-1-
	BB3	2		BC1	ICLK_\
	BB30		272	BC10	
A UIT	BB31		0.	BC11	VSS
	BB32	DDI_VGG_S0iX		BC12	
"uger.	BB33	Aline		BC13	
ed u	BB34	DDI_VGG_S0iX		BC14	
ie fine	BB35			BC15	
	BB36	DDI_VGG_S0iX		BC16	
undefined undefined un	BB37			BC17	C+
	BB38	DDI_VGG_S0iX		BC18	
<u>.</u>	BB39		efil	BC19	
ed u	BB4	PCIE_REFCLK[0]_N). T	BC2	
Jundefined undefined V	BB40	DDI_VGG_S0iX		BC20	
unat	BB41	defill		BC21	
	BB42	VSS		BC22	
defill	BB43			BC23	
une	BB44	VSS		BC24	76; !!U
	BB45	2 n,		BC25	GE

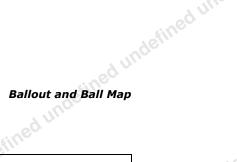
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Ball #	Customer Name - LPDDR3	ndefined und
BB46	VSS	od uli.
BB47		Hines
BB48	LPDDR3_M1_DQ[30]_A	uge.
BB49	201	
BB5	leftine	
BB50	LPDDR3_M1_DQ[28]_A	
BB51	::00	
BB52	VSS	
BB53	4 0/70	undefined und
BB54	VSS	ed ui.
BB55		Sine
BB56	LPDDR3_M1_DQS[1]_N_A	inge
BB57		
BB58	VSS	
BB59		
BB6	VSS	
BB7		
BB8	VSSA	
BB9	V33A 	ed u.
BC1	ICLK_VSFR_G3	iefine
BC10		undefinedur
BC11	VSS	
BC12	adelli	
BC13	2011	
BC14		
BC15	''Uge'	
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BC19		d undefined s
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BC22	48 [†] 1110	
BC23	Uno	
BC24		-81
BC25	9-6-111.	ed undefined b
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	Datasheet	
	#ineo	
	Datasheet	
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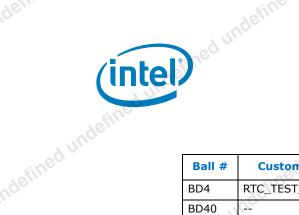
Jo undefined undefine L25
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	all Map	Jefined undefiner	y un.	
Ballout and B		defined		
	Ball #	Customer Name - LPDDR3	Ball	# C
	BC26	1 Effil	BC6	Silv Sign
	BC27	<u>-</u>	BC7	VSS
	BC28		BC8	
	BC29		BC9	RES
4 Une	ВС3	PCIE_REFCLK[1]_P	BD1	
	BC30	3d W	BD10) RES
adeili	BC31	Fine	BD11	
efined undefined unde	BC32	inde	BD12	
	BC33		BD13	
	BC34	+S/1/10	BD14	-00
	BC35	Y	BD15	- الم
	BC36		BD16	
ed undefined und	BC37		BD17	
4 UING	BC37	under	BD17	
	BC30	20 1111		
geili	BC39		BD19	
dulli	BC4	" " " " " " " " " " " " " " " " " "	BD2	PCIE
	BC40	eq 0.	BD20	
	BC41	fine	BD21	
	BC42	noc	BD22	
	DC 13	Ĭ	BD23	
	BC44		BD24	
7 110	BC45	"ge,	BD25	5
	BC46	d uli.	BD26	DDI_
	BC47		BD27	7
Ullie	BC48	"ugle"	BD28	GPIC
Jundefined un	BC49	VSS	BD29)
	BC5	VSS	BD3	:-ne
	BC50	UPOS	BD30	96
		VSS	BD31	GPIC
	BC52		BD32	2
الله لم	BC53	VSS	BD33	B DDI
	BC54	ad all	BD34	ļ
gein	BC55	LPDDR3_M1_DM[1]_A	BD35	5 DDI
dun	BC56	inge	BD36	5
	BC57	LPDDR3_M1_DQ[14]_A	BD37	d DDI
ined undefined u	BC58	- 46/1/10	BD38	
	BC59	vss vss	BB 36	

Ball #	Customer Name - LPDDR3	efined '
BC6	2-	69,
BC7	VSS	Silve
BC8	,,,,,	
BC9	RESERVED	
BD1	48/11/1	
BD10	RESERVED	
BD11	::000	
BD12	VSS	
BD13	7 1/1/2	
BD14	RTC_V3P3A_G5	69
BD15		Jefined
BD16	VSS	
BD17		
BD18	VSS	
BD19	4 11/06	
BD2	PCIE_REFCLK[1]_N	
BD20	UNCORE_VNN_S4	
BD21	0 31	
BD22	DDI_VGG_S0iX	ine
BD23		idefine
BD24	VSS	
BD25	fine	
BD26	DDI_VGG_S0iX	
BD27	20	
BD28	GPIOSE_V1P8A_G3	
BD29	Und	
BD3	-neo	
BD30	72.	ndefin
BD31	GPIOSE_V1P8A_G3	
BD32		
BD33	DDI_VGG_S0iX	
BD34	LING	
BD35	DDI_VGG_S0iX	
BD36	dell	
BD37	DDI_VGG_S0iX	
BD38	Tine	
BD39	DDI_VGG_S0iX	Aefil ¹
eg n.		nu _{Ore}
	DDI_VGG_S0iX DDI_VGG_S0iX 307	
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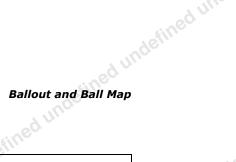
Aer		idefine		defil	red
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cined b	Ball #	Customer Name - LPDDR3		Ball #	Cus
dell'	3D4	RTC_TEST_N		BE2	-6g
E	3D40	090		BE20	
	3D41	VSS		BE21	
A CE	3D42			BE22	
, Uno E	3D43	VSS		BE23	
ineo F	3D44			BE24	
defill	3D45	VSS		BE25	
4 Une	3D 13 3D46	''''de'		BE26	
	3D40 3D47	eq 111.		BE27	3
ye,	3D47 3D48	LPDDR3 M1 OCAVREF		BE28	150
<u> </u>	3D48 3D49	LPDDR3_M1_OCAVREF		BE29	
_					
	3D5	LDDDD3 M1 ODOVDEE		BE30	PMC_F
	3D50	LPDDR3_M1_ODQVREF	10.	BE30	
ineo E	3D51	un		BE31	
defill	3D52	LPDDR3_M1_CA[08]		BE32	
d um	3D53	- 1096,		BE33	
eineu E	3D54	LPDDR3_M1_DQ[15]_A		BE34	
E	3D55	sing		BE35	ec
E	3D56	VSS		BE36	77
	3D57	Y		BE37	
E	3D58	LPDDR3_M1_DQ[12]		BE38	
UL E	3D59	2		BE39	
Edited	BD6	VSS		BE4	
defill.	3D7	sine		BE40	
4 Uno	BD8	RESERVED		BE41	
ined undefined ur	3D9	eq 01		BE42	
E	3E1	VSS		BE43	e
E	3E10	1006		BE44	6-
-	3E11	VSS		BE45	
F	3E12			BE46	
. 1	3E13		ei,	BE47	
F ASS	3E14	7 710,		BE48	
4efill	3E15	sineo		BE49	RESER
in in	3E16	"upe,,		BE5	RESER
sineo I	3E17	60 n//,		BE50	
4611,	3E18	lefine		BE51	RESER
- <u> [</u>	3E18 3E19	00		DEED	KESEK
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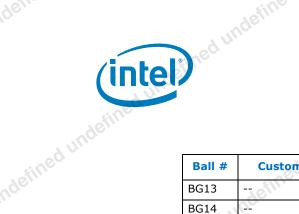
Ball #	Customer Name - LPDDR3	
2	(SO)	
3E20		
3E21		
BE22		O.
3E23	defili	
BE24	dunc	
BE25	sine	
BE26	nder	
BE27	9 71.	
3E28	it and the second secon	
BE29		
BE3	PMC_RSMRST_N	-6
BE30	cin	20
BE31	"ger,	
BE32	eq n,	
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BE36	47	
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BE4	unoc	
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BE48	11/10	_
BE49	RESERVED	_
BE5	RESERVED	_
BE50		
BE51	RESERVED	\dashv
BE52	9-	
ued un		
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	ned ur		Inug	
		adefine		
Ballout and Ba	ин гар	ed une		
inder		define		
	Ball #	Customer Name - LPDDR3	Ball	# C
	BE53	LPDDR3_M1_CA[09]	BF33	20
	BE54		BF34	VSS
	7 /	LPDDR3_M1_DQ[13]_A	BF35	
	BE56	«:\C	BF36	VSS
IIIO	BE57	VSS	BF37	
ined of	BE58		BF38	PWR
defill	BE59	VSS	BF39	
ndefined undefined undef	BE6	V55	BF4	RTC
	DEO DE7	70.		
Hezz.	BE7	VSS	BF40	VSS
	BE8		BF41	
		RESERVED	BF42	VSS
20	BF1		BF43	
ined undefined u	BF10	RTC_X2	BF44	VSS
	BF11	A Une	BF45	
defill	BF12	VSS	BF46	VSS
4 unc	BF13	"Uge,	BF47	
	BF14	du	BF48	LPDI
	BF15	VSS	BF49	0
	BF16	inde i	BF5	6/1 7-
	BF17	VSS	BF50	RESI
	BF18		BF51	
1100	BF19	VSS	BF52	VSS
i sed	BF2	PCIeCLK_V1P05A_G3	BF53	
defill	BF20	sine	BF54	LPDI
	BF21	VSS	BF55	
	BF22	39 m	BF56	LPDI
	BF23	SDIO_V3P3A_V1P8A_G3	BF57	0
	BF24	1000	BF58	VSS
d undefined uni	BF25	LPC_V3P3A_V1P8A_S4	BF59	
			BF6	VSS
10	BF27	VSS	BF7	
ined to	BF28	3 2/0	BF8	RESI
defill	BF29	GPIOSE_V1P8A_G3	BF9	
4 Unc	BF3		BG1	PCIe
	BF30	60 m//	BG10	
SII.	BF31	lefine	BG10	RTC
	BESS DI 31	VSS	PC12	
undefined undefined un	BF32	VSS	BG12	00
Datasheet	ndefine	vss undefined undefined unde	Hineo	
ad un.		Inde		
filler				
76,		ci (C		

	76,	
Ball #	Customer Name - LPDDR3	idefined l
BF33	5.0	60
BF34	VSS	Gine
BF35		
BF36	VSS	
BF37	defille	
BF38	PWR_RSVD_OBS	
BF39	singo	
BF4	RTC_RST_N	
BF40	VSS	ndefined
BF41	<u>~~~~</u>	
BF42	VSS	46/11/10
BF43		
BF44	VSS	
BF45	adefi	
BF46	VSS	
BF47	sine	
BF48	LPDDR3_M1_CA[02]	
BF49	0 111	
BF5	2	undefine
BF50	RESERVED	geill
BF51	2	III
BF52	VSS	
BF53	"Jdell	
BF54	LPDDR3_M1_CK_N_A	
BF55	ISTING	
BF56	LPDDR3_M1_CK_P_A	
BF57		
BF58	VSS	4efine
BF59		undefil.
BF6	VSS	U.
BF7	Lefting	
BF8	RESERVED	
BF9		
BG1	PCIeCLK_V1P05A_G3	
BG10	4 Unic	
BG11	RTC_EXTPAD	
BG12	<u> </u>	rifor
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ined C	RTC_EXTPAD 309	90.
	od undefil.	





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Stines	Ball #	Customer Name - LPDDR3		Ball #	Cus
uge.	BG13	-Zeff.		BG47	US.
	BG14	(C.		BG48	
	BG15		-0	BG49	VSS
	BG16		100	BG5	VSS
od ui.	BG17	, ₁₁₀₀		BG50	
istine	BG18	eq		BG51	LPDDR
Indefined undefined und	BG19	defill'		BG52	
	BG2	" nu		BG53	VSS
defill	BG20	sines		BG54	6
	BG21	-9e1.		BG55	LPDDR
	BG22	77.		BG56	
	BG23		6	BG57	LPDDR
	BG24			BG58	
ed u.	BG25	- unc		BG59	DDR_\
4efilne	BG26	sined		BG6	
undefined undefined un	BG27	gen		BG7	VSS
	BG28	duit		BG8	
defill	BG29	sine		BG9	RTC_X
nue	BG3	PMC_CORE_PWROK		BH1	6777
	BG30	2		BH10	PMC_P
	BG31		e5.10	BH11	
	BG32		Sim	BH12	VSS
ned t	BG33	4010		BH13	
defill	BG34	fines		BH14	MMC1_
4 unit	BG35	inde		BH15	
	BG36	60		BH16	SD3_R
undefined undefined u	BG37	Teling		BH17	06
n.	BG38	-nuos		BH18	SD3_D
	BG39	D		BH19	
	BG4		13	BH2	VSS
٨ ٨	BG40		76,,	BH20	VSS
	BG41	ed on		BH21	
aden.	BG42	Line		BH22	LPC_R
ed uli.	BG43	Inde		BH23	
	BG44			BH24	PMC_R
d undefined undefined l	BG45	define		BH25	
4 D).	BG46			BH26	UART2

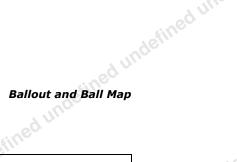
Ball #	Customer Name - LPDDR3
G47	CE CO
G48	
G49	VSS
3G5	VSS
3G50	telline
3G51	LPDDR3_M1_CA[06]
3G52	ined
3G53	VSS
3G54	A UP
3G55	LPDDR3_M1_CK_N_B
3G56	
3G57	LPDDR3_M1_CK_P_B
3G58	::08
3G59	DDR_VDDQG_S4
3G6	4 0/2
3G7	VSS
3G8	"/96/
3G9	RTC_X1
3H1	E P
3H10	PMC_PWRBTN_N
3H11	
3H12	VSS
3H13	ndell
3H14	MMC1_RCOMP
3H15	- Kine
3H16	SD3_RCOMP
3H17	280
3H18	SD3_D[2]
3H19	
3H2	VSS
3H20	VSS
H21	
3H22	LPC_RCOMP
3H23	18111
3H24	PMC_RSTBTN_N
3H25	
3H26	UART2_RTS_N
- 44	PMC_RSTBTN_N UART2_RTS_N
	Datashe
	Datasne

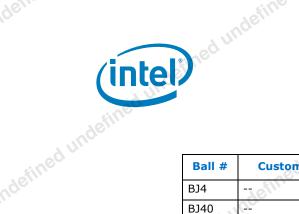
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	define adefined undefined	, un	
Ball # BH27 BH28	defined &		
Ball #	Customer Name - LPDDR3	Ball #	C
BH27		BH7	S.O.
BH28	UART2_DATAIN	BH8	VSS
BH29		BH9	
BH3		BJ1	ICLK
BH30	ndell	BJ10	
BH31	20 111.	BJ11	VSS
BH32	LPE_I2S0_CLK	BJ12	
ВН33	''''	ВЈ13	VSS
BH29 BH3 BH30 BH31 BH32 BH33 BH34 BH35 BH36	I2C6_CLK/NMI_N	BJ14	\
BH35	÷8111	BJ15	MMC
BH36	I2C2_DATA	BJ16	
BH37		BJ17	VSS
BH38	VSS	BJ18	
BH38 BH39 BH4 BH40 BH41 BH42 BH43	''''de'	BJ19	LPC
BH4	PMC_BATLOW_N	5515	SPI2
BH40	LPE_I2S2_FRM	ВЈ2	
BH41	LFL_1232_FRM	BJ20	
BH42	VSS	BJ21	GPIC
BH43	v33	6	ISH_
ВН44	LPDDR3_M1_DQ[09]_B	BJ22	
Billio	FPDDK3_M1_DQ[09]_B	BJ23	VSS
BH45		BJ24	
BH46	LPDDR3_M1_DM[1]_B	BJ25	FST_
BH47		ВJ26	
BH45 BH46 BH47 BH48 BH49 BH5 BH50 BH51 BH52	RESERVED	BJ27	VSS
BH49	4000	BJ28	
BH5	LDDDD2 M1 CA[01]	BJ29	
BH50	LPDDR3_M1_CA[01]	ВЈ3	PMC_
BH51	LVCC .	ВЈ30	LPE_
	VSS	ВЈ31	
BH53		ВЈ32	
BH54	LPDDR3_M1_CA[04]	ВЈ33	NFC_
BH55		ВЈ34	
BH56	VSS	ВЈ35	VSS
BH57	dunc	ВЈ36	
BH58	VSS	ВЈ37	UAR
BH59	6	ВЈ38	3/1/1
ВН6		BJ39	VSS
	PMC_SUS_STAT_N	ВЈ39	

Ball #	Customer Name - LPDDR3	idefined uni
BH7	50	4 Um
BH8	VSS	sinec.
BH9		961.
BJ1	ICLK_VSFR_G3	1
BJ10	isline	-
BJ11	VSS	-
BJ12	280	-
BJ13	VSS	-
BJ14	1 U/70	
BJ15	MMC1_CMD	od ui
BJ16		ndefined un
BJ17	VSS	uge
BJ18		
BJ19	LPC_FRAME_N/UARTO_DATAIN/	-
5313	SPI2_MISO	
BJ2	inco	-
BJ20	dett	
BJ21	GPIO_ALERT/ISH_GPIO[11]/ ISH_UART_DATAIN	indefined v
BJ22		fine
BJ23	VSS	"uge"
BJ24		0.1
BJ25	FST_SPI_D[2]	
BJ26	June	
BJ27	VSS	
BJ28	den	
BJ29	d n,	
ВЈЗ	PMC_SLP_S3_N	, sed
BJ30	LPE_I2S1_DATAIN	undefined,
BJ31		nu _o
BJ32	sine(
BJ33	NFC_I2C_CLK	
BJ34		
BJ35	VSS	
BJ36		
BJ37	UARTO_DATAIN	_
BJ38	ci ll	eineo
BJ39	VSS	age11.
efined	UARTO_DATAIN VSS 311	du
	d undefine	





el.	Indefine	_	indefil	red
Ball #	Indefined undefin	ed'		
Ball #	Customer Name - LPDDR3		Ball #	Cus
BJ4	eline		BK2	VSS
BJ40	1100		BK20	LPC_C
BJ41	VSS		nue	ISH_U
BJ42	0	Uen	BK21	
BJ43	LPDDR3_M1_DQ[14]_B		BK22	PMC_S
BJ44	- 20,7//		BK23	
BJ45	VSS		BK24	VSS
BJ42 BJ43 BJ44 BJ45 BJ46 BJ47 BJ48 BJ49	'''''		BK25	
BJ47	LPDDR3_M1_DQ[07]_B		BK26	FST_S
BJ48			BK27	" LEO
BJ49	LPDDR3_M1_CA[00]		BK28	UART2
BJ5	PMC_PLTRST_N		BK29	
	PMC_PLIRSI_N		BK3	
	76	_	BK30	
BJ51	LPDDR3_M1_CA[03]		BK31	
BJ52		-	BK32	LPE_I2
BJ53	RESERVED	-	BK33	
BJ54	ed u'	-	BK34	I2C5_0
BJ55	LPDDR3_M1_CA[05]	_	BK35	400
BJ56	-inde	-	BK36	SPI3_I
B337	LPDDR3_M1_CA[07]		BK37	 SP13_I
BJ58		0	<u> </u>	
BJ59	DDR_VDDQG_S4	9	BK38	LPE_I2
ВЈ6	duli		BK39	
BJ59 BJ6 BJ7 BJ8 BJ9 BK1 BK10 BK11	PMC_WAKE_N	-	BK4	PMC_A
ВЈ8	"Joer		BK40	LPE_I2
ВЈ9	PMC_SLP_S4_N		BK41	
BK1	sine		BK42	LPDDR
BK10	ISH_GPIO[6]/I2S4_DATAOUT		BK43	ē, iii
BK11	2		BK44	LPDDR
BK12	MMC1_D[3]	251	BK45	
BK13		eil	BK46	LPDDR
BK14	MMC1_D[1]		BK47	
BK15			BK48	VSS
BK15	SD3_D[0]		BK49	
BK17			BK5	
BK13 BK14 BK15 BK16 BK17 BK18 BK19	SPI1_MOSI		BK50	VSS
DK19	0		BK51	7-5////
BK19	<u>2</u> n,			LPDDR
312 undefined undefined	ned undefined un	defi	ineo.	<u>'</u>
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3K21 3K22 PMC_SUSPWRDNACK 3K23 3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33	Jefin ^e
3K21 3K22 PMC_SUSPWRDNACK 3K23 3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	<i>jefine</i>
3K21 3K22 PMC_SUSPWRDNACK 3K23 3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	Jefim
3K21 3K22 PMC_SUSPWRDNACK 3K23 3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K23 3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K24 VSS 3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K25 3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K26 FST_SPI_D[1] 3K27 3K28 UART2_DATAOUT 3K29 3K3 3K31 3K31 3K32 LPE_I2S0_FRM 3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K30 3K31 3K32	
3K30 3K31 3K32	
3K30 3K31 3K32	
3K30 3K31 3K31 3K32	120
3K30 3K31 3K31 3K32	
3K31 3K32	
BK32	
3K33 3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
3K34 I2C5_CLK 3K35 3K36 SPI3_MOSI 3K37 3K38 LPE_I2S2_CLK	
BK38 LPE_I2S2_CLK	
BK38 LPE_I2S2_CLK	
BK38 LPE_I2S2_CLK	
BK38 LPE_I2S2_CLK	ndef
	UC
31/30	
JK39	
BK4 PMC_ACPRESENT	
BK40 LPE_I2S2_DATAOUT	
3K41	
BK42 LPDDR3_M1_DQ[15]_B	
3K43	
BK44 LPDDR3_M1_DQ[10]_B	.60
3K42	
BK46 LPDDR3_M1_DQS[1]_P_B	
3K47	
BK48 VSS	
3K49	
BK5	
BK50 VSS	
BK51	
BK52 LPDDR3_M1_DQ[03]_B	ind
3K50 VSS 3K51 3K52 LPDDR3_M1_DQ[03]_B	O.
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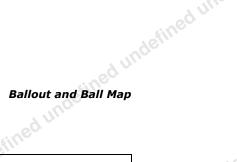
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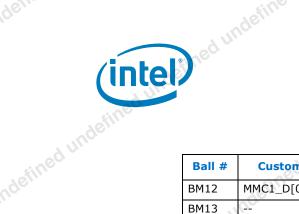


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	BK54	VSS		BL33	I2C6
	70.		<u>.</u>	BL34	
46	BK56	LPDDR3_M1_CKE[0]_A		BL35	I2C2
i Uno	BK57	20cm		BL36	
ineo .	BK58	VSS		BL37	UAR
aden.	BK59	Lefines		BL38	
ed un	BK6	VSS		BL39	LPE
Sine	BK7	000		BL4	\
indefined undefined undef	BK8	ISH_GPIO[9]/ISH_SPI_MISO/ I2S5_FS		BL40	VCC
	DICO		۷	BL41	VSS
undefined undefined unde	BL1	UNCORE_VNN_S4		BL42	
4 Uno	BL10	Joell		BL43 BL44	LPD[
eineo.	BL11	SD2_CLK		BL45	LPDI
adelli	BL12	Line		BL45	
ed ni.	BL13	VSS		BL47	LPDI
istine	BL14			BL48	0
uge	BL15	SD3_D[3]		BL49	LPDI
	BL16) <u>);</u>		BL5	VSS
	D	SD3_CLK		BL50	
601.	BL18	26	100	BL51	LPDI
ed un	BL19	SPI1_MISO		BL52	
1efine	BL2	aneo		BL53	LPDI
, unoc	BL20	dein		BL54	
Indefined undefined und	BL21	LPC_CLKRUN_N/ UART0_DATAOUT/SPI2_CLK		BL55	RESI
ings.	BL22	Jeffill		BL56	-ne
· ·	BL23	VSS		BL57	LPDI
	BL24			BL58	
	BL25	FST_SPI_D[3]		BL59	DDR
ad un	BL26	unde		BL6	
afinet	BL27	UART2_CTS_N		BL7	VSS
inde.	BL28	defill		BL8	
Jundefined undefined un	BL29	duno		BL9	ISH_ I2S5
defin	BL3	PMC_SLP_S0IX_N		BM1	
11/10	BL30	VSS		BM10 🔉	VSS
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SH_GPIO[8]/ISH_SPI_CS[0]_N/ 2S5_CLK	
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	PDDR3_M1_DQ[11]_B - PDDR3_M1_DQ[08]_B - PDDR3_M1_DQS[1]_N_B - PDDR3_M1_DQ[01]_B PDDR3_M1_DQ[00]_B - PDDR3_M1_DQ[02]_B - PDDR3_M1_CS[0]_N - PDDR3_M1_CS[0]_N - PDR_VDDQG_S4 - SS - SH_GPIO[8]/ISH_SPI_CS[0]_N/

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	Ball #	Customer Name - LPDDR3		Ball #	Cus
ell.	BM12	MMC1_D[0]		BM46	VSS
	BM13	(C)		BM47	
	BM14	MMC1_D[2]		BM48	LPDDR
	BM15	&	Ue,	BM49	
4 Uno	BM16	VSS		BM5	
	BM17	20 111		BM50	LPDDR
adem.	BM18	VSS		BM51	
Jefined undefined und	BM19	''''		BM52	LPDDR
	BM2	ISH_GPIO[7]/I2S4_DATAIN		BM53	A'
	BM20	LPC_CLKOUT[1]/ISH_GPIO[11]/		BM54	RESER
		ISH_UART_DATAIN		BM55	
	BM21			BM56	VSS
	BM22	VSS	1100	BM57	
ned undefined unf	BM23			BM58	LPDDR
	BM24	LPC_SERIRQ/SPI2_CS[0]_N		BM59	
age,	BM25	(6)		BM6	PMC S
od uli	BM26	VSS		BM7	
	BM27				ISH_IZ
	BM28	VSS		BM8	12S5_I
	BM29	JU.		BM9	
	BM3			BN1	UNCOF
	BM30		2112	BN10	
4 UI	BM31		0.	BN11	SD2_C
	BM32	LPE_I2S0_DATAOUT		BN12	
inde.	BM33	48110		BN13	VSS
g or	BM34	VSS		BN14	
	BM35			BN15	MMC1_
d undefined un	BM36	VSS		BN16	
	BM37			BN17	VSS
	BM38	SPI3_CS[0]_N		BN18	
	BM39		all	BN19	SPI1_0
~9 V	BM4	ISH_GPIO[3]/I2S3_DATAIN		BN2	
Sine	BM40	VSS		BN20	
inde	BM41			BN21	VSS
ed	BM42	LPDDR3_M1_DQ[13]_B		BN22	
	BM43	LPDDR3_M1_DQ[13]_B		BN23	VSS
ined undefined u	BM44	76/			V55
314 undefined		VSS		BN24	
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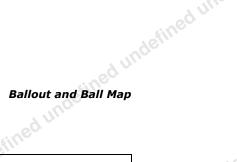
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BM46	Customer Name - LPDDR3 VSS LPDDR3_M1_DQ[06]_B
BM47	(1)
BM48	LPDDR3_M1_DQ[06]_B
BM49	20
BM5	46/11/20
BM50	LPDDR3_M1_DQS[0]_P_B
BM51	ined
BM52	LPDDR3_M1_DQ[04]_B
BM53	RESERVED VSS
BM54	RESERVED
BM55	Left
BM56	VSS
BM57	sine
BM58	LPDDR3_M1_CKE[0]_B
BM59	d'ul.
ВМ6	PMC_SUSCLK[0]
BM7	unde
BM8	ISH_I2C1_DATA/ISH_SPI_MOSI/ I2S5_DATAOUT UNCORE_VNN_S4
BM9	76
BN1	UNCORE_VNN_S4
BN10	::\(\gamma^2\)
BN11	SD2_CMD
BN12	dun
BN13	VSS
BN14	11000
BN15	MMC1_CLK VSS SPI1_CLK
BN16	S. J. L.
BN17	VSS
BN18	duli
BN19	SPI1_CLK
BN2	
BN20	
BN21	VSS
BN22	unc
BN23	VSS
BN24	7.5//
BN25	FST_SPI_D[0]
BNZ3	VSS FST_SPI_D[0]
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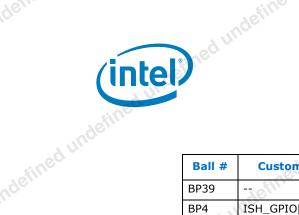
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Inc	Ball #	Customer Name - LPDDR3	Ball #	, C
	BN26	18 July 1	BN6	57.
	BN27	VSS	BN7	VSS
ġ.	BN28		BN8	
ade)	BN29		BN9	RES
fined undefined undef	BN3	ISH_I2C1_CLK/ISH_SPI_CLK/ I2S5_DATAIN	BP1	
efine	BN30	VSS VSS	BP10	VSS
Inoc	BN31		BP11	
ed	BN32	dunc	BP12	SD2
11.			BP13	6
	BN33	NFC_I2C_DATA	BP14	MMC
	BN34		BP15	
	BN35	VSS	BP16	SD3
nde	BN36		BP17	
ed u.	BN37	SPI3_MISO	BP18	VSS
18 fine	BN38		BP19	
Inor	BN39	VSS	BP2	UNC
undefined unde	BN4	dune	BP20	LPC_
	BN40	VCC	BD21	ISH_
	BN41	VSS	BP21	
	BN42	¥	BP22	USB
_	BN43	LPDDR3_M1_DQ[12]_B	BP23	 FCT
, uno	BN44		BP24	FST_
ined 5	BN45	VSS	BP25	
defili	BN46		BP26	VSS
Un	BN47	LPDDR3_M1_DM[0]_B	BP27	
	BN48	d ''''	BP28	LPE_
Indefined und	BN49	LPDDR3_M1_DQ[05]_B	BP29	
	BN5	ISH_GPIO[1]/I2S3_FS	BP3	77
		5.	BP30	
	BN51	LPDDR3_M1_DQS[0]_N_B	BP31	
יוט י	BN52	269	BP32	VSS
eineo.	BN53	VSS	BP33	
odein	BN54		BP34	I2C4 DDI
Ulli	BN55	RESERVED	BDSE	
	BN56	697	BP35	
ed undefined un	BN57	RESERVED	BP36	I2C1
	BN58	Tho	BP37	
	BN59	DDR_VDDQG_S4	BP38	GPIC

Ball #	Customer Name - LPDDR3	
BN6	20	idefined u
BN7	VSS	Gines
BN8		IQ.
BN9	RESERVED	
BP1	defin	
BP10	VSS	
BP11	singo	
BP12	SD2_D[3]_CD_N	
BP13	-d un	ndefined
BP14	MMC1_D[6]	red.
BP15		defills
BP16	SD3_D[1]	Ur.
BP17	singo	
BP18	VSS	
BP19	0 01	
BP2	UNCORE_VNN_S4	
BP20	LPC_AD[2]/ISH_GPIO[14]/ ISH_I2C0_DATA	undefined
BP21	(Contraction of the Contraction	· red
BP22	USB_OC[0]_N	defill
BP23		nu.
BP24	FST_SPI_CLK	
BP25	adeli	
BP26	VSS	
BP27	Sine	
BP28	LPE_I2S1_DATAOUT	
BP29	ed	
BP3	77	undefine
BP30		"Uger.
BP31		011
BP32	VSS	
BP33	""	
BP34	I2C4_CLK/DDI0_DDC_CLK/ DDI2_DDC_CLK/MDSI_DDC_CLK	
BP35	"uggs,	
BP36	I2C1_CLK	
BP37		0113
BP38	GPIO_SW93	"dell"
heo	I2C1_CLK GPIO_SW93	d ui.
	d undefir.	





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Ball # BP39 BP4	ndefined undefin			
Ball #	Customer Name - LPDDR3		Ball #	Cus
BP39	Chine		BR19	LPC_A
BP4	ISH_GPIO[5]/I2S4_FS		46 _L	ISH_U
BP40	VSS		BR2	
BP41			BR20	
BP42	LPDDR3_M1_DQ[28]_B		BR21	LPC_A ISH_I2
BP43	ed 3		BR22	
BP44	LPDDR3_M1_DQ[31]_B		BR23	FST_S
BP41 BP42 BP43 BP44 BP45 BP46 BP47	Ino		BR24	
BP46	LPDDR3_M1_DM[3]_B		BR25	UART1
BP47	10 h		BR26	UART1
BP48	VSS		BR27	UART1
BP49			BR28	UARTI
BP5				
BP5 BP50 BP51 BP52 BP53 BP54 BP55	LPDDR3_M1_DQ[19]_B		BR29	
BP51			BR3	ISH_G
BP52	LPDDR3_M1_DQ[16]_B		BR30	LPE_I2
BP53	7 71/03=-		BR31	
BP54	RESERVED		BR32	
BP55			BR33	I2C5_I
BP56	RESERVED		BR34	7004
BP57			BR35	I2C1_I
BP58	VSS	717	BR36	
BP59			BR37	ISH_G
BP59	VSS		BR38	
BP7	V55		BR39	PCIE_0
BP0			BR4	
BP58 BP59 BP6 BP7 BP8 BP9 BR1	PMC_PLT_CLK[0]/ISH_GPIO[10]/ ISH_UART_DATAOUT		BR40	 VSS
BP9	inde		BR41	VSS
BR1	VSS		BR42	
BR10			BR43	LPDDR
BR11	SD2_D[1]	eil)	BR44	
BR12	4011		BR45	LPDDR
BR13	MMC1_D[4]		BR46	
BR14	inder		BR47	LPDDR
BR15	SD3_CMD		BR48	
BR16	Gine		BR49	LPDDR
BR17	SPI1_CS[1]_N		BR5	VSS
BR18			BR50	<u> </u>
	4 13	'96	BR50	(67
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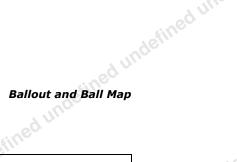
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Ball #	Customer Name - LPDDR3	
BR19	LPC_AD[1]/ISH_GPIO[13]/ ISH_UART_RTS_N	Indefined un
BR2		
BR20		
BR21	LPC_AD[3]/ISH_GPIO[15]/ ISH_I2C0_CLK/SPI2_MOSI	
BR22	eq v	
BR23	FST_SPI_CS[1]_N	
BR24	- 11000	
BR25	UART1_RTS_N	الللح
BR26	177	
BR27	UART1_CTS_N	undefined ur
BR28	oò	O.
BR29		
BR3	ISH_GPIO[0]/I2S3_CLK	
BR30	LPE_I2S1_CLK	
BR31	delin	
BR32	' nu	
BR33	I2C5_DATA	Jundefined L
BR34	27.	Filher
BR35	I2C1_DATA	"uge"
BR36		y or.
BR37	ISH_GPIO[12]/ISH_UART_CTS_N	
BR38	IInoc	
BR39	PCIE_CLKREQ[0]_N	
BR4	10/11/1	
BR40	June	
BR41	VSS	d
BR42	<u> </u>	istine
BR43	LPDDR3_M1_DQ[29]_B	Inde
BR44		d undefined
BR45	LPDDR3_M1_DQ[27]_B	
BR46	d und	
BR47	LPDDR3_M1_DQ[23]_B	
BR48	"ge,	
BR49	LPDDR3_M1_DM[2]_B	
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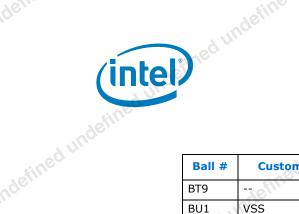
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BR51	LPDDR3 M1 DO[18] B	BT30	Sq
		611	
7 //	VSS		I2C4
BR54	6	O.	DDI2
BR55	RESERVED		MDS
BR56	411		
BR57			VSS
BD58	96.		
BP 50	A 0.	BT36	I2C0
BP6		BT37	<u>E0</u>
DRU DD7	AO	BT38	VSS
	ISH_I2C0_DATA/SPI2_MISO	BT39	
BR8		BT4	ISH_
BR9	PMC PLT CLK[1]/ISH GPIO[11]/	BT40	SD3
	ISH_UART_DATAIN/SPI2_CS[1]_N	BT41	
BT1	Fine	BT42	VSS
BT10	SD2_D[0]	BT43	
BT11	80	BT44	LPDI
BT12	VSS	BT45	480
BT13	(Co.	BT46	VSS
BT14	MMC1_D[7]	BT47	
BT15		BT48	LPDI
BT16	VSS	BT49	
BT17	3d m	BT5	
BT18	SPI1_CS[0]_N	BT50	VSS
BT19	1000	BT51	
BT2	ISH_GPIO[2]/I2S3_DATAOUT	BT52	LPD
BT20	VSS	BT53	:100
BT21	uno.	BT54	VSS
BT22	SD3_1P8_EN	BT55	
BT23		BT56	VSS
BT24	VSS	BT57	
BT25	260	BT58	LPDI
BT26	UART1_DATAIN/UART0 DATAIN	BT59	
BT27	' ////	BT6	PMC
BT28	VSS		ISH_
BT29	96.	BT7	7777
BT3	undefined undefined undef	BT8	VSS
	Ball # BR51 BR52 BR53 BR54 BR55 BR56 BR57 BR58 BR59 BR6 BR7 BR8 BR9 BT1 BT10 BT11 BT12 BT13 BT14 BT15 BT16 BT17 BT18 BT19 BT2 BT20 BT21 BT20 BT21 BT22 BT23 BT24 BT25 BT26 BT27 BT28	Ball # Customer Name - LPDDR3 BR51 LPDDR3_M1_DQ[18]_B BR52 BR53 VSS BR54 BR55 RESERVED BR56 BR57 RESERVED BR58 BR7 PMC_PLT_CLK[4]/ISH_GPIO[14]/ ISH_IZCO_DATA/SPI2_MISO BR8 BR9 PMC_PLT_CLK[1]/ISH_GPIO[11]/ ISH_UART_DATAIN/SPI2_CS[1]_N BT1 BT10 SD2_D[0] BT11 BT12 VSS BT13 BT14 MMC1_D[7] BT15 BT16 VSS BT17 BT18 SPI1_CS[0]_N BT19 BT2 ISH_GPIO[2]/I2S3_DATAOUT BT20 VSS BT21 BT22 SD3_1P8_EN BT23 BT24 VSS BT25 <t< th=""><th> Ball # Customer Name - LPDDR3 </th></t<>	Ball # Customer Name - LPDDR3

Ball #	Customer Name - LPDDR3	-
BT30	50	od ui
BT31		Sine
BT32	I2C4_DATA/DDI2_DDC_DATA/ DDI2_DDC_DATA/ MDSI_DDC_DATA	defined un
BT33	10de,	
BT34	VSS	
BT35	stine	
BT36	I2C0_CLK	
BT37	<u></u>	۵ ر
BT38	VSS	eineo.
BT39		ndefined v
BT4	ISH_GPIO[4]/I2S4_CLK	
BT40	SD3_WP	
BT41	"10%,	1
BT42	VSS	1
BT43	leffre	
BT44	LPDDR3_M1_DQ[26]_B	1
BT45	450	-9,
BT46	VSS	indefined.
BT47		"uge"
BT48	LPDDR3_M1_DQ[21]_B	0.1
BT49	defin	
BT5	i une	
BT50	VSS	
BT51	dell	
BT52	LPDDR3_M1_DQ[20]_B	
BT53	(TO)	. sed
BT54	VSS	defill
BT55		undefined
BT56	VSS	
BT57	dell'	
BT58	LPDDR3_M1_CKE[1]_A	
BT59	sine	
ВТ6	PMC_PLT_CLK[5]/ISH_GPIO[15]/ ISH_I2CO_CLK/SPI2_MOSI	
BT7	FINE	e
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ined with	ISH_I2CO_CLK/SPI2_MOSI VSS	dunc
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intel [®]		idefined undefined undefine	6	n,	
singo I	Ball #	Customer Name - LPDDR3		Ball #	Cus
B	T9	61112	•	BU41	VSS
В	U1	VSS		BU42	
В	U10		- 1	BU43	LPDDR
	U11	SD2_D[2]	16,	BU44	
.,00	U12	10		BU45	LPDDR
B	U13	MMC1_RCLK/MMC1_RESET_N		BU46	
B	U14		•	BU47	LPDDR
R	U15	MMC1_D[5]		BU48	
ine.	U16			BU49	LPDDR
B	U17	SD3_CD_N	ŀ	BU5	PWM[1
	U18			202	ISH_U
	U19	LPC_AD[0]/ISH_GPIO[12]/	•	BU50	
	019	ISH_UART_CTS_N	UG	BU51	LPDDR
B B B B B	U2	10°		BU52	
B	U20	20 111.	-	BU53	LPDDR
B	U21	USB_OC[1]_N		BU54	
A UITTO	U22	100		BU55	LPDDR
B	U23	SD3_PWREN_N	•	BU56	\
В	U24	16/11		BU57	LPDDR
В	U25	FST_SPI_CS[0]_N		BU58	
R	U26			BU59	VSS
В	U27	UART1_DATAOUT/	17	BU6	V33
111/10	027	UARTO_DATAOUT			PMC P
B	U28	- Gd III.		BU7	ISH_U
1 3/1/1	U29	- sine	•	BU8	
В	U3	VSS	-	BU9	PMC_P
В	U30	LPE_I2S0_DATAIN			ISH_U
В	U31	46/170		BV1	-ine
B	U32	-41700		BV10	DDI_V
B	U33	I2C3_DATA		BV11	
-	U34		41	BV12	VSS
A VIR	U35	I2C0_DATA	2,	BV13	
sineo B	U36		ŀ	BV14	DDI_V
ndel.	U37	GPIO_SW78		BV15	
9 111.	U38		ŀ	BV16	VSS
D	U39	PCIE_CLKREQ[1]_N	•	BV17	
	U39 U4	PCIE_CLKREQ[1]_N		BV18	LPC_V
В		.00	ŀ	BV19	Gerri.
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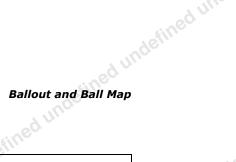
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BU41	VSS	ed ui.
BU42		Sine
BU43	LPDDR3_M1_DQ[25]_B	inde
BU44	cd	· ·
BU45	LPDDR3_M1_DQ[24]_B	
BU46	I UNG	
BU47	LPDDR3_M1_DQS[3]_N_B	
BU48	dell	
BU49	LPDDR3_M1_DQ[22]_B	201
BU5	PWM[1]/ISH_GPIO[10]/ ISH_UART_DATAOUT	undefined un
BU50		Inde
BU51	LPDDR3_M1_DQS[2]_N_B	~
BU52	Jeffin	
BU53	LPDDR3_M1_DQ[17]_B	
BU54	ineo	
BU55	LPDDR3_M1_ODT_A	
BU56	4 Une	
BU57	LPDDR3_M1_CKE[1]_B	ed u
BU58	9	18fine
BU59	VSS	undefined ur
BU6		3
BU7	PMC_PLT_CLK[2]/ISH_GPI0[12]/ ISH_UART_CTS_N/SPI2_CS[0]_N	
BU8	ineo	
BU9	PMC_PLT_CLK[3]/ISH_GPIO[13]/ ISH_UART_RTS_N/SPI2_CLK	
BV1	-ineo	d undefined v
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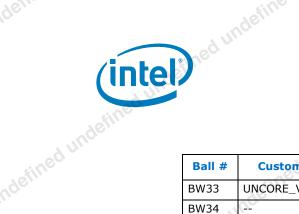
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Ball #	Customer Name - LPDDR3	Ball #	C
BV2	VSS	BV53	50
BV20	VSS	BV54	LPDI
BV21		BV55	
BV22	GPIOSE_V1P8A_G3	BV56	LPDI
BV23	:,06%	BV57	
BV24	FST_SPI_CS[2]_N	BV58	VSS
BV25		BV59	
BV26	GPIOSE V1P8A G3	BV6	VSS
BV21 BV22 BV23 BV24 BV25 BV26 BV27 BV28 BV29		BV7	
BV28	LPE_I2S1_FRM	BV8	VSS
BV29		BV9	
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DV3			
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BV31		BW11	DDI_
BV32	UNCORE_V1P8A_G3	BW12	
BV33		BW13	DDI_
BV34	I2C3_CLK	BW14	
BV35	stills	BW15	SDIC
BV36	DDI_V1P15_S0iX	BW16	12-
BV37	Υ	BW17	LPC_
BV38	MMC1_RESET_N /SPI3_CS[1]_N	BW18	
BV39	76,	BW19	VSS
BV38 BV39 BV4 BV40 BV41 BV42 BV43 BV44 BV45	PWM[0]	BW2	
BV40	DDR_V1P05A_G3	BW20	
BV41	index	BW21	GPIC
BV42	LPDDR3_M1_DQ[30]_B	BW22	
BV43	Sing	BW23	GPIC
BV44	VSS	BW24	2
BV45		BW25	GPIC
	LPDDR3_M1_DQS[3]_P_B	BW26	
BV47		BW27	GPIC
BV48	VSS	BW28	
BV49	filled	BW29	
BV5	:\del.	BW3	VSS
BV50	LPDDR3_M1_DQS[2]_P_B	BW30	VSS
BV51		BW31	733
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BV53 BV54		- 2/6/11	1
BV56	Ball #	Customer Name - LPDDR3	
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BV56	BV55		100
BV58 VSS BV59 BV6 VSS BV7 BV8 VSS BV9 BW1 BW10 BW11 DDI_VGG_SOiX BW12 BW13 DDI_VGG_SOiX BW14 BW15 SDIO_V3P3A_V1P8A_G3 BW16 BW17 LPC_V3P3A_V1P8A_S4 BW18 BW19 VSS BW2 BW20 BW20 BW21 GPIOSE_V1P8A_G3 BW22 BW23 GPIOSE_V1P8A_G3 BW24 BW25 GPIOSE_V1P8A_G3 BW26 BW27 GPIOSE_V1P8A_G3 BW28 BW29 BW29 BW29 BW29 BW29 BW29 BW3 VSS	BV56	LPDDR3_M1_CS[1]_N	
BV59 BV6 VSS BV7 BV8 VSS BV9 BW1 BW10 BW11 DDI_VGG_SOiX BW12 BW13 DDI_VGG_SOiX BW14 BW15 SDIO_V3P3A_V1P8A_G3 BW16 BW17 LPC_V3P3A_V1P8A_S4 BW18 BW19 VSS BW2 BW20 BW21 GPIOSE_V1P8A_G3 BW22 BW23 GPIOSE_V1P8A_G3 BW24 BW25 GPIOSE_V1P8A_G3 BW26 BW27 GPIOSE_V1P8A_G3 BW28 BW29 BW29 BW29 BW29 BW29 BW29 BW3 VSS	BV57	defill	
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BW25	BW22	June	
BW25	BW23	GPIOSE_V1P8A_G3	-6
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	Ball #	Customer Name - LPDDR3		Ball #	Cus
der.	BW33	UNCORE_V1P8A_G3		C13	RESER
	BW34	100		C14	
	BW35	DDI_V1P15_S0iX		C15	MCSI_
	BW36		Ue	C16	
40	BW37	DDI_V1P15_S0iX		C17	MCSI_
indefined undefined v	BW38	ed tr		C18	
"uge,	BW39	VSS		C19	MCSI_
ed u.	BW4	June		C2	
4efine	BW40	cineo		C20	6
	BW41	DDR_V1P05A_G3		C21	DDI2_
	BW42	777		C22	
	BW43	DDR_V1P05A_G3		C23	CORE_
	BW44			C24	
ndefined undefined	BW45	VSS		C25	VSS
ie fine	BW46	sineo		C26	
Inoc	BW47	VSS		C27	GPIO_
	BW48	4000		C28	
Still.	BW49	VSS		C29	69
	BW5	VSS		C3	DDI1_
	BW50	5,		C30	GPIO_
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	BW7	VSS	70.	C4	
	BW8	ed		C40	
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ed u.	C1	VSS		C42	
lefine	C10	:: 00		C43	LPDDR
Nor	C11	MDSI_A_CLKN		C44	
	C12	7-1110		C45	LPDDR
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C14		eineo.
C15	MCSI_2_DN[0]	age,
C16		21.
C17	MCSI 1 CLKP	
C18	'''''	
C19	MCSI_1_DP[1]	
C2	40	
C20	4 Unit	
C21	DDI2 HPD	ed un
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C23	CORE_VCC1_S0iX	undefined un
C24		
C25	VSS	1
C26	A Unit	1
C27	GPIO_CAMERASB07	
C28	ngeli	
C29	- 9 711	, ui
C3	DDI1_TXP[3]	ined.
C30	GPIO_CAMERASB04	defill
C31		undefined ur
C32		
C33	SVID_ALERT_N	
C34	- 80 0	
C35	GPIO_SUS5/PMC_SUSCLK[1]	
C36	Illion	
C37	GPIO_SUS3/JTAG2_TDI	90
C38	e ^{tt}	Finec
C39	ISH_GPIO[13]/C0_BPM2_TX/	d undefined u
ver.	C1_BPM2_TX	90.
C4	76//	
C40		
C41	VSS	
C42		
C43	LPDDR3_M0_DQ[22]_A	
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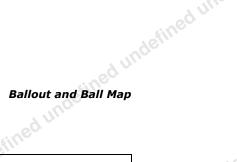
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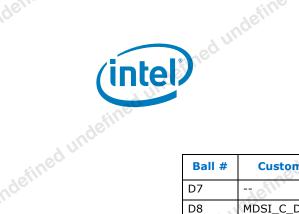


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ige,	C47	LPDDR3_M0_DQS[2]_N_A		D27	57.
	C48	~-		D28	VSS
es.	C49	LPDDR3_M0_DQ[25]_A	-9.	D29	
dei	C5	MDSI_C_CLKN		D3	
4 um	C50			D30	
Fineca	C51	LPDDR3_M0_DQS[3]_N_A		D31	
ndefined undefined undef	C52	16/11/2		D32	SVID
ed n.	C53	LPDDR3_M0_DQ[30]_A		D33	
istine	C54	60		D34	VSS
nde	C55	LPDDR3_M0_ODT_B		D35	16
	C56 \			D36	GPIC
		LPDDR3_M0_CKE[1]_A	a d	D37	
undefined undefined unde	C58			D38	VSS
ed uli.	C59	VSS		D39	
fine	C6			D4	DDI
inde	C7	MDSI_C_DP[2]		D40	GPIC
edu	C8	4 Unio			C1_E
16 fine	C9	MDSI_C_DP[0]		D41	6
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	D10	MDSI_A_DN[1]		D43	
	D11			D44	LPDI
, nd	D12	RESERVED	1111	D45	
ed ui	D13	11170		D46	VSS
efine	D14	RESERVED		D47	
, unoc	D15	adelli		D48	LPDI
ined -	D16	MCSI_1_CLKN		D49	
defill	D17			D5	
nuc	D18	MCSI_1_DN[2]		D50	VSS
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	D2	DDI1_TXP[2]		D52	LPDI
10	D20	VSS		D53	
ned o	D21			D54	VSS
defill	D22	VSS		D55	
4 Unc	D23	100611		D56	VSS
eineo	D23	CORE_VCC1_S0iX		D57	
Jundefined undefined un	D24			D58	LPDI
, UII	D25	GPIO_CAMERASB10		D59	97,
	D20	GITO_CAPIENASDIO		D6	MDS

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D27	20	ad u
D28	VSS	Gine
D29		
D3		
D30	defin	
D31	une	
D32	SVID_DATA	
D33	961	
D34	VSS	
D35	2	ed.
D36	GPIO_SUS6/PMC_SUSCLK[2]	ndefined '
D37	3	
D38	VSS	
D39	defin	
D4	DDI1_TXN[3]	
D40	GPIO_N0/C0_BPM0_TX/ C1_BPM0_TX	
D41	4 1/1/2	Indefined
D42	VSS	
D43		46,111
D44	LPDDR3_M0_DQ[21]_A	IUO
D45	"ineo	
D46	VSS	
D47	d 01	
D48	LPDDR3_M0_DQ[26]_A	
D49	11006	
D5	ed	
D50	VSS	
D51		oge,,
D52	LPDDR3_M0_DQ[27]_A	undefine
D53	Gine	
D54	VSS	
D55		
D56	VSS	
D57	Ino	
D58	LPDDR3_M0_CKE[1]_B	
D59	9-7	niin
D6	MDSI_C_DN[2]	
Vec	LPDDR3_M0_CKE[1]_B MDSI_C_DN[2] 321	3 un.
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E11	VSS	-	E42	
E12			E43	LPDDR
E13	RESERVED	-	E44	
L13		-	E45	LPDDR
E14		-	E46	1700
E15	VSS	-	E47	LPDDR
		F	E48	
E17	MCSI_1_DP[2]	_ a	E49	LPDDR
E18 E19 E2 E20 E21		1,,,	E5	DDI1
E19	VSS		E50	
E2	sineu	F	E51	LPDDR
E20	den	F		
E21	DDI2_DDC_CLK/DDI1_DDC_CLK/	F	E52	
	UARTO_DATAOUT/ MDSI_DDC_CLK/MDSI_A_TE	F	E53	VSS
E22		F	E54	477
E23	CORE_VCC1_S0iX	L	E55	RESER
E23			E56	
E24			E57	RESER
E25	DDI1_HPD		E58	
E25 E26 E27 E28 E29 E3 E30			E59	VSS
E27	GPIO_CAMERASB06	Ī	E6	
E28	unc	-	E7	VSS
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E3	DDI1_TXN[2]		E9	MDSI
E30	GPIO_CAMERASB02		F1	
E31	Ø		F10	VSS
E32		- 67	F11	
E33	JTAG_TDI	<i>></i>	F12	MDSI
E34			F13	
E35	JTAG_TRST_N			
E36	Junos	L	F14	VSS
E37	GPIO_SUS0	-	F15	
E38			F16	VSS
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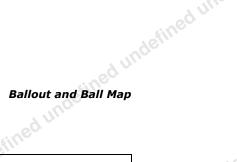
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E4	"dell	
E40	ad),,	
E41	VSS	
E42	1100	
E43	LPDDR3_M0_DQ[18]_A	
E44	46ff	
E45	LPDDR3_M0_DQ[20]_A	
E46	Weo.	901
E47	LPDDR3_M0_DQ[24]_A	
E48	LPDDR3_M0_DQ[20]_A LPDDR3_M0_DQ[24]_A LPDDR3_M0_DM[03]_A	
E49	LPDDR3_M0_DM[03]_A	
E5	DDI1_TXN[1]	
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E52	Jeffi	
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E9	MDSI_A_DP[1]	
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F12	MDSI_A_DP[2]	
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	Ball #	Customer Name - LPDDR3	Ball #	C
ge,	F19	- file	F50	LPDI
	F2	VSS	F51	
	F20	DDI2_DDC_DATA/	F52	LPDI
		DDI1_DDC_DATA/UART0_DATAIN/ MDSI_DDC_DATA/MDSI_C_TE	F53	
4 une	F21		F54	RESI
	F22	DDI0 VDDEN	F55	
dell	F23		F56	RESI
od m.	F23	CORE_VCC1_S0iX	F57	
istine	F24 F25	CORE_VCC1_SUIX	F58	VSS
uge.	F25		F59	V60.
ndefined undefined undef	F26	DDIO_DDC_CLK/DDI1_DDC_CLK/ MDSI_DDC_CLK	F6	VSS
	F27		F7	
undefined undefined unde	F28	GPIO_CAMERASB11	F8	VSS
dulle	F29	11/961	F9	
	F3		G1	DDI2
inde.	F30	46/11	G10	
ed u.	F31	, uno	G11	MDS
iefine	F32	SVID_CLK	G12	0
	F33	-9e	G13	VSS
	F34	JTAG_TCK	G14	
	_ 0,0		G15	MCS
	F36	GPIO_SUS8	G16	
od uli	F37		G17	VSS
igfine	F38	GPIO_N2/C0_BPM2_TX/	G17	
inde		C1_BPM2_TX	G19	MCS
ndefined undefined und	F39	dunc	G2	
defill	F4	DDI1_TXP[1]	G20	e
	F40	VSS	G20	VSS
	F41	2	G21	
		LPDDR3_M0_DQ[19]_A	.0	
	F43	465	G23 G24	COR
ad u.	F44	LPDDR3_M0_DQ[16]_A		
4efine	F45	417	G25	VSS
, nuor	F46	LPDDR3_M0_DM[2]_A	G26	
ined in	F47	3	G27	GPIC
defili	F48	VSS	G28	
undefined undefined un	F49	068	G29	DDI.
	F5	ned undefined undef	G3	DDI

	161	1
Ball #	Customer Name - LPDDR3	nd!
F50	LPDDR3_M0_DQ[28]_A	defined und
F51		1. Fine
F52	LPDDR3_M0_DQ[31]_A	loc
F53	ed	
F54	RESERVED	
F55	A Une	
F56	RESERVED	
F57	"Jqe,	
F58	VSS	Inc
F59	(C)	ndefined uni
F6	VSS	defill.
F7		luc.
F8	VSS	1
F9	John	
G1	DDI2_VDDQ_G3	
G10	Stine	
G11	MDSI_A_DN[2]	
G12	89	indefined un
G13	VSS	eineo.
G14		ageill
G15	MCSI_2_DP[1]	
G16	sine	1
G17	VSS	
G18		
G19	MCSI_1_DP[3]	
G2	, 1/1/0	
G20		Jefined v
G21	VSS	FILLER
G22		undefille
G23	CORE_VCC1_S0iX	O.
G24	46/11	1
G25	VSS	1
G26	:: 100	1
G27	GPIO_CAMERASB05	1
G28	4011	
G29	Hiller	ed'
G3	DDI1_TXN[0]	4efine
ed or		, uno
	 DDI1_TXN[0]	
	29.	





	led
all#	Cus
0	MDSI_
100	
2	VSS
.3	
.4	MCSI
.5	
.6	MCSI
.7	
.8	MCSI
.9	141031_
9	DDI1
:0	MCSI
1	MCS1_
.2	DDI1_
:3	
.4	CORE_
.5	
.6	DDI0_ DDI1_
.00	MDSI_
.7	
.8	VSS
:9	
;	
0	
1	
- 32	PROCH
3	-5100
4	JTAG_I
5	
6	VSS
7	V33
	GPIO_
0	DDI1_
	VSS
.1	76 ₍₁₎ ,
2	LPDDR
	8 9 0 1

Ball #	Customer Name - LPDDR3	iined
H10	MDSI_A_DN[3]	60
H11		ine
H12	VSS	
H13		
H14	MCSI_2_DN[1]	
H15	dune	
H16	MCSI_2_CLKP	
H17	age,	
H18	MCSI_1_DN[3]	
H19	1 2	
H2	MCSI_1_DN[3] DDI1_AUXP MCSI_1_DP[0]	3/1.
H20	MCSI_1_DP[0]	
H21	cine	
H22	DDI1_VDDEN/MDSI_DDC_DATA	
H23		
H24	CORE_VCC1_S0iX	
H25	Wo	
H26	DDI0_DDC_DATA/ DDI1_DDC_DATA/ MDSI_DDC_DATA	efin
H27		e,
H28	VSS	
H29	Lefine	
H3	INDO	
H30	ineo	
H31	dell	
H32	PROCHOT_N	
H33	Tines	
H34	JTAG_PREQ_N	Aefil
H35	4 117	
H36	PROCHOT_N JTAG_PREQ_N VSS	
H37	dell	
H38	GPIO_N5	
H39	Lefineu	
H4	DDI1_TXP[0]	
H40	VSS	
H41	- Fill	
H42	LPDDR3_M0_DQ[02]_A	ge,
iu _{eq} m	VSS LPDDR3_M0_DQ[02]_A Datasheet	

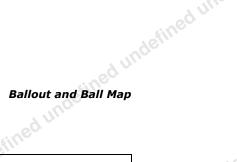
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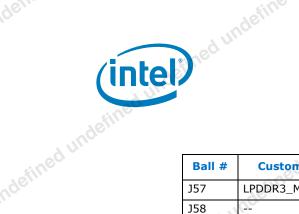


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	ed nur		, under		
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Ballout and Ba	Ball #	Customer Name - LPDDR3		Ball #	~ 6
96,	H43	75/11		J23	COR
	H44	VSS		J24	
e?	H45		6	J25	COR
dei	H46	VSS	0	J26	
dum	H47	Inde		J27	GPIC
idefined undefined undef	H48	LPDDR3_M0_DQ[09]_A		J28	
inde.	H49	48fills		J29	
ed u.	H5	Junos		J3	DDI:
16fin	H50	LPDDR3_M0_DQS[1]_P_A	J30		GPIC
10-	H51	, d ella		J31	15
	H52	LPDDR3_M0_DQ[11]_A		J32	
	H53		eg.	J33	JTAG
idefined undefined unde	H54	RESERVED		J34	
ed un.	H55	uno		J35	GPIC
ight	H56	VSS		J36	
Inde	H57	defin		J37	JTAG
ned v	H58	LPDDR3_M0_CKE[0]_A		J38	
	H59	*ine		J39	GPIC
	H6	MDSI_C_DN[1]		ائم.	C1_E
	H7			J4	
<u> </u>	Н8	MDSI_C_DN[3]	20	J40	
on,	H9	76	10.	J41	VSS
ned u	J1	DDI2_VDDQ_G3		J42	
4efill.	J10	sineo		J43	LPDI
4 Uho.	J11	MDSI_A_DP[0]		J44	
eineo	J12	39 m		J45	LPDI
gen	J13	VSS		J46	
defined undefined und	J14	140 g		J47	LPDI
	J15	MCSI_2_CLKN		J48	
	J16		in	J49	LPDI
nu ,	J17	MCSI_3_CLKP	11.	J5	DDI
ndefined undefined un	J18	ad 2/1/		J50	
adein.	J19	MCSI_1_DN[0]		J51	LPDI
dun	J2	''''''		J52	
fines	J20	080		J53	LPDI
ge,	J21	DDI1_BKLTEN/MDSI_DDC_CLK		J54	
	J22	41000		J55	RESI
L				J56	

Ball #	Customer Name - LPDDR3 CORE_VCC1_S0iX CORE_VCC1_S0iX	
J23	CORE_VCC1_S0iX	0
J24	Istin	
J25	CORE_VCC1_S0iX	
J26		
J27	GPIO_CAMERASB09	
J28	une	
J29	singo	
J3	DDI1_AUXN	
J30	GPIO_CAMERASB00 JTAG_TDO	
J31	<u> </u>	
J32	defil	
J33	JTAG_TDO	
J34	"ineo	
J35	GPIO_SUS9	
J36	dun	
J37	JTAG2_TMS	
J38	Inde	
J39	GPIO_N6/C0_BPM3_TX/ C1_BPM3_TX 	
J4		111
J40	Inc	
J41	VSS	
J42	delt	
J43	LPDDR3_M0_DQ[04]_A	
J44	Sine	
J45	LPDDR3_M0_DQ[07]_A	
J46	60	
J47	LPDDR3_M0_DQS[0]_N_A	
J48	206	
J49	LPDDR3_M0_DQS[0]_N_A LPDDR3_M0_DQ[14]_A	
J5	DDI0_TXP[0]	
J50		
J51	LPDDR3_M0_DQ[15]_A	
J52	46killi	
J53	LPDDR3_M0_DQ[13]_A	
J54	-nec	
J55	RESERVED	
J56	Ind	0
J52 J53 J54 J55	LPDDR3_M0_DQ[13]_A RESERVED	

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aned u.	Ball #	Customer Name - LPDDR3		Ball #	Cus
	J57	LPDDR3_M0_CS[0]_N		K37 .	~60
	J58	02		K38	GPIO_
	J59	DDR_VDDQG_S4		K39	
A	J6	6		K4	DDI0
, unc	J7	DDI1_RCOMP_N		K40	GPIO_
	J8				C1_BP
defill	J9	MDSI_C_DP[3]		K41	
efined undefined und	K1			K42	LPDDR
	K10	VSS		K43	
	K10	48		K44	LPDDR
		20-		K45	
	K12	MDSI_A_DN[0]		K46	LPDDR
	K13	MDCI DCOMP		K47	
מני ,	K14	MDSI_RCOMP	12.	K48	VSS
led undefined un	K15	un		K49	
defill	K16	MCSI_3_CLKN		K5	
4 un	K17	"96",		K50	VSS
	K18	MCSI_RCOMP		K50	V33
	K19	file		_	0.0
	K2	VSS		K52	LPDDR
	K20	DDI1_BKLTCTL/MDSI_A_TE/		K53	
	18,100	MDSI_C_TE		K54	VSS
	K21		3/1/2	K55	
red v	K22	DDI0_BKLTCTL		K56	LPDDR
	K23	sineo		K57	
	K24	CORE_VCC1_S0iX		K58	VSS
	K25	4011		K59	
	K26	DDI0_HPD		K6	VSS
	K27	Jdet		K7	ē!III
undefined u	K28	GPIO_CAMERASB08		K8	DDI1_
	K29			K9	
	K3)	eli	L1	DDI1_
ed !	K30	4 UN		L10	
	K31	ined		L11	VSS
INOC	K32	GPIO_CAMERASB01		L12	
	K33			L13	VSS
	K34	GPIO_SUS10		L14	V33
		0.10_30310		L14	VSS
	レクロ				V.7.7
ined undefined in 326 stined undefined	K35	GPIO_SUS7/PMC_SUSCLK[3]		L16	

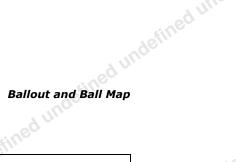
	i unoc
Ball #	Customer Name - LPDDR3 GPIO_SUS1/JTAG2_TCK
K37	
K38	GPIO_SUS1/JTAG2_TCK
K39	'nde'
K4	DDI0_TXN[0]
K40	GPIO_N8/C0_BPM1_TX/ C1_BPM1_TX
K41	
K42	LPDDR3_M0_DQ[00]_A
K43	, un
K44	LPDDR3_M0_DQ[05]_A
K45	LPDDR3_M0_DQ[05]_A LPDDR3_M0_DQS[0]_P_A
K46	LPDDR3_M0_DQS[0]_P_A
K47	
K48	VSS
K49	i nuo
K5	
K50	VSS
K51	d Unc
K52	LPDDR3_M0_DQ[12]_A
K53	do-
K54	LPDDR3_M0_DQ[12]_A VSS
K55	
K56	LPDDR3_M0_CKE[0]_B
K57	4 0/2
K58	VSS
K59	index
K6	VSS
K7	
K8	DDI1_RCOMP_P
K9	VSS DDI1_RCOMP_P DDI1_VDDQ_G3
L1	DDI1_VDDQ_G3
L10	, <u>n</u> de
L11	VSS
L12	Chine
L13	VSS
L14	eo
L15	VSS
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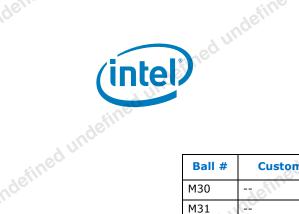


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	Ball #	Customer Name - LPDDR3	Ball #	C
ger	L17	VSS	L50	So
	L18	-	L51	LPDI
	L19	VSS	L52	
	L2	S	L53	RESI
4 Uno	L20	::\dell'	L54	
	L21	DDI0_BKLTEN	L55	LPDI
deill	L22	6170.6	L56	
d une	L23	CORE_VCC1_S0iX	L57	LPDI
	L24		L58	
idefined undefined undef	L25	CORE_VCC1_S0iX	L59	DDR
	L26		L6	
		VSS	L7	VSS
A	L28		L8	
4 nuc	L29	""96.	L9	DDI
ndefined undefined und	L29	VSS	M1	
adelli	L30	VSS	M10	
od uli	L31		M11	DDI
fine	F31	-0		
ige.	L32	4100	M12	VSS
	L33	VSS	M13	
			M14	VSS
	L35	VSS	M15	
4 nu	L36		M16	VSS
	L37	PWR_RSVD_OBS	M17	
defined undefined uni	L38	Agine	M18	VSS
ed m.	L39	VSS	M19	
	L4	ed	M2	DDI:
	L40	lefill	M20	VSS
	L41	VSS	M21	
			M22	VSS
	L43	LPDDR3_M0_DQ[01]_A	M23	
ad ul	L44	unde	M24	COR
Stines	L45	VSS	M25	
inde.	L46	Lefill	M26	COR
ed n.	L47	LPDDR3_M0_DQ[08]_A	M27	
undefined undefined un	L48		M28	COR
	L49	LPDDR3_M0_CA[0]	M29	777
	L5	DDIO_TXN[1]	M3	<u>0.</u>

	Ball #	Customer Name - LPDDR3	defined ur
ľ	L50	20	ed ui
	L51	LPDDR3_M0_CA[3]	Gine
	L52		
Ī	L53	RESERVED	
	L54	46/11	
	L55	LPDDR3_M0_CA[5]	
	L56	sing	
	L57	LPDDR3_M0_CA[7]	
	L58	9 ny	ndefined v
	L59	DDR_VDDQG_S4	red o
	L6		defille
9	L7	VSS	
	L8	sine	
ľ	L9	DDI0_AUXP	
ľ	M1	od ou	
ľ	M10	DDI0_TXN[3]	
	M11	'luge,	
	M12	VSS	Indefined
	M13	22	cineo.
	M14	VSS	
8	M15		711.
	M16	VSS	
	M17	11006	
	M18	VSS	
	M19	46/11	
	M2	DDI1_VDDQ_G3	
	M20	VSS	-6-
	M21	17.	
	M22	VSS	undefined
P	M23		
ľ	M24	CORE_VCC1_S0iX	
ľ	M25	Indo	
ľ	M26	CORE_VCC1_S0iX	
ľ	M27	dell	
ľ	M28	CORE_VCC1_S0iX	
ľ	M29	THE	
ľ	M3	2	defile
_	ed a.		una
10		CORE_VCC1_S0iX 327	
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961.		ndefine		defil	red
inte	*	idefine	red	MUC	
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	Ball #	Customer Name - LPDDR3		Ball #	Cus
	M30	-10/1/10		N10	450
	M31	C.		N11	DDI2_
	M32	VSS		N12	
	M33		Ue	N13	
od uli	M34	VSS		N14	
stines	M35	ed		N15	
Indefined undefined uni	M36	VSS		N16	
	M37	Inc.		N17	
defille	M38	VSS		N18	6
	M39	-9e//		N19	140
	M4	DDI0_TXP[1]		N2	
	M40	GPIO0_RCOMP	~ 6	N20	
	M41			N21	
undefined undefined ur	M42	VSS		N22	
46fills	M43	sined		N23	
uno	M44	LPDDR3_M0_DQ[06]_A		N24	
	M45	duit		N25	
defill	M46	LPDDR3_M0_DM[0]_A		N26	69
	M47	-nde		N27	5/7//
	M48	RESERVED		N28	
	M49		e5.10	N29	
	M5		Sim	N3	VSS
ined "	M50	LPDDR3_M0_CA[1]		N30	
defil.	M51	fines		N31	
4 unc	M52	VSS		N32	
	M53	60		N33	
undefined undefined u	M54	LPDDR3_M0_CA[4]		N34	ne
, Ur	M55	-nuos		N35	6-
	M56	VSS		N36	
	M57		41	N37	
A ^r	M58	VSS	e,	N38	
	M59	ed of		N39	
aden	M6	DDI0_TXP[2]		N4	
od m.	M7	nuos		N40	
isfines	M8	DDI0_AUXN		N41	
d undefined undefined	M9	defill		N42	
	N1	USB_V3P3A_G3		N43	Go,

	Ball #	Customer Name - LPDDR3	indefined un
	N10	Co.	od un
	N11	DDI2_TXN[0]	Sine
3	N12		"uge.
UG,	N13		J
	N14	tefin	
	N15	'Una	
	N16		
	N17	defill	
	N18	- d une	undefined u
	N19	14760	ed u
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	N25	vqe _{II} ,	
	N26	0 1111	undefined i
	N27	<u>an</u>	red.
	N28		defill,
	N29		und
	N3	VSS)·
	N30	Joeli	
	N31	29 711.	
	N32	- Fine	
	N33	Inde	
	N34	260	۸
	N35	Cill.	sine c
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cial	N37		d undefined
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	N39	- inde	
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	N40	Jeline	
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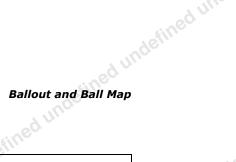
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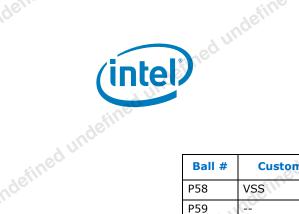


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fined L	Ball #	Customer Name - LPDDR3	Ball #	C
der	N44	- file	P24	5.0
	N45	0	P25	COR
.0	N46		P26	
Ae [§]	N47		P27	COR
4 Unce	N48	170°C	P28	
sineo.	N49	VSS	P29	VSS
adelli	N5	DDI0_TXN[2]	P3	
dulle	N50	1/26	P30	
fines	N51	LPDDR3_M0_CA[6]	P31	
Ye.	N52		P32	COR
	N53	VSS	P33	
	N54		P34	COR
. 0	N55	LPDDR3_M0_CK_N_A	P35	
4 Unex	N56		P36	COR
eineo.	N57	LPDDR3_M0_CK_P_A	P37	
adelli				
d ull	N58		P38	COR
fine	N59	DDR_VDDQG_S4	P39	
96,	N6	file	P4	DDI
	N7	VSS	P40	VSS
	N8		P41	
- 2	N9	DDI0_TXP[3]	P42	VSS
4 Unic	P1		P43	
eineo.	P10	DDI2_TXP[0]	P44	VSS
dein	P11	Siin	P45	
-0	P12	VSS	P46	VSS
Stines	P13	690	P47	
	P14	Jefins	P48	LPDI
	P15	VSS	P49	77.
	P16		P5	
	P17	VSS	P50	RESI
dun	P18		P51	
-tines.	P19	VSS	P52	VSS
inder.	P2	USB_V3P3A_G3	P53	
ed un	P20	Illuog	P54	LPDI
Gline	P21	VSS	P55	
Inde	P22	Jeffitt	P56	LPDI
undefined undefined un	P23	VSS	P57	5.
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46/11		ein ^e		

Ball #	Customer Name - LPDDR3	idefined uni
P24	20.0	4 UIV
P25	CORE_VCC1_S0iX	eineo
P26		dell.
P27		
P27	CORE_VCC1_S0iX	
	ade.	
P29	VSS	
P3	46/1/10	
P30	1 11000	indefined ur
P31		4 11
P32	CORE_VCC0_S0iX	*inec
P33		ude.
P34	CORE_VCC0_S0iX	
P35		
P36	CORE_VCC0_S0iX	_
P37		_
P38	CORE_VCC0_S0iX	_
P39		
P4	DDIO_RCOMP_N	30 V
P40	VSS 	undefined v
P41		MOS
P42 P43	VSS	
P43	VSS	1
P45		4
P46	VSS	_
P47	170	
P48	LPDDR3_M0_CA[2]	undefined
P49		eineo.
P5		delli
P50	RESERVED	Julia
P51	RESERVED	
P52	VSS	-
P53		-
P54	LPDDR3_M0_CK_N_B	1
P55	4 <i>Ung</i>	1
P56	LPDDR3_M0_CK_P_B	60
P57	2	istine
-9 m		Inde
ifined un	LPDDR3_M0_CK_P_B	
	ed undefine	

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Rail # Customer Na P58	me - LPDDR3	Ball # R38 R39 R4 R40 R41	Cus
P6 VSS P7 P8 VSS P9 R1 VSS R10 R11 VSS R10 R11 VSS R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R27 R28 R29 R3 DDI2_AUXN R30	me - LPDDR3	R38 R39 R4 R40	~eq.
P6 VSS P7 P8 VSS P9 R1 VSS R10 R11 VSS R10 R11 VSS R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R27 R28 R29 R3 DDI2_AUXN R30	efined under ne	R39 R4 R40	
P6 VSS P7 P8 VSS P9 R1 VSS R10 R11 VSS R10 R11 VSS R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R27 R28 R29 R3 DDI2_AUXN R30	efined undefine	R4 R40	
P7 P8 VSS P9 R1 VSS R10 R11 VSS R10 R11 VSS R12 R13 R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN P30	efined under ne	R40	
P8	efined undefine		
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	efined under	R41	
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	ethed H	LINTA	
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	efinec	R42	
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	6,	R43	
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN R30		R44	
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R45	\
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R45	1-0eg
R14 R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R45	
R15 R16 R17 R18 R19 R2 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		4777	
R16 R17 R18 R19 R2 R20 R21 R22 R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R48	
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	~96/11.	R49	RESER
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	d III.	R5	DDI0_
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	- ine	R50	
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN	qe,	R51	RESER
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R52	
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R53	LPDDR
R22 R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R54	2-1
R23 R24 R25 R26 R27 R28 R29 R3 DDI2_AUXN		R55	LPDDR
R30	200	R56	
R30	29811	R57	VSS
R30	d uli	R58	
B30	sines	R59	VSS
R30	uge.	R6	
R30		R7	VSS
R30		R8	e
P30		R9	VSS
R30		T1	
R31		T10	DDI2_
R32	e	T11	
	770	T12	VSS
R33	sineu.	T13	
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R34	71.	T14	ļ
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R36		T16	VSS
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R4	
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R41	46411
R42	June
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R44	adel
R45	901
R46	1420°
R47	
R48	
R49	RESERVED
₹5	DDI0_RCOMP_P
R50	og un.
R51	RESERVED
R52	'Wge,
R53	LPDDR3_M0_CA[9]
R54	ELL.
R55	LPDDR3_M0_DQ[02]_B
R56	
R57	VSS
R58	"Inde
R59	VSS
₹6	Lefill
27	VSS
₹8	-ineo
39	VSS
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10	DDI2_TXN[2]
11	defil
12	VSS
Г13	sineo
T14	UNCORE_VSFR_G3
15	Aunce
16	VSS
T17	ge,
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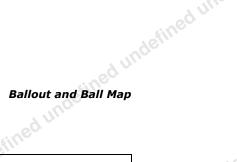
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dell	T18	VSS	T51	50
_	T19	2-	T52	LPDI
_	T2	DDI2_TXP[1]	T53	
<u> del</u>	T20	VSS	T54	LPDI
unc	T21	0001:	T55	
sineo	T22	VSS	T56	VSS
adeii.	T23		T57	
dulle	T24	VSS	T58	LPDI
fine	T25	280	T59	
46,	T26	VSS	T6	VSS
-	T27		T7	
<u> </u>	T28	VSS	T8	USB
de	T29		T9	
d nuce	T3	""	U1	USB
	T30	60 0.	U10	
nder.	T31	CORE_VCC0_S0iX	U11	DDI
od uli	T32		U12	
fine	T33	CORE_VCC0_S0iX	U13	6
nde.	T34		U14	17
-	T35	CORE_VCC0_S0iX	U15	
			U16	
20	T37	CORE_VCC0_S0iX	U17	
ed m.	T20			
fine	T38	20	U18	
inde	T39	VSS ALIVE	U19	
-0,	T4	DDI2_AUXP	U2	
16/il/10	T40		U20	
	T41	VSS	U21	100
_	T42	TVCC	U22	
		VSS	U23	
	T44		U24	
ed uli	T45	VSS	U25	
ighthe	T46		U26	
Inde	T47		U27	
bed	T48	LPDDR3_M0_OCAVREF	U28	
46till.	T49	- inec	U29	
unc	T5	dell.	U3	DDI
	T50	LPDDR3_M0_ODQVREF	U30	Y
Datasheet		LPDDR3_M0_ODQVREF	U30	<u> </u>

1 1		defille	
	Ball #	Customer Name - LPDDR3	idefined und
	T51	22	ed ui
	T52	LPDDR3_M0_CA[8]	istine
-8	T53		
S	T54	LPDDR3_M0_DQ[00]_B	
	T55	48/1/1	
	T56	VSS	
	T57	::100	
	T58	LPDDR3_M0_DQ[03]_B	
	T59	d Ulus	indefined un
	T6	VSS	ed u.
	T7.		18fine
6	T8	USB_VBUSSNS	
10	T9		
	U1	USB_VDDQ_G3	
	U10	4 unc	
	U11	DDI2_TXP[2]	
	U12	461	
	U13)),
	U14	<u>U.</u>	
	U15		defille
.0	U16		undefined ur
100	U17	:1000	
	U18	adelli	
	U19		
	U2	Sine	
	U20	"uge,	
	U21	60	undefinedu
	U22 AC	1100	
	U23		geil.
0	U24	6	Ulli
	U25	indefined	
	U26	inde	
	U27	60 01	
	U28	18/1/10	
	U29	Uno	
	U3	DDI2_TXN[1]	- 2
	U30 - 0		Filler
]	700		
efil		DDI2_TXN[1] 331	90.
		331	
		adefine	
		od um	

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ndefined undefine		indefil.	1		1
16 fine	Ball #	Customer Name - LPDDR3		Ball #	Cus
Jos	U31	ge _{LL} ,		V11	T-E
-	U32 U33			V12 V13	USB_C
\(\frac{1}{2}\)	U34		Neg	V13	
, uno	U35			V15	VSS
sined.	U36	00411.		V16	
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od un	U38	""		V18	
efine	U39	ed		V19	VSS
Inde	U4	76411		V2	USB_V
7	U40	77.	1	V20	
	U41		- 0	V21	UNCO
undefined undefined und	U42	30	110,	V22	
edu	U43	Ind		V23	UNCO
18 fine	U44	sineo		V24	
unoe	U45	adett		V25	UNCO
ined	U46	d ul.,		V26	
deill	U47	Fine		V27	PWR_F
nuc	U48	-1096		V28	27
	U49	VSS		V29	VSS
	U5	VSS	21/2	V3	
الله الم	U50		8,,	V30	
eineo.	U51	VSS		V31	
inder.	U52	tine		V32	CORE_
ed ui	U53	VSS		V33	
18fine	U54			V34	CORE_
unos	U55	LPDDR3_M0_DM[0]_B		V35	
Jundefined undefined ur	U56 U57	A VIV		V36 V37	CORE_
	U57	LPDDR3_M0_DQ[01]_B		V37	CORE_
	U59	VSS	efil	V36 V39	
nedu	U6			V4	DDI2_
defill	U7	USB_OTG_ID		V40	CORE_
d undefined undefined v	U8			V41	
sine c	U9	RESERVED	-	V42	VSS
inder.	V1	1611		V43	
g n.	V10	USB_DN[1]		V44	VSS
			j	700	1

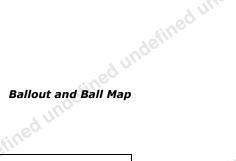
	Customer Name - LPDDR3	
V11	(20	undefi
V12	USB_DP[0]	igil
V13		Moje
V14	ed	7
V15	VSS	
V16	Juno	
V17	VSS	
V18	260	1
V19	VSS	1
V2	USB_VDDQ_G3	1
V20		46
V21	UNCORE_VNN_S4	unde
V22	"inec	
V23	UNCORE_VNN_S4	
V24	dune	1
V25	UNCORE_VNN_S4	1
V26	inde	1
V27	PWR_RSVD_OBS	1
V28	ALINE	1
V29	VSS	d unds
V3		dun
V30	stine	
V31	"luge,	1
V32	CORE_VCC0_S0iX	1
V33	Lefine	1
V34	CORE_VCC0_S0iX	1
V35	ned	ed und
V36	CORE_VCC0_S0iX	
V37		500
V38	CORE_VSS0_SENSE	9000
V39	DD12 TYP[3]	
V4	DDI2_TXP[3]	1
V40	CORE_VCC0_SENSE	1
V41	deill	1
V42	VSS	1
V43	sined	1
V44	VSS	1
ned w	Datashee	ned ur

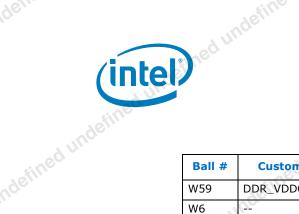
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Ball #	Customer Name - LPDDR3	Ball #	C
V45		W25	Sō
V46	VSS	W26	UNC
V47		W27	
V48	LPDDR3 M0 DQ[17] B	W28	UNC
V49	2001	W29	
V5	d 411,		USB
V50	LPDDR3 M0 DO[19] B		
V51	400		COR
V52	70.		
V53			COR
V54	40.	46/1	
		4777	COR
V56			
V50			COR
V5/	70.		COR
V50	410		
V 39			F_V1
V0	0		
V /			
VÖ		76	VSS
		7 0.	
W1	4	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	VSS
W10		W44	
W11			VSS
W12	Stine	W46	
W13	unde	W47	
W14	VSS	W48	
W15	efill	W49	LPDI
W16	VSS	W5	DDI
		W50	
W18	VSS	W51	LPDI
W19		W52	
W2	ed 0.	W53	VSS
W20	UNCORE_VNN_S4	W54	
W21	UNOCC	W55	LPDI
W22	UNCORE_VNN_S4	W56	
W23	defin	W57	LPDI
W24	UNCORE_V1P15_S0iX	W58	5.
	Ball # V45 V46 V47 V48 V49 V5 V50 V51 V52 V53 V54 V55 V56 V57 V58 V59 V6 V7 V8 V9 W1 W10 W11 W12 W13 W14 W15 W16 W17 W18 W19 W2 W20 W21	Ball # Customer Name - LPDDR3 V45 V46 VSS V47 V48 LPDDR3_M0_DQ[17]_B V49 V5 V50 LPDDR3_M0_DQ[19]_B V51 V52 VSS V53 V54 VSS V55 V56 LPDDR3_M0_DQS[0]_N_B V57 V58 VSS V59 V6 VSS V7 V8 VSS V9 W1 USB_VDDQ_G3 W10 W11 USB_DN[0] W12 W13 W16 VSS W17	Ball # Customer Name - LPDDR3 W25 W26 W27 W26 W27 W28 W29 W29 W29 W29 W30 W31 W31 W31 W32 W33 W32 W33 W34 W35 W35 W36 W37 W38 W35 W36 W37 W38 W39 W36 W37 W38 W39 W36 W37 W38 W37 W38 W39 W39 W30 W30 W31 W30 W31
Ball #	Customer Name - LPDDR3	defined ur	
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W25	20	od ui	
W26	UNCORE_VNN_S4	Silver	
W27		ge.	
W28	UNCORE_VNN_S4		
W29	Letin		
W3	USB_DN[2]		
W30	"1060		
W31	COREO_VSFR_G3		
W32	0 01		
W33	CORE_VCC0_S0iX		
W34		ndefined v	
W35	CORE_VCC0_S0iX		
W36	":1000		
W37	CORE_VCC0_S0iX		
W38	dun		
W39	F_V1P15_S0iX		
W4	''loge'		
W40		Indefined '	
W41	VSS	"ineo	
W42		gelli	
W43	VSS	71.	
W44	Sine		
W45	VSS		
W46			
W47	Actili		
W48	un		
W49	LPDDR3_M0_DQ[16]_B	60	
W5	DDI2_TXN[3]	undefined	
W50		INGE	
W51	LPDDR3_M0_DQS[2]_N_B		
W52	defill.		
W53	VSS		
W54	sineo		
W55	LPDDR3_M0_DQS[0]_P_B		
W56	9 _{n,}		
W57	LPDDR3_M0_DQ[05]_B		
W58	<u>0'</u>	defil.	
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	d undefile		

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raed u.	Ball #	Customer Name - LPDDR3		Ball #	Customer Name - LPDDR3	2
defill	W59	DDR_VDDQG_S4		Y39	~80 P. Como	4 nuo
1	W6	2.		Y4	USB_DP[2]	sineo.
	W7	VSS		Y40		ugel.
	W8	ú	ne	Y41	30	31.
uno	W9	USB_DP[1]		Y42	18/1/10	
ineo .	Y1		•	Y43	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
deili	Y10	VSS	-	Y44		
d un	Y11	''Uge.	}	Y45	76/1/	
	Y12	VSS	ŀ	Y46	4 NUO	
de,	Y13	46/1/10	ŀ	Y47	(4)e0	ed ni.
,	Y14	17.00	•	Y48	LPDDR3_M0_DQ[20]_B	Sine
<u> </u>	Y15			Y49		Inde
35	Y16		100	Y5		0
	Y17	1706	•	Y50	LPDDR3_M0_DQS[2]_P_B	
sinec.	Y18	60	•	Y51	7/1/2	
inder.	Y19	46110	•	Y52	LPDDR3_M0_DQ[22]_B	
ed u.	Y2	VSS	•	Y53	200	
iefine .	Y20	::100	•	Y54	LPDDR3_M0_DQ[04]_B)).
inac.	Y21	de ⁱ ///	•	Y55	77.	sed to
,	Y22	7,00	•	Y56	VSS	defille
 	V22			Y57		und
.0	Y24	20		Y58	LPDDR3_M0_DQ[06]_B	D
ed ul	Y25	duno	-	Y59		
fine	Y26	::/69		Y6	USB_DP[3]	
201	Y27					
, ed v	Y28	4 400	}	V8	VSS	
defill.	Y29	*!/\e\co	}	V9	00	
illo.	Y3	dein.	Ĺ	1 9	Chine	I sined
<u> </u>	Y30	2-			§	defill
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ed V	Y33	7 AU			ndeir	
Jefin .	Y33 Y34	*ineo			ed m.	
, uno	Y34 Y35	indelli			Stines	
ined.	Y35 Y36	ed ulli			Inde	
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334					Datasheet	
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Ball #	Customer Name - LPDDR3	indefined unde
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Y4	USB_DP[2]	istine
Y40		Inde
Y41		
Y42	Yellin	
Y43	4 UN	
Y44	sines	
Y45	adel	
Y46	d 01	Inc
Y47	120	ned o
Y48	LPDDR3_M0_DQ[20]_B	undefined und
Y49	3	Unc
Y5	sine	
Y50	LPDDR3_M0_DQS[2]_P_B	
Y51	ad u.	
Y52	LPDDR3_M0_DQ[22]_B	
Y53	inde	
Y54	LPDDR3_M0_DQ[04]_B	4 110
Y55	\$27°	Jundefined un
Y56	VSS	dell
Y57		y on,
Y58	LPDDR3_M0_DQ[06]_B	
Y59	inde	
Y6	USB_DP[3]	
Y7	defilt	
Y8	VSS	
Y9	-inec	ed u



Package Information materinad un

The SoC comes in Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Care should be taken to avoid contact with the package inside this area.

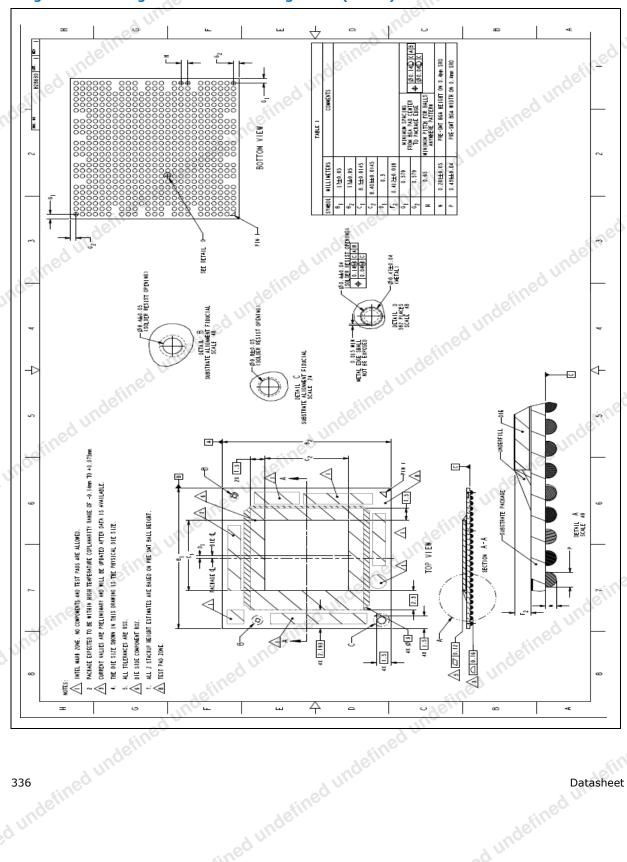
Table 165. SoC Attributes

, uno	bottom sid	le. Care shoul	ld be taken to avoic	I contact with the p	ackage inside this area.	
			Jefined unde		"Inge.	
defin			efines		ed v	
ad Uli 21.1	SoC A	ttribute	S		defill	
efine	20011	ined.	_	A UI		
Z1.1 Table 165.	SoC Attril	butes		lefined	ackage inside this area.	ined
		Category	Т4	4 UMO T3]	ndefill
.8	efilli	Туре	17x17mm Type 4	17x17mm Type 3	edu	
4 nuc		IO count	628	378	Aefins	
Jefined undefined und	Package	Core Process	14	14	defined undefined u	
ad un		Ball count	1380	592	defill	
efines		Ball pitch	0.4mm	0.65mm		
36.		Z-height	0.937mm	1.002mm		
	4 11					16/11.
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Package Diagrams 21.2

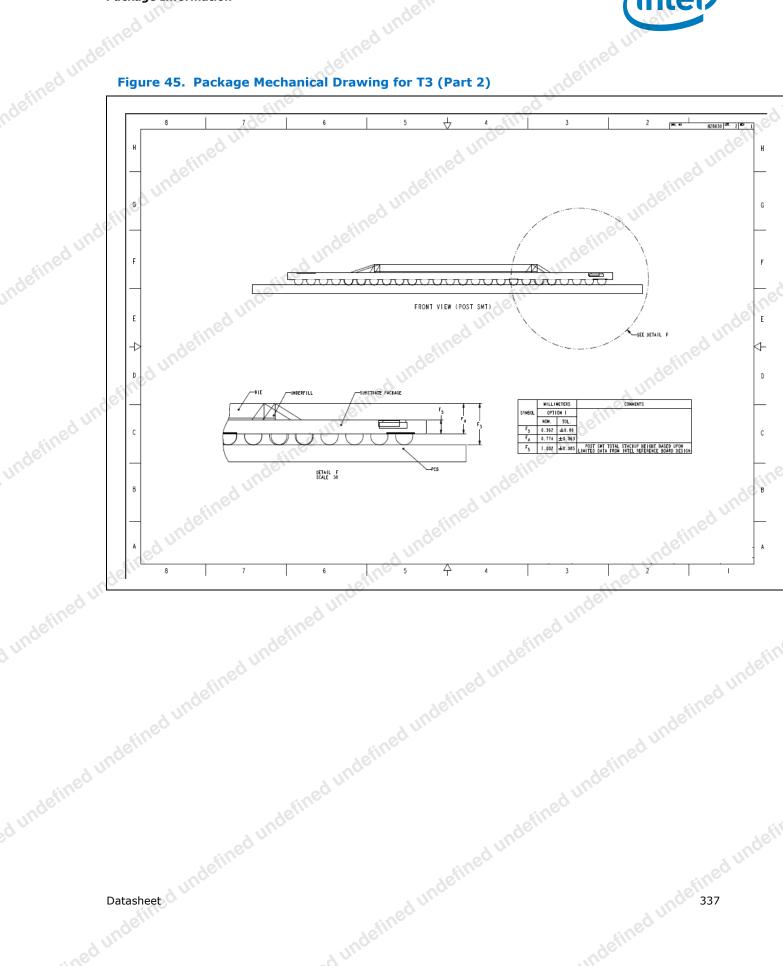
Figure 44. Package Mechanical Drawing for T3 (Part 1)



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Figure 45. Package Mechanical Drawing for T3 (Part 2)



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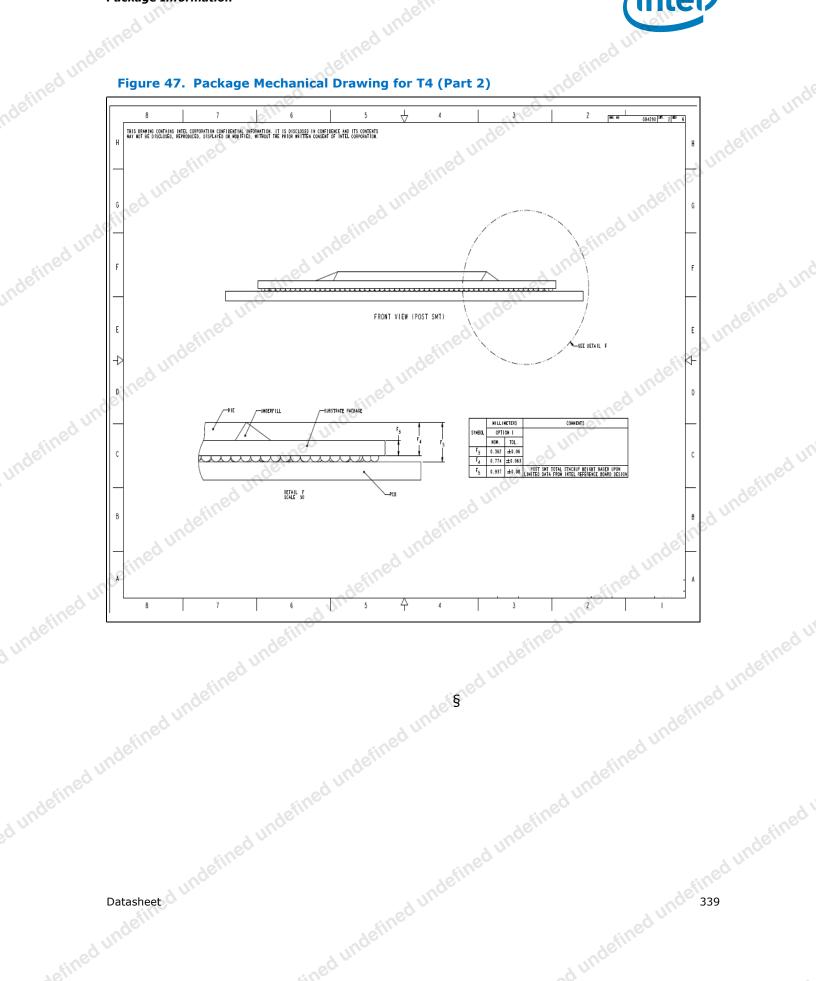
ANYMERE PATTERN
ANYMERE PATTERN
PRE-SWT BGA HEIGHT ON 0.25mm SRO
PRE-SWT BGA WIDTH ON 0.25mm SRO PRE-SMT BGA HEIGHT ON 0.3mm SRO PRE-SMT BGA WIDTH ON 0.3mm SRO LABLE 1 BOTTOM VIEW 0.111±0.05 0,334±0.05 0.144±0.05 0.285±0.05 0.412±0.018 (SOLDER RESIST OPENING) <u>₹</u> CSQLDER RESIST OPENINGS DETAIL B SUBSTRATE ALIGNMENT FIDUCIAL SCALE 48 -Ø0.8±0.05 (SOLDER RESIST OPENING) (\$0.3±0.04 (\$0L0ER RESIST OPENING) DETAIL C E ALIGNMENT FIDUCIAL SCALE 24 → \triangleleft DETAIL E 304 PLACES (INNER BOA AREA) SCALE 60 PACKAGE EXPECTED TO BE WITHIN HIGH TEMPERATURE COPLANARITY BANGE OF -0.11mm TO +0.100mm 2X ...5 CURRENT VALUES ARE PRELIMIMARY AND WILL BE UPDATED AFTER DATA IS AVAILABLE. \triangleleft V SUBSTRATE PACKAGE ALL Z STACKUP HEIGHT ESTIMATES ARE BASED ON PRE SNT BALL HEIGHT \triangleleft INTEL WARR ZONE, NO COMPONENTS AND TEST PADS ARE ALLOWED. Monde (THE WEIGHT OF THE PACKAGE IS ESTINATED TO BE 9.49 GRANS. SECTION A-A TOP VIEW 2.3 \triangleleft ALL TOLERANCES ARE 855. DIE SIDE COMPONENT NOZ. 4X 2, 193 ± 6 ≅ ADM 0.18 TEST PAD ZONE. ~i≪ 4 indefined undefined undefined undefin

Figure 46. Package Mechanical Drawing for T4 (Part 1)

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Figure 47. Package Mechanical Drawing for T4 (Part 2)



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