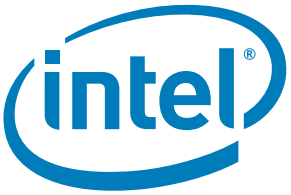


Intel® Atom™ Processor D2000 and N2000 Series

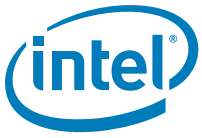
Datasheet - Volume 1 of 2

Refer to Doc ID 326137-003 for Volume 2 of 2

July 2012

Revision 003

Document Number: 326136-003



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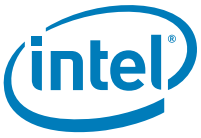

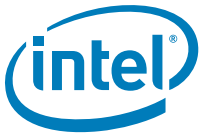

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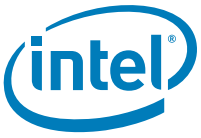

Revision History

Revision Number	Description	Date
001	• Initial Release	September 2011
002	**Chapter 1** • Section 1.2 — Added the DDR3L feature with Next Generation Intel® Atom™ Processor based Mobile Platform CPU. — Updated the Raw Card support type for DDR3 and DDR3L. • Section 1.4- Added Next Generation Intel® Atom™ Processor based (Desktop and Mobile) Platform SKU model. • Section 1.5- Added the Next Generation Intel® Atom™ Processor based (Desktop and Mobile) Platform SKU model. • Table 1-2- Added D2550 core clock frequency. • Section 1.7.1- Added DDR3L Terminology. **Chapter 2** • Table 2-5- Updated DDR3 buffer voltage with 1.35 V. • Table 2-8- Added the signal description of DDR3_DRAMRST#. • Table 2-20- Added the voltage of V_SM and VCCCKDDR with 1.35 V when implementing DDR3L. **Chapter 3** • Section 3.1 — Added the DDR3L features with Next Generation Intel® Atom™ Processor based Mobile Platform CPU. — Added support for DDR3L. • Section 3.2.4.12- Added D2550 related information. **Chapter 4** • Table 4-30- Added Next Generation Intel® Atom™ Processor based (Desktop and Mobile) Platform SKU model in Parameter Column. • Table 4-32 — Updated VCCGFX voltage. — Added the max/min voltage of V_SM and VCCCKDDR when implementing DDR3L. — Added refreshed CPU SKU model. • Table 4-34- Added the max input leakage current value when implementing DDR3L. • Table 4-42- Corrected the max value of LSB current. **Chapter 8** • Table 8-60- Updated new Next Generation Intel® Atom™ Processor based (Desktop and Mobile) Platform SKU with CPU frequency, TDP, Average Power and Idle Power.	December 2011

Revision Number	Description	Date
003	**Chapter 1** • Section 1.2 - Removed 512 MB from Supported total max memory size. Removed 4 Gbit from Supported max densities. Added raw card support type for memory down design. • Section 1.4- Removed DX*10 support • Section 1.5- Changed the Hardware Decode support description. It is now for Adobe 11.0 and newer versions. • Section 1.8 - Updated reference document number in the table. **Chapter 2** • Table 2-9 - Removed RSVD_NCTF_* and XDP_RSVD_[17:0] • Table 2-12 - Modified DAC_IRFEF resistor value from 680 Ohm to 649 Ohm. Changed DAC_IREF signal name to CRT_IREF. • Table 2-20 - Added VCC_GFX for N2000 series **Chapter 3** • Section 3.1- Removed SO-DIMM only • Section 3.1.2- Added raw card support type for memory down design • Section 3.2.4.8- Updated the states that the Display Port audio does not support **Chapter 4** • Table 4-32 - For D2000 series, separated VCCRAMXXX from other 1.067 V power rails and created a new row for it; also reversed other 1.067 V values back to 1.05 V. The voltage requirements of VCCRAMXXX for different CPUs are different now.	July 2012

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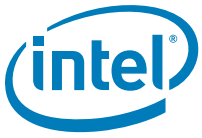


1 Introduction

This Datasheet (DS) provides Direct Current (DC) and Alternate Current (AC) electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Note: Throughout this document, the Intel® Atom™ Processor D2000 series and N2000 Series processor is referred to as processor and Intel® NM10 Express Chipset is referred to as chipset.

The processor is built on 32-nanometer Hi-K process technology. The processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the chipset and enables higher performance, lower cost, easier validation, and improved x-y footprint.

Included in this family of processors is an integrated memory controller (IMC), integrated graphics processing unit (GPU) and integrated I/O on a single silicon die. This single die solution is known as a monolithic processor.

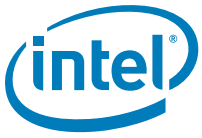
1.1 Intel® Atom™ Processor D2000 Series and N2000 Series Features

The following list provides some of the key features on this processor:

- On die, primary 32kB, 4-way L1 instructions cache and 24kB, 6-way L1 write-back data cache
- Intel® Hyper-Threading Technology 2-threads per core except for D2500 - no HT support
- 512-kB, 8-way ECC protected L2 cache per core processor
- Support for IA 32-bit
- Intel® Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Intel® 64 architecture
- Micro-FCBGA11 packaging technologies
- Thermal management support via Intel® Thermal Monitor (TM1 & TM2) - ELD TM1 only
- Supports C0 and C1 states only for D2000 series; C0-C4, C1E-C4E and Deep Power Down Technology (code named C6) state for N2000 series processor
- Execute Disable Bit support for enhanced security

1.2 System Memory Features

- One channel of DDR3
- memory (consists of 64 data lines):
  - — Maximum of two SODIMMs per channel for D2000 series and N2800 Processor performance, containing single or double-sided SODIMM
  - — Maximum of one SODIMMs per channel for N2600 series Processor only, containing single or double-sided SODIMM.
- Memory DDR3 data transfer rates of 800 MT/s (6.4 GB/s) and 1066 MT/s (8.5 GB/s)
- Only non-ECC SODIMMs are supported
- Refreshed SKU of Next Generation Intel® Atom™ Processor based Mobile Platform Processors support DDR3/DDR3L.
- Support Small Outline DIMMs Raw Cards RC-A (2Rx16), RC-B(1Rx8), RC-C (1Rx16) and RC-F (2Rx8) for DDR3. Support Small Outline DIMMs Raw Cards RC-B (1Rx8) and RC-F (2Rx8) for DDR3L.
  - — Does not support RC-D (2Rx16 dual die), and RC-E(2Rx16)
  - — No mixed Raw Card support.
- Support unbuffered SODIMMs
- Supports Memory Down Design with Raw Card Type B only
- I/O Voltage of 1.5 V for DDR3. I/O Voltage of 1.35 V for DDR3L.
- Max memory size by sku: N2600 series 2 GB; N2800, D2500 & D2700 series 4 GB
- Supports total memory size of 1 GB, 2 GB and 4 GB max
- Supports Max densities 1 Gbit, 2 Gbit for both x8 and x16 for DDR3
- DRAM Chip Data Width: x8 and x16
- Banks / DRAM Chip: 8
- Support up to 32 simultaneous open pages per channel (assuming 4 ranks of 8 devices)
- Support Partial Writes to memory using Data Mask signals (DM)
- Enhances Address Mapping
- Support DIMM page size of 1 KB and 2 KB
- Support data burst length of 8 and Burst Chopped of 4 for all memory configurations
- Support memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered by either on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.

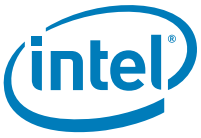


1.3 Direct Media Interface Features

- Compliant to Direct Media Interface (DMI)
- Support 2 lanes in each direction for N2000 series processor and 4 lanes in each direction for D2000 series, Gen1 (2.5 Gbps) per lane per direction, point-to-point DMI interface to Intel® NM10 Express Chipset or PCH respectively.
- The N2000 series processor can only work on boards that have a DMI x2 connection. It will not work on a board with a DMI x4 connection. While the D2000 series processor can only work on the boards have a DMI x4 connection.
- 100 MHz reference.
- Support 64 bit downstream address (only 36-bit addressable from CPU)
- Support APIC messaging support. Will send Intel-defined “End of Interrupt” broadcast message when initiated by CPU.
- Support messaging in both directions, including Intel-Vendor specific messages.
- Support Message Signal Interrupt (MSI) messages.
- Support Power Management state change messages.
- Support SMI, SCI and SERR error indication.
- Support PCI INTA interrupt from CHAP Counters device and Integrated Graphics.
- Support Intel® NM10 Express Chipset with on board hybrid AC-DC coupling solution.
- Support polarity inversion (However, NM10 does not support)

1.4 Graphics Processing Unit Features

- Support Directx*9 compliant Pixel Shader* v3.0 and OGL 3.0
- 640 MHz (D2550, D2700 & N2800/N2850) and 400 MHz (D2500 & N2600/N2650) graphic core frequency
- 200 MHz render clock frequency
- Seven display planes, Display Plane A, B, Display Sprite C (can be connected to either pipes), Display OV (can be connected to either pipes), Cursor A, Cursor B, and VGA
- Two display pipes, Pipe A and B support the dual independent displays
- Max Pixel Clock: SC LVDS: 112 MHz, 18bpp (N2000 series) & 18bpp and 24bpp (D2000 series); DDI: 2x 4, 1.62GHz, 2.7GHz; VGA: up to 350MHz
- Display Ports: eDP/DP x4, HDMI, LVDS (single channel), CRT/DAC
- Embedded panel: eDP1.1 or LVDS
- External panel: DP1.1, HDMI1.3a, LVDS, CRT/DAC.
- Supports HDCP 1.3 & PAVP1.1c (D2550, D2700 & N2800/N2850 processor) for Blu-ray playback while HDCP is needed for High Definition playback in Intel® Atom™ Processor D2000 and N2000 series



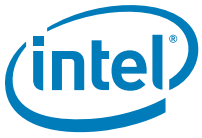
  - — PAVP: Collection of HW-based security mechanisms designed to provide a secure path for content from a media player application to the graphics hardware
  - — HDCP: Specification developed by Intel Corporation to protect digital entertainment content across the DVI interface
  - — Subsequently ported to HDMI and Display Port
- Supports HDMI 1.3a through SW lip-sync
- Supports NV12 data format
- 3x3 Panel Fitter shared by two pipes
- Support Intel HD Audio Codec
- Support Intel® Display Power Saving Technology (Intel® DPST) 4.0
- No Frame Buffer Compensation (FBC)
- No TVOut

Table 1-1. Summary of the Resolution of Graphic interface

Interfaces	Processor	Max Resolution	Remark
LVDS (Single Ch)	N2000 series	1366 x 768	60 Hz; 18 bpps
	D2000 series	1440 x 900	60 Hz; 18 & 24 bpps
eDP	N2000 series	1366 x 768	60 Hz
	D2000 series	1920 x 1080	60 Hz
VGA (CRT/DAC)	N2000 series	1920 x 1200	60 Hz at 267 MHz Max
	D2000 series	1920 x 1200	60 Hz at 355 MHz Max
DP	N2000 series	1600 x 1200	60 Hz with 4 lanes at 162 MHz link clock
	D2000 series	2560 x 1600	60 Hz with 4 lanes at 270 MHz link clock
HDMI/ DVI	N2000 series	1920 x 1200	60 Hz; up to 165MHz
	D2000 series	1920 x 1200	60 Hz; up to 165MHz

1.5 Video

- The Intel Atom Processor D2000 series and N2000 series supports full MPEG2 (VLD/ iDCT/MC), WMV, Fast video Composing, HW decode/ acceleration for MPEG4 Part 10 (AVC/H.264) & VC-1; 720p60, 1080i60, 1080p@24 up to 20 Mps
- MPEG4 part2 does not utilize Next Generation Intel® Atom™ Processor based desktop platform H/W
- Hardware Decode assist for Flash Decode for Adobe 11.0 and newer versions
- D2550, D2700 and N2800/N2850 processor supports Blu-Ray* 2.0 playback - 1 x HD and 1 x SD streaming
- Video image Enhancement: Hue, Saturation, Brightness, Contrast (HSBC) adjust, Bob De-Interlacing
- Support two Streams of 1080p HD @ 267 MHz



1.6 Clocking

- Differential Host clock of 100 MHz (HPL_CLKINP/HPL_CLKINN).
- Memory clocks - 100MHz differential for both DDR3-800 and DDR3-1066
  - — When running DDR3-800 or DDR3-1066, the 1x memory clocks is generated from internal Host PLL and the 2x memory clock is generated from Memory PLL
- The differential DMI clock of 100 MHz (EXP_CLKINP/EXP_CLKINN) generates the DMI core clock of 250 MHz.
- Display timings are generated from display PLLs that use a 96 MHz differential non-SSC for VGA only, and 100 MHz differential clock with SSC or non-SSC as reference.
- Host, Memory, DMI, Display PLLs and all associated internal clocks are disabled until PWROK is asserted.
- The Display core clock Frequency by Skus

Table 1-2. The Display core clock Frequency by Skus

Display Core Clock	D2500	D2550/ D2700	N2600	N2800	Remark
Frequency/ MHz	355	355	200	267	

- 27 MHz crystal is needed to resolve digital display quality concerns.

Table 1-3. 27 MHz Requirement Range

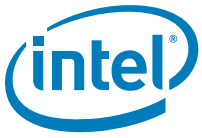
Min/MHz	Nominal/ MHz	Max/MHz	Remark
26.9919	27	27.0081	300 ppm

1.7 Power Management

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 kB)
- Support extended SMRAM space above 256 MB, additional 1MB TSEG from the base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by CPU).
- ACPI Rev 1.0b compatible power management
- Support CPU states: C0 and C1 (for D2000 series); C0-C4, C1E-C4E, Deep Power Down Technology (code named C6)(for N2000 series)
- Support System states: S0, S3, S4 and S5
- Support CPU Thermal Management (TM1 & TM2) while D2000 series is TM1 only

1.7.1 Terminology

Term	Description
BGA	Ball Grid Array
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR3	Third generation Double Data Rate SDRAM memory technology
DDR3L	Low Voltage DDR3
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Micro-FBGA	Micro Flip Chip Ball Grid Array
(G)MCH	Legacy component - Graphics Memory Controller Hub. Platforms designed for the N2000 series and D2000 series do not use an (G)MCH.
GPU	Graphics Processing Unit
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI. Platforms designed for the Intel Atom Processor D2000 series and N2000 series do not use an ICH.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
LCD	Liquid Crystal Display
LLC	Last Level Cache. The LLC is the shared cache amongst all processor execution cores
LVDS	Low Voltage Differential Signaling A high speed, low power data transmission standard used for display connections to LCD panels.
MCP	Multi-Chip
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Processor	The 64-bit, multi-core component



Term	Description
Processor Core	The term “processor core” refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
SMT	Simultaneous Multi-Threading
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TOM	Top of Memory
TTM	Time-To-Market
V_{CC}	Processor core power supply
V_{SS}	Processor ground
V_{CCGFX}	Graphics core power supply
V_SM	DDR3 power rail
VLD	Variable Length Decoding

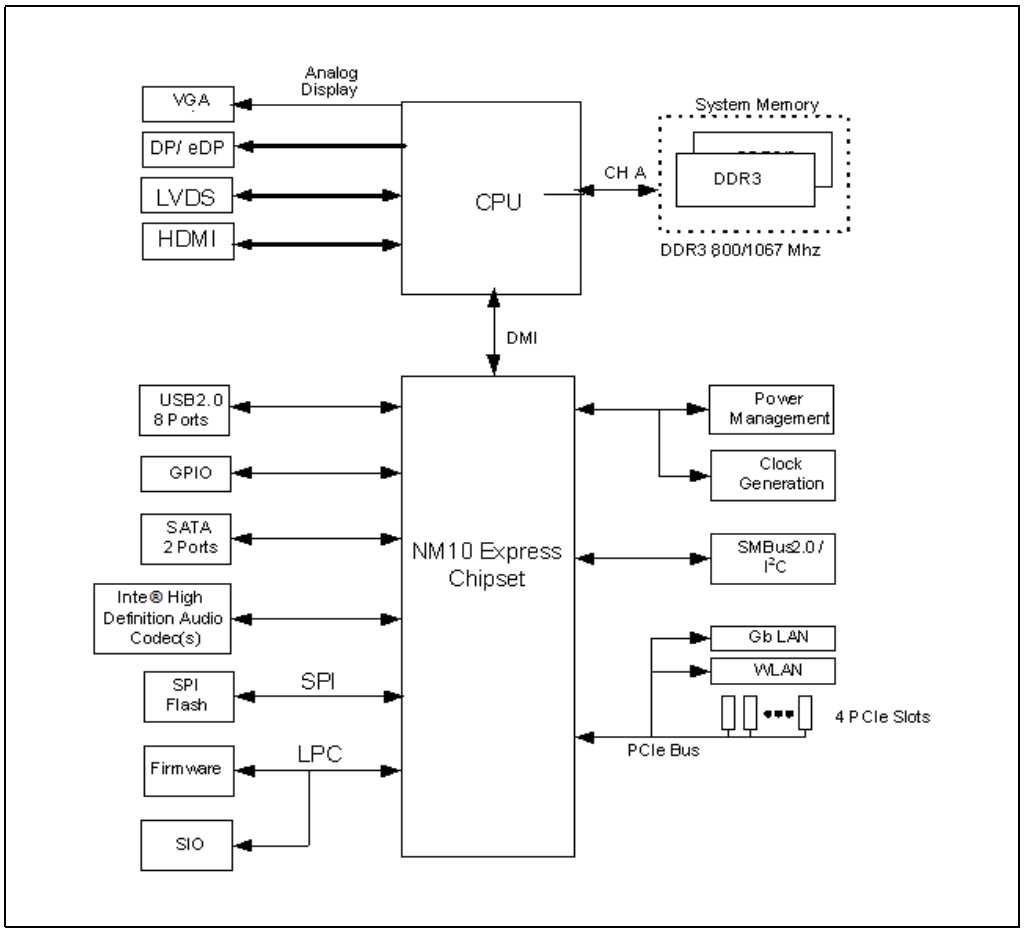
1.8 References

Material and concepts available in the following documents may be beneficial when reading this document:

Document	Document Number
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html?wapkw=architectures+software+developers+manuals
Intel Atom Processor D2000 series and N2000 Series Specification Update	326140
Intel Atom Processor D2000 series and N2000 Series Datasheet Volume 2 of 2	326137

1.9 System Block Diagram

Figure 1-1. Intel® Atom™ D2000 series/N2000 series System Block Diagram



1.9.1 PHOLD limitation on Legacy Feature

PHOLD protocol is a mechanism for ISA to lock the system so that it can do a DMA. Hence, the Intel Atom Processor D2000 series and N2000 series does NOT support PHOLD protocol which impacts the devices behind LPC (ISA) Super I/O only (No LPC mastering is allowed). These will need to be connected via USB adaptor if required.

This will not impact other legacy devices such as serial port, keyboard/mouse as well as USB based peripheral. If one of these devices are connected to LPC and a PHOLD is requested, Intel Atom Processor D2000 series and N2000 series will drop the request, set an error bit, and the system will immediately hang.

§

2 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type:

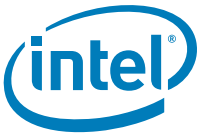
Table 2-4. Signal Type

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal.

Table 2-5. Signal Description Buffer Types

Signal	Description
CMOS	CMOS buffers. 1.05 V tolerant
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signalling Environment AC Specifications but are DC coupled. The buffers is 1.05 V/1.08 V and not 3.3 V tolerant.
HVCMOS	High Voltage buffers. 3.3 V tolerant
DDR3	DDR3 buffers: 1.5 V tolerant. When implementing DDR3L, the buffer is 1.35 V tolerant.
GTL+	Open Drain Gunning Transceiver Logic signaling technology. Refer to GTL+ I/O Specification fro complete details.
TAP	Test Access Port signal
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Ref	Voltage reference signal
Asynch	This signal is asynchronous and has no timing relationship with any reference clock.
LVDS	Low Voltage Differential Signalling. A high speed, low power data transmission standard used for display connections to LCD panels.



2.1 CPU Legacy Signal

Table 2-6. CPU Legacy Signal (Sheet 1 of 2)

Signal Name	Description	Direction	Type
EXTBGREF	External Band gap Reference. SOC and Core Debug feature.	I	Core Analog
HV_GPIO_RCOMP	RCOMP for 3.3V GPIO pins: 50 ohm 1% PD to VSS.	N/A	Analog
MV_GPIO_RCOMP	RCOMP for DFX_GPIO_GRPx pins: 50 ohm 1% PD to VSS.	N/A	Analog
PBE#	When STPCLK# is not asserted, the Intel Atom Processor D2000 series and N2000 series processor will always deassert PBE#. The Intel Atom Processor D2000 series and N2000 series processor is always allowed to use PBE to request a break to C0 - even if in C4 and in Deep Power Down Technology (code named C6)	O	Core Open Drain
INIT#	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. CPU then restarts at the reset vector. Snoops are handled during INIT# assertion.	I	Core CMOS
INTR /LINT00	Interrupt Request/Local APIC Interrupt 0: When the APIC is disabled, the LINT0 signal becomes INTR, a maskable asynchronous interrupt request signal. This signal (and NMI/LINT1) must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.	I	Core CMOS
NMI/ LINT10	Non-Maskable Interrupt Request/Local APIC Interrupt 1: When the APIC is disabled, the LINT1 signal becomes NMI, a non-maskable asynchronous interrupt request signal. This signal (and INTR/LINT0) must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.	I	Core CMOS
CPUPWRGOOD	CPUPWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Rise time and monotonicity requirements are shown in Chapter 4 Electrical Specifications. CPUPWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of CPUPWRGOOD. It must also meet the minimum pulse width specification. The CPUPWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	I	Core CMOS

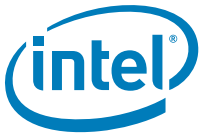


Table 2-6. CPU Legacy Signal (Sheet 2 of 2)

Signal Name	Description	Direction	Type
SMI#	System Management Interrupt. When asserted, CPU enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.	I	Core CMOS
STPCLK#	Stop Clock: When asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units, except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.	I	Core CMOS
PRDY#	Probe Mode Ready: CPU's response to PREQ# assertion. Indicates CPU is in probe mode. Input unused.	O	CMOS
PREQ#	Probe Mode Request: Assertion is a Request for the CPU to enter probe mode. CPU will response with PRDY# assertion once it has entered. PREQ# can be enabled to cause the CPU to break from C4 and C6. External 51-Ohms resistor to 1.8 V.	I	CMOS
CPUSLP#	CPI Sleep	I	CMOS
DPRSTP#	DPRSTP# when asserted on the platform causes the processor to transition from Deep Sleep State to the Deeper Sleep State. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the chipset. This function is supported for N2000 series only processor	I	Core CMOS
DPSLP#	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep State. In order to return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the chipset. This function is supported for N2000 series only processor.	I	Core CMOS

2.2 System Memory Interface

Table 2-7. Memory Channel A

Signal Name	Description	Direction	Type
DDR3_CK[3:0] DDR3_CK#[3:0]	SDRAM and inverted Differential Clock: (3pairs per DIMM) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to rank on DRAM side.	O	DDR3
DDR3_CS#[3:0]	Chip Select: (1 per Rank). Used to qualify the command on the command bus for a particular rank.	O	DDR3
DDR3_CKE[3:0]	Clock Enable: (power management - 1 per Rank) It is used during DRAM power up/power down and Self refresh.	O	DDR3
DDR3_MA[15:0]	Multiplexed Address. Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol w.r.t. CK/CK# pairs	O	DDR3
DDR3_BS[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank	O	DDR3
DDR3_RAS#	Write Enable Control Signal: Used with SA_WE# and SA_CAS# (along with, control signal, SA_CS#) to define the SDRAM Commands.	O	DDR3
DDR3_CAS#	Write Enable Control Signal: Used with SA_WE# and SA_CAS# (along with control signal, SA_CS#) to define the SDRAM Commands.	O	DDR3
DDR3_WE#	Write Enable Control Signal: Used with SA_WE# and SA_CAS# (along with control signal, SA_CS#) to define the SDRAM Commands.	O	DDR3
DDR3_DQ[63:0]	Data Lines. Write Enable Control Signal: Used with SA_WE# and SA_CAS# (along with control signal, SA_CS#) to define the SDRAM Commands.	I/O	DDR3
DDR3_DM[7:0]	Write Enable Control Signal: Used with SA_WE# and SA_CAS# (along with control signal, SA_CS#) to define the SDRAM Commands.	O	DDR3
DDR3_DQS[7:0] DDR3_DQS#[7:0]	Data Strobes: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[8:0] and its SA_DQS#[8:0] during read and write transactions. For Read, the Strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.	I/O	DDR3
DDR3_ODT[3:0]	ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.	O	DDR3

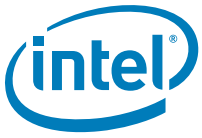


Table 2-8. Memory Reference and Compensation

Signal Name	Description	Direction	Type
DDR3_ODTPU	This signal needs to be terminated to VSS on board using the RES of 275 ohms. This external resistor termination scheme is used for Resistor compensation of DDR ODT strength.	O	Analog
DDR3_DQPU	This signal needs to be terminated to VSS on board using the RES of 35 ohms. This external resistor termination scheme is used for Resistor compensation of DQ buffers	O	Analog
DDR3_CMDPU	This signal needs to be terminated to VSS on board using the RES. This external resistor termination scheme is used for Resistor compensation of CMD buffers.	O	Analog
DDR3_VREF	DDR interface Reference Voltage	I	Analog
DDR3_DRAM_PWROK	This signal indicates the status of 1.5-V power supply.	I	Asynchronous CMOS
DDR3_MON1P DDR3_MON1N DDR3_MON2P DDR3_MON2N	These signals are for internal electrical validation. They do not carry functionality on customer platform	O	CMOS
DDR3_REFP DDR3_REFN	100MHz Differential Board clock input for DDR PLL.	I	Differential Clock
DDR3_DRAMRST#	Asynchronous output Reset signal to the DRAM devices. It is common to all ranks.	O	DDR3

Table 2-9. Reset and Miscellaneous Signal (Sheet 1 of 2)

Signal Name	Description	Direction	Type
PWROK/ DDR3_VCCA_PWROK	PowerOK: Asserted once the VRM is settled. Used primarily in the DDR PHY to determine S3.	I	CMOS
HPLL_REFCLK_P, HPLL_REFCLK_N	Differential refclk for the Intel Atom Processor D2000 series and N2000 series processor's HPLL. The "_P" signal corresponds to the rising edge of the internal clock. 100 MHz. 100 MHz	I	CMOS

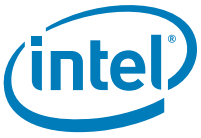


Table 2-9. Reset and Miscellaneous Signal (Sheet 2 of 2)

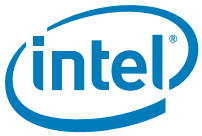
Signal Name	Description	Direction	Type
RESET#	Reset: Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be de-asserted prior to RESET# de-assertion.	I	CMOS
RSVD_*	Reserved. Must be left unconnected on the board. Intel does not recommend a test point on the board for this ball.	NC	
RSVD_TP_*	Reserved-test-point. A test point may be placed on the board for this ball.	I/O	

NOTE: RSVD_* numbering needs to be observed for BSDL testing purposes.

2.3 DMI - Direct Media Interface

Table 2-10.DMI - Processor to Intel NM10 Express Chipset Serial Interface

Signal Name	Description	Direction	Type
DMI_RXP[3:0] DMI_RXN[3:0]	DMI input from Intel NM10 Express Chipset: Direct Media Interface receive differential pair.	I	DMI
DMI_TXP[3:0] DMI_TXN[3:0]	DMI output to Intel NM10 Express Chipset: Direct Media Interface transmit differential pair.	O	DMI
DMI_RCOMP	Connects externally to a 7.5 kOhms pull-up to 1.5 V (DMI_REF1P5) This pin and the external resistor is used to set internal bias level. Package resistance must be less than 0.15 Ohms for this Bump.	I	-
DMI_REF1P5	current reference for DMI. Connects to 1.5 V	I	-



2.4 PLL Signals

Table 2-11.PLL Signals

Signal Name	Description	Direction	Type
DDR3_REFP DDR3_REFN	Differential DDR3 I/O Clock In	I	Diff Clk CMOS
HPLL_REFCLK_N HPLL_REFCLK_P	Differential Host Clock In	I	Diff Clk CMOS
DMI_REFCLKP DMI_REFCLKN	Differential DMI Clock In	I	Diff Clk CMOS
DPL_REFCLKN DPL_REFCLKP	Differential PLL Clock In. 27 MHz XTAL required to reduce error to <1000 ppm	I	Diff Clk CMOS
DPL_REFSSCLKN DPL_REFSSCLKP	Differential Spread Spectrum Clock In	I	Diff Clk CMOS

2.5 Analog Display Signals

Table 2-12.Analog Display Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
CRT_RED	RED Analog Video Output: this signal is a CRT analog video signal output from the internal color palette DAC. The DAC is designed to drive a double terminated 75 Ohm DC resistance without the need for external buffering. A dual 150 Ohm termination scheme is implemented on the board for optimal signal integrity: one 150 Ohm termination to ground placed in close proximity to the chip and one 150 Ohm termination resistor to ground placed in close proximity to the VGA connector. The equivalent DC resistance of the two 150 Ohm termination resistors with the 75 Ohm termination within the CRT display is 37.5 Ohms (DC).	O	Analog
CRT_GREEN	GREEN Analog Video Output: this signal is a CRT analog video signal output from the internal color palette DAC. The DAC is designed to drive a double terminated 75 Ohm DC resistance without the need for external buffering. A dual 150 Ohm termination scheme is implemented on the board for optimal signal integrity: one 150 Ohm termination to ground placed in close proximity to the chip and one 150 Ohm termination resistor to ground placed in close proximity to the VGA connector. The equivalent DC resistance of the two 150 Ohm termination resistors with the 75 Ohm termination within the CRT display is 37.5 Ohms (DC).	O	Analog
CRT_BLUE	BLUE Analog Video Output: this signal is a CRT analog video signal output from the internal color palette DAC. The DAC is designed to drive a double terminated 75 Ohm DC resistance without the need for external buffering. A dual 150 Ohm termination scheme is implemented on the board for optimal signal integrity: one 150 Ohm termination to ground placed in close proximity to the chip and one 150 Ohm termination resistor to ground placed in close proximity to the VGA connector. The equivalent DC resistance of the two 150 Ohm termination resistors with the 75 Ohm termination within the CRT display is 37.5 Ohms (DC).	O	Analog

Table 2-12.Analog Display Signals (Sheet 2 of 2)

Signal Name	Description	Direction	Type
CRT_IRTN	CRT_IRTN: this signal is the complement video signal output from the internal color palette DAC channels and this signal connects directly to the ground plane of the board	O	Analog
CRT_IREF	DAC_IREF Resistor: resistor for the internal color palette DAC reference circuit. A 649 Ohm 0.5% resistor is required to be connected between DAC_IREF and the board ground plane.	O	Analog
CRT_HSYNC	CRT Horizontal Synchronization: This signal is used as the vertical sync (polarity is programmable) or "sync interval". 3.3V output.	O	HVCMOS
CRT_VSYNC	CRT Vertical Synchronization: This signal is used as the vertical sync (polarity is programmable). 3.3V output.	O	HVCMOS
CRT_DDC_CLK	Monitor Control Clock	I/O	COD
CRT_DDC_DATA	Monitor Control Data	I/O	COD

2.6 LVDS Signals

Table 2-13.LVDS Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
LVDS_TXP[3:0]	Differential data output - positive	O	LVDS
LVDS_TXN[3:0]	Differential data output - negative	O	LVDS
LVDS_CLKP	Differential clock output - positive	O	LVDS
LVDS_CLKN	Differential clock output - negative	O	LVDS
LVDS_IBG	LVDS Reference Current. Need 2.37 kOhm (high precession type 1% or less) pull-down resistor	I	Ref
LVDS_VBG	Reserved. No connect.	I	Analog
LVDS_VREFH	VREFH: DC reference pin. DC reference pin can be connected to Vss.	I	Analog
LVDS_VREFL	VREFL: DC reference pin can be connected to Vss.	I	Analog
PANEL_VDDEN	LVDS or eDP panel power enable: Panel power enable control.	O	HVCMOS
PANEL_BKLTEN	LVDS or eDP panel backlight enable: Panel backlight enable control.	O	HVCMOS
PANEL_BKLTCTL	LVDS or eDP panel backlight brightness control: Panel brightness control.	O	HVCMOS
LVDS_CTRL_CLK	Display Data Channel clock: LVDS I2C backlight control: Some panels still support this, but most have gone to using PWM	I/O	COD

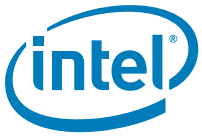


Table 2-13.LVDS Signals (Sheet 2 of 2)

Signal Name	Description	Direction	Type
LVDS_CTRL_DATA	Display Data Channel data: LVDS I2C backlight control: Some panels still support this, but most have gone to using PWM LVDS I2C EDID:	I/O	COD
LVDS_DDC_CLK	LVDS I2C EDID: LVDS Flat Panel I2C Clock and Data for EDID read and control. LVDS_DDC_DATA sampled as a pin-strap for LVDS port presence detect.	I/O	COD
LVDS_DDC_DATA	LVDS Flat Panel I2C Clock and Data for EDID read and control. I2C based control signal (data) for External SSC clock chip control. LVDS_DDC_DATA sampled as a pin-strap for LVDS port presence detect.	I/O	COD

2.7 DDI Audio Interface

Table 2-14.DDI Audio Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
AZIL_BCLK	Intel HD Audio BCLK: Bit Clock: 24.00-MHz clock sourced from the controller and connecting to all codecs on the Link.	I	CMOS
AZIL_RST#	Intel HD Audio Reset: Active low link reset signal. RST# is sourced from the controller and connects to all Codecs on the link. Assertion of RST# results in all link interface logic being reset to default power on state.	I	CMOS
AZIL_SYNC	Intel HD Audio SYNC: This signal marks input and output frame boundaries (frame synch) as well as identifies outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codecs on the link	I	CMOS

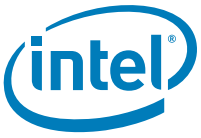
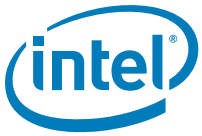


Table 2-14.DDI Audio Signals (Sheet 2 of 2)

Signal Name	Description	Direction	Type
AZIL_SDI	Intel HD Audio SDI - Serial Data In: Point-to-point serial data input signals driven by each codec (in this case the Intel Atom Processor D2000 series and N2000 series processor) to the controller. Data is single pumped; codecs drive SDI and the controller samples SDI with respect to the rising edge of BCLK. Controllers are required to support weak pull-down on all SDI signals. These pull-down are active whenever the controller is powered or in a wake enabled state. SDI pull-down are required to prevent spurious wake event in electrically noisy environments. Note: Although the name is misleading, the Intel Atom Processor D2000 series and N2000 series processor follows prior GMCH naming convention: the SDI pin on the GMCH/Intel Atom Processor D2000 series and N2000 series processor should connect to the SDI pin on the Intel HD Audio Controller/ICH. This is why this pin's direction is "I/O" - Input and Output.	I/O	CMOS
AZIL_SDO	Intel HD Audio SDO - Serial Data Out: one or more serial data output signal(s) driven by the Controller to all codecs on the link. Data is double pumped - i.e., the controller drives data onto SDO, and codecs sample data present on SDO with respect to every edge of BCLK. Note: Although the name is misleading, the Intel Atom Processor D2000 series and N2000 series processor follows prior GMCH naming convention: the SDO pin on the GMCH/Intel Atom Processor D2000 series and N2000 series processor should connect to the SDO pin on the Intel HD Audio Controller/ICH. This is why this pin's direction is Input ("I")	I	CMOS



2.8 DDI Port 0

Table 2-15.DDI Port 0

Signal Name	Description	Direction	Type
DDI0_TXP[3:0], DDI0_TXN[3:0]	PORT0: Capable of HDMI/DVI/DP HDMI/DVI: _TX[0]: TMDSB_DATA2 _TX[1]: TMDSB_DATA1 _TX[2]: TMDSB_DATA0 _TX[3]: TMDSB_BLK DP: _TX[0]: DPort Lane 0 (BLUE, HSYNC, VSYNC) _TX[1]: DPort Lane 1 (GRN, CTL0, CTL1) _TX[2]: DPort Lane 2 (RED, CTL2, CTL3) _TX[3]: DPort Lane 3	O	Diff
DDI0_AUXP, DDI0_AUXN	DP: Display port aux HDMI/DVI: Unused	I/O	Diff
DDI0_HPD	DDI0 Hot Plug Detect	I	CMOS
DDI0_DDC_SDA, DDI0_DDC_SCL	I2C Control Clock and Data. HDMI and DP dual mode DDI0_DDC_SDA sampled as a pin-strap for HDMI/DVI/DP port presence detect.	I/O	OD
BREFREXT	Connects externally to a 7.5 kOhms ±1% Pull up to a 1.50 V ±5% voltage supply (BREF1P5). This pin and the external resistor is used to set internal bias levels.	N/A	Analog
BREF1P5	Reference Voltage: Connects externally to a 1.50 V ±5% voltage supply. Needed to create voltage references. Used also as supply for all ESD & Clamp connections. **NOTE**: This connects to 1.50 V not 1.80 V.	I	Analog
DPL_REFCLKP, DPL_REFCLKN	Fixed (non-SSC) Display PLL Reference: 27 MHz XTAL, 96 MHz, 100 MHz 96 & 100 MHz: Result in <= 5000 ppm error (1 Judder event every X sec). 27 MHz XTAL: Result in <= 1000 ppm error (1 Judder event every X sec).	I	Diff

2.9 DDI Port1

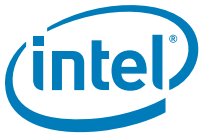
Table 2-16.DDI Port 1

Signal Name	Description	Direction	Type
DDI1_TXP[3:0], DDI1_TXN[3:0]	PORT1: Capable of HDMI/DVI/DP/eDP HDMI/DVI: TX[0]: TMDSB_DATA2 TX[1]: TMDSB_DATA1 TX[2]: TMDSB_DATA0 TX[3]: TMDSB_BLK eDP/DP: TX[0]: DPort Lane 0 (BLUE, HSYNC, VSYNC) TX[1]: DPort Lane 1 (GRN, CTL0, CTL1) TX[2]: DPort Lane 2 (Red, CTL2, CTL3) TX[3]: DPort Lane 3	O	Diff
DDI1_AUXP, DDI1_AUXN	DP: Display port aux HDMI/DVI: Unused	I/O	Diff
DDI1_HPD	DDI1 Hot Plug Detect	I	OD
DDI1_DDC_SDA, DDI1_DDC_SCL	I2C Control Clock and Data. HDMI and DP dual mode DDI1_DDC_SDA sampled as a pin-strap for HDMI/DVI/DP port presence detect.	I/O	OD
DPL_REFSSCCLKP, DPL_REFSSCCLKN	SSC Display PLL Reference: 100 MHz SSC (Spread Spectrum Clocking)	I	Diff

2.10 JTAG / ITP Signals

Table 2-17.JTAG / ITP Signals

Signal Name	Description	Direction	Type
TCLK	TCLK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	I	CMOS
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I	CMOS
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O	OD
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.	I	CMOS
TRST#	TRST_B (Test Reset) resets the Test Access Port (TAP) logic.	I	CMOS



2.11 Error and Thermal Protection

Table 2-18.Error and Thermal Protection

Signal Name	Description	Direction	Type
PROCHOT#	**Processor Hot**: Asserted if any Intel Atom Processor D2000 series and N2000 series processor thermal sensor (one in each CPU and one in the MCH) indicates the part is hot. If any of these sensors trip or if the external pin is asserted, all sensors act as if the pin was asserted. Each sensor can be programmed to cause various actions on assertion or deassertion such as: an interrupt (SCI, SMI, MSI for example), 2x DDR self refresh mode, DDR bandwidth throttling, CPU or GFX performance throttling. In Deep Power Down Technology (code named C6), the CPU's prochot output will automatically deassert. The bi-directional nature of the pin (ability for system to assert the signal), allows a system design to protect various external components from overheating situations. PMIC/VR, ICH, or external logic can choose to drive this in the event it's overheating to reduce vcc_cpu and vcc_GFX current consumption.	I/O	I: CMOS O: OD
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 C. This is signaled to the system by the THERMTRIP# pin.	O	Open Drain

2.12 Processor Core Power Signals

Table 2-19.Processor Core Power Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
VCC_CPU	Processor core power supply. The voltage supplied to these pins is determined by the VID pins.		PWR
VCC_CPUSENSE	VCC_CPUSENSE and VSS_CPUSENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog
VSS_CPUSENSE	VCC_CPUSENSE and VSS_CPUSENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog

Table 2-19.Processor Core Power Signals (Sheet 2 of 2)

Signal Name	Description	Direction	Type
SVID_ALERT#	sVID Alert: Used by the VR to signal the prior request has not reach the requested operating point.	I	OD
SVID_DATA	sVID Data: Used by Intel Atom Processor D2000 series and N2000 series processor to send request and data to the VR and then by the VR to respond. Data is driven with a 12.5 Ohms Pull Down.	I/O	OD
SVID_CLK	sVID Clock: sVID request are driven out on SVID_DATA using this as the clock and are then registered in the VR using this for the clock. When the VR responds with data on SVID_DATA, it also uses this clock (still sent by Intel Atom Processor D2000 series and N2000 series processor) to drive the data. This means the VR starts driving data/alert using a clock that is late (by the Intel Atom Processor D2000 series and N2000 series processor->VR flight time + VR setup time). Clock is driven with a 12.5 Ohms PD. Frequency: 25 MHz when using DDR3-800 26 MHz with DDR3-1066	O	OD

2.13 Graphics, DMI and Memory Core Power Signals

Table 2-20.Power Signals (Sheet 1 of 2)

Signal Name	Description	Direction / V	Type
VCCAZILAON	Audio Power Supply	3.3	PWR
VCC_GFX	Graphics core power supply - D2000 series Graphics core power supply - D2000 series	0.75-1.05 1.05	PWR
V_SM	DDR I/O power supply	1.5(DDR3) 1.35(DDR3L)	PWR
VCCADMI_SFRPLL	DMI SFR PLL power supply	1.5	PWR
VCCADMI	DMI I/O power supply	1.05	PWR
VCCADAC	CRT/VGA DAC power supply	1.8	PWR
VCCTHRM	GFX, CPU0 and CPU1 Thermal Sensor power supply	1.8	PWR
VCCADP	DDI I/O power supply	1.05	PWR
VCCADP_0	Display PLLs SFR power Supply	1.5	PWR
VCCADP_1	Display PLLs SFR power Supply	1.5	PWR
VCCAGPIO	GPIO power supply	3.3	PWR
VCCRAMXXX	CPU L2 Caches, DTS and Arrays Power Supply N2000 series D2000 series	 1.05 1.067	PWR
VCCDIO	CRT digital Voltage	1.05	PWR
VCCADLLDDR	DDR DLL power supply	1.05	PWR

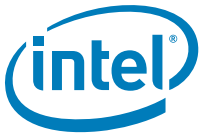


Table 2-20.Power Signals (Sheet 2 of 2)

Signal Name	Description	Direction / V	Type
VCCFHV	Graphic, CPU 1 and CPU 0 power supply	1.05	PWR
VCCAGPIO_LV	Low Voltage GPIO and LVDS Digital power supply	1.05	PWR
VCCAGPIO_REF	Reference Voltage to VCCAGPIO(3.3V) & VCCAGPIO_DIO (1.8V)	1.5	PWR
VCCAGPIO_DIO	Debug I/O power Supply	1.8	PWR
VCCADDR	DDR Digital power supply	1.05	PWR
VCCAHPLL	CPU0 and CPU1 Quiet power supply	1.05	PWR
VCCDLVDS	LVDS power supply	1.8	PWR
VCCALVDS	LVDS power supply	1.8	PWR
VCCSFRMPL	MPLL power supply	1.5	PWR
VCCACKDDR	DDR clock power supply	1.05	PWR
VCCDMPL	MPLL Digital power supply	1.05	PWR
VCCCKDDR	DDR clock power supply	1.5(DDR3) 1.35(DDR3L)	PWR

NOTE: N2000 series VCC_GFX is SVID controlled.

2.14 Ground

Table 2-21.Ground

Signal Name	Description	Direction	Type
VSS	VSS are the ground pins for the processor and should be connected to the system ground plane.		GND
VSSA_CRTDAC	This analog ground signal should connect directly to the board ground plane		GND
VSSGFX_sense	This signal can be left floating for D2000 series		GND

§

3 Functional Description

3.1 System Memory Controller

The system memory controller supports DDR3 protocols with one 64 bit wide single channel accessing two DIMMs. The controller supports a maximum of two non-ECC DDR3 SODIMMs or two un-buffered DDR3 DIMMs, single or double sided; thus allowing up to four device ranks. Refreshed SKU of Next Generation Intel Atom Processor based Mobile Platform Processors support DDR3/DDR3L.

3.1.1 System Memory Organization Modes

The system memory controller supports only one memory organization mode: single channel. In this mode, all memory cycles are directed to a single channel.

3.1.2 System Memory Technology Supported

The system memory controller supports the following DDR3/DDR3L Data Transfer Rates, DIMM Modules and DRAM Device Technologies:

- DDR3/DDR3L Data Transfer Rates: 800MT/s (6.4 GB/s) and 1066MT/s (8.5 GB/s)
- DDR3/DDR3L Memory Down Technology:
  - Raw Card B Type supported only.
- DDR3 SODIMM Modules (unbuffered, non-ECC)
  - Raw Card A = 2 rank of x16 SDRAM (double sided)
  - Raw Card B = 1 rank of x8 SDRAM (double sided)
  - Raw Card C = 1 rank of x16 SDRAM (single sided)
  - Raw Card F = 2 ranks of x8 SDRAM (double Sided)

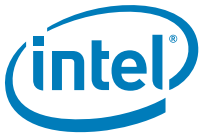
Note: x8 means that each SDRAM component has 16/8 data lines. x16 means that each SDRAM component has 16 data lines.

- DDR3/DDR3L DRAM Device Technology:

Standard 1-Gb and 2-Gb technologies and addressing are supported for both x8 and x16 devices. There is no support for SO-DIMMs with different technologies or capacities on opposite sides of the same SO-DIMM. If one side of a SO-DIMM is populated, the other side is either identical or empty.

- Supported DDR3/DDR3L SO-DIMM module configurations

"Single sided" above is a logical term referring to the number of Chip Selects attached to the DIMM. A real DIMM may put the components on both sides of the substrate, but be logically indistinguishable from single sided DIMM if all components on the DIMM are attached to the same Chip Select signal.



There is no support for DIMMs with different technologies or capacities on opposite sides of the same DIMM. If one side of a DIMM is populated, the other side is either identical or empty.

There is no support for 4Gb & 8Gb technology.

Supported components for DDR3/DDR3L at 800MTs and 1066 MTs.

Table 3-22.Support DRAM Devices

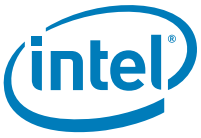
DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
1Gb	x8	8	BA[2:0]	A[13:0]	A[9:0]	1KB
2Gb	x8	8	BA[2:0]	A[14:0]	A[9:0]	1KB
1Gb	x16	8	BA[2:0]	A[12:0]	A[9:0]	2KB
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB

Table 3-23.Supported Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
1GB	8	1Gb	x8	8KB = 1KB * 8 chips
2GB	8	2Gb	x8	8KB = 1KB * 8 chips
512MB	4	1Gb	x16	8KB = 2KB * 4chips
1GB	4	2Gb	x16	8KB = 2KB * 4 chips

Table 3-24.Support Memory Configurations

DRAM Chip Density (Gb)	Memory Size (MB)	# of chips needed	DRAM Chip Data Width	Data Bus Width	# of Ranks needed	# of chips /rank
1	512	4	16	64	1	4
1	1024	8	8	64	1	8
1	1024	8	16	64	2	4
1	2048	16	8	64	2	8
2	1024	4	16	64	1	4
2	2048	8	8	64	1	8
2	2048	8	16	64	2	4
2	4096	16	8	64	2	8



3.1.3 Rules for populating DIMM Slots

The frequency of system memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs. Timing parameters [CAS latency (or CL + AL for DDR3), tRAS, tRCD, tRP] must be programmed to match within a channel.

3.2 Graphics Processing Unit

Intel Atom Processor D2000 series and N2000 series contains an integrated graphics engine, video decode and a display controller that supports two pipes to LVDS, CRT, HDMI/DVI, DP, eDP.

3.2.1 3-D Core Key Features

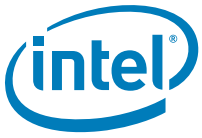
The Intel Atom Processor D2000 series and N2000 series GPU 3D has two pipe scalable unified shader implementation.

  - 3-D Peak Performance
  - Fill Rate: 4 Pixels per clock
  - Vertex Rate: One Triangle 8 clocks (Transform Only)
  - Vertex / Triangle Ratio average = 1 vtx/tri, peak 0.5 vtx/tri
- Texture max size = 2048 x 2048
- Programmable 4x and 2x multi-sampling anti-aliasing (MSAA)
  - Rotated grid
  - ISP performance related to AA mode, TSP performance unaffected by AA mode
- Optimized memory efficiency using multi-level cache architecture
- Optimized memory efficiency using multi-level texture cache architecture

3.2.1.1 Shading Engine Key Features

The unified pixel/vertex shader engine supports a broad range of instructions.

- Unified programming model
  - Multi-threaded with 16 concurrently running threads and up to 64 data simultaneous instances
  - Zero-cost swapping in/out of threads
  - Cached program execution model – max program size 262144 instructions
  - Dedicated pixel processing instructions
  - Dedicated vertex processing instructions
  - 4096 32-bit registers and 48 40-bit registers
  - 3-way 10 bit integer and 4-way 10 bit integer operations
- SIMD pipeline supporting operations in:



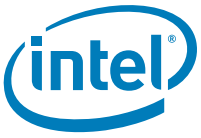
  - 32-Bit IEEE Float
  - 2-way, 16-bit fixed point
  - 4-way, 8-bit integer
  - 32-bit integer
  - 32-bit, bit-wise (logical only)
- Static and Dynamic flow control
  - Subroutine calls
  - Loops
  - Conditional branches
  - Zero-cost instruction predication
- Procedural Geometry
  - Allows generation of more primitives on output compared with input data
  - Effective geometry compression
  - High order surface support
- External data access
  - Permits reads from main memory by cache (can be bypassed)
  - Permits writes to main memory
  - Data fence facility provided
  - Dependent texture reads

3.2.1.2 Vertex Processing

Modern graphics processors perform two main procedures to generate 3-D graphics. First, vertex geometry information is transformed and lit to create a 2-D representation in the screen space. Those transformed and lit vertices are then processed to create display lists in memory. The pixel processor then rasterizes these display lists on a regional basis to create the final image.

The Intel Atom Processor D2000 series and N2000 series integrated graphics supports DMA data accesses from SDRAM. DMA accesses are controlled by a main scheduler and data sequencer engine. This engine coordinates the data and instruction flow for the vertex processing, pixel processing, and general purpose operations.

Transform, lighting, and tiling operations are performed by the vertex processing pipeline. A 3-D object is usually expressed in terms of triangles, each of which is made up of three vertices defined by X-Y-Z coordinate space. The transform and lighting process is performed by processing data through the unified shader core. The results of this process are sent to the pixel processing function. The steps to transform and light a triangle or vertex are explained below.



3.2.1.2.1 Vertex Transform Stages

- **Local space:** relative to the model itself (e.g., using the model centre at reference point). Prior to being placed into a scene with other objects.
- **World space:** transform LOCAL to WORLD: this is needed to bring all objects in the scene together into a common coordinate system.
- **Camera space:** transform WORLD to CAMERA (also called EYE): this is required to transform the world in order to align it with camera view. In OpenGL, the local to world and world to camera transformation matrix is combined into one, called the ModelView matrix.
- **Clip space:** transform CAMERA to CLIP: The projection matrix defines the viewing frustum onto which the scene will be projected. Projection can be orthographic, or perspective. Clip is used because clipping occurs in clip space.
- **Perspective space:** transform CLIP to PERSPECTIVE: The perspective divide is basically what enables 3-D objects to be projected onto a 2-D space. A divide is necessary to represent distant objects as smaller on the screen. Coordinates in perspective space are called normalized device coordinates ([-1,1] in each axis).
- **Screen space:** transform PERSPECTIVE to SCREEN: this is where 2-D screen coordinates are finally computed, by scaling and biasing the normalized device coordinates according to the required render resolution.

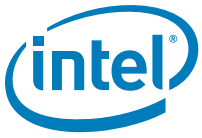
3.2.1.2.2 Lighting Stages

Lighting is used to generate modifications to the base color and texture of vertices; examples of different types of lighting are:

- **Ambient** lighting is constant in all directions and the same color to all pixels of an object. Ambient lighting calculations are fast, but objects appear flat and unrealistic.
- **Diffuse** lighting takes into account the light direction relative to the normal vector of the object's surface. Calculating diffuse lighting effects takes more time because the light changes for each object vertex, but objects appear shaded with more three-dimensional depth.
- **Specular** lighting identifies bright reflected highlights that occur when light hits an object surface and reflects back toward the camera. It is more intense than diffuse light and falls off more rapidly across the object surface. Although it takes longer to calculate specular lighting than diffuse lighting, it adds significant detail to the surface of some objects.
- **Emissive** lighting is light that is emitted by an object, such as a light bulb.

3.2.1.3 Pixel Processing

After vertices are transformed and lit by the vertex processing pipeline, the pixel processor takes the vertex information and generates the final rasterized pixels to be displayed. The steps of this process include removing hidden surfaces, applying textures and shading, and converting pixels to the final display format. The vertex/pixel shader engine is described in Unified Shader.



The pixel processing operations also have their own data scheduling function that controls image processor functions and the texture and shader routines.

3.2.1.3.1 Hidden Surface Removal

The image processor takes the floating-point results of the vertex processing and further converts them to polygons for rasterization and depth processing. During depth processing, the relative positions of objects in a scene, relative to the camera, are determined. The surfaces of objects hidden behind other objects are then removed from the scene, thus preventing the processing of un-seen pixels. This improves the efficiency of subsequent pixel-processing.

3.2.1.3.2 Applying Textures and Shading

After hidden surfaces are removed, textures and shading are applied. Texture maps are fetched, mipmaps calculated, and either is applied to the polygons. Complex pixel-shader functions are also applied at this stage.

3.2.1.3.3 Final Pixel Formatting

The pixel formatting module is the final stage of the pixel-processing pipeline and controls the format of the final pixel data sent to the memory. It supplies the unified shader with an address into the output buffer, and the shader core returns the relevant pixel data. The pixel formatting module also contains scaling functions, as well as a dithering and data format packing function.

3.2.1.4 Unified Shader

The unified shader engine contains a specialized programmable microcontroller with capabilities specifically suited for efficient processing of graphics geometries (vertex shading), graphics pixels (pixel shading), and general-purpose video and image processing programs. In addition to data processing operations, the unified shader engine has a rich set of program-control functions permitting complex branches, subroutine calls, tests, etc., for run-time program execution.

The unified shader core also has a task and thread manager which tries to maintain maximum performance utilization by using a 16-deep task queue to keep the 16 threads full.

The unified store contains 16 banks of 128 registers. These 32-bit registers contain all temporary and output data, as well as attribute information. The store employs features which reduce data collisions such as data forwarding, pre-fetching of a source argument from the subsequent instruction. It also contains a write back queue.

Like the register store, the arithmetic logic unit (ALU) pipelines are 32-bits wide. For floating-point instructions, these correlate to IEEE floating point values. However, for integer instructions, they can be considered as one 32-bit value, two 16-bit values, or four 8-bit values. When considered as four 8-bit values, the integer unit effectively acts like a four-way SIMD ALU, performing four operations per clock. It is expected that in legacy applications pixel processing will be done on 8-bit integers, roughly quadrupling the pixel throughput compared to processing on float formats.

3.2.1.4.1 Multi Level Cache

The multi-level cache is a three-level cache system consisting of two modules, the main cache module and a request management and formatting module. The request management module also provides Level-0 caching for texture and unified shader core requests.

The request management module can accept requests from the data scheduler, unified shaders and texture modules. Arbitration is performed between the three data streams, and the cache module also performs any texture decompression that may be required.

3.2.2 2D Engine

3.2.2.1 VGA Registers

The 2D registers are a combination of registers defined for the original Video Graphics Array (VGA) and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

3.2.2.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

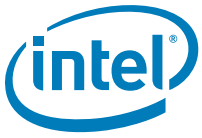
Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the graphics controller can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.



The graphics controller has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The graphics controller can perform hardware clipping during BLTs.

3.2.3 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

Table 3-25.Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage Range	0.7 Vp-p nominal only
	CRT/Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	3.3 V
	Enable/Disable	Port control
	Polarity Adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	External buffered to 5 V
	Control	Through GPIO interface

3.2.3.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. CPU's integrated 350 MHz RAMDAC supports resolutions up to 1920 x 1200 @ 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the CRT display.

3.2.3.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

3.2.3.3 VESA / VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

3.2.3.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and DDC 2 is implemented. The CPU uses the CRT_DDC_CLK and CRT_DDC_DATA signals to communicate with the analog monitor. The CPU will generate these signals at 3.3V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The CPU implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 100 kHz.

3.2.4 Digital Display Interfaces

The Intel Atom Processor D2000 series and N2000 series can drive HDMI, LDVS, eDP and Display Port natively. The digital ports B and or C can be configured to drive HDMI, DVI and Display Port. The digital ports are muxed onto the PEG interface.

Since Intel Atom Processor D2000 series and N2000 series has two display ports available for its two pipes, it can support up to two different images on two different display devices. Timings and resolutions for these two images may be different.

3.2.4.1 LVDS

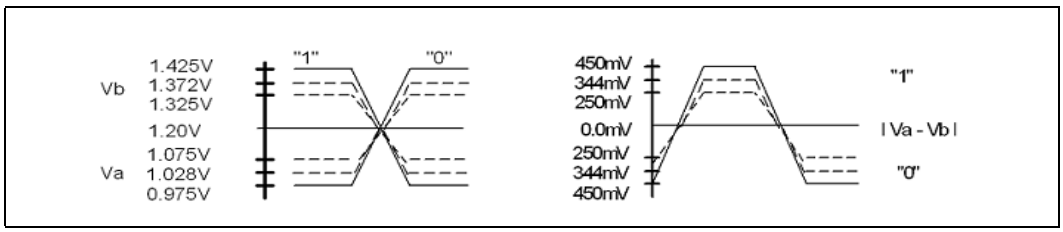
LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics.

Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input.

There is one LVDS transmitter channel consist of 4-data pairs and a clock pair each. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

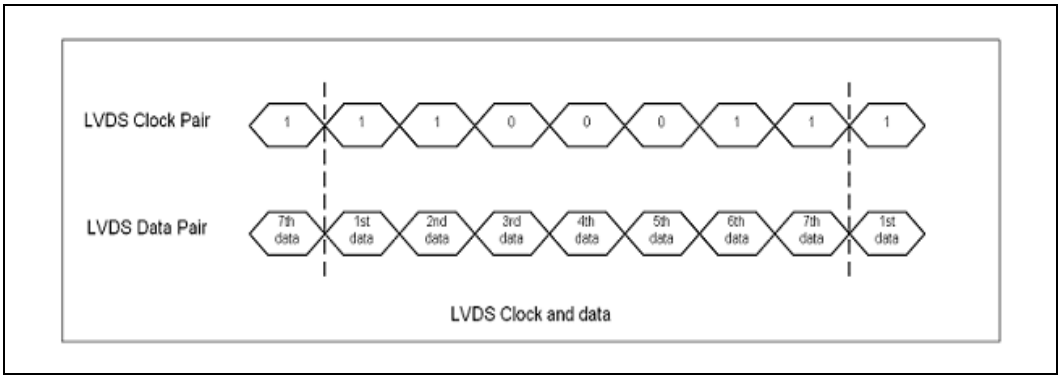
Figure below shows a pair of LVDS signals and swing voltage.

Figure 3-2. LVDS Signals and Swing Voltage



1s and 0s are represented the differential voltage between the pair of signals. As shown in the figure below a serial pattern of 1100011 represents one cycle of the clock.

Figure 3-3. LVDS Clock and Data Relationship



3.2.4.2 LVDS Pair States

The LVDS pairs can be put into one of five states:

- Active
- Powered down tri-state
- Powered down 0-V
- Send zeros

When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0-V or tri-states on both the output pins for the entire channel. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

The LVDS Port can be enabled/disabled using software. A disabled port enters a low power state. Once the port is enabled, individual driver pairs may be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0s output.

Individual pairs or sets of LVDS pairs can be selectively powered down when not being used. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

3.2.4.3 Single Channel Mode

In Single Channel mode, Channel A can take 18 bits of RGB pixel data, plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB (plus 4 bits of timing control) output on four differential data pair outputs. A dual channel interface converts 36 or 48 bits of color information plus the 3 or 4 bits of timing control respectively and outputs it on six or eight sets of differential data outputs respectively.

Note: Platforms using the ICH for integrated graphics support 24 bpp display panels of Type 1 only (compatible with VESA LVDS color mapping).

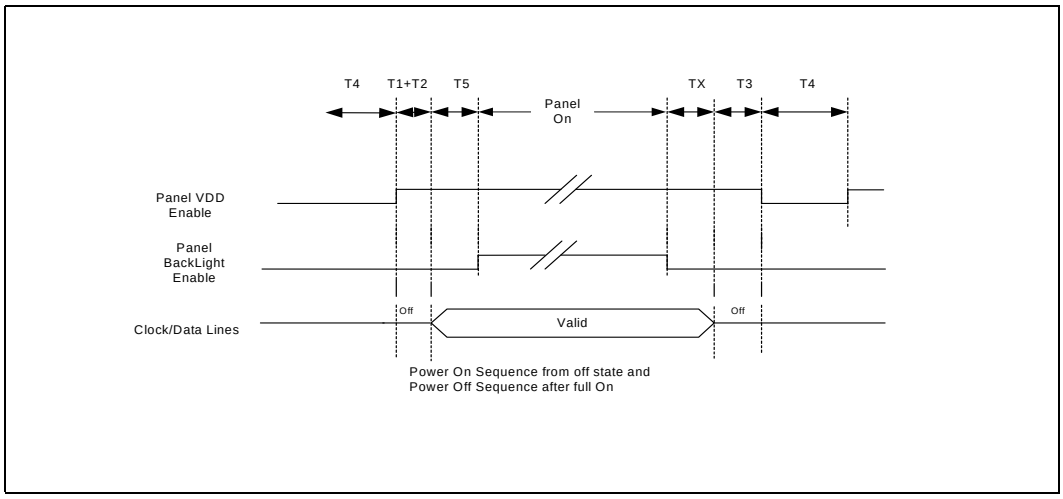
3.2.4.4 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. To meet the panel power timing specification requirements two signals, LFP_VDD_EN and LFP_BKLT_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 3-4. Panel Power Sequencing



Note: Support for programming parameters TX and T1 through T5 using software is provided.

Table 3-26. Panel Power Sequence Timing Parameters

Panel Power Sequence Timing Parameters			Min	Max	Name	Unit
Spec Name	From	To				
VDD On	0.1 VDD	0.9 VDD	0	10	T1	ms
LVDS active	VDD stable on	LVDS active	0	50	T2	ms
Backlight	LVDS active	Backlight on	200		T5	ms
Backlight state	Backlight off	LVDS off	x	x	TX	ms
LVDS state	LVDS off	Start power off	0	50	T3	ms
Power cycle delay	Power Off	Power on sequence start	0	400	T4	ms

3.2.4.5 LVDS DDC

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then 'locked' into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA.

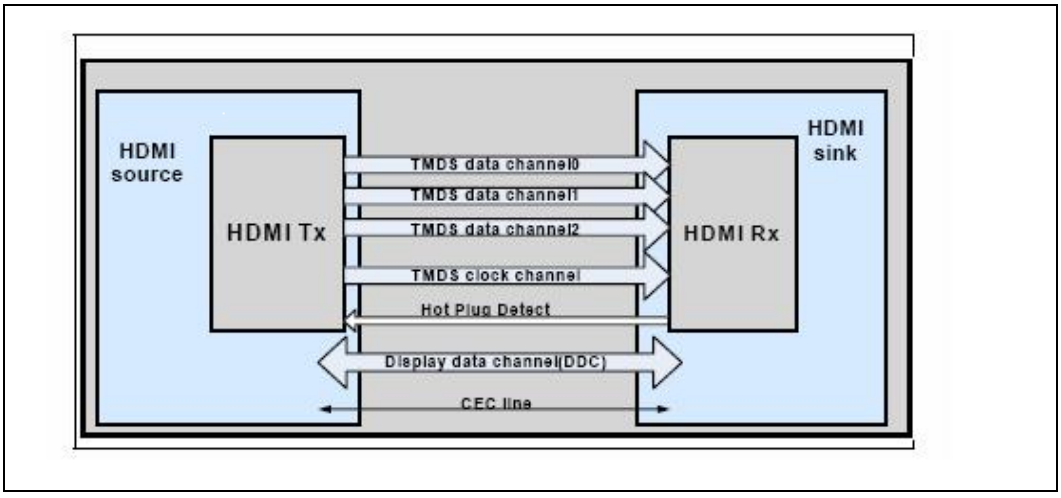
3.2.4.6 High Definition Multimedia Interface HDMI)

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the PCH and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). As shown in Figure 3-5, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA Display data channel (DDC). The DDC channel is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifter to convert the AC coupled signals to the HDMI compliant digital signals.

Figure 3-5. HDMI Overview



3.2.4.7 Digital Video Interface (DVI)

The PCH digital ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but the audio and CEC. Refer to the Section 3.2.4.6, "High Definition Multimedia Interface HDMI)" for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals is connected along with the digital data and clock signals from one of the digital port. When a system has support for DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

The digital display data signals driven natively through the Intel Atom Processor D2000 series and N2000 series are AC coupled and needs level shifter to convert the AC coupled signals to the HDMI compliant digital signals.

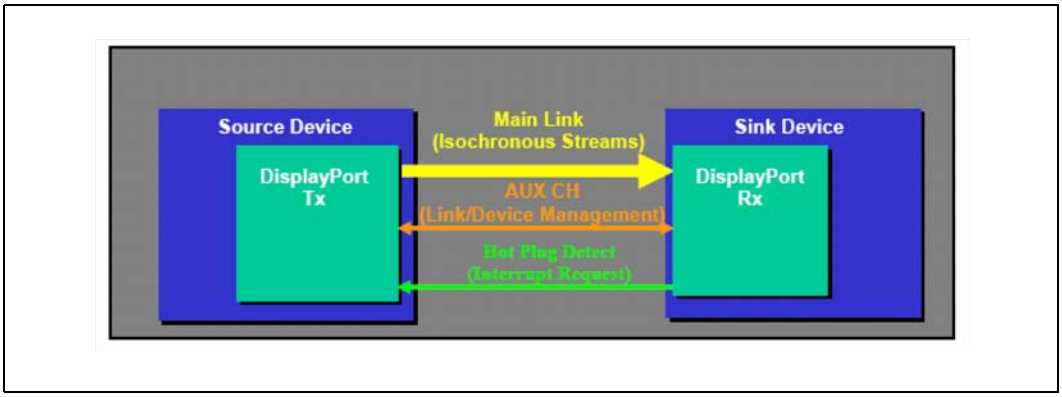
3.2.4.8 Display Port

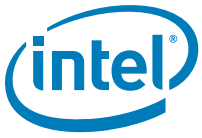
Display Port is a digital communication interface that utilizes differential signalling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video*. The Auxiliary Channel (AUX CH) is a half-duplex bi-directional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

Note: Audio is not supported on Display Port on the D2000 series and N2000 series processors

Figure 3-6. DP Overview





3.2.4.9 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP*) is a embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. eDP is supported only on Digital Display Port 1. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

The eDP support on Intel Atom Processor D2000 series and N2000 series is possible because of the addition of the panel power sequencing pins: PANEL_VDD, PANEL_BKLT_EN and PANEL_BLKT_CTRL.

The Intel Atom Processor D2000 series and N2000 series supports Embedded DisplayPort* (eDP*) Standard Version 1.1.

3.2.4.10 DisplayPort Aux Channel

A bi-directional AC coupled AUX channel interface replaces the I2C for EDID read, link management and device control. I2C-to-Aux bridges are required to connect legacy display devices.

3.2.4.11 DisplayPort Hot-Plug Detect (HPD)

The Intel Atom Processor D2000 series and N2000 series support HPD for Hot-Plug sink events on the HDMI and DisplayPort interface.

3.2.4.12 Blu-Ray* - HDCP (D2550, D2700 & N2800 SKU Only)

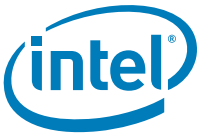
The HDCP Unit implements the industry standard HDCP (High-bandwidth Digital Content Protection) link protection protocol as specified by the Digital Content Protection, LLC organization. This implementation is based on version 1.1 of the specification, which includes references necessary to apply HDCP to HDMI as well as DP.

This unit's end result is to provide a 24-bit Cipher stream, which is used to encrypt the data sent to user-accessible digital output port(s). This key value changes each video pixel to produce a snowy image when the receiver is not synchronized to the transmitter (SOC). The key value is specific to each receiver, and as such the HDCP function can only be applied to one port at a time in this configuration. The video data and data-island periods (audio) are encrypted, whereas sync and control information is not. This allows the receiver to synchronize to the stream, even if the results are scrambled.

3.2.4.13 PAVP (Protected Audio and Video Path)

The Intel Atom Processor D2000 series and N2000 series PAVP provided a protected path between application and Intel Atom Processor D2000 series and N2000 series hardware decoder for media player applications that implements a compatible key exchange and data encryption scheme.

The application processed the AACS or DRM encrypted contents with the embedded AACS or DRM keys then immediately encrypted contents with a session key that was communicated with the Intel Atom Processor D2000 series and N2000 series. The PAVP



encrypted contents can be stored in unprotected memory. When hardware decoder requests the encrypted compressed video stream the data will pass through AES engine and decrypted by it. The clear data are then forwarded directly to video decoder unit. During video decoding process video decoder temporarily store some video parameters and uncompressed pictures to system memory for its own reference, post processing by graphic engine, or send to output interface by display controller. The uncompressed pictures have less value and can be protected software mechanism provided by OS.

The application should employed Tamper Resistance Software (TRS) mechanisms to protect attacks by debugger and other similar schemes when processing the above steps.

3.2.5 Multiple Display Configurations

Microsoft Windows 7* operating systems supports for multi-monitor display. Since the Intel Atom Processor D2000 series and N2000 series has several display ports available for its two pipes, it can support up to two different images on different display devices.

Timings and resolutions for these two images may be different. The Intel Atom Processor D2000 series and N2000 series supports Dual Display Clone and Extended Desktop.

Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

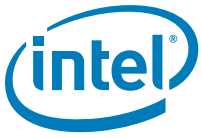
Extended Desktop uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows Desktop by utilizing both displays as a work surface.

3.3 Thermal Sensor

There are several registers that need to be configured to support the uncore thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point as protection for the CPU. If the Catastrophic Trip Point is crossed, then the CPU will instantly turn off all clocks inside the device. Customers may optionally enable the Hot Trip Point to generate SMI#. Customers will be required to then write their own SMI# handler in BIOS that will speed up the CPU (or system) fan to cool the part.

3.3.1 PCI Device 0, Function 0

The SMICMD register requires that a bit be set to generate an SMI# when the Hot Trip point is crossed. The ERRSTS register can be inspected for the SMI alert.



Address	Register Symbol	Register Name	Default Value	Access
C8-C9	ERRST	Error Status	0000h	RWC/S, RO
CC-CDh	SMICMD	SMI Command	0000h	RO, R/W

3.4 Power Management

The CPU uncore has many permutations of possibly concurrently operating modes. Care should be taken (Hardware and Software) to disable unused sections of the silicon when this can be done with sufficiently low performance impact. Refer to Chapter 6, "Signal Quality Specifications" and the *ACPI Specification*, *Rev3.0* for more detail.

3.4.1 Interface Power States Supported

Table 3-27.Main Memory States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge power down	KE De-asserted; All banks Closed; Not a self-refresh Mode. Supported only the fast (DLL ON) exit Mode
Active power down	CKE De-asserted; At least one bank active; Not a self-refresh Mode. Supported only the fast (DLL ON) exit Mode

3.4.2 Intel® Hyper-Threading Technology

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), which allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled via the BIOS and requires operating system support.

Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7* and disabling Hyper- Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see http:// www.intel.com/products/ht/hyperthreading_more.htm.

§

4 Electrical Specifications

Note: All data and specifications for DDR3/DDR3L in this chapter are based on post-silicon/ validation data. These specifications will be updated with characterized data from silicon measurements in the later version of the EDS spec document.

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification and power sequencing. The chapter also includes DC and AC specifications, including timing diagrams.

4.1 Power and Ground Balls

The processor has V_{CC} and V_{SS} (ground) inputs for on-chip power distribution. All power balls must be connected to their respective processor power planes, while all V_{SS} balls must be connected to the system groundplane. Use of multiple power and ground planes is recommended to reduce I*R drop. The V_{CC} balls must be supplied with the voltage determined by the processor Voltage IDentification (VID) signals.

4.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full-power states. This may cause voltages on power planes to sag below their minimum values, if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand (for example, coming out of an idle condition). Similarly, capacitors act as a storage well for current when entering an idle condition from a running condition. To keep voltages within specification, output decoupling must be properly designed.

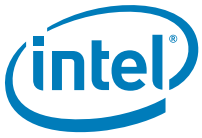
Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications. Failure to do so can result in timing violations or reduced lifetime of the processor. For further information and design guidelines.

4.2.1 Voltage Rail Decoupling

The voltage regulator solution needs to provide:

- Bulk capacitance with low effective series resistance (ESR).
- A low path impedance from the regulator to the CPU.
- Bulk decoupling to compensate for large current swings generated during power-on, or low-power idle state entry/exit.

The power delivery solution must ensure that the voltage and current specifications are met, as defined in Table 4-32.



4.3 Processor Clocking

BCLKP, BCLKN, HPL_CLKINP, HPL_CLKINN, EXP_CLKINP, EXP_CLKINN, DPL_REFCLKINP, DPL_REFCLKINN

The processor utilizes differential clocks to generate the processor core(s) and uncore operating frequencies, memory controller frequency, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by 100 or 133 MHz. Clock multiplying within the processor is provided by an internal phase locked loop (PLL), which requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC).

HPLL, DMIPLL and MPLL expecting the reference source clock will be generated by the same PLL and SS logic in the external clock generation

Table 4-28.PLL Reference Clock

PLL Reference	Pins / Balls	Frequency	Description
Host PLL (HPLL)	HPLL_REFCLK_P, HPLL_REFCLK_N	100 MHz	Drives all MCH core clocks, Gfx, Video, Display and provides reference for CPU PLLs.
DDRIO PLL (MPLL)	DDR3_REFCLKP, DDR3_REFCLKN	100 MHz	DDRIO PLL must be matched to clock DDR at the same transfer rate as fused for HPLL.
DMIIO PLL (DMIPLL)	DMI_IREFCLKP, DMI_IREFCLKN	100 MHz	For the DMI interface to the ICH which operates at Gen1 speeds.
Display I/O Fixed Ref Clock (DPLL0)	DPL_REFCLKP, DPL_REFCLKN	27 XTAL, 96, 100 Fixed Frequency.	27 MHz XTAL required to reduce error to <1000 ppm. DPLL0 is non SSC clock
Display I/O SSC Ref Clock (DPLL1)	DPL_REFSSCCLKP, DPL_REFSSCCLKN	100 SSC.	If SSC is used for display, it must be connected at this pins. SSC enables better emissions testing performance (EMI) at the system level. Internally DPLL0 and DPLL1 can use each others' reference clock.
CPU Core PLLs (CPLL)	NONE	N/A	Derived from HPLL.

4.3.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 4-32 for DC specifications and to the Platform Design Guide for decoupling and routing guidelines.

4.4 Voltage Identification (VID)

The Intel Atom Processor D2000 series and N2000 series processor supports Serial VID based power delivery for CPU core and Graphic Core. The Next Generation Intel® Atom™ Processor based desktop platform will support Intel MVP 7 1+1 for Core & Gfx / Vnn VR.

While for Entry Level Desktop Customer option will be provided to choose either Intel Mobile Voltage Positioning (IMVP) 7 1+1 for core & gfx/ Vnn or VR12/ IMVP7 1 +0 for core and fixed Voltage LVR for Gfx/ Vnn (VR12) 1 +0 could be chapter and preferred solution.

The VID specifications for the processor VCC_CPU and VCC_GFX are defined by the IMVP 7 Voltage Regulator Controller Design Guidelines. The processor uses three signals for the serial voltage identification interface to support automatic selection of voltages. Table 4-29 specifies the voltage level corresponding to the eight bit VID value transmitted over serial VID. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. VID signals are CMOS push/ pull drivers. Refer to Table 4-34 for the DC specifications for these signals. The VID codes will change due to temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Table 4-30. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 4-30. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 1 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000

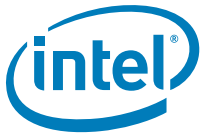


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 2 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500

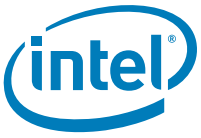


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 3 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000

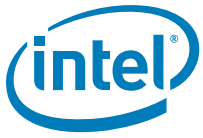


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 4 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500

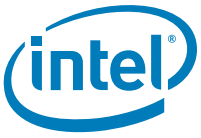


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 5 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	0	0	1	0	0	0	0	8	0	0.88500
1	0	0	1	0	0	0	1	8	1	0.89000
1	0	0	1	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	0	0	0	0	0	9	0	0.96500
1	0	0	0	0	0	0	1	9	1	0.97000
1	0	0	0	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	1	0	0	0	0	A	0	1.04500
1	0	1	1	0	0	0	1	A	1	1.05000

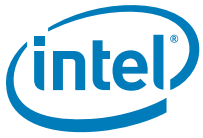


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 6 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
1	0	1	1	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	0	0	0	0	0	B	0	1.12500
1	0	1	0	0	0	0	1	B	1	1.13000
1	0	1	0	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500

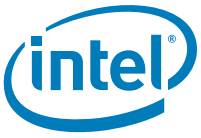


Table 4-29.VRD 12.0 Voltage Identification Definition (Sheet 7 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	VCC (V)
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	1	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	0	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	1	0	0	D	0	1.28500
1	1	0	1	0	1	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000

4.5 Catastrophic Thermal Protection

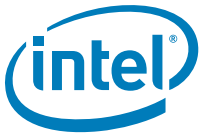
The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 degree Celsius (maximum), or the THERMTRIP# signal is asserted, the Vcc supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to the thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

4.6 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to V_{CC}, V_{SS}, or to any other signal (including each other) may result in component malfunction. Refer to Chapter 2 for a land listing of the processor and the location of all reserved signals.



For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines.

4.7 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Chapter 2. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. Refer to Section 4.9 for the DC and AC specifications.

4.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

4.9 DC Specifications

Section 4.9 list the DC specifications for the processor and are valid only while meeting the thermal specifications (as specified in the Thermal / Mechanical Specifications and Guidelines), clock frequency, and input voltages. Table 4-32 lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

4.9.1 Flexible Motherboard Guidelines (FMB)

This is not applicable for D2000 series and N2000 series Next Generation Intel® Atom™ Processor based desktop platform.

4.9.2 Voltage and Current Specifications

Table 4-30 and Table 4-32 list the DC specifications for the processor core and I/O buffer; they are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deeper Sleep state. VCC,BOOT is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at TJ = 100°C. Care should be taken to read all notes associated with each parameter.

Table 4-30. Processor Core Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	I_TDC	Unit	Note
VID	VID Range	0.91		1.21		V	
V_{CC}	V_{CC} for processor core	Refer to Table 4-29 and Figure 4-7 0.00000- 1.21				V	2, 3
$V_{CC,BOOT}$	Default V_{CC} voltage for initial power up	1.0945	1.1	1.1055		V	
I_{CC}	I_{CC} for processor core Dual Core N2600/N2650 N2800/N2850 D2500/D2550 D2700			 3.5 4.72 6.7 6.7	 2.07 3.257 3.886 5.073	A	
V_{CC_HFM}	V_{CC} at Highest Frequency Mode (HFM)	0.91		1.21		V	2, 3
V_{CC_LFM}	V_{CC} at Lowest Frequency Mode (LFM) N2600/N2650 N2800/N2850	 0.70 0.75		 0.90 0.90		V	2, 3
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4) N2600/N2650 N2800/N2850	 0.70 0.75					
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C6)		0.35			V	
I_{AH}	I_{CC} Auto-Halt Dual-core processors	0.6072	1.3883	3.872		A	@VID =1.1V
I_{SGNT}	I_{CC} Stop-Grant Dual-core processors	0.4470	1.2242	3.696		A	@VID= 1.1V
I_{DPRSLP}	I_{CC} Deeper Sleep (C4) Dual-core processors	0.1302	0.5852	1.9976		A	@VID= 0.9V
I_{DPRSLP}	I_{CC} Deeper Sleep (C6) Dual-core processors	0.0810	0.3649	1.2162		A	@VID= 0.7V

Table 4-30. Processor Core Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	I_TDC	Unit	Note
$SLOPE_{LL}$	Processor Core Supply DC Loadline		-5.9			mΩ	Figure 4-7
	Processor Core Supply AC Loadline			-9.0		mΩ	
	Graphic Core Supply Loadline - N2000 series only		0			mΩ	
	Ripple	-10		+10		mV	
	TOB	-19		+19		mV	

NOTE:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Please note this differs from the VID employed by the processor during a power management event.
3. These are pre-silicon estimates and are subject to change.
4. Long term reliability cannot be assured in conditions above or below Max/Min functional limits

Figure 4-7. Vcc and Icc Processor Loadline

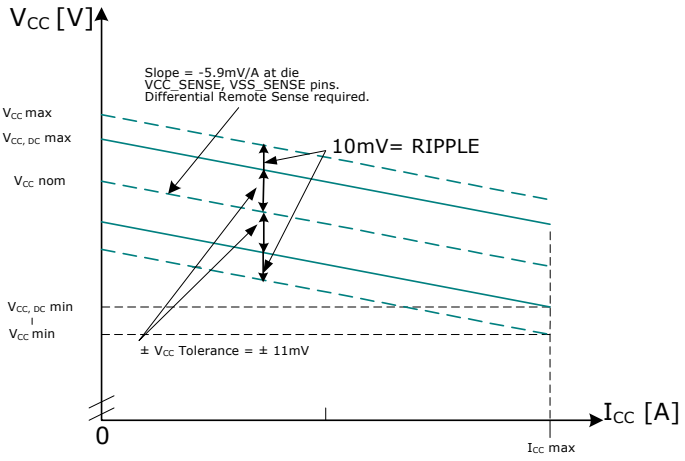


Figure 4-8. Vcc AC Vs. DC Loadline

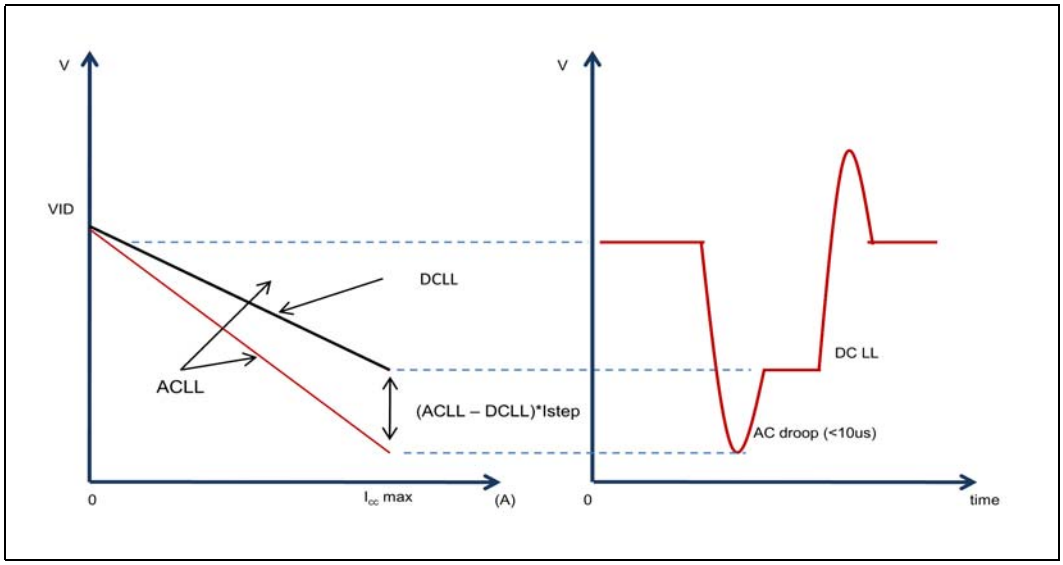


Table 4-31. Istep

		min	typ	max
Istep	N2600			2.2
	N2800			3.0
	D2500	-	-	4.0
	D2700	-	-	4.0

The I/O buffer supply voltage should be measured at the processor package pins. The tolerances shown in Table 4-32 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 4-32 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Table 4-32. Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications (Sheet 1 of 4)

	Symbol Parameter	Min	Typ	Max	I_TDC	Unit	Note 1
V_{CCGFX}	N2000 series VID controlled GFX supply voltage D2000 series fixed VID GFX supply voltage	0.75 1.01365	1.067	1.05 1.12035		V	

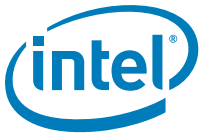


Table 4-32.Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications (Sheet 2 of 4)

	Symbol Parameter	Min	Typ	Max	I_TDC	Unit	Note 1
V_{CCGFX}	GFX supply voltage D2000 series is fixed VID Voltage	1.01365	1.067	1.12035		V	
$V_{CCGFX,BOOT}$	Default V_{CCGFX} voltage for initial power up	1.0945	1.1	1.1055		V	
I_{CCGFX}	GFX supply current --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			 1.86 3.5707 3.4544 3.7132	 1.252 2.644 2.21 2.693	A	
V_{CCGPIO_DIO} V_{CCDLVD}, V_{CCALVD} V_{CCADAC} V_{CCTHRM}	Debug I/O supply voltage LVDS supply voltage LVDS supply voltage CRT/VGA DAC supply voltage Thermal Sensor SFR supply voltage	1.71	1.8	1.89		V	2
I_{CCGPIO_DIO} I_{CCDLVD}, I_{CCALVD} I_{CCADAC} I_{CCTHRM}	Debug I/O supply current LVDS supply current LVDS supply current CRT/VGA DAC supply current Thermal Sensor SFR supply current --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			 0.151 0.151 0.151 0.151	 0.116 0.116 0.116 0.116	A	
V_{CCFHV} V_{CCADMI} $V_{CCAGPIO\_LV}$ V_{CCADDR} $V_{CCACKDDR}$ $V_{CCADLLDDR}$ V_{CCDMPL} V_{CCDIO} V_{CCADP} $V_{CCPLLCPU0}$ $V_{CCPLLCPU1}$ $V_{CCAHPLL}$	Fusing Programming supply voltage DMI IO supply voltage GPIO sVID and Legacy supply voltage DDR Digital supply voltage DDR Clk Digital Quiet supply voltage DDR DLL Quiet supply voltage MPLL Digital supply voltage Digital Logic CRT supply voltage DDI IOs supply voltage CPU0 PLL supply voltage CPU1 PLL supply voltage SOC PLL supply voltage	0.9975	1.05	1.1025		V	

Table 4-32. Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications (Sheet 3 of 4)

	Symbol Parameter	Min	Typ	Max	I_TDC	Unit	Note 1
$V_{CCRAMXXX}$	CPU L2 Caches, DTS, Arrays supply voltage N2000 series D2000 series (D2500/D2550/ D2700)	0.9975 1.0137	1.05 1.067	1.1025 1.1204		V	
I_{CCFHV} I_{CCADMI} $I_{CCRAMXXX}$ $I_{CCAGPIO\_LV}$ I_{CCADDR} $I_{CCACKDDR}$ $I_{CCADLLDDR}$ I_{CCDMPL} I_{CCDIO} I_{CCADP} $I_{CCPLLCPU0}$ $I_{CCPLLCPU1}$ $I_{CCAHPLL}$	Fusing Programming supply current DMI analog supply current CPU L2 Caches, DTS, Arrays supply current GPIO sVID and Legacy supply current DDR Digital supply current DDR Clk Digital Quiet supply current DDR DLL Quiet supply current MPLL Digital supply current Digital Logic CRT supply current DDI IOs supply current CPU0 PLL supply current CPU1 PLL supply current SOC PLL supply current --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			0.99 1.13 1.268 1.268	0.551 0.619 0.976 0.976	A	
$V_{\_SM}$ $V_{CCCKDDR}$	DDR I/O supply voltage DDR CLK Quiet DDR I/O supply voltage (DDR3)	1.425	1.5	1.575		V	
$V_{\_SM}$ $V_{CCCKDDR}$	DDR I/O supply voltage DDR CLK Quiet DDR I/O supply voltage (DDR3L)	1.283	1.35	1.418		V	
I_{CC_SM} $I_{CCCKDDR}$	DDR I/O supply current DDR CLK Quiet I/O supply current --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			0.404 0.869 0.869 0.869	0.175 0.340 0.583 0.583	A	

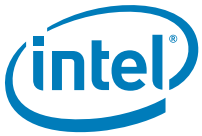


Table 4-32.Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications (Sheet 4 of 4)

	Symbol Parameter	Min	Typ	Max	I_TDC	Unit	Note 1
V_{CCADMI_SFRPLL} $V_{CCAGPIO\_REF}$ V_{CCADP0_SFR} V_{CCADP1_SFR} $V_{CCSFRMPL}$	DMI SFRPLL Supply voltage GPIOs reference supply voltage Display PLLs SFR supply voltage Display PLLs SFR supply voltage MPLL SFR input voltage with respect to VSS	1.425	1.5	1.575		V	
I_{CCADMI} $I_{CCAGPIO\_REF}$ I_{CCADP0_SFR} I_{CCADP1_SFR} $I_{CCSFRMPL}$	DDR DMI I/O Supply current GPIOs reference supply current Display PLLs SFR supply current Display PLLs SFR supply current MPLL SFR input current with respect to VSS --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			 0.124 0.125 0.125 0.125	 0.095 0.096 0.096 0.096	A	
$V_{CCAGPIO}$ $V_{CCAZILAON}$	GPIO supply voltage Intel HD-Audio Supply Voltage	3.135	3.3	3.465		V	
$I_{CCAGPIO}$ $I_{CCAZILAON}$	GPIO supply current Intel HD-Audio Supply current --N2600/N2650 --N2800/N2850 --D2500 --D2550/D2700			 0.004 0.004 0.004 0.004	 0.003 0.003 0.004 0.003	A	

NOTE:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. These rails are filtered from other voltage rails on the platform and should be measured at the input of the filter.
3. VRM tolerance, ripple and core noise parameters which states that reliability cannot be assured if these are violated.
4. VCCPLLCPU0 & VCCPLLCPU1 & VCCAHPLL: AC requirement 1.5%

4.9.3 DC Specifications

Platform reference voltages at the top of Table 4-32 are specified at DC only. V_{REF} measurements should be made with respect to the supply voltage.

4.9.3.1 Input Clock DC Specification

Table 4-33. Input Clocks (BCLK, HPL_CLKIN, DPL_REFCLKIN, EXP_CLKIN) Differential Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.30	0		V	
V_{IH}	Input High Voltage			1.15	V	
V_{CROSS}	Absolute crossing voltage	0.3		0.550	V	2,3
dV_{CROSS}	Range of crossing points			0.14	V	
C_{IN}	Input Capacitance	1.0		3.0	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. Crossing voltage defined as instantaneous voltage when rising edge of CLKN equalize CLKP. The crossing point must meet the absolute and relative crossing point specification simultaneously.

4.9.3.2 DDR3 / DDR3L DC Specifications

Table 4-34. DDR3 / DDR3L Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}(DC)	Input Low Voltage			SM_VREF - 100mV	V	1, 3
V_{IH}(DC)	Input High Voltage	SM_VREF + 100mV			V	2, 3
V_{OL}	Output Low Voltage		(VDDQ / 2)* (RON / (RON+RVTT _TERM))			3
V_{OH}	Output High Voltage		VDDQ - ((VDDQ / 2)* (RON/ (RON+RVTT _TERM))		V	3
I_{IL}	Input Leakage Current			40(DDR3) 35(DDR3L)	µA	For all DDR Signals, CMD, CTL, CK, DQ, DQS
R_{ON}	DDR3 Clock Buffer strength		26		Ω	

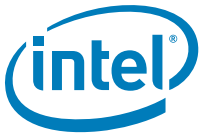


Table 4-34.DDR3 / DDR3L Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
$C_{I/O}$	DQ/DQS/DQS# DDR3 I/O Pin Capacitance		2.6		pF	

NOTES:
1. V_{IL} is defined as the maximum voltage level at a DDR input buffer that will be received as a logical low value. SM_VREF is normally VCC_DDR/2
2. V_{IH} is defined as the minimum voltage level at a DDR input buffer that will be received as a logical high value. SM_VREF is normally VCC_DDR/2
3. V_{IH} and V_{OH} may experience excursions above VDDQ. However, input signal drivers must comply with the signal quality specifications.
4. RON is DDR driver resistance whereas RTT_TERM is DRAM ODT resistance which is controlled by DRAM.

Table 4-35.CPU Sideband CMOS Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	0.9975		1.1025	V	
V_{IH}	Input High Voltage	0.8* V_{CCP}			V	1
V_{IL}	Input Low Voltage			0.5* V_{CCP}	V	2
Z_{pu}	Pull up Impedance			60	Ohm	3
Z_{pd}	Pull down Impedance			60	Ohm	3
R_{wpu}	Weak Pull Impedance	1		4	KOhm	3
R_{wpd}	Weak Pull Down Impedance	1		4	KOhm	3
$R_{wpu-40K}$	Weak Pull Up Impedance 40K	20		70	KOhm	4
$R_{wpd-40K}$	Weak Pull Down Impedance 40K	20		70	KOhm	4
I_i	Input Pin Leakage	-15		15	µA	5

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at V_{ccp}/2.
4. Rwpu_40k and Rwpd_40k are only used for TRST_B
5. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.
6. The DC specification applicable to TCLK, TRST#, TMS, TDI, CPUSLP#, PWRGOOD, INIT#, LINT01, LINT00, SMI#, DPRSTP#, DPLSLP#, STPCLK# and SVID_ALERT#.

Table 4-36.CPU Sideband OD 25 Ohm 1.05 V Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	0.9975		1.1025	V	
V_{IH}	Input High Voltage	0.8* V_{CCP}			V	1
V_{IL}	Input Low Voltage			0.5 * V_{CCP}	V	2
Z_{pd}	Pull down Impedance			30	Ohm	3
R_{wpu}	Weak Pull Impedance	1		4	KOhm	3
R_{wpd}	Weak Pull Down Impedance	1		4	KOhm	3

Table 4-36.CPU Sideband OD 25 Ohm 1.05 V Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_i	Input Pin Leakage	-20		20	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at Vccp/2.
4. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.
5. The DC specification applicable to TDO, PROCHOT#, PBE# and THERMTRIP#

Table 4-37.CPU Sideband OD 12.5 Ohms 1.05 V Signal Group DC Specification

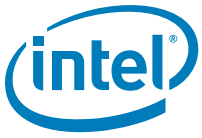
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	0.9975		1.1025	V	
V_{IH}	Input High Voltage	0.8* V_{CCP}			V	1
V_{IL}	Input Low Voltage			0.5 * V_{CCP}	V	2
Z_{pd}	Pull down Impedance			15	Ohm	3
R_{wpu}	Weak Pull Impedance	1		4	KOhm	3
R_{wpd}	Weak Pull Down Impedance	1		4	KOhm	3
I_i	Input Pin Leakage	-40		40	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at Vccp/2.
4. For V_{IN} between 0-V and V_{CCP}. Measured when driver is tri-stated.
5. The DC specification applicable SVID_DATA and SVID_CLK.

Table 4-38.CPU Sideband OD 1.8 V Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	1.71		1.89	V	
V_{IH}	Input High Voltage	0.64* V_{CCP}			V	1
V_{IL}	Input Low Voltage			0.41 * V_{CCP}	V	2
Z_{pd}	Pull down Impedance			30	Ohm	3
R_{wpu}	Weak Pull Impedance	1		4	KOhm	3
I_i	Input Pin Leakage (PRDY)	-30		30	µA	4
I_i	Input Pin Leakage (PREQ)	-15		15	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at Vccp/2.
4. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.



5. THe DC Specification covers PRDY# and PREQ#.

4.9.3.3 Intel® HD Audio DC Specification

This section defines the electrical characteristics of Intel HD Audio components for 3.3-V signaling scheme. The 3.3 V Intel HD Audio components can be designed with standard CMOS I/O technology. Unless specifically stated otherwise, component parameters apply at the package pins; not at bare silicon pads nor at card edge connectors.

Table 4-39.3.3-V DC Specification

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{CC}	Supply Voltage		3.135	3.465	V	
V_{IH}	Input High Voltage		0.65 x V_{CC}		V	
V_{IL}	Input Low Voltage			0.35 x V_{CC}	V	
V_{OH}	Output High Voltage	Iout =-500 µA	0.9 x V_{CC}		V	
V_{OL}	Output Low Voltage	Iout =1500 µA		0.10 x V_{CC}	V	
I_{IL}	Input Leakage Current	0<Vin<Vcc		±175	µA	1
C_{IN}	Input Pin Capacitance			7.5	pF	
L_{PIN}	Pin Inductance			20	nH	2

NOTES:
1. For SDI buffers (or in general any bi-directional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

Table 4-40.1.5-V DC specification

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{CC}	Supply Voltage		1.418	1.583	V	
V_{IH}	Input High Voltage		0.6 x V_{CC}		V	
V_{IL}	Input Low Voltage			0.4 x V_{CC}	V	
V_{OH}	Output High Voltage	Iout =-500 µA	0.9 x V_{CC}		V	
V_{OL}	Output Low Voltage	Iout =1500 µA		0.10 x V_{CC}	V	
I_{IL}	Input Leakage Current	0<Vin<Vcc		±175	µA	1
C_{IN}	Input Pin Capacitance			7.5	pF	
L_{PIN}	Pin Inductance			20	nH	2

NOTES:
1. For SDI buffers (or in general any bi-directional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

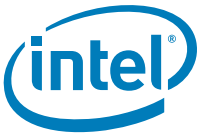


Table 4-41.High Voltage GPIO CMOS Signal DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	3.135		3.465	V	
V_{IH}	Input High Voltage	2		Vccp	V	1
V_{IL}	Input Low Voltage	0		0.8	V	2
Z_{pu}	Pull up Impedance	40	50	60	Ohm	3
Z_{pd}	Pull down Impedance	40	50	60	Ohm	3
I_i	Input Pin Leakage	-45		45	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at Vccp/2.
4. For VIN between 0V and V_{CCP}. Measured when driver is tri-stated.
5. The DC specification applicable to DDI0_HPD, HV_DDI1_HPD, RESET#, PANEL_VDDEN, BKLTEN, and BKLTCTL

4.9.3.4 Display DC Specification

4.9.3.4.1 Analog Video and LVDS Signals

Both interface DC Specifications are referred to the VESA Video Signal Standard, version 1 revision 2.

Table 4-42.R,G,B/CRT DAC Display DC specification (Functional Operating Range)

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Resolution		8		bits	1
	Max Luminance (full-scale)	0.665	0.700	0.770	V	1,2,4 (white video level voltage)
	Min Luminance		0.0		V	1,3,4 (black video level voltage)
	LSB Current		73.2	80.5	µA	4,5
	Integral Non Linearity (INL)	-1.0		+1.0	LSB	1,6
	Differential Non-Linearity (DNL)	-1.0		+1.0	LSB	1,6
	Video Channel-to-Channel Voltage amplitude mismatch			6	%	7
	Monotonicity		Guaranteed			

NOTE:
1. Measured at each R,G,B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude

4. Defined for a double 75 Ohm termination
5. Set by external reference resistor value
6. INL & DNL measured and calculated according to VESA Video Signal Standards
7. Max fill-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).

Table 4-43.High Voltage GPIO OD Signal DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	3.135		3.465	V	
V_{IH}	Input High Voltage	2			V	1
V_{IL}	Input Low Voltage	0		0.8	V	2
V_{OL}	Output Low Voltage			0.4	V	3
I_i	Input Pin Leakage	-45		45	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. 3mA sink current.
4. For VIN between 0V and V_{CCP}. Measured when driver is tri-stated.
5. The DC specification covers DDI0_DDC_SDA, DDI0_DDC_SCL, DDI1_DDC_SDA,DDI1_DDC_SCL, LVDS_DDC_CLK, LVDS_DDC_DATA, LVDS_CTRL_CLK, LVDS_CTRL_DATA, CRT_DDC_CLK, CRT_DDC_DATA

Table 4-44.CRT_HSYNC and CRT_VSYNC DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CCP}	I/O Voltage	3.135		3.465	V	
V_{OH}	Output High Voltage	2.4		Vccp	V	
V_{OL}	Output Low Voltage	0		0.5	V	
I_{OH}	Output High Current			8	mA	
I_{OL}	Output Low Current			8	mA	
I_i	Input Pin Leakage	-35		35	µA	1

NOTES:
1. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.

Table 4-45.LVDS Interface DC Specification (Functional Operating Range, V_{CCLVDS} = 1.8 V ±5%)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{OD}	Differential Output Voltage	250	350	450	mV	2
ΔV_{OD}	Change in V_{OD} between Complementary Output States			50	mV	2
V_{OS}	Offset Voltage	1.125	1.25	1.375	V	2
ΔV_{OS}	Change in V_{OS} between Complementary Output States			50	mV	2
I_I	Input Leakage Current			40	µA	
I_{OS}	Output Short Circuit Current		-3.5	-10	mA	2
I_{OZ}	Output TRI-STATE Current		±1	±10	µA	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All LVDS active lanes must be terminated with 100 Ohm resistor for correct V_{OS} performance and measurement.

4.9.3.4.2 Digital Display Interface (DDI) Signals DC Specification

The interface DC Specifications are referred to the VESA Video Signal Standard, version 1 revision 2.

Table 4-46.DDI Main Transmitter DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{TX-DIFFp-p-Level1}$	Differential Peak-to-peak Output Voltage Level 1	0.34	0.4	0.46	V	1
$V_{TX-DIFFp-p-Level2}$	Differential Peak-to-peak Output Voltage Level 2	0.51	0.6	0.68	V	1
$V_{TX-DIFFp-p-Level3}$	Differential Peak-to-peak Output Voltage Level 3	0.69	0.8	0.92	V	1
$V_{TX-DIFFp-p-Level4}$	Differential Peak-to-peak Output Voltage Level 4	1.02	1.2	1.38	V	1
$V_{TX-PREEMP-RATIO}$	No Pre-emphasis	0.0	0.0	0.0	dB	1
	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB	1
	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	1
	9.5 dB Pre-emphasis	7.6	9.5	11.4	dB	1
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0		2.0	V	1
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12			dB	4
	Differential Return Loss at 1.35GHz at Tx Package pins	9			dB	4
C_{TX}	AC Coupling Capacitor	75		200	nF	5
V_{off}	Single Ended Standby (off), output voltage	-10		10	mV	@ AVcc 3.3V
V_{swing}	Single Ended output swing voltage	400		600	mV	
V_{OH}(<=165 MHz)	Single Ended high level output voltage	-10		10	mV	@ AVcc 3.3V
V_{OH}(>165 MHz)	Single Ended high level output voltage	-200		+10	mV	@ AVcc 3.3V
V_{OL}(<=165 MHz)	Single Ended low level output voltage	-600		-400	mV	@ AVcc 3.3V
V_{OL} (>165 MHz)	Single Ended low level output voltage	-700		-400	mV	@ AVcc 3.3V

NOTES:
1. For embedded connection, support of programmable voltage swing levels is optional.

2. Total drive current of the transmitter when it is shorted to its ground.
3. Common mode voltage is equal to Vbias_Tx voltage shown in Figure 4-3.
4. Straight loss line between 0.675 GHz and 1.35 GHz.
5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on.

Table 4-47.DDI AUX Channel DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{AUX-DIFFp-p}$	AUX Peak-to-peak Voltage at a transmitting Device	0.39		1.38	V	1
$V_{AUX-\_TERM\_R}$	AUX CH termination DC resistance		100		Ohm	2
$V_{AUX-DC-CM}$	AUX DC Common Mode Voltage	0		2.0	V	3
$V_{AUX-TURN-CM}$	AUX turn around common mode voltage			0.4	V	4
$V_{AUX-TERM-R}$	AUX CH termination DC resistance		100		Ohm	
I_{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	5
C_{AUX}	AC Coupling Capacitor	75		200	nF	6

NOTES:
1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} - V_{AUXM}|$
2. Informative
3. Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
4. Steady state common mode voltage shift between transmit and receive modes of operation.
5. Total drive current of the transmitter when it is shorted to its ground.
6. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on.

Figure 4-9. Definition of Differential Voltage and Differential Voltage Peak-to-Peak

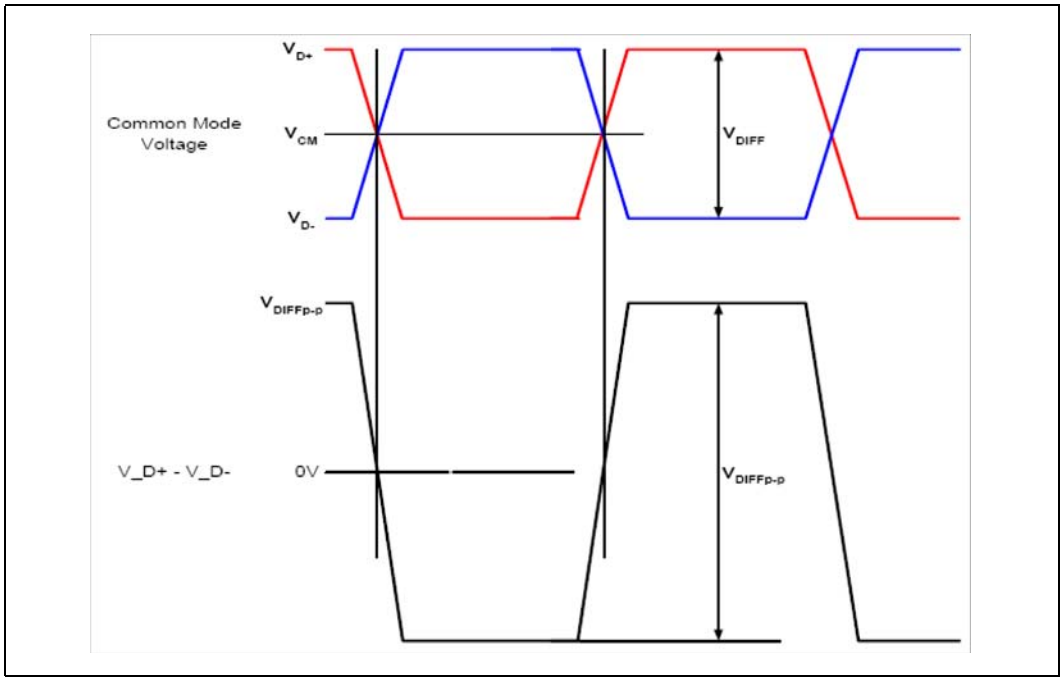
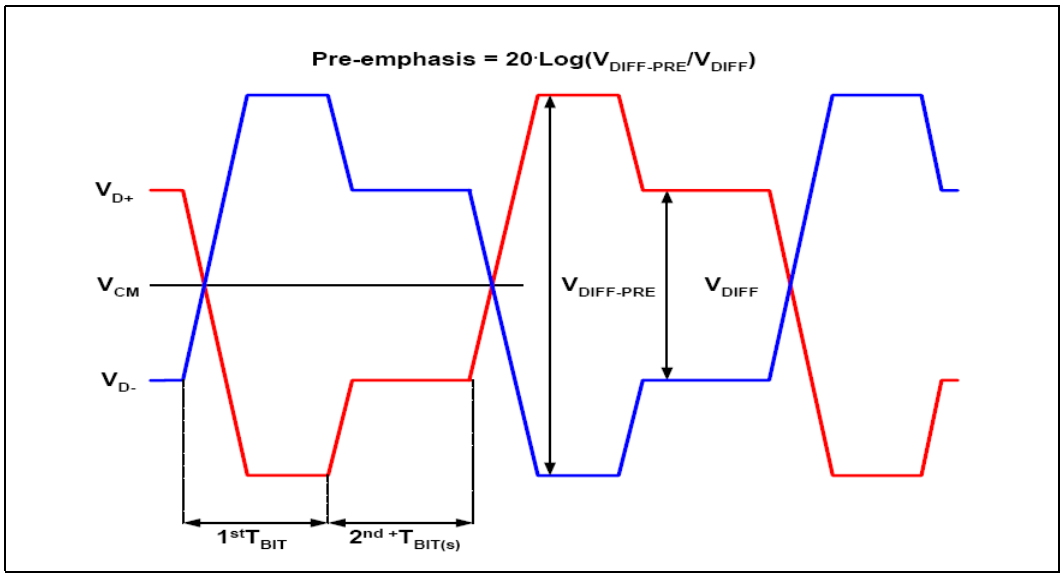
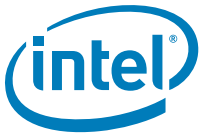


Figure 4-10. Definition of Pre-emphasis





4.9.3.5 DMI DC specification

Table 4-48.DMI Receiver DC specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.987		1.1031	V	1

NOTES:
1. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.

§

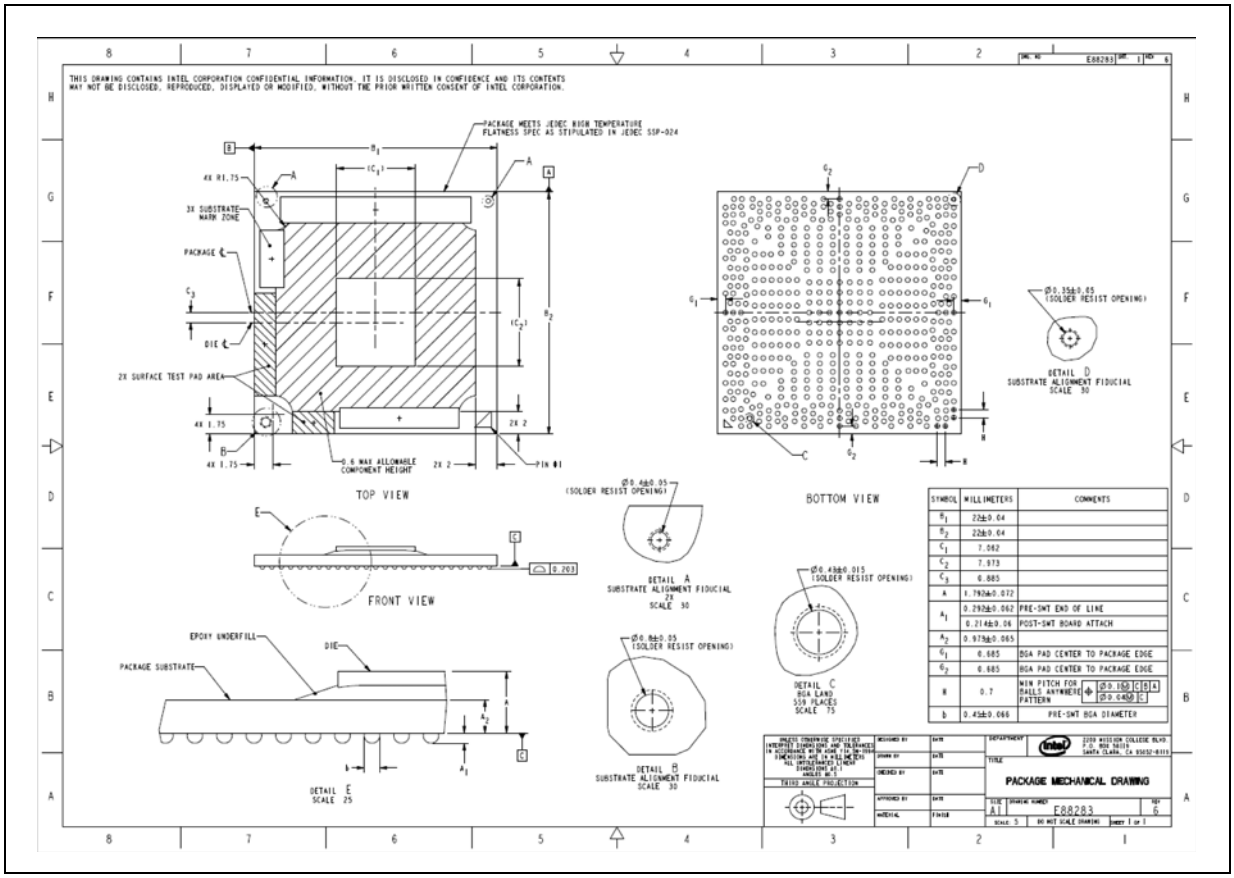
5 Mechanical Specifications and Ball Information

This chapter provides the specifications, and ballout assignments.

5.1 Mechanical Specifications

5.1.1 Mechanical Drawings

Figure 5-11. Mechanical Drawings



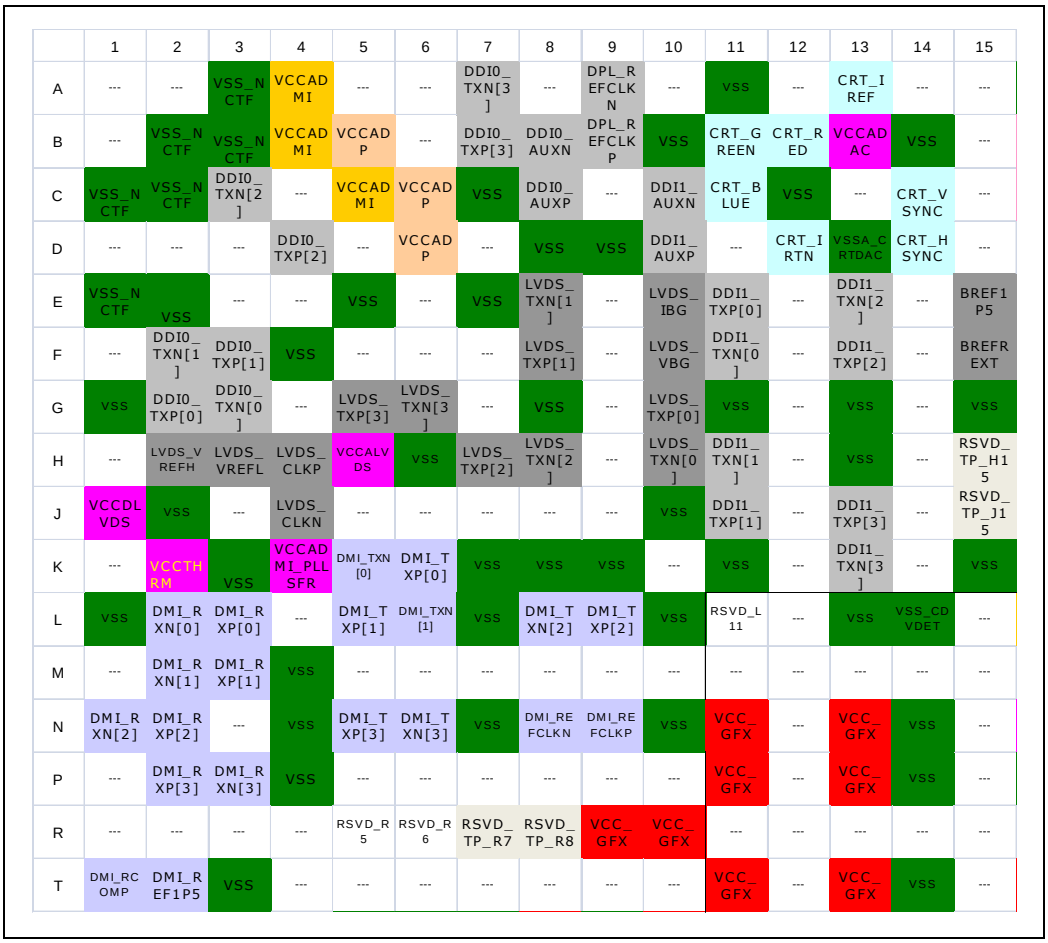
5.1.2 Loading Specifications

Loading is 15 lb max static compressive.

5.2 Processor Ballout Assignment

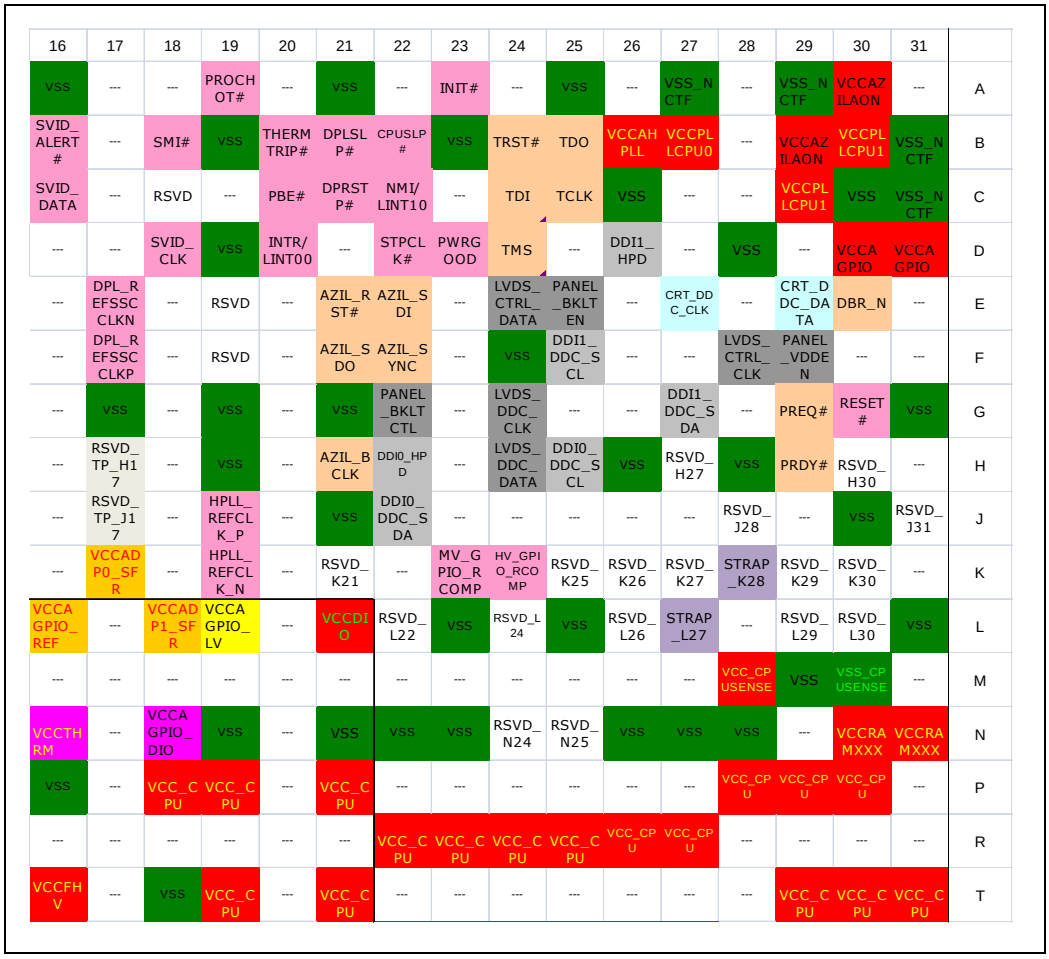
Figure 5-12 to Figure 5-15 are graphic representations of the processor ballout assignments. Table 5-49 lists the ballout by signal name.

Figure 5-12. Pinmap (Top View, Upper-Left Quadrant)



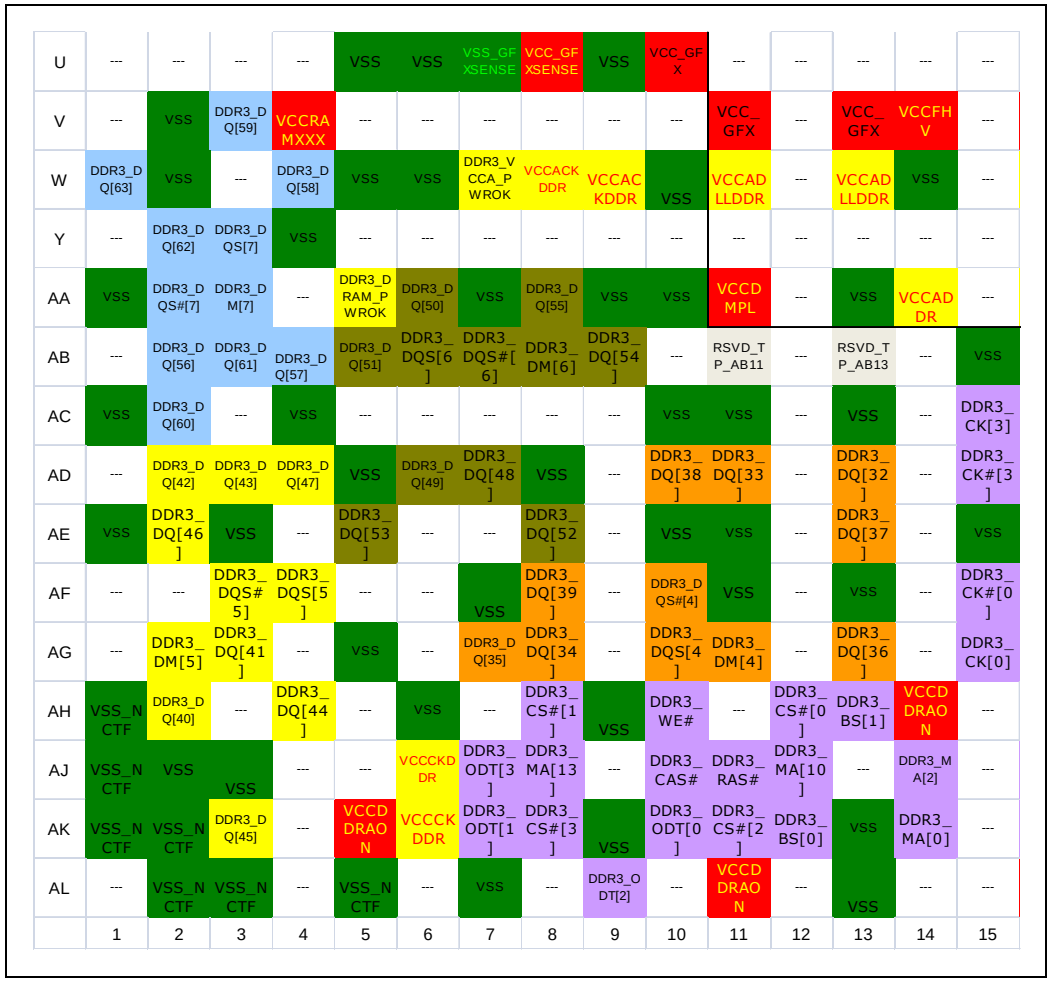
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	---	---	VSS_NCTF	VCCADMI	---	---	DDI0_TXN[3]	---	DPL_REFCLKN	---	VSS	---	CRT_IREF	---	---
B	---	VSS_NCTF	VSS_NCTF	VCCADMI	VCCADP	---	DDI0_TXP[3]	DDI0_AUXN	DPL_REFCLKP	VSS	CRT_GREEN	CRT_RED	VCCADAC	VSS	---
C	VSS_NCTF	VSS_NCTF	DDI0_TXN[2]	---	VCCADMI	VCCADP	VSS	DDI0_AUXP	---	DDI1_AUXN	CRT_BLUE	VSS	---	CRT_VSYNC	---
D	---	---	---	DDI0_TXP[2]	---	VCCADP	---	VSS	VSS	DDI1_AUXP	---	CRT_IRTN	VSSA_CRTDAC	CRT_HSYNC	---
E	VSS_NCTF	VSS	---	---	VSS	---	VSS	LVDS_TXN[1]	---	LVDS_IBG	DDI1_TXP[0]	---	DDI1_TXN[2]	---	BREF1P5
F	---	DDI0_TXN[1]	DDI0_TXP[1]	VSS	---	---	---	LVDS_TXP[1]	---	LVDS_VBG	DDI1_TXN[0]	---	DDI1_TXP[2]	---	BREFREXT
G	VSS	DDI0_TXP[0]	DDI0_TXN[0]	---	LVDS_TXP[3]	LVDS_TXN[3]	---	VSS	---	LVDS_TXP[0]	VSS	---	VSS	---	VSS
H	---	LVDS_VREFH	LVDS_VREFL	LVDS_CLKP	VCCALVDS	VSS	LVDS_TXP[2]	LVDS_TXN[2]	---	LVDS_TXN[0]	DDI1_TXN[1]	---	VSS	---	RSVD_TP_H15
J	VCCDLVDS	VSS	---	LVDS_CLKN	---	---	---	---	---	VSS	DDI1_TXP[1]	---	DDI1_TXP[3]	---	RSVD_TP_J15
K	---	VCCTHRM	VSS	VCCADMI_PLLSFR	DMI_TXN[0]	DMI_TXP[0]	VSS	VSS	VSS	---	VSS	---	DDI1_TXN[3]	---	VSS
L	VSS	DMI_RXN[0]	DMI_RXP[0]	---	DMI_TXP[1]	DMI_TXN[1]	VSS	DMI_TXN[2]	DMI_TXP[2]	VSS	RSVD_L11	---	VSS	VSS_CDVDET	---
M	---	DMI_RXN[1]	DMI_RXP[1]	VSS	---	---	---	---	---	---	---	---	---	---	---
N	DMI_RXN[2]	DMI_RXP[2]	---	VSS	DMI_TXP[3]	DMI_TXN[3]	VSS	DMI_REFCLKN	DMI_REFCLKP	VSS	VCC_GFX	---	VCC_GFX	VSS	---
P	---	DMI_RXP[3]	DMI_RXN[3]	VSS	---	---	---	---	---	---	VCC_GFX	---	VCC_GFX	VSS	---
R	---	---	---	---	RSVD_R5	RSVD_R6	RSVD_TP_R7	RSVD_TP_R8	VCC_GFX	VCC_GFX	---	---	---	---	---
T	DMI_RCOMP	DMI_REF1P5	VSS	---	---	---	---	---	---	---	VCC_GFX	---	VCC_GFX	VSS	---

Figure 5-13. Pinmap (Top View, Upper-Right Quadrant)



16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
VSS	---	---	PROCHOT#	---	VSS	---	INIT#	---	VSS	---	VSS_NCTF	---	VSS_NCTF	VCCAZILAON	---	A
SVID_ALERT#	---	SMI#	VSS	THERMTRIP#	DPLSLP#	CPUSLP#	VSS	TRST#	TDO	VCCAHPLL	VCCPLLCPU0	---	VCCAZILAON	VCCPLLCPU1	VSS_NCTF	B
SVID_DATA	---	RSVD	---	PBE#	DPRSTP#	NMI/LINT10	---	TDI	TCLK	VSS	---	---	VCCPLLCPU1	VSS	VSS_NCTF	C
---	---	SVID_CLK	VSS	INTR/LINT00	---	STPCLK#	PWRGOOD	TMS	---	DDI1_HPD	---	VSS	---	VCCAGPIO	VCCAGPIO	D
---	DPL_REFSSCCLKN	---	RSVD	---	AZIL_RST#	AZIL_SDI	---	LVDS_CTRL_DATA	PANEL_BKLTEN	---	CRT_DDC_CLK	---	CRT_DDC_DATA	DBR_N	---	E
---	DPL_REFSSCCLKP	---	RSVD	---	AZIL_SDO	AZIL_SYNC	---	VSS	DDI1_DDC_SCL	---	---	LVDS_CTRL_CLK	PANEL_VDDEN	---	---	F
---	VSS	---	VSS	---	VSS	PANEL_BKLTCTL	---	LVDS_DDC_CLK	---	---	DDI1_DDC_SDA	---	PREQ#	RESET#	VSS	G
---	RSVD_TP_H17	---	VSS	---	AZIL_BCLK	DDI0_HPD	---	LVDS_DDC_DATA	DDI0_DDC_SCL	VSS	RSVD_H27	VSS	PRDY#	RSVD_H30	---	H
---	RSVD_TP_J17	---	HPLL_REFCLK_P	---	VSS	DDI0_DDC_SDA	---	---	---	---	---	RSVD_J28	---	VSS	RSVD_J31	J
---	VCCADP0_SFR	---	HPLL_REFCLK_N	---	RSVD_K21	---	MV_GPIO_RCOMP	HV_GPIO_RCOMP	RSVD_K25	RSVD_K26	RSVD_K27	STRAP_K28	RSVD_K29	RSVD_K30	---	K
VCCAGPIO_REF	---	VCCADP1_SFR	VCCAGPIO_LV	---	VCCDIO	RSVD_L22	VSS	RSVD_L24	VSS	RSVD_L26	STRAP_L27	---	RSVD_L29	RSVD_L30	VSS	L
---	---	---	---	---	---	---	---	---	---	---	---	VCC_CPUSENSE	VSS	VSS_CPUSENSE	---	M
VCCTHRM	---	VCCAGPIO_DIO	VSS	---	VSS	VSS	VSS	RSVD_N24	RSVD_N25	VSS	VSS	VSS	---	VCCRAMXXX	VCCRAMXXX	N
VSS	---	VCC_CPU	VCC_CPU	---	VCC_CPU	---	---	---	---	---	---	VCC_CPU	VCC_CPU	VCC_CPU	---	P
---	---	---	---	---	---	VCC_CPU	VCC_CPU	VCC_CPU	VCC_CPU	VCC_CPU	VCC_CPU	---	---	---	---	R
VCCFHV	---	VSS	VCC_CPU	---	VCC_CPU	---	---	---	---	---	---	---	VCC_CPU	VCC_CPU	VCC_CPU	T

Figure 5-14. Pinmap (Top View, Lower-Left Quadrant)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
U	---	---	---	---	VSS	VSS	VSS_GFXSENSE	VCC_GFXSENSE	VSS	VCC_GFX	---	---	---	---	---
V	---	VSS	DDR3_DQ[59]	VCCRAMXXX	---	---	---	---	---	---	VCC_GFX	---	VCC_GFX	VCCFHV	---
W	DDR3_DQ[63]	VSS	---	DDR3_DQ[58]	VSS	VSS	DDR3_VCCA_PWROK	VCCACKDDR	VCCACKDDR	VSS	VCCADLLDDR	---	VCCADLLDDR	VSS	---
Y	---	DDR3_DQ[62]	DDR3_DQS[7]	VSS	---	---	---	---	---	---	---	---	---	---	---
AA	VSS	DDR3_DQS#[7]	DDR3_DM[7]	---	DDR3_DRAM_PWROK	DDR3_DQ[50]	VSS	DDR3_DQ[55]	VSS	VSS	VCCDMPL	---	VSS	VCCADDR	---
AB	---	DDR3_DQ[56]	DDR3_DQ[61]	DDR3_DQ[57]	DDR3_DQ[51]	DDR3_DQS[6]	DDR3_DQS#[6]	DDR3_DM[6]	DDR3_DQ[54]	---	RSVD_TP_AB11	---	RSVD_TP_AB13	---	VSS
AC	VSS	DDR3_DQ[60]	---	VSS	---	---	---	---	---	VSS	VSS	---	VSS	---	DDR3_CK[3]
AD	---	DDR3_DQ[42]	DDR3_DQ[43]	DDR3_DQ[47]	VSS	DDR3_DQ[49]	DDR3_DQ[48]	VSS	---	DDR3_DQ[38]	DDR3_DQ[33]	---	DDR3_DQ[32]	---	DDR3_CK#[3]
AE	VSS	DDR3_DQ[46]	VSS	---	DDR3_DQ[53]	---	---	DDR3_DQ[52]	---	VSS	VSS	---	DDR3_DQ[37]	---	VSS
AF	---	---	DDR3_DQS#[5]	DDR3_DQS[5]	---	---	VSS	DDR3_DQ[39]	---	DDR3_DQS#[4]	VSS	---	VSS	---	DDR3_CK#[0]
AG	---	DDR3_DM[5]	DDR3_DQ[41]	---	VSS	---	DDR3_DQ[35]	DDR3_DQ[34]	---	DDR3_DQS[4]	DDR3_DM[4]	---	DDR3_DQ[36]	---	DDR3_CK[0]
AH	VSS_NCTF	DDR3_DQ[40]	---	DDR3_DQ[44]	---	VSS	---	DDR3_CS#[1]	VSS	DDR3_WE#	---	DDR3_CS#[0]	DDR3_BS[1]	VCCDDRAON	---
AJ	VSS_NCTF	VSS	VSS	---	---	VCCCKDDR	DDR3_ODT[3]	DDR3_MA[13]	---	DDR3_CAS#	DDR3_RAS#	DDR3_MA[10]	---	DDR3_MA[2]	---
AK	VSS_NCTF	VSS_NCTF	DDR3_DQ[45]	---	VCCDDRAON	VCCCKDDR	DDR3_ODT[1]	DDR3_CS#[3]	VSS	DDR3_ODT[0]	DDR3_CS#[2]	DDR3_BS[0]	VSS	DDR3_MA[0]	---
AL	---	VSS_NCTF	VSS_NCTF	---	VSS_NCTF	---	VSS	---	DDR3_ODT[2]	---	VCCDDRAON	---	VSS	---	---

Figure 5-15.Pinmap (Top View, Lower-Right Quadrant)

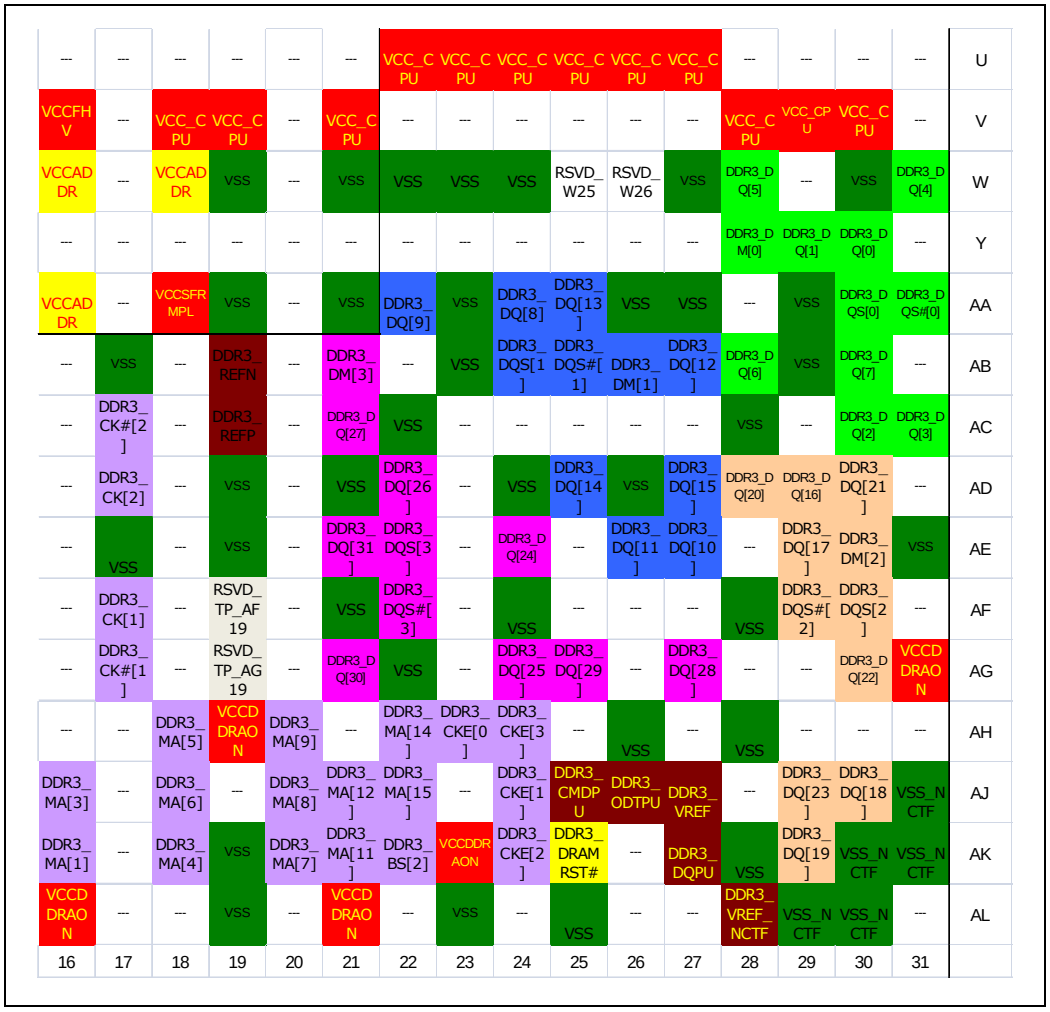


Table 5-49.Processor Ball list by Ball Name (Sheet 1 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
AZIL_BCLK	H21	AUDIO	
AZIL_RST#	E21	AUDIO	
AZIL_SDI	E22	AUDIO	
AZIL_SDO	F21	AUDIO	
AZIL_SYNC	F22	AUDIO	
BREF1P5	E15	Analog	I
BREFREXT	F15	Analog	
CPUSLP#	B22		
CRT_BLUE	C11	CRTDAC	O
CRT_DDC_CLK	E27	CRTDAC	I/O

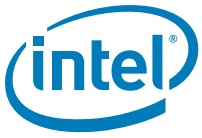


Table 5-49.Processor Ball list by Ball Name (Sheet 2 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
CRT_DDC_DATA	E29	CRTDAC	I/O
CRT_GREEN	B11	CRTDAC	O
CRT_HSYNC	D14	CRTDAC	O
CRT_IREF	A13	CRTDAC	O
CRT_IRTN	D12	CRTDAC	O
CRT_RED	B12	CRTDAC	O
CRT_VSYNC	C14	CRTDAC	O
PRDY#	H29	CMOS	O
PREQ#	G29	CMOS	I
DBR_N	E30		
DDI0_AUXN	B8	Diff	I/O
DDI0_AUXP	C8	Diff	I/O
DDI0_DDC_SCL	H25	OD	I/O
DDI0_DDC_SDA	J22	OD	I/O
DDI0_HPD	H22	CMOS	I
DDI0_TXN[0]	G3	Diff	O
DDI0_TXN[1]	F2	Diff	O
DDI0_TXN[2]	C3	Diff	O
DDI0_TXN[3]	A7	Diff	O
DDI0_TXP[0]	G2	Diff	O
DDI0_TXP[1]	F3	Diff	O
DDI0_TXP[2]	D4	Diff	O
DDI0_TXP[3]	B7	Diff	O
DDI1_AUXN	C10	Diff	I/O
DDI1_AUXP	D10	Diff	I/O
DDI1_DDC_SCL	F25	OD	I/O
DDI1_DDC_SDA	G27	OD	I/O
DDI1_HPD	D26	CMOS	I
DDI1_TXN[0]	F11	Diff	O
DDI1_TXN[1]	H11	Diff	O
DDI1_TXN[2]	E13	Diff	O
DDI1_TXN[3]	K13	Diff	O
DDI1_TXP[0]	E11	Diff	O
DDI1_TXP[1]	J11	Diff	O
DDI1_TXP[2]	F13	Diff	O
DDI1_TXP[3]	J13	Diff	O
DDR3_BS[0]	AK12	DDR3_Cntl	O
DDR3_BS[1]	AH13	DDR3_Cntl	O

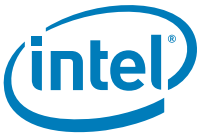


Table 5-49.Processor Ball list by Ball Name (Sheet 3 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
DDR3_BS[2]	AK22	DDR3_Cntl	O
DDR3_CAS#	AJ10	DDR3_Cntl	O
DDR3_CK[0]	AG15	DDR3_Clk	O
DDR3_CK[1]	AF17	DDR3_Clk	O
DDR3_CK[2]	AD17	DDR3_Clk	O
DDR3_CK[3]	AC15	DDR3_Clk	O
DDR3_CK#[0]	AF15	DDR3_Clk	O
DDR3_CK#[1]	AG17	DDR3_Clk	O
DDR3_CK#[2]	AC17	DDR3_Clk	O
DDR3_CK#[3]	AD15	DDR3_Clk	O
DDR3_CKE[0]	AH23	DDR3_Cntl	O
DDR3_CKE[1]	AJ24	DDR3_Cntl	O
DDR3_CKE[2]	AK24	DDR3_Cntl	O
DDR3_CKE[3]	AH24	DDR3_Cntl	O
DDR3_CMDPU	AJ25	Analog	I/O
DDR3_CS#[0]	AH12	DDR3_Cntl	O
DDR3_CS#[1]	AH8	DDR3_Cntl	O
DDR3_CS#[2]	AK11	DDR3_Cntl	O
DDR3_CS#[3]	AK8	DDR3_Cntl	O
DDR3_DM[0]	Y28	DDR3_Ad	O
DDR3_DM[1]	AB26	DDR3_Ad	O
DDR3_DM[2]	AE30	DDR3_Ad	O
DDR3_DM[3]	AB21	DDR3_Ad	O
DDR3_DM[4]	AG11	DDR3_Ad	O
DDR3_DM[5]	AG2	DDR3_Ad	O
DDR3_DM[6]	AB8	DDR3_Ad	O
DDR3_DM[7]	AA3	DDR3_Ad	O
DDR3_DQ[0]	Y30	DDR3_Ad	I/O
DDR3_DQ[1]	Y29	DDR3_Ad	I/O
DDR3_DQ[10]	AE27	DDR3_Ad	I/O
DDR3_DQ[11]	AE26	DDR3_Ad	I/O
DDR3_DQ[12]	AB27	DDR3_Ad	I/O
DDR3_DQ[13]	AA25	DDR3_Ad	I/O
DDR3_DQ[14]	AD25	DDR3_Ad	I/O
DDR3_DQ[15]	AD27	DDR3_Ad	I/O
DDR3_DQ[16]	AD29	DDR3_Ad	I/O
DDR3_DQ[17]	AE29	DDR3_Ad	I/O
DDR3_DQ[18]	AJ30	DDR3_Ad	I/O

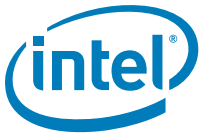


Table 5-49.Processor Ball list by Ball Name (Sheet 4 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
DDR3_DQ[19]	AK29	DDR3_Ad	I/O
DDR3_DQ[2]	AC30	DDR3_Ad	I/O
DDR3_DQ[20]	AD28	DDR3_Ad	I/O
DDR3_DQ[21]	AD30	DDR3_Ad	I/O
DDR3_DQ[22]	AG30	DDR3_Ad	I/O
DDR3_DQ[23]	AJ29	DDR3_Ad	I/O
DDR3_DQ[24]	AE24	DDR3_Ad	I/O
DDR3_DQ[25]	AG24	DDR3_Ad	I/O
DDR3_DQ[26]	AD22	DDR3_Ad	I/O
DDR3_DQ[27]	AC21	DDR3_Ad	I/O
DDR3_DQ[28]	AG27	DDR3_Ad	I/O
DDR3_DQ[29]	AG25	DDR3_Ad	I/O
DDR3_DQ[3]	AC31	DDR3_Ad	I/O
DDR3_DQ[30]	AG21	DDR3_Ad	I/O
DDR3_DQ[31]	AE21	DDR3_Ad	I/O
DDR3_DQ[32]	AD13	DDR3_Ad	I/O
DDR3_DQ[33]	AD11	DDR3_Ad	I/O
DDR3_DQ[34]	AG8	DDR3_Ad	I/O
DDR3_DQ[35]	AG7	DDR3_Ad	I/O
DDR3_DQ[36]	AG13	DDR3_Ad	I/O
DDR3_DQ[37]	AE13	DDR3_Ad	I/O
DDR3_DQ[38]	AD10	DDR3_Ad	I/O
DDR3_DQ[39]	AF8	DDR3_Ad	I/O
DDR3_DQ[4]	W31	DDR3_Ad	I/O
DDR3_DQ[40]	AH2	DDR3_Ad	I/O
DDR3_DQ[41]	AG3	DDR3_Ad	I/O
DDR3_DQ[42]	AD2	DDR3_Ad	I/O
DDR3_DQ[43]	AD3	DDR3_Ad	I/O
DDR3_DQ[44]	AH4	DDR3_Ad	I/O
DDR3_DQ[45]	AK3	DDR3_Ad	I/O
DDR3_DQ[46]	AE2	DDR3_Ad	I/O
DDR3_DQ[47]	AD4	DDR3_Ad	I/O
DDR3_DQ[48]	AD7	DDR3_Ad	I/O
DDR3_DQ[49]	AD6	DDR3_Ad	I/O
DDR3_DQ[5]	W28	DDR3_Ad	I/O
DDR3_DQ[50]	AA6	DDR3_Ad	I/O
DDR3_DQ[51]	AB5	DDR3_Ad	I/O
DDR3_DQ[52]	AE8	DDR3_Ad	I/O

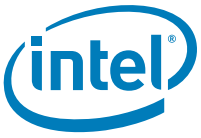


Table 5-49.Processor Ball list by Ball Name (Sheet 5 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
DDR3_DQ[53]	AE5	DDR3_Ad	I/O
DDR3_DQ[54]	AB9	DDR3_Ad	I/O
DDR3_DQ[55]	AA8	DDR3_Ad	I/O
DDR3_DQ[56]	AB2	DDR3_Ad	I/O
DDR3_DQ[57]	AB4	DDR3_Ad	I/O
DDR3_DQ[58]	W4	DDR3_Ad	I/O
DDR3_DQ[59]	V3	DDR3_Ad	I/O
DDR3_DQ[6]	AB28	DDR3_Ad	I/O
DDR3_DQ[60]	AC2	DDR3_Ad	I/O
DDR3_DQ[61]	AB3	DDR3_Ad	I/O
DDR3_DQ[62]	Y2	DDR3_Ad	I/O
DDR3_DQ[63]	W1	DDR3_Ad	I/O
DDR3_DQ[7]	AB30	DDR3_Ad	I/O
DDR3_DQ[8]	AA24	DDR3_Ad	I/O
DDR3_DQ[9]	AA22	DDR3_Ad	I/O
DDR3_DQPU	AK27	Analog	I/O
DDR3_DQS[0]	AA30	DDR3_Ad	O
DDR3_DQS[1]	AB24	DDR3_Ad	O
DDR3_DQS[2]	AF30	DDR3_Ad	O
DDR3_DQS[3]	AE22	DDR3_Ad	O
DDR3_DQS[4]	AG10	DDR3_Ad	O
DDR3_DQS[5]	AF4	DDR3_Ad	O
DDR3_DQS[6]	AB6	DDR3_Ad	O
DDR3_DQS[7]	Y3	DDR3_Ad	O
DDR3_DQS#[0]	AA31	DDR3_Ad	O
DDR3_DQS#[1]	AB25	DDR3_Ad	O
DDR3_DQS#[2]	AF29	DDR3_Ad	O
DDR3_DQS#[3]	AF22	DDR3_Ad	O
DDR3_DQS#[4]	AF10	DDR3_Ad	O
DDR3_DQS#[5]	AF3	DDR3_Ad	O
DDR3_DQS#[6]	AB7	DDR3_Ad	O
DDR3_DQS#[7]	AA2	DDR3_Ad	O
DDR3_DRAM_PWROK	AA5	DDR3_Ana	I
DDR3_DRAMRST#	AK25		O
DDR3_MA[0]	AK14	DDR3_Cntl	O
DDR3_MA[1]	AK16	DDR3_Cntl	O
DDR3_MA[10]	AJ12	DDR3_Cntl	O
DDR3_MA[11]	AK21	DDR3_Cntl	O

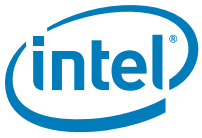


Table 5-49.Processor Ball list by Ball Name (Sheet 6 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
DDR3_MA[12]	AJ21	DDR3_Cntl	O
DDR3_MA[13]	AJ8	DDR3_Cntl	O
DDR3_MA[14]	AH22	DDR3_Cntl	O
DDR3_MA[15]	AJ22	DDR3_Cntl	O
DDR3_MA[2]	AJ14	DDR3_Cntl	O
DDR3_MA[3]	AJ16	DDR3_Cntl	O
DDR3_MA[4]	AK18	DDR3_Cntl	O
DDR3_MA[5]	AH18	DDR3_Cntl	O
DDR3_MA[6]	AJ18	DDR3_Cntl	O
DDR3_MA[7]	AK20	DDR3_Cntl	O
DDR3_MA[8]	AJ20	DDR3_Cntl	O
DDR3_MA[9]	AH20	DDR3_Cntl	O
DDR3_ODT[0]	AK10	DDR3_Cntl	O
DDR3_ODT[1]	AK7	DDR3_Cntl	O
DDR3_ODT[2]	AL9	DDR3_Cntl	O
DDR3_ODT[3]	AJ7	DDR3_Cntl	O
DDR3_ODTPU	AJ26	DDR3_Ana	I/O
DDR3_RAS#	AJ11	DDR3_Cntl	O
DDR3_REFN	AB19		I/O
DDR3_REFP	AC19		I/O
DDR3_VCCA_PWROK	W7	DDR3_Ana	I
DDR3_VREF	AJ27	DDR3_Ana	I
DDR3_VREF_NCTF	AL28	DDR3_Ana	I
DDR3_WE#	AH10	DDR3_Cntl	O
DMI_RCOMP	T1	3GIO_CTC_Ana	I
DMI_REF1P5	T2	3GIO_CTC_Ana	I/O
DMI_REFCLKN	N8	3GIO_CTC_Clk	I
DMI_REFCLKP	N9	3GIO_CTC_Clk	I
DMI_RXN[0]	L2	3GIO_CTC_Rx	I
DMI_RXN[1]	M2	3GIO_CTC_Rx	I
DMI_RXN[2]	N1	3GIO_CTC_Rx	I
DMI_RXN[3]	P3	3GIO_CTC_Rx	I
DMI_RXP[0]	L3	3GIO_CTC_Rx	I
DMI_RXP[1]	M3	3GIO_CTC_Rx	I
DMI_RXP[2]	N2	3GIO_CTC_Rx	I
DMI_RXP[3]	P2	3GIO_CTC_Rx	I
DMI_TXN[0]	K5	3GIO_CTC_Tx	O
DMI_TXN[1]	L6	3GIO_CTC_Tx	O

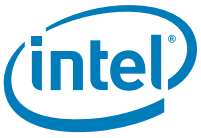


Table 5-49.Processor Ball list by Ball Name (Sheet 7 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
DMI_TXN[2]	L8	3GIO_CTC_Tx	O
DMI_TXN[3]	N6	3GIO_CTC_Tx	O
DMI_TXP[0]	K6	3GIO_CTC_Tx	O
DMI_TXP[1]	L5	3GIO_CTC_Tx	O
DMI_TXP[2]	L9	3GIO_CTC_Tx	O
DMI_TXP[3]	N5	3GIO_CTC_Tx	O
DPL_REFCLKN	A9	Display PLL	I
DPL_REFCLKP	B9	Display PLL	I
DPL_REFSSCCLKN	E17	LVDS_Clk	I
DPL_REFSSCCLKP	F17	LVDS_Clk	I
DPLSLP#	B21	CPU_Sideband	I
DPRSTP#	C21	CPU_Sideband	I
HPLL_REFCLK_N	K19	CMOS	I
HPLL_REFCLK_P	J19	CMOS	I
HV_GPIO_RCOMP	K24	Analog	
INIT#	A23	CMOS	I
INTR/LINT00	D20	CPU_Sideband	I
NMI/LINT10	C22	CPU_Sideband	I
PANEL_BKLTCTL	G22	LVDS	O
PANEL_BKLTEN	E25	LVDS	O
LVDS_CLKN	J4	LVDS	O
LVDS_CLKP	H4	LVDS	O
LVDS_CTRL_CLK	F28	LVDS	I/O
LVDS_CTRL_DATA	E24	LVDS	I/O
LVDS_DDC_CLK	G24	LVDS	I/O
LVDS_DDC_DATA	H24	LVDS	I/O
LVDS_IBG	E10	LVDS	I/O
LVDS_TXN[0]	H10	LVDS	O
LVDS_TXN[1]	E8	LVDS	O
LVDS_TXN[2]	H8	LVDS	O
LVDS_TXN[3]	G6	LVDS	O
LVDS_TXP[0]	G10	LVDS	O
LVDS_TXP[1]	F8	LVDS	O
LVDS_TXP[2]	H7	LVDS	O
LVDS_TXP[3]	G5	LVDS	O
LVDS_VBG	F10	LVDS	O
PANEL_VDDEN	F29	LVDS	O
LVDS_VREFH	H2	LVDS	I

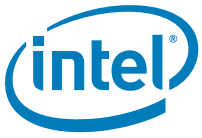


Table 5-49.Processor Ball list by Ball Name (Sheet 8 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
LVDS_VREFL	H3	LVDS	I
MV_GPIO_RCOMP	K23	Analog	
PBE#	C20		O
PROCHOT#	A19	AsyncGTL	I/O
PWRGOOD	D23	CPU Legacy	I
RESET#	G30	CMOS	I
RSVD_W25	W25		
RSVD_W26	W26		
RSVD_N24	N24		
RSVD_N25	N25		
RSVD_L26	L26		
STRAP_L27	L27		
STRAP_K28	K28		
RSVD_K25	K25		
RSVD_J28	J28		
RSVD_K26	K26		
RSVD_K27	K27		
RSVD_H27	H27		
RSVD_K30	K30		
RSVD_L29	L29		
RSVD_L30	L30		
RSVD_K29	K29		
RSVD_J31	J31		
RSVD_H30	H30		
RSVD_L11	L11		
RSVD_L24	L24		
RSVD_E19	E19		
RSVD_F19	F19		
RSVD_K21	K21		
RSVD_L22	L22		
RSVD_R5	R5		
RSVD_R6	R6		
RSVD_C18	C18		
RSVD_TP_R7	R7		
RSVD_TP_R8	R8		
RSVD_TP_AB13	AB13		
RSVD_TP_AB11	AB11		
RSVD_TP_AG19	AG19		

Table 5-49.Processor Ball list by Ball Name (Sheet 9 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
RSVD_TP_AF19	AF19		
RSVD_TP_J15	J15		
RSVD_TP_H15	H15		
RSVD_TP_H17	H17		
RSVD_TP_J17	J17		
SMI#	B18	CPU_Sideband	I/O
STPCLK#	D22	CPU_Sideband	I
SVID_ALERT#	B16	CPU_Legacy	I
SVID_CLK	D18	CPU_Legacy	I
SVID_DATA	C16	CPU_Legacy	I/O
TCLK	C25	CPU_Legacy	I/O
TDI	C24	CPU_Legacy	I/O
TDO	B25	CPU_Legacy	I/O
THERMTRIP#	B20	CPU_Sideband	O
TMS	D24	CPU_Legacy	I/O
TRST#	B24	CPU_Legacy	I/O
VCC_CPU	P18	PWR	-
VCC_CPU	P19	PWR	-
VCC_CPU	P21	PWR	-
VCC_CPU	P28	PWR	-
VCC_CPU	P29	PWR	-
VCC_CPU	P30	PWR	-
VCC_CPU	R22	PWR	-
VCC_CPU	R23	PWR	-
VCC_CPU	R24	PWR	-
VCC_CPU	R25	PWR	-
VCC_CPU	R26	PWR	-
VCC_CPU	R27	PWR	-
VCC_CPU	T19	PWR	-
VCC_CPU	T21	PWR	-
VCC_CPU	T29	PWR	-
VCC_CPU	T30	PWR	-
VCC_CPU	T31	PWR	-
VCC_CPU	U22	PWR	-
VCC_CPU	U23	PWR	-
VCC_CPU	U24	PWR	-
VCC_CPU	U25	PWR	-
VCC_CPU	U26	PWR	-

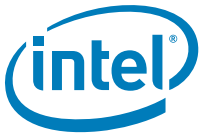


Table 5-49.Processor Ball list by Ball Name (Sheet 10 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VCC_CPU	U27	PWR	-
VCC_CPU	V18	PWR	-
VCC_CPU	V19	PWR	-
VCC_CPU	V21	PWR	-
VCC_CPU	V28	PWR	-
VCC_CPU	V29	PWR	-
VCC_CPU	V30	PWR	-
VCC_CPUSENSE	M28	Analog	-
VCC_GFX	N11	PWR	-
VCC_GFX	N13	PWR	-
VCC_GFX	P11	PWR	-
VCC_GFX	P13	PWR	-
VCC_GFX	R10	PWR	-
VCC_GFX	R9	PWR	-
VCC_GFX	T11	PWR	-
VCC_GFX	T13	PWR	-
VCC_GFX	U10	PWR	-
VCC_GFX	V11	PWR	-
VCC_GFX	V13	PWR	-
VCC_GFXSENSE	U8	Analog	-
VCCACKDDR	W8	DDR PWR	-
VCCACKDDR	W9	DDR PWR	-
VCCADAC	B13	PWR	-
VCCADDR	AA14	DDR PWR	-
VCCADDR	AA16	DDR PWR	-
VCCADDR	W16	DDR PWR	-
VCCADDR	W18	DDR PWR	-
VCCADLLDDR	W11	DDR PWR	-
VCCADLLDDR	W13	DDR PWR	-
VCCADMI	B4	PWR	-
VCCADMI	C5	PWR	-
VCCADMI	A4	PWR	-
VCCADMI_PLLSFR	K4	PWR	-
VCCADP	B5	DP PWR	-
VCCADP	C6	DP PWR	-
VCCADP	D6	DP PWR	-
VCCADP0_SFR	K17	PWR	-
VCCADP1_SFR	L18	PWR	-

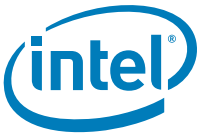


Table 5-49.Processor Ball list by Ball Name (Sheet 11 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VCCAGPIO	D30	PWR	-
VCCAGPIO	D31	PWR	-
VCCAGPIO_DIO	N18	PWR	-
VCCAGPIO_LV	L19	GPIO PWR	-
VCCAGPIO_REF	L16	PWR	-
VCCAHPLL	B26	HPLL PWR	-
VCCALVDS	H5	PWR	-
VCCAZILAON	B29	PWR	-
VCCAZILAON	A30	PWR	-
VCCCKDDR	AJ6	PWR	-
VCCCKDDR	AK6	PWR	-
V_SM	AH14	PWR	-
V_SM	AH19	PWR	-
V_SM	AK23	PWR	-
V_SM	AK5	PWR	-
V_SM	AL11	PWR	-
V_SM	AL16	PWR	-
V_SM	AL21	PWR	-
V_SM	AG31	PWR	-
VCCDIO	L21	VGADAC PWR	-
VCCDLVDS	J1	PWR	-
VCCDMPL	AA11	DDR PWR	-
VCCFHV	V16	FUSES PWR	-
VCCFHV	T16	FUSES PWR	-
VCCFHV	V14	FUSES PWR	-
VCCPLLCPU0	B27	CPU0 PWR	-
VCCPLLCPU1	C29	CPU1 PWR	-
VCCPLLCPU1	B30	CPU1 PWR	-
VCCRAMXXX	N30	SRAM PWR	-
VCCRAMXXX	N31	SRAM PWR	-
VCCRAMXXX	V4	SRAM PWR	-
VCCSFRMPL	AA18	PWR	-
VCCTHRM	K2	PWR	-
VCCTHRM	N16	PWR	-
VSS	A11	GND	-
VSS	A16	GND	-
VSS	A21	GND	-
VSS	A25	GND	-

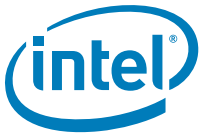


Table 5-49.Processor Ball list by Ball Name (Sheet 12 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VSS	AA1	GND	-
VSS	AA10	GND	-
VSS	AA13	GND	-
VSS	AA19	GND	-
VSS	AA21	GND	-
VSS	AA23	GND	-
VSS	AA26	GND	-
VSS	AA27	GND	-
VSS	AA29	GND	-
VSS	AA7	GND	-
VSS	AA9	GND	-
VSS	AB15	GND	-
VSS	AB17	GND	-
VSS	AB23	GND	-
VSS	AB29	GND	-
VSS	AC1	GND	-
VSS	AC10	GND	-
VSS	AC11	GND	-
VSS	AC13	GND	-
VSS	AC22	GND	-
VSS	AC28	GND	-
VSS	AC4	GND	-
VSS	AD19	GND	-
VSS	AD21	GND	-
VSS	AD24	GND	-
VSS	AD26	GND	-
VSS	AD5	GND	-
VSS	AD8	GND	-
VSS	AE1	GND	-
VSS	AE10	GND	-
VSS	AE11	GND	-
VSS	AE15	GND	-
VSS	AE17	GND	-
VSS	AE19	GND	-
VSS	AE3	GND	-
VSS	AE31	GND	-
VSS	AF11	GND	-
VSS	AF13	GND	-

Table 5-49.Processor Ball list by Ball Name (Sheet 13 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VSS	AF21	GND	-
VSS	AF24	GND	-
VSS	AF28	GND	-
VSS	AF7	GND	-
VSS	AG22	GND	-
VSS	AG5	GND	-
VSS	AH26	GND	-
VSS	AH28	GND	-
VSS	AH6	GND	-
VSS	AH9	GND	-
VSS	AJ2	GND	-
VSS	AJ3	GND	-
VSS	AK13	GND	-
VSS	AK19	GND	-
VSS	AK28	GND	-
VSS	AK9	GND	-
VSS	AL13	GND	-
VSS	AL19	GND	-
VSS	AL23	GND	-
VSS	AL25	GND	-
VSS	AL7	GND	-
VSS	B10	GND	-
VSS	B14	GND	-
VSS	B19	GND	-
VSS	B23	GND	-
VSS	C12	GND	-
VSS	C26	GND	-
VSS	C30	GND	-
VSS	C7	GND	-
VSS	D19	GND	-
VSS	D28	GND	-
VSS	D8	GND	-
VSS	D9	GND	-
VSS	E2	GND	-
VSS	E5	GND	-
VSS	E7	GND	-
VSS	F24	GND	-
VSS	F4	GND	-

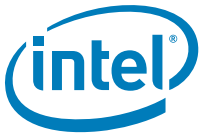


Table 5-49.Processor Ball list by Ball Name (Sheet 14 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VSS	G1	GND	-
VSS	G11	GND	-
VSS	G13	GND	-
VSS	G15	GND	-
VSS	G17	GND	-
VSS	G19	GND	-
VSS	G21	GND	-
VSS	G31	GND	-
VSS	G8	GND	-
VSS	H13	GND	-
VSS	H19	GND	-
VSS	H26	GND	-
VSS	H28	GND	-
VSS	H6	GND	-
VSS	J10	GND	-
VSS	J2	GND	-
VSS	J21	GND	-
VSS	J30	GND	-
VSS	K11	GND	-
VSS	K15	GND	-
VSS	K3	GND	-
VSS	K7	GND	-
VSS	K8	GND	-
VSS	K9	GND	-
VSS	L1	GND	-
VSS	L10	GND	-
VSS	L13	GND	-
VSS	L23	GND	-
VSS	L25	GND	-
VSS	L31	GND	-
VSS	L7	GND	-
VSS	M29	GND	-
VSS	M4	GND	-
VSS	N10	GND	-
VSS	N14	GND	-
VSS	N19	GND	-
VSS	N21	GND	-
VSS	N22	GND	-

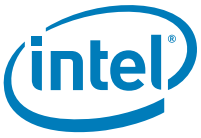


Table 5-49.Processor Ball list by Ball Name (Sheet 15 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VSS	N23	GND	-
VSS	N26	GND	-
VSS	N27	GND	-
VSS	N28	GND	-
VSS	N4	GND	-
VSS	N7	GND	-
VSS	P14	GND	-
VSS	P16	GND	-
VSS	P4	GND	-
VSS	T14	GND	-
VSS	T18	GND	-
VSS	T3	GND	-
VSS	U5	GND	-
VSS	U6	GND	-
VSS	U9	GND	-
VSS	V2	GND	-
VSS	W10	GND	-
VSS	W14	GND	-
VSS	W19	GND	-
VSS	W2	GND	-
VSS	W21	GND	-
VSS	W22	GND	-
VSS	W23	GND	-
VSS	W24	GND	-
VSS	W27	GND	-
VSS	W30	GND	-
VSS	W5	GND	-
VSS	W6	GND	-
VSS	Y4	GND	-
VSS	A27	GND	-
VSS	A29	GND	-
VSS	A3	GND	-
VSS	AH1	GND	-
VSS	AJ1	GND	-
VSS	AJ31	GND	-
VSS	AK1	GND	-
VSS	AK2	GND	-
VSS	AK30	GND	-

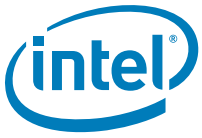


Table 5-49.Processor Ball list by Ball Name (Sheet 16 of 16)

EDS Ball List	Pkg Ball	Buffer Type	Direction
VSS	AK31	GND	-
VSS	AL2	GND	-
VSS	AL29	GND	-
VSS	AL3	GND	-
VSS	AL30	GND	-
VSS	AL5	GND	-
VSS	B2	GND	-
VSS	B3	GND	-
VSS	B31	GND	-
VSS	C1	GND	-
VSS	C2	GND	-
VSS	C31	GND	-
VSS	E1	GND	-
VSS_CDVDET	L14	GND	-
VSS_CPUSENSE	M30	Analog	-
VSS_GFXSENSE	U7	Analog	-
VSSA_CRTDAC	D13	GND	-

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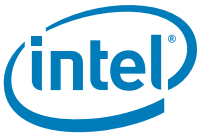


6 Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is important that the design ensures acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation and for interpreting results for signal quality measurements of actual designs.

6.1 Signal Quality Specifications and Measurement Guidelines

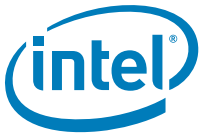
Various scenarios have been simulated to generate a set of layout guidelines which are available in the Next Generation Intel® Atom™ Processor based desktop platform design guides.

Table 6-50 provide the signal quality specifications for all processor signals for use in simulating signal quality at the processor core silicon (pads). Figure 6-16 illustrates the overshoot, undershoot, and ringback measurements.

6.1.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage (or below V_{SS}) as shown in Figure 6-16. The overshoot guideline limits transitions beyond V_{TT} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Permanent damage to the processor is the likely result of excessive overshoot/ undershoot.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modelled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the interfaces, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.



6.1.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to V_{SS}. It is important to note that overshoot and undershoot conditions are separated and their impact must be determined independently.

Overshoot/undershoot magnitude levels must comply to the absolute maximum specifications listed in Table 6-50. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations.

6.1.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

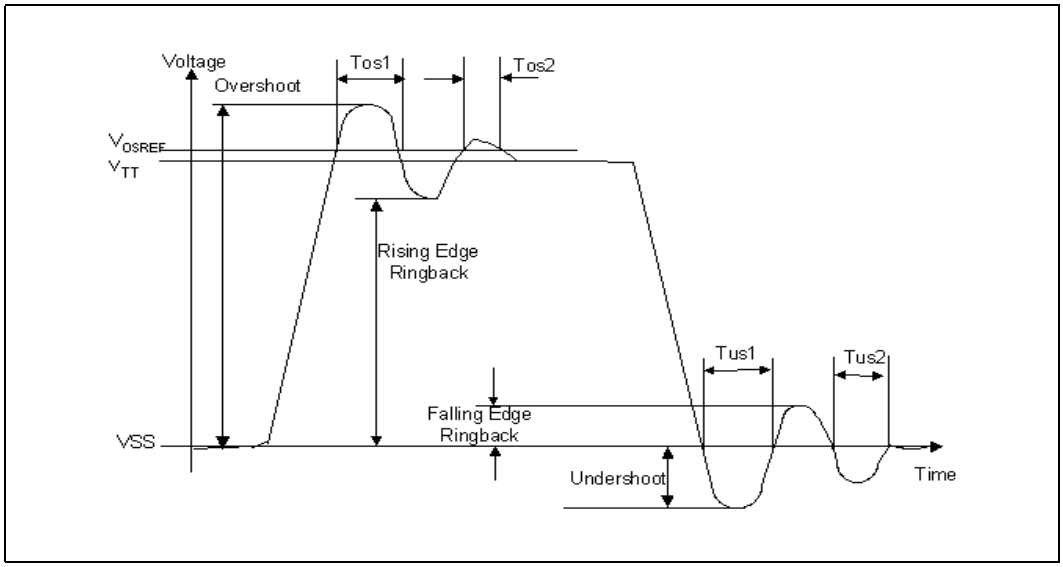
Note: *Oscillations* below *the reference voltage can not be subtracted from the total overshoot/undershoot pulse duration.*

Table 6-50. Input Signal Group Ringback Duration Specification

		Max OS limit	Max US limit	Duration	Note
DDR	VCCSM	1.2*VCCSM	-0.1*VCCSM	0.25 * Tch	
Misc. signals	Vxx	1.2 * Vxx	- 0.1 * Vxx	0.25 * Tch	1, 2
BCLK/HCLK/REFCLK/ REFSSCLK		1.15	- 0.3		3

NOTES:
1. Tch = clock high time period for the specific signal.
2. Other signals include CRTDAC, DIM, LGI, GIO, xPLL.
3. The maximum OS/US limits for clock signals are limited by reliability. However within these limits, the permissible Vcc* is entirely dependent on functionality requirement.

Figure 6-16.Overshoot, Undershoot, and Ringback Illustration



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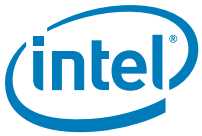


7 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- Integrated Memory Controller (IMC)
- Direct Media Interface (DMI)
- Integrated Graphics Controller

Note: Reliability is not assured if the P unit to VRM communication is not working properly

7.1 ACPI state Supported

The ACPI states supported by the processor are described in this section.

7.1.1 System States

Table 7-51.System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory.
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on Chipset)
G2/S5	Soft off. All power lost (except wakeup on Intel NM10 Express Chipset). Total reboot. (swh - I changed to ecpd_2#)
G3	Mechanical/hard off. All power (AC and battery) (AC and battery) removed from system.

7.1.2 Processor Idle States

Table 7-52.Processor Core/ States Support (Sheet 1 of 2)

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C2	Stop Clock. Clock to processor is still running. Clock stopped to processor core
C3/C4	Deeper Sleep. Clock to processor stopped with reduced voltage on the processor

Table 7-52.Processor Core / States Support (Sheet 2 of 2)

State	Description
Deep Power Down Technology (code named C6)	Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage completely shutoff. The two Intel Atom Processor D2000 series and N2000 series processor threads will enter TC6 state independent of each other. Each thread will save its state into a dedicated on die SRAM. The last thread to enter TC6 will shrink the L2 cache.
C1E, C2E, C4E	Extended C-state; C1/C2/C4 states work together with Enhanced Intel SpeedStep Technology

7.1.3 Integrated Graphics Display States

Table 7-53.Integrated Graphics Display Device Control

State	Description
D0	Full on, Display active
D3	Power off display

7.1.4 Integrated Memory Controller States

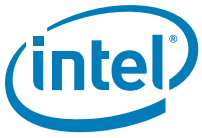
Table 7-54.Main Memory States

States	Description
Powerup	CKE asserted. Active mode.
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed.
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active.
Self-Refresh	CKE de-asserted using device self-refresh

7.1.5 DMI States

Table 7-55.DMI States

States	Link System States	Description
L0	C0 - C6	Full on – Active transfer state.
L0s	C0 - C6	First Active Power Management low power state – Low exit latency.
L1	C2 - C4	Lowest Active Power Management - Longer exit latency.
L3	S3, S4 and S5	Lowest power state (power-off) – Longest exit latency.



7.1.6 Interface State Combinations

Table 7-56.G, S and C State combinations

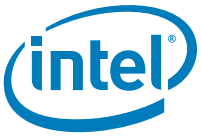
Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C2/C2E	Stop-Grant	On	Stop-Grant
G0	S0	C4/C4E	Deeper Sleep	On	Deeper Sleep
G1	S3	Power off		Off except RTC	Suspend to RAM
G1	S4	Power off		Off except RTC	Suspend to Disk
G2	S5	Power off		Off except RTC	Soft Off
G3	NA	Power Off		Power off	Hard Off

Table 7-57.D, S and C state Combinations

Graphics Adapter (D) State	Sleep (S) State	(C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C2/C4	Stop Grant/ Deeper Sleep, Displaying
D3	S0	Any	Not Displaying
D3	S3		Not Displaying Uncore host core power off.
D3	S4		Not Displaying Suspend to disk Uncore host core power off

7.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-state have longer entry and exit latencies.



7.2.1 Enhanced Intel SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep Technology:

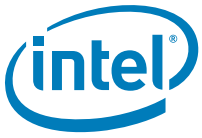
- Applicable to Processor Core Voltage and Graphic Core Voltage (N2000 series only)
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
  - If the target frequency is higher than the current frequency, VCC is ramped up in steps to an optimized voltage. This voltage is signaled by the VID pins to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the VID pins.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.
- Improved Thermal Monitor mode.
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.

7.2.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.



7.2.3 Low-Power Idle States

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-state. However, higher C-state have longer exit and entry latencies. Resolution of C-state occur at the thread, processor core, and processor core level. Thread level C-state are available if Hyper-Threading Technology is enabled.

7.2.3.1 Clock Control and Low-Power States

The processor core supports low power states at the thread level and core/ level. Thread states (TCx) loosely correspond to ACPI processor core power states (Cx). A thread may independently enter TC1/AutoHALT, TC1/MWAIT, TC2, TC3 and TC4 lower power states, but this does not always cause a power state transition. Only when both threads request a low-power state (TCx) greater than the current processor core state will a transition occur. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done by initiating a P_LVLx (P_LVL2, P_LVL3, P_LVL4) I/O read to both threads. States that require external intervention and typically map back to processor core power states. States for processor core include Normal (C0, C1), and Stop Grant, Stop Grant Snoop (C2), and Deeper Sleep (C4).

The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR by BIOS. If a thread encounters a chipset break even while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# (multifunction of FERR#) when STPCLK# is asserted indicates to system logic that individual threads should return to the C0 state and the processor core should return to the Normal state.

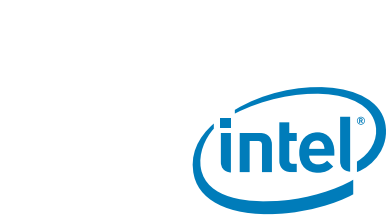
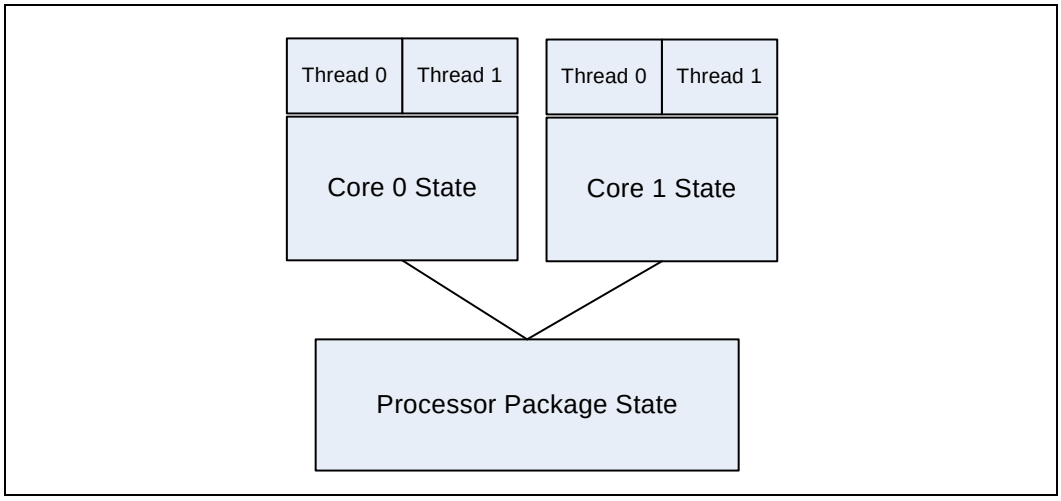
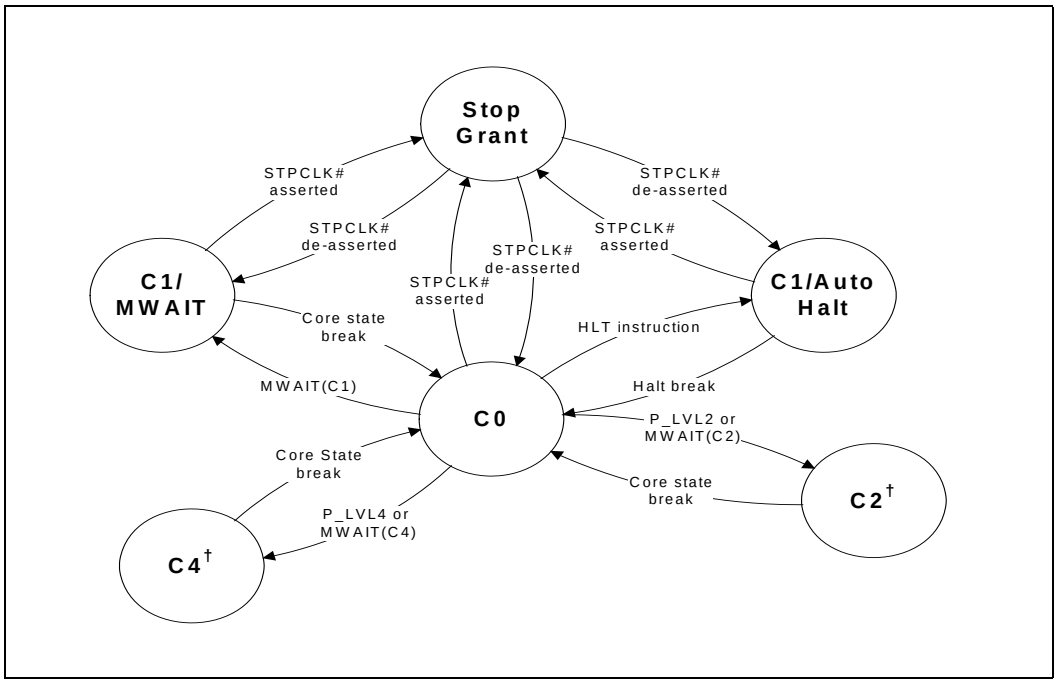


Figure 7-17.Idle Power Management Breakdown of the Processor Cores



Entry and exit of C-states at the thread and core level are show in Figure 7-18

Figure 7-18.Thread and Core C-state Entry and Exit



Note: halt break = A20M# transition, INIT#, LINT01, LINT00, PREQ#, SMI# or APIC interrupt.

Note: core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)

Note: STPCLK# assertion and de-assertion have no effect if a thread is in C2 state.

Figure 7-19.Processor Core Low-Power States

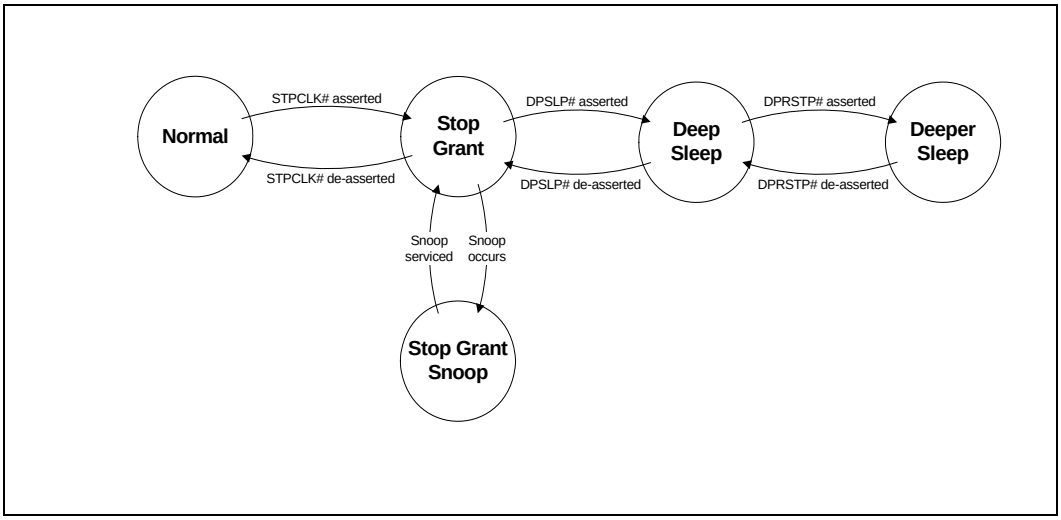


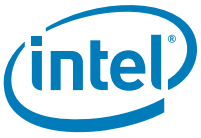
Table 7-58.Coordination of Thread Low-power States at the /Core Level

Processor Core C-State		Thread 1					
		C0	C1	C2	C3	C4	C6
Thread 0	C0	C0	C0	C0	C0	C0	C0
	C1	C0	C1	C1	C1	C1	C1
	C2	C0	C1	C2	C2	C2	C2
	C3	C0	C1	C2	C3	C3	C3
	C4	C0	C1	C2	C3	C4	C4
	C6	C0	C1	C2	C3	C4	C6

7.2.4 Graphics Power Management

7.2.4.1 Graphics and video decoder C-State

GFX C-State (GC6) and VED C-State (VC6) are techniques designed to optimize the average power to the graphics and video decoder engines during times of idleness. GFX C-state is entered when the graphics engine, has no workload being currently worked on and no outstanding graphics memory transactions. Using the same concept, VED C-state is entered when the video decoder engine has no workload being currently worked on and no outstanding video memory transactions. When the idleness condition is met, the Processor will power gate the Graphics and video decoder engines.



7.2.4.2 Intel® Display Power Saving Technology (Intel® DPST)

This is a mobile only supported power management feature. The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel® DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image. Intel DPST 5.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

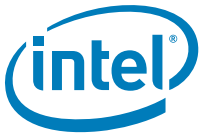
7.2.4.3 Intel® Automatic Display Brightness

This is a mobile only supported power management feature. Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the back light setting.

7.2.4.4 Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology)

This is a mobile only supported power management feature. When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel® Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the notebook is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel SDRRS—static and seamless. The static Intel SDRRS method uses a mode change to assign the new refresh rate. The seamless Intel SDRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.



7.2.5 Thread C-state Description

7.2.5.1 Thread C0 State

This is the normal operating state for threads in the processor core.

7.2.5.2 Thread C1/AutoHALT Powerdown State

C1/AutoHALT is a low-power state entered when one thread executes the HALT instruction while the other is in the TC1 or greater thread state. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT00/LINT10 (NMI, INTR), or internal bus interrupt messages. RESET# will cause the processor core to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT power down state. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate STPCLK# while the processor core is in the AutoHALT power down state. When the system de-asserts the STPCLK# interrupt, the processor core will return to the HALT state.

While in AutoHalt power down state, the processor core will process bus snoops. The processor core will enter an internal snoopable sub-state to process the snoop and then return to the AutoHALT power down state.

7.2.5.3 Thread C1/MWAIT Power-down State

C1/MWAIT is a low-power state entered when one thread executes the MWAIT (C1) instruction while the other thread is in the TC1 or greater thread state. Processor core behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. Refer to the *Intel® 64 and* IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set *Reference, A-M and Volume 2B: Instruction Set Reference, N-Z*, for more information.

7.2.5.4 Thread C2 State

Individual threads of the dual-threaded processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the processor will process bus snoops and snoops from the other thread. The processor thread will enter a snoopable sub-state to process the snoop and then return to the C2 state.

7.2.5.5 Thread C4 State

Individual threads of the processor can enter the C4 state by initiating a P_LVL4 I/O read to the P_BLK or an MWAIT(C4) instruction. If both processor threads are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep low-power state.

To enable the level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the PMG_CST_CONFIG_CONTROL MSR.

7.2.6 Processor Core / C-states Description

The following state descriptions assume that both threads are in common low power state. For cases when only 1 thread is in a low power state, no change in Core/ Power state will occur.

7.2.6.1 Core C0 State

The normal operating state of a core where code is being executed.

7.2.6.2 Core C1 / C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. Refer to the Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, Refer to "Package C1/C1E".

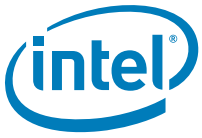
7.2.6.3 C2 State

Individual threads of the dual-threaded processor core can enter TC2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT (C2) instruction. Once both threads have C2 as a common state, the processor core will transition to the C2 state; however, the processor core will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted by the chipset.

While in the C2 state, the processor core will process bus snoops. The processor core will enter a snoopable sub-state to process the snoop and return to the C2 state.

7.2.6.4 C4 State

Individual threads of a core can enter the C4 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C4) instruction. A core in C4 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C4 state when either a snoop is detected or when another core accesses cacheable memory.



7.2.6.5 C6 State

Individual threads of a core can enter the C6state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM.Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

7.2.6.6 C-State Auto-Demotion

In general, deeper C-states such as C6 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore incorrect or inefficient usage of deeper C-states have a negative impact on battery life. In order to increase residency and improve battery life in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C6 to C3
- C6/C3 To C1

The decision to demote a core from C6 to C3 or C3/C6 to C1 is based on each core's immediate residency history. Upon each core C6 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

7.2.7 Package C-States

The processor supports C0, C1/C1E, C2/C2E, C4/C4E and C6 power states. The following is a summary of the general rules for package C-state entry. These apply to all package Cstates unless specified otherwise:

- Package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
- Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
- The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.

- If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
- If the break event is masked, the processor attempts to re-enter its previous package state.

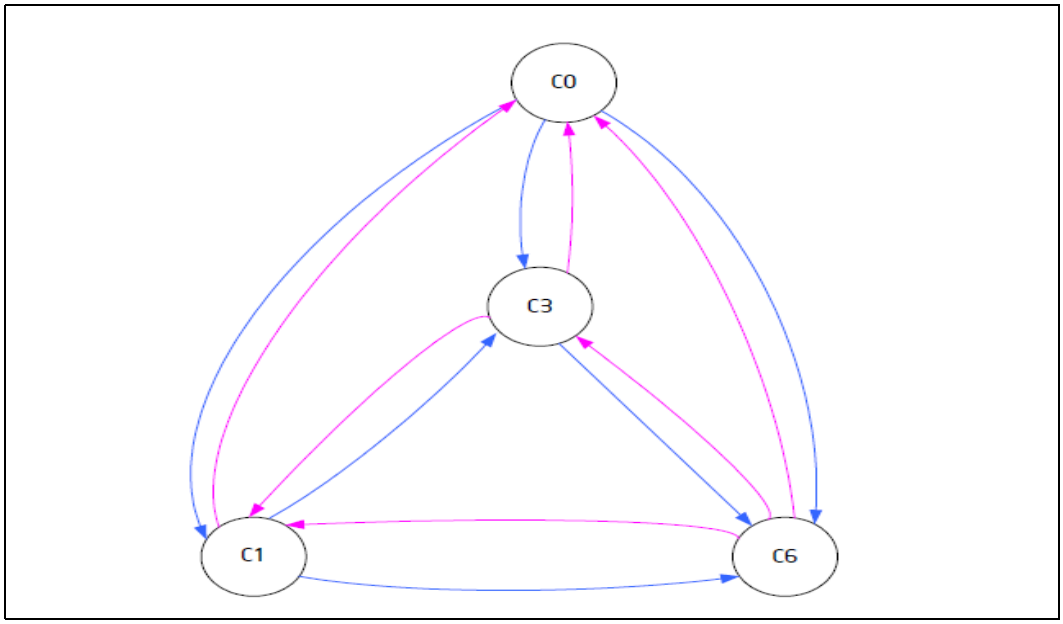
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package Cstate, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

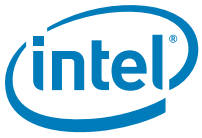
Table 7-59.Coordination of Core Power States at the package Level

Package C-State		Core 1					
		C0	C1	C2	C3	C4	C6
Core 0	C0	C0	C0	C0	C0	C0	C0
	C1	C0	C1	C1	C1	C1	C1
	C2	C0	C1	C2	C2	C2	C2
	C3	C0	C1	C2	C3	C3	C3
	C4	C0	C1	C2	C3	C4	C4
	C6	C0	C1	C2	C3	C4	C6

NOTE: 1. If enabled, the package C-state will be C1E if all actives cores have resolved a core C1 state or higher.

Figure 7-20.Package C-state Entry and Exit





7.2.7.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

7.2.7.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E via MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower thatC1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES. No notification to the system occurs upon entry to C1/C1E.

7.2.7.3 Package C3 State

A processor enters the package C3 low power state when:

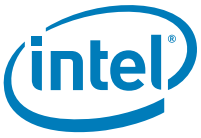
- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6 state but has allowed a package C6 state.

In package C3-state, the L3 shared cache is snoopable.

7.2.7.4 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 request but has allowed a C6 package state.



In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The L3 shared cache is still powered and snoopable in this state. The processor remains in package C6 state as long as any part of the L3 cache is active.

7.2.7.5 Power Status Indicator (PSI#) and DPRSLPVR#

PSI# and DPRSLPVR# are signals used to optimize VR efficiency over a wide power range depending on amount of activity within the processor core. The PSI# signal is utilized by the processor core to:

- Improve intermediate and light load efficiency of the voltage regulator when the processor is active (P-states).
- Optimize voltage regulator efficiency in very low power states. Assertion of DPRSLPVR# indicates that the processor core is in a C6 low power state.

The VR efficiency gains result in overall platform power savings and extended battery life.

7.3 IMC Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

7.3.1 Disabling Unused System Memory Outputs

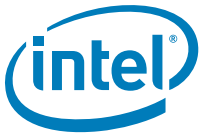
Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an SO-DIMM present, the DIMM is not guaranteed to maintain data integrity.

SCKE tristate should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.



7.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

7.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during powerup.

CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

7.3.2.2 Conditional Self-Refresh

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package C3 and C6 low-power states. RMPM functionality depends on graphics/display state (relevant only when internal graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

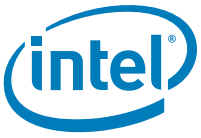
When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then enters all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package C3 and C6 states as long as there are no memory requests to service.

7.3.2.3 Dynamic Power Down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state.The processor core controller can be configured to put the devices in active power down (CKE deassertion with open pages) or precharge power down (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.



7.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

7.4 DMI Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

7.4.1 Stop-Grant State

When STPCLK# pin is asserted, each thread of the processor cores enter the Stop-Grant state within 1384 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. When the STPCLK# pin is deasserted, the core returns to its previous low-power state.

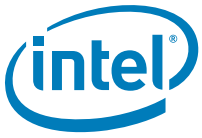
RSTIN# causes the processor core to immediately initialize itself, but the processor core will stay in Stop-Grant state. When RSTIN# is asserted by the system, the STPCLK#, DPSLP#, and DPRSTP# pins must be de-asserted prior to RSTIN# deassertion as per AC Specification.

While in Stop-Grant state, the processor core will service snoops and latch interrupts delivered on the internal bus. The processor core will latch SMI#, INIT# and LINT[1:0]

interrupts and will service only one of each upon return to the Normal state.

The PBE# (FERR#) signal may be driven when the processor core is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor core. Pending interrupts that are blocked by the EFLAGS. IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor core should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor core detects a snoop on the internal bus.



7.4.2 Stop-Grant Snoop State

The processor core responds to snoop or interrupt transactions on the internal bus while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor core will stay in this state until the snoop on the internal bus has been serviced (whether by the processor core or another agent on the internal bus) or the interrupt has been latched. The processor core returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

7.4.3 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. Deep Sleep State is mapped into the Deeper Sleep State for this processor.

BCLK stop/restart timings on appropriate chipset-based platforms with the clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tri-state BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit**: the system clock chip must start toggling BCLK within 10 BCLK periods within DPSLP# de-assertion.

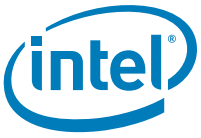
7.4.4 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID [6:0] pins. Exit from Deeper Sleep is initiated by DPRSTP# de-assertion when the core requests a state other than C4 or the core requests a processor performance state other than the lowest operating point.

7.4.5 Extended Low-Power States

Extended low-power states (C1E, C2E, C4E) optimize for power by forcibly reducing the performance state of the processor when it enters a low-power state. Instead of directly transitioning into the low-power state, the extended low-power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the low-power state, control will be returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the low power states. **Also, long-term reliability may not** be assured if the Extended Low-Power States are not enabled.



The processor implements two software interfaces for requesting extended low-power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring IA32_MISC_ENABLES MSR bits to automatically promote low-power states to extended low-power states. Extended Stop-Grant and Extended Deeper Sleep must be enabled via the BIOS for the processor to remain within specification. Not complying to this guideline may affect the long-term reliability of the processor.

Enhanced Intel SpeedStep Technology transitions are multi-step processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep low-power states since processor clocks are not active in these states. Extended Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in the IA32_MISC_ENABLES MSR. This Extended Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency.

The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

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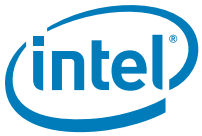


8 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section Thermal Specifications. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsink attached to the exposed processor die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a system fan used to evacuate or pull air through the system. For more information on designing a component level thermal solution. Alternatively, the processor may be in a fan-less system, but would likely still use a multi-component heat spreader. Note that trading of thermal solutions also involves trading performance.

8.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 8-60. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design.

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 8-60 instead of the maximum processor power consumption. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section Section 8.1.1. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

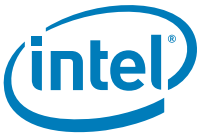


Table 8-60.Power Specifications for the Standard Voltage Processor (Updated)

Symbol	Processor Number	Core Frequency / GHz	Thermal Design Power	Unit	Tj min (°C)	Tj max (°C)	Notes
TDP	N2600	1.6	<=3.5	W	0	100	
	N2650	1.7	<=3.6	W		100	
	N2800	1.86	<=6.5	W		100	
	N2850	2.0	<=6.6	W		100	
	D2500	1.86	<=10	W		100	
	D2550	1.86	<=10	W		100	
	D2700	2.13	<=10	W		100	
Symbol	**Parameter**		**Max**	**Unit**			
$P_{AVERAGE}$	N2600		~1.09	W	0	50	
	N2650		~1.10	W			
	N2800		~1.81	W			
	n2850		~1.7	W			
P_{IDLE}	D2500		~2.72	W	0	50	
	D2550		~2.74	W			
	D2700		~2.74	W			

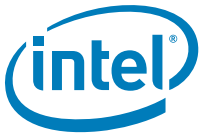
NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
4. V_{CC} is determined by processor VID[6:0].
5. Silicon projection.

The processor incorporates 2 methods of monitoring die temperature: Digital Thermal Sensor and Intel Thermal Monitor. The Intel Thermal Monitor (detailed in Section Section 8.1.1) must be used to determine when the maximum specified processor junction temperature has been reached.

8.1.1 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and



may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

Intel Thermal Monitor 1 (TM1 & TM2) mode is selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

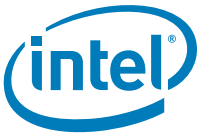
When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.



If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 4.

8.1.2 Digital Thermal Sensor

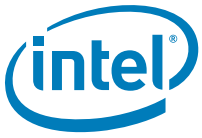
The processor also contains an on die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal level low power state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Spec status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor 1(TM1) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 hardware thermal control mechanism will activate. The DTS and TM1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

Note: The Digital Thermal Sensor (DTS) accuracy is in the order of -5°C to +5°C between 60°C and 100°C. It deteriorates to -10°C to +10°C between 25°C and 60°C. The DTS temperature reading saturates at some temperature below 25°C. Any DTS reading



below 25°C should be considered to indicate only a temperature below 25°C and not a specific temperature.

8.1.3 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 is triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt. For more details on the interrupt mechanism.

8.1.4 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a level of the processor. When the core's thermal sensor trips, PROCHOT# signal will be driven by the processor. If TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clock modulated. It is important to note that Intel recommends TM1 to be enabled.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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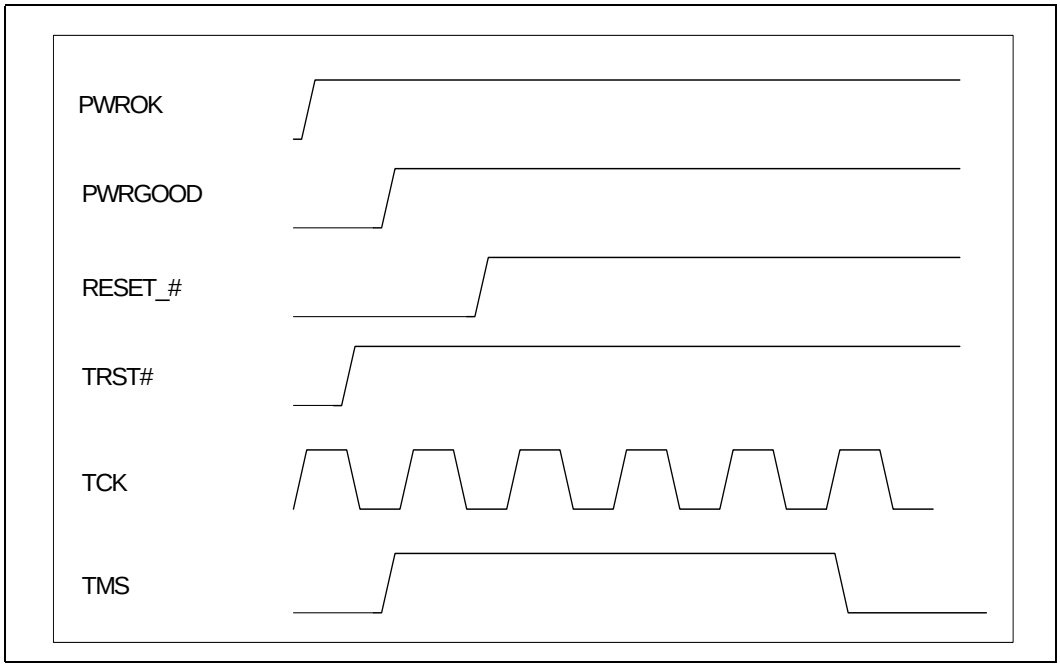
9 Testability

In Intel Atom Processor SC and DC Series, testability for Automated Test Equipment (ATE) board level testing has been implemented as JTAG boundary scan.

9.1 JTAG Boundary Scan

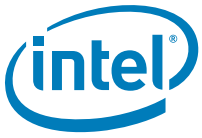
The Intel Atom Processor D2000 and N2000 series add Boundary Scan ability compatible with the IEEE 1149.1-2001 Standard (Test Access Port and Boundary-Scan Architecture) specification. Refer to following figure for test mode entry.

Figure 9-21.JTAG Boundary Scan Test Mode Initialization Cycles



TRST# can be deasserted any time after PWROK. After TRST# deassertion, it is advisable (but not compulsory) to keep TMS high for at least 5 TCKs.

There are no straps or other clocks that need to be driven during BScan. All power rails need to be supplied with power during Boundary scan



9.2 TAP Instructions and Opcodes

The TAP controller supports the JTAG instructions as listed in table below. The instruction register length is 6 bits. For details of the boundary-scan register.

Table 9-61.Supported TAP Instructions

Opcode (Binary)	Instruction	Selected Test Data Register	TDR Length
000000	EXTEST	Boundary Scan	413
000001	SAMPLE	Boundary Scan	413
000011	IDCODE	Device Identification	32
000100	CLAMP	Bypass	1
000101	EXTEST_TOGGLE	Boundary Scan	413
001000	HIGHZ	Bypass	1
111111	BYPASS	Bypass	1
Others	Reserved		

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10 Debug Tool Specifications

The ITP-XDP debug port connector is the recommended debug port for platforms using Intel Atom Processor SC and DC Series. Refer to the appropriate Debug Port Design Guide and Platform Design Guide for more detailed information regarding debug tools specifications. Contact your Intel representative for more information.

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DF8064101211300S R0VY DF8064101055400S R0W0 DF8064101050503S R0W1 DF8064101050706S R0W2 DF8064101211300S R0QB