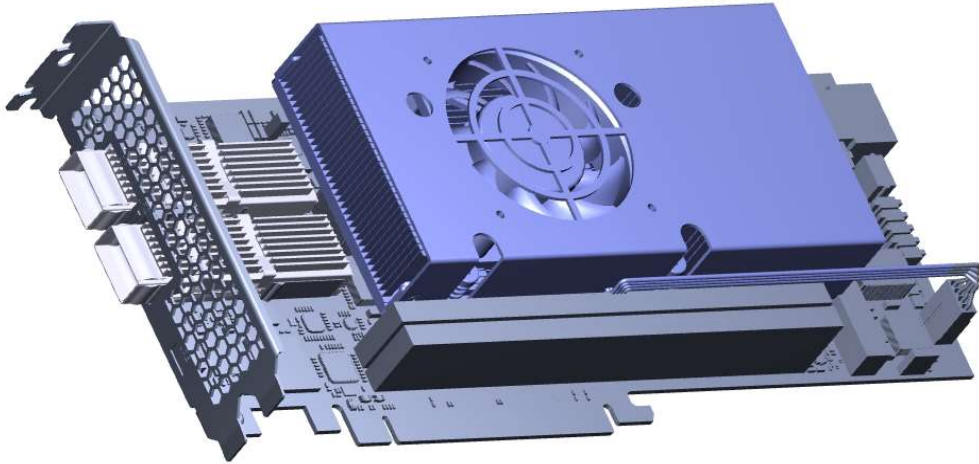
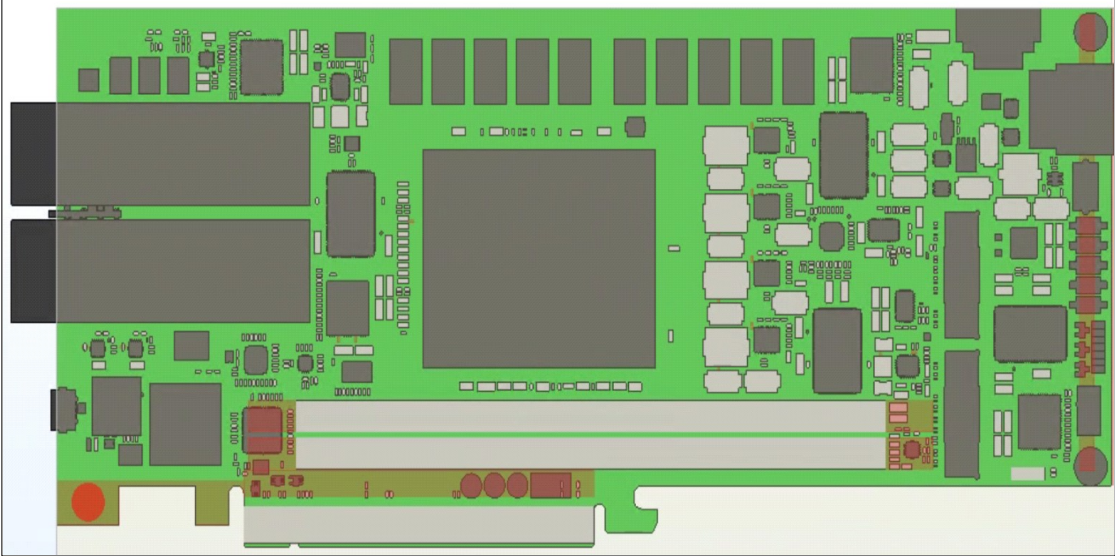


PAGE	DESCRIPTION	PAGE	DESCRIPTION
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37	FPGA Power 1	75	PWR - VCCCLK_GXR
38	FPGA Power 2	76	Decoupling Caps 1
		77	Decoupling Caps 2

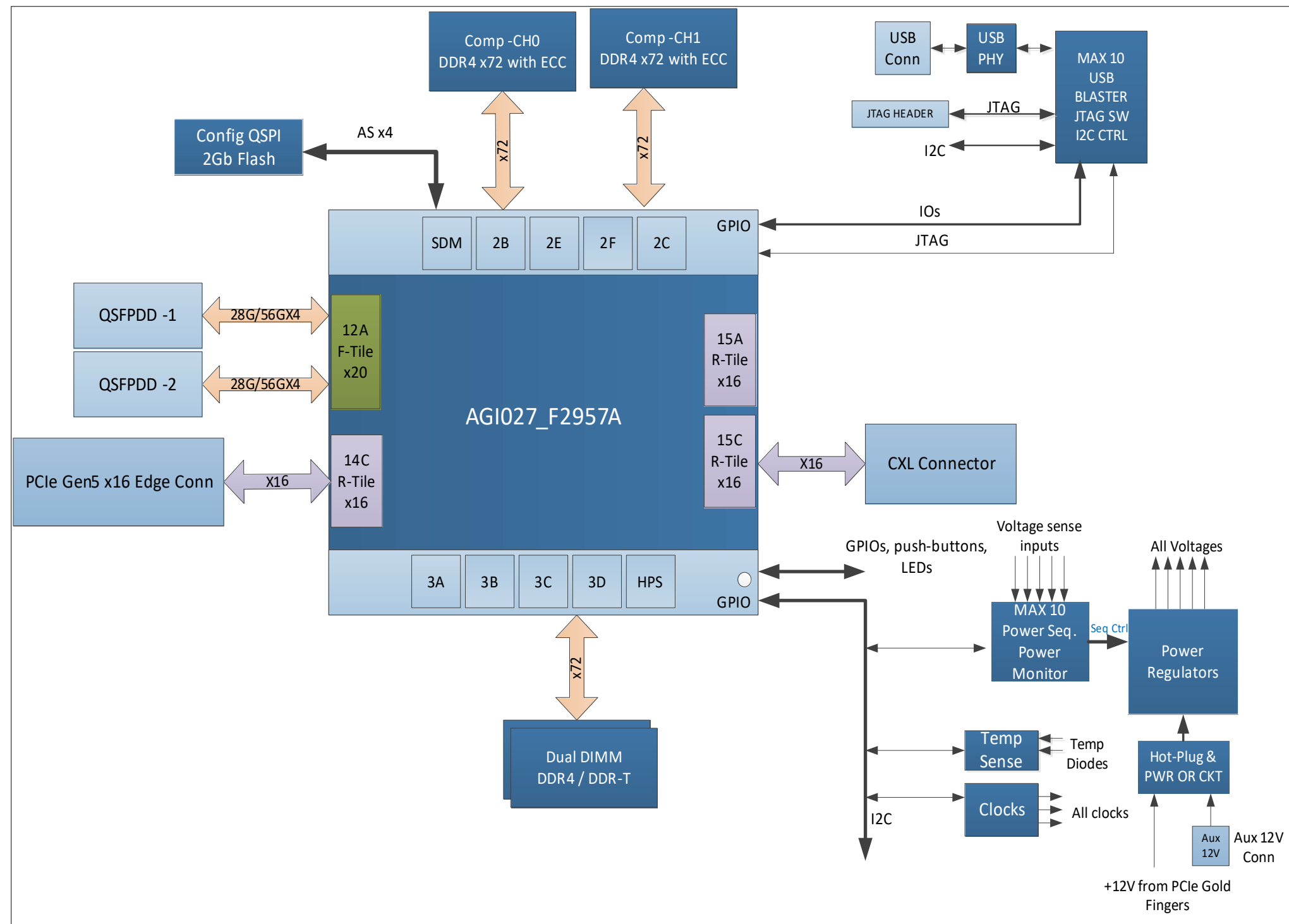
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SPEED Item			
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Gerber Files		150-0330672-A1	
Schematic Design File	M17472	180-0330672-A1	
PBA BOM	M17471-100		



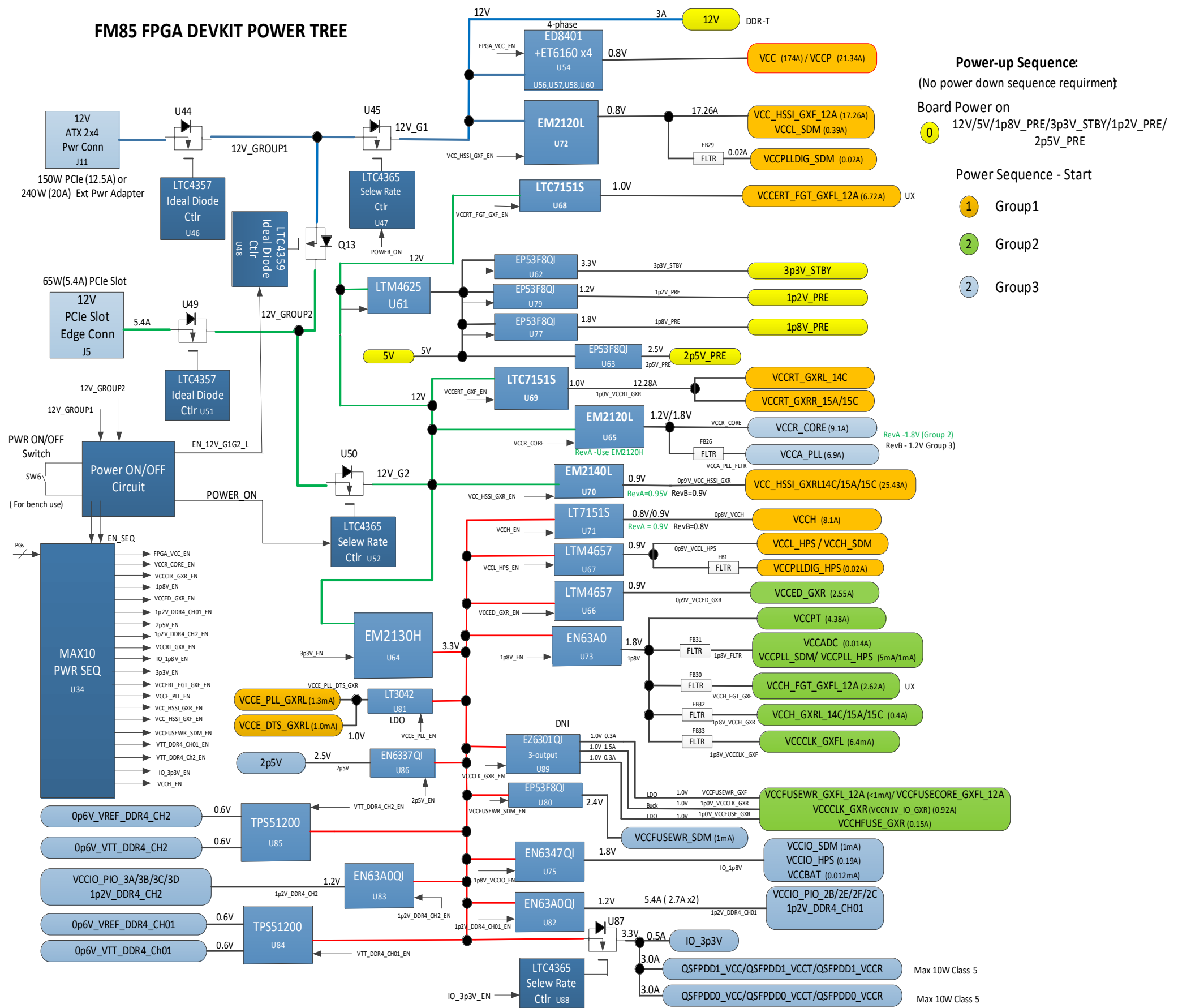
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System Block Diagram

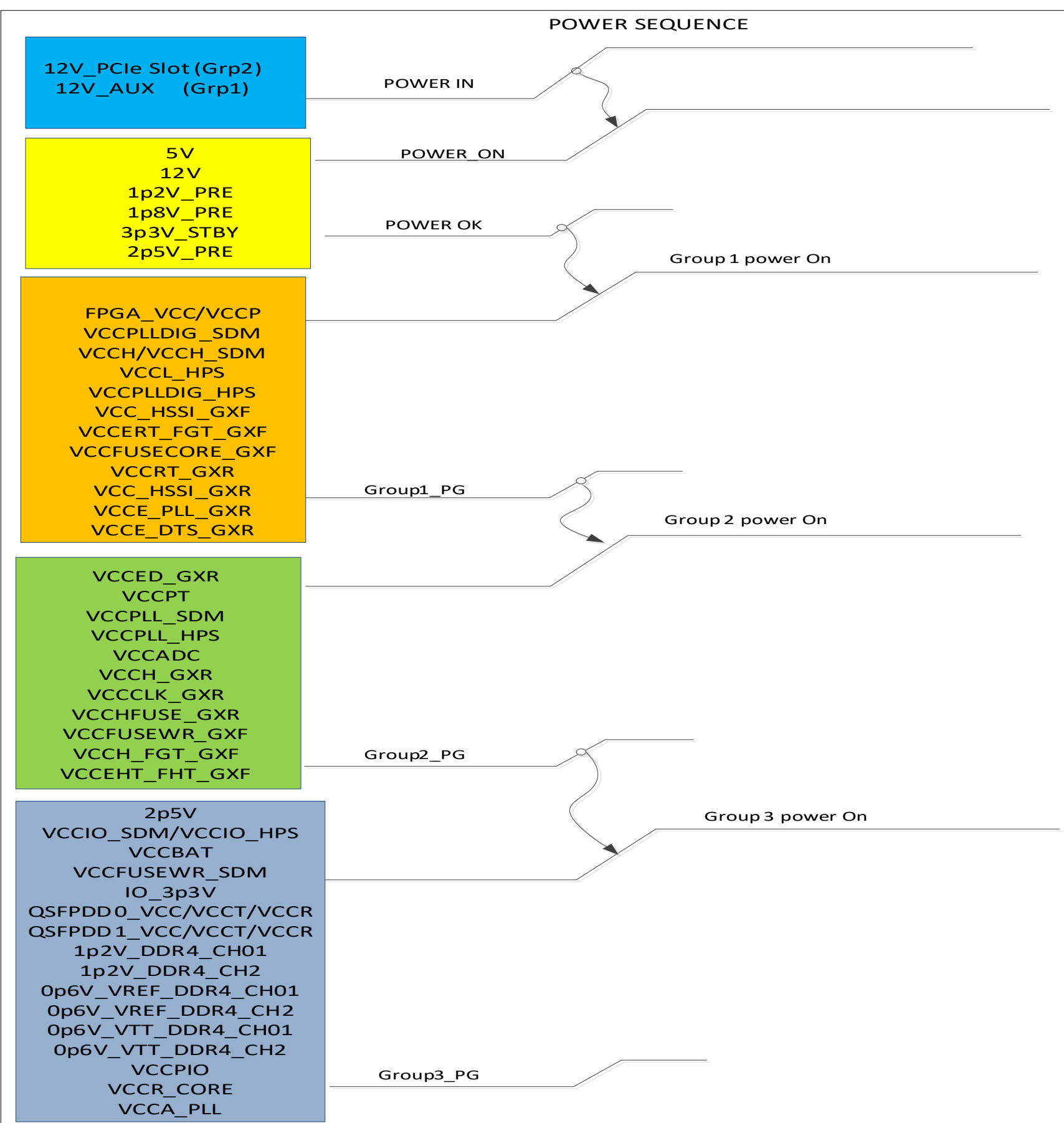


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FM85 FPGA DEVKIT POWER TREE



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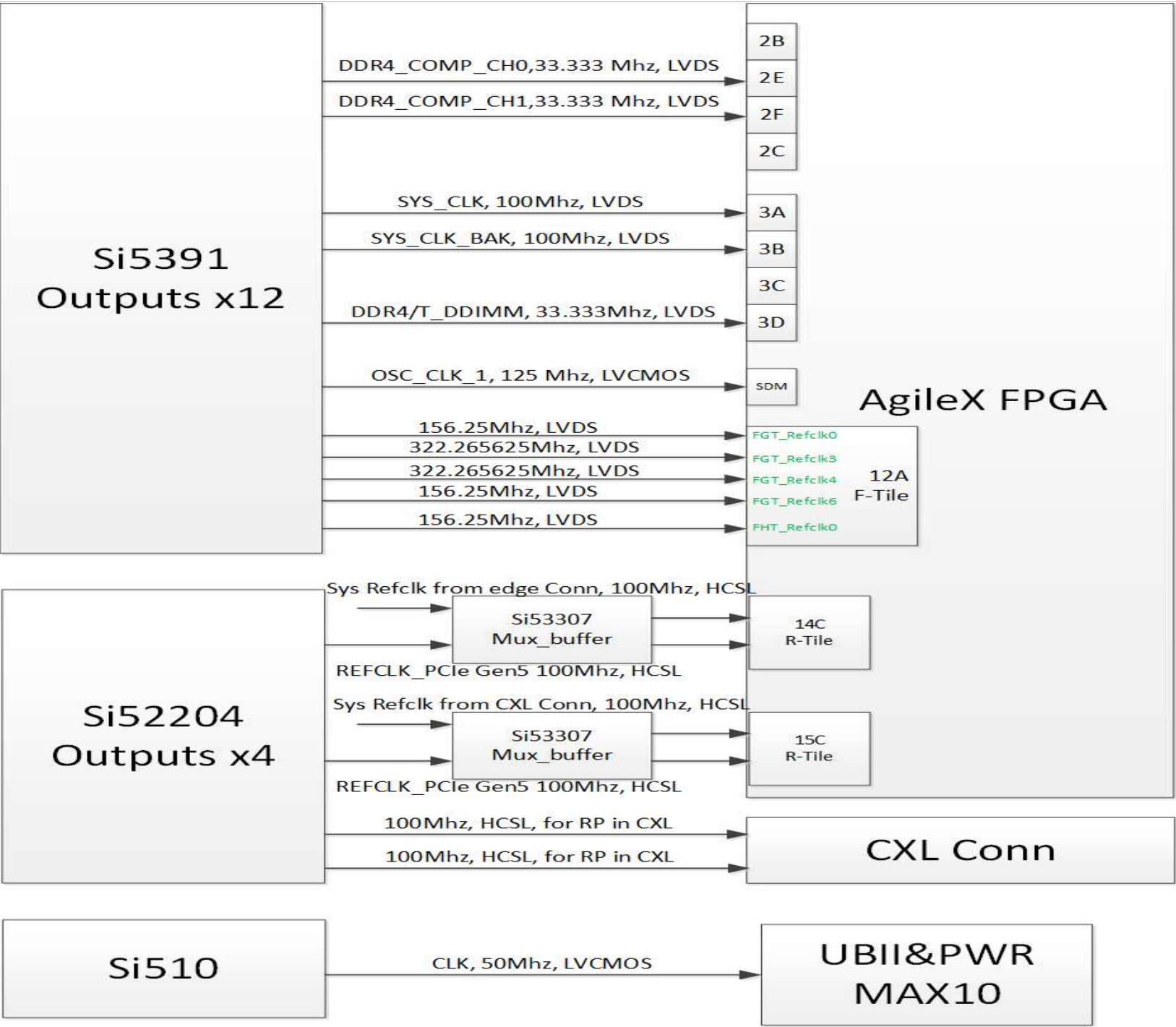


Power Sequence Diagram



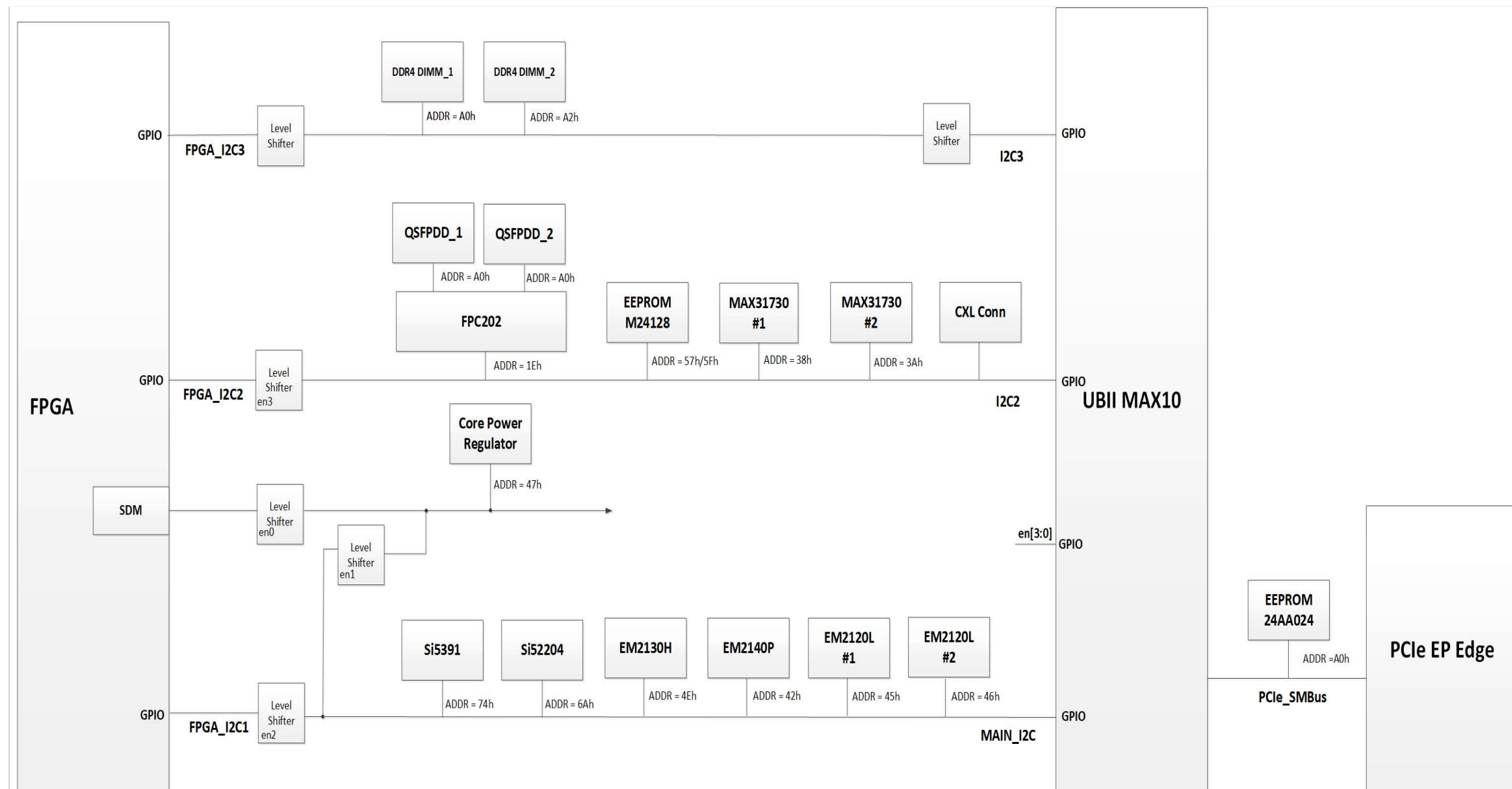
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Clock Tree



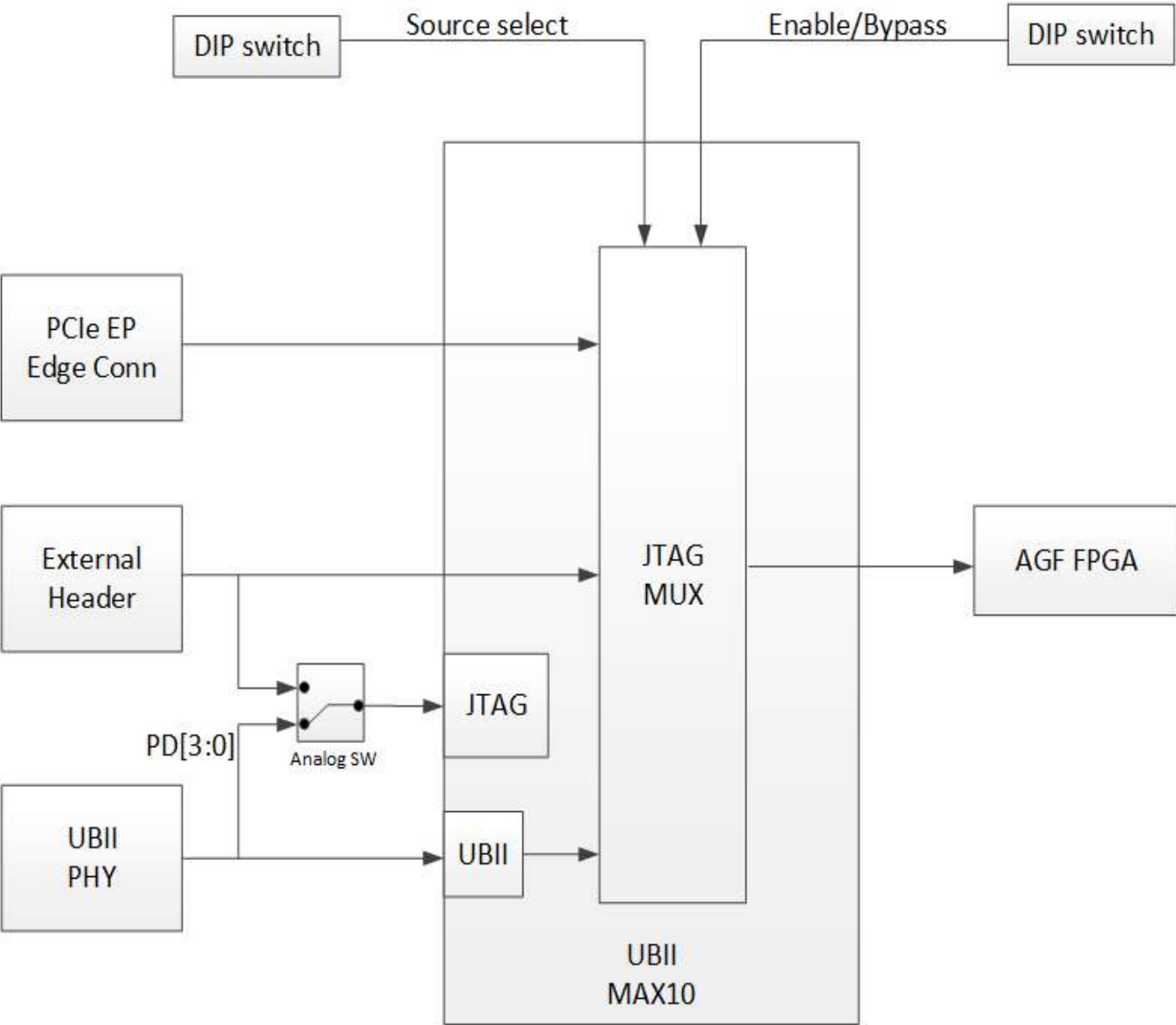
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I2C Diagram



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JTAG Block Diagram



DDR4/DDR-T DIMM Pin Map

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	12V	145	12V	38	DQ24	182	VSS	75	CLK0#	219	CLK1#	108	DQ40	252	VSS
2	VSS	146	VREFCA	39	VSS	183	DQ25	76	VDD	220	VDD	109	VSS	253	DQ41
3	DQ4	147	VSS	40	DQS12	184	VSS	77	VTT	221	VTT	110	DQS14	254	VSS
4	VSS	148	DQ5	41	DQS12#	185	DQS3#	KEY				111	DQS14#	255	DQS5#
5	DQ0	149	VSS	42	VSS	186	DQS3					112	VSS	256	DQS5
6	VSS	150	DQ1	43	DQ30	187	VSS					113	DQ46	257	VSS
7	DQS0	151	VSS	44	VSS	188	DQ31					114	VSS	258	DQ47
8	DQS0#	152	DQS0#	45	DQ26	189	VSS	78	EVENT	222	PARITY	115	DQ42	259	VSS
9	VSS	153	DQS0	46	VSS	190	DQ27	79	A0	223	VDD	116	VSS	260	DQ43
10	DQ6	154	VSS	47	CB4	191	VSS	80	VDD	224	BA1	117	DQ52	261	VSS
11	VSS	155	DQ7	48	VSS	192	CB5	81	BA0	225	A10	118	VSS	262	DQ53
12	DQ2	156	VSS	49	CB0	193	VSS	82	RAS#/A16	226	VDD	119	DQ48	263	VSS
13	VSS	157	DQ3	50	VSS	194	CB1	83	VDD	227	RFU	120	VSS	264	DQ49
14	DQ12	158	VSS	51	DQS17	195	VSS	84	CS0#	228	WE#/A14	121	DQS15	265	VSS
15	VSS	159	DQ13	52	DQS17#	196	DQS8#	85	VDD	229	VDD	122	DQS15#	266	DQS6#
16	DQ8	160	VSS	53	VSS	197	DQS8	86	CAS#/A15	230	SAVE#	123	VSS	267	DQS6
17	VSS	161	DQ9	54	CB6	198	VSS	87	ODT0	231	VDD	124	DQ54	268	VSS
18	DQS10	162	VSS	55	VSS	199	CB7	88	VDD	232	A13	125	VSS	269	DQ55
19	DQS10#	163	DQS1#	56	CB2	200	VSS	89	CS1#	233	VDD	126	DQ50	270	VSS
20	VSS	164	DQS1	57	VSS	201	CB3	90	VDD	234	A17	127	VSS	271	DQ51
21	DQ14	165	VSS	58	RESET#	202	VSS	91	ODT1	235	C2	128	DQ60	272	VSS
22	VSS	166	DQ15	59	VDD	203	CKE1	92	VDD	236	VDD	129	VSS	273	DQ61
23	DQ10	167	VSS	60	CKE0	204	VDD	93	C0	237	C1	130	DQ56	274	VSS
24	VSS	168	DQ11	61	VDD	205	RFU	94	VSS	238	SA2	131	VSS	275	DQ57
25	DQ20	169	VSS	62	ACT#	206	VDD	95	DQ36	239	VSS	132	DQS16	276	VSS
26	VSS	170	DQ21	63	BG0	207	BG1	96	VSS	240	DQ37	133	DQS16#	277	DQS7#
27	DQ16	171	VSS	64	VDD	208	ALERT#	97	DQ32	241	VSS	134	VSS	278	DQS7
28	VSS	172	DQ17	65	A12	209	VDD	98	VSS	242	DQ33	135	DQ62	279	VSS
29	DQS11	173	VSS	66	A9	210	A11	99	DQS13	243	VSS	136	VSS	280	DQ63
30	DQS11#	174	DQS2#	67	VDD	211	A7	100	DQS13#	244	DQS4#	137	DQ58	281	VSS
31	VSS	175	DQS2	68	A8	212	VDD	101	VSS	245	DQS4	138	VSS	282	DQ59
32	DQ22	176	VSS	69	A6	213	A5	102	DQ38	246	VSS	139	SA0	283	VSS
33	VSS	177	DQ23	70	VDD	214	A4	103	VSS	247	DQ39	140	SA1	284	VDDSPD
34	DQ18	178	VSS	71	A3	215	VDD	104	DQ34	248	VSS	141	SCL	285	SDA
35	VSS	179	DQ19	72	A1	216	A2	105	VSS	249	DQ35	142	VPP	286	VPP
36	DQ28	180	VSS	73	VDD	217	VDD	106	DQ44	250	VSS	143	VPP	287	VPP
37	VSS	181	DQ29	74	CLK0	218	CLK1	107	VSS	251	DQ45	144	RFU	288	VPP

DDR-T DIMM Pin Map is Identical to standard DDR4 DIMM Pin Map except the DDR-T protocol repurposes five of these pins:

CS1# (pin 89) : Grant, GNT# <0> Input

CKE1 (pin 203) : Request, REQ# <0> Output

ODT1 (pin 91) : Error, ERR# Output

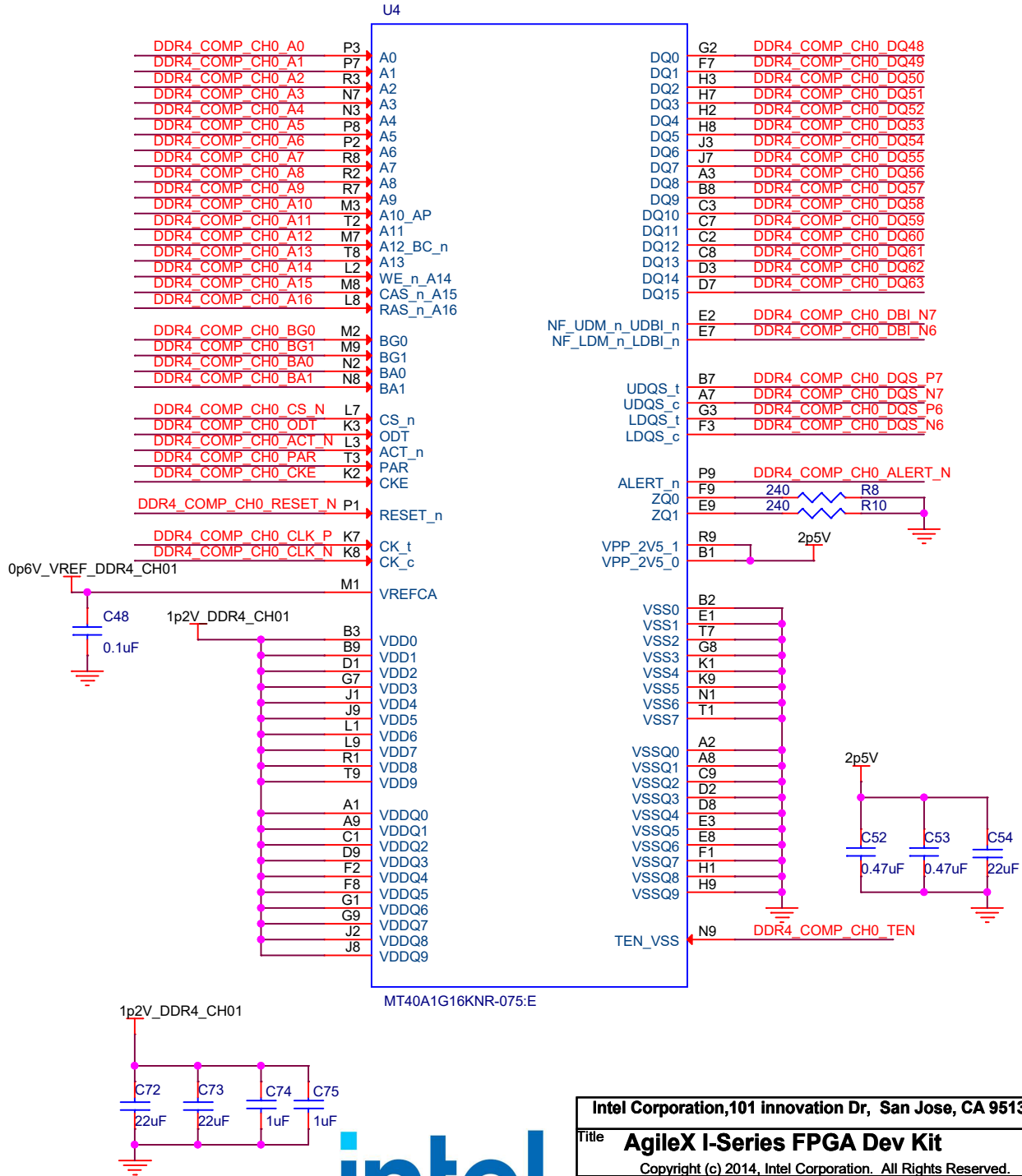
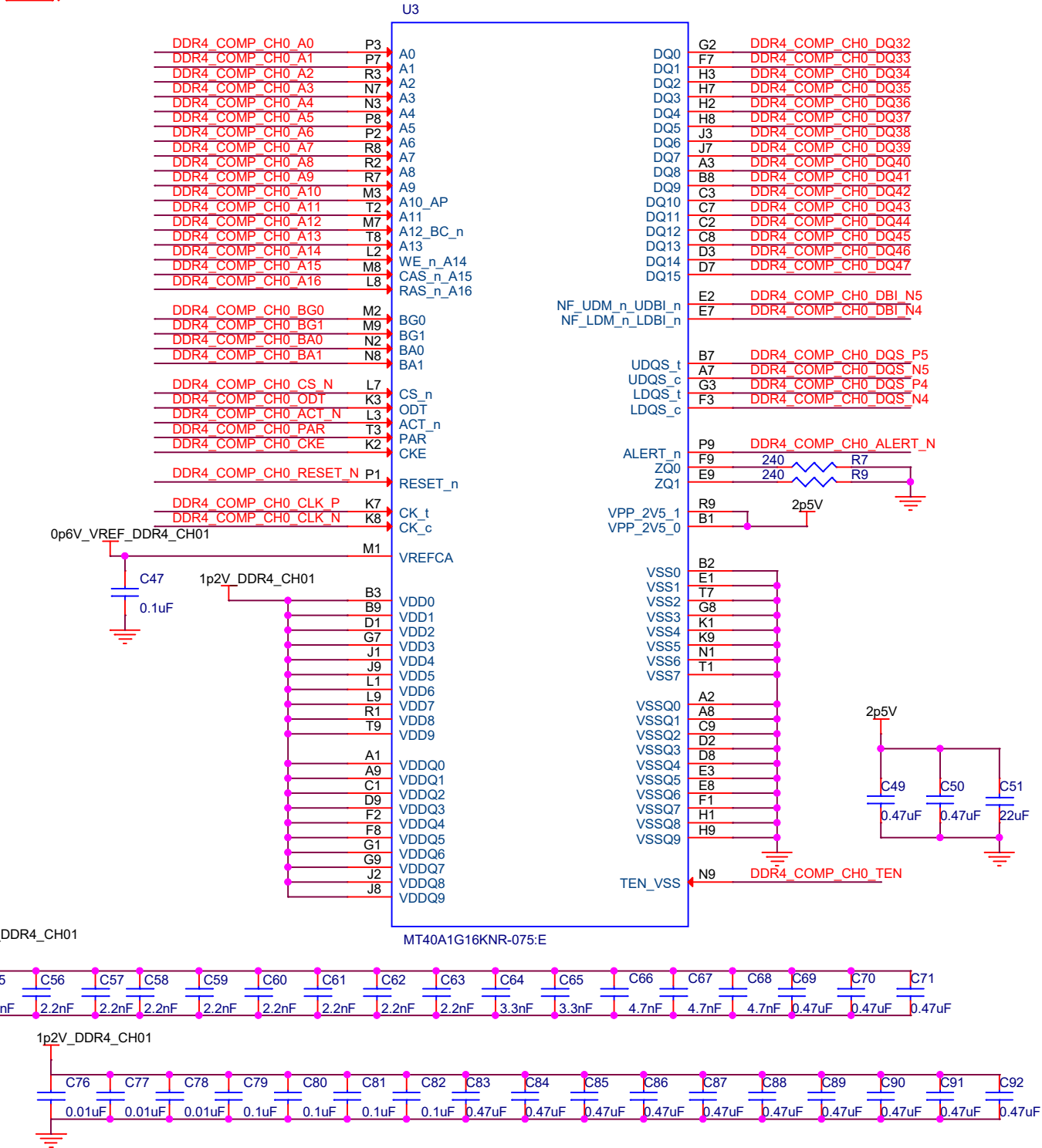
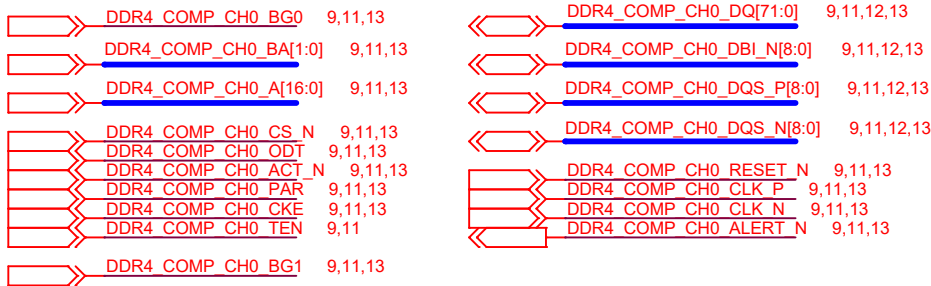
CLK1 (pin 218):Early Read ID, ERID<0> Output

CLK1# (pin 219):Early Read ID, ERID<1> Output



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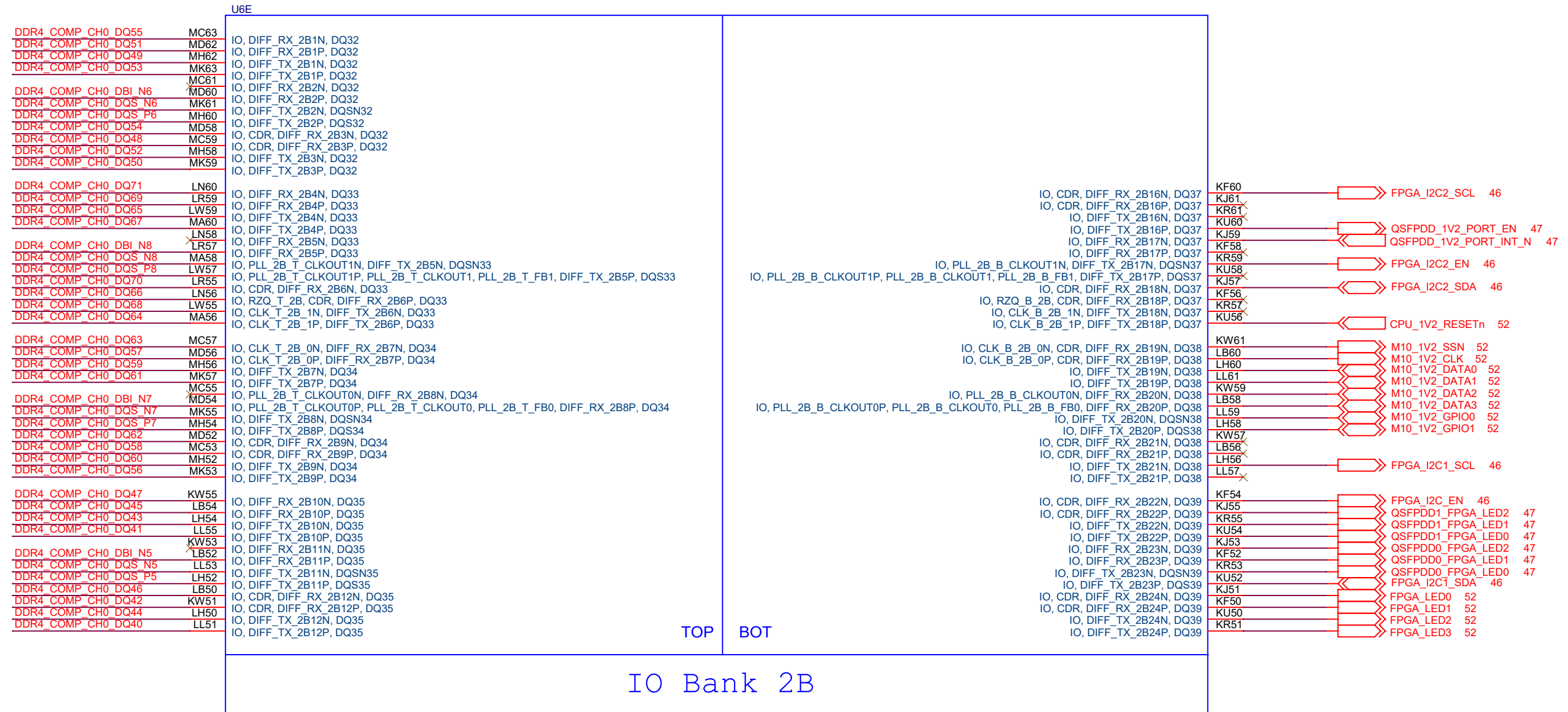
DDR4 COMPONENT #3/#4



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DDR4/T CH0 INTERFACE -- FPGA SIDE 3A



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9,10,11,13 DDR4_COMP_CH0_DBI_N[8:0] 

9,10,11,13 DDR4_COMP_CH0_DQ[71:0] 

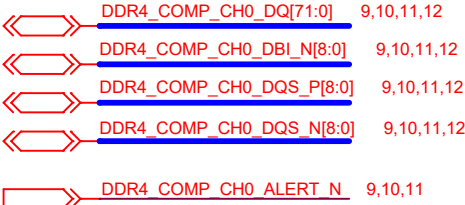
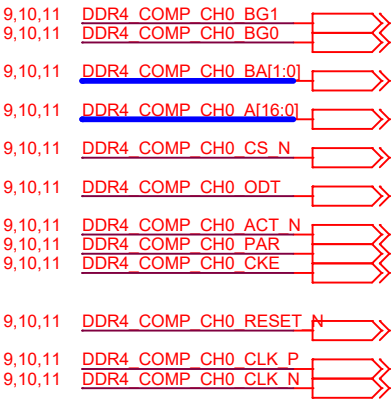
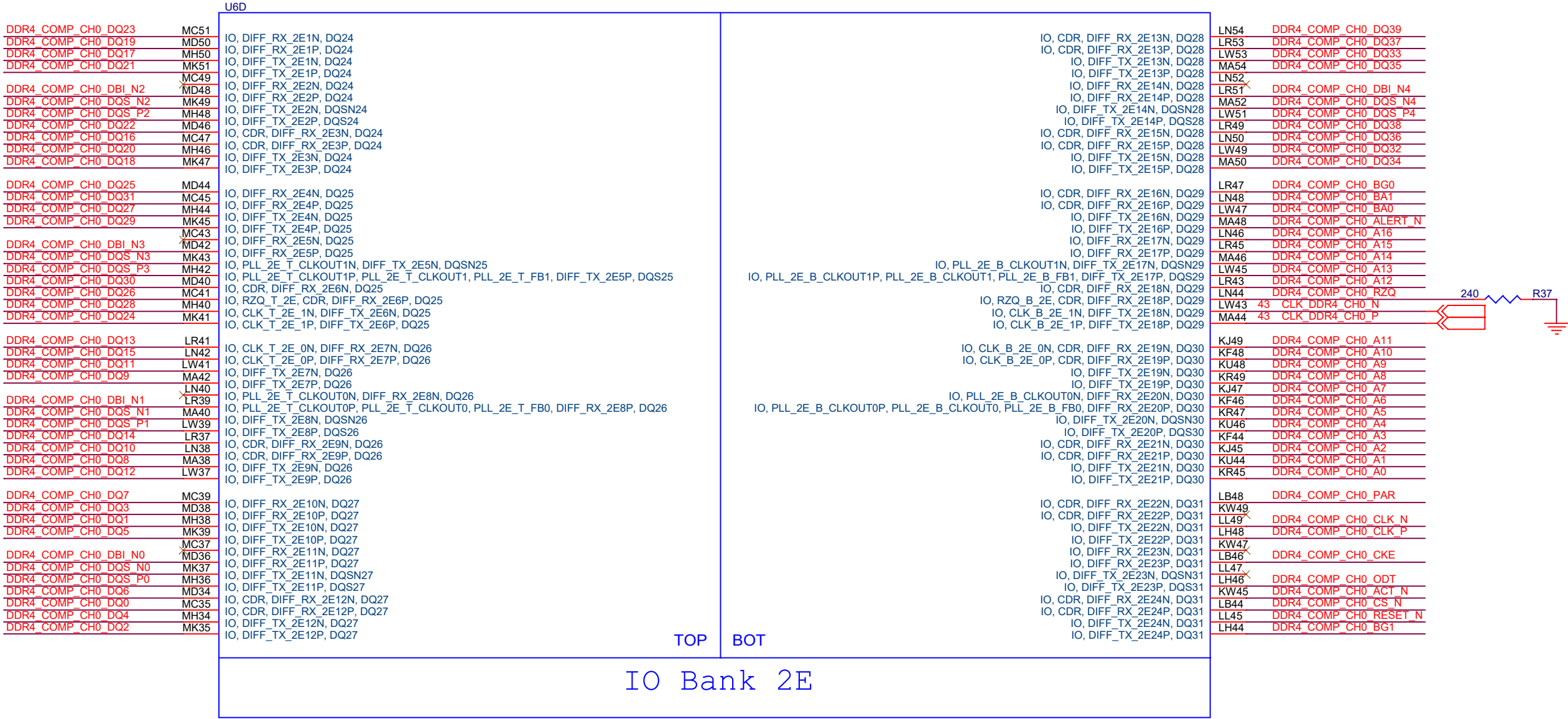
9,10,11,13 DDR4_COMP_CH0_DQS_P[8:0] 

9,10,11,13 DDR4_COMP_CH0_DQS_N[8:0] 



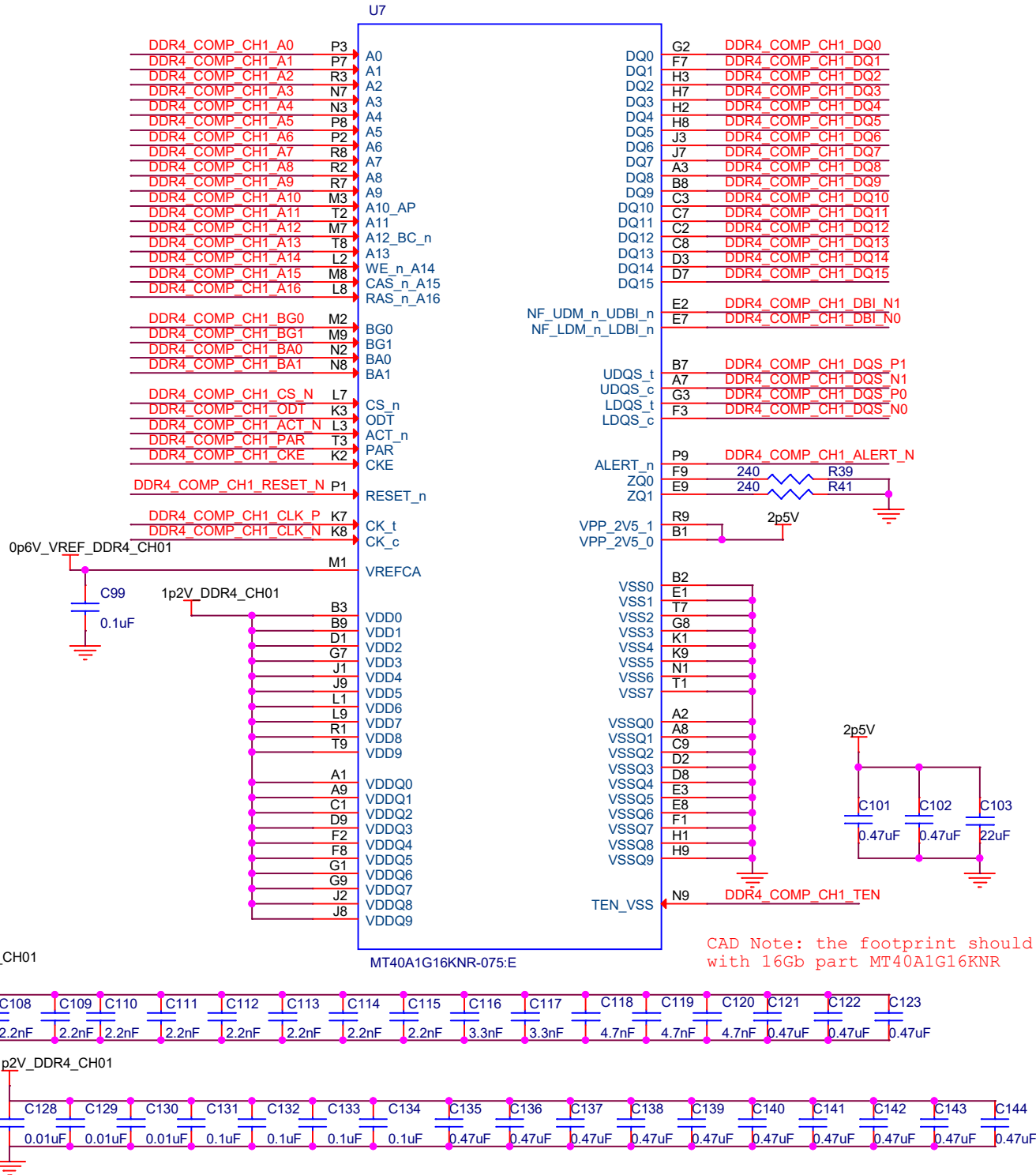
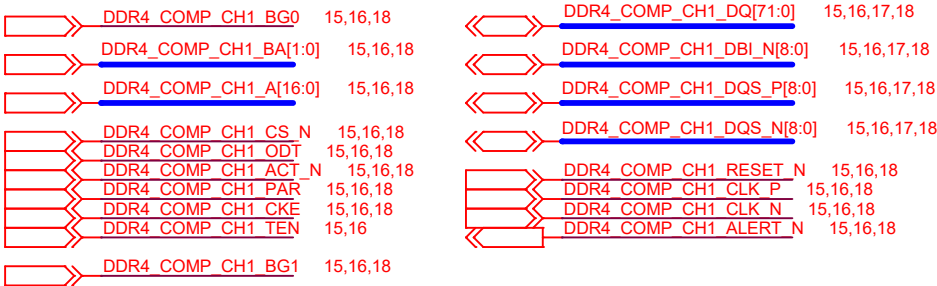
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DDR4/T CH1 INTERFACE -- FPGA SIDE 3B

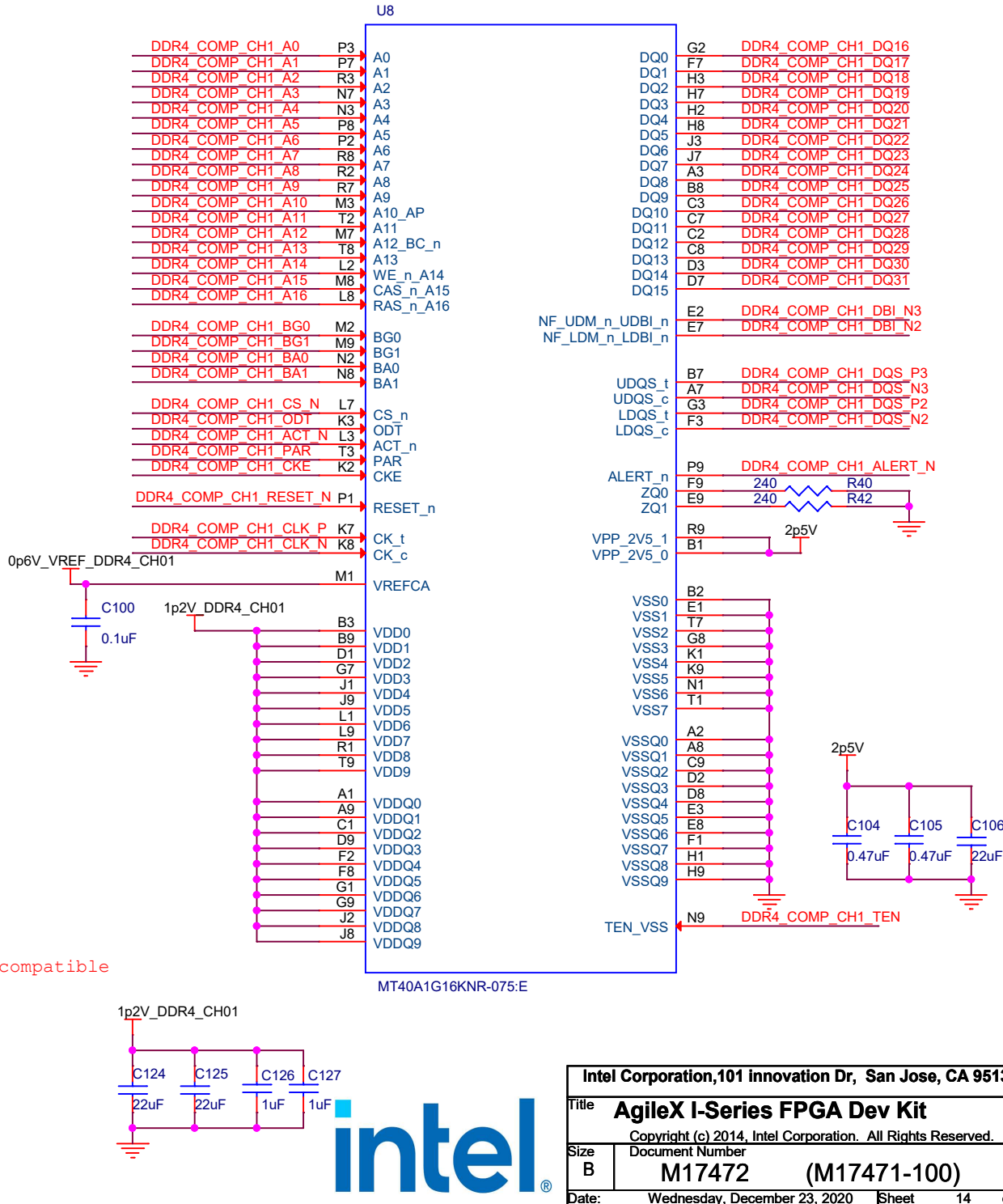


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DDR4 COMPONENT #1/#2

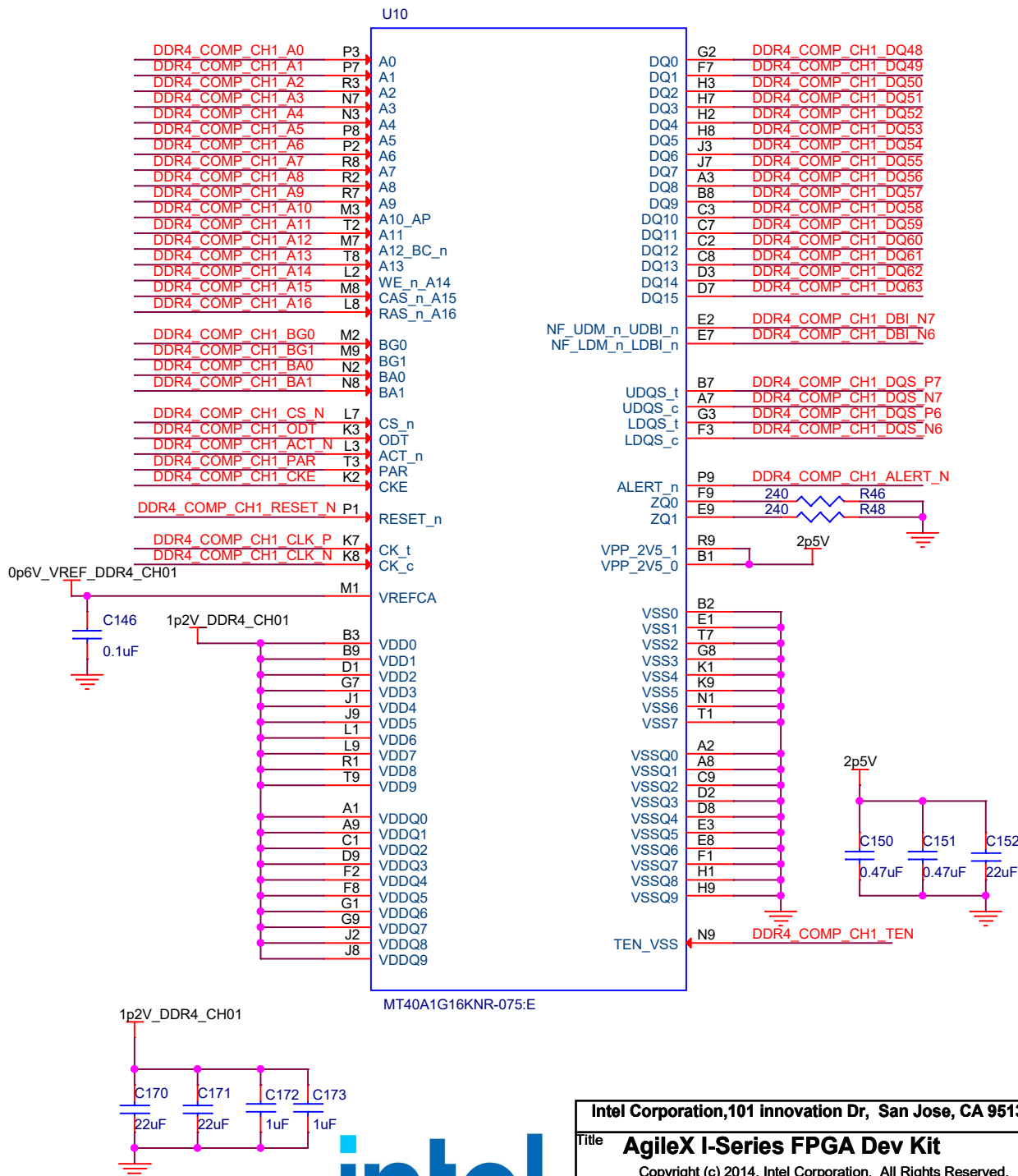
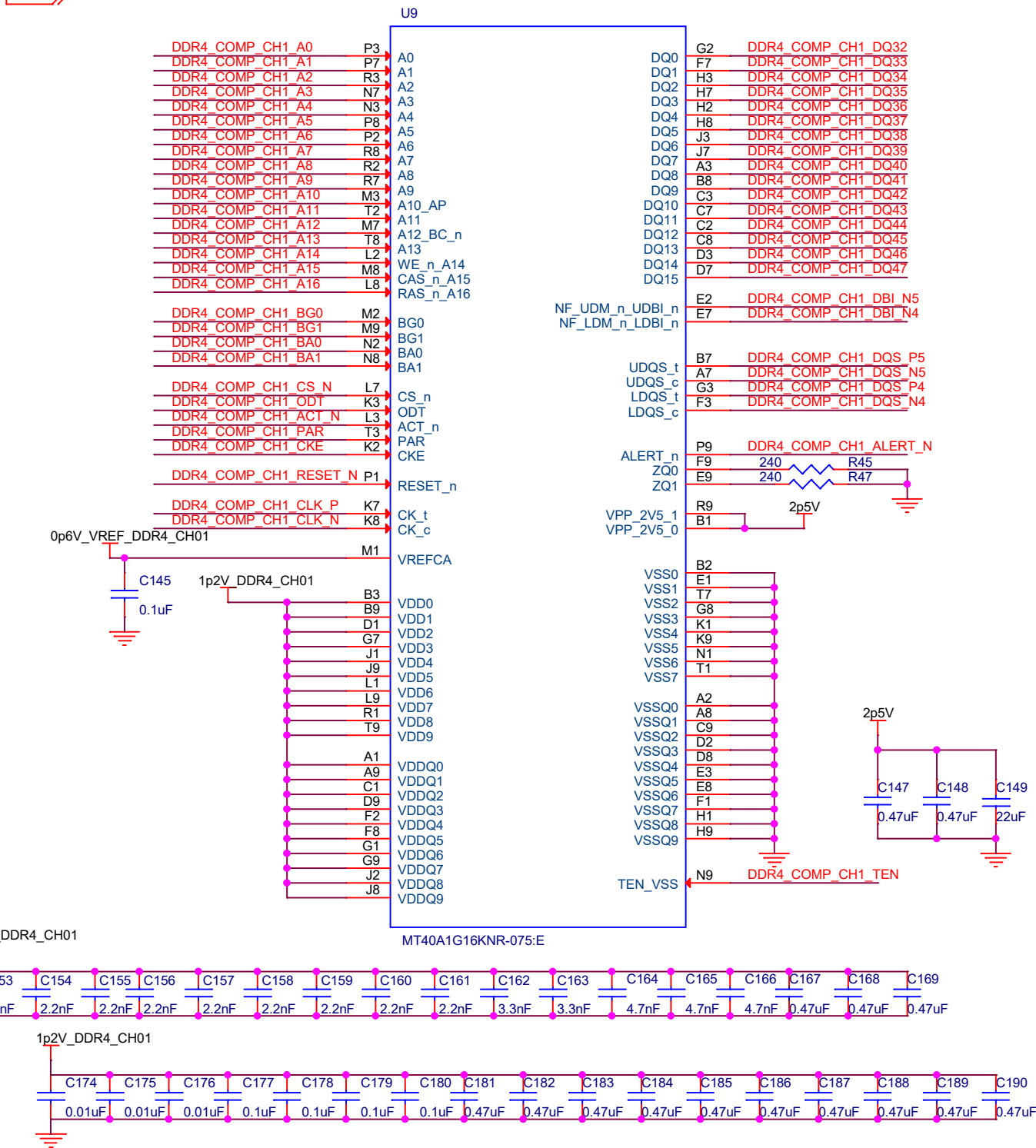
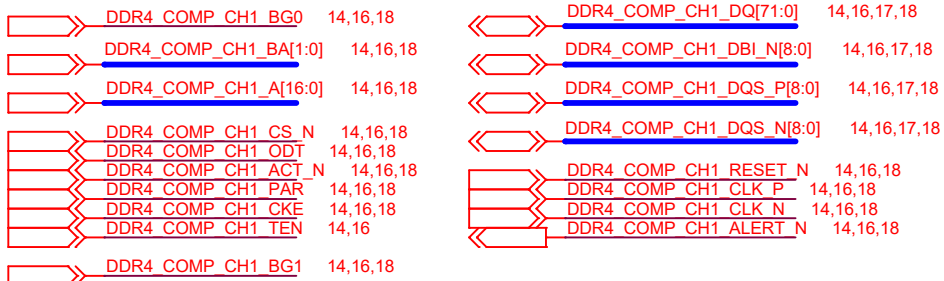


CAD Note: the footprint should be compatible with 16Gb part MT40A1G16KNR



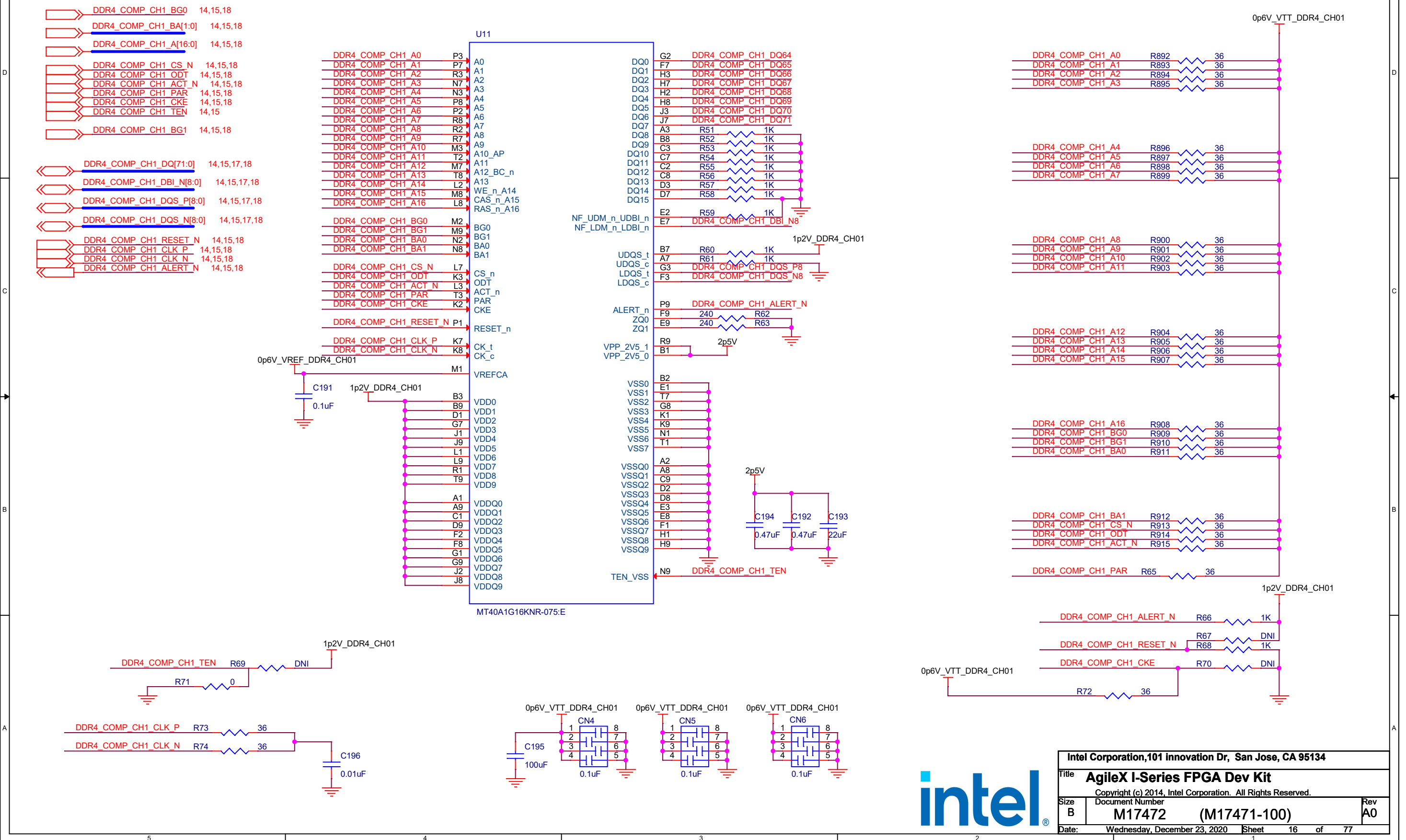
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DDR4 COMPONENT #3/#4

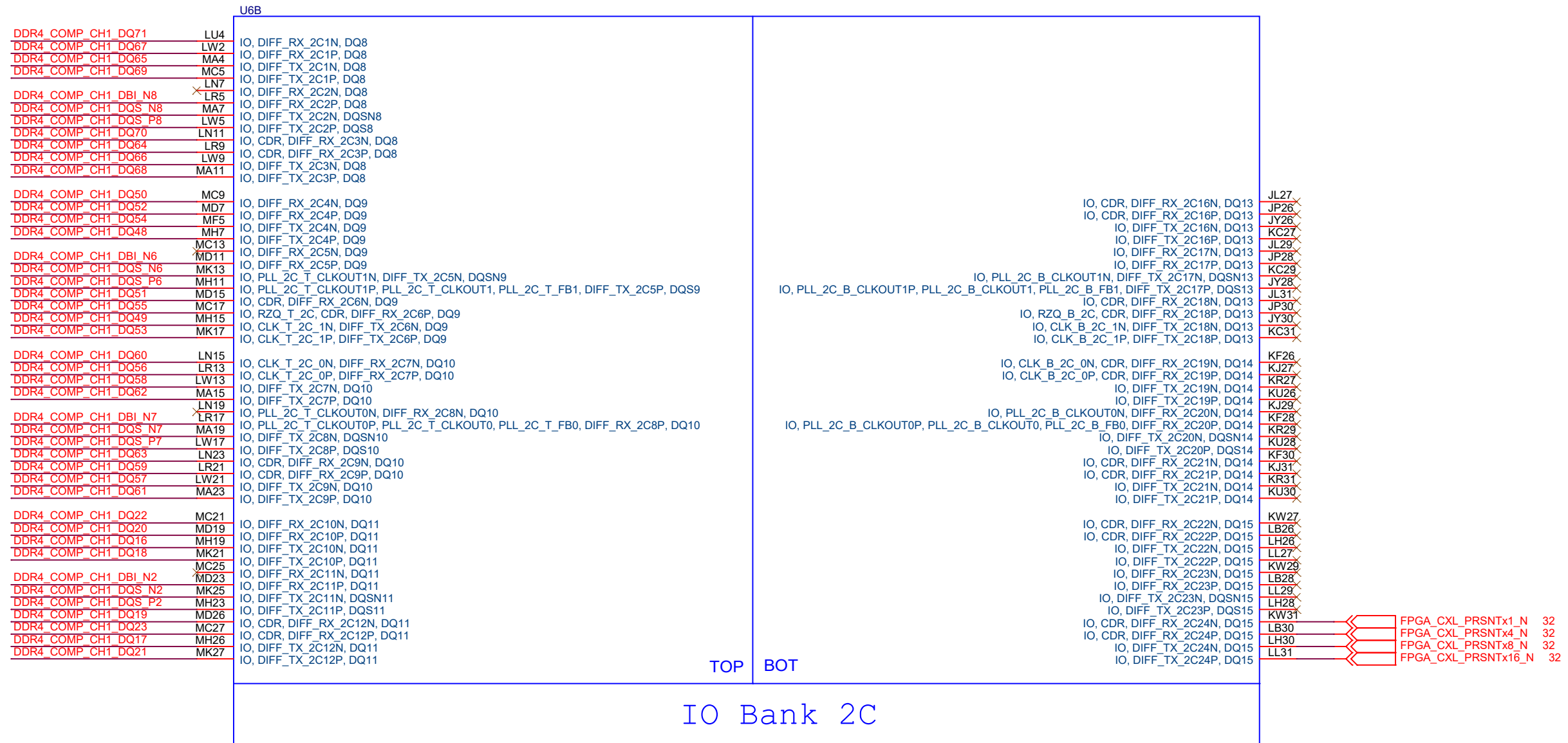


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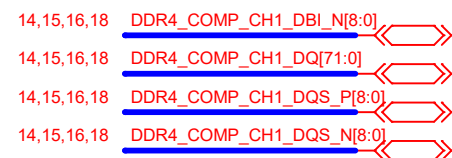
DDR4 COMPONENT #5 & Termination



DDR4/T CH2 INTERFACE -- FPGA SIDE 2A

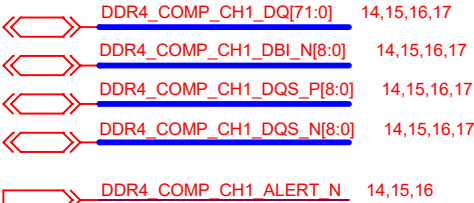
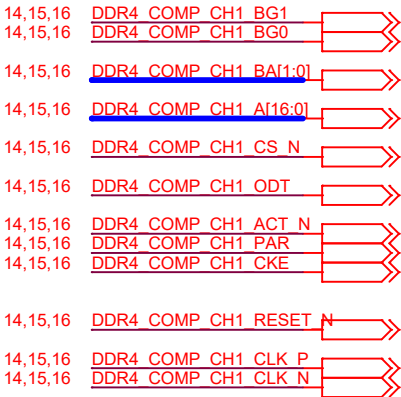
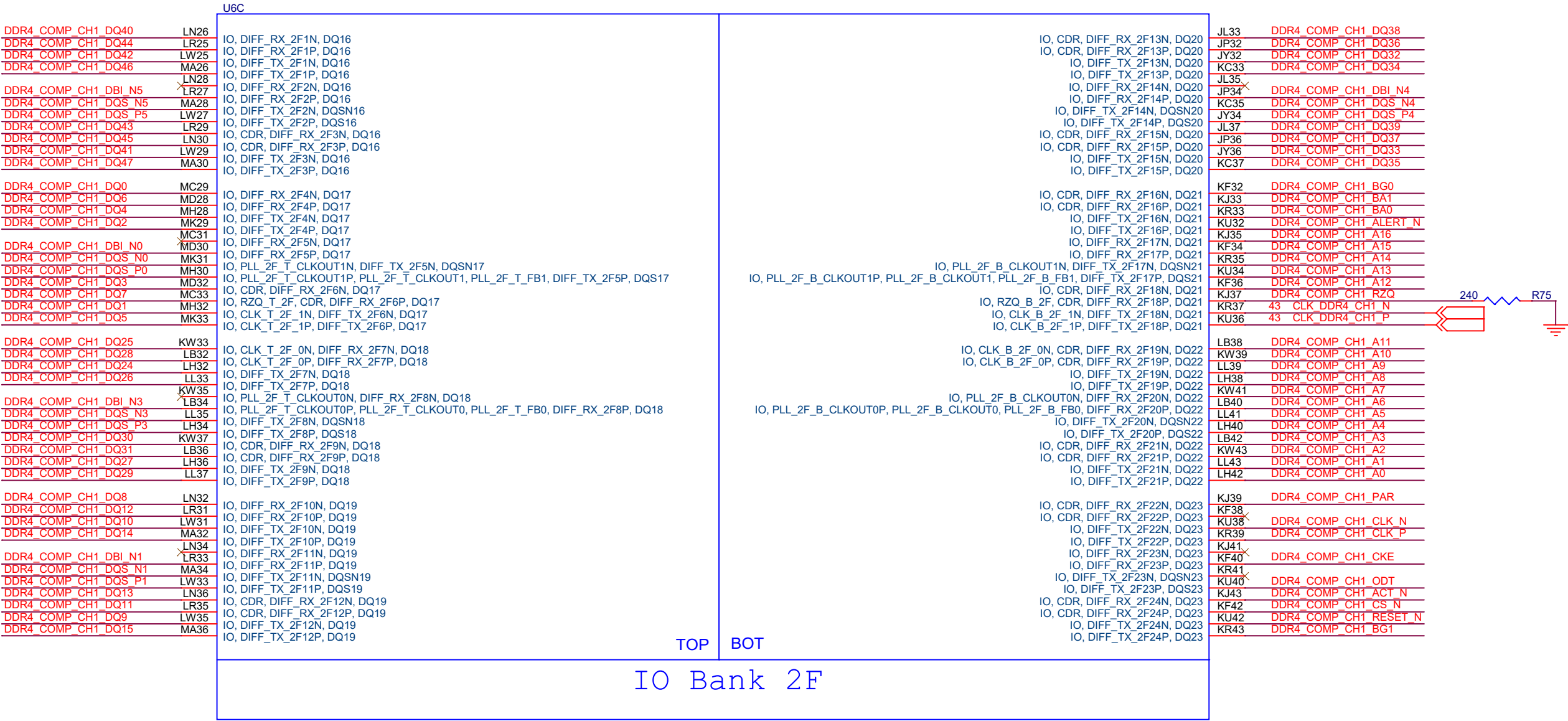


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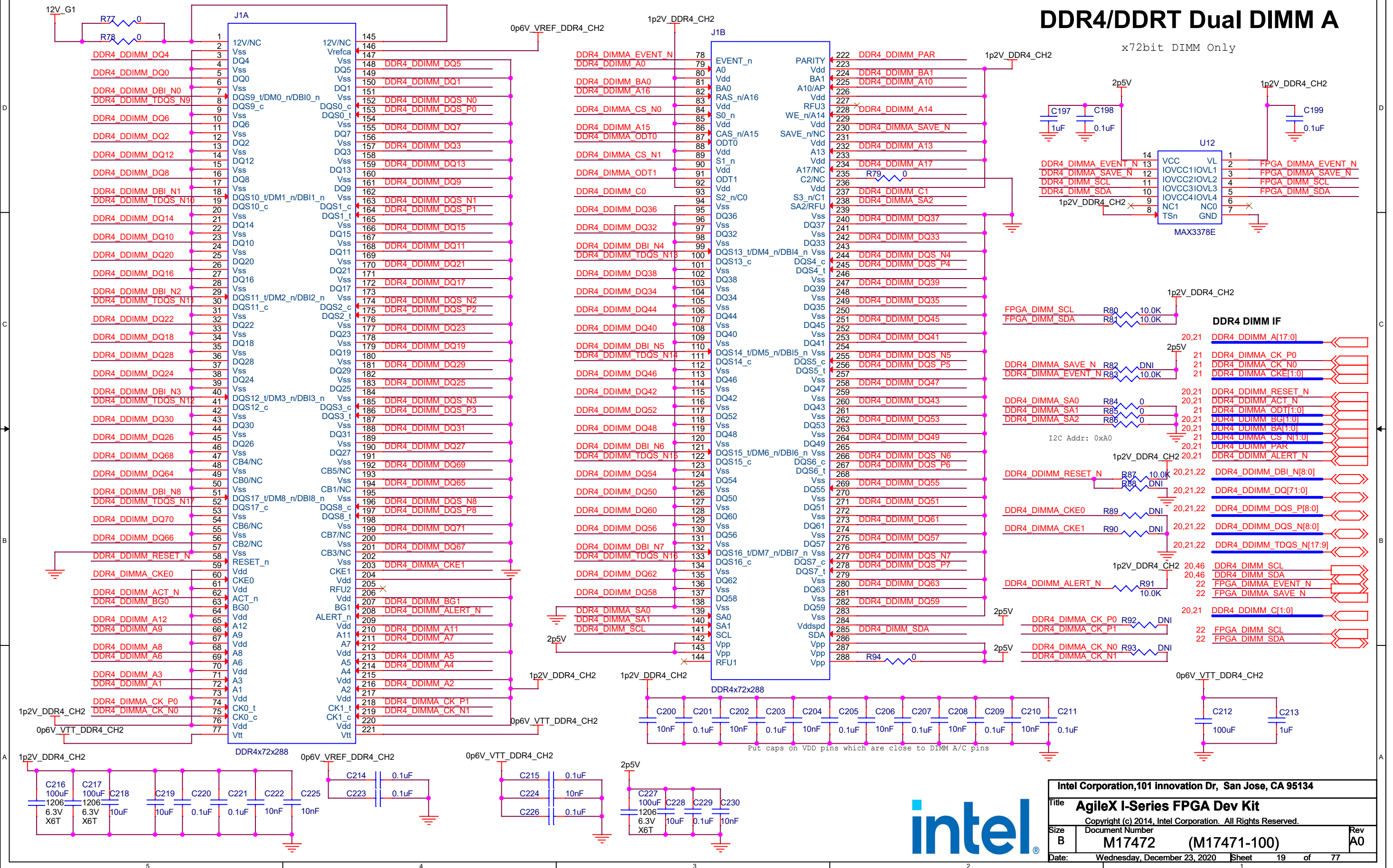
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DDR4 DIMM CH1 Interface - FPGA Side 3C



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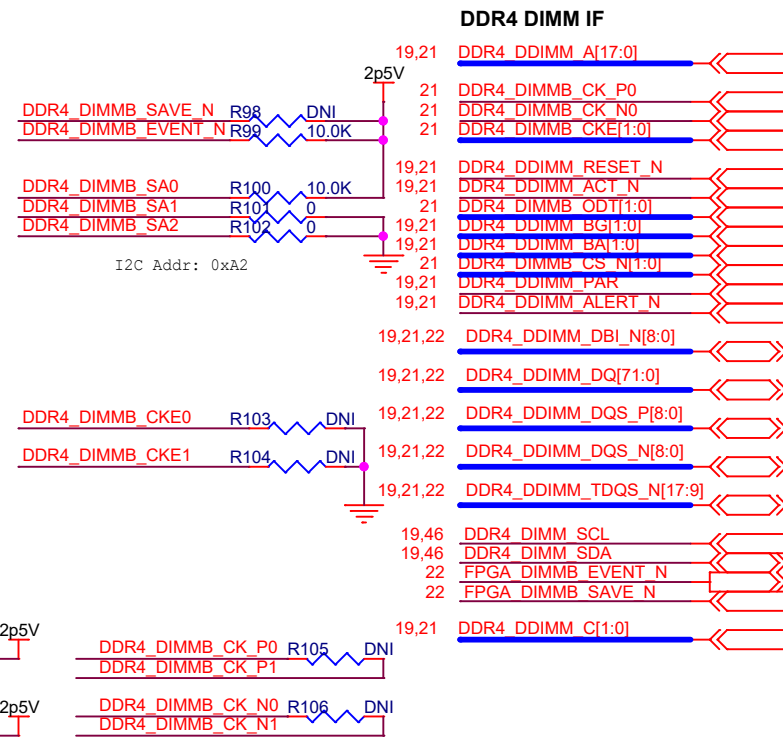
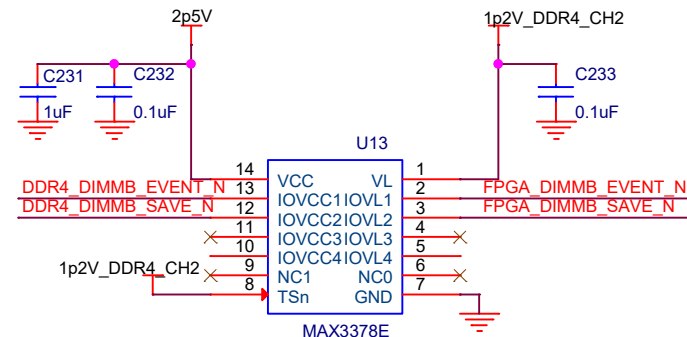
DDR4/DDRT Dual DIMM A



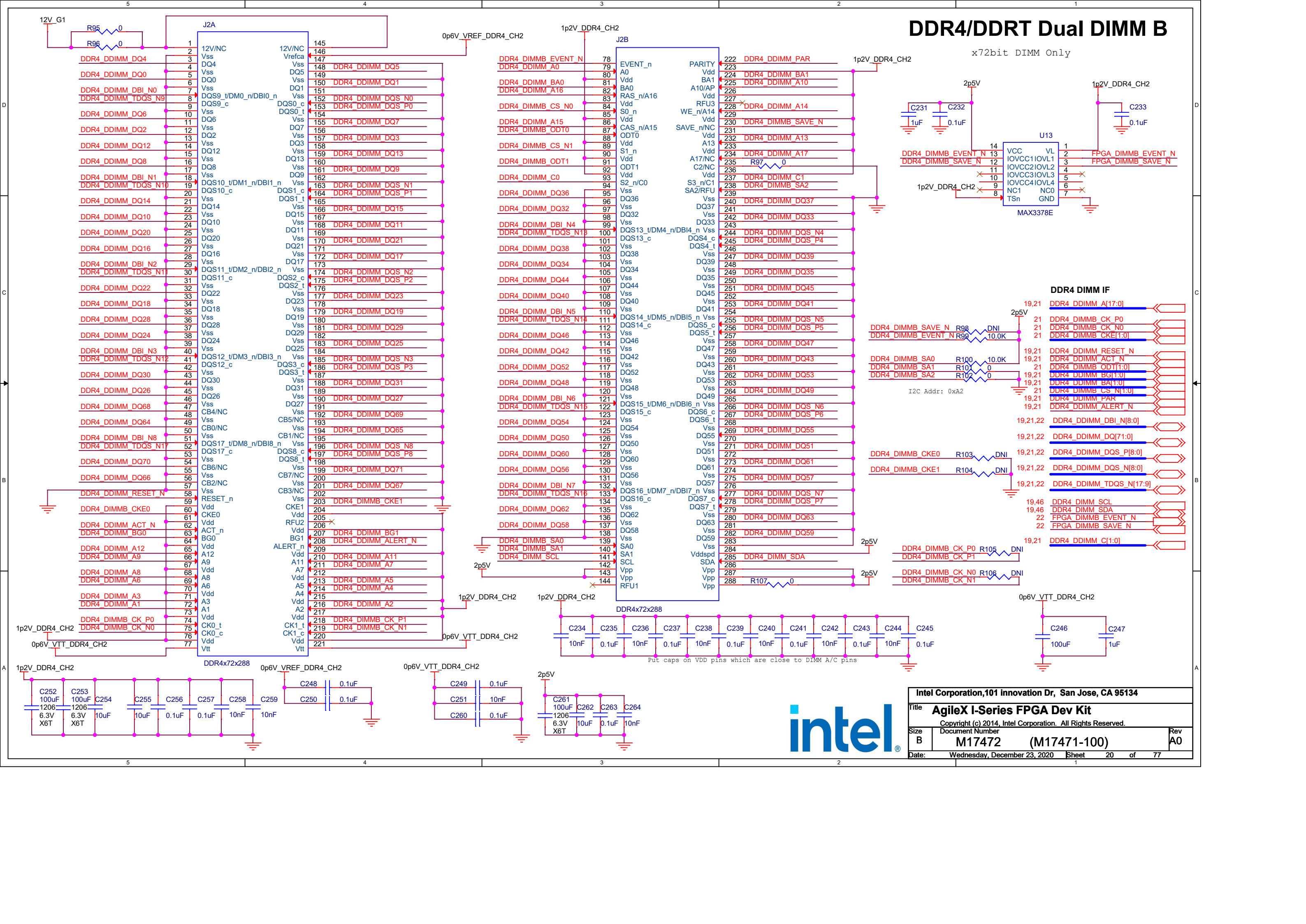
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DDR4/DDRT Dual DIMM B

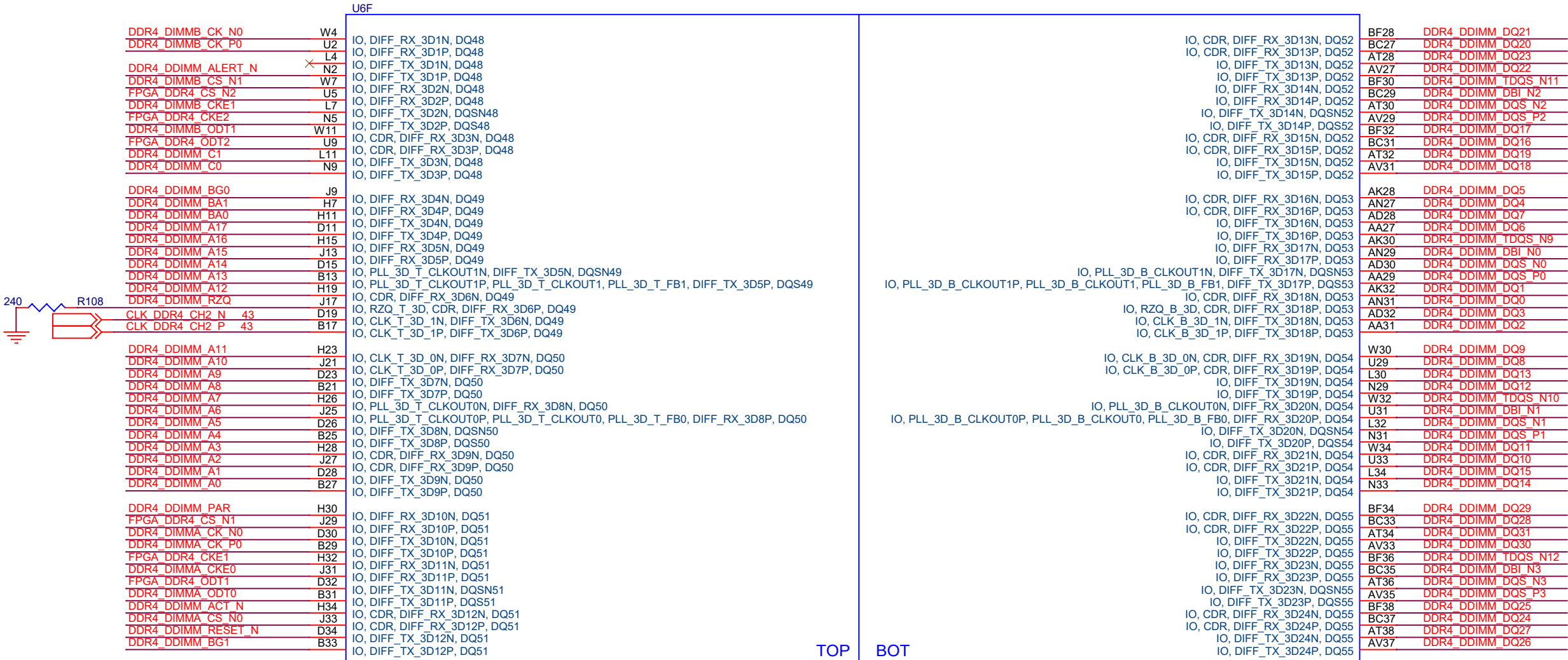
x72bit DIMM Only



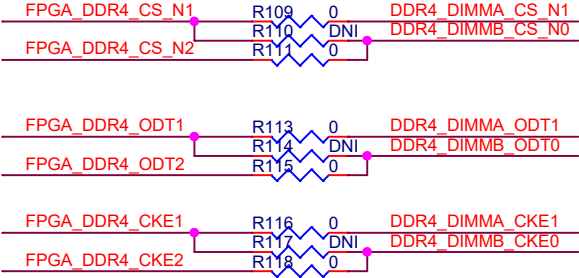
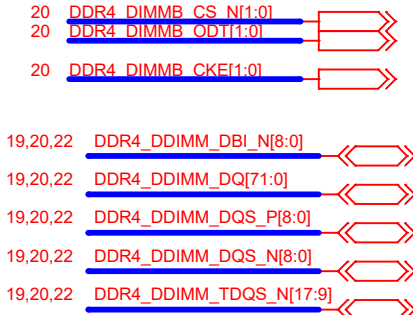
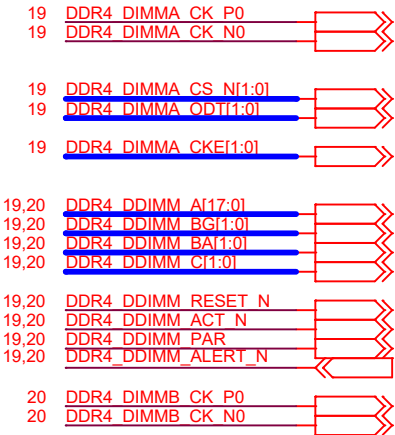
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DDR4/T CH3 INTERFACE -- FPGA SIDE 2C



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Layout notes: Place these resistors near to DIMM

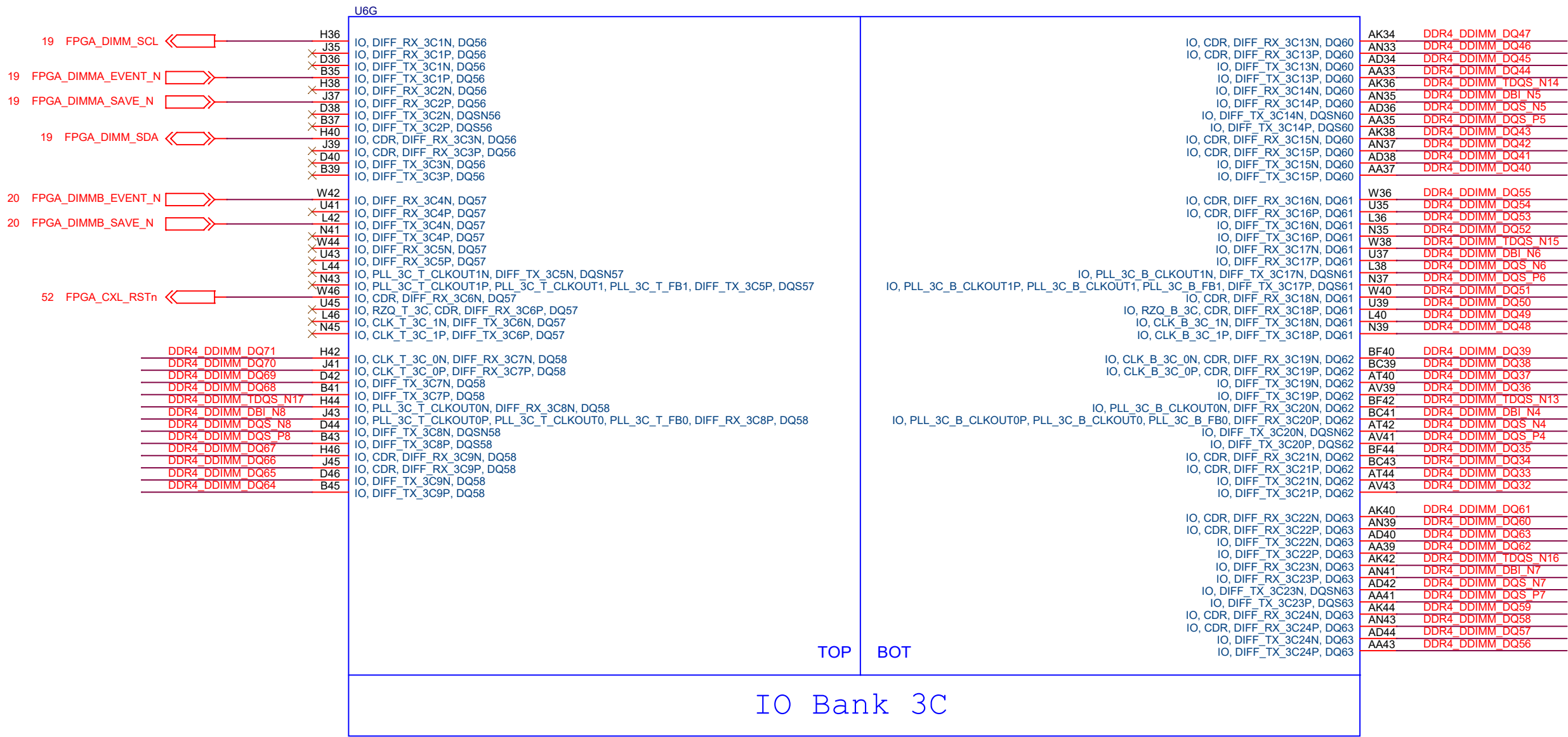


Type	Option
Single DIMM (Single&Dual Rank)	J1, R109, R111, R113, R115, R116, R118
DDR4 w/ 3DS Dual DIMMs (Single&Dual Rank)	J1,J2, R109, R111, R113, R115, R116, R118
DDR-T Dual DIMM	J1,J2, R109, R111, R113, R115, R116, R118
Non-3DS DDR4 Dual DIMM Single Rank only	J1,J2, R110, R114, R117



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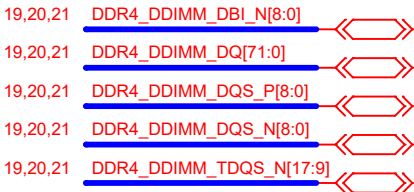
DDR4 CH1 Interface - FPGA Side 3D



TOP BOT

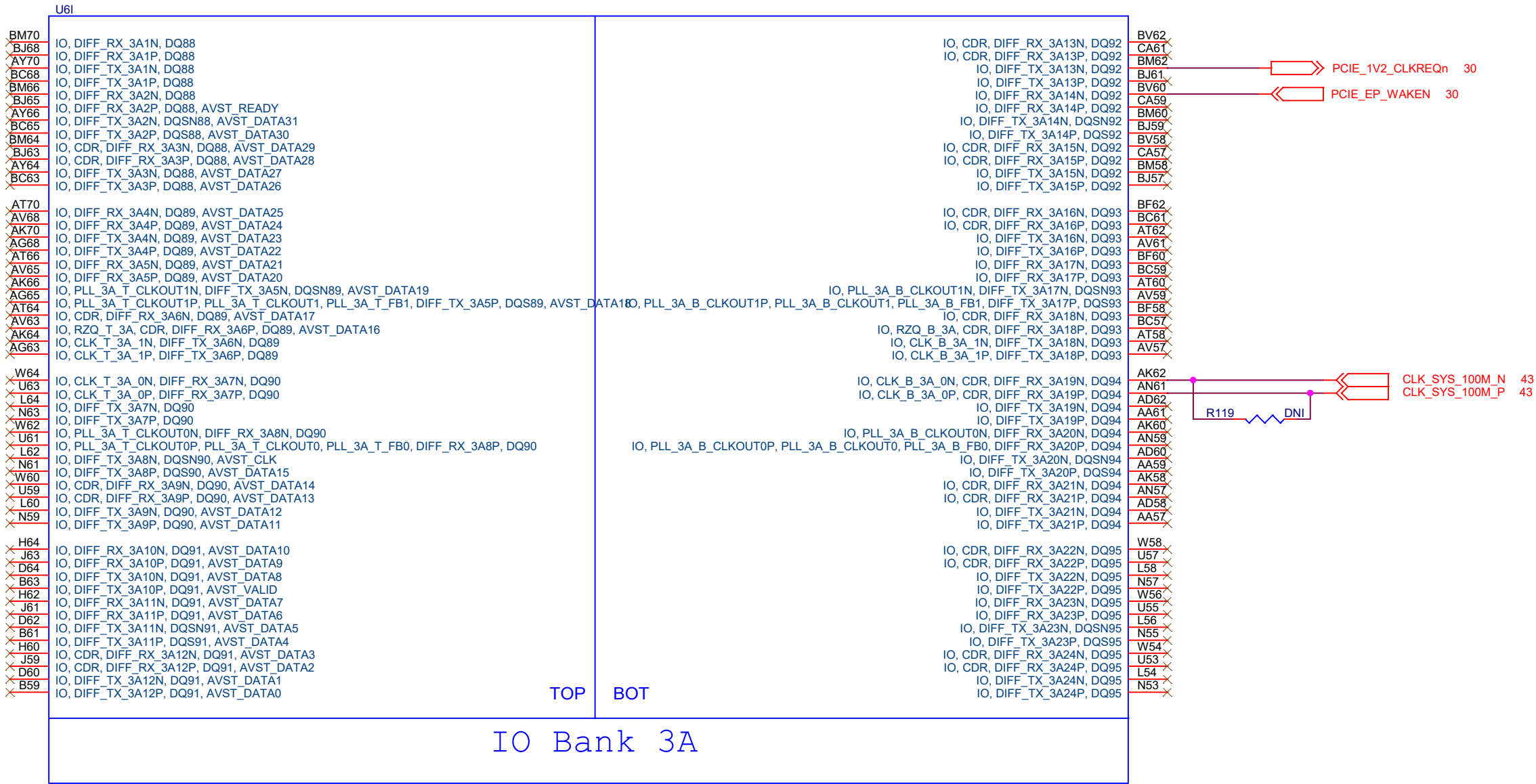
IO Bank 3C

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FPGA BANK 3A

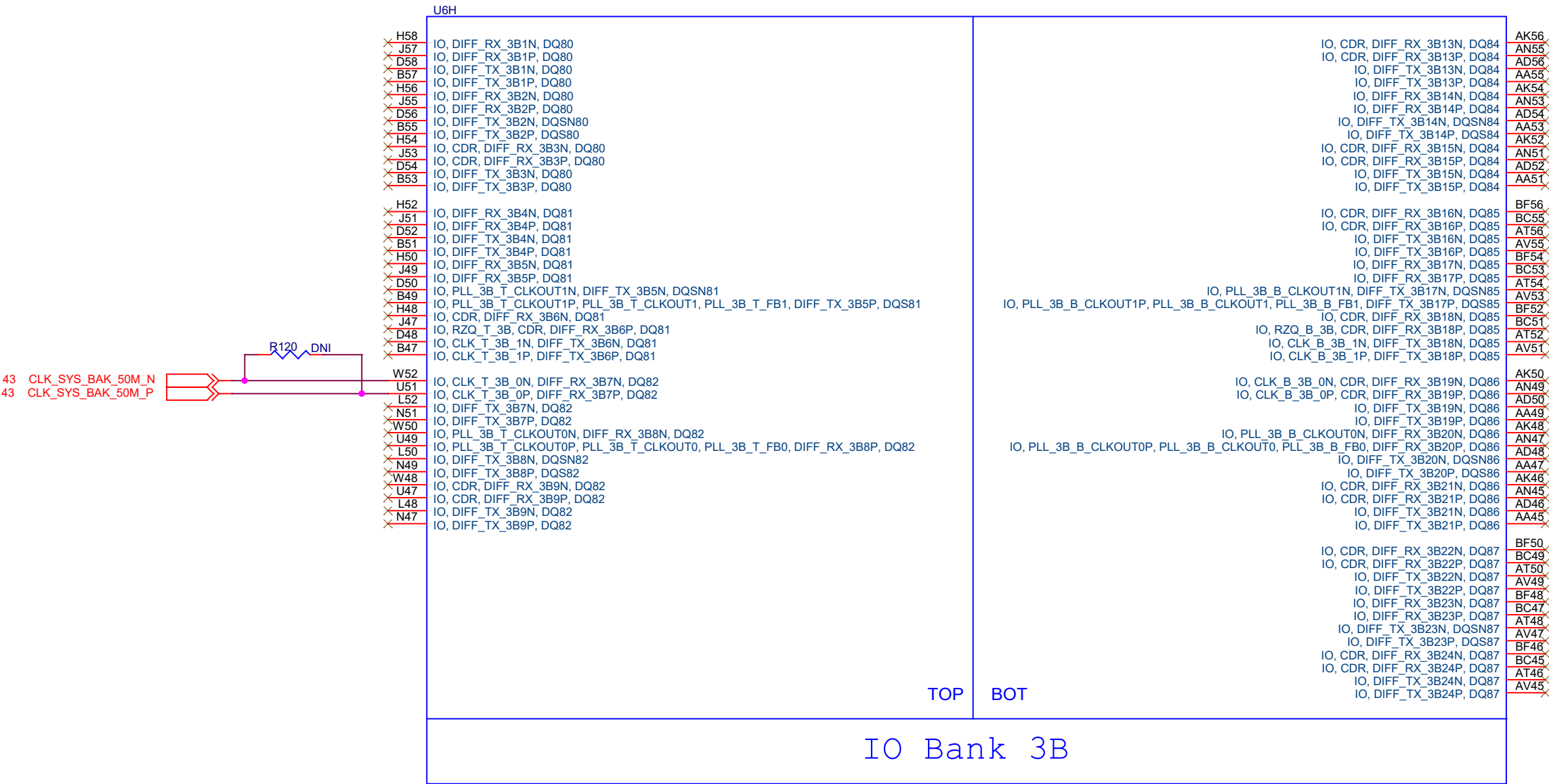


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FPGA BANK 3B



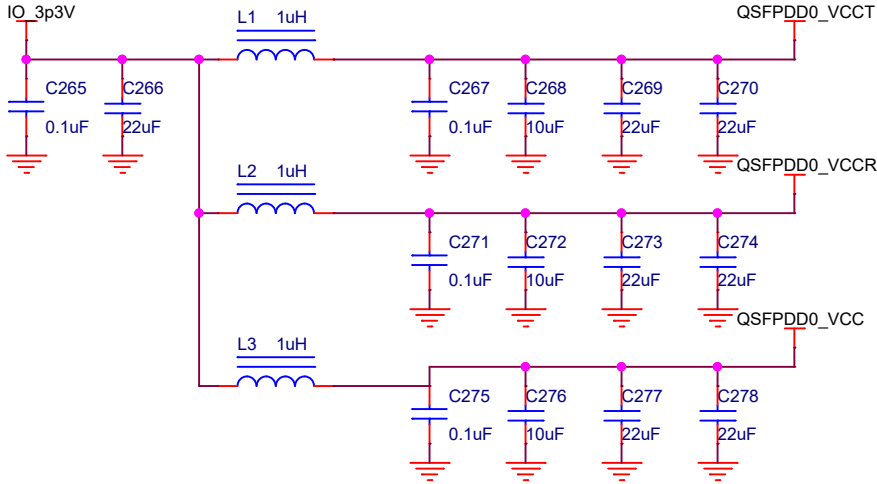
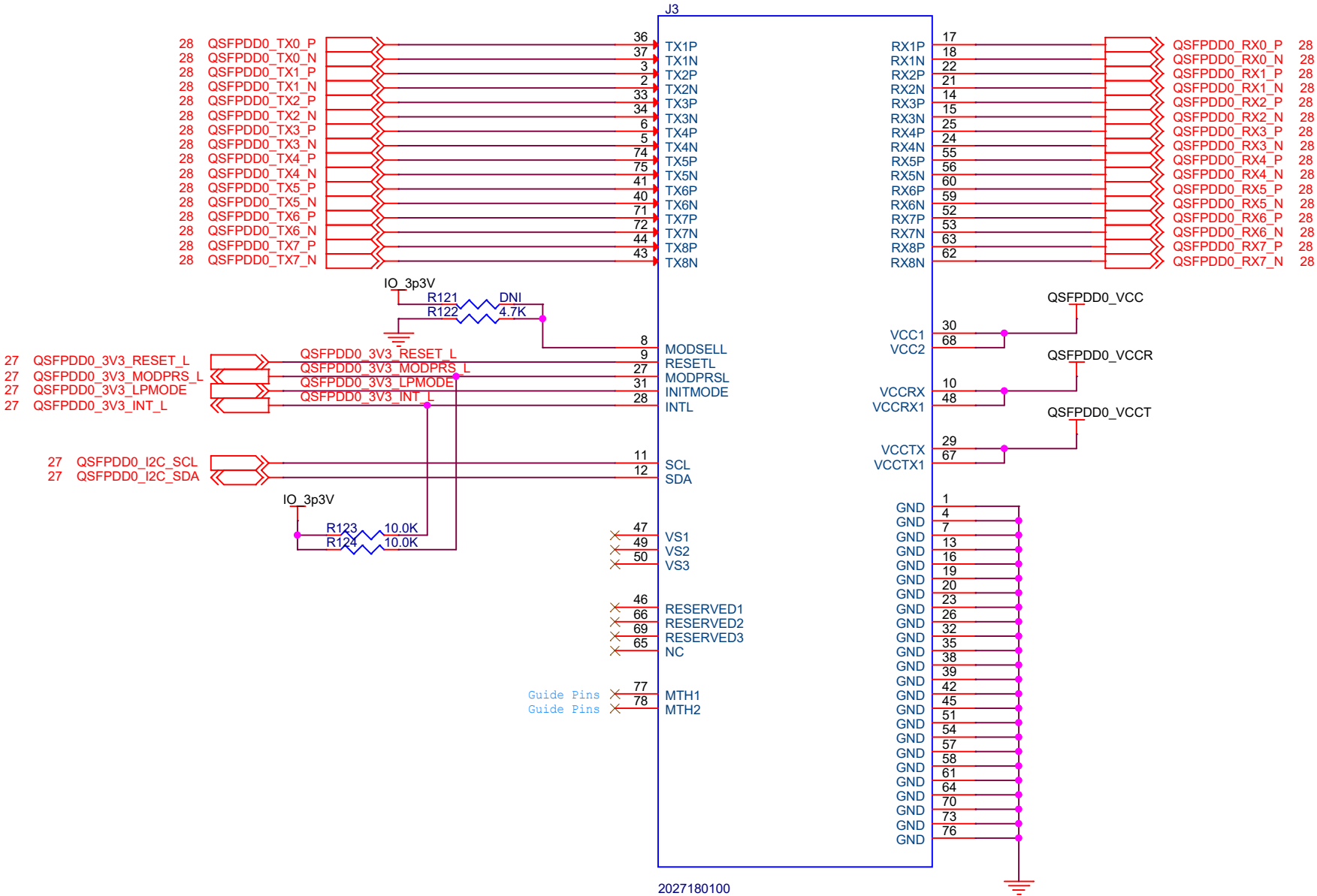
AgileX-I_2957A



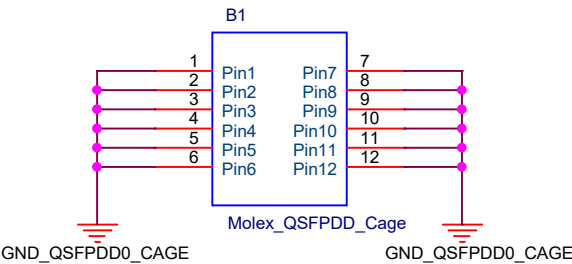
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QSFPDD0

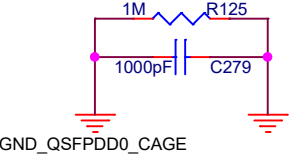
- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



Place close to QSFPDD Connector



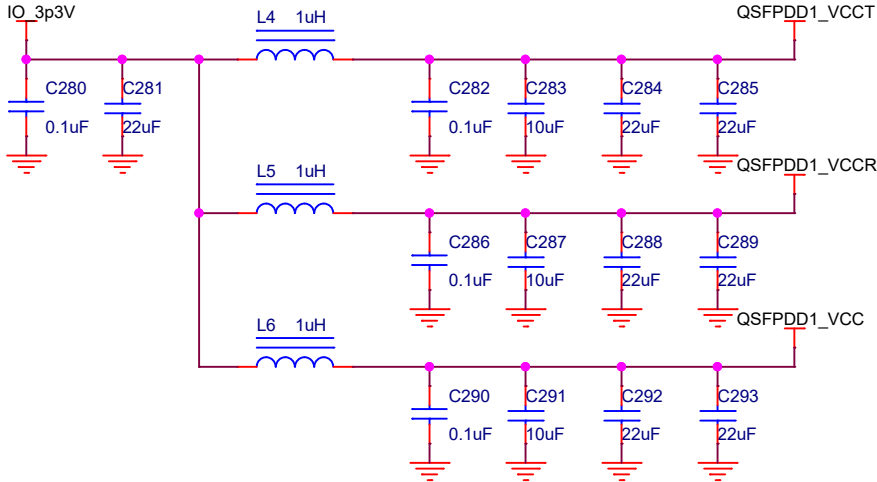
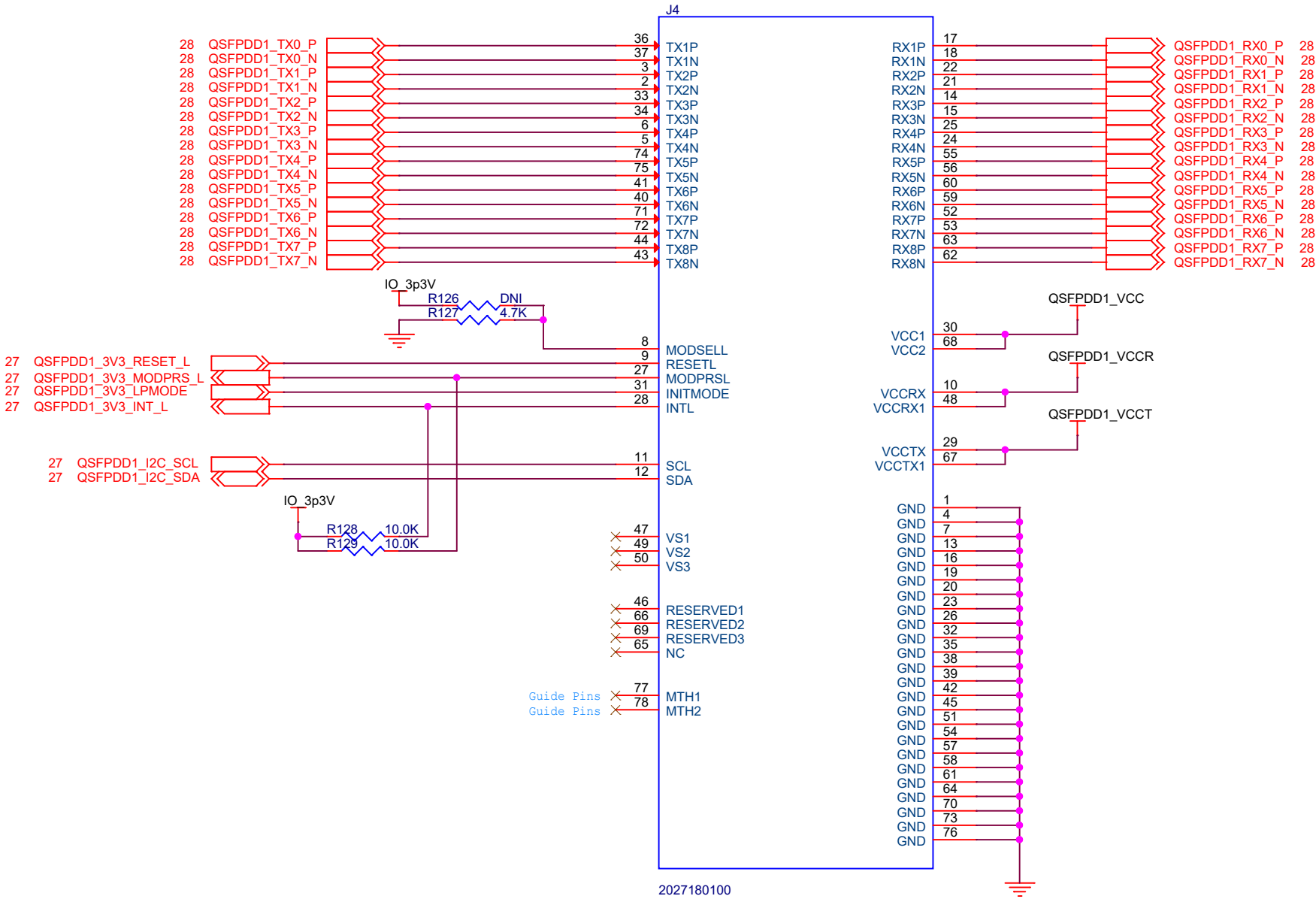
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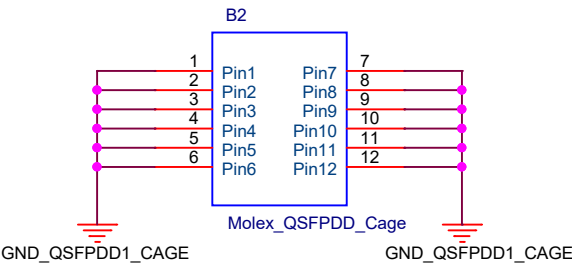
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QSFPDD1

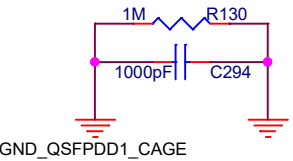
- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



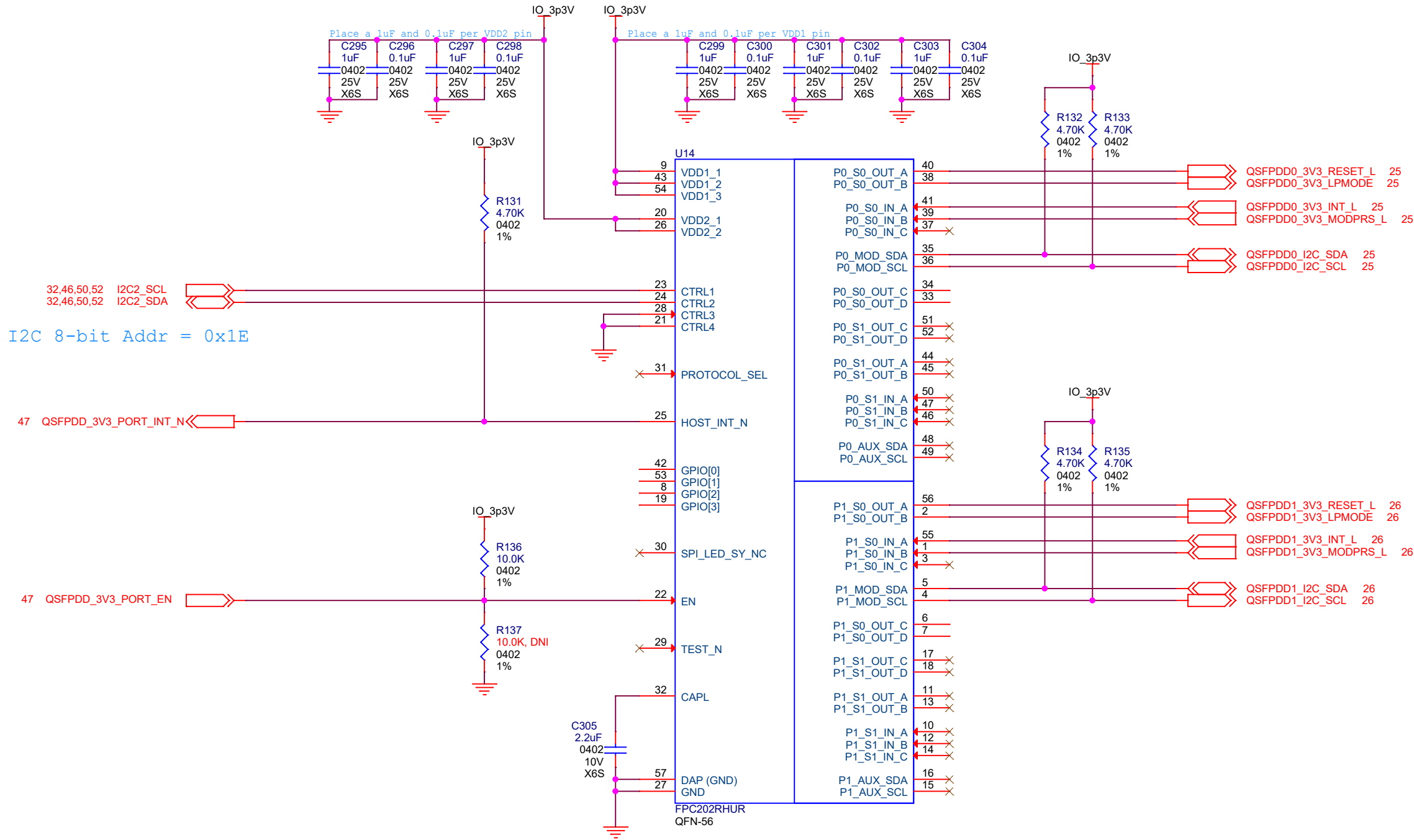
Place close to QSFPDD Connector



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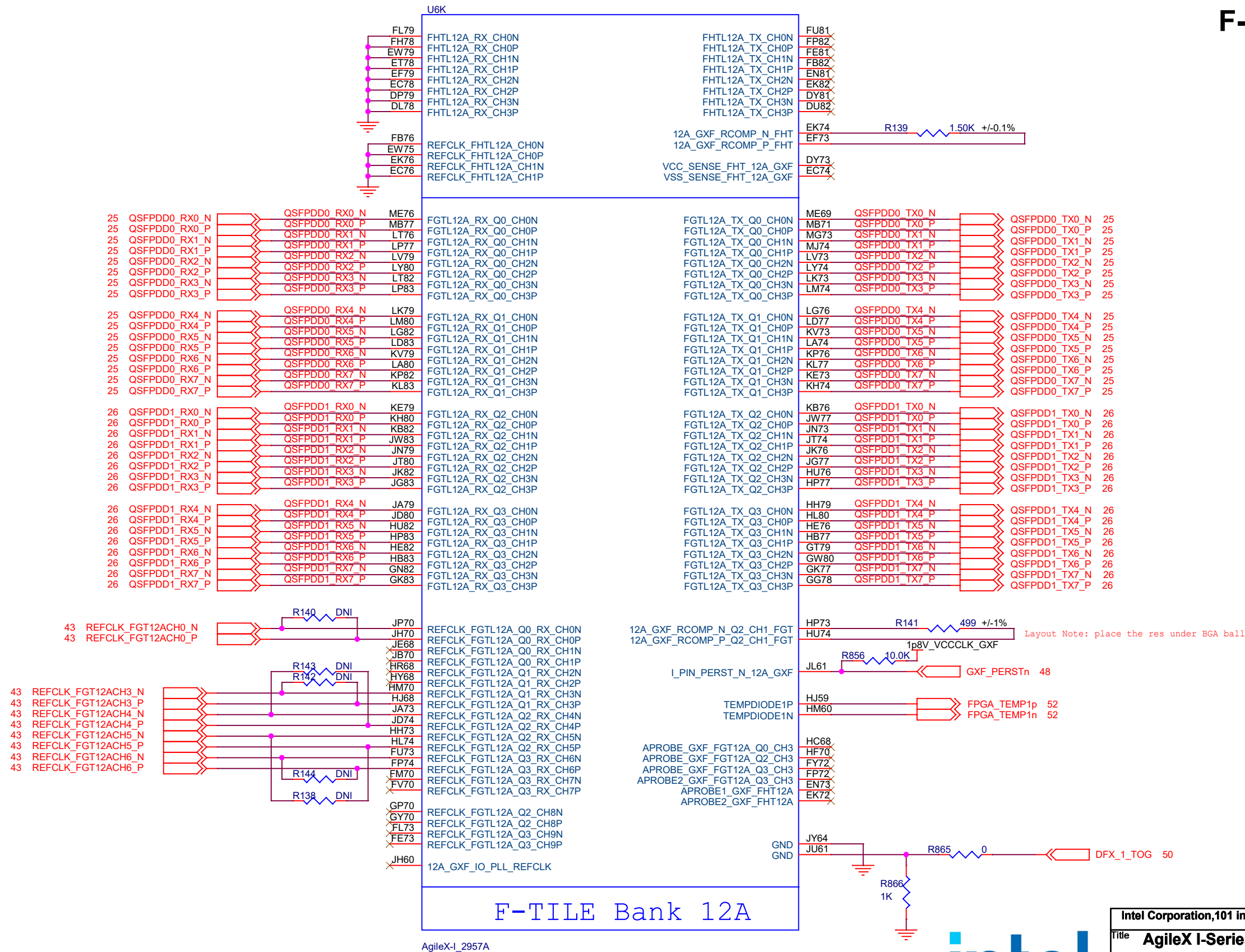


I2C 8-bit Addr = 0x1E



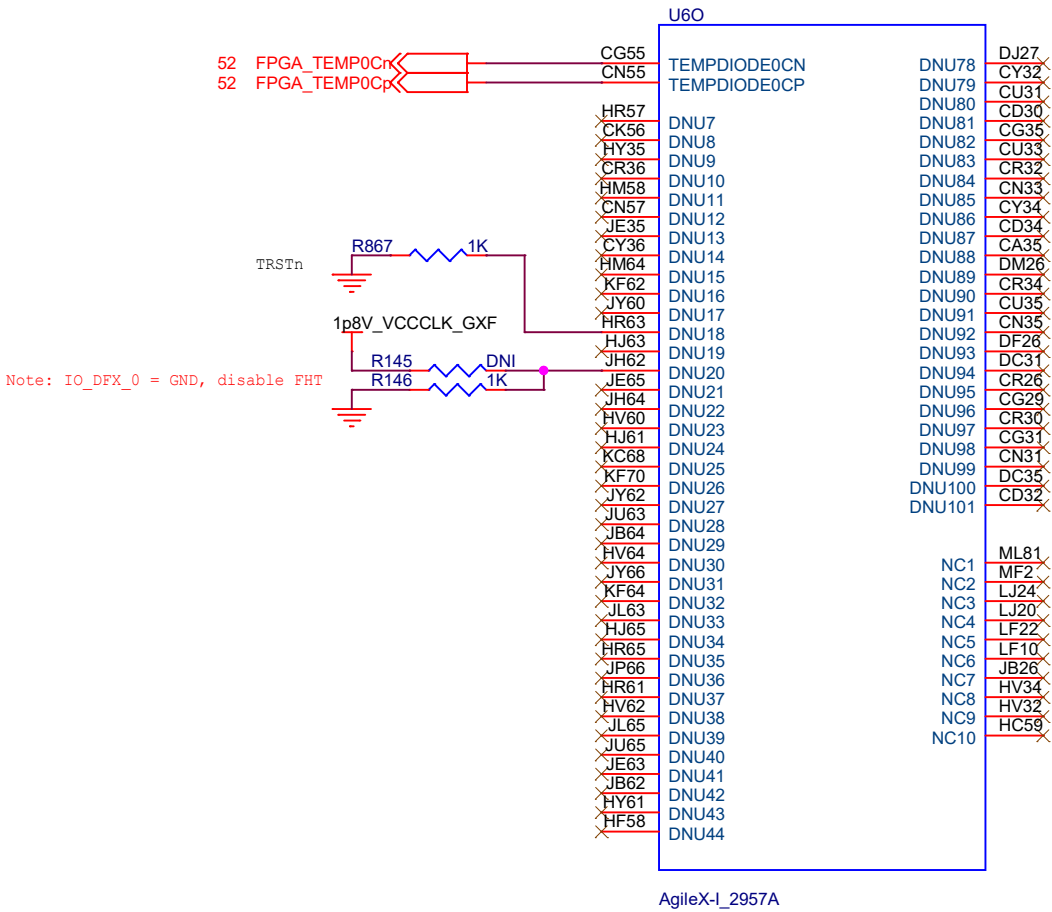
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F-TILE BANK 12A



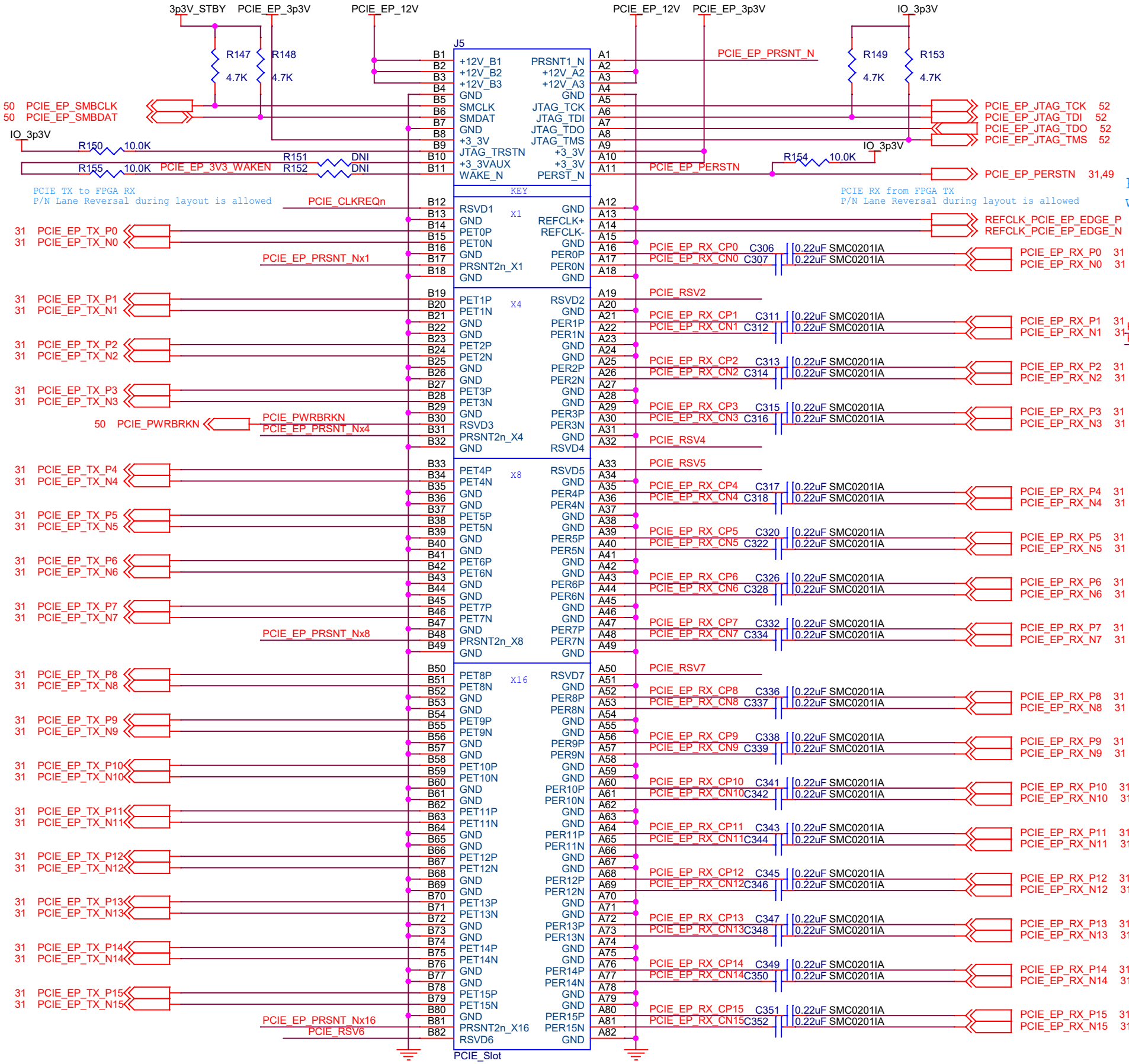
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F-TILE BANK 12A DNU

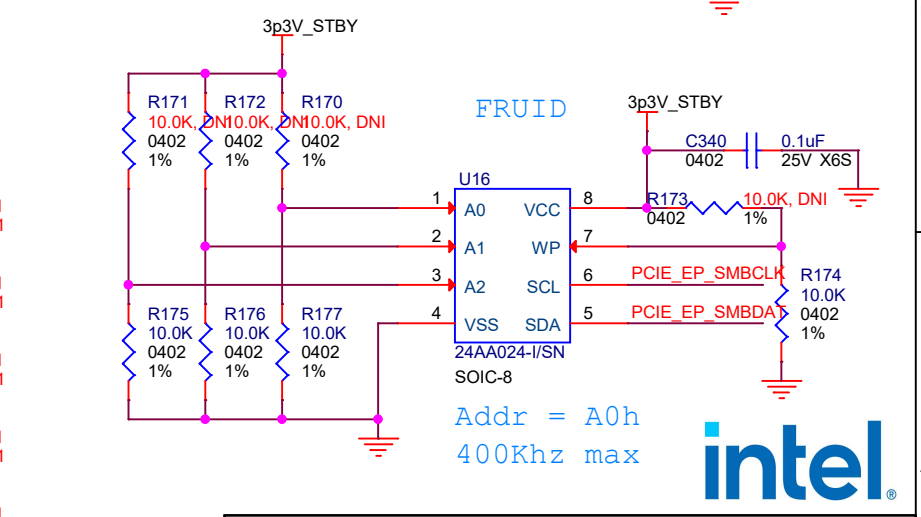
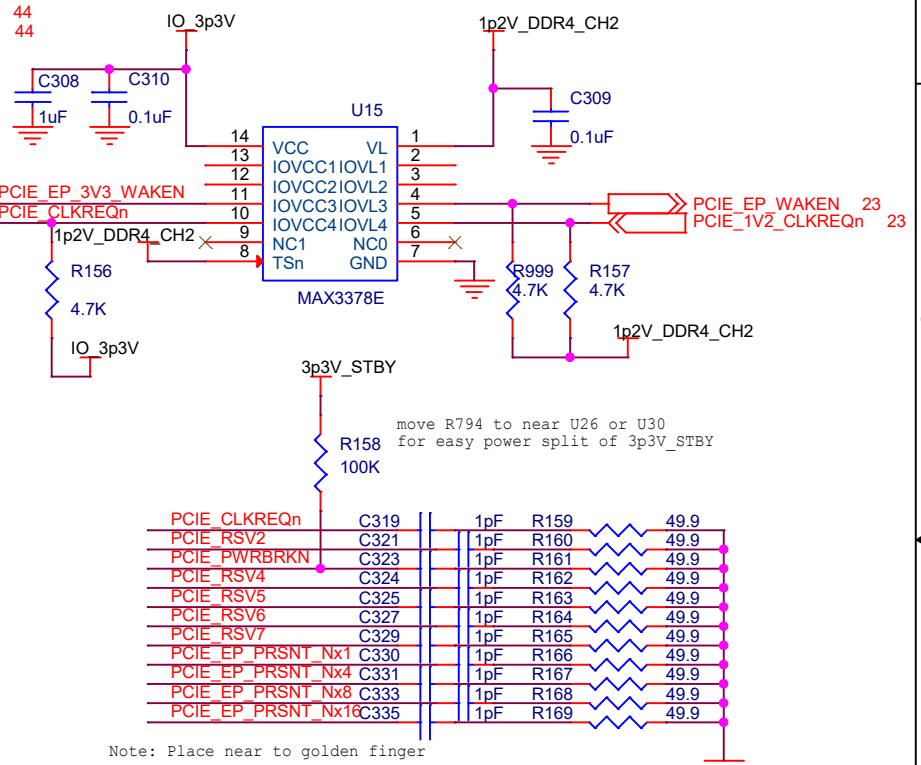


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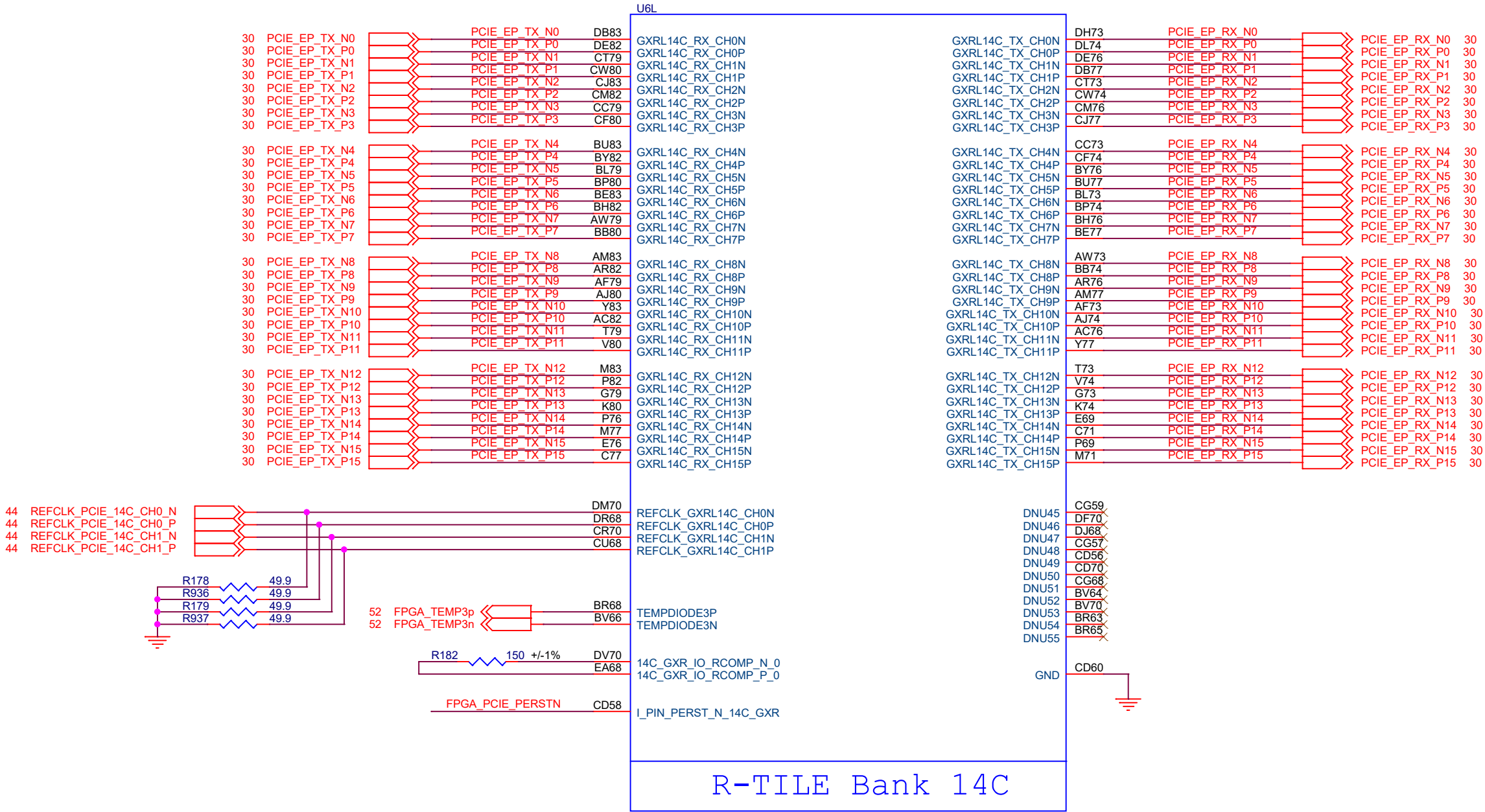
PCIe Endpoint Edge Connector



PCIe TX/RX signal naming convention with respect to CPU



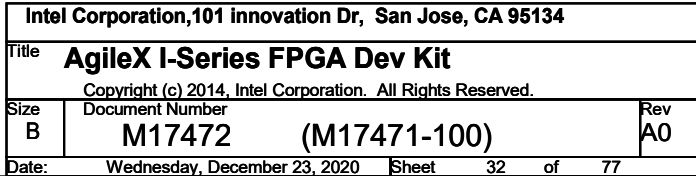
R-TILE BANK 14C



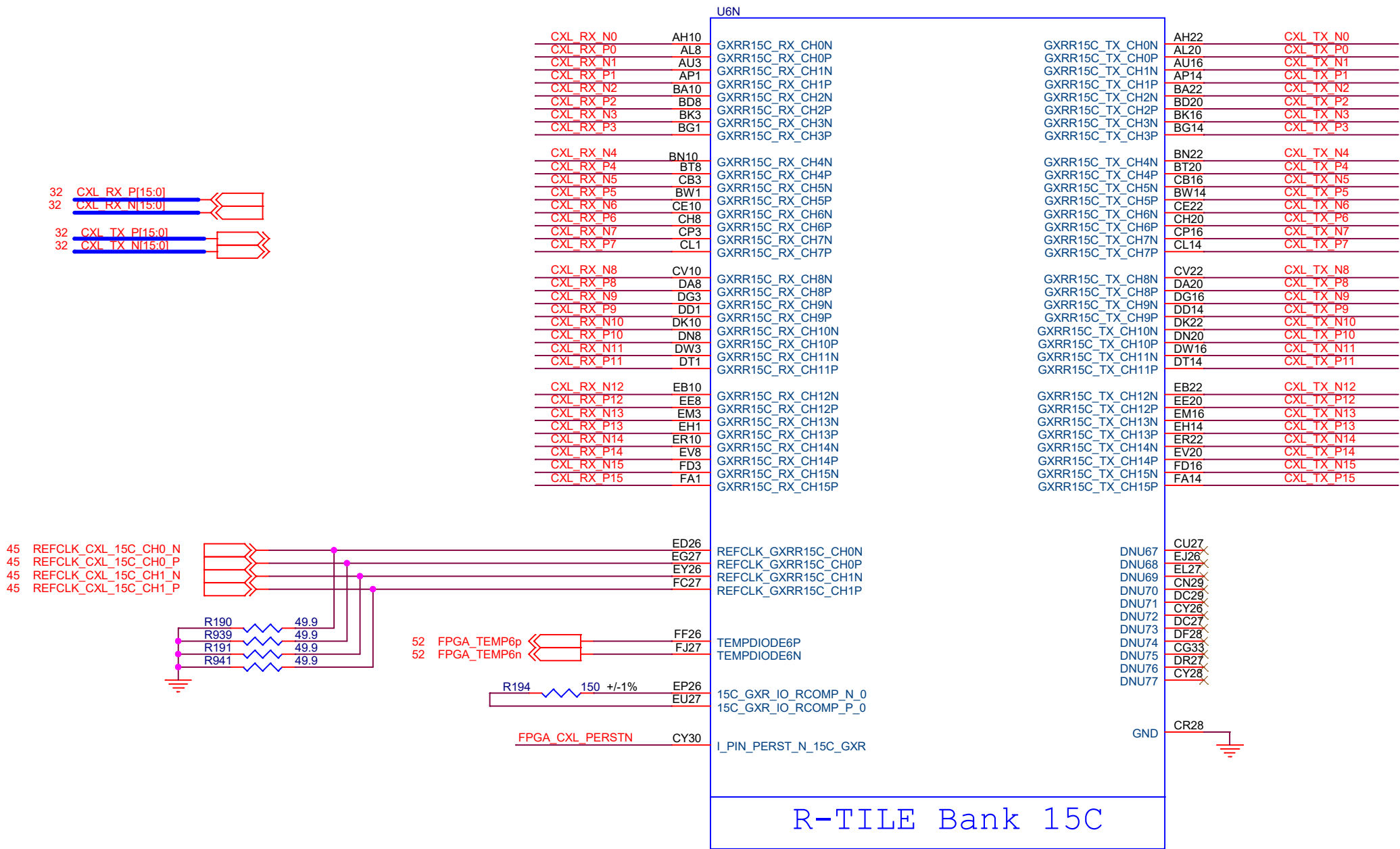
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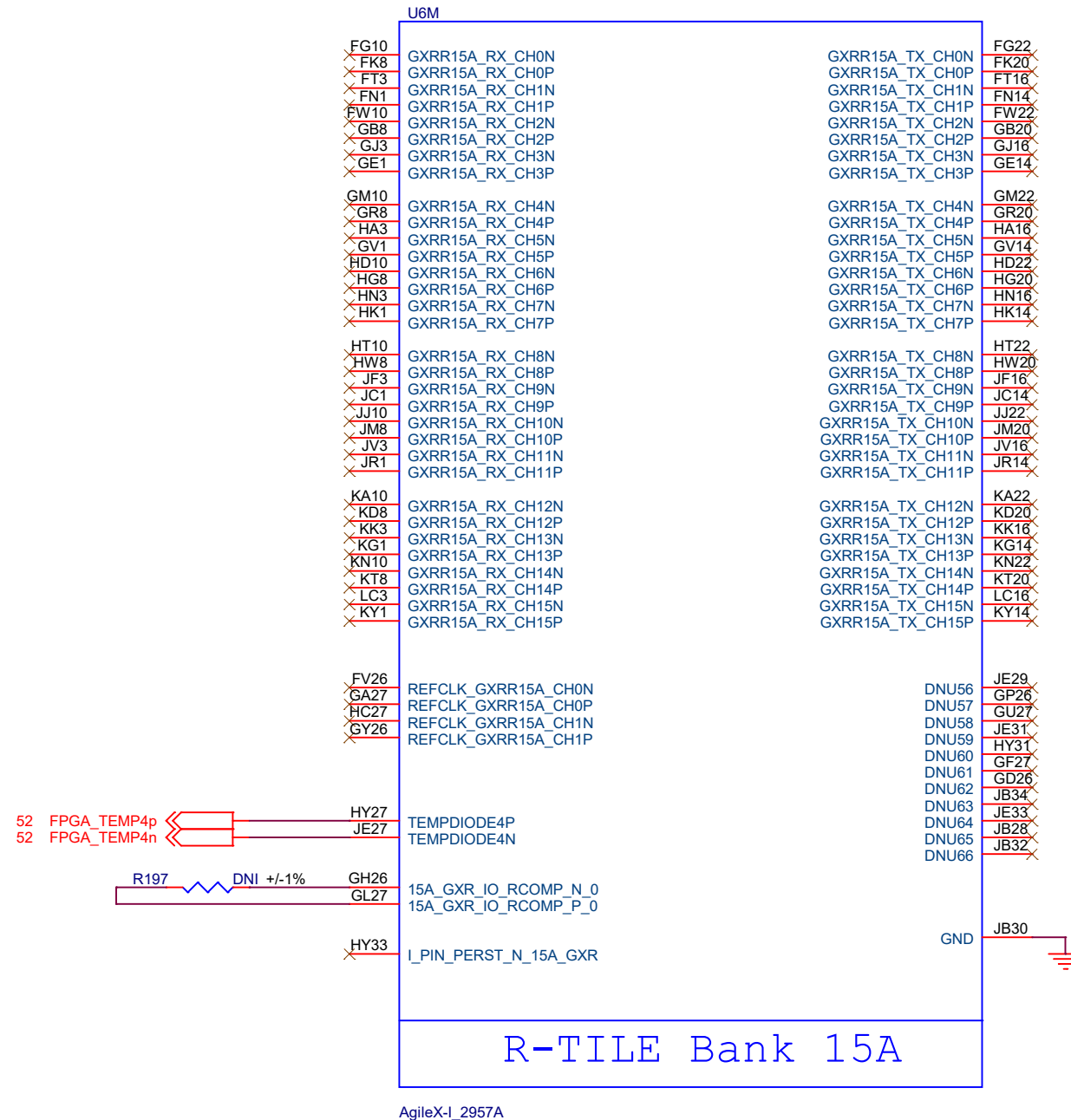


R-TILE BANK 15C



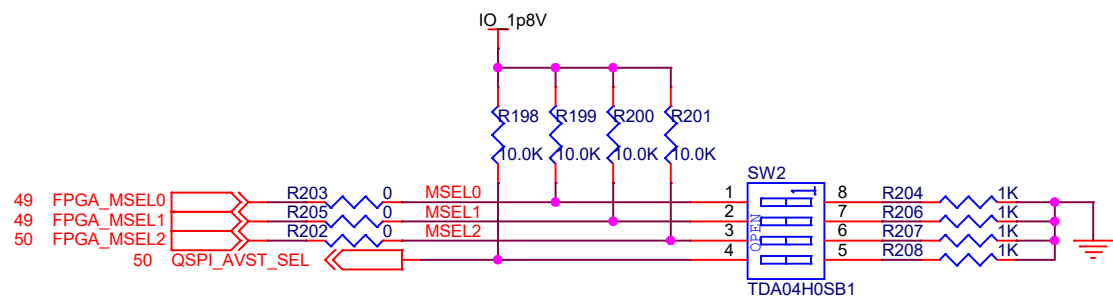
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R-TILE BANK 15A



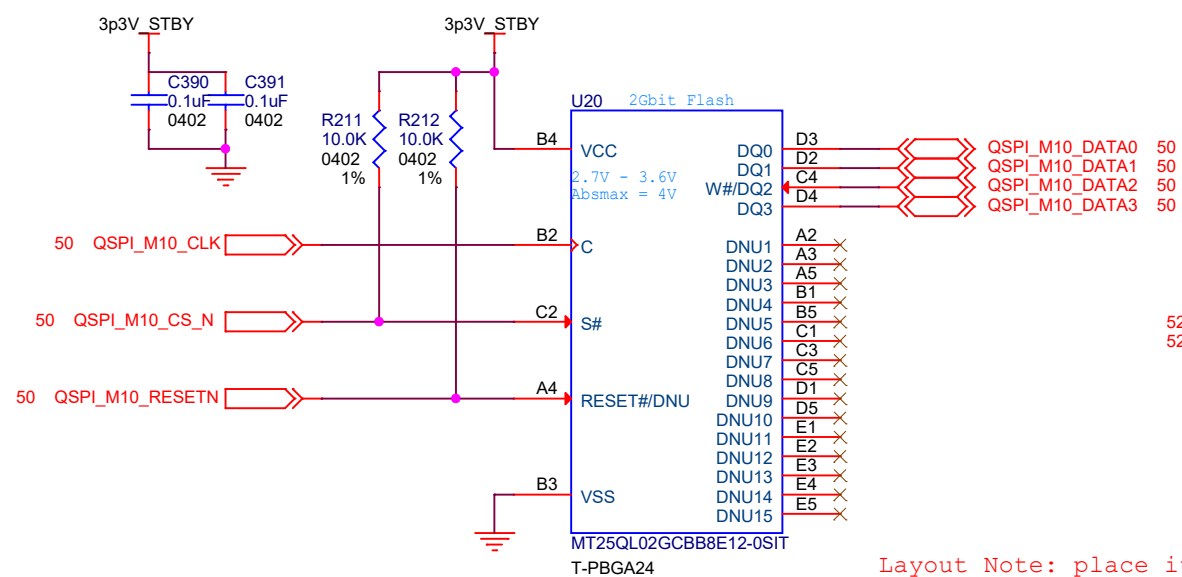
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SDM & Configuration



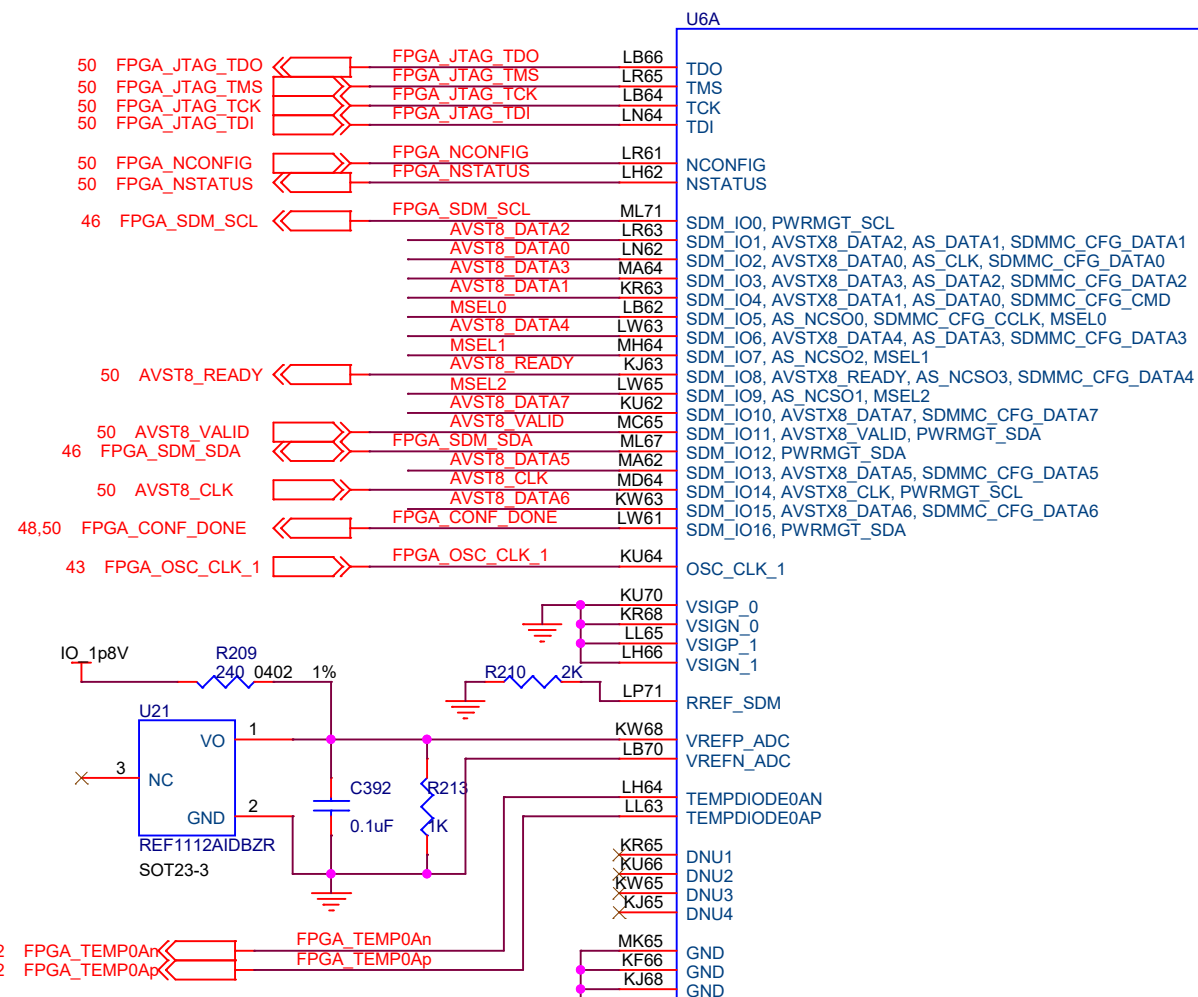
Close = 0, Open = 1

Config Mode	MSEL2	MSEL1	MSEL0
JTAG	1	1	1
AVST x8	1	1	0



2Gb Serial Flash

Layout Note: place it near to max10

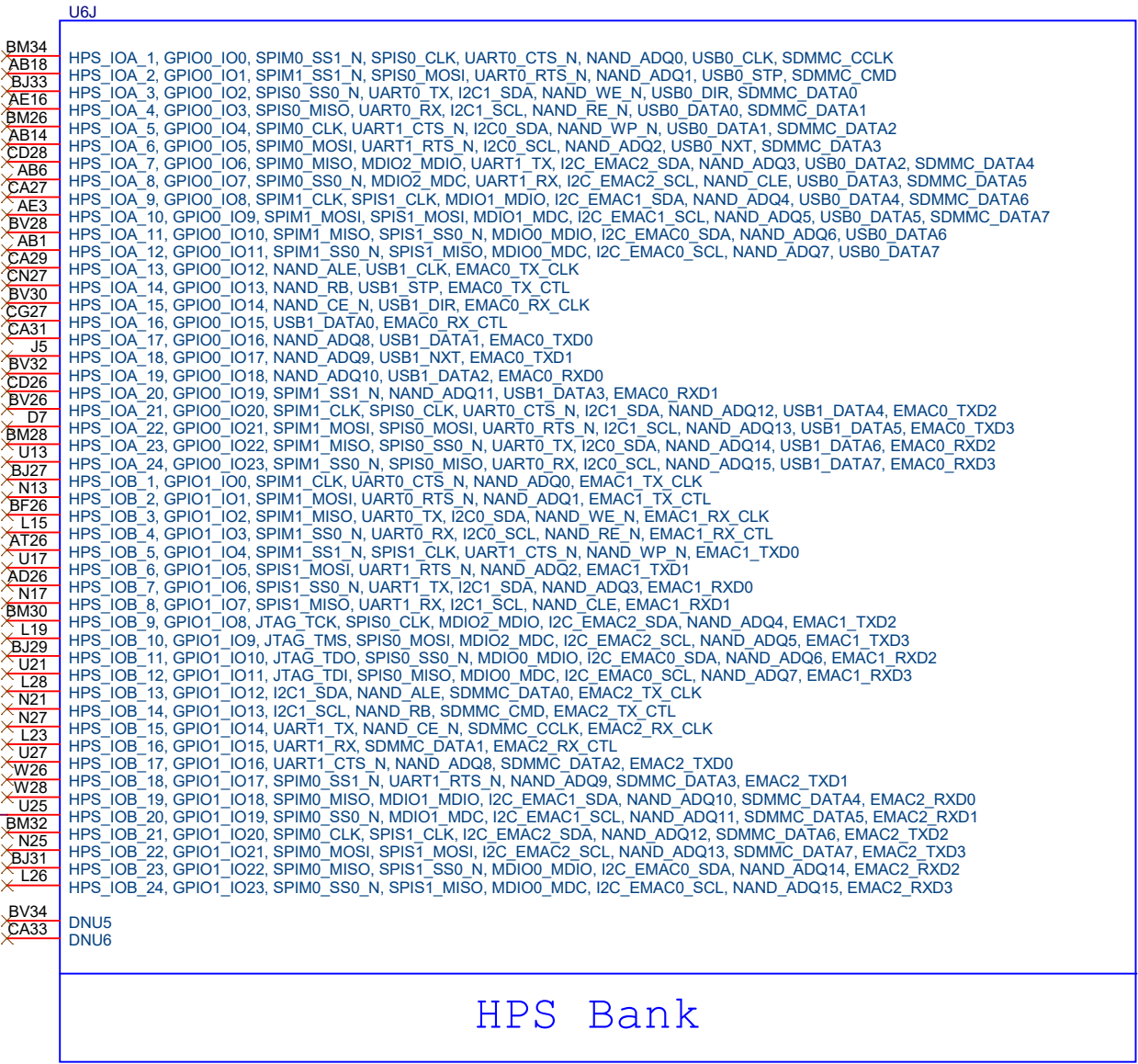


SDM Bank

AgileX-I_2957A



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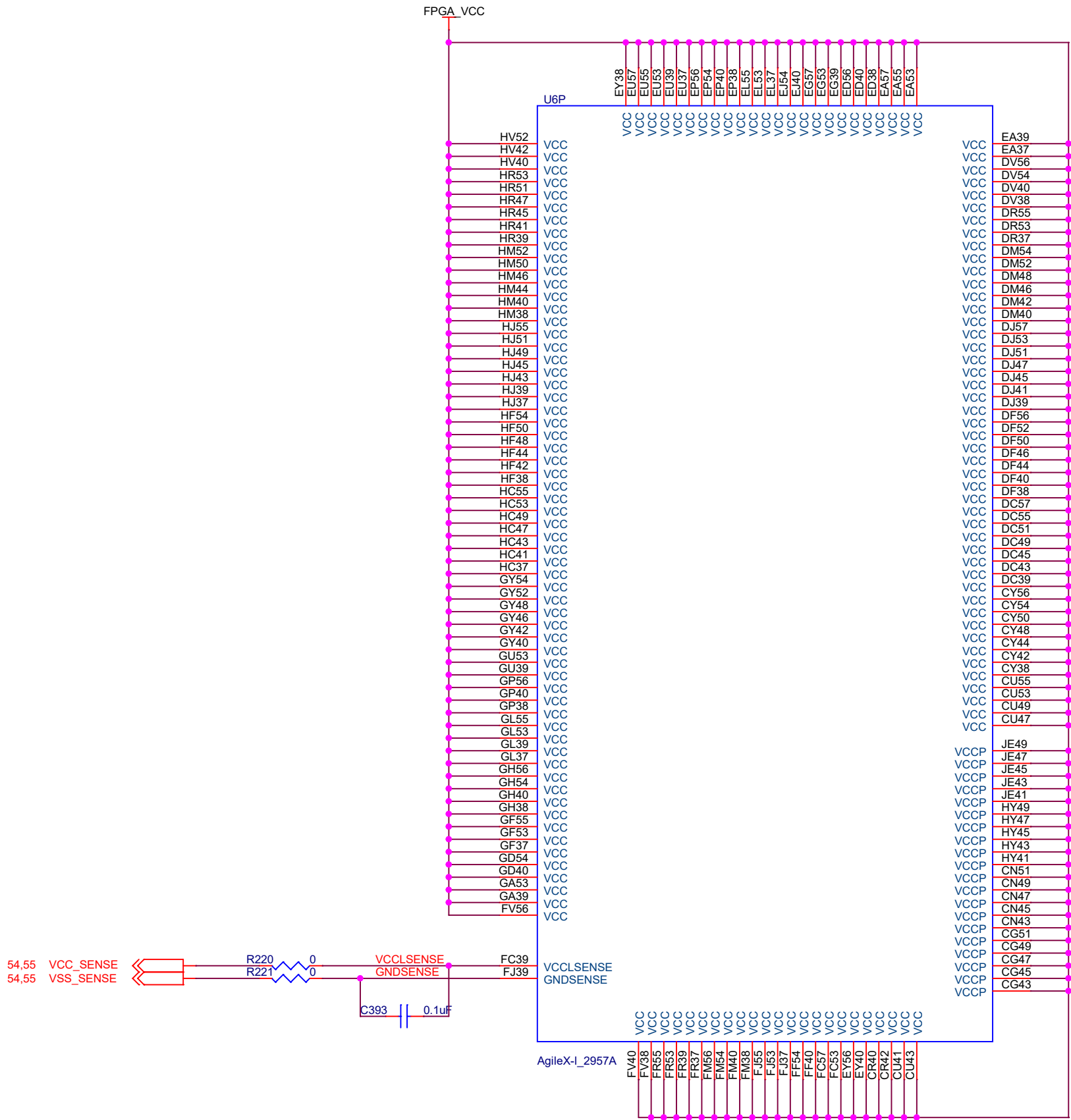
AgileX-I_2957A

43 HPS_OSC_CLK



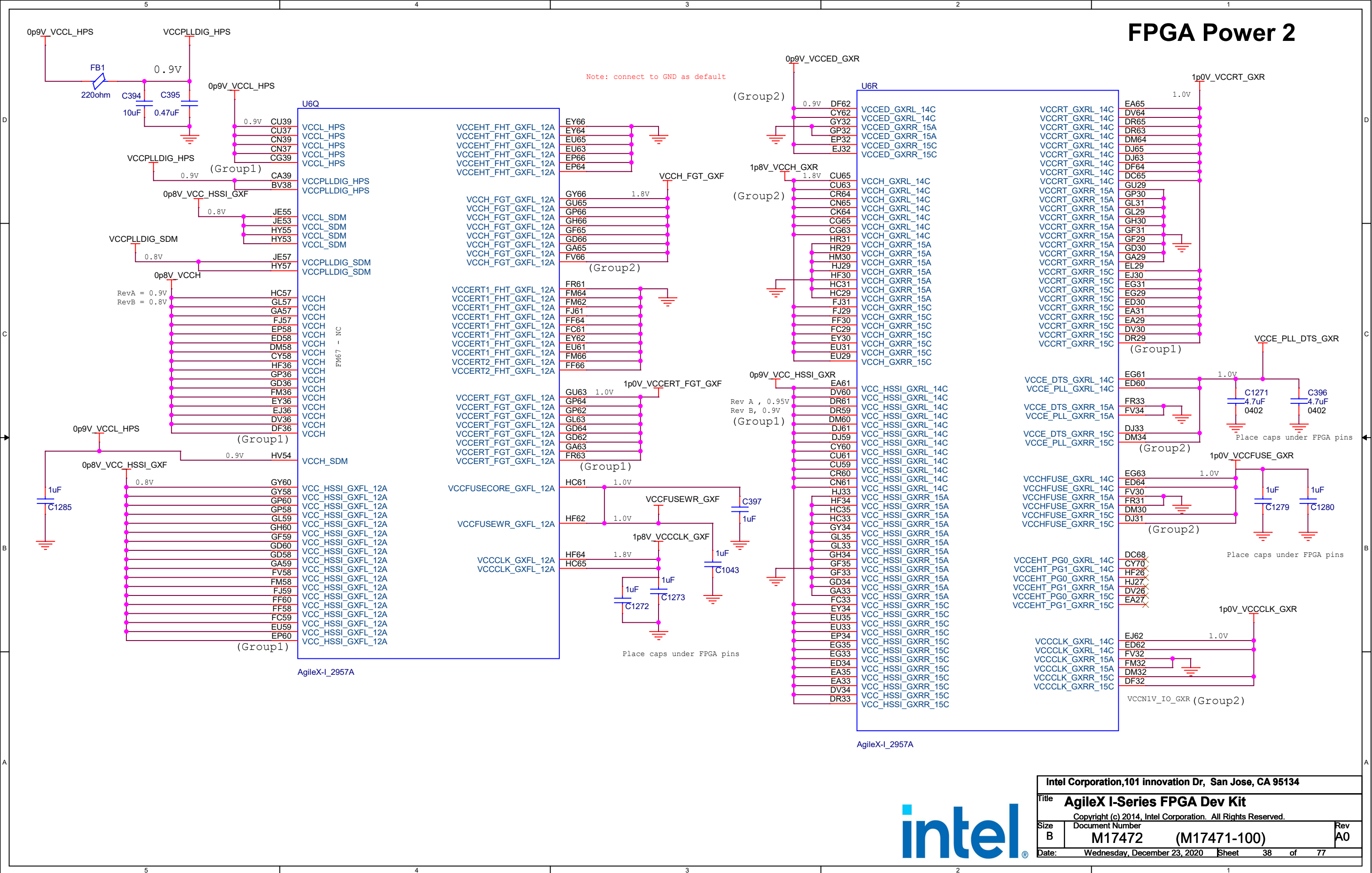
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FPGA Power 1

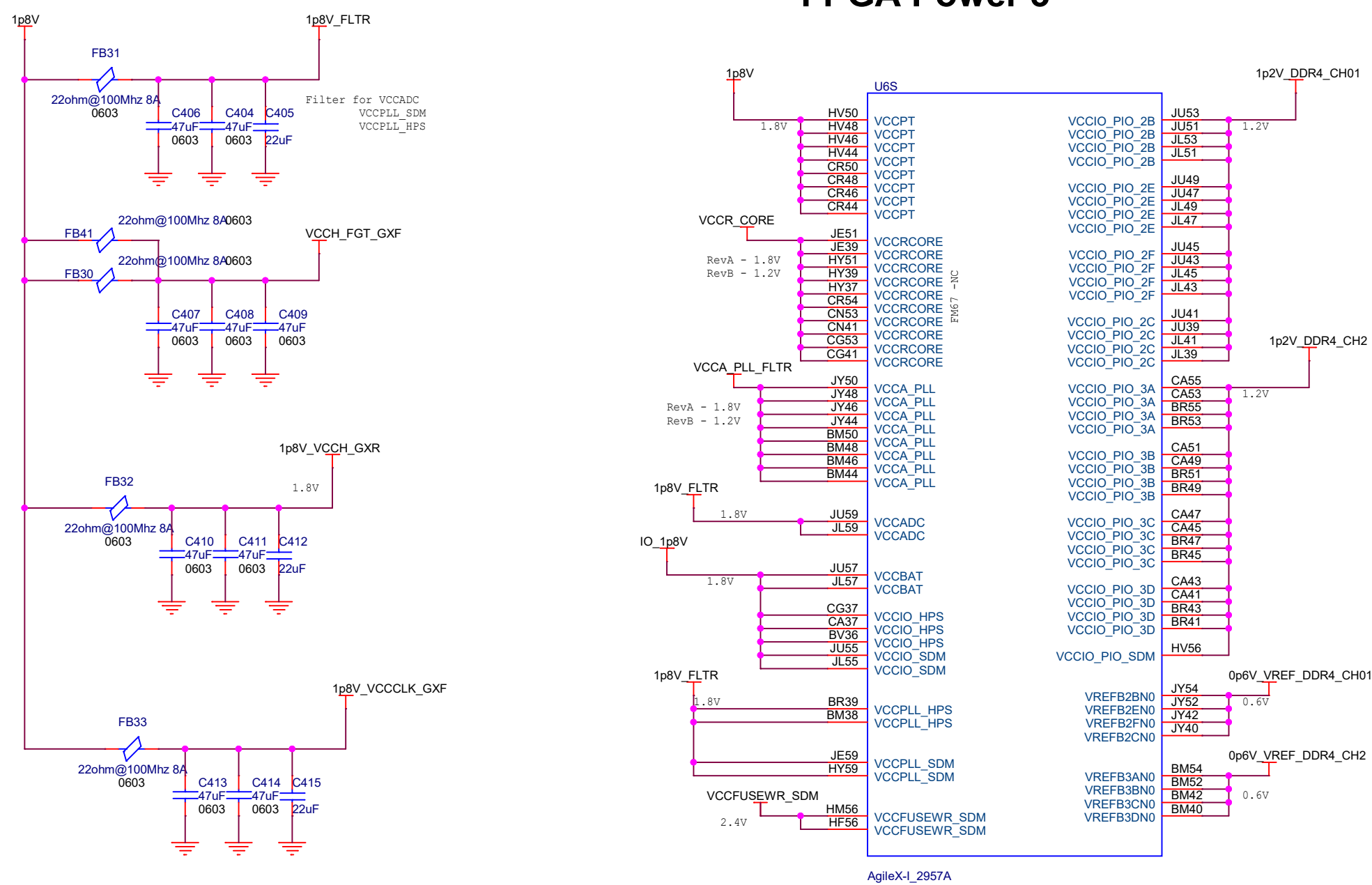


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FPGA Power 2

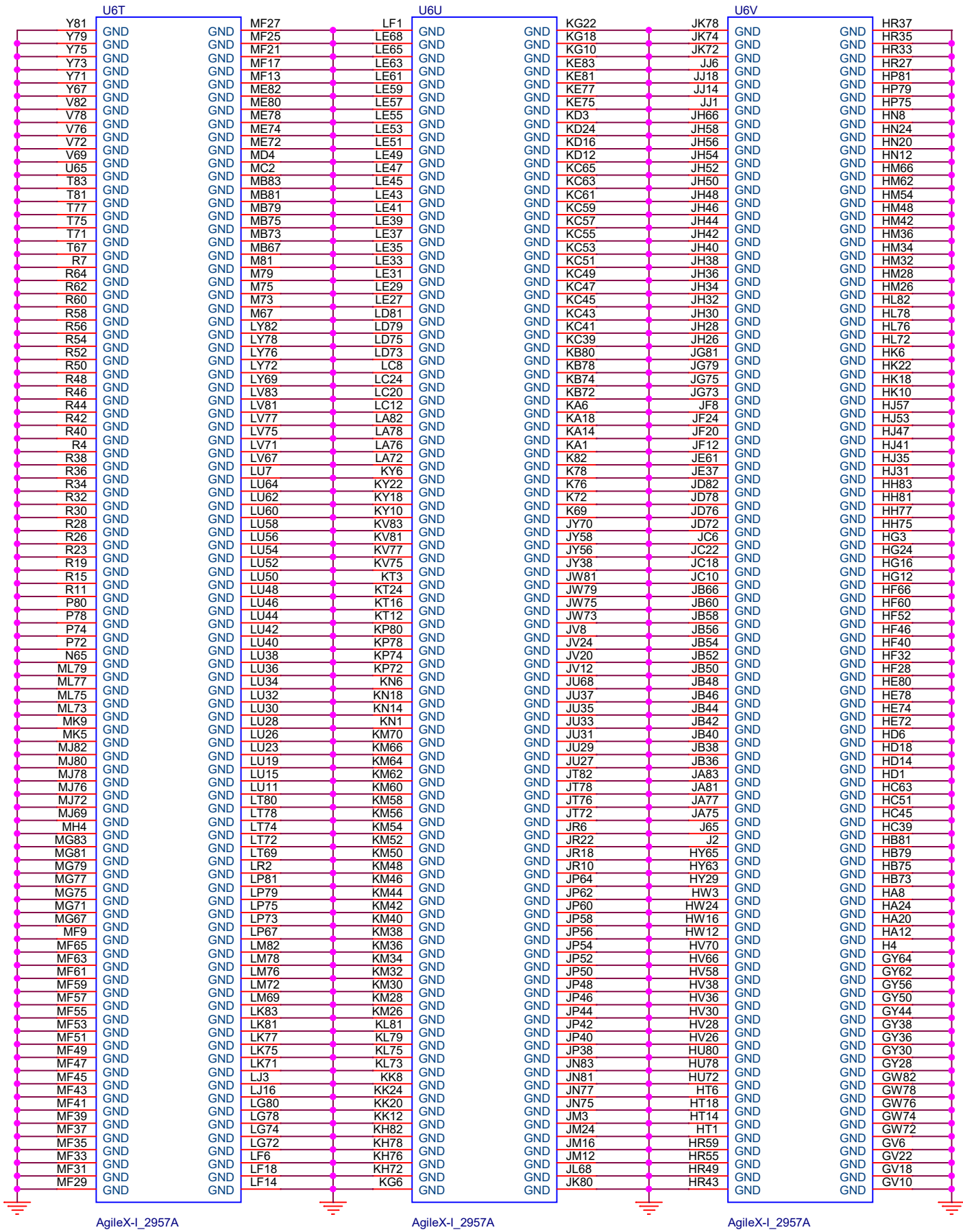


FPGA Power 3



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FPGA GND 1



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FPGA GND 2

U6W		
GU68	GND	FY82
GU61	GND	FY80
GU59	GND	FY78
GU57	GND	FY76
GU55	GND	FY74
GU37	GND	FW6
GU35	GND	FW18
GU33	GND	FW14
GU31	GND	FW1
GT83	GND	FV64
GT81	GND	FV62
GT77	GND	FV60
GT75	GND	FV54
GT73	GND	FV36
GR3	GND	FV28
GR24	GND	FU83
GR16	GND	FU79
GR12	GND	FU77
GP54	GND	FU75
GP34	GND	FT8
GP28	GND	FT24
GN80	GND	FT20
GN78	GND	FT12
GN76	GND	FR68
GN74	GND	FR65
GN72	GND	FR59
GM6	GND	FR57
GM18	GND	FR35
GM14	GND	FR29
GM1	GND	FR27
GL68	GND	FP80
GL65	GND	FP78
GL61	GND	FP76
GK81	GND	FN6
GK79	GND	FN22
GK75	GND	FN18
GK73	GND	FN10
GJ8	GND	FM60
GJ24	GND	FM34
GJ20	GND	FM30
GJ12	GND	FM28
GH70	GND	FM26
GH64	GND	FL83
GH62	GND	FL81
GH58	GND	FL77
GH36	GND	FL75
GH32	GND	FK3
GH28	GND	FK24
GG82	GND	FK16
GG80	GND	FK12
GG76	GND	FJ68
GG74	GND	FJ65
GG72	GND	FJ63
GF68	GND	FJ35
GF63	GND	FJ33
GF61	GND	FH82
GF57	GND	FH80
GF39	GND	FH76
GE6	GND	FH74
GE22	GND	FH72
GE18	GND	FG6
GE10	GND	FG18
GD70	GND	FG14
GD56	GND	FG1
GD38	GND	FF70
GD32	GND	FF62
GD28	GND	FF56
GC83	GND	FF38
GC81	GND	FF36
GC79	GND	FF34
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GC75	GND	FF28
GC73	GND	FE83
GB3	GND	FE79
GB24	GND	FE77
GB16	GND	FE75
GB12	GND	FD8
GA68	GND	FD24
GA61	GND	FD20
GA55	GND	FD12
GA37	GND	FC68
GA35	GND	FC65
GA31	GND	FC63
G83	GND	FC55
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G71	GND	FB80
G67	GND	FB78

AgileX-I_2957A

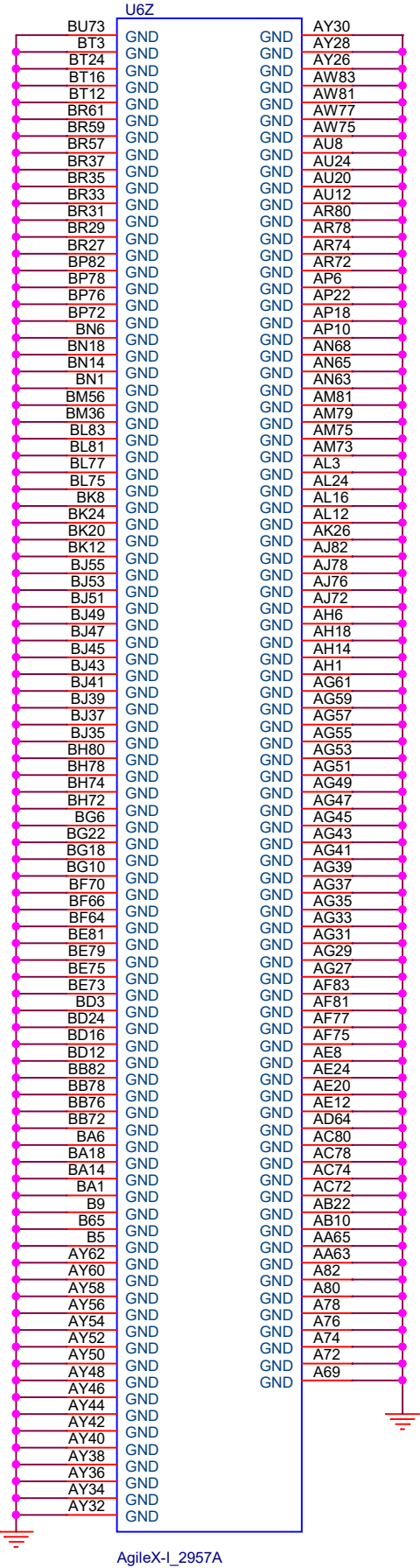
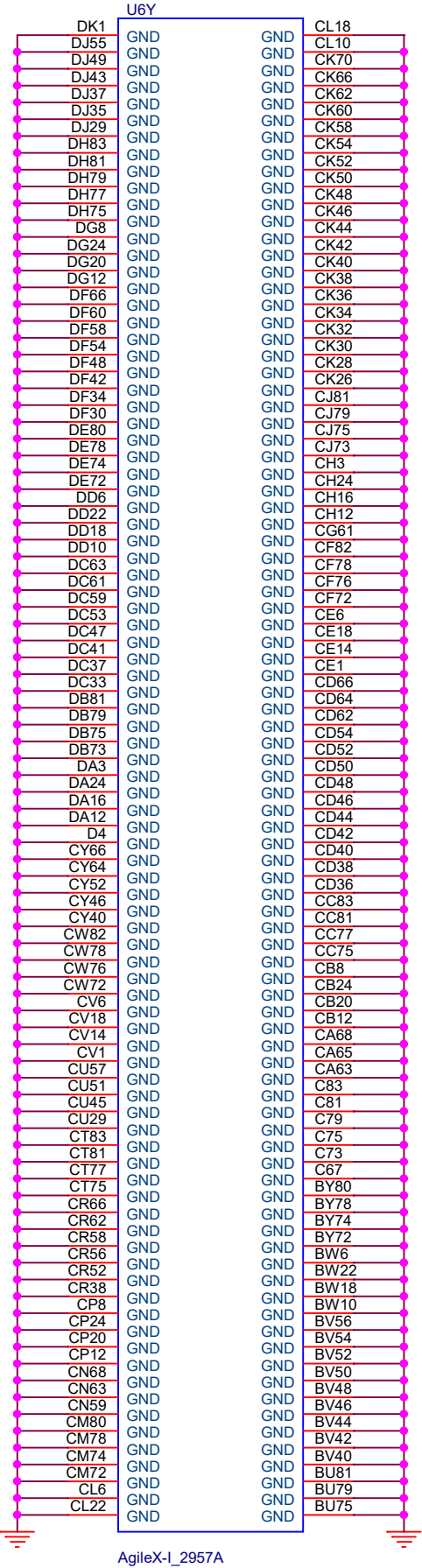
U6X		
FB74	GND	EJ34
FB72	GND	EJ28
FA6	GND	EH6
FA22	GND	EH22
FA18	GND	EH18
FA10	GND	EH10
F9	GND	EG68
F65	GND	EG65
F63	GND	EG59
F61	GND	EG55
F59	GND	EG37
F57	GND	EF83
F55	GND	EF81
F53	GND	EF77
F51	GND	EF75
F5	GND	EE3
F49	GND	EE24
F47	GND	EE16
F45	GND	EE12
F43	GND	ED70
F41	GND	ED66
F39	GND	ED54
F37	GND	ED36
F35	GND	ED32
F33	GND	ED28
F31	GND	EC82
F29	GND	EC80
F27	GND	EC72
F25	GND	EB6
F21	GND	EB18
F2	GND	EB14
F17	GND	EB1
F13	GND	EA63
EY70	GND	EA59
EY60	GND	E82
EY58	GND	E80
EY54	GND	E78
EY32	GND	E74
EY28	GND	E72
EW83	GND	DY83
EW81	GND	DY79
EW77	GND	DY77
EW73	GND	DY75
EV3	GND	DW8
EV24	GND	DW24
EV16	GND	DW20
EV12	GND	DW12
EU68	GND	DV66
ET82	GND	DV62
ET80	GND	DV58
ET76	GND	DV32
ET74	GND	DV28
ET72	GND	DU80
ER6	GND	DU78
ER18	GND	DU76
ER14	GND	DU74
ER1	GND	DU72
EP70	GND	DT6
EP62	GND	DT22
EP36	GND	DT18
EP30	GND	DT10
EP28	GND	DR57
EN83	GND	DR39
EN79	GND	DR35
EN77	GND	DR31
EN75	GND	DP83
EM8	GND	DP81
EM24	GND	DP77
EM20	GND	DP75
EM12	GND	DP73
EL68	GND	DN3
EL65	GND	DN24
EL63	GND	DN16
EL61	GND	DN12
EL59	GND	DM66
EL57	GND	DM62
EL39	GND	DM56
EL35	GND	DM50
EL33	GND	DM44
EL31	GND	DM38
EK80	GND	DM36
EK78	GND	DM28
EJ70	GND	DL82
EJ66	GND	DL80
EJ64	GND	DL76
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EJ38	GND	DK14

AgileX-I_2957A



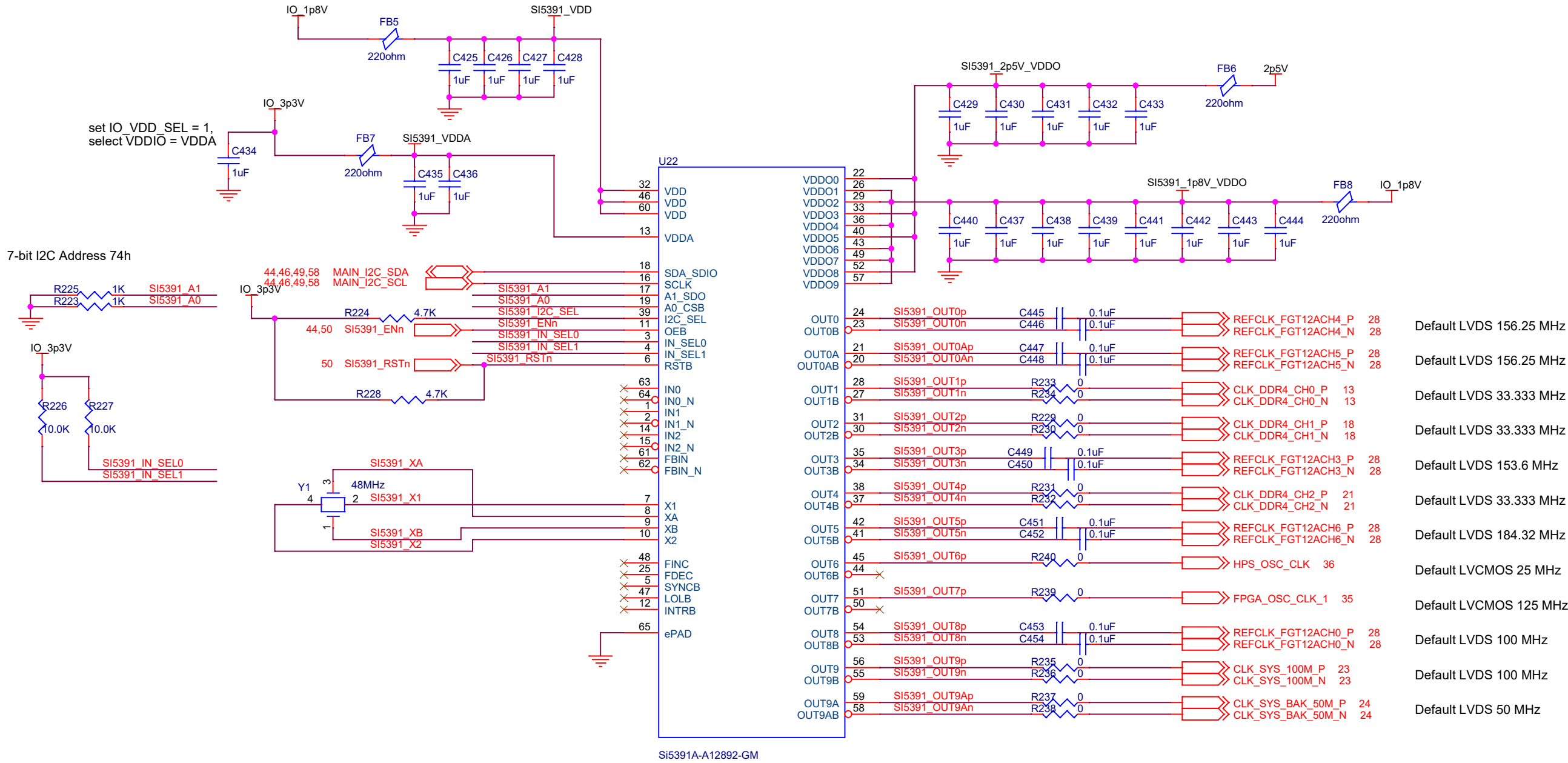
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FPGA GND 3



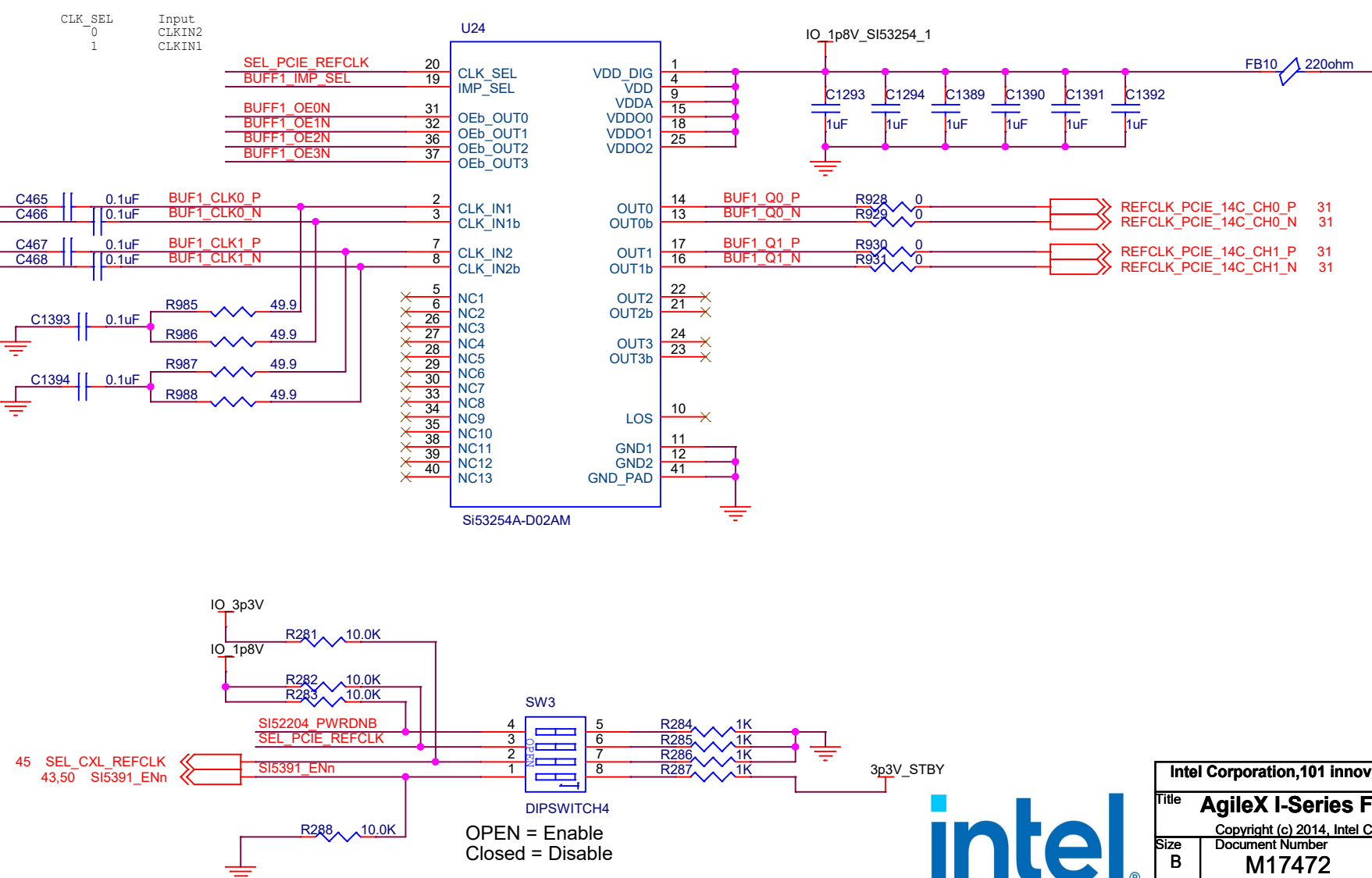
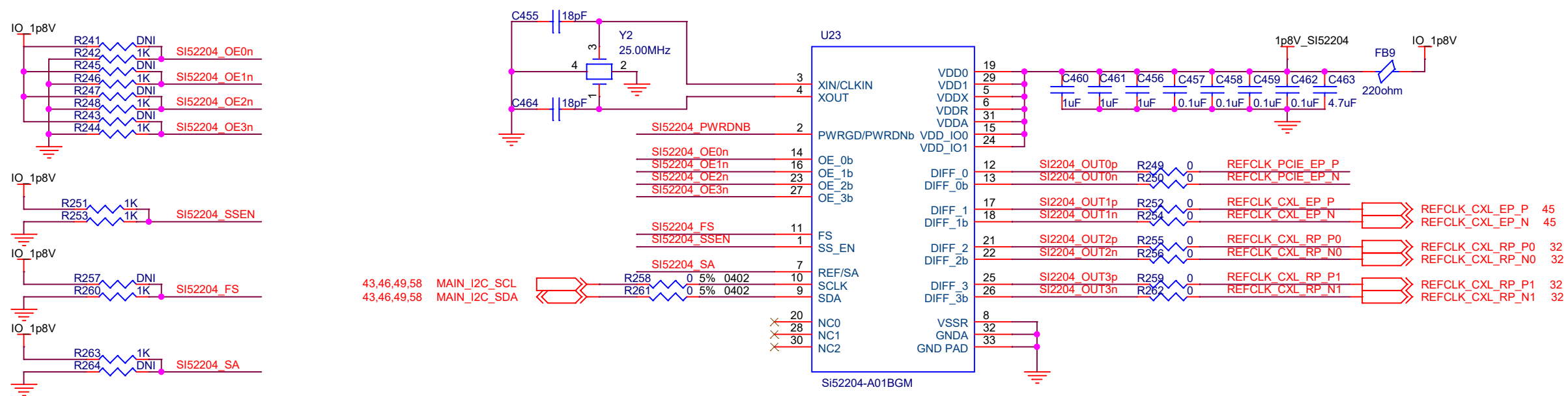
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Clock 1



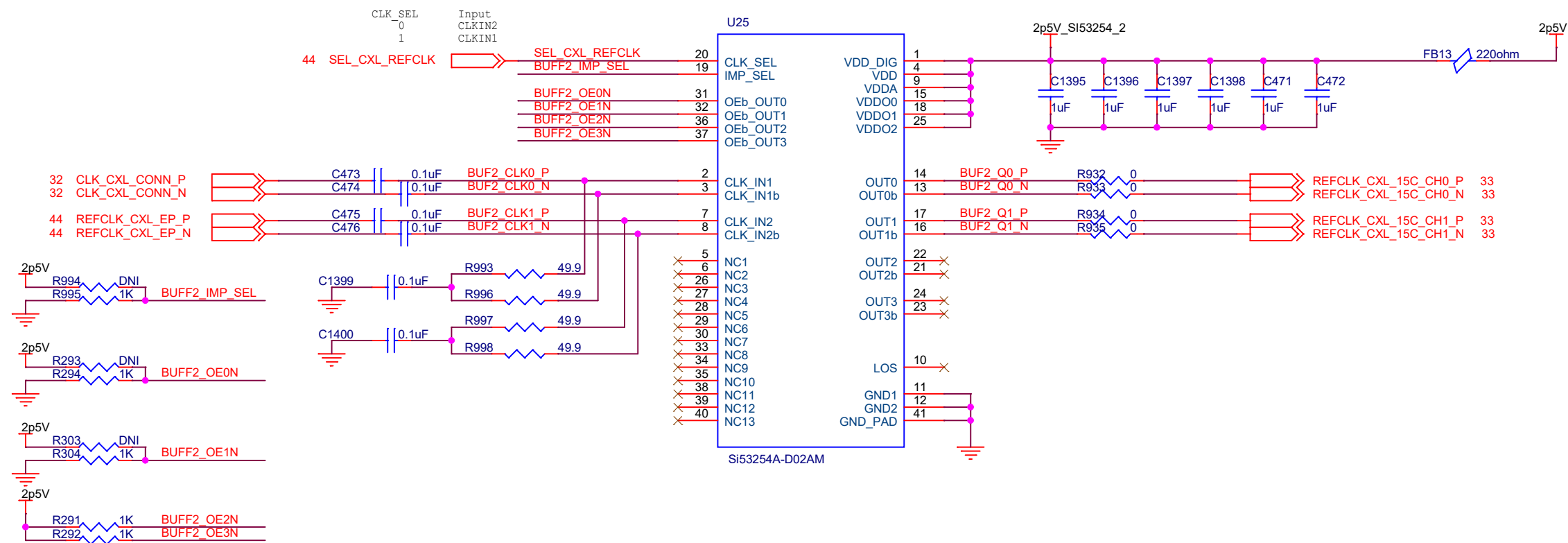
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Clock 2



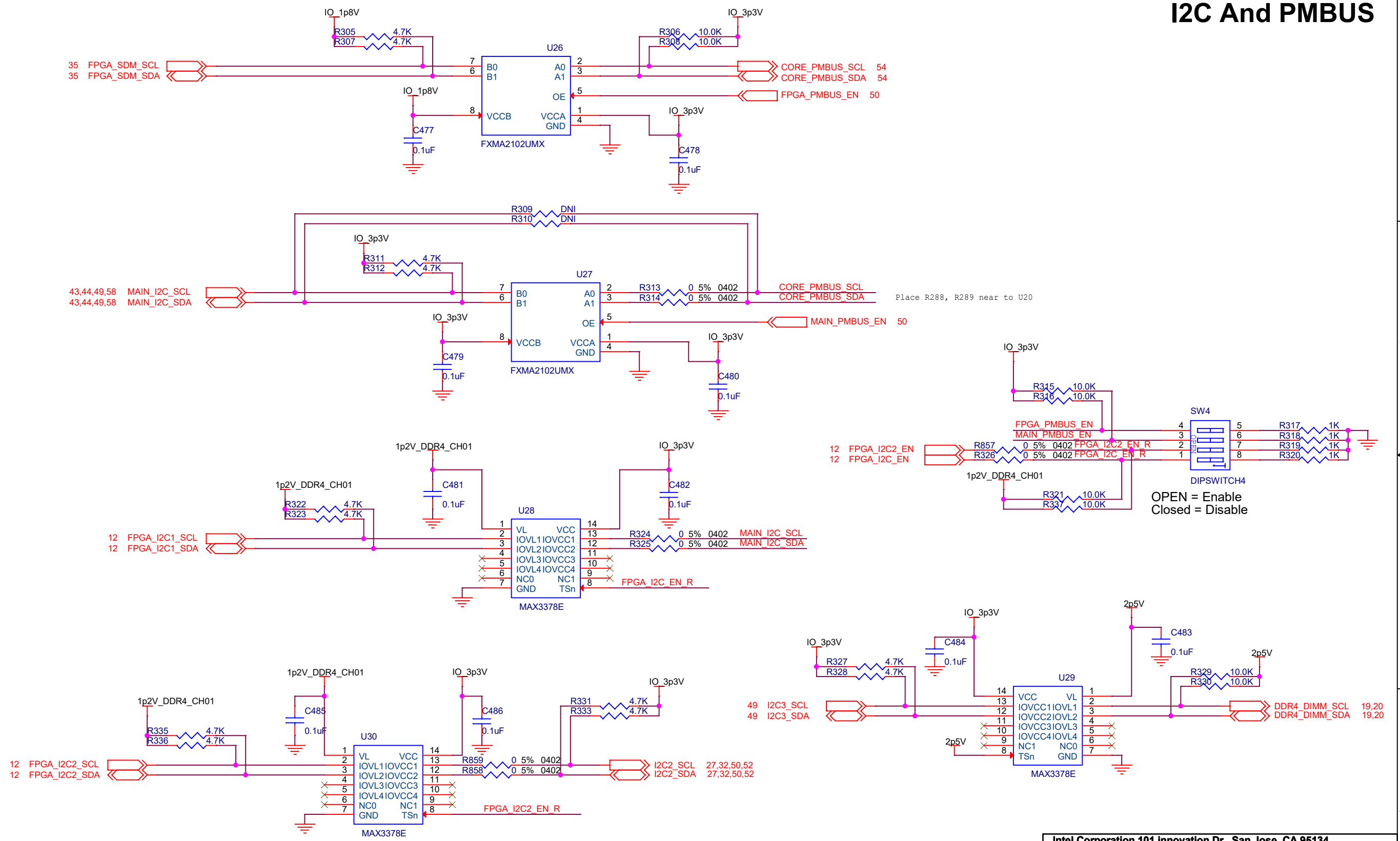
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Clock 3



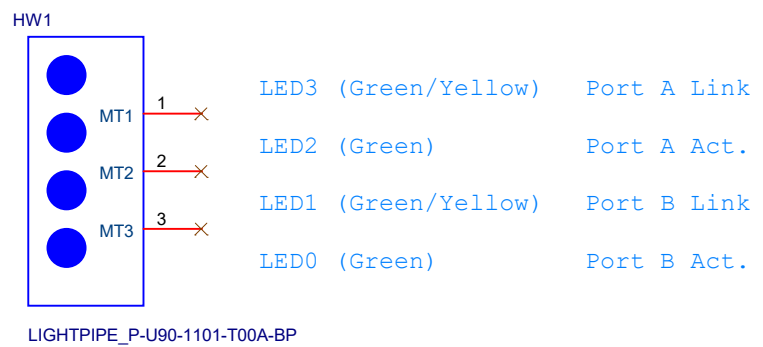
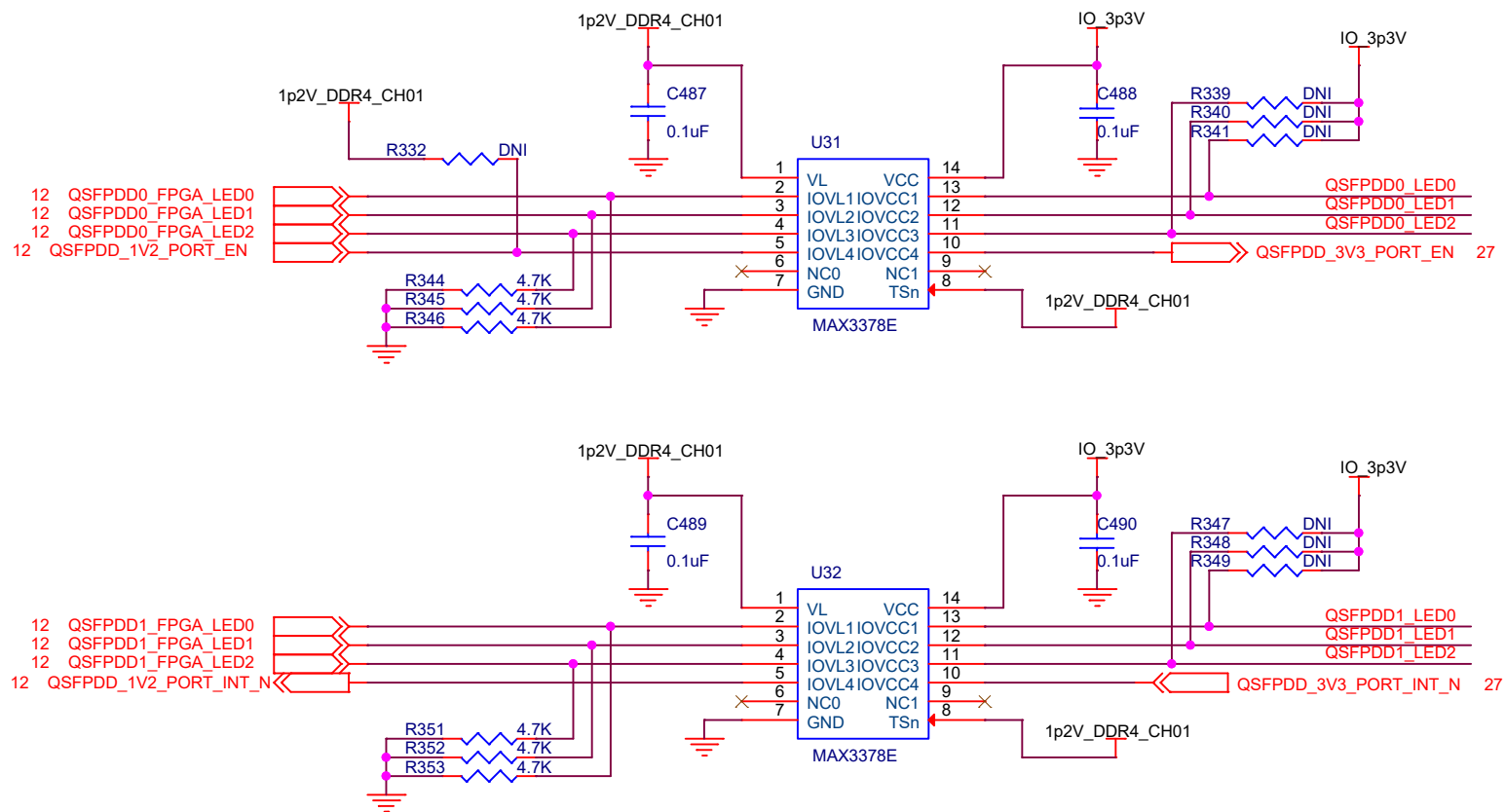
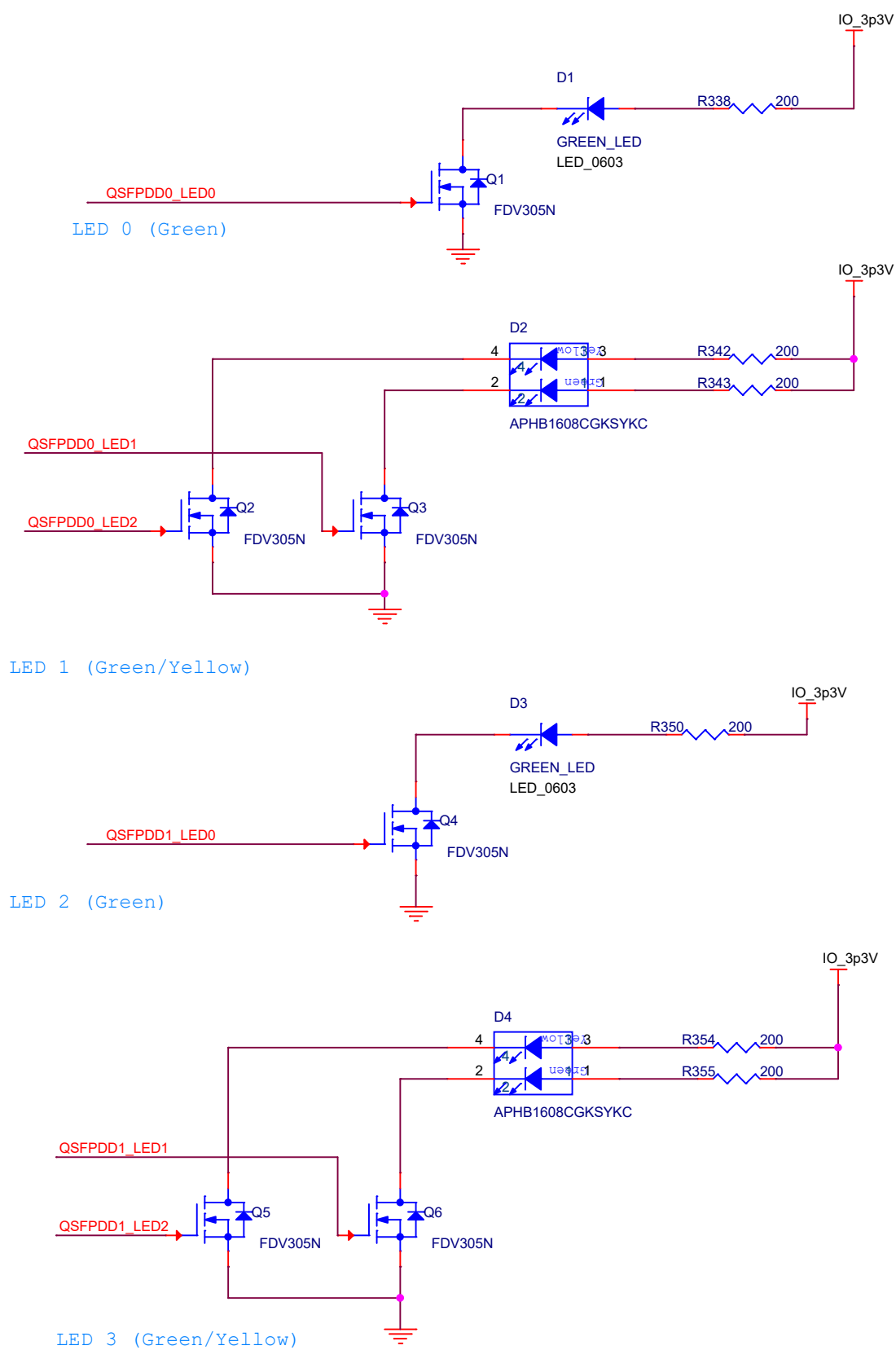
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I2C And PMBUS



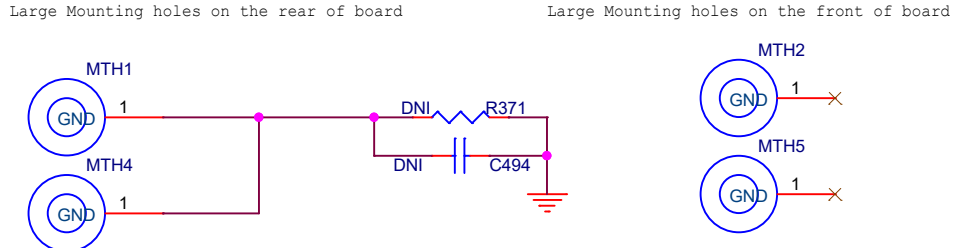
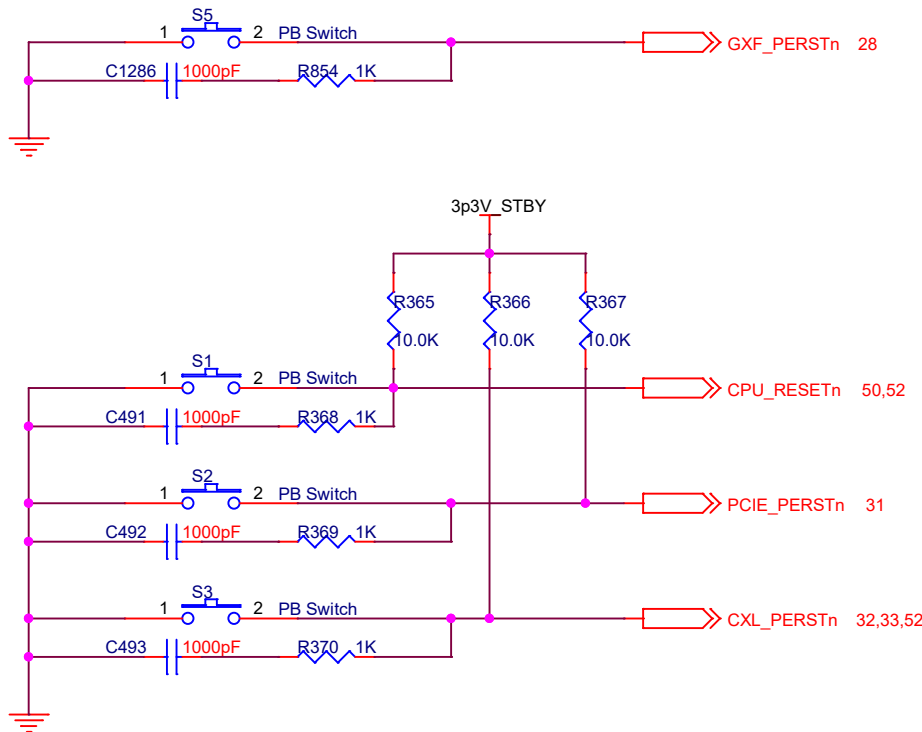
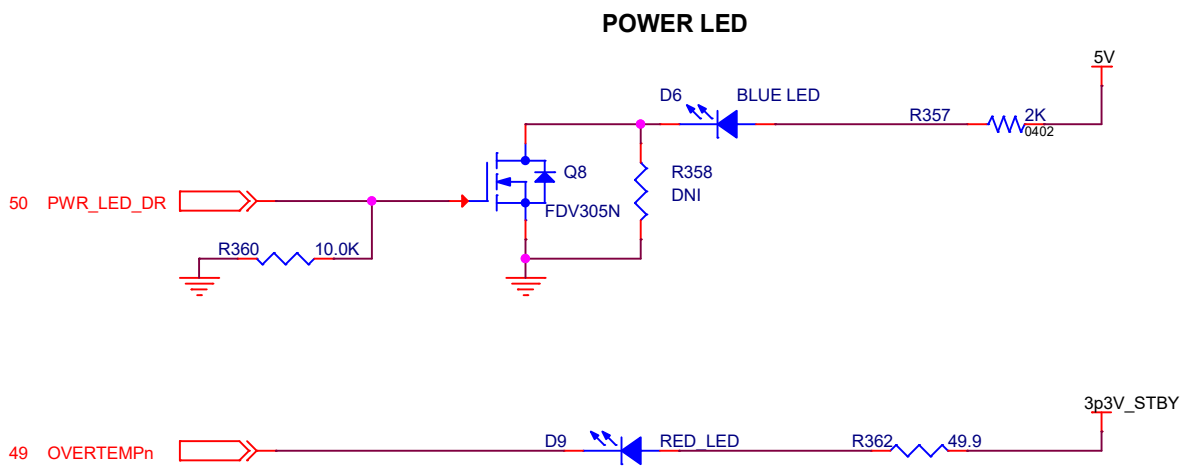
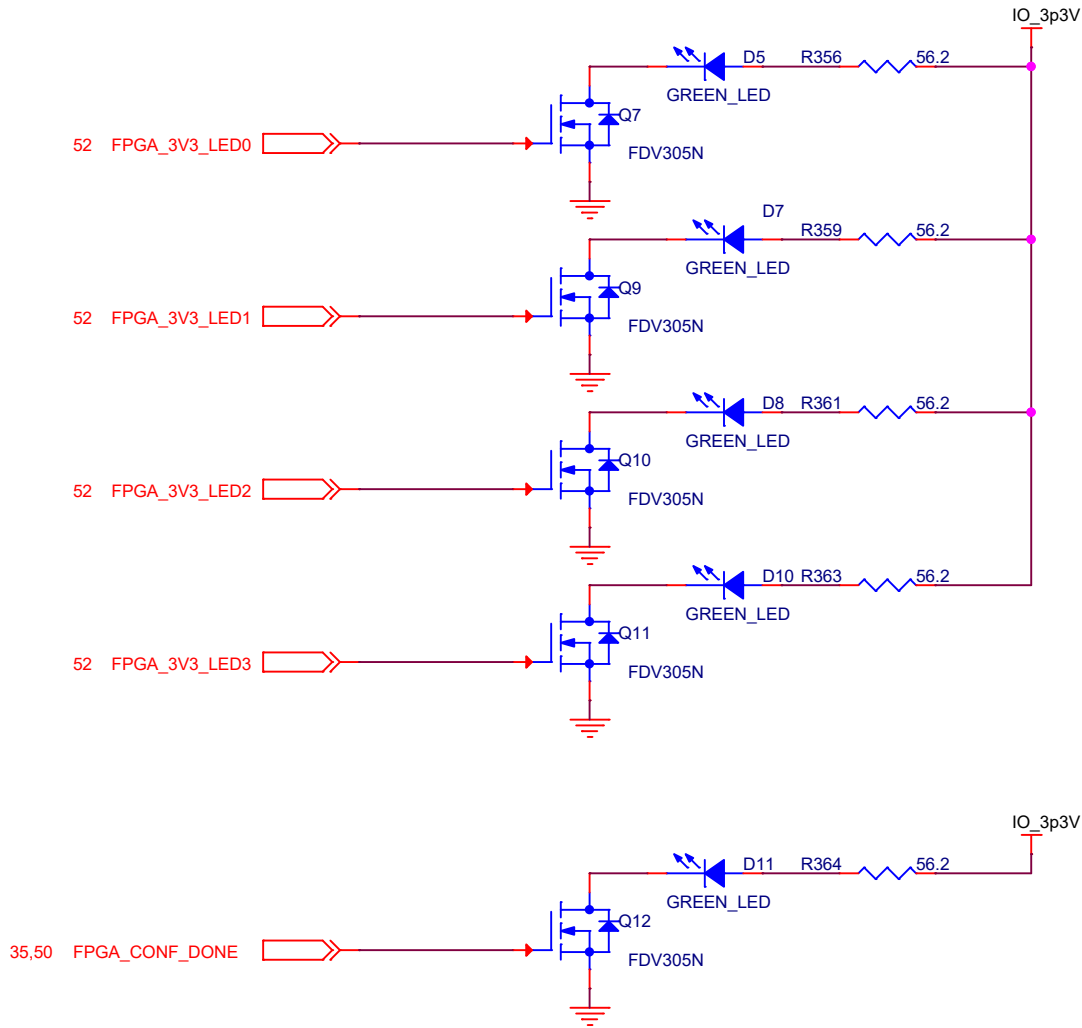
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QSFPDD LED



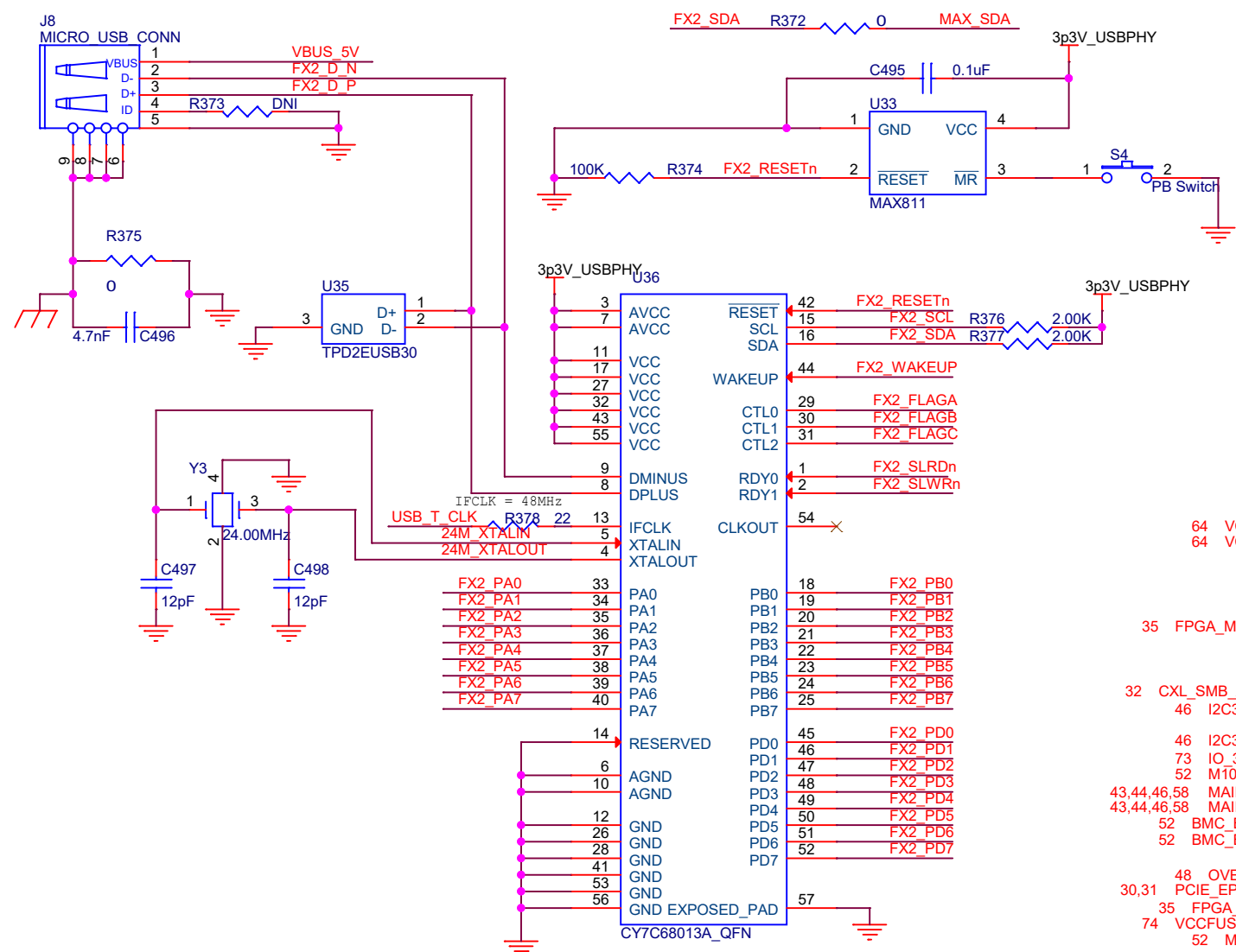
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LEDs And PushButtons

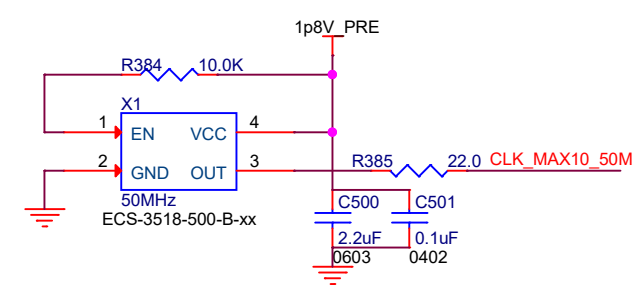
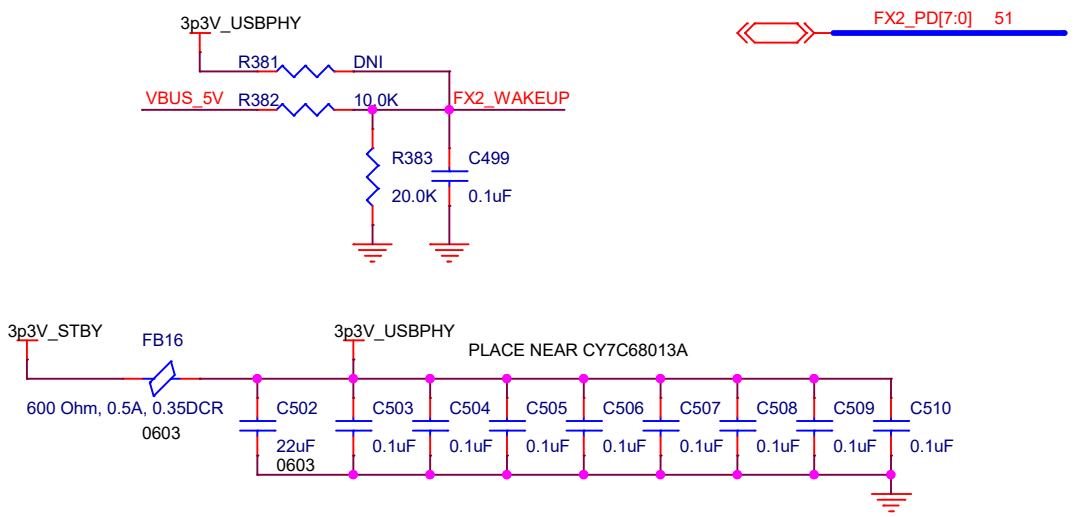
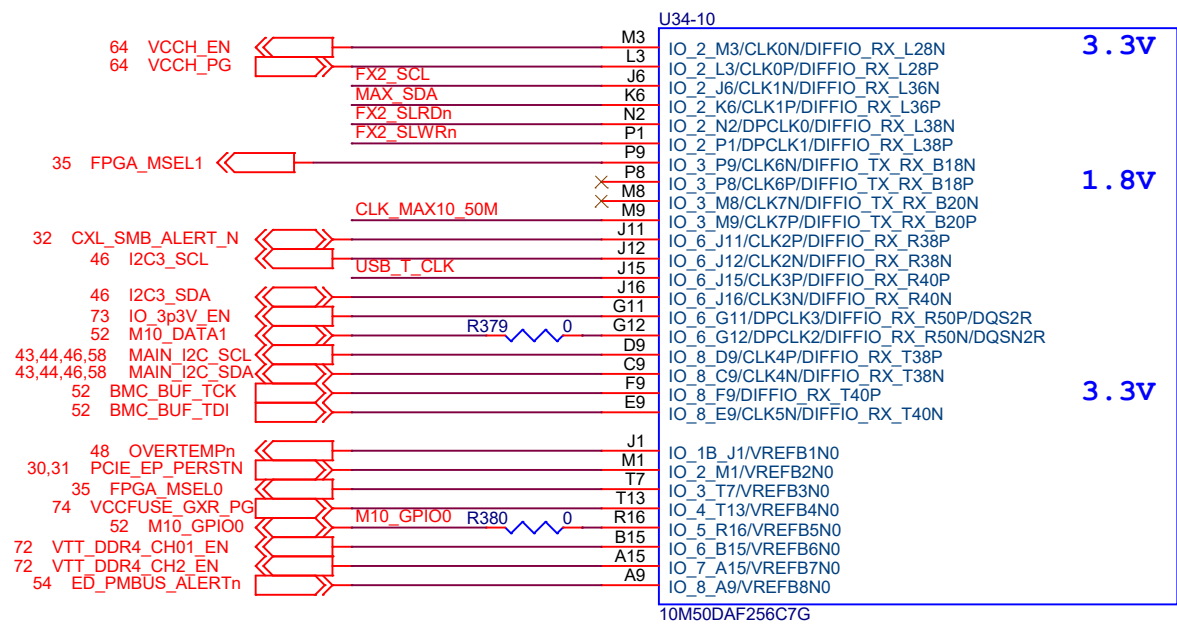


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UBII-MAX10 1

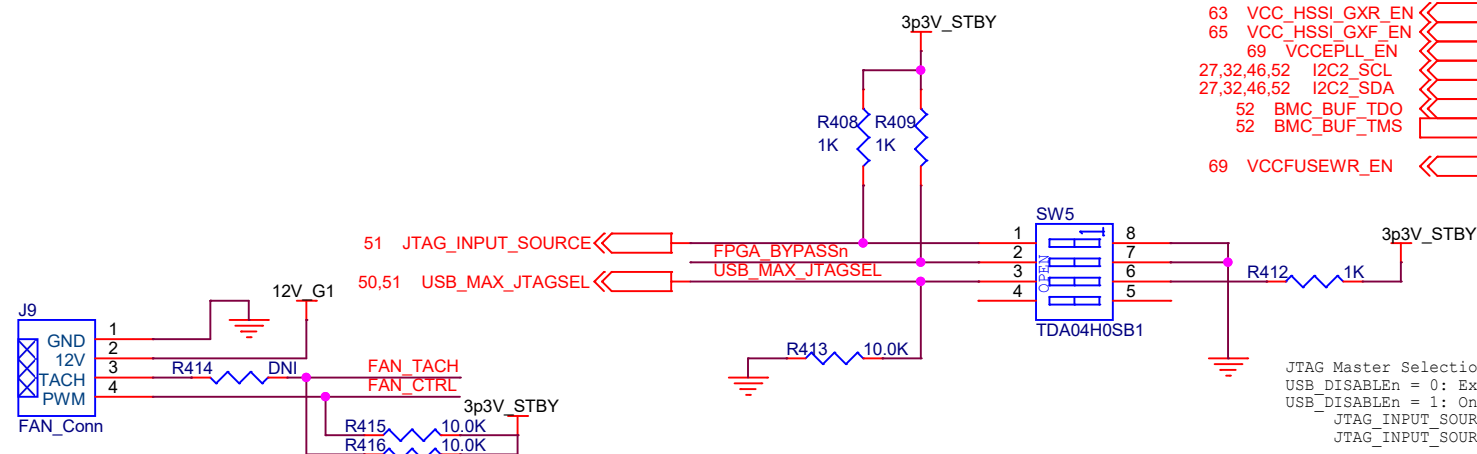
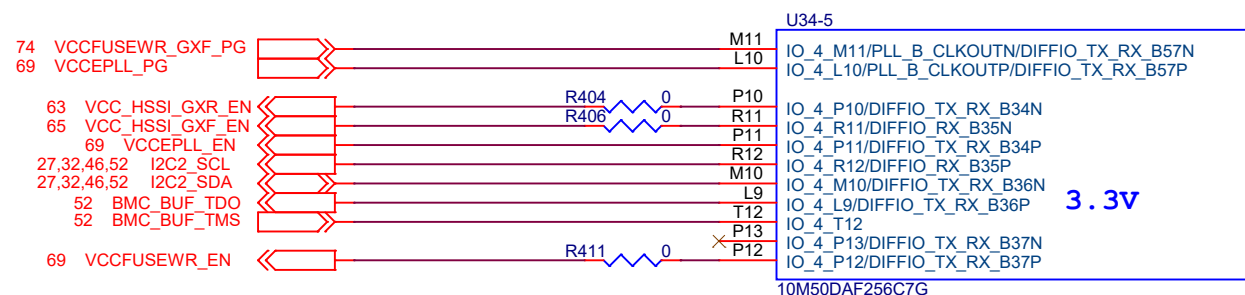
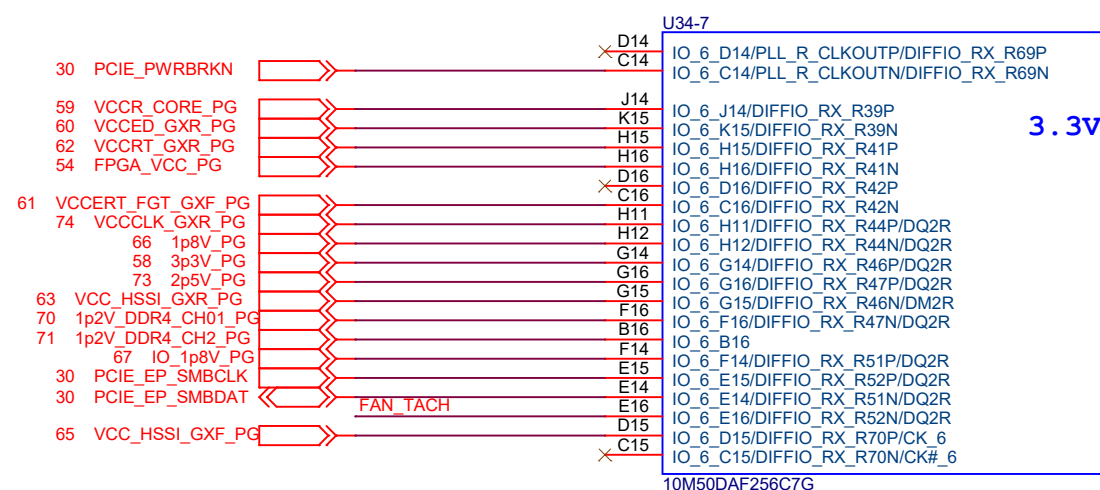
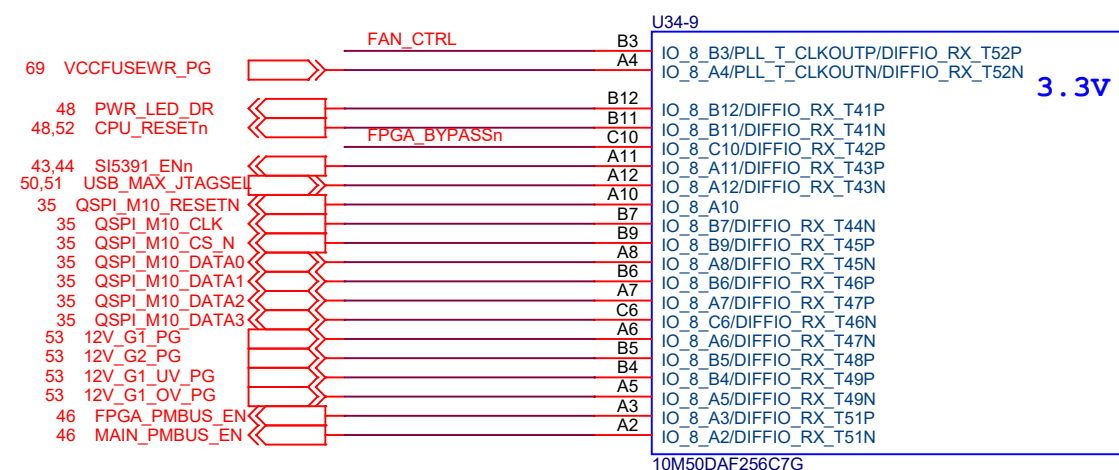
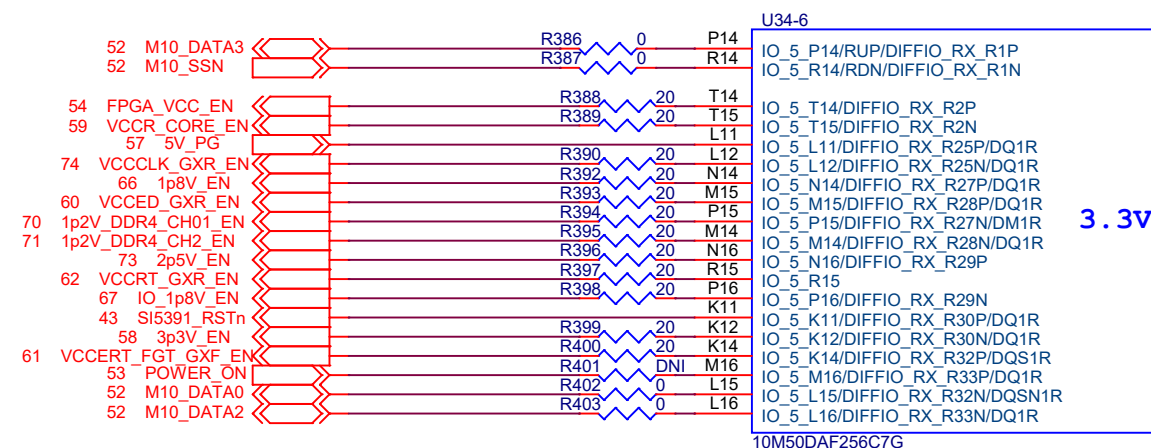
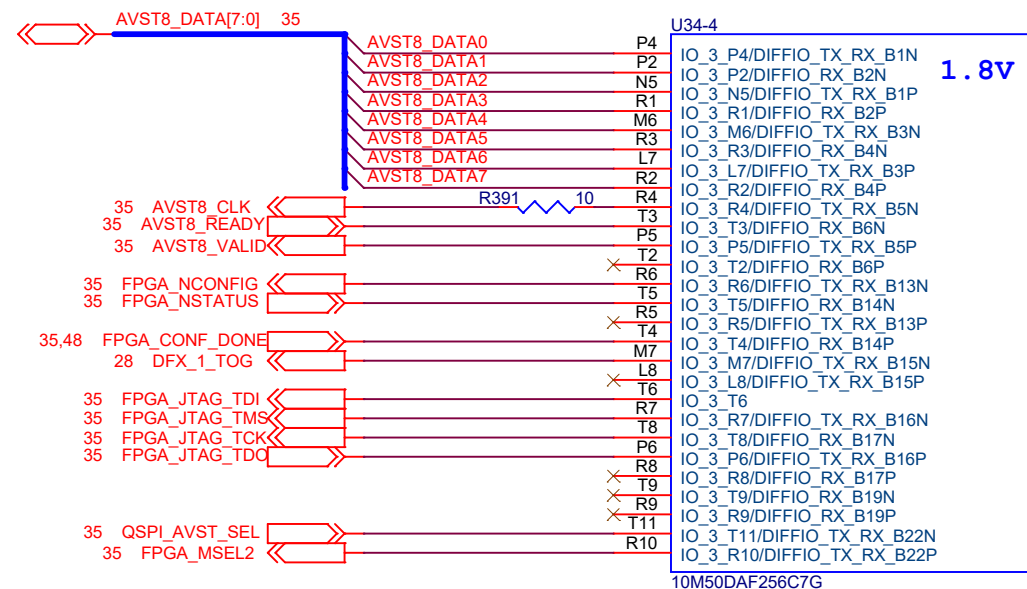


FX2 PA0	F5	IO_1A_F5/ADC1IN1/DIFFIO_RX_L1N
FX2 PA1	C4	IO_1A_C4/ADC2IN1/DIFFIO_RX_L2N
FX2 PA2	F4	IO_1A_F4/ADC1IN2/DIFFIO_RX_L1P
FX2 PA3	C3	IO_1A_C3/ADC2IN2/DIFFIO_RX_L2P
FX2 PA4	H5	IO_1A_H5/ADC1IN3/DIFFIO_RX_L3N
FX2 PA5	E3	IO_1A_E3/ADC2IN3/DIFFIO_RX_L4N
FX2 PA6	G5	IO_1A_G5/ADC1IN4/DIFFIO_RX_L3P
FX2 PA7	F2	IO_1A_F2/ADC2IN4/DIFFIO_RX_L4P
FX2 PB0	G2	IO_1A_G2/ADC1IN5/DIFFIO_RX_L5N
FX2 PB1	C2	IO_1A_C2/ADC2IN5/DIFFIO_RX_L6N
FX2 PB2	F1	IO_1A_F1/ADC1IN6/DIFFIO_RX_L5P
FX2 PB3	B2	IO_1A_B2/ADC2IN6/DIFFIO_RX_L6P
FX2 PB4	E1	IO_1A_E1/ADC1IN7/DIFFIO_RX_L7N
FX2 PB5	B1	IO_1A_B1/ADC2IN7/DIFFIO_RX_L8N
FX2 PB6	D1	IO_1A_D1/ADC1IN8/DIFFIO_RX_L7P
FX2 PB7	C1	IO_1A_C1/ADC2IN8/DIFFIO_RX_L8P
FX2 FLAGA	J5	IO_1B_J5/DIFFIO_RX_L20N
FX2 FLAGB	H6	IO_1B_H6/DIFFIO_RX_L20P
FX2 FLAGC	J3	IO_1B_J3/DIFFIO_RX_L22N
FX2 RESETn	J2	IO_1B_J2/DIFFIO_RX_L22P



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AVST_READY must be double
registered inside MAX10 for
synchronization to AVST_CLK



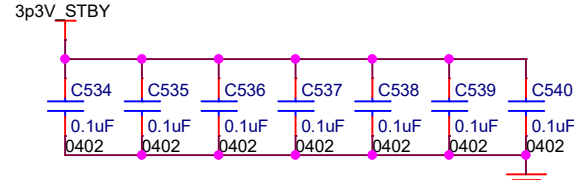
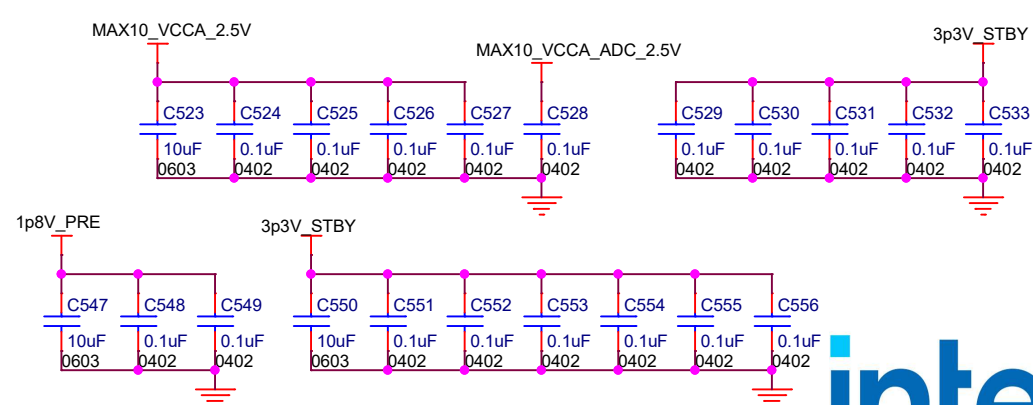
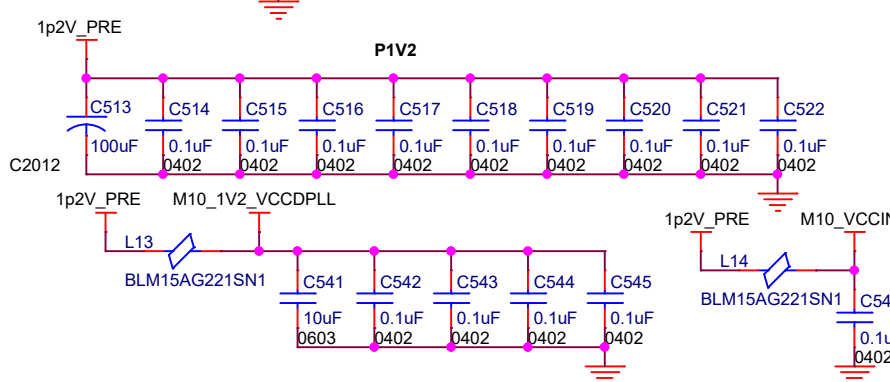
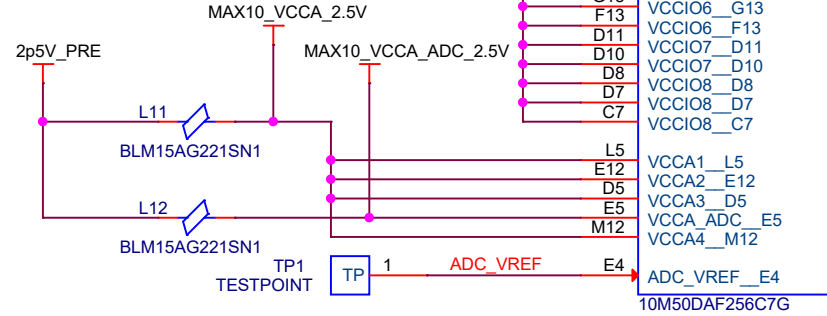
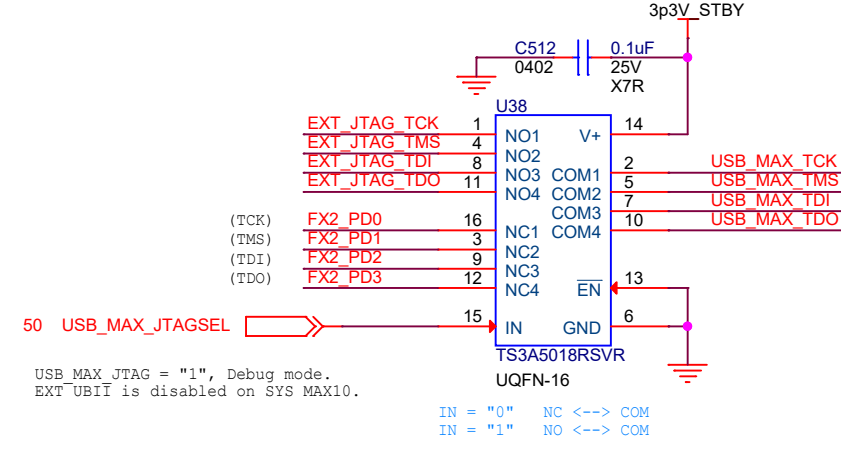
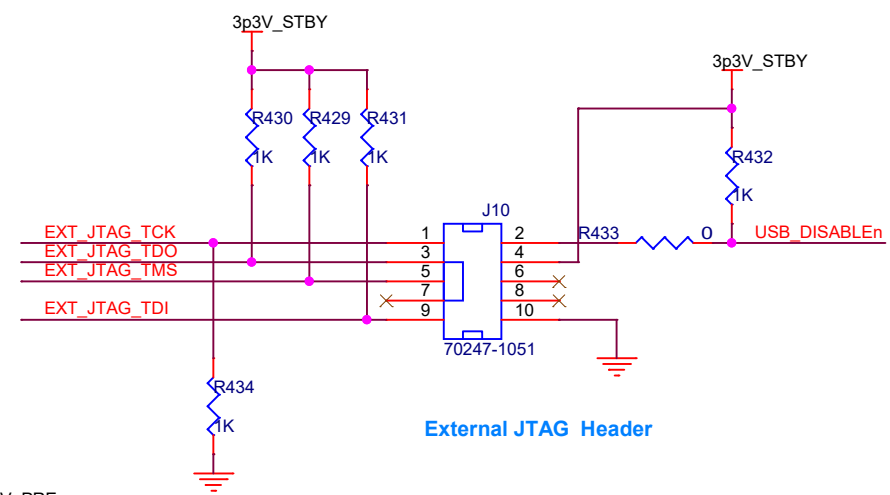
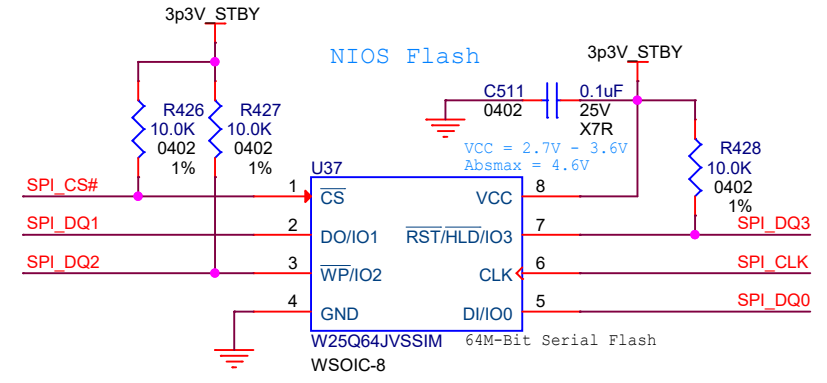
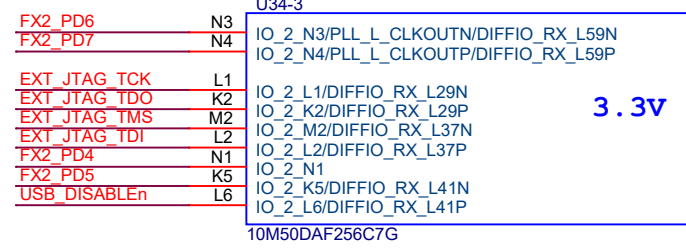
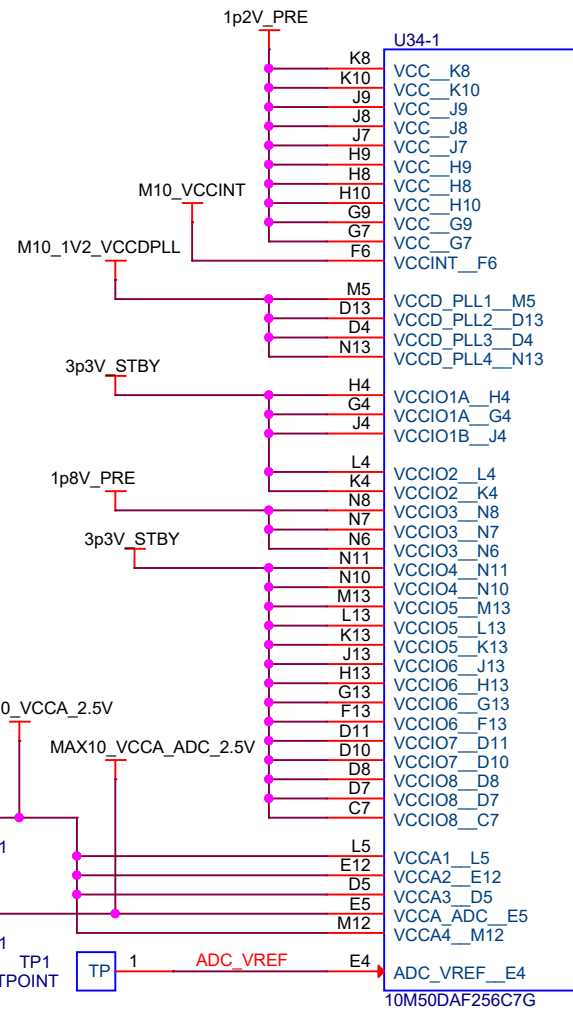
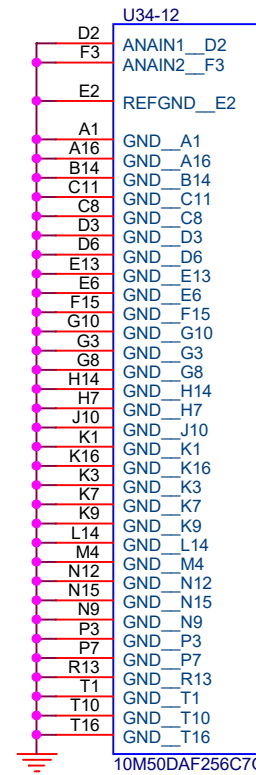
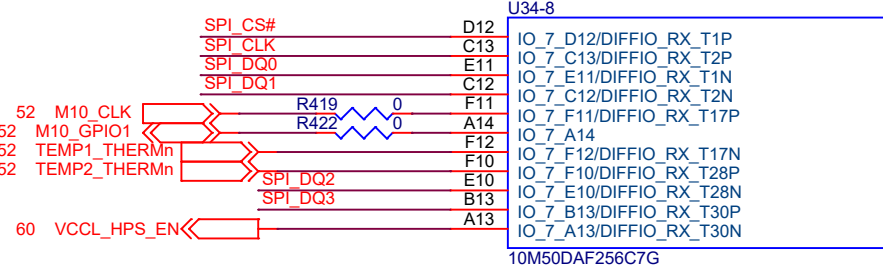
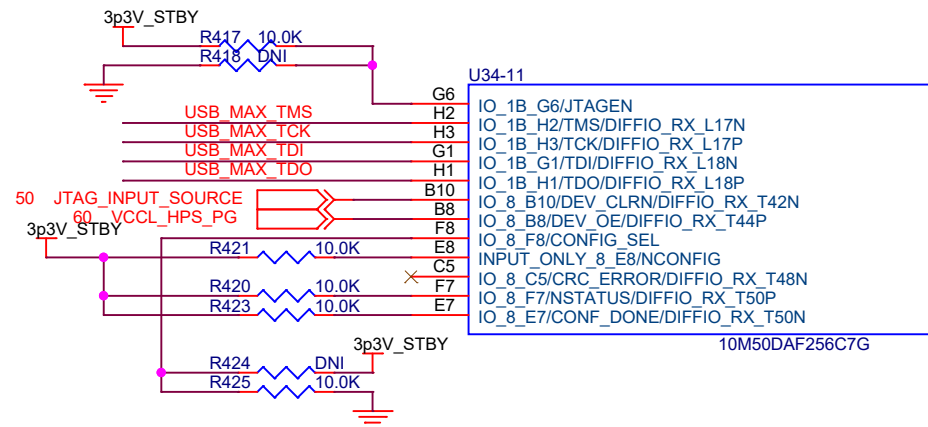
JTAG Master Selection:
USB_DISABLEn = 0: External JTAG
USB_DISABLEn = 1: On-Board UBII/PCIE EP Edge
JTAG_INPUT_SOURCE = 0: PCIE EP edge
JTAG_INPUT_SOURCE = 1: On-Board UBII

JTAG Chain:
SW4_2 = Low : Bypass
SW4_2 = High: Enable



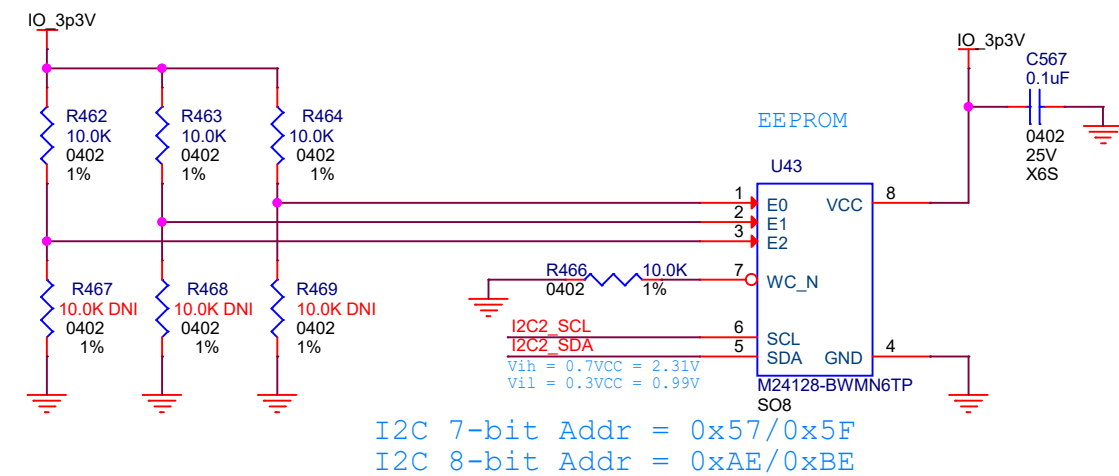
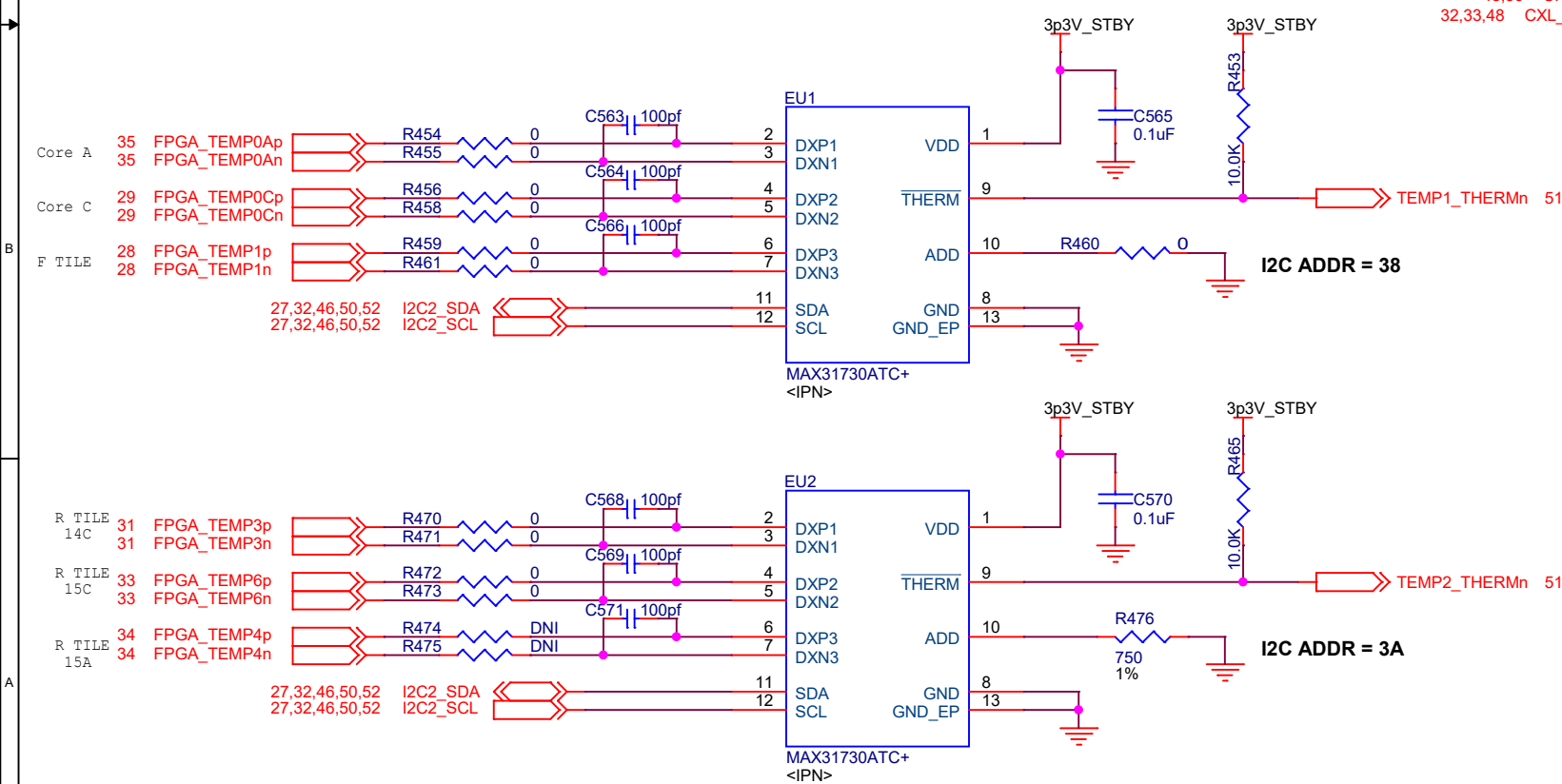
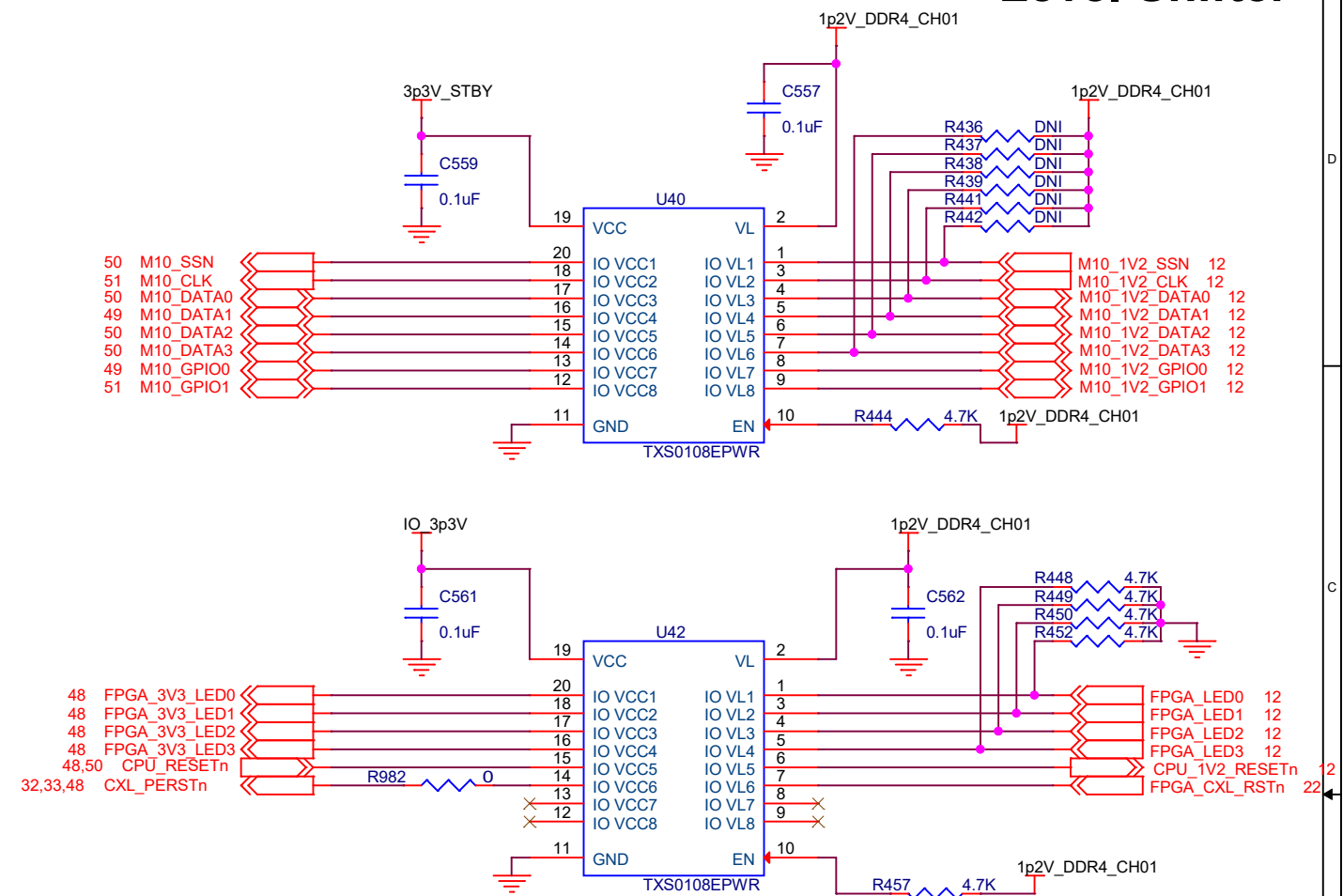
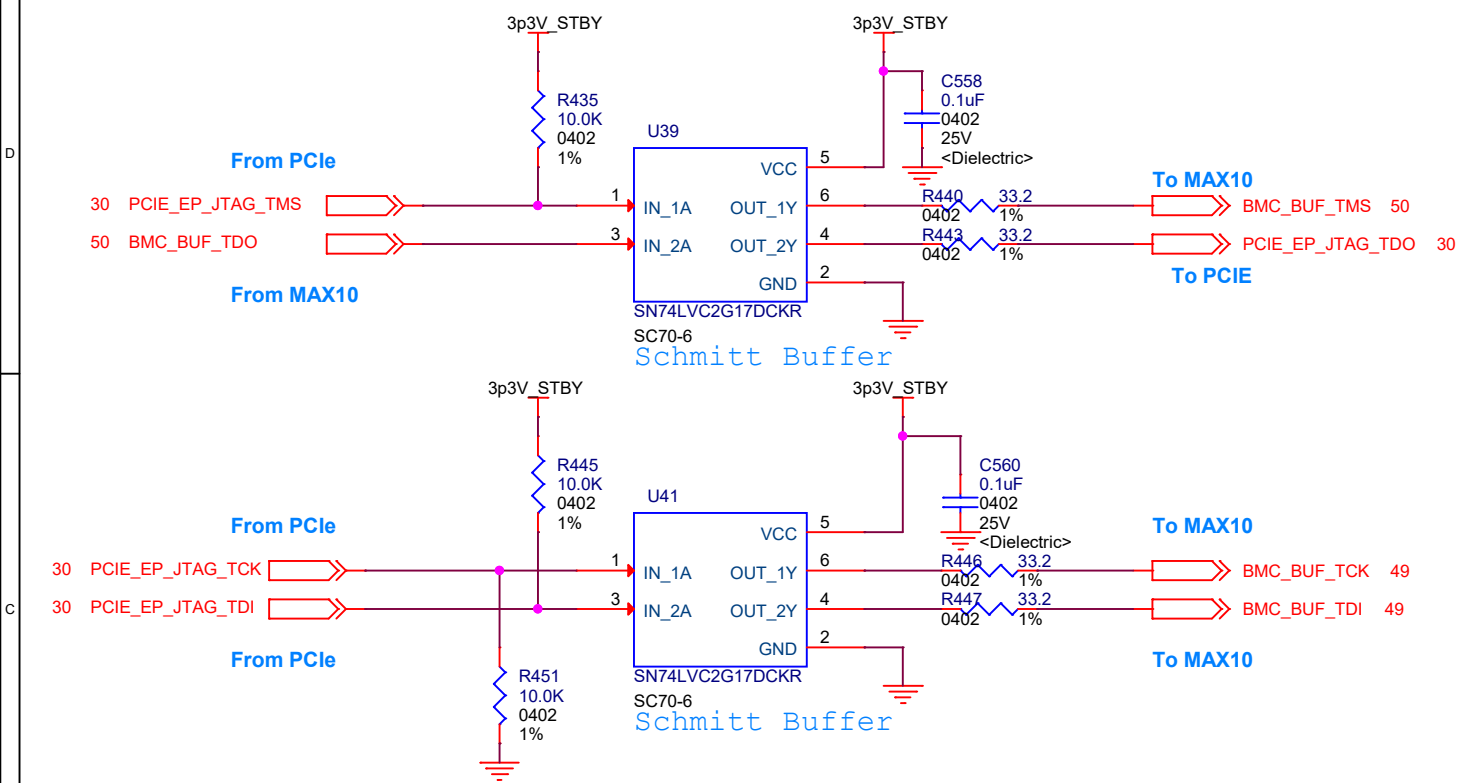
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MAX 10 PWR Manager 1



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Level Shifter



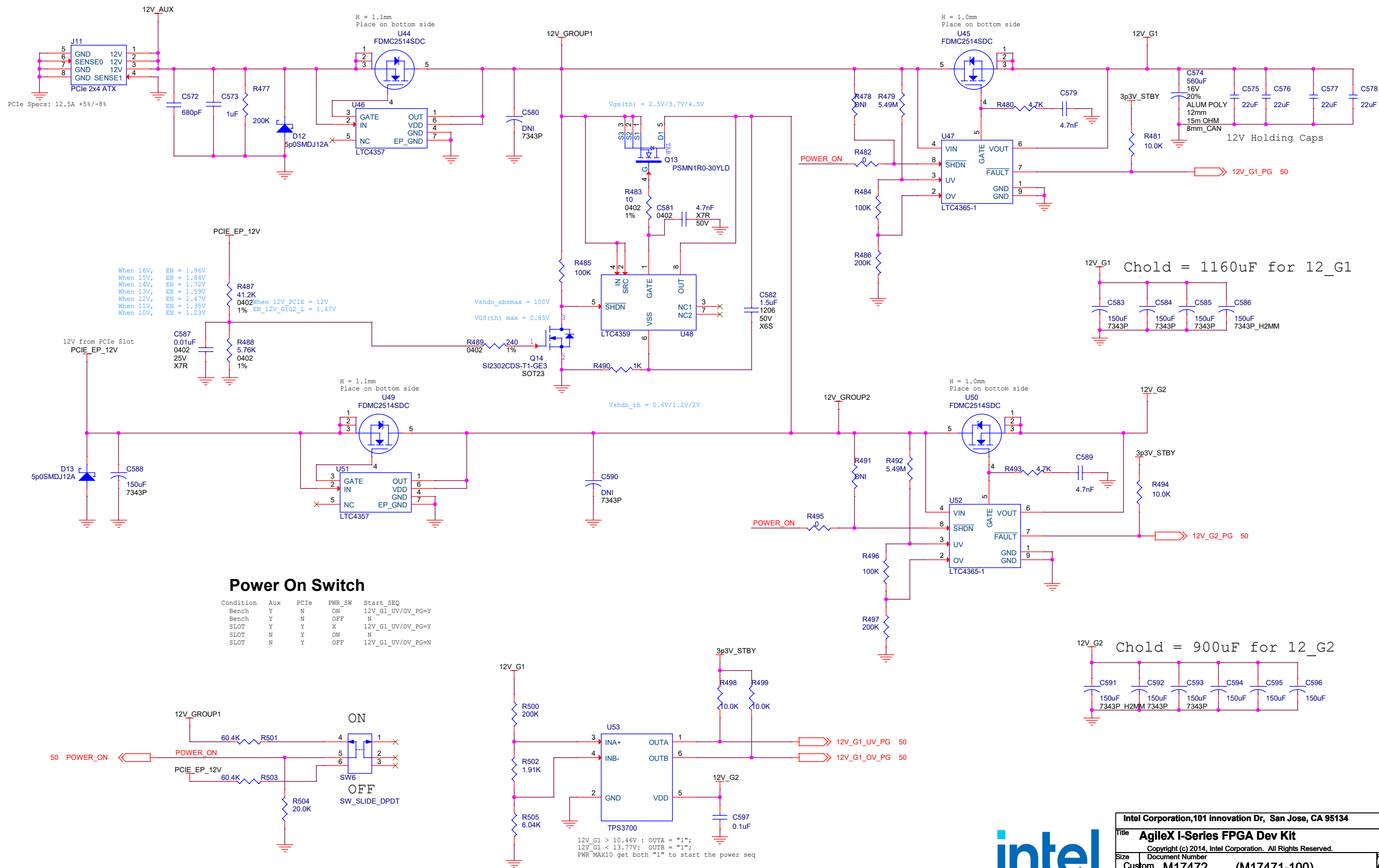
```
I2C 7-bit Addr = 0x57/0x5F
I2C 8-bit Addr = 0xAE/0xBE
```

Board Temp Sensor



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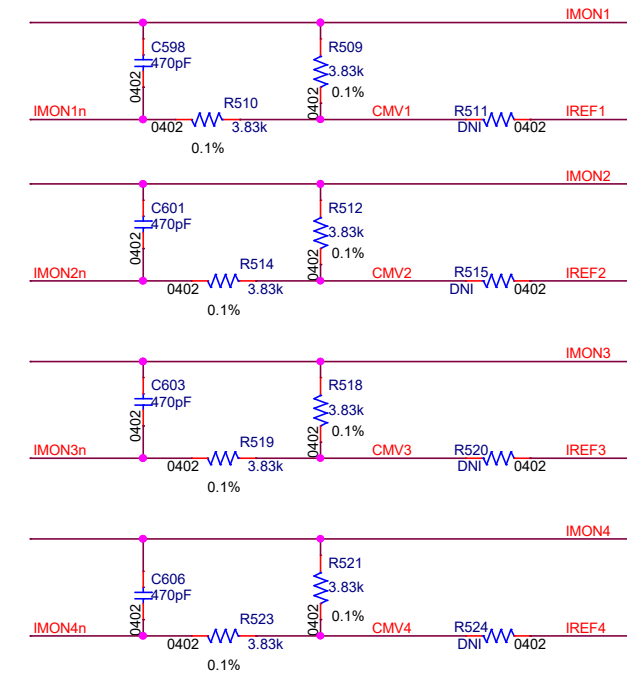
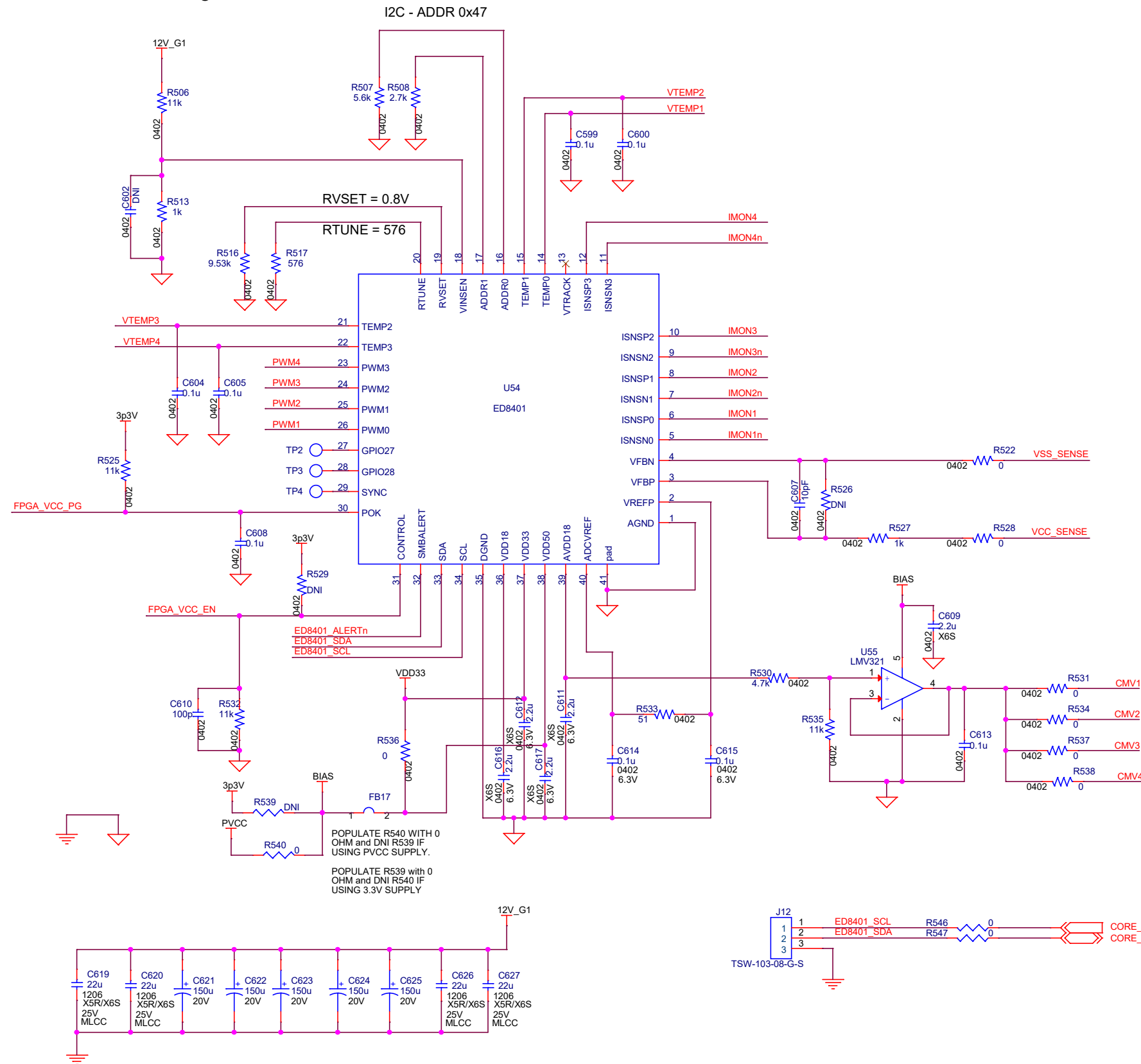
Power - Select Power Input



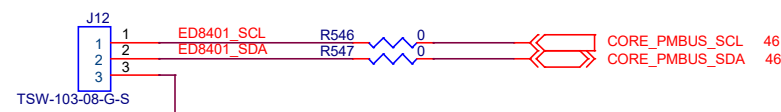
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Default Core Voltage = 0.8V

VCC Core Controller

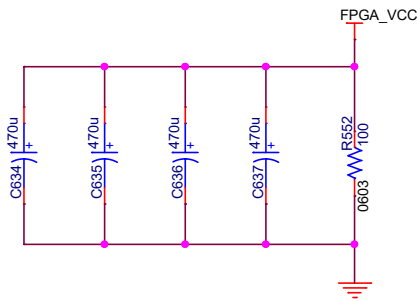
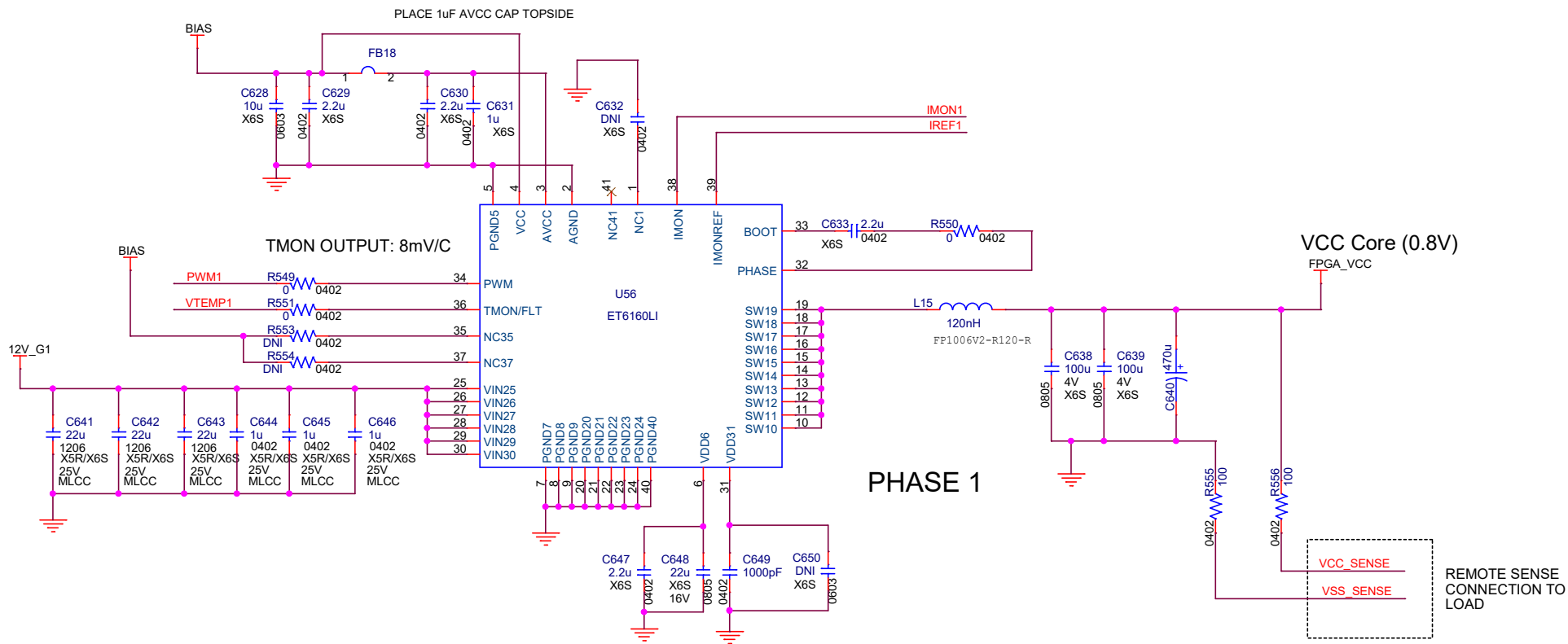


IMON1		IMON1	55
IMON2		IMON2	55
IMON3		IMON3	56
IMON4		IMON4	56
IREF1		IREF1	55
IREF2		IREF2	55
IREF3		IREF3	56
IREF4		IREF4	56
PWM1		PWM1	55
PWM2		PWM2	55
PWM3		PWM3	56
PWM4		PWM4	56
VTEMP1		VTEMP1	55
VTEMP2		VTEMP2	55
VTEMP3		VTEMP3	56
VTEMP4		VTEMP4	56
FPGA_VCC_EN		FPGA_VCC_EN	50
FPGA_VCC_PG		FPGA_VCC_PG	50
VCC_SENSE		VCC_SENSE	37.55
VSS_SENSE		VSS_SENSE	37.55

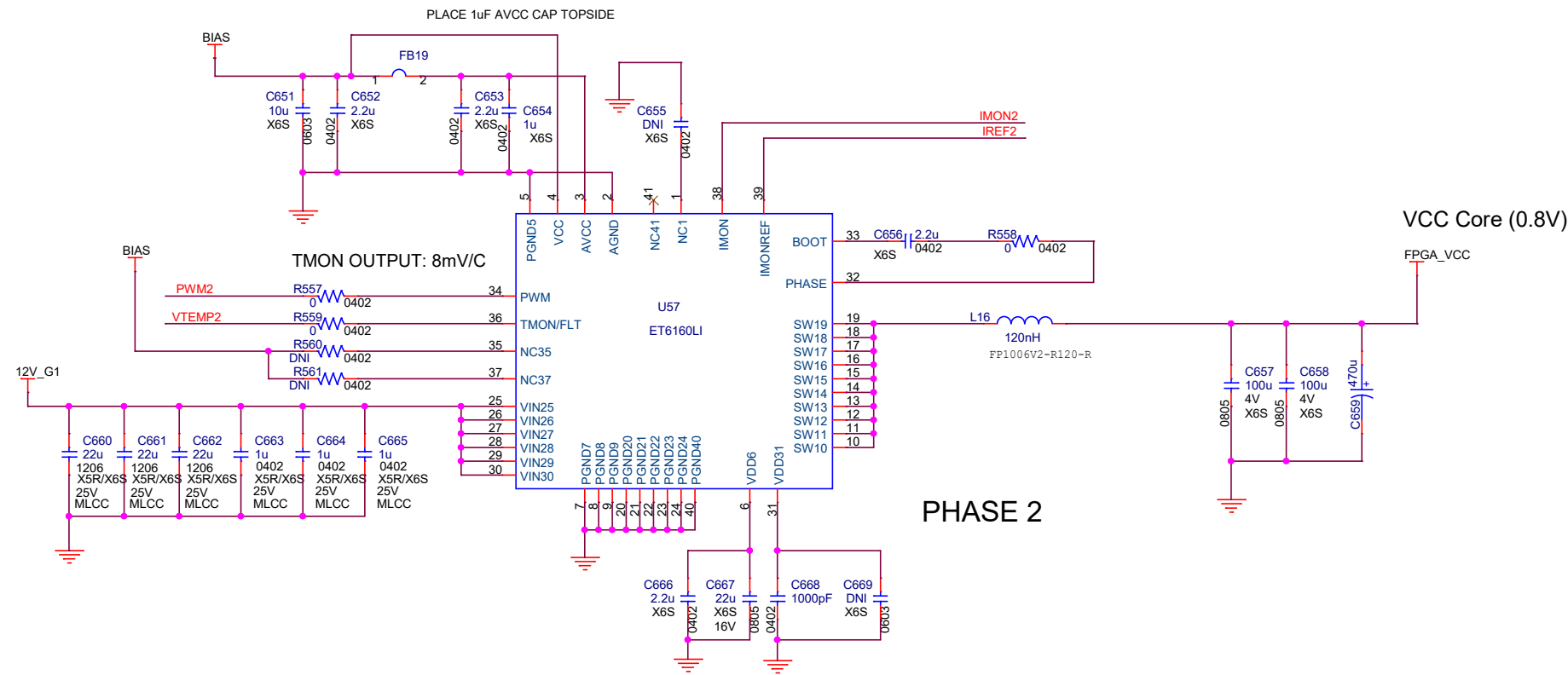


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VCC Core Phase 1 - 2



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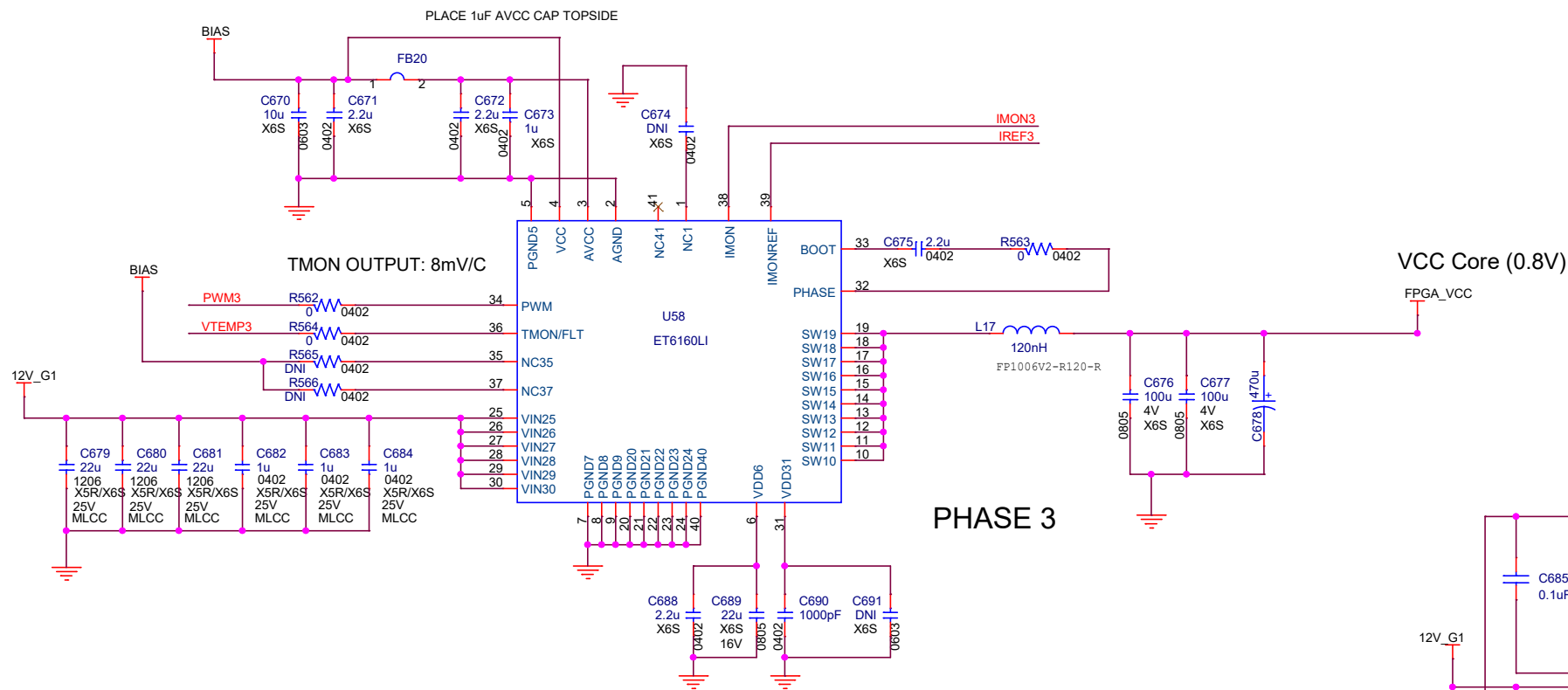


VCC_SENSE	VCC_SENSE	37.54
VSS_SENSE	VSS_SENSE	37.54
IMON1	IMON1	54
IREF1	IREF1	54
PWM1	PWM1	54
VTEMP1	VTEMP1	54
IMON2	IMON2	54
IREF2	IREF2	54
PWM2	PWM2	54
VTEMP2	VTEMP2	54

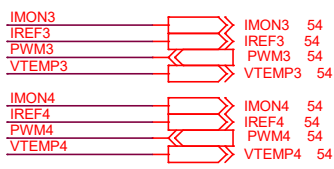
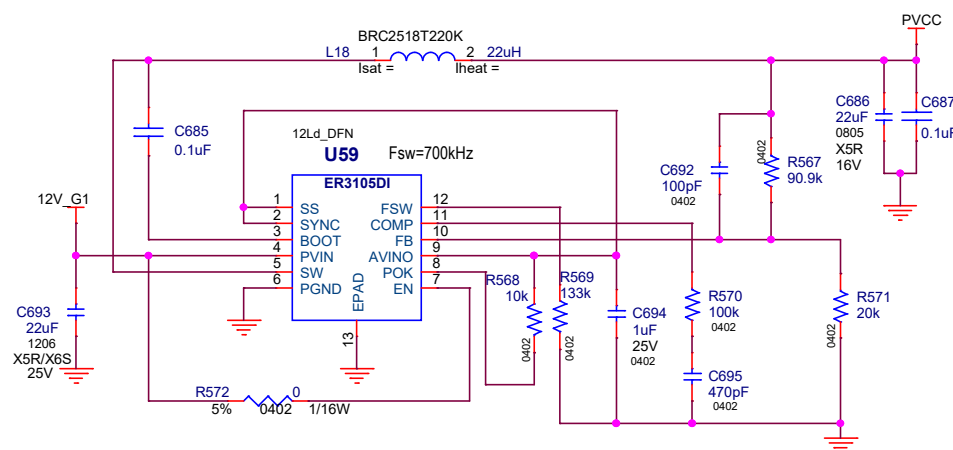
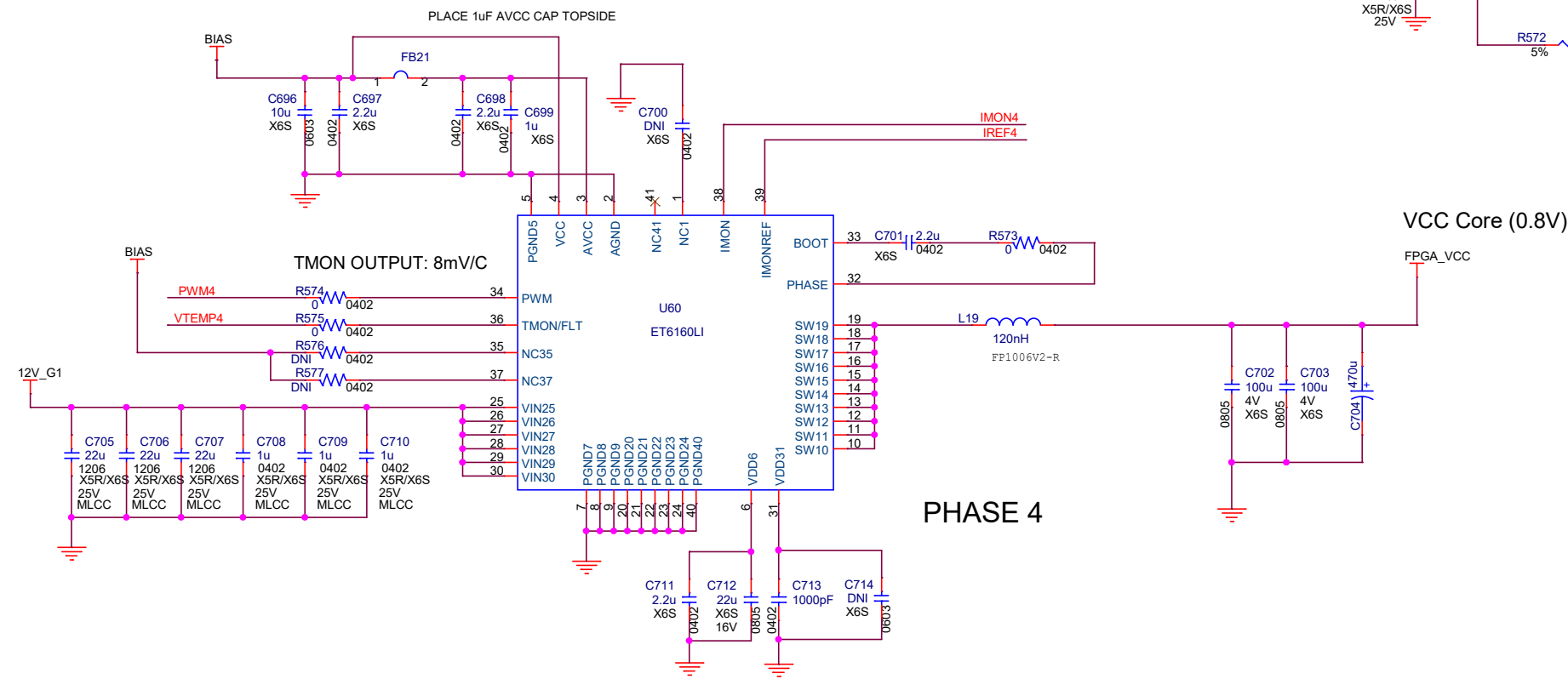


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VCC Core Phase 3 - 4

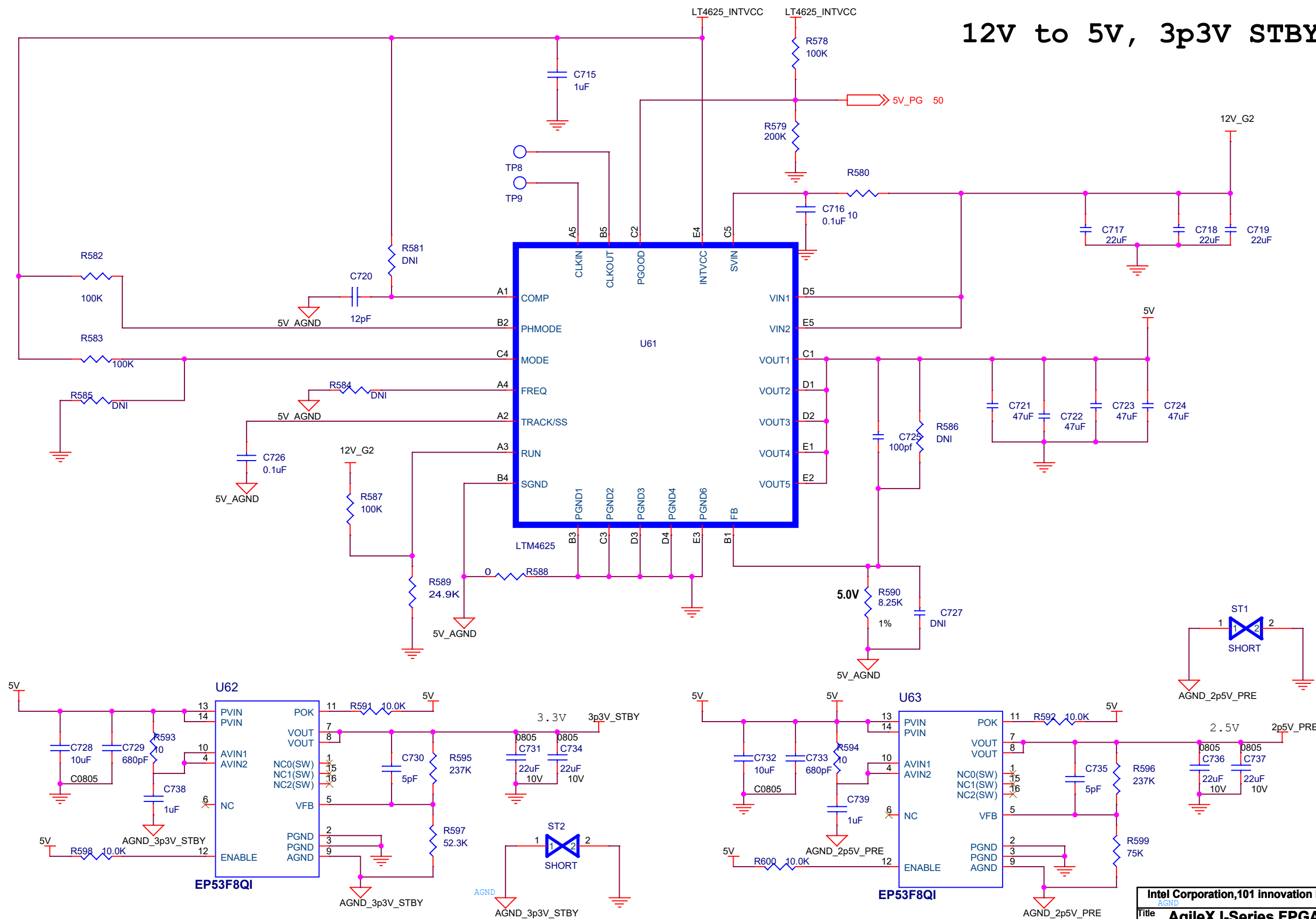


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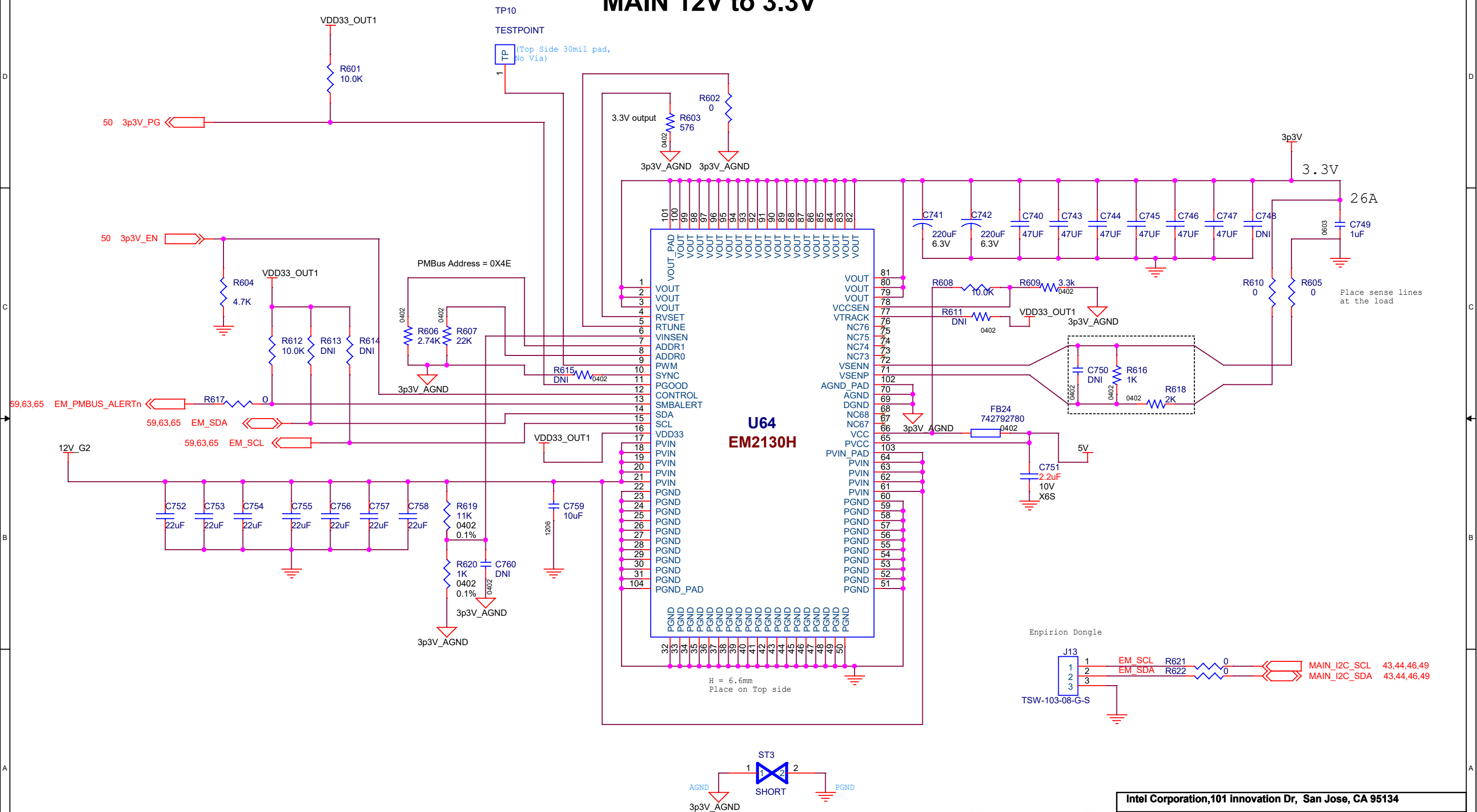
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12V to 5V, 3p3V STBY, 2p5V_PRE



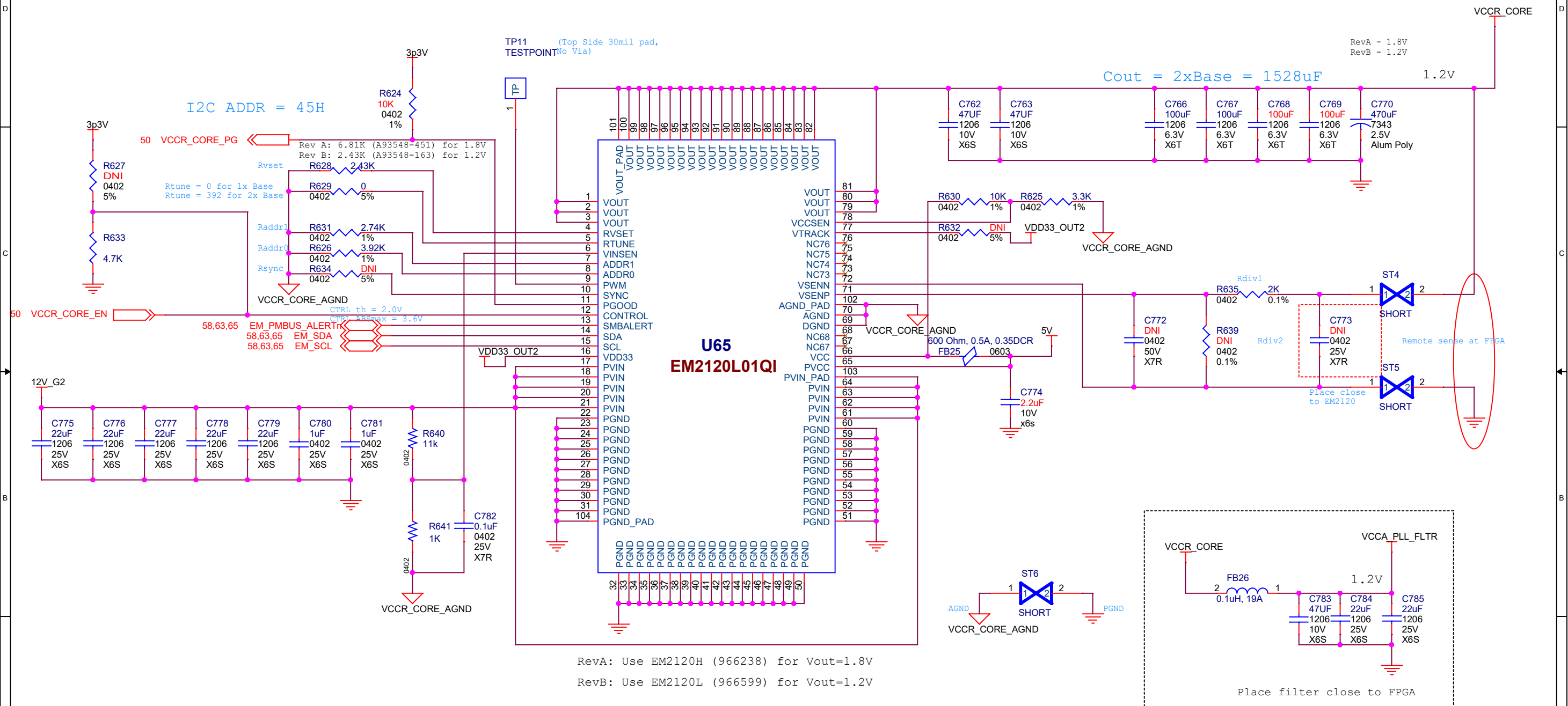
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MAIN 12V to 3.3V



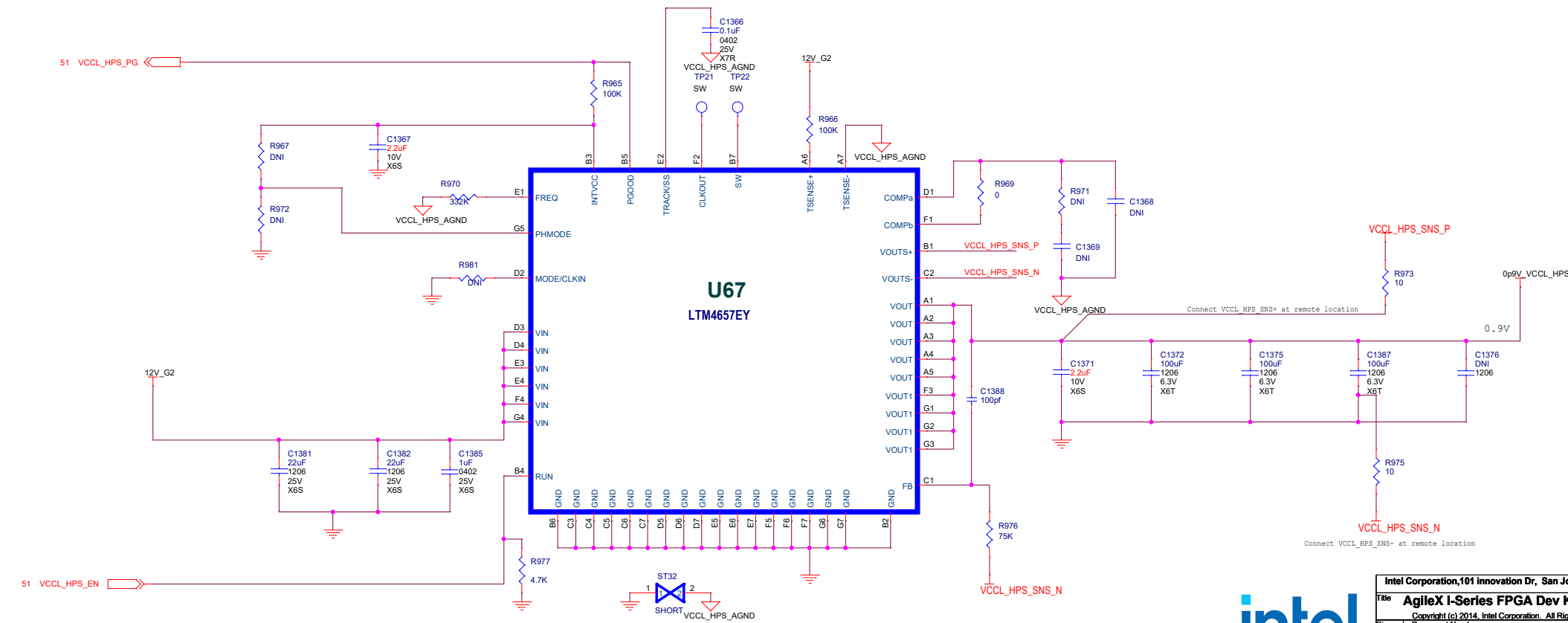
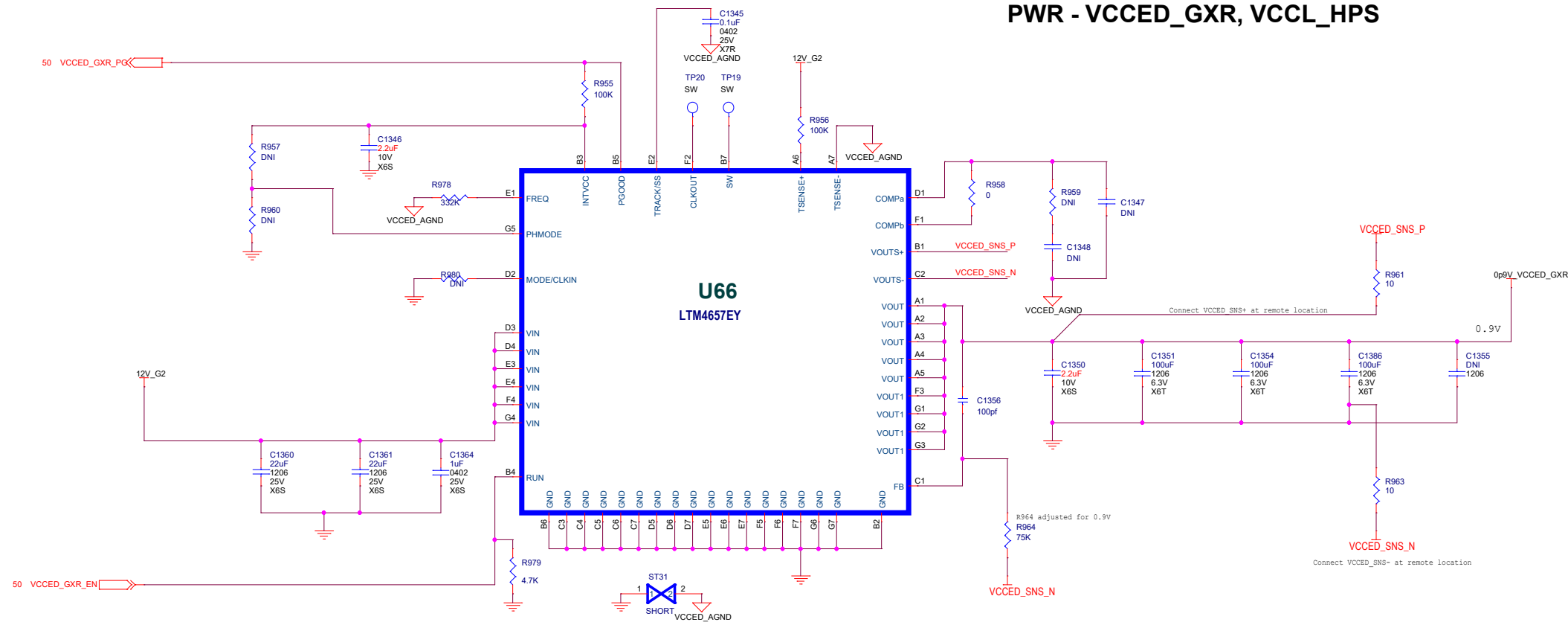
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PWR - VCCR_CORE, VCCA_PLL



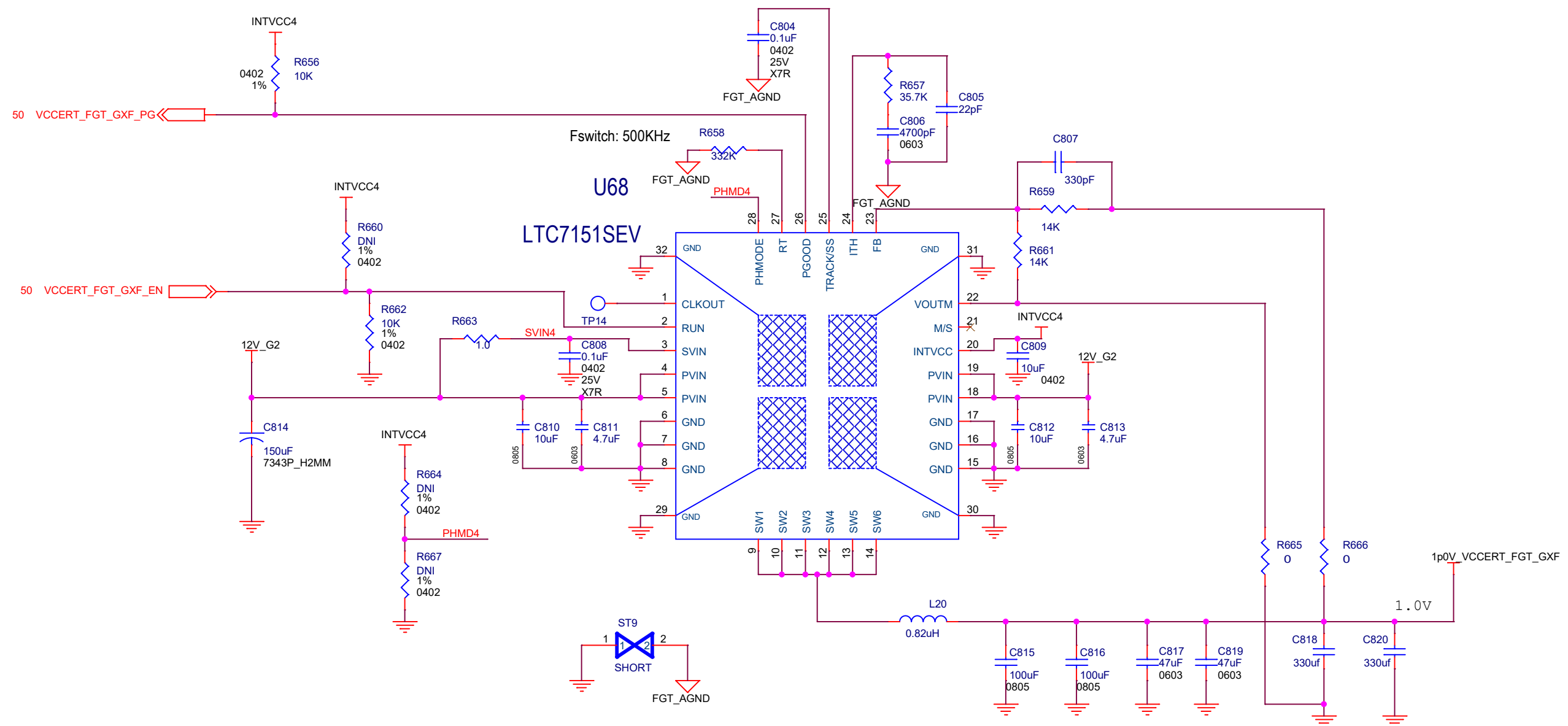
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PWR - VCCED_GXR, VCCL_HPS



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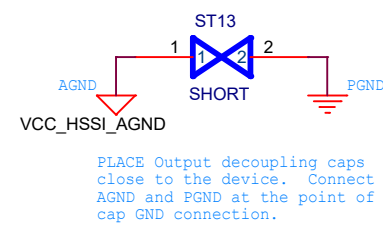
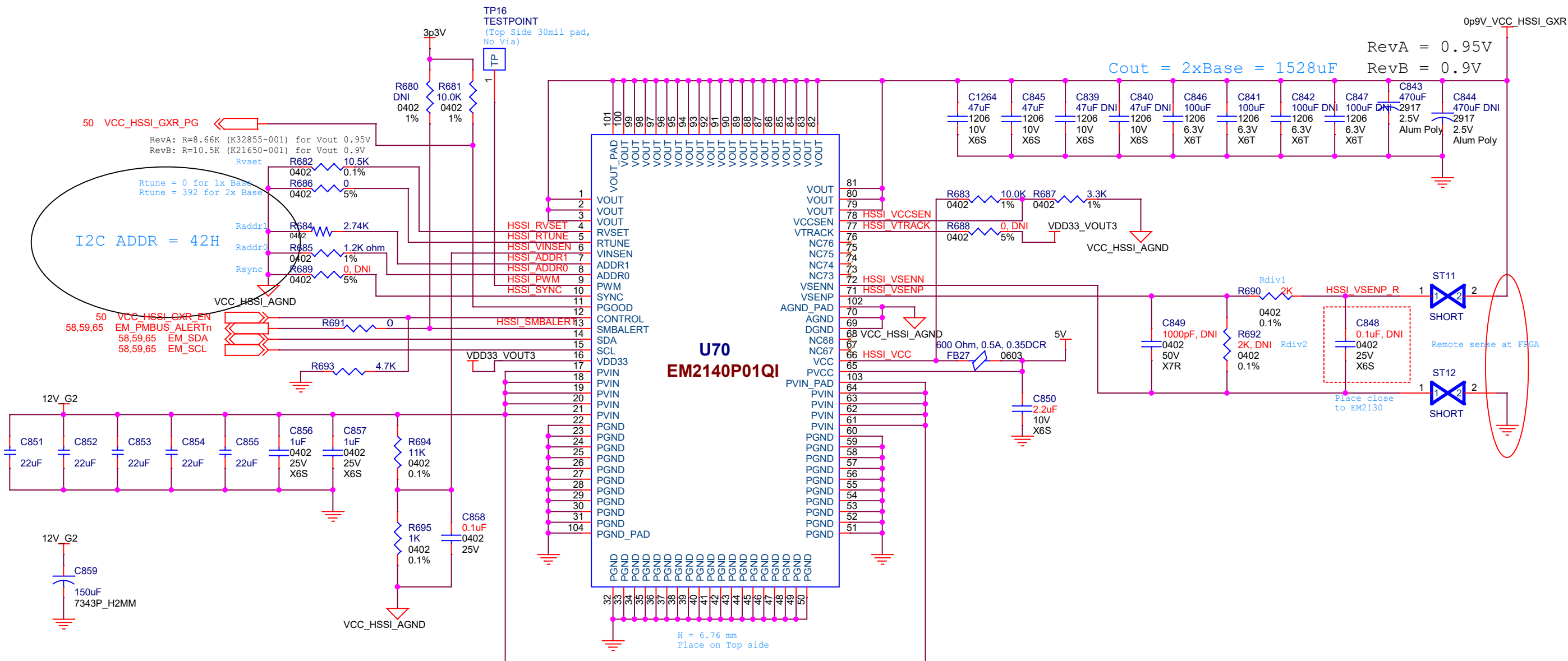
PWR - VCCERT_FGT_GXF



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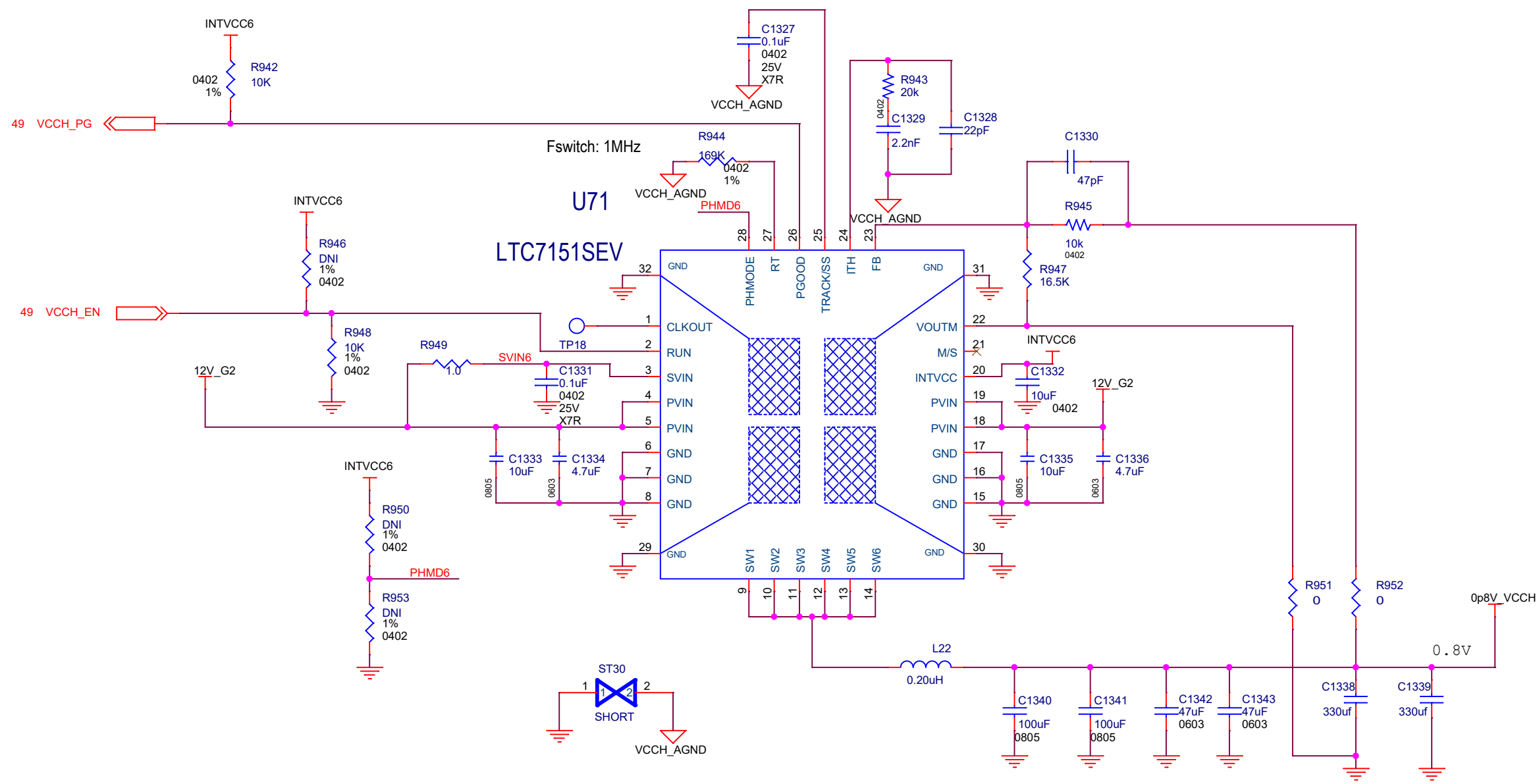


PWR - VCC_HSSI_GXR



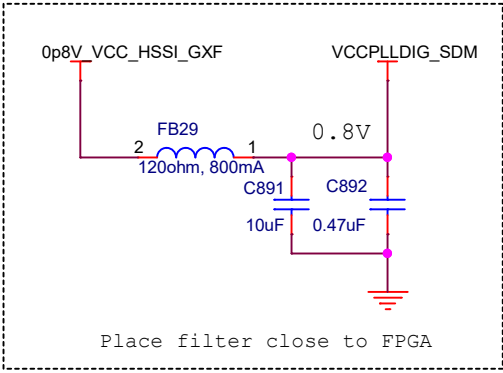
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Power - VCCH



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Speed

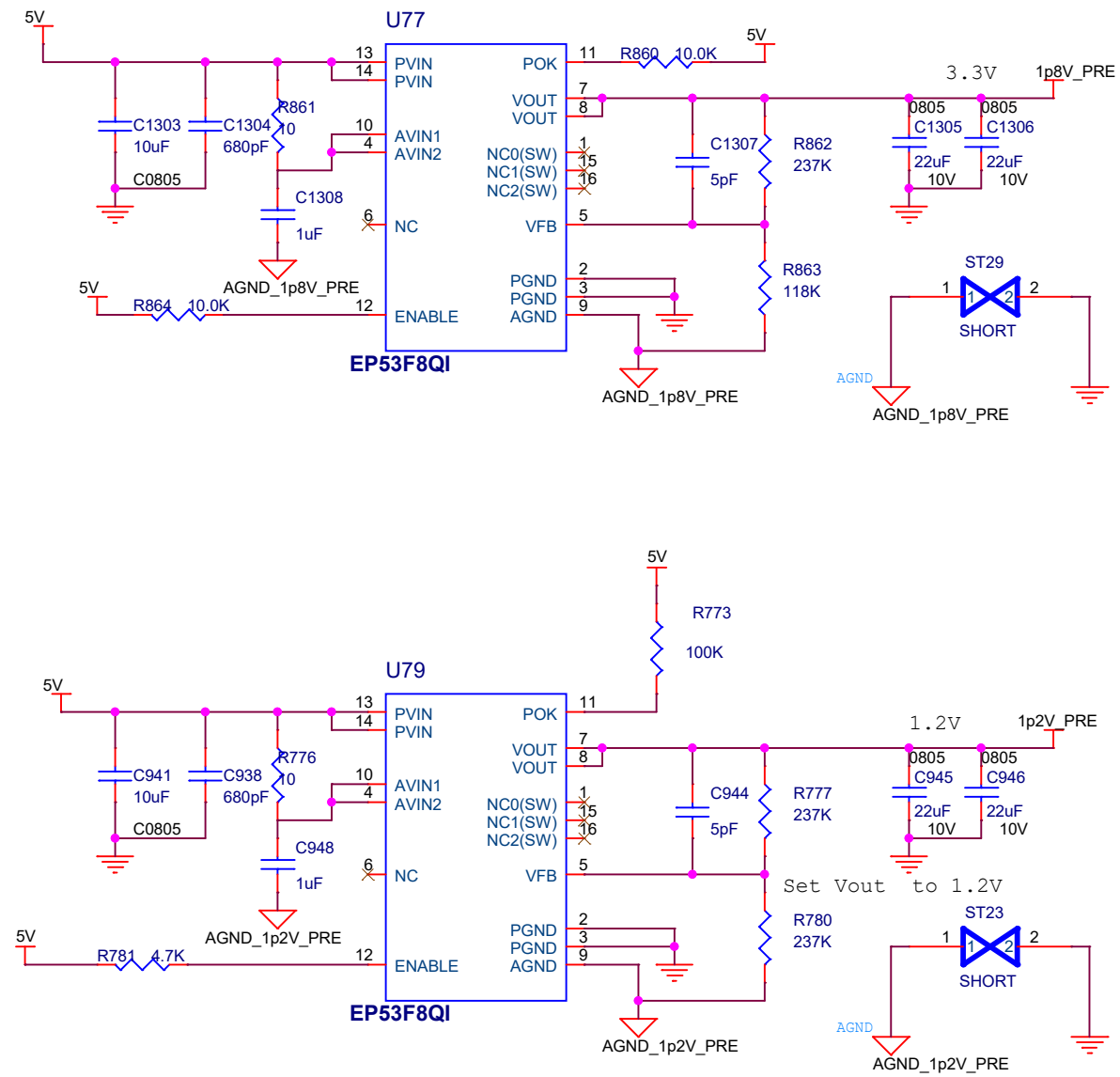


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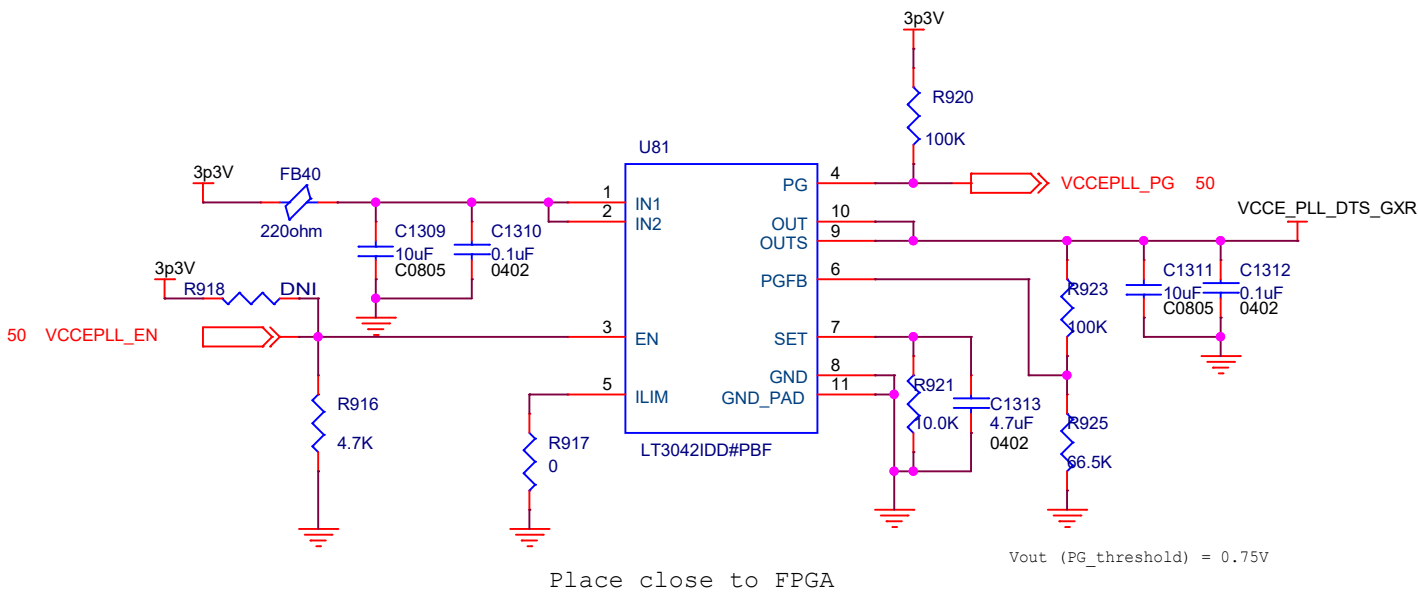


PWR - 1p8V_PRE,1p2V_PRE



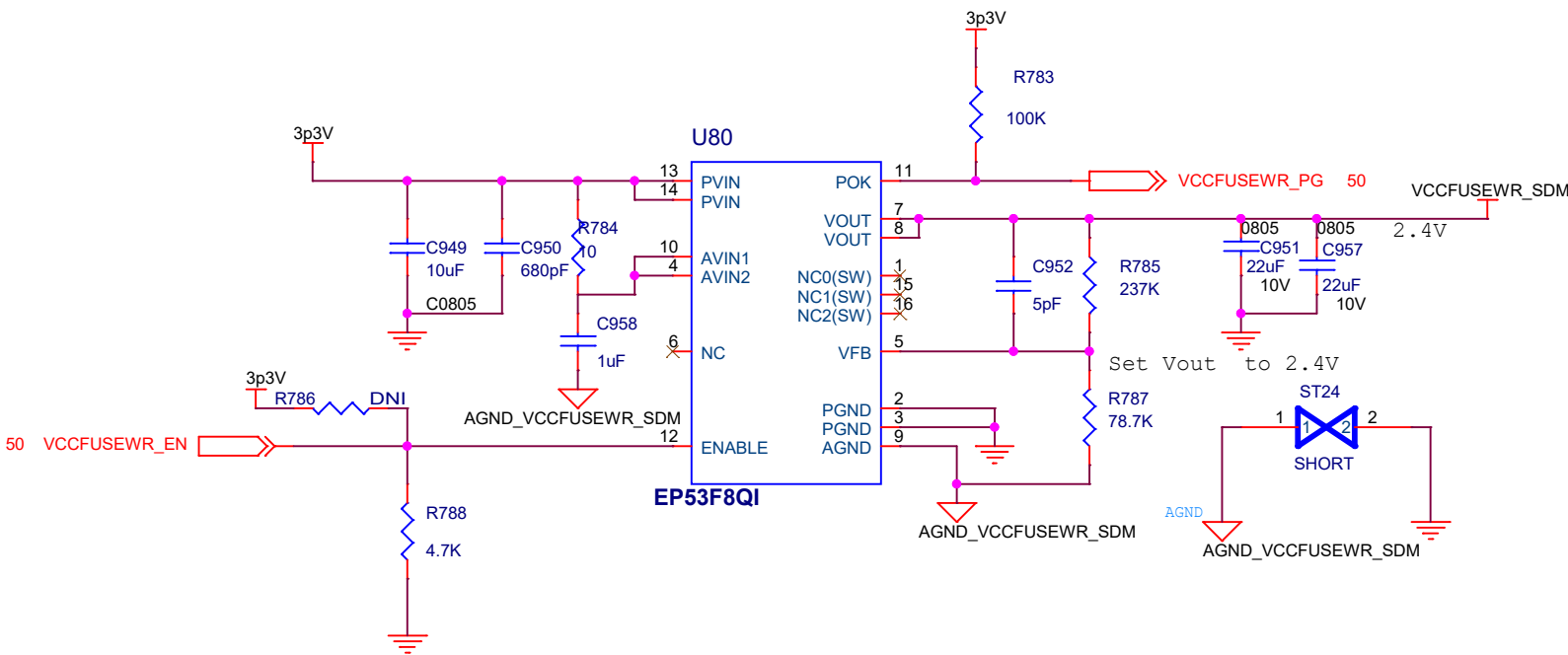
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PWR - VCCFUSEWR_SDM



PWR - VCCE_PLL_GXR, VCCE_DTS_GXR

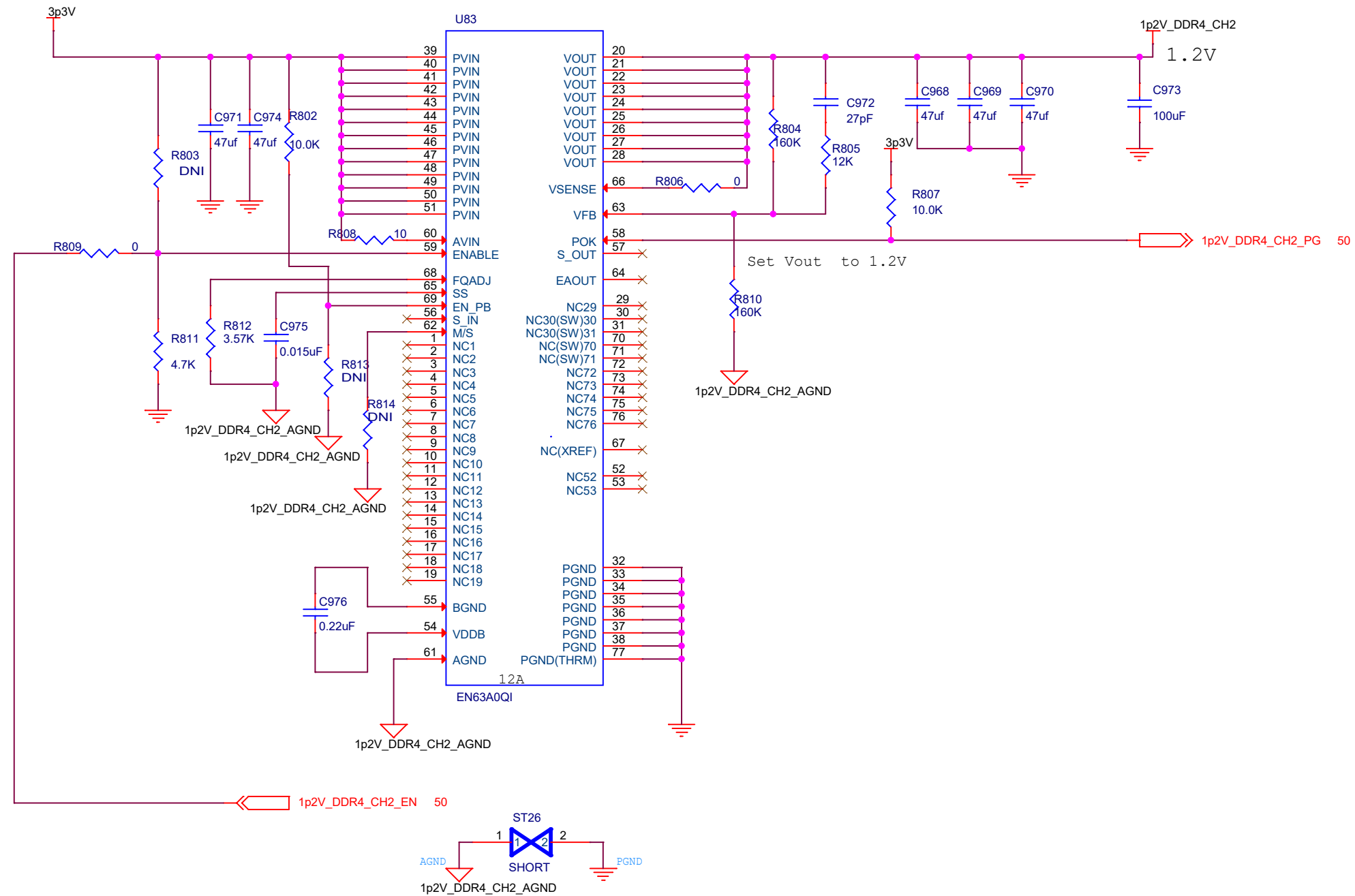
PWR - VCCFUSEWR_SDM



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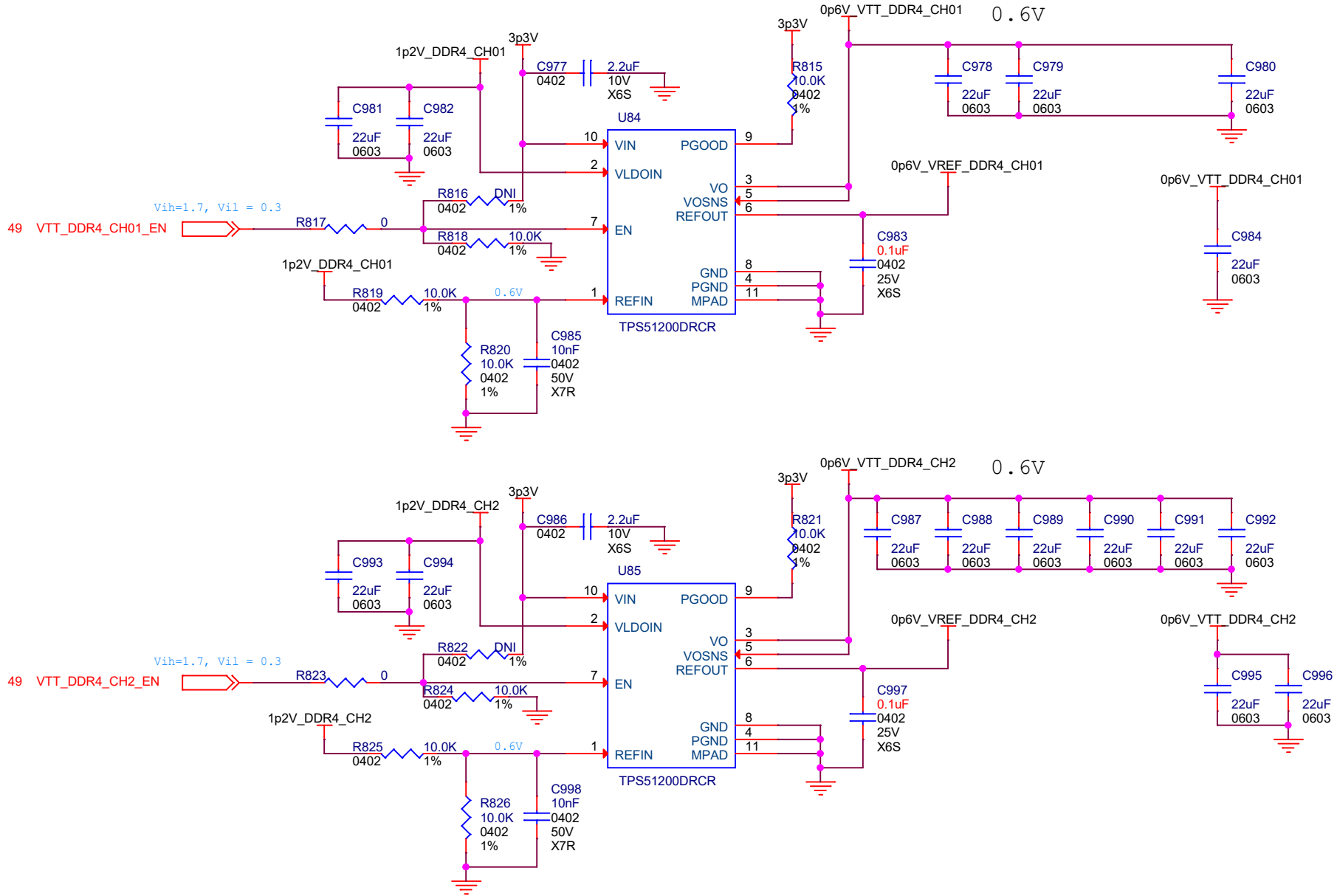


PWR - 1p2V_DDR4_CH2, VCCIO_PIO_3A/3B/3C/3D



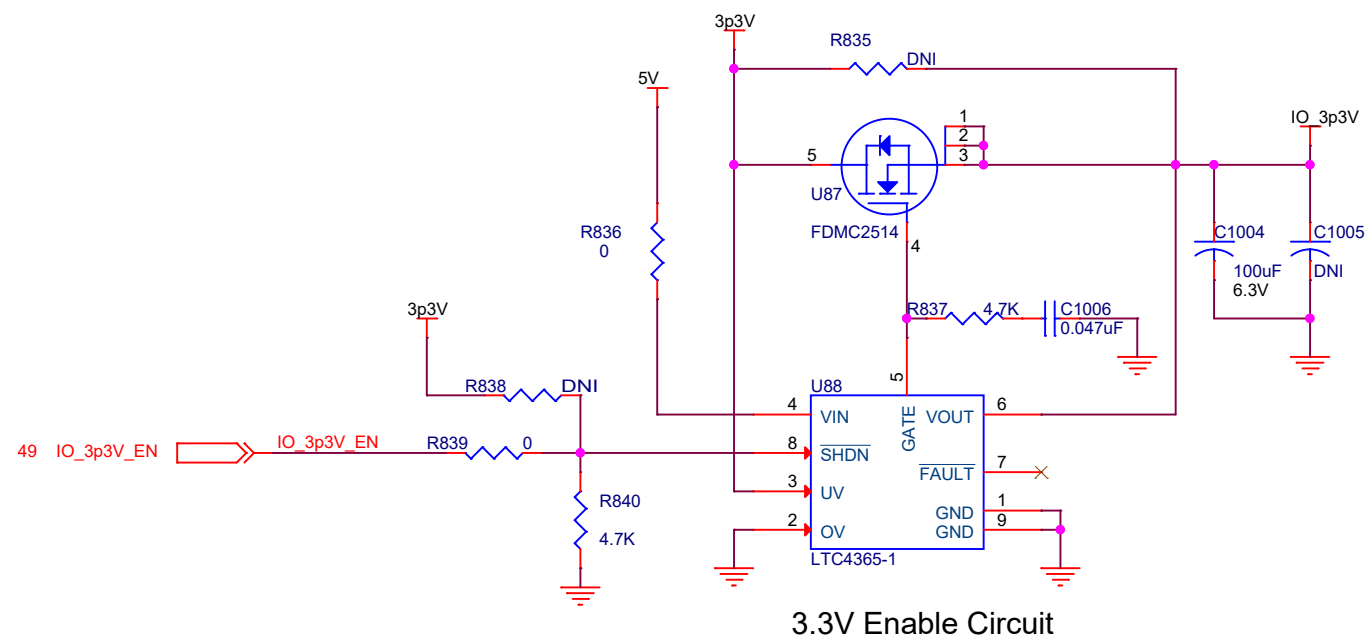
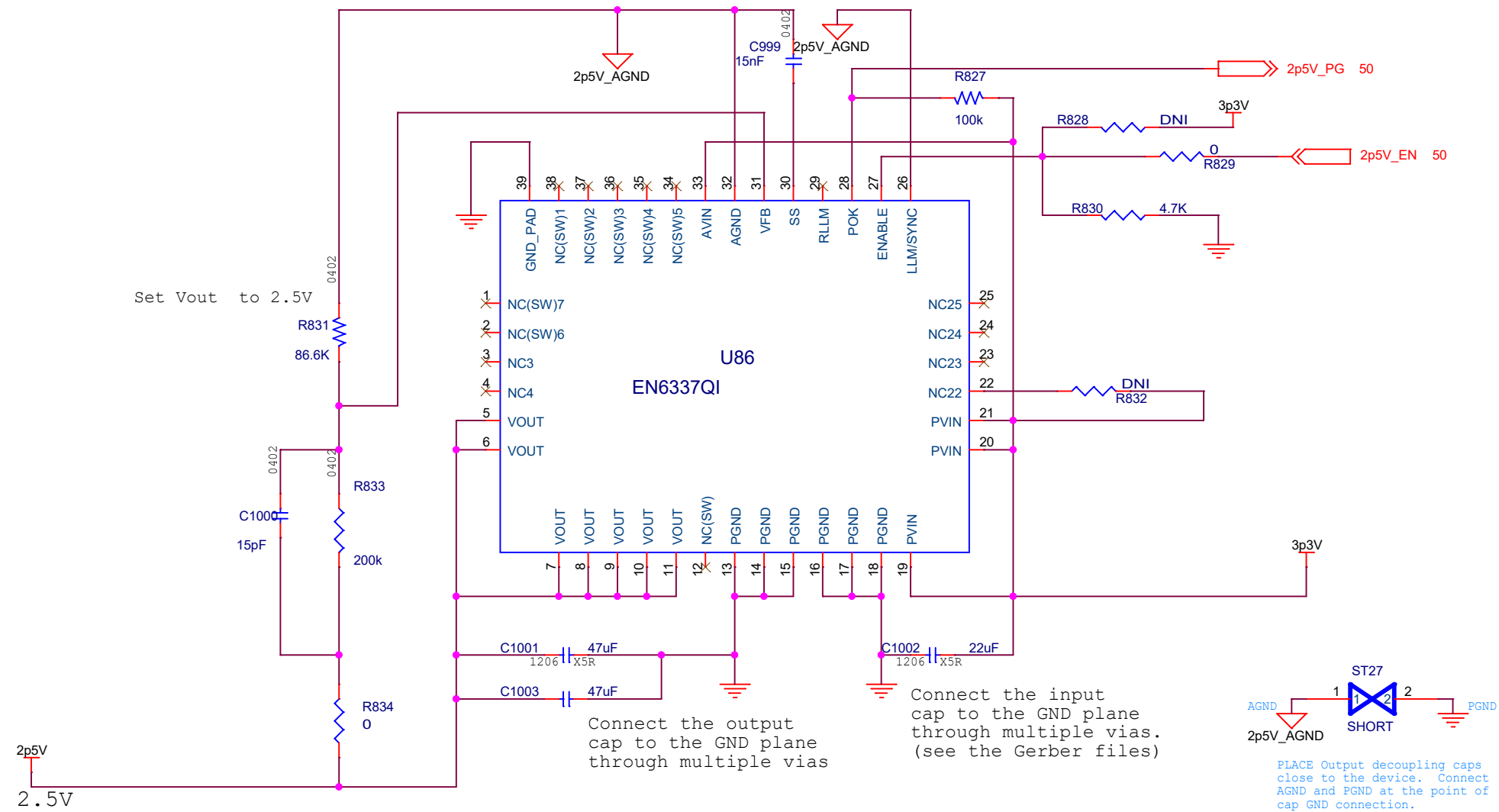
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PWR - DDR4 VREF/VT



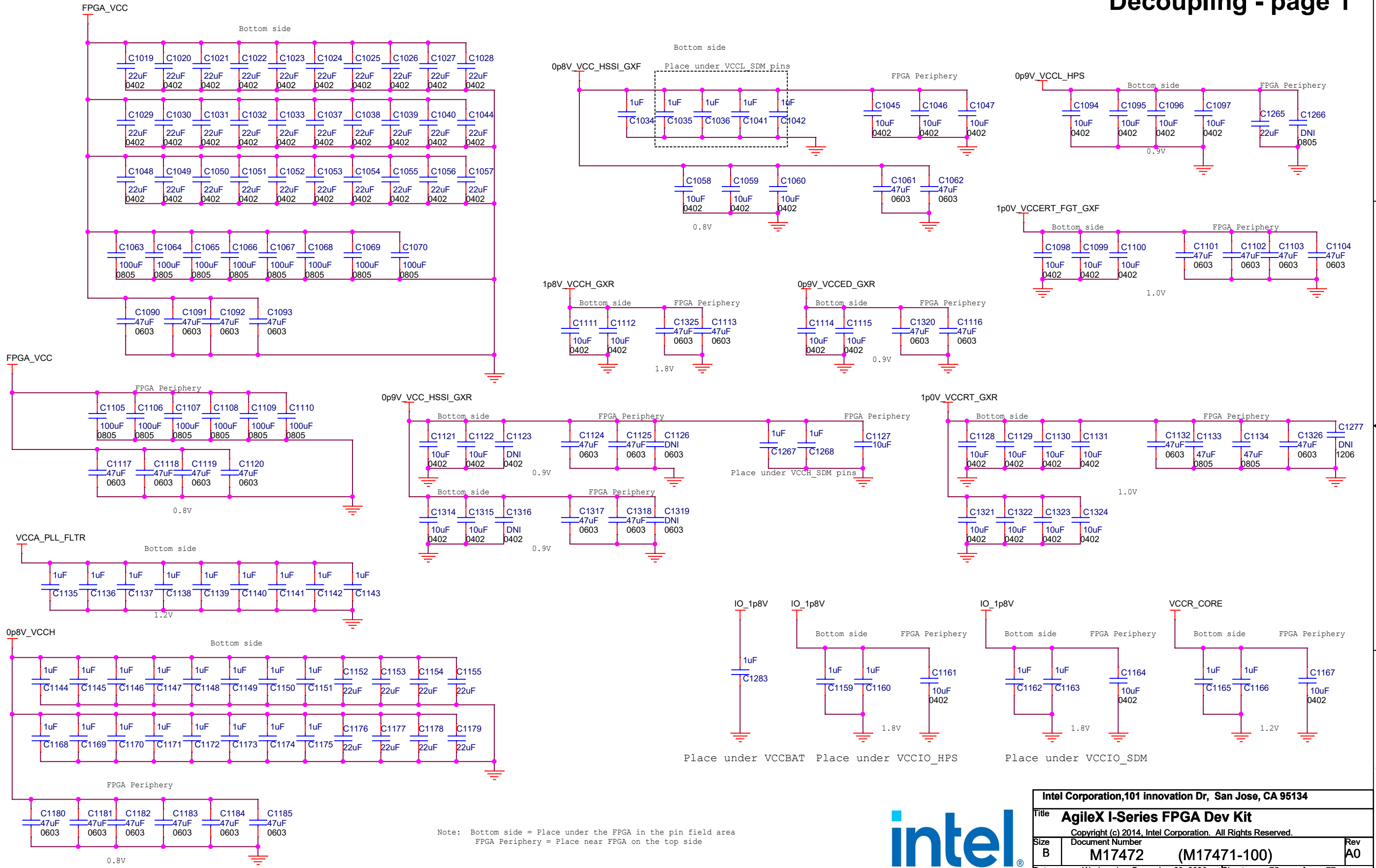
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PWR - 2p5V

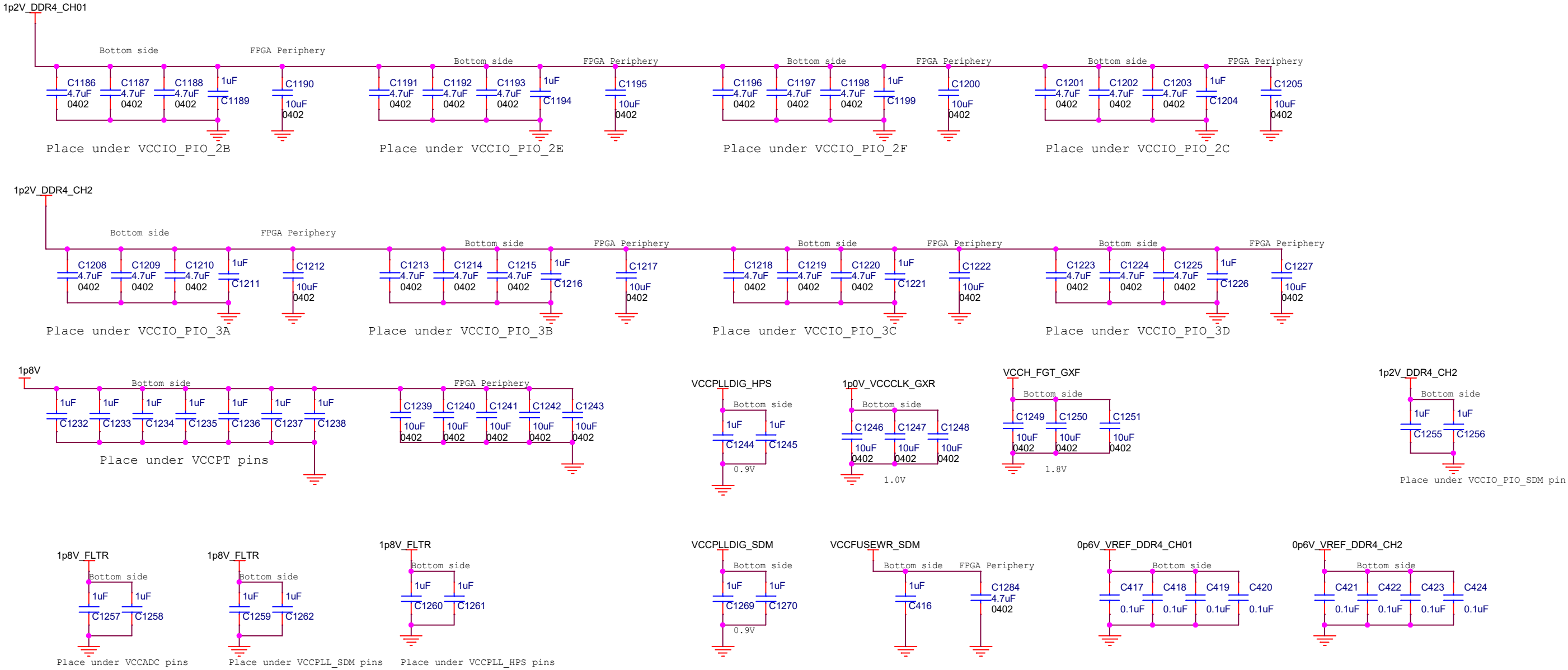


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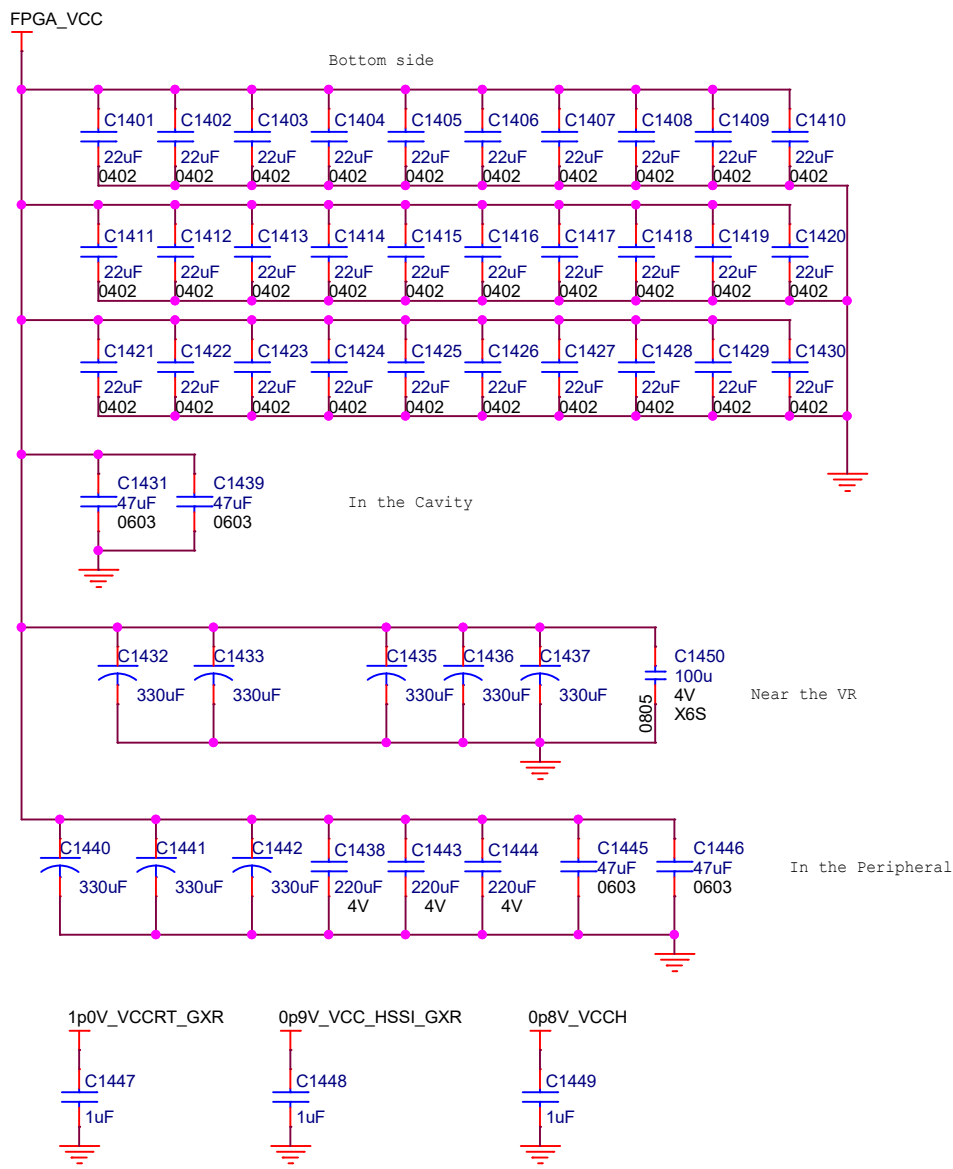
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Note: Bottom side = Place under the FPGA in the pin field area
FPGA Periphery = Place near FPGA on the top side



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