REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					

REV STATUS OF PAGES	REV																
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13			

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime
Original date of drawing YY MM DD 20-01-22	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, QUAD CHANNEL, 256-POSITION, SPI, NONVOLATINE DIGITAL POTENTIOMETER, MONOLITHIC SILICON
	APPROVED BY Muhammad A. Akbar	
	SIZE A / CODE IDENT. NO. 16236	DWG NO. **V62/20603**
	REV	PAGE 1 OF 13

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

AMSC N/A

5962-V015-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Quad Channel, 256-Position, SPI, Nonvolatile Digital Potentiometer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/20603	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5144-EP	Quad Channel, 256-Position, SPI, Nonvolatile Digital Potentiometer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-153-AC	Small Outline Transistor Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

V_{DD} to GND .... -0.3 V to +7.0 V
V_{SS} to GND .... +0.3 V to -7.0 V
V_{DD} to V_{SS} .... 7 V
V_{LOGIC} to GND .... -0.3 V to V_{DD} +0.3 V or +7.0 V (whichever is less)
V_A, V_W, V_B to GND .... V_{SS} – 0.3 V, V_{DD} + 0.3 V
IA, IW, IB:
Pulsed 3/, R_{AW} = 10 kΩ
Frequency > 10 kHz .... ±6 mA/d 4/
Frequency ≤ 10 kHz .... ±6 mA/√d 4/
Digital Inputs .... -0.3 V to V_{LOGIC} +0.3 V or +7.0 V (whichever is less)
Operating Temperature Range, T_A 5/ .... -55°C to +125°C
Maximum Junction Temperature, T_J Maximum .... 150°C
Storage Temperature Range .... -65°C to +150°C
Reflow Soldering:
Peak Temperature .... 260°C
Time at Peak Temperature .... 20 sec to 40 sec
Package Power Dissipation .... (T_J max – T_A)/ θ_{JA}
Field Induced Charged Device Model (FICDM) .... 1.5 kV

1.4 Thermal Resistance.

Case outline	θ_{JA} 6/	θ_{JC}	Unit
Case X	143	45	°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ TA = 25°C, unless otherwise noted.
3/ The maximum terminal current is bounded by the maximum current handling of the switches, the maximum power dissipation of the package, and the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
4/ d = pulse duty factor.
5/ T_A includes programming of EEPROM memory.
6/ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board, still air (0 m/sec airflow). See JEDEC JESD-51.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Input Shift Register Contents. The Input Shift Register Contents shall be as shown in figure 5.

3.5.6 SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1. The SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1 shall be as shown in figure 6.

3.5.7 SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0. The SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0 shall be as shown in figure 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits Min	Limits Typ 3/	Limits Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RESISTIVE DIGITAL-TO-ANALOG CONVERTERS (RDACs))						
Resolution	N		8			Bits
Resistor Integral Nonlinearity 4/	R-INL	Terminal A and Terminal B resistor (R_{AB}) = 10 kΩ $V_{DD} \geq 2.7$ V $V_{DD} < 2.7$ V	 -2 -5	 ±0.2 ±1.5	 +2 +5	 LSB LSB
Resistor Differential Nonlinearity 4/	R-DNL		-0.5	±0.2	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		-8	±1	+8	%
Resistance Temperature Coefficient 5/	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance 5/	RW	Code = zero scale, R_{AB} = 10 kΩ		55	125	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}	R_{AB} = 10 kΩ		40	80	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	-1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity 6/	INL	R_{AB} = 10 kΩ	-1	±0.2	+1	LSB
Differential Nonlinearity 6/	DNL		-0.5	±0.2	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	-2.5	-0.1		LSB
Zero-Scale Error	V_{WZSE}	RAB = 10 kΩ		1.2	3	LSB
Voltage Divider Temperature Coefficient 5/	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W	R_{AB} = 10 kΩ	-6		+6	mA
Terminal Voltage Range 7/			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B 5/	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, R_{AB} = 10 kΩ		25		pF
Capacitance W 5/	C_W	f = 1 MHz, measured to GND, code = half scale, R_{AB} = 10 kΩ		12		pF
Common-Mode Leakage Current 5/		Terminal A voltage (V_A) = wiper terminal voltage (V_W) = Terminal B voltage (V_B)	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic High Low	 V_{INH} V_{INL}	 V_{LOGIC} = 1.8 V to 2.3 V V_{LOGIC} = 2.3 V to 5.5 V	 $0.8 \times V_{LOGIC}$ $0.7 \times V_{LOGIC}$		 $0.2 \times V_{LOGIC}$	 V V V
Input Hysteresis 5/	V_{HYST}		$0.1 \times V_{LOGIC}$			V
Input Current 5/	I_{IN}				±1	µA
Input Capacitance 5/	C_{IN}			5		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	Pull-up resistor ($R_{PULL-UP}$) = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage	V_{OL}	Sink current (I_{SINK}) = 3 mA I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.4 0.6	V V
Three-State Leakage Current			-1		+1	µA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND Dual supply, V_{SS} < GND	1.8 2.25		V_{DD} V_{DD}	V
Positive Supply Current	I_{DD}	V_{INH} = V_{LOGIC} or V_{INL} = GND V_{DD} = 5.5 V V_{DD} = 2.3 V		 0.7 400	 5.5	 µA nA
Negative Supply Current	I_{SS}	V_{INH} = V_{LOGIC} or V_{INL} = GND	-5.5	-0.7		µA
EEPROM Store Current 5/ 8/	$I_{DD\_EEPROM\_STORE}$	V_{INH} = V_{LOGIC} or V_{INL} = GND		2		mA
EEPROM Read Current 5/ 9/	$I_{DD\_EEPROM\_READ}$	V_{INH} = V_{LOGIC} or V_{INL} = GND		320		µA
Logic Supply Current	I_{LOGIC}	V_{INH} = V_{LOGIC} or V_{INL} = GND		0.05	1.4	µA
Power Dissipation 10/	P_{DISS}	V_{INH} = V_{LOGIC} or V_{INL} = GND		3.5		µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = V_{DD} ± 10%, code = full scale		-66	-60	dB
DYNAMIC CHARACTERISTICS 11/						
Bandwidth	BW	−3 dB, R_{AB} = 10 kΩ		3		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz		-80		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz, R_{AB} = 10 kΩ		7		nV/√Hz
VW Settling Time	t_S	VA = 5 V, VB = 0 V, from zero scale to full scale, ±0.5 LSB error band, R_{AB} = 10 kΩ		2		µs
Crosstalk (CW1/CW2)	C_T	R_{AB} = 10 kΩ		10		nV-sec
Analog Crosstalk	C_{TA}			-90		dB
Endurance 12/		T_A = 25°C		1		Mcycles
		−40°C < T_A < +125°C	100			kcycles
Data Retention 13/ 14/				50		Years

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test 16/	Symbol	Test conditions 15/	Limits			Unit
			Min	Typ	Max	
INTERFACE TIMING SPECIFICATIONS **SPI Interface**						
SCLK cycle time	t1	V_{LOGIC} > 1.8 V	20			ns
		V_{LOGIC} = 1.8 V	30			
SCLK high time	t2	V_{LOGIC} > 1.8 V	10			
		V_{LOGIC} = 1.8 V	15			
SCLK low time	t3	V_{LOGIC} > 1.8 V	10			
		V_{LOGIC} = 1.8 V	15			
$\overline{SYNC}$ to SCLK falling edge setup time	t4		10			
Data setup time	t5		5			
Data hold time	t6		5			
$\overline{SYNC}$ rising edge to next SCLK fall ignored	t7		10			
Minimum $\overline{SYNC}$ high time	t8 17/		20			
SCLK rising edge to SDO valid	t9 18/			50		
$\overline{SYNC}$ rising edge to SDO pin disable	t10				500	
Start-up time (not shown in Figure 6 and Figure 7)	$t_{POWER-UP}$				75	µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.3 V to 5.5 V and V_{SS} = 0 V for the single-supply range, V_{DD} = 2.25 V to 2.75 V and V_{SS} = −2.25 V to −2.75 V for the dual-supply range, V_{LOGIC} = 1.8 V to 5.5 V, and −55°C < T_A < +125°C, unless otherwise noted. See the manufacturer data sheet for the test circuits that define the test conditions used in the Specifications section.

3/ Typical values represent average readings at 25°C, VDD = 5 V, VSS = 0 V, and VLOGIC = 5 V.

4/ Resistor integral nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to (0.7 × VDD)/RAB.

5/ Guaranteed by design and characterization, not subject to production test.

6/ INL and DNL are measured across the Terminal W and Terminal B voltage (VWB) with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

7/ Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment

8/ $I_{DD\_EEPROM\_STORE}$ is different from the operating current. Supply current for EEPROM program lasts approximately 30 ms.

9/ $I_{DD\_EEPROM\_READ}$ is different from the operating current. Supply current for EEPROM read lasts approximately 20 μs.

10/ PDISS is calculated from (I_{DD} × V_{DD}) + (I_{LOGIC} × V_{LOGIC}).

11/ All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.

12/ Endurance is qualified per JEDEC Standard 22, Method A117 to 100,000 cycles measured at −40°C to +125°C.

13/ Retention lifetime equivalent at junction temperature (TJ) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.

14/ 50 years apply to an endurance of 1000 cycles. An endurance of 100,000 cycles has an equivalent retention lifetime of 5 years.

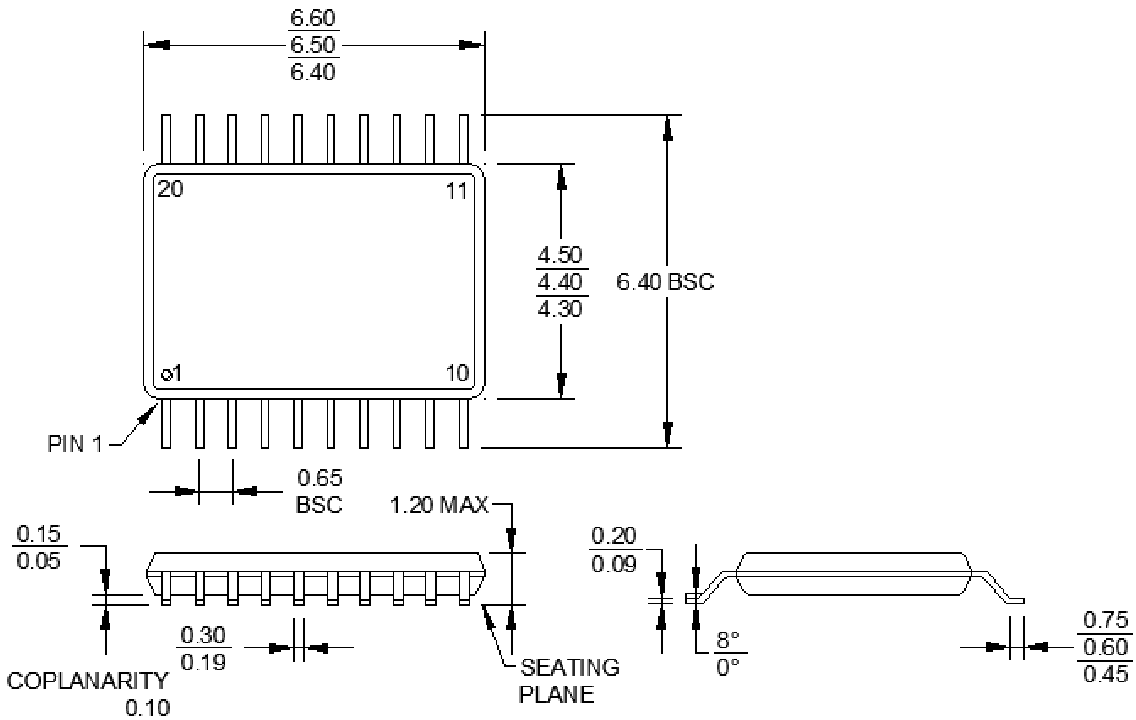
15/ V_{LOGIC} = 1.8 V to 5.5 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

16/ All input signals are specified with rising time (t_R) = falling time (t_F) = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

17/ Refer to $t_{EEPROM\_PROGRAM}$ and $t_{EEPROM\_READBACK}$ for memory command operations (see the control pins table in the AD5144 manufacturer data sheet for additional information).

18/ The pull-up resistance (R_{PULL_UP}) = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.

Case X



NOTES:

1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AC.

FIGURE 1. Case outline.

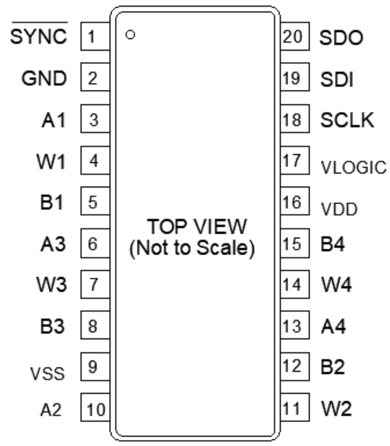


FIGURE 2. Terminal connections.

Pin No.	Mnemonic	Description
1	$\overline{SYNC}$	Synchronization Data Input, Active Low. When $\overline{SYNC}$ returns high, data is loaded into the input shift register.
2	GND	Ground Pin, Logic Ground Reference.
3	A1	Terminal A of RDAC 1. $V_{SS} \leq V_A \leq V_{DD}$.
4	W1	Wiper Terminal of RDAC 1. $V_{SS} \leq V_W \leq V_{DD}$.
5	B1	Terminal B of RDAC 1. $V_{SS} \leq V_B \leq V_{DD}$.
6	A3	Terminal A of RDAC 3. $V_{SS} \leq V_A \leq V_{DD}$.
7	W3	Wiper Terminal of RDAC 3. $V_{SS} \leq V_W \leq V_{DD}$.
8	B3	Terminal B of RDAC 3. $V_{SS} \leq V_B \leq V_{DD}$.
9	VSS	Negative Power Supply. Decouple this pin with 0.1 μF ceramic capacitors and 10 μF capacitors.
10	A2	Terminal A of RDAC 2. $V_{SS} \leq V_A \leq V_{DD}$.
11	W2	Wiper Terminal of RDAC 2. $V_{SS} \leq V_W \leq V_{DD}$.
12	B2	Terminal B of RDAC 2. $V_{SS} \leq V_B \leq V_{DD}$.
13	A4	Terminal A of RDAC 4. $V_{SS} \leq V_A \leq V_{DD}$.
14	W4	Wiper Terminal of RDAC 4. $V_{SS} \leq V_W \leq V_{DD}$.
15	B4	Terminal B of RDAC 4. $V_{SS} \leq V_B \leq V_{DD}$.
16	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 μF ceramic capacitors and 10 μF capacitors.
17	V_{LOGIC}	Logic Power Supply, 1.8 V to V_{DD}. Decouple this pin with 0.1 μF ceramic capacitors and 10 μF capacitors.
18	SCLK	Serial Clock Line. Data is clocked in at the logic low transition.
19	SDI	Serial Data Input.
20	SDO	Serial Data Output. SDO is an open-drain output pin that must have an external pull-up resistor.

FIGURE 3. Terminal function.

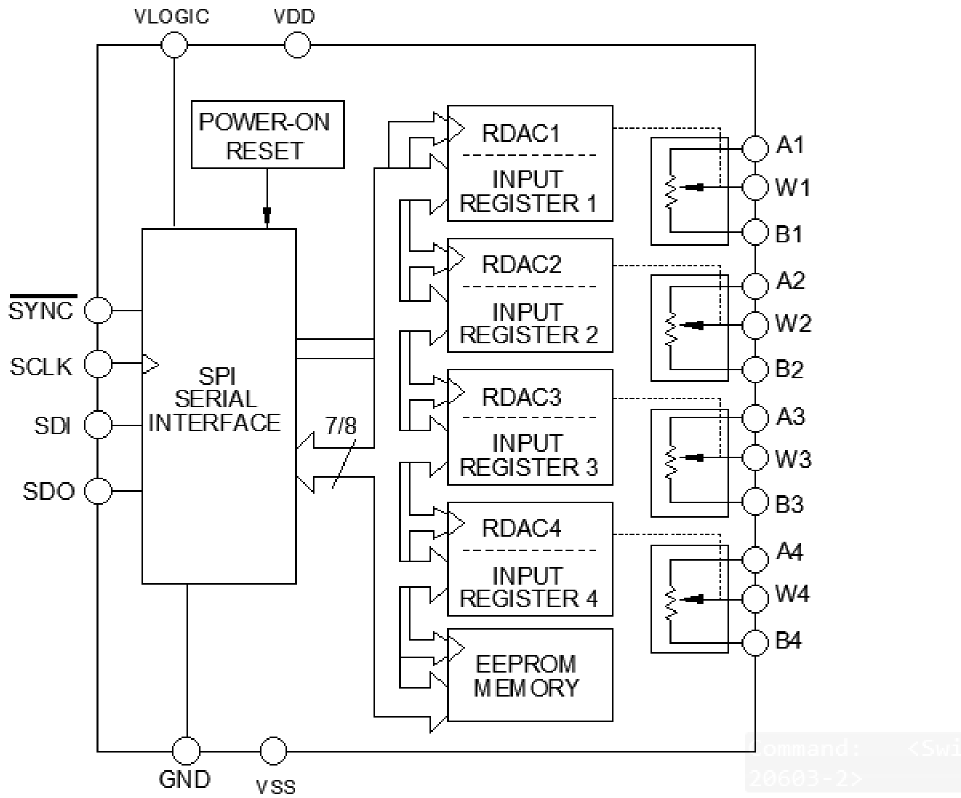


FIGURE 4. Functional block diagram.

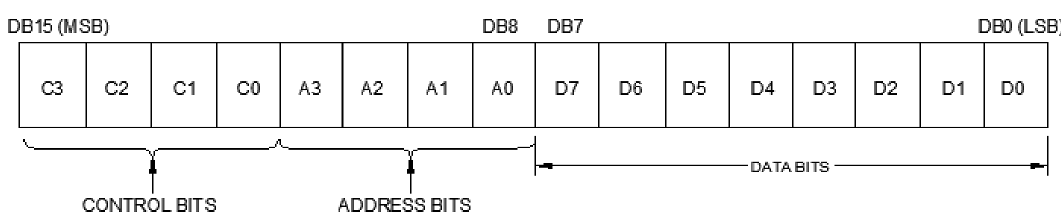


FIGURE 5. Input Shift Register Contents.

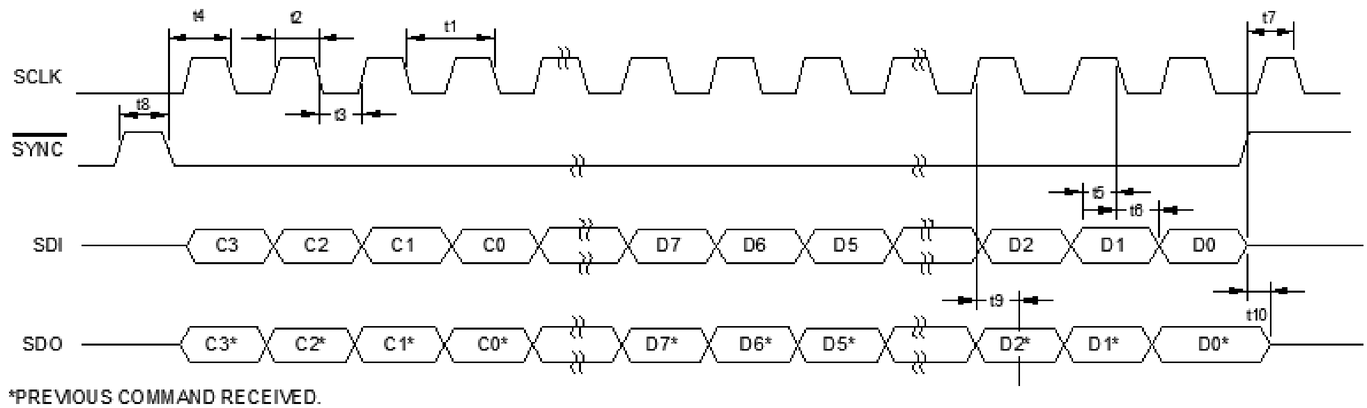


FIGURE 6. SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1.

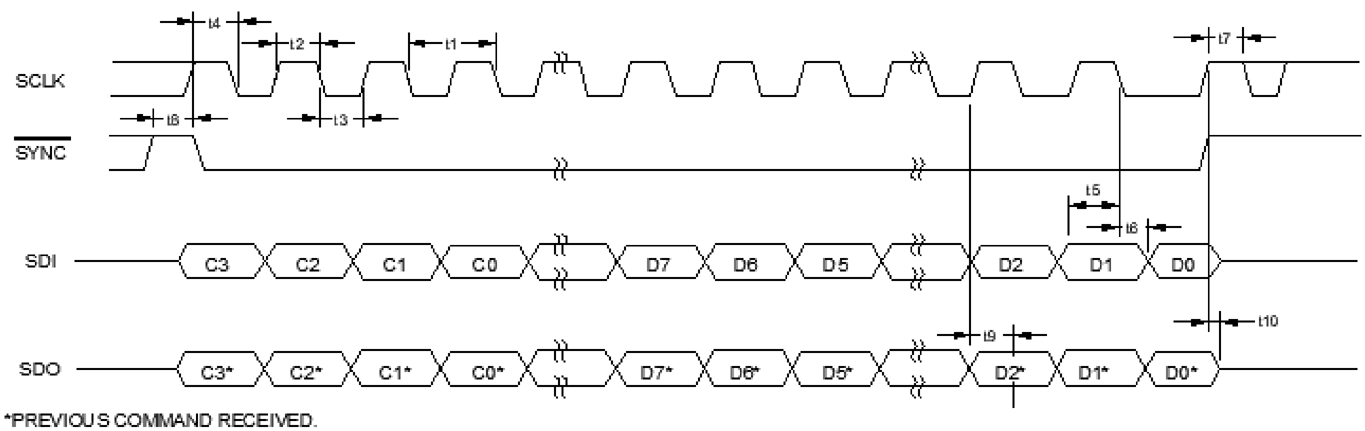


FIGURE 7. SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/20603-01XE	24355	Tube quantities = 75	AD5144TRUZ10-EP
		Reel quantities = 1000	AD5144TRUZ10-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106