

DS1609 Dual Port RAM

DS1609

FEATURES

- Totally asynchronous 256-byte dual port memory
- Multiplexed address and data bus keeps pin count low
- · Dual port memory cell allows random access with minimum arbitration
- · Each port has standard independent RAM control signals
- · Fast access time
- Low power CMOS design
- 24-pin DIP or 24-pin SOIC surface mount package
- Both CMOS and TTL compatible
- Operating temperature of -40°C to +85°C
- Standby current of 100 nA @ 25°C makes the device NOT RE ideal for battery backup or battery operate applica-



PIN ASSIGNMENT

AD0–AD7	 Port address/d
CE	 Port enable
WE	 Write enable
OE	 Output enable
V _{CC}	 +5 volt supply
GND	 Ground

DESCRIPTION

The DS1609 is a random access 256-byte dual port memory designed to connect two asyncronous address/data buses together with a common memory element. Both ports have unrestricted access to all 256 bytes of memory, and with modest system discipline no arbitration is required. Each port is controlled by three control signals: output enable, write enable, and port enable. The device is packaged in plastic 24-pin DIP and 24-pin SOIC. Output enable access time of 50 ns is available when operating at 5 volts.

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OPERATION – READ CYCLE

The main elements of the dual port RAM are shown in Figure 1.

A read cycle to either port begins by placing an address on the multiplexed bus pins AD0 – AD7. The port enable control (\overline{CE}) is then transitioned low. This control signal causes address to be latched internally. Addresses can be removed from the bus provided address hold time is met. Next, the output enable control (\overline{OE}) is transitioned low, which begins the data access portion of the read cycle. With both \overline{CE} and \overline{OE} active low, data will appear valid after the output enable access time t_{OEA}. Data will remain valid as long as both port enable and output enable remains low. A read cycle is terminated with the first occurring rising edge of either \overline{CE} or \overline{OE} . The address/data bus will return to a high impedance state after time t_{CEZ} or t_{OEZ} as referenced to the first occurring rising edge. WE must remain high during read cycles.

OPERATION – WRITE CYCLE

A write cycle to either port begins by placing an address on the multiplexed bus pins AD0 – AD7. The port enable control (\overline{CE}) is then transitioned low. This control signal causes address to be latched internally. As with a read cycle, the address can be removed from the bus provided address hold time is met. Next the write enable control signal (\overline{WE}) is transitioned low which begins the write data portion of the write cycle. With both \overline{CE} and $\overline{\text{WE}}$ active low the data to be written to the selected memory location is placed on the multiplexed bus. Provided that data setup (t_{DS}) and data hold (t_{DH}) times are met, data is written into the memory and the write cycle is terminated on the first occurring rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$. Data can be removed from the bus as soon as the write cycle is terminated. $\overline{\text{OE}}$ must remain high during write cycles.

ARBITRATION

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports (see Figure 2). Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or for writing from both ports at the same instant. A simple way to assure that read/write conflicts don't occur is to perform redundant read cycles. Write/write arbitration needs can be avoided by assigning groups of addresses for write operation to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

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BLOCK DIAGRAM: DUAL PORT RAM Figure 1 PORT A PORT B 8 ADDRESS 8 ADDRESS ADDRESS/ DATA MUX LATCH DECODE ADDRESS/ DATA MUX LATCH DECODE MUX ADDRESS/DATA MUX ADDRESS/DATA 256 BYTE DUAL PORT MEMORY MATRIX 8 DATA 8 DATA LUGIC LUGIC VCC OR MENNEN LUGIC LUGIC VCC OR MENNEN LUGIC LU WE OE WE CE DATA-PORT A DATA-PORT B ÷

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ABSOLUTE MAXIMUM RATINGS* Voltage on Any Pin Relative to Ground

Voltage on Any Pin Relative to Ground Operating Temperature Storage Temperature Soldering Temperature -0.5V to +7.0V -40°C to +85°C -55°C to +125°C 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS					(-40 °)	C to +85°C
PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Power Supply	V _{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V _{IH}	2.0		V _{CC} + 0.3	VC	Ч
Input Logic 0	V _{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

 $(-40^{\circ}\text{C to } +85^{\circ}\text{C}; \text{ V}_{\text{CC}} = 5\text{V} \pm 10\%)$

SYMBOL	MIN	ТҮР	МАХ	UNITS	NOTES
Z _{IN}	50K	FU.		Ω	2
ILO	-1.0		+1.0	μΑ	
I _{CCS1}	Ż	3.0	5.0	mA	3, 4, 13
I _{CCS2}		50	300	μΑ	3, 5, 13
I _{CCS3}		100		nA	3, 6, 13
I _{CC}		18	30	mA	7, 13
V _{OH}	2.4			V	8
V _{OL}			0.4	V	9
	SYMBOL ZIN ILO ICCS1 ICCS2 ICCS3 ICCS3 VOH VOL	SYMBOL MIN ZIN 50K ILO -1.0 ICCS1 -1.0 ICCS2 -1.0 ICCS3 -1.0 ICC -1.0 VOH 2.4 VOL -1.0	SYMBOL MIN TYP ZIN 50K -1.0 ILO -1.0 3.0 ICCS1 3.0 -1.0 ICCS2 50 50 ICCS3 100 100 ICC 18 18 VOH 2.4 -10	SYMBOL MIN TYP MAX Z _{IN} 50K - I _{LO} -1.0 +1.0 I _{CCS1} 3.0 5.0 I _{CCS2} 50 300 I _{CCS3} 100 - I _{CC} 18 30 V _{OH} 2.4 0.4	SYMBOL MIN TYP MAX UNITS Z _{IN} 50K Ω Ω I _{LO} -1.0 +1.0 μA I _{CCS1} 3.0 5.0 mA I _{CCS2} 50 300 μA I _{CCS3} 100 nA nA I _{CCC3} 1100 NA NA V _{CH} 2.4 18 30 MA V _{OH} 0.4 V V

CAPACITANCE						$(t_A = 25^{\circ}C)$
PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Capacitance	C _{IN}		5	10	pF	
I/O Capacitance	C _{I/O}		5	10	pF	

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AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Address Setup Time	t _{AS}	5			ns	
Address Hold Time	t _{AH}	25			ns	
Output Enable Access	t _{OEA}	0		50	ns	10
OE to High Z	t _{OEZ}	0		20	ns	
CE to High Z	t _{CEZ}	0		20	ns	
Data Setup Time	t _{DS}	0			ns	
Data Hold Time	t _{DH}	10			ns	
Write Pulse Width	t _{WP}	50			ns	(11)
CE Recovery Time	t _{CER}	20			ns	12
WE Recovery Time	t _{WER}	20		14	ns	12
OE Recovery Time	t _{OER}	20		E	ns	12
\overline{CE} to \overline{OE} Setup Time	t _{COE}	25	2		ns	
CE to WE Setup Time	t _{CWE}	25	çU'		ns	
AC ELECTRICAL CHARACTERISTICS $(-40^{\circ}C \text{ to } +85^{\circ}C; V_{CC} = 2.5V - 4.5V)$						

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Address Setup Time	t _{AS}	5			ns	
Address Hold Time	t _{AH}	25			ns	
Output Enable Access	t _{OEA}	0		100	ns	10
OE to High Z	t _{OEZ}	0		20	ns	
CE to High Z	t _{CEZ}	0		20	ns	
Data Setup Time	t _{DS}	0			ns	
Data Hold Time	t _{DH}	10			ns	
Write Pulse Width	t _{WP}	100			ns	11
CE Recovery Time	t _{CER}	20			ns	12
WE Recovery Time	t _{WER}	20			ns	12
OE Recovery Time	t _{OER}	20			ns	12
CE to OE Setup Time	t _{COE}	25			ns	
CE to WE Setup Time	t _{CWE}	25			ns	

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DUAL PORT RAM TIMING: READ CYCLE

DURING READ CYCLE $\overline{WE} = V_{IH}$



NOTES:

- 1. During read cycle the address must be off the bus prior to t_{OEA} minimum to avoid bus contention.
- 2. Read cycles are terminated by the first occurring rising edge of $\overline{\text{OE}}$ or $\overline{\overline{\text{CE}}}$.

DUAL PORT RAM TIMING: WRITE CYCLE

DURING WRITE CYCLE $\overline{OE} = V_{IH}$



NOTE:

1. Write cycles are terminated by the first occurring edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

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NOTES:

- 1. All Voltages are referenced to ground.
- 2. All pins other than CE, WE, OE, V_{CC} and ground are continuously driven by a feedback latch in order to hold the inputs at one power supply rail or the other when an input is tristated. The minimum driving impedance presented to any pin is $50K\Omega$. If a pin is at a logic low level, this impedance will be pulling the pin to ground. If a pin is at a logic high level, this impedance will be pulling the pin to V_{CC} .
- 3. Standby current is measured with outputs open circuited.
- 4. I_{CCS1} is measured with all pins within 0.3V of V_{CC} or GND and with CE at a logic high or logic low level.
- 5. I_{CCS2} is measured with all pins within 0.3V of V_{CC} or ground and with \overline{CE} within 0.3V of V_{CC} .
- 6. I_{CCS3} is measured with all pins at V_{CC} or ground potential and with $\overline{CE} = V_{CC}$. Note that if a pin is floating, the internal feedback latches will pull all the pins to one power supply rail or the other.
- 7. Active current is measured with outputs open circuited, and inputs swinging full supply levels with one port reading and one port writing at 100 ns cycle time. Active currents are a DC average with respect to the number of 0's and RNEW 1's being read or written.
- 8. Logic one voltages are specified at a source current of 1 mA.
- 9. Logic zero voltages are specified at a sink current of 4 mA
- 10. Measured with a load as shown in Figure 3.
- 11. t_{WP} is defined as the time from \overline{WE} going low to the first of the rising edges of \overline{WE} and \overline{CE} .
- 12. Recovery time is the amount of time control signals must remain high between successive cycles.
- 13. Typical values are at 25°C

LOAD SCHEMATIC Figure 3



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