MAX77785/MAX77786

18.2VIN, 3.5A/5.5A 1-Cell Li+ Battery Charger for USB Type-C Power Delivery

General Description

The MAX77785/MAX77786 is a high-performance high-input 3.5/5.5A fast charger with Smart Power Selector™. The ICs can operate as a reverse boost converter without an additional inductor, allowing the battery to share its power through the charging port, and offer programmable output voltage from 4.505V to 10.805V. The devices feature fully integrated low-loss power switches to provide a small solution size and high efficiency, even at high input voltage and high charging current. Its high switching frequency allows the use of a smaller-sized inductor. The ICs feature true load disconnection in reverse boost mode and have an adjustable output current protection limit. The device is highly flexible and programmable through I^2C configuration. Li-ion, Li-polymer, and $LiFePO_4$ battery chemistries are supported. It can also provide fast programmable unplug detection of sources for dynamic system load management. To support a variety of legacy USBs as well as proprietary adapters, the device also integrates BC1.2 detection using the D+ and D- pins.

The battery charger includes a Smart Power Selector to accommodate a wide range of battery sizes and system loads. The Smart Power Selector allows the system to start up gracefully when an input source is available, even when the battery is deeply discharged (dead battery) or missing. It can be configured so that when power is applied to the charger input, the battery charging can automatically start.

Applications

- Gaming Devices
- VR Applications
- mPOS
- Tablet PCs

Smart Power Selector is a trademark of Maxim Integrated Products, Inc

USB Type-C is a registered trademark of USB Implementers Forum, Inc.

Power Path is a trademark of Linear Technology Corporation.

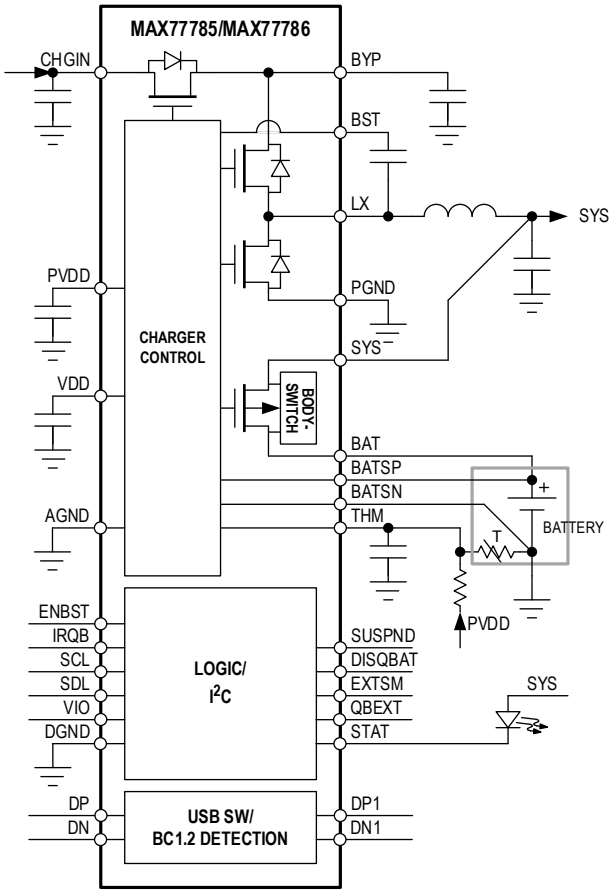
Benefits and Features

- High-Efficiency Single-Cell Switching Charger
  - Up to 5.5A Charging with MAX77786
  - Up to 3.5A Charging with MAX77785
  - 90% Buck Efficiency at 4A, 15V Input
  - Up to 5.5A Input Current Limit with AICL (MAX77786)
  - Up to 3.5A Input Current Limit with AICL (MAX77785)
- +26V Absolute Maximum Input Voltage Rating
- 4.7V to 18.2V Input Operating Voltage Range
- Reverse Boost with Programmable Output Voltage Options up to 10.805V
  - Up to 16.2W for MAX77786
  - Up to 10.8W for MAX77785
  - Dedicated Boost enable input
- Integrated Battery True-Disconnect FET
  - R_{DSON} = 7.7mΩ
  - Programmable Discharge Current Limit up to 10A
  - Shipping Mode and Low Battery Leakage Current
  - 1.3MHz Switching Frequency with 1µH Inductor
  - Disconnect Input (DISQBAT)
- Safety
  - Battery Temperature Sensing and Charge Safety Timer
  - JEITA Guideline Compliant
  - Thermal Regulation and Thermal Shutdown
  - System Voltage OVLO/UVLO
- USB Switch with BC1.2 Detection
- Spread Spectrum for Noise-Sensitive Applications
- Charge Status Output for LED
- Push-Button Input for Exiting from Ship Mode
- Programmable Unplug Detection Output
- Dedicated Input for Suspend Mode (SUSPND)
- I^2C Interface
- 2.96 mm x 2.96 mm WLP

***Ordering Information* appears at end of data sheet.**

19-101772; Rev 0; 2/24

Simplified Block Diagram



Absolute Maximum Ratings

CHGIN to PGND ..... -0.3V to +26V
BYP to PGND..... -0.3V to +26V
BYP to CHGIN ..... -0.3V to +16V
BYP to LX..... -0.3V to +26V
BYP to SYS..... -0.3V to +26V
LX to PGND ..... -0.3V to +26V
BST to PVDD ..... -0.3V to +26V
BST to LX..... -0.3V to +2.2V
SYS to AGND..... -0.3V to +6.0V
BATT to AGND..... -0.3V to +6.0V
BATSP to AGND .....-0.3V to V_{BATT} +0.3V
BATSP to BATT ..... -0.3V to +0.3V
BATSN to AGND..... -0.3V to +0.3V
PGND to AGND ..... -0.3V to +0.3V
DGND to AGND ..... -0.3V to +0.3V
PVDD to PGND..... -0.3V to +2.2V
VDD to AGND ..... -0.3V to +2.2V
VIO to AGND..... -0.3V to +6.0V

DP, DN, DP1, DN1 .....-0.3V to +6.0V
DISQBAT, SUSPEND, QBEXT to AGND.....-0.3V to +6.0V
ENBST .....-0.3V to +6.0V
EXTSM to AGND ..... -0.3V to V_{BATT} +0.3V
IRQB, STAT to AGND .....-0.3V to +6.0V
THM to AGND..... -0.3V to V_{PVDD}+0.3V
SDA, SCL to AGND ..... -0.3V to +6.0VV
CHGIN Continuous Current..... 5.5A_{RMS}
BYP Continuous Current ..... 3.4A_{RMS}
PGND Continuous Current ..... 6.8A_{RMS}
LX Continuous Current ..... 10.2A_{RMS}
SYS, BATT Continuous Current ..... 10A_{RMS}
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, duration is 23.68mW/°C above +70°C) ..... mW to 1894.4mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

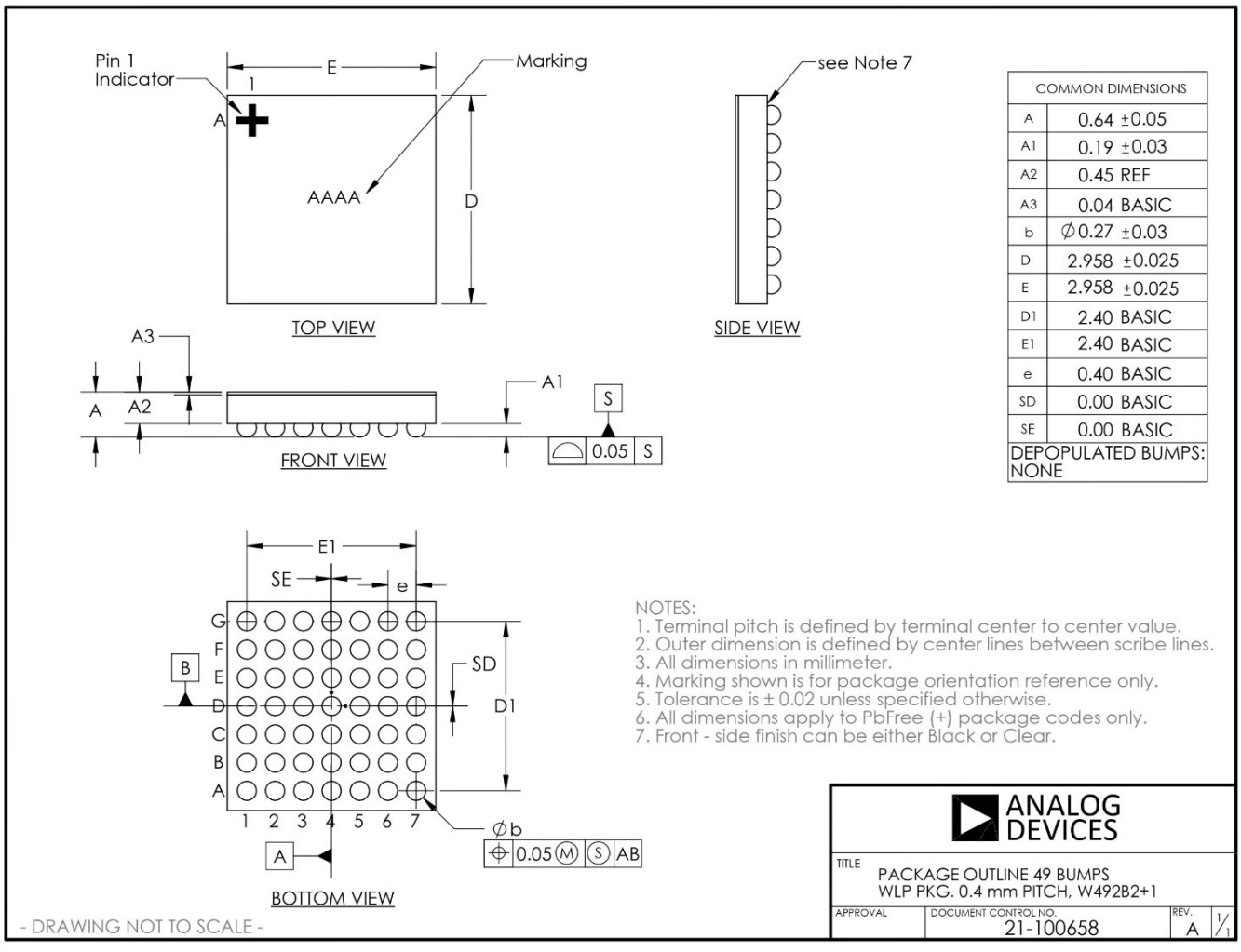
Package Information

WLP

Package Code	W492B2+1
Outline Number	*21-100658*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	42.23 (°C/W)
Junction-to-Case Thermal Resistance (θ_{JC})	
Junction-to-Case Thermal Resistance (θ_{JB})	

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.



Electrical Characteristics

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS						
CHGIN Quiescent Current	I_{CHGIN}	V_{CHGIN} = 5.0V, SUSPEND pin digital high or MODE = 0, DEEP_SUSP_DIS = 1		0.19	0.32	mA
		V_{CHGIN} = 5.0V, SUSPEND pin digital high or MODE = 0, DEEP_SUSP_DIS = 0		65		µA
		V_{CHGIN} = 5.0V, V_{BATT} = 4.2V, MODE = 5, DONE state (V_{SYS} = 4.35V), I_{SYS} = 0A		2.35		mA
Input Undervoltage Supply Current	I_{IN}	V_{CHGIN} = 2.4V, the input is undervoltage		0.035		mA
BAT Quiescent Current	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, $Q_{BATT\ FET}$ is on, B2SOVRC_CTRL = 0, LPM = 0, I_{SYS} = 0A		29		µA
BAT Quiescent Current in Low-Power Mode	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, $Q_{BATT\ FET}$ is on, B2SOVRC = 0, LPM = 1, I_{SYS} = 0A		22		µA
BAT Quiescent Current in Factory-Ship Mode	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, $Q_{BATT\ FET}$ is off, V_{SYS} = V_{VDD} = 0V, factory-ship mode		3	4.6	µA
BAT Quiescent Current in Done State	IMBDN	V_{CHGIN} = 5V, I_{BYP} = 0A, V_{BATT} = 4.2V, I_{SYS} = 0A, $Q_{BATT\ FET}$ is off, B2SOVRC = 0, MODE = 5, DONE state		7.2	10.1	µA
		V_{CHGIN} = 18.2V, I_{BYP} = 0A, V_{BATT} = 4.2V, I_{SYS} = 0A, $Q_{BATT\ FET}$ is off, B2SOVRC = 0, MODE = 1, DONE state		7.2	10.1	
SYS Quiescent Current in Done State	IMSDN	V_{CHGIN} = 18.2V, I_{BYP} = 0A, V_{BATT} = 4.2V, I_{SYS} = 0A, $Q_{BATT\ FET}$ is off, B2SOVRC = 0, MODE = 1, DONE state		1.1	1.4	mA
SYS Operating Voltage	V_{SYS}	Guaranteed by $V_{SYS\_UVLO\_R}$ and $V_{SYS\_OVLO\_R}$	$V_{SYS\_UVLO\_R}$		$V_{SYS\_OVLO\_R}$	V
VIO Voltage Range	V_{VIO}		1.62		5.5	V
SCL, SDA Input Low Level	$V_{SCL\_SDA\_IN\_L}$	T_A = +25°C			0.3 x V_{VIO}	V
SCL, SDA Input High Level	$V_{SCL\_SDA\_IN\_H}$	T_A = +25°C	0.7 x V_{VIO}			V
SCL, SDA Input Hysteresis	$V_{SCL\_SDA\_HYS}$	T_A = +25°C		0.05 x V_{VIO}		V
SCL, SDA Logic Input Current	I_{SCL_SDA}	V_{SCL} = V_{SDA} = V_{VIO} = 1.9V	-10		+10	µA
SDA Output Low Voltage	$V_{SDA\_OUT\_L}$	I_{SDA} = 20mA sinking			0.4	V
IRQB Output Low Voltage	$V_{IRQB\_OUT\_L}$	I_{IRQB} = 1mA sinking			0.4	V
IRQB Output High Leakage	I_{IRQB_H}	V_{IRQB} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{IRQB} = 5.5V, T_A = +85°C		0.1		
CHGIN INPUT LIMITER						
CHGIN Operating Voltage Range	V_{CHGIN}	V_{CHGIN} must be less than V_{CHGIN_OVLO} and greater than both V_{CHGIN_UVLO} and (V_{SYS} + $V_{CHGIN2SYS\_TH}$) for the charger to turn on	V_{CHGIN_UVLO}		V_{CHGIN_OVLO}	V

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} rising	18.2	18.45	18.7	V
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OVLO\_HYS}$			500		mV
CHGIN Undervoltage Threshold Setting Range	V_{CHGIN_UVLO}	V_{CHGIN} rising, programmable at 4.7V, 4.8V, 4.9V, 5.1V	4.7		5.1	V
CHGIN Undervoltage Threshold Hysteresis	$V_{CHGIN\_UVLO\_HYS}$			1		V
CHGIN Undervoltage Threshold Accuracy	$V_{CHGIN\_UVLO\_ACC}$	V_{CHGIN} rising, 4.7V setting	4.625	4.7	4.775	V
CHGIN to SYS Undervoltage Threshold Rising	$V_{CHGIN2SYS\_TH}$	V_{CHGIN} - V_{SYS}, rising	0.15	0.20	0.25	V
CHGIN Turn-On Threshold Validation Delay	t_{D-UVLO}	Delay from V_{CHGIN} > V_{CHGIN_UVLO} to $Q_{CHGIN\ FET}$ enable		8		ms
CHGIN Switching Start Delay	t_{START}	Delay from Input Validation to LX switching (if charge or buck mode is selected and charger is not suspended); see the *Input Validation* section for input validation conditions		150		ms
CHGIN Adaptive Voltage Regulation Threshold Setting Range	V_{CHGIN_REG}	Programmable at 4.5V, 4.6V, 4.7V, 4.9V. The input voltage regulation loop decreases the input current to regulate V_{CHGIN} at V_{CHGIN_REG} under weak input source conditions. If the input current is decreased to I_{IULO_DET} and the input voltage is equal to or below V_{CHGIN_REG}, then the charger input is turned off.	4.5		4.9	V
CHGIN Adaptive Voltage Regulation Threshold Accuracy	$V_{CHGIN\_REG\_ACC}$	4.5V setting	4.4	4.5	4.6	V
CHGIN Input Current Limit Setting Range	$I_{INLIMIT}$	Programmable, 500mA default, 50mA step, production tested at 100mA, 500mA, 1000mA, 1800mA and 3200mA (MAX77785)	0.05		3.5	A
		Programmable, 500mA default, 50mA step, production tested at 100mA, 500mA, 1000mA, 1800mA, 3200mA, and 5000mA settings only (MAX77786)	0.05		5.5	
CHGIN Input Current Limit Accuracy	$I_{INLIMIT}$	CHGIN_ILIM ≥ 0.5A	-7.8		-0.8	%
CHGIN Input Current Low Threshold	I_{IULO_DET}	Charger enabled, 3200mA input current limit setting		26		mA
CHGIN Unplug Detection Threshold Setting Range	V_{CHGIN_UNPLG}	V_{CHGIN} falling	CHGIN_REG (AICL enabled) or $V_{CHGIN\_UVLO\_F}$		17.50	V

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
			(AICL disabled)			
CHGIN Unplug Detection Threshold Accuracy	$V_{CHGIN\_UNPLG\_ACC}$	V_{CHGIN} falling, UNPLUG_TH = 0x02 (7.95V)	-0.09		+0.09	V
		V_{CHGIN} falling, UNPLUG_TH = 0x27 (13.1V)	-0.16		+0.16	
CHGIN Unplug Detection Threshold Hysteresis	$V_{CHGIN\_UNPLUG\_HYS}$			500		mV
CHGIN Input Self-Discharge Resistance	R_{INSD}			88		kΩ
SYSTEM BUCK						
Buck Output Voltage Setting Range	V_{BCKSYS}	Programmable 3V to 5V in 50mV steps (5-bits). Production tested at 4.2V only; MODE = 4, 7	3		5	V
Buck Output Voltage Accuracy	V_{BCKSYS_ACC}	MODE = 4, 7	-3		+3	%
Buck Output Tracking Voltage Range	V_{TRACK}	$V_{TRACK\_LOW\_RANGE}$ = 0; MODE = 4 or 5 DONE; MODE = 7, V_{TRACK} = SYS-BAT, valid when BAT + V_{TRACK} > V_{BCKSYS} (More detail in $V_{TRACK\_LOW\_RANGE}$ register)	450		900	mV
		$V_{TRACK\_LOW\_RANGE}$ = 1; MODE = 4 or 5 DONE; V_{TRACK} = SYS-BAT, valid when BAT + V_{TRACK} > V_{BCKSYS} (More detail in $V_{TRACK\_LOW\_RANGE}$ register)	0		450	
Buck Inductor Current Limit	I_{HSILIM}	For MAX77786	10.0	11.1	12.2	A
		For MAX77785	7.5	8.3	9.1	
Buck Minimum On Time	t_{ON-MIN}	Measured on LX		100		ns
Buck Minimum Off Time	$t_{OFF-MIN}$	Measured on LX		100		ns
System Power-Up Current (from BYP)	I_{SYSPU_BYP}	Charger present, V_{SYS} < $V_{SYS\_UVLO\_R}$	50	75	100	mA
System Power-Up Time-Out (from BYP)	t_{SYSPU_BYP}			150		ms
Spread Spectrum Modulation Envelope	ΔFSS	SS_ENB = 0b01		±4		%
		SS_ENB = 0b10		±8		
		SS_ENB = 0b11		±16		
CHARGER						
Precharge Charge Current	I_{PRECHG}	V_{BATT} < V_{PRECHG}	40	55	80	mA
Precharge Voltage Threshold	V_{PRECHG}	V_{BATT} rising	2.425	2.5	2.575	V
Precharge Voltage Threshold Hysteresis	V_{PRECHG_HYS}			500		mV
Trickle Charge Current Accuracy	$I_{TRICKLE\_ACC}$	TKEN = 1 by default, V_{PRECHG} < V_{BATT} < $V_{TRICKLE}$	270	300	330	mA
Trickle Charge Voltage Threshold Range	$V_{TRICKLE}$	Programmable by VTK[2:0], TKEN = 1	2.8		3.5	V

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Trickle Charge Voltage Threshold Accuracy	$V_{TRICKLE\_ACC}$	V_{BATT} rising, TKEN = 1 by default, VTK[2:0] = 0b011	3.0	3.1	3.2	V
Trickle Charge Voltage Threshold Hysteresis	$V_{TRICKLE\_HYS}$	TKEN = 1 by default		100		mV
Prequalification Time	t_{PQ}	This applies to the total time of precharge and trickle charge mode		30		min
Fast-Charge Current Setting Range	I_{FC}	100mA to 5500mA in 50mA steps; production tested at 500mA, 1000mA, 3000mA, and 5000mA settings (MAX77786 only)	0.05		5.5	A
		100mA to 3500mA in 50mA steps; production tested at 500mA, 1000mA, and 3000mA settings (MAX77785 only)	0.05		3.5	
Fast-Charge Current Accuracy (Mode = 0x5)	I_{FC_ACC}	Programmed I_{FC} ≥ 500mA, V_{BATT} > V_{MINSYS}, T_A = +25°C	-3.5		+3.5	%
		Programmed I_{FC} ≥ 500mA, V_{BATT} > V_{MINSYS}, T_A = -5°C to +85°C	-6		+6	
		Programmed I_{FC} ≥ 500mA, $V_{TRICKLE}$ < V_{BATT} < V_{MINSYS} (LDO mode), T_A = -5°C to +85°C	-10		+10	
Fast-Charge Current Accuracy (Mode = 0x1 or 7)	I_{FC_ACC}	Programmed I_{FC} ≥ 500mA, V_{SYS} > SYSAICL, T_A = -5°C to +85°C	-10		+10	%
Fast-Charge Current Thermal Regulation Setting Range	T_{REG}	Junction temperature when charge current starts to reduce for thermal regulation; programmable from +86°C to +128°C in 6°C steps; default value is +116°C	86		128	°C
Fast-Charge Termination Voltage Setting Range	$V_{BATTREG}$	Programmable from 3.5V to 4.6V in 10mV step; production tested at 4.2V and 4.35V only	3.5		4.6	V
Fast-Charge Termination Voltage Accuracy at Room Temp	$V_{BATTREG\_ACC}$	$V_{BATTREG}$ = 4.35V setting, represented as percentage of $V_{BATTREG}$; T_A = +25°C	-0.4	-0.3	-0.2	%
Fast-Charge Termination Voltage Accuracy	$V_{BATTREG\_ACC}$	$V_{BATTREG}$ = 4.35V setting, represented as percentage of $V_{BATTREG}$; T_A = -5°C to +85°C	-0.6	-0.3	+0.0	%
Fast-Charge Termination Debounce Time	t_{TERM}			100		ms
Fast-Charge Constant Current + Constant Voltage Safety Time	t_{FC}	Adjustable from 3hrs, 4hrs, 5hrs, 6hrs, 7hrs, 8hrs, 10hrs including a disable setting; 5hrs default		5		hrs
Top-Off Current Setting Range	I_{TO}	Programmable by TO_ITH[4:0] production tested at 50mA, 200mA, 500mA, and 1000mA settings	50		1000	mA
Top-Off Current Accuracy	I_{TO_ACC}	50mA setting	36		64	mA
		200mA setting	170		230	
		500mA setting	455		545	
		1000mA setting	910		1090	

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Top-Off Time	t_{TO}	Adjustable from 30sec to 70min in 10min steps; default setting is 30min		30		min
Charge Restart Threshold Setting Range	V_{RSTRT}	Adjustable at 100mV, 150mV, and 200mV; it can also be disabled	100	150	200	mV
Charge Restart Debounce Time	t_{CRDG}			130		ms
Charge State Change Interrupt Debounce Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
Charge Watchdog Time	t_{WD}			80		s
Charge Timers Accuracy	t_{ACC}		-20		+20	%
Charge-Overvoltage Threshold	V_{COV}	V_{BAT_SP} - V_{BAT_SN}, relative to $V_{CHG\_CV\_PRM}$		200		mV
Remote Sense BAT_SN Input Current in Charging Mode	$I_{BAT\_SN\_CHG}$	V_{BATT_SN} = 0, MODE = 5, T_A = +25°C		10		µA
SMART POWER SELECTOR						
System Regulation Voltage Range (Charging Enabled, Low Battery)	V_{MINSYS}	Charging enabled, V_{BATT} < V_{MINSYS} – V_{MINSYS_TRK}, Programmable by MINSYS[2:0] MODE = 5	3.0		3.7	V
System Regulation Voltage Accuracy	V_{MINSYS_ACC}	Charging enabled, V_{BATT} < V_{MINSYS} – V_{MINSYS_TRK} MODE = 5, production tested at 3.6V only	-3		3	%
System Regulation Voltage (Charging Enabled, Low Battery)	V_{MINSYS_TRK}	Charging enabled, V_{MINSYS} - V_{SYSTRK} < V_{BATT} < V_{MINSYS}, measure of V_{SYS} – V_{BATT}; MODE = 5		0.45		V
System Regulation Voltage Range (Charging Enabled, Low Battery)	$V_{SYSAICL}$	Charging enabled, V_{BATT} < $V_{SYSAICL}$ – $V_{SYSAICL\_TRK}$, Programmable by SYSAICL[4:0]; MODE = 1, 7	2.85		4.85	V
System Regulation Voltage Accuracy	$V_{SYSAICL\_ACC}$	Charging enabled, V_{BATT} < $V_{SYSAICL}$ – $V_{SYSAICL\_TRK}$ MODE = 1, 7; production tested at 3.45V and 4.85 only	-3		+3	%
System Regulation Voltage (Charging Enabled, Low Battery)	$V_{SYSAICL\_TRK}$	Charging enabled, V_{BATT} > $V_{SYSAICL}$ – $V_{SYSAICL\_TRK}$, measure of V_{SYS} – V_{BATT}; Mode = 1		V_{TRACK} – 0.15		V
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	Measure of V_{SYS} - V_{BATT}; production tested at 10mA and 2A		-60		mV
SYS Self-Discharge Resistor	R_{SYSSD}	Switching is disabled, Q_{BATT} FET is off, V_{SYS} < $V_{SYSUVLO\_F}$		600		Ω
BATTERY OVERCURRENT PROTECTION						
Battery Overcurrent Protection Quiescent Current	I_{Q_OVRC}	B2SOVRC_CTRL = 0; I_{BATT} represented in units of µA		3 + I_{BATT} / 75000		µA
Battery Overcurrent Protection Setting Range	IBOVRC	Programmable from 3A to 10A with 0.5A steps; can be disabled	3		10	A

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Overcurrent Protection Accuracy	I_{BOVRC_ACC}	B2SOVRC setting 0x4 (4.5A) and below; production tested at 3.0A setting	-15		+15	%
		B2SOVRC setting 0x5 (5A) and above; production tested at 5.0A setting	-10		+10	
Battery Overcurrent Debounce Time	t_{BOVRC}	B2SOVRC_CTRL = 1; from battery overcurrent event to BAT_I interrupt is generated		105		µs
Battery Overcurrent Delay	t_{OCP}	Delay from IRQB toggling low to Q_{BATT} FET opening (B2SOVRC_DTC = 0)		105		µs
		Delay from IRQB toggling low to Q_{BATT} FET opening (B2SOVRC_DTC = 1)		10		ms
Battery Overcurrent Retry Timer	t_{OCP_RETRY}	Retry is one time		150		ms
System Power-Up Current (from BATT)	I_{SYSPU_BAT}	V_{CHGIN} = 0V	35	50	80	mA
System Power-Up Voltage (from BATT)	V_{SYSPU_BAT}	V_{SYS} rising, 100mV hysteresis	1.9	2.0	2.1	V
System Power-Up Time-Out (from BATT)	t_{SYSPU_BAT}			150		ms
REVERSE BOOST						
Reverse Boost Quiescent Current		V_{BYP} = 5.045V, V_{BATT} = 3.8V, MODE = 0x0A, V_{BYPSET} = 0x6		2.5		mA
Reverse Boost Output Voltage Setting Range	V_{BYP_OTG}	Measured on BYP pin, 2.5V < V_{BATT} < 4.0V; adjustable from 4.505V to 10.805V with 0.09V step; production tested at 4.505V and 10.805V	4.505		10.805	V
Reverse Boost Output Voltage Accuracy	V_{BYP_ACC}	Measured on BYP, MODE = 0x0A, V_{BYPSET} = 0x0	4.355	4.505	4.655	V
Reverse Boost Inductor Current Limit	I_{LSILIM}	For MAX77786	8.5	9.5	10.5	A
		For MAX77785	5.95	7.00	8.05	
CHGIN OUTPUT LIMITER						
OTG Output Current Limit Setting Range (MAX77785)	$I_{CHGIN\_OTG\_LIM}$	Configurable from 500mA to 2400mA in 100mA steps; clamped to 10.8W power limit	500		2400	mA
OTG Output Current Limit Setting Range (MAX77786)	$I_{CHGIN\_OTG\_LIM}$	Configurable from 500mA to 3100mA in 100mA steps; clamped to 16.2W power limit	500		3100	mA
OTG Output Current Limit	$I_{CHGIN\_OTG\_LIM}$	3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x00	500	537	575	mA
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x04	900	967	1035	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x0A	1500	1612	1725	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x19 (MAX77785 only)	2400	2580	2760	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x19 (MAX77786 only)	3000	3225	3450	
OTG Output Current Limit Alarm Time	t_{OTG_ALARM}	Delay from OTG overcurrent event to BYP_I interrupt generated		20		ms
OTG Output Current Limit Fault Time	t_{OTG_FAULT}	Delay from OTG overcurrent event to Q_{CHGIN} FET opening		30		ms
OTG Output Current Limit Retry Time	t_{OTG_RETRY}	Delay from Q_{CHGIN} FET opening to Q_{CHGIN} FET closing again (OTG_REC_EN = 1)		300		ms

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH IMPEDANCES AND LEAKAGE CURRENTS						
CHGIN to BYP On Resistance at Room Temp	$R_{CHGIN2BYP\_ROOM}$	CHGIN pin to BYP pin, T_A = +25°C		14.3	18.6	mΩ
CHGIN to BYP On Resistance	$R_{CHGIN2BYP}$	CHGIN pin to BYP pin, T_A = -40°C to +85°C		14.3	22.0	mΩ
LX High-Side On Resistance at Room Temp	R_{HS_ROOM}	BYP pin to LX pin, T_A = +25°C		31.0	43.4	mΩ
LX High-Side On Resistance	R_{HS}	BYP pin to LX pin, T_A = -40°C to +85°C		31.0	54.3	mΩ
LX Low-Side On Resistance at Room Temp	R_{LS_ROOM}	LX pin to PGND pin, T_A = +25°C		14.0	20.4	mΩ
LX Low-Side On Resistance	R_{LS}	LX pin to PGND pin, T_A = -40°C to +85°C		14.0	24.0	mΩ
BATT to SYS On Resistance at Room Temp	$R_{BAT2SYS\_ROOM}$	BATT pin to SYS pin, V_{BATT} = 4.4V, T_A = +25°C		7.70	11.05	mΩ
BATT to SYS On Resistance	$R_{BAT2SYS}$	BATT pin to SYS pin, V_{BATT} = 4.4V, T_A = -40°C to +85°C		7.70	12.75	mΩ
LX Leakage Current	I_{LX_LEAK}	V_{LX} = V_{PGND} or V_{BYP}, T_A = +25°C		0.01	10	µA
		V_{LX} = V_{PGND} or VBYP, T_A = +85°C		1		
BST Leakage Current	I_{BST_LEAK}	V_{BST} - V_{LX} = 1.8V, T_A = +25°C		0.01	10	µA
		V_{BST} - V_{LX} = 1.8V, T_A = +85°C		1		
BYP Leakage Current	I_{BYP_LEAK}	V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{LX} = 0V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{LX} = 0V, charger disabled, T_A = +85°C		1		
BATSP Input Current Leakage	I_{BATSP}	Charger disabled, V_{BATSP} = V_{BATT}, T_A = +25°C		±1		µA
BATSN Input Current Leakage	I_{BATSN}	Charger disabled, V_{BATSN} = V_{AGND}, T_A = +25°C		±1		µA
LOGIC AND CONTROL I/Os						
Input Low Level	V_{IL}	SUSPND, DISQBAT, ENBST, T_A = +25°C			0.4	V
		EXTSM, T_A = +25°C, V_{HVAL} = max (V_{SYS}, V_{BATT})			0.3 x VHVAVL	
Input High Level	V_{IH}	SUSPND, DISQBAT, ENBST, T_A = +25°C	1.4			V
		EXTSM, T_A = +25°C	0.7 x VHVAL			
Input Leakage Current	ILK	SUSPND, DISQBAT, ENBST, EXTSM pin, at 5.5V (including current through pulldown resistor)		24	60	µA
Output Low Voltage QBEXT	$V_{OLQBEXT}$	Sourcing 1mA, T_A = +25°C			0.4	V
Output High Leakage QBEXT	I_{LQBEXT}	V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUSPND Internal Pulldown Resistor	R_{SUSPND}			235		kΩ
DISQBAT Internal Pulldown Resistor	$R_{DISQBAT}$			235		kΩ
EXTSM Internal Pullup Resistor	R_{EXTSM}			235		kΩ
ENBST Internal Pulldown Resistor	R_{ENBST}			235		kΩ
EXTSM Debounce Time	t_{EXTSM_DEB}	V_{BATT} in 3.3V to 4.5V range, EXTSM_T = 0		10		ms
		V_{BATT} in 3.3V to 4.5V range, EXTSM_T = 1		0.1		
CHARGE STATUS INDICATOR						
Charge Status Current Setting Range	I_{STAT_RNG}	5mA to 20mA in 5mA steps; production tested at $V_{STAT} - V_{AGND}$ = 1.0V and 5.0V	5		20	mA
Charge Status Current Accuracy	I_{STAT_ACC}	Production tested at 5mA and 20mA	-20		+20	%
THERMISTOR MONITOR						
THM Threshold, COLD	THM_COLD	V_{THM}/V_{PVDD} rising, 0.5% hysteresis (thermistor temperature falling)	73.8	75.0	76.2	%
THM Threshold, COOL	THM_COOL	V_{THM}/V_{PVDD} rising, 0.5% hysteresis (thermistor temperature falling)	64.3	65.5	66.7	%
THM Threshold, WARM	THM_WARM	V_{THM}/V_{PVDD} falling, 1% hysteresis (thermistor temperature rising)	30.8	32.0	33.2	%
THM Threshold, HOT	THM_HOT	V_{THM}/V_{PVDD} falling, 1% hysteresis (thermistor temperature rising)	20.8	22.0	23.2	%
THM Threshold, Disabled	THM_DIS	V_{THM}/V_{PVDD} falling, 1% hysteresis, THM function is disabled below this voltage	4.8	6.0	7.2	%
THM Threshold, Battery Removal Detection	THM_RM	V_{THM}/V_{PVDD} rising, 0.5% hysteresis, battery removal	85	87	89	%
THM Input Leakage Current	I_{LKTHM}	$V_{THM} = V_{AGND}$ or V_{PVDD}, charger disabled, T_A = +25°C		0.1	1	μA
		$V_{THM} = V_{AGND}$ or V_{PVDD}, charger disabled, T_A = +85°C		0.1		
SUPPLIES AND MONITORING						
VDD Output Voltage	V_{VDD_1P8}	V_{SYS} or V_{BATT} = 3.8V, I_{VDD} = 20mA	1.71	1.80	1.89	V
SYS Undervoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_UVLO\_R}$		2.74	2.80	2.86	V
SYS Undervoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_UVLO\_F}$		2.55	2.60	2.65	V
SYS Undervoltage-Lockout Hysteresis	$V_{SYS\_UVLO\_H}$			200		mV
SYS Overvoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_OVLO\_R}$	SYS rising	5.40	5.45	5.50	V
SYS Overvoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_OVLO\_F}$	SYS falling	5.26	5.31	5.36	V

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Overvoltage-Lockout Hysteresis	$V_{SYS\_OVLO\_H}$			140		mV
Thermal Shutdown Threshold	T_{SHDN_R}	T_j rising		155		°C
Thermal Shutdown Threshold Hysteresis	T_{SHDN_H}			15		°C
Thermal Warning Threshold	T_{WARN}			T_{REG} + 12		°C
PVDD Output Voltage	V_{PVDD_1P8}	V_{SYS} = 3.8V, I_{PVDD} = 20mA	1.71	1.80	1.89	V
USB ANALOG SWITCH (DP/DN/DP1/DN1)						
Analog Signal Range	V_{DPx}/V_{DNx}		0		Min(SYS, BAT)	V
On-Resistance	R_{ONUSB}			3.7	6.5	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	V_{SYS} = 3.0V, I_{DN} / I_{DP} = 10mA, V_{DN} / V_{DP} = 400mV			0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$			0.1	0.4	Ω
Off Leakage Current	$I_{LUSBOFF}$		-360		+360	nA
Analog Switch Turn-On Time	t_{ON}	I²C stop to Switch On; R_L= 50Ω		0.1	0.4	ms
Analog Switch Turn-Off Time	t_{OFF}	I²C stop to Switch Off; R_L = 50Ω		0.1	0.4	ms
DN, DP On Capacitance	C_{ON}	Freq. = 200MHz		5		pF
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, V_{DP}, V_{DN} = 0dBm, DC Bias = 350mV		500		MHz
Off Isolation at 10MHz	V_{ISO}	R_L = 50Ω, V_{DP}, V_{DN} = 0dBm, DC Bias = 350mV		-41		dB
Off Isolation at 240MHz	V_{ISO}	R_L = 50Ω, V_{DP}, V_{DN} = 0dBm, DC Bias = 350mV		-15		dB
USB BC1.2 / CHARGER DETECTION						
BC1.2 State Timeout	t_{TMO}		180	200	220	ms
Data Contact Detect Timeout	t_{DCDtmo}	DCDCpl = 0b1 (default)	700	800	900	ms
		DCDCpl = 0b0	1800	2000	2200	
Primary to Secondary Timer	$t_{PDSWait}$		27	35	39	ms
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
V_{BUS64} Threshold	V_{BUS64}	DP and DN pins, Threshold in percent of V_{BUS} voltage; 3V < V_{BUS} < 5.5V	57	64	71	%
V_{BUS64} Hysteresis	V_{BUS64_H}			0.015		V
V_{BUS47} Hysteresis	V_{BUS47}	DP and DN pins, Threshold in percent of V_{BUS} voltage; 3V < V_{BUS} < 5.5V	43.3	47	51.7	%
	V_{BUS47_H}			0.015		V
V_{BUS31} Hysteresis	V_{BUS31}	DP and DN pins, Threshold in percent of V_{BUS} voltage; 3V < V_{BUS} < 5.5V	26	31	36	%
	V_{BUS31_H}			0.015		V
R_{DM_DWN} Resistor	R_{DM_DWN}		14.25	20	24.8	kΩ
IDP_SRC Current	$I_{DP\_SRC/IDCD}$	Accurate over 0V to 2.5V	7	10	13	µA

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

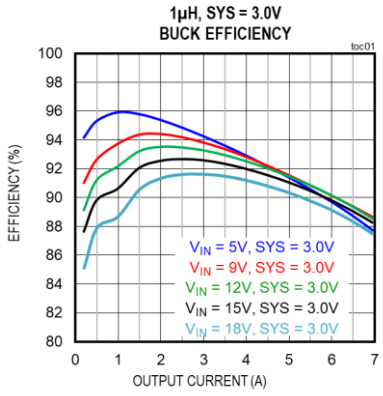
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDM_SINK Current	I_{DM_SINK}/I_{DAT_SINK}	Accurate over 0.15V to 3.6V	65	80	95	µA
V_{LGC} Threshold	V_{LGC}		1.62	1.7	1.9	V
V_{LGC} Hysteresis	V_{LGC_H}			0.015		V
V_{DAT_REF} Threshold	V_{DAT_REF}		0.25	0.32	0.4	V
$V_{DAT\_REF\_Hysteresis}$	$V_{DAT\_REF\_H}$			0.015		V
OVDX Comparator Falling Threshold	V_{OVDX_THF}	Falling DP/DN threshold	3.6			V
OVDX Comparator Rising Threshold	V_{OVDX_THR}	Rising DP/DN threshold			4	V
OVDX Comparator Hysteresis	V_{OVDX_HYS}	DP/DN Hysteresis between rising and falling		50		mV
DN/DP Load Resistor	RUSB	Load resistor on DP/DN	3	6.1	12	MΩ
VD33 Voltage	V_{DP}/DM_3p3V SRC/VSRC33	Tested at zero load and 200µA load	2.6	3.0	3.3	V
$V_{SRC33ILIM}$ Current Limit	$I_{LIMVSRC33}$	Force 1.6V on DP/DN, measure current		1.5	3	mA
V_{DN_SRC} Voltage	$V_{DN\_SRC/VSRC06}$	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DP_SRC} Voltage	$V_{DP\_SRC/VSRC06}$	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
USBC FRS						
V_{SAFE5V} MAX Rising Threshold	$V_{SAFE5V\_max\_R}$	Rising			5.5	V
V_{SAFE5V} MAX Falling Threshold	$V_{SAFE5V\_max\_F}$	Falling	5.2			V
I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Set-Up time	$t_{SU;DAT}$		50			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			50		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF)						

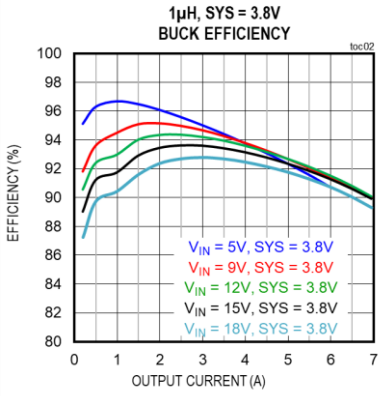
(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V)

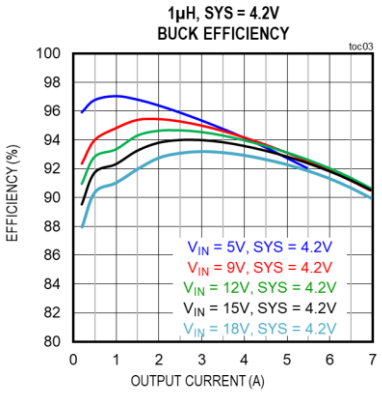
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency	f_{SCL}				3.4	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			10		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			10		ns

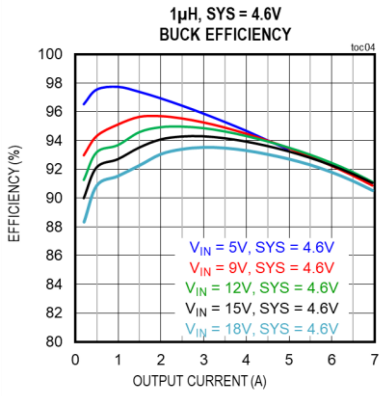
Typical Operating Characteristics

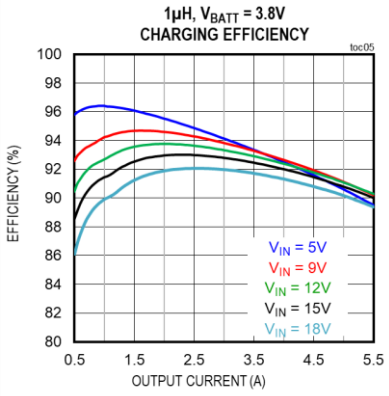
(T_A = +25°C, unless otherwise noted.)

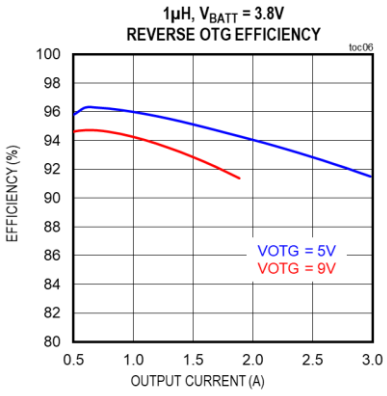








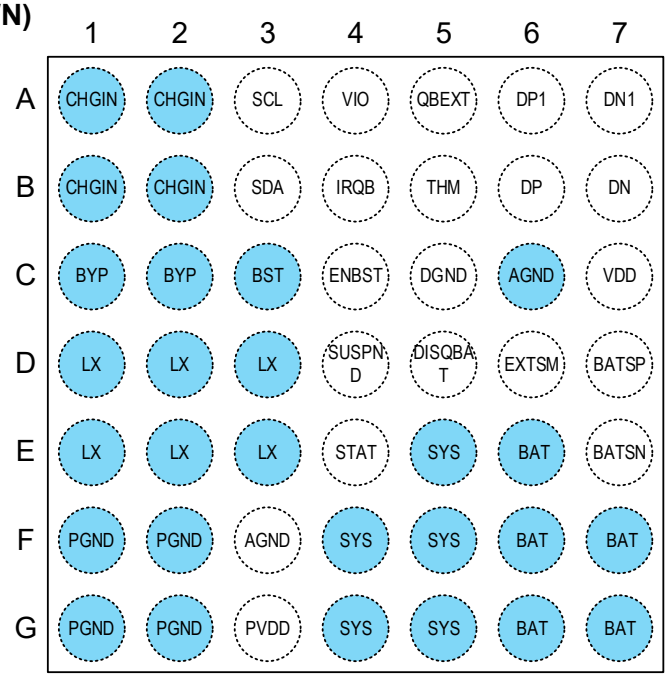




Pin Configurations

TOP VIEW
(BUMP SIDE DOWN)

MAX77785
MAX77786



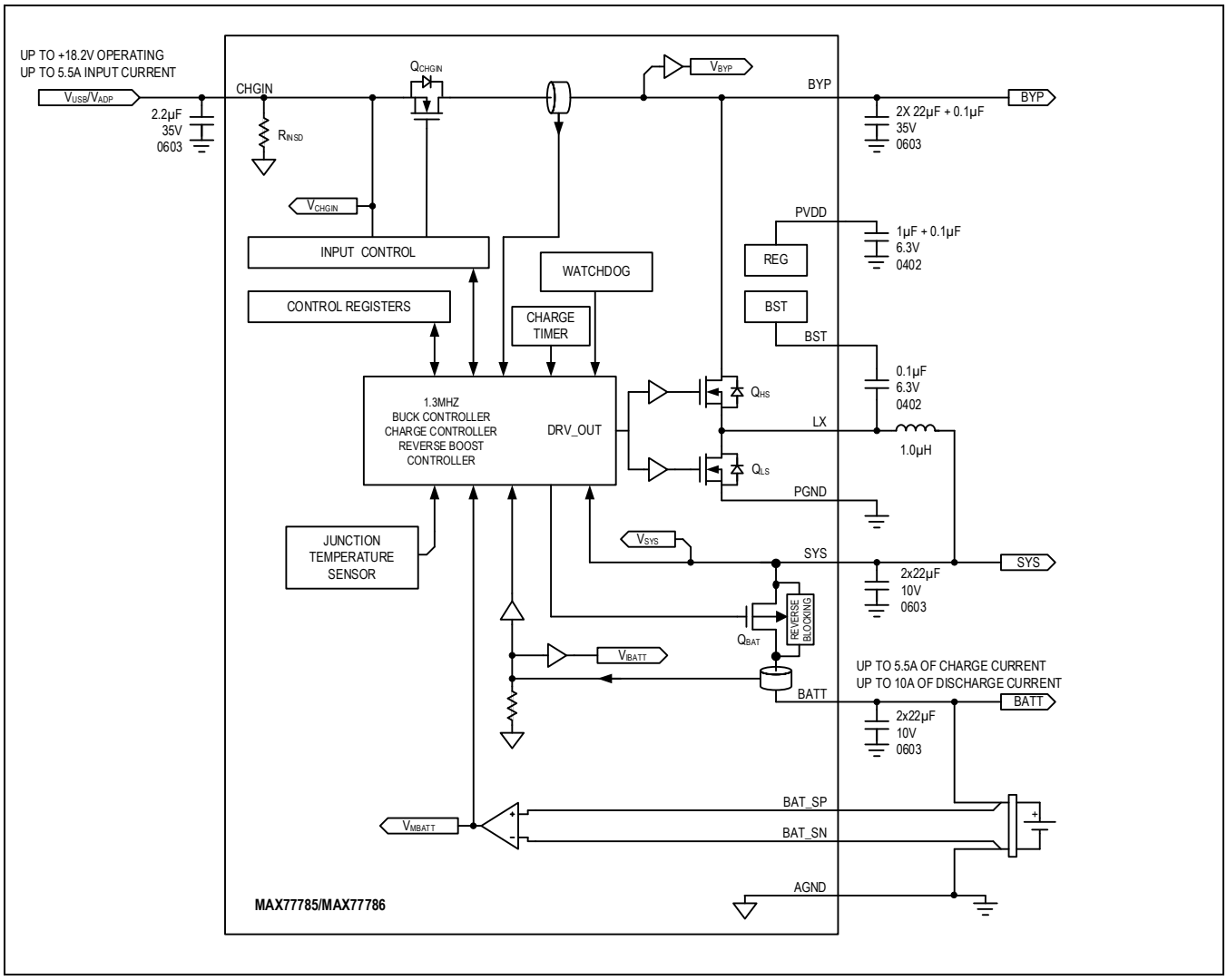
(2.96mm X 2.96mm WLP)

Pin Descriptions

PIN	NAME	FUNCTION	Type
B6	DP	Common Positive Output. Connect to D+ in USB connector.	A
B7	DN	Common Negative Output. Connect to D+ in USB connector.	A
A6	DP1	USB Input 1 for D+	A
A7	DN1	USB Input 1 for D-	A
D5	DISQBAT	Active-high to disable internal Q_{BATT} FET between SYS and BATT.	DI
B5	THM	Thermistor Connection. Connect an external thermistor between THM and AGND.	A
C7	VDD	Analog Voltage Level. The output of on-chip low voltage LDO is used to power on-chip, low-noise circuits. Bypass with a 1µF (6.3V) ceramic capacitor to AGND. Powering external loads from VDD is not recommended, other than pullup resistors.	A
E7	BATSN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal as close as possible.	A
D7	BATSP	Battery Positive Differential Sense Pin. Connect to battery positive terminal as closely as possible to eliminate errors due to trace/connector voltage drops.	A
E6, F6, F7, G6, G7	BATT	Connection with Battery. Connect to the positive terminal of a single-cell Li-ion battery. Bypass with a 10µF (6.3V) ceramic capacitor from BATT to PGND.	P

E5, F4, F5, G4, G5	SYS	Connection with System. Bypass with at least 2x 22µF (6.3V) ceramic capacitors from SYS to PGND. This ensures that the minimum effective capacitance on the SYS node is 12µF (effective), for stability purposes. For application purposes, SYS node capacitance can increase up to 350µF total (effective). If BCKSYS is set to ≥ 4.5V, then it requires at least 100µF in addition to the default 2x 22µF.	P
G3	PVDD	Internal Bias Regulator High Current Output Bypass Pin. Supplies internal noisy and high current gate drive loads. Bypass with a 1µF + 0.1µF (6.3V) from PVDD to PGND. Powering external loads from PVDD is not recommended, other than pullup resistors.	P
C5	DGND	Digital Ground	A
F1, F2, G1, G2	PGND	Charger Power Ground	P
D1, D2, D3, E1, E2, E3	LX	Charger Switching Node. Connect the inductor between LX and SYS.	P
C3	BST	High-Side FET Driver Supply. Bypass BST to LX with a 1x 100nF (6.3V) ceramic capacitor.	A
C1, C2	BYP	CHGIN Bypass Pin. This pin is the input for the switching charger and the output for the boost converter when the charger is operating in reverse-boost mode. Bypass with 2x 22µF + 0.1µF (35V) ceramic capacitors from BYP to PGND.	P
A1, A2, B1, B2	CHGIN	Charger Input. Connect 1x 2.2µF (35V) between CHGIN and PGND.	P
A3	SCL	I^2C Interface Clock Input	DI
B3	SDA	I^2C Interface Data Input	DI
D6	EXTSM	Exit Ship Mode Input by Push-Button. Active-low input.	DI
A4	VIO	I^2C Supply Voltage Input. Bypass to AGND with a 0.1µF (6.3V) capacitor.	P
C6, F3	AGND	Analog Ground	A
E4	STAT	LED Low-Side Driver Output for Indicating Charging Status	A
A5	QBEXT ($\overline{PGOOD}$)	When UNPLUG_TH = 0x00, this pin is configured to QBEXT which is the External Battery FET Control Output. Connect a pullup resistor to VIO, SYS, or BATT supply. When UNPLUG_TH≠ 0x00, this pin is configured to $\overline{PGOOD}$ which is the unplug detection comparator output.	DO
D4	SUSPND	Active-High Input to Disable the DC-DC Between CHGIN Input and SYS Output	DI
B4	IRQB	Interrupt Output. Connect a 100kΩ pullup resistor between IRQB and VIO.	DO
C4	ENBST	Active-High Input to enable the Reverse Boost operation during a Fast Role Swap event only. For more details, see the *Fast Role Swap Implementation Considerations* section.	DI

Functional Diagrams



Detailed Description

Switching Mode Charger

Features

- Complete Li+/LiPoly/LiFePO$_4$ Battery Charger
  - Prequalification, Constant Current, and Constant Voltage
  - 55mA Precharge Current
  - 300mA Trickle Charge Current
  - Adjustable Constant Current Charge
    - 50mA to 5.5A in 50mA Steps
  - Adjustable Charge-Termination Threshold
    - 50mA to 1000mA in 50mA Steps
  - Adjustable Battery Regulation Voltage
    - 3.5V to 4.6V in 10mV Steps
    - -0.6%/+0.0% Accuracy from -5°C to +85°C
    - Remote Differential Sensing
- Synchronous Switch-Mode-Based Design
- Smart Power Selector
  - Optimally distributes power between the charge adapter, system, and battery.
  - When powered by a charge adapter, the battery can provide supplemental current to the system.
  - The charge adapter can support the system with a dead battery or without a battery.
- No External MOSFETs Required for Switcher
- CHGIN Input
  - Adjustable Input Current Limit
    - 50mA to 5.5A in 50mA steps (CHGIN_ILIM) – MAX77786
    - 50mA to 3.5A in 50mA steps (CHGIN_ILIM) – MAX77785
    - Default is set to 500mA
  - Supports AC-to-DC Wall Adapters
  - V_{CHGIN_OVLO} = 18.2V
  - Reverse-Leakage Protection Prevents the Battery Leaking Current to the Inputs
- Charge Safety Watchdog Timer
  - Selectable: 3hr to 10hr, plus a Disable Setting
- Die Temperature Monitor with Thermal Foldback Loop
  - Selectable Die-Temperature Thresholds (°C): +86°C to +128°C in +6°C Steps
- Input Voltage Dropout Control Allows Operation from High-Impedance Sources (AICL)
- BATT to SYS Switch is 7.7mΩ (Typ)
  - Capable of 10A Steady-State Operation from BATT to SYS
- Short-Circuit Protection
  - Programmable BATT to SYS Overcurrent Threshold from 3A to 10A, plus a Disable Setting
  - DISIBS bit allows the host to disable the battery to the system discharge path to protect against a short circuit.

- SYS Short to Ground
  - Buck current is limited by the switcher current limit and disabling of the synchronous rectifier.
  - BATT currents above the programmed B2SOVRC threshold generate an interrupt. The host can then disable the battery to the system discharge path by setting DISIBS or asserting the DISQBAT pin high.
- Programmable Unplug Detection Output
- Spread Spectrum Modulation for Reduced EMI

Detailed Description

The MAX77785/MAX77786 includes a full-featured switch-mode charger for a one-cell lithium-ion (Li+), lithium-polymer (Li-polymer) battery, or $LiFePO_4$ battery. The current limit for CHGIN input is independently programmable allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port.

The synchronous switch-mode DC-DC converter utilizes a high 1.3MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery, the converter operates as a buck. The DC-DC buck operates from a 4.7V to 18.2V source. The battery charge current is programmable from 50mA to 5.5A.

As a boost converter, the DC-DC uses energy from the main battery to boost the voltage at BYP. The BYP supplies the USB OTG voltage and USB Type-C® PD Source Voltages (5V to 9V). The programmable boost output current limit range is from 0.5A to 3.1A with a 0.1A step.

The Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up-to-buck current limit from the buck to the system. (Additionally, supplement mode provides additional current from the battery to the system up to B2SOVRC.) Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between the battery and adapter power are included on-chip—no external MOSFETs are required.

A multitude of safety features ensures reliable charging. Features include a charge timer, watchdog, junction thermal regulation, over/under voltage protection, and short circuit protection.

The BATT to SYS switch has overcurrent protection (see the *Main-Battery Overcurrent Protection Due to Fault* section for more information).

Table 1. Recommended Buck Output Current Range

	MINIMUM SYS CURRENT (A)	MAXIMUM SYS CURRENT (A)
MAX77785	0	4.5
MAX77786	0	7

Smart Power Selector (SPS)

The SPS architecture is a network of internal switches and control loops that distribute energy between external power sources CHGIN, BYP, SYS, and BATT.

The *Simplified Functional Diagram* shows a simplified arrangement for the Smart Power Selector's power steering switches. *Figure 1* shows a more detailed arrangement of the Smart Power Selector switches and gives them the following names: Q_{CHGIN}, Q_{HS}, Q_{LS}, and Q_{BATT}.

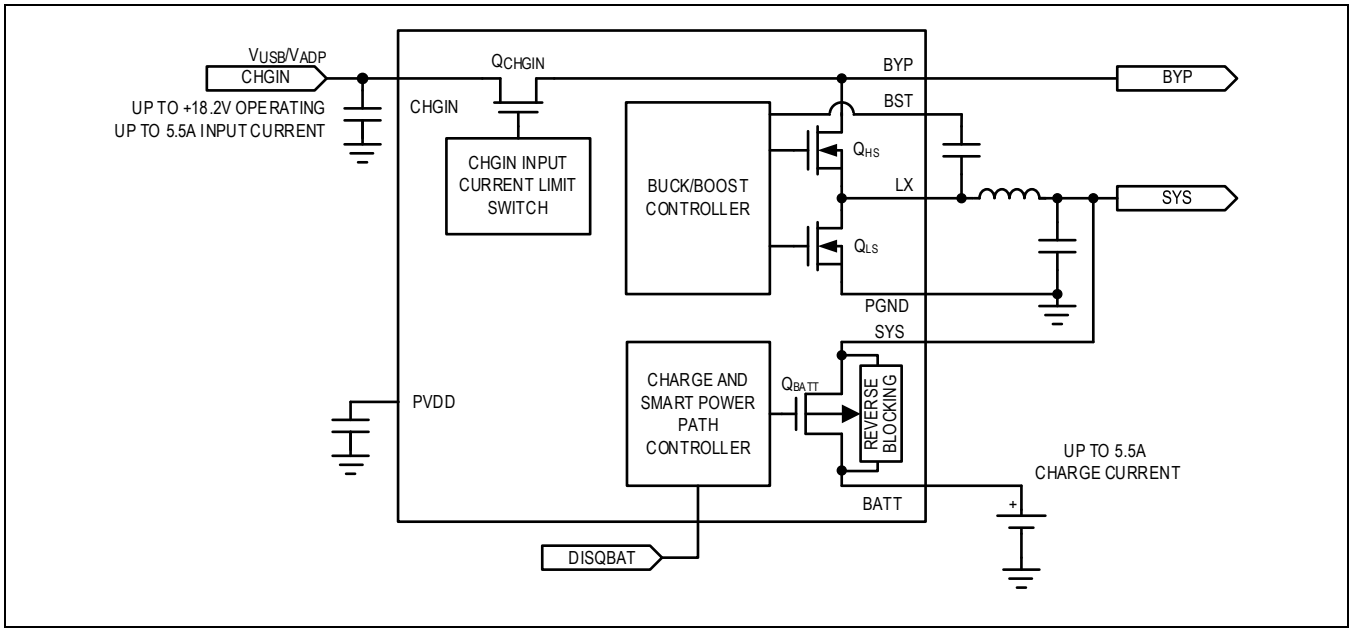


Figure 1. Smart Power Selector Functional Diagram

Switch and Control Loop Descriptions

- CHGIN Input Switch: The input switch is either completely on or completely off. As shown in *Figure 1*, there are SPS control loops that monitor the current through the input switches as well as the input voltage.
- DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.
- Battery-to-System Switch: Q_{BATT} controls the battery charging and discharging. Additionally, Q_{BATT} allows the battery to be isolated from the system (SYS). An SPS control loop monitors the Q_{BATT} current.

Control Bits

- MODE configures the Smart Power Selector
- V_{BYPSET} sets the BYP regulation voltage target
- B2SOVRC configures the main-battery overcurrent protection

Energy Distribution Priority

- With a valid external power source:
  - The external power source is the primary source of energy
  - The main battery is the secondary source of energy
  - Energy delivery to BYP is the highest priority
  - Energy delivery to SYS is the second priority
  - Any energy that is not required by BYP or SYS is available to the main battery charger.
- With no power source available at CHGIN:
  - The main battery is the primary source of energy
  - Energy delivery to BYP (if boost mode is selected) and SYS share the same priority
  - BYP includes CHGIN if boost OTG mode is selected, itself limited by the OTG_ILIM threshold
  - Energy delivery to BYP (if boost mode is selected) and SYS is limited by the B2SOVRC threshold

BYP Regulation Voltage

- When the DC-DC is off or in one of its buck modes and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times R_{CHGIN2BYP}$.
- When the DC-DC is off and there is no valid power source at CHGIN, BYP is connected to LX through the high-side switch's body diode.

SYS Regulation Voltage

- In MODE 0x4, the DC-DC is enabled as a Buck and the charger is disabled, Q_{BAT} is off and V_{SYS} is regulated by the BCKSYS register as shown in *Figure 2*.

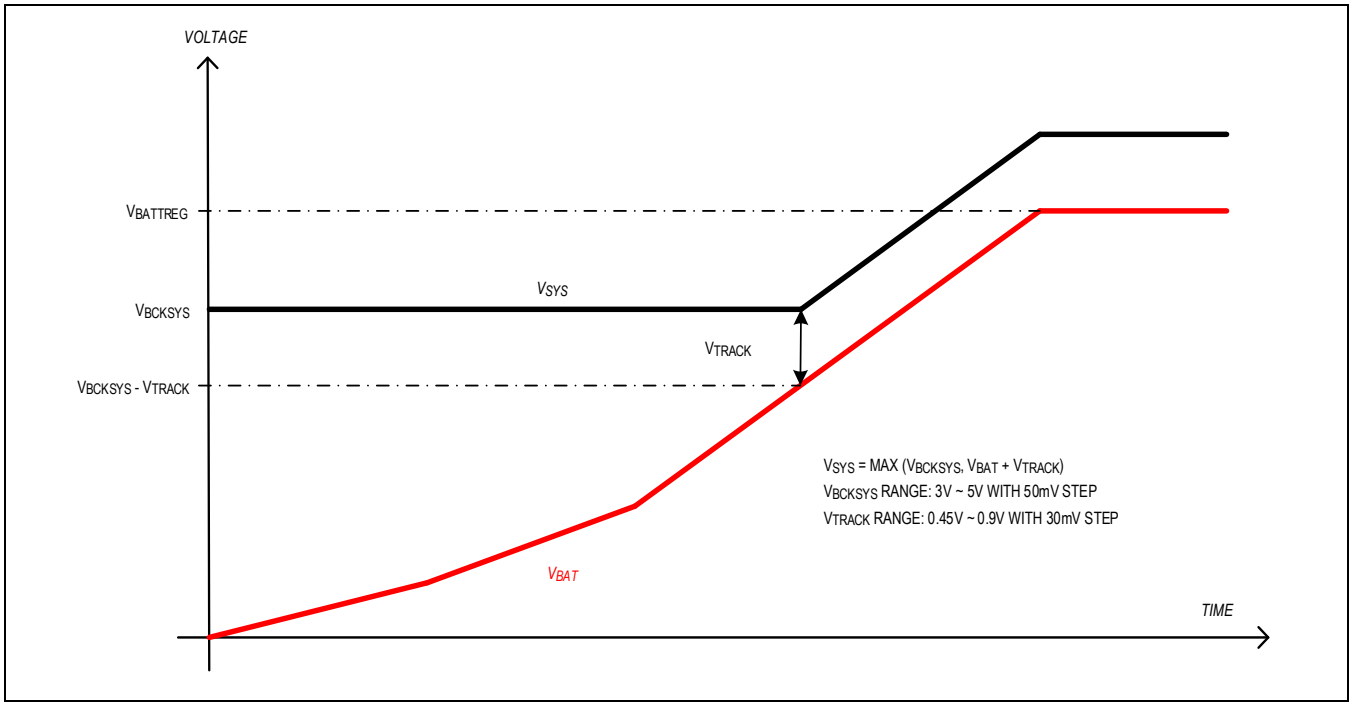


Figure 2. MODE 0x4

- In MODE 0x5, the DC-DC is enabled as a Buck, and the charger is enabled. V_{SYS} is regulated by the MINSYS register. Q_{BAT} is off in a non-charging state such as Done, Suspend (by thermistor, watchdog, or timer fault)
    - V_{MINSYS} must be lower than $V_{BATTREG}$. But by accident, V_{MINSYS} (chosen by MINSYS bits) can be selected higher than $V_{BATTREG}$ (chosen by CHG_CV_REG bits). So, in this case, the state machine provides the automatic correction feature as follows:
        - If V_{MINSYS} > $V_{BATTREG}$-200mV, then the state machine clamps V_{MINSYS} to $V_{BATTREG}$-200mV.
        - For instance, 3.6V is selected as $V_{BATTREG}$, and 3.6V is also selected as V_{MINSYS}, then the V_{MINSYS} clamps at 3.4V by the state machine sets MINSYS to 3.4V value.
    - TRACK should be selected carefully with CHG_CV_PRM so that V_{TRACK} + $V_{BATTREG}$ < $V_{SYS\_OVLO\_F}$. There should be some margin between V_{TRACK} + $V_{BATTREG}$ and $V_{SYS\_OVLO\_F}$ considering transient overshoot and BAT_SN voltage.

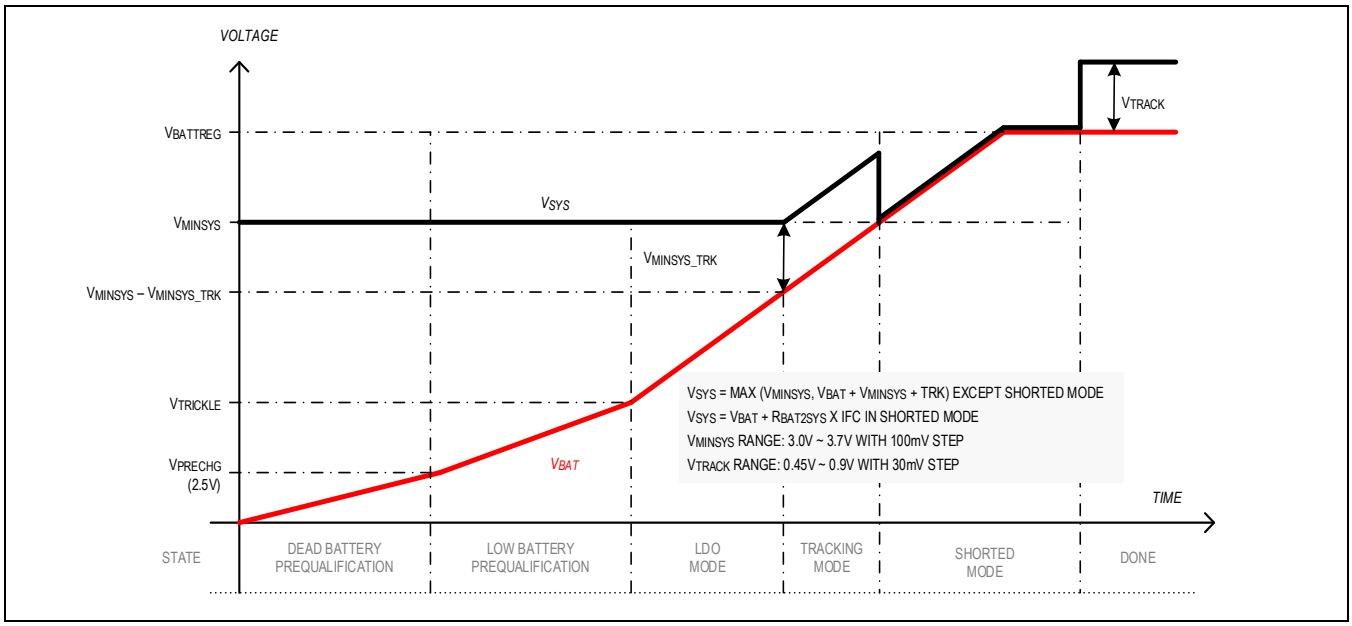


Figure 3. MODE 0x5

- In MODE 0x7, the DC-DC is enabled as a Buck, and the charger is enabled. V_{SYS} is regulated by the BCKSYS register. Q_{BAT} operates as a linear charger. In the dead battery prequalification region and done region, the SYSAICL interrupt would not be generated.

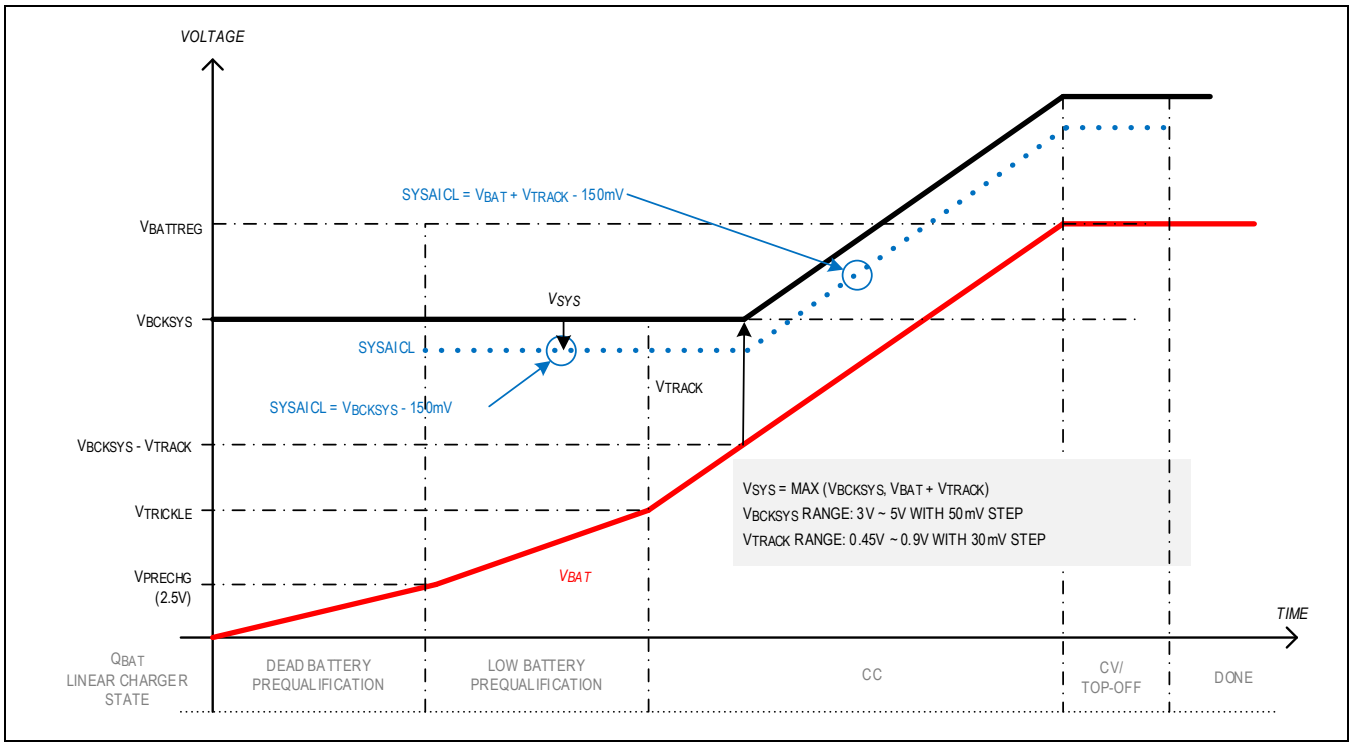


Figure 4. MODE 0x7

- In all the above modes, if the combined SYS and BYP loading exceeds the input current limit, then V_{SYS} drops to V_{BATT} - V_{BSREG} and the battery provides supplemental current.
- In MODE 0x1, the V_{SYS} needs to be regulated by an external converter. Q_{BAT} operates as a linear charger as MODE 0x7. SYSAICL has to be set at 150mV lower than the external SYS voltage so that the SYSAICL interrupt is generated properly to inform that the application processor increases the external SYS voltage. In the dead battery prequalification region and done region, the SYSAICL interrupt would not be generated.
- In the MODE 0x1 case, the SYS exceeds the current limits of the external converter, and V_{SYS} drops to V_{BATT} - V_{BSREG} then the battery provides supplemental current.

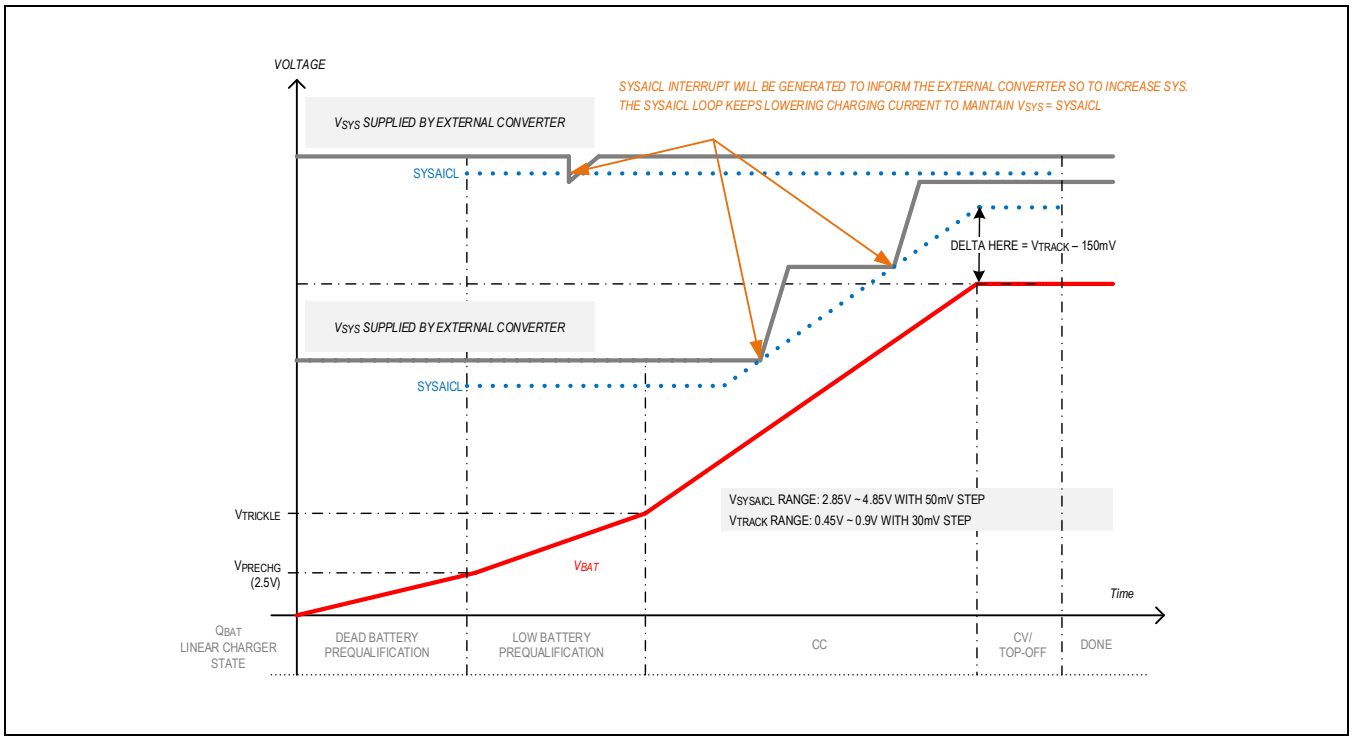


Figure 5. MODE 0x1

- When the DC-DC is enabled as a boost, then the Q_{BATT} switch is closed, and V_{SYS} = V_{BATT} - I_{BATT} x RBAT2SYS

Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following four characteristics to be valid:

- CHGIN must be above V_{CHGIN_UVLO} to be valid. Once CHGIN is above the UVLO threshold, the information (together with IN2SYS, described below) is latched and can only be reset when the charger is in an adaptive input current loop (AICL) and the input current is lower than the IULO_DET threshold.
- CHGIN must be below its overvoltage-lockout threshold (V_{CHGIN_OVLO}).
- CHGIN must be above the system voltage by IN2SYS dropout.
- CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read with CHGIN_OK and CHGIN_DTLS. Interrupts can be masked with CHGIN_M.

Input Current Limit

The default settings of the CHGIN_ILIM and MODE control bits are such that when a charge source is applied to CHGIN, the IC turns its DC-DC converter on in BUCK mode, limits V_{SYS} to V_{SYSREG_TRK}, and limits the charge source current to $I_{INLIMIT}$. All control bits are reset on global shutdown.

Input Voltage Regulation Loop

An input voltage regulation loop allows the charger to be well-behaved when it is attached to a poor-quality charge source. The loop improves performance with relatively high resistance charge sources that exist when long cables are used, or devices are charged with non-compliant USB hub configurations. Additionally, this input voltage regulation loop improves performance with current-limited adapters. If the IC input current limit is programmed above the current-limit threshold of a given adapter, the input voltage loop allows the IC to regulate at the current limit of the adapter. Finally, the input-voltage regulation loop allows the IC to perform well with adapters that have poor transient load response times.

The input voltage regulation loop automatically reduces the inductor average current to keep the input voltage at V_{CHGIN_REG}. If the input current is reduced to I_{ULO_DET} and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off. V_{CHGIN_REG} is programmable with V_{CHGIN_REG}[1:0].

After operating with the input voltage regulation loop active, an AICL_I interrupt is generated, and AICL_OK sets to 0. To optimize input power when working with a current limited charge source, monitor the AICL_OK status while decreasing the input current limit. When the input current limit is set below the limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage is allowed to rise.

Example 1. Optimum use of the Input Voltage Regulation Loop along with a current-limited adapter.

Sequence of events:

1. V_{BATT} = 3.2V, the system is operating normally.
2. MODE = 0x04, CHGIN_ILIM = 100mA, CHG_CV_PRM = 4.2V, V_{CHGIN_REG} = 4.5V, CHG_CC_TOT = 2.0A.
3. A 5.0V 1.2A current limited dedicated USB charger is applied to CHGIN.
4. The DC-DC buck regulator turns on, V_{SYS} is regulated to $V_{BATTREG}$ (4.2V) and the input is allowed to provide 100mA to the system.
5. The system detects that the charge source is a dedicated USB charger and enables the battery charger (MODE = 0x05) and programs an input current limit to 1.8A (CHGIN_ILIM = 1.8A).
6. The input current limit starts to ramp up from 100mA to 1.8A, but at the input current limit of the adapter (1.2A), the adapter voltage collapses. The ICs input voltage regulation loop prevents the adapter voltage from falling below 4.5V (V_{CHGIN_REG} = 4.5V). An AICL_I interrupt is generated and AICL_OK sets to 0.
7. With the input-voltage regulation loop active, the adapter provides 1.2A at 4.5V which is a total of 5.4W being delivered to the system.
8. The system software detects that the input voltage regulation loop is active, and it begins to ramp down the programmed input current limit. When the current limit ramps down to 1.175A, the adapter is no longer in the current limit, and the adapter voltage increases from 4.5V to 5.0V.
9. With the adapter operating just below its current limit, it provides 1.175A at 5.0V which is a total of 5.88W to the system. This is 440mW more than when the adapter was in the current limit.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the ICs actively discharge the SYS nodes when Q_{BATT} and switcher are disabled and V_{SYS} is less than $V_{SYSUVLO}$. As shown in *Figure 6*, the SYS discharge resistor is 600Ω.

Example 1. Basic System Self-Discharge

Initial Conditions: No charger adapter is present at CHGIN, the BAT-to-SYS switch is closed, C_{BAT} = 100µF, C_{SYS} = 200µF, V_{BATT} = 3.6V, and $V_{SYSUVLO}$ falling is SYS_UVLOB_F.

Sequence of Events:

1. With the system in its normal operating mode it is drawing 1A.
2. The main battery is removed.
3. The system continues to draw 1A until V_{SYS} falls below $V_{SYSUVLO}$. This takes 480µs ((3.6V-2.0V)/1A x 300µF).
4. When the system voltage falls below $V_{SYSUVLO}$, the system turns off the leakage current. To facilitate discharging C_{BAT} and C_{SYS} the IC engages its 600Ω discharge resistors.

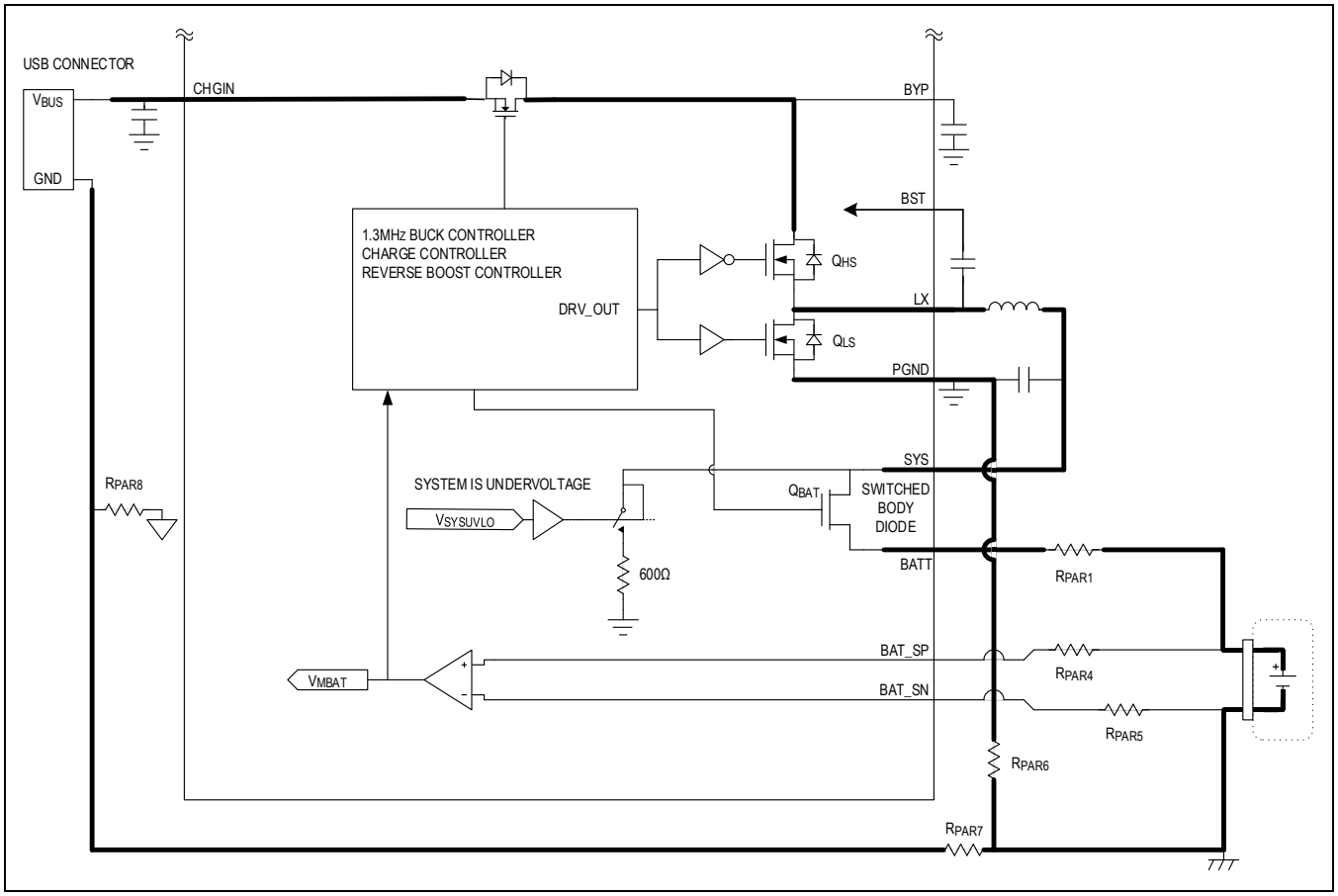


Figure 6. System Self-Discharge Circuit

Power States

The MAX77785/MAX77786 transitions between power states as input/battery and load conditions dictate; see *Figure 7*.

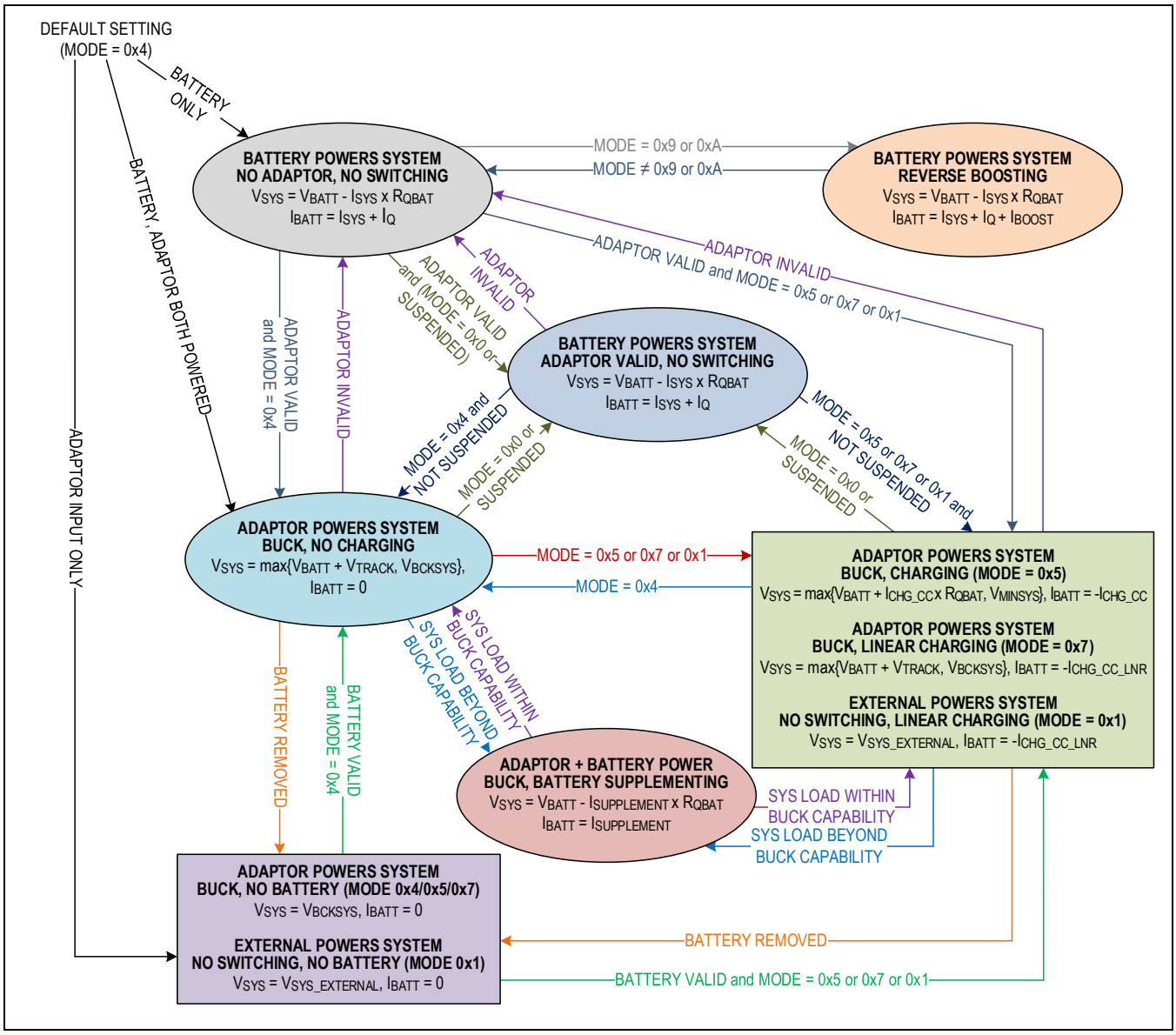


Figure 7. Power State Diagram

The IC provides five (5) power modes and one (1) no power mode (MODE detailed description is at register CHG_CNFG_00 [3:0]). Under power-limited conditions, the PowerPath™ feature maintains SYS load at the expense of battery charge current. Also, the battery supplements the input power when required. As shown, transitions between power states are initiated by the detection/removal of valid power sources, OTG events, and undervoltage conditions. Details of the SYS voltage and BATT current are provided for each state. There are six main usage modes:

1. NO INPUT POWER, MODE = undefined: No input adapter or battery is detected. The charger and system are off. The battery is disconnected, and the charger is off.
2. BATTERY-ONLY, MODE = any modes: The Adapter is invalid and outside the input voltage operating range (Q_{CHGIN} = OFF). The battery is connected to power the SYS load (Q_{BATT} = ON).
3. External SYS-Linear Charge, MODE = 0x01: The adapter is valid, but the external converter supplies power to SYS. INPUT FET and BUCK are disabled. QBAT works as a linear charger with supplement mode.
4. NO CHARGE-BUCK, MODE = 0x04: The adapter is valid, buck supplies power to SYS. The battery is disconnected (Q_{BATT} = OFF) when the SYS load is less than the power that the buck can supply.

   When the SYS load is larger than the power that the buck can supply, the battery is reconnected (Q_{BATT} = ON) and supplements the extra SYS load.
5. CHARGE-BUCK, MODE = 0x05: The adapter is valid, the buck supplies power to SYS by MINSYS with tracking and charges the battery with I_{BATT}.
6. CHARGE-QBAT, MODE = 0x07: The adapter is valid, the buck supplies power to SYS by BCKSYS with tracking, and charges the battery with QBAT (as a linear charger)
7. BATTERY-BOOST (FLASH), MODE = 0x09: OTG is inactive (Q_{CHGIN} = OFF). The battery is connected to support SYS and BYP loads (Q_{BATT} = ON), and the charger is operating in boost mode (Boost = ON).
8. BATTERY-BOOST (OTG), MODE = 0x0A: OTG is active (Q_{CHGIN} = ON). The battery is connected to support SYS and OTG loads (Q_{BATT} = ON), and the charger is operating in boost mode (Boost = ON).

Charger States

The ICs utilize several charging states to safely and quickly charge batteries as shown in *Figure 8*. The figure shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature. It shows a complete charging state transition process with four states: prequalification, fast-charge, top-off, and done.

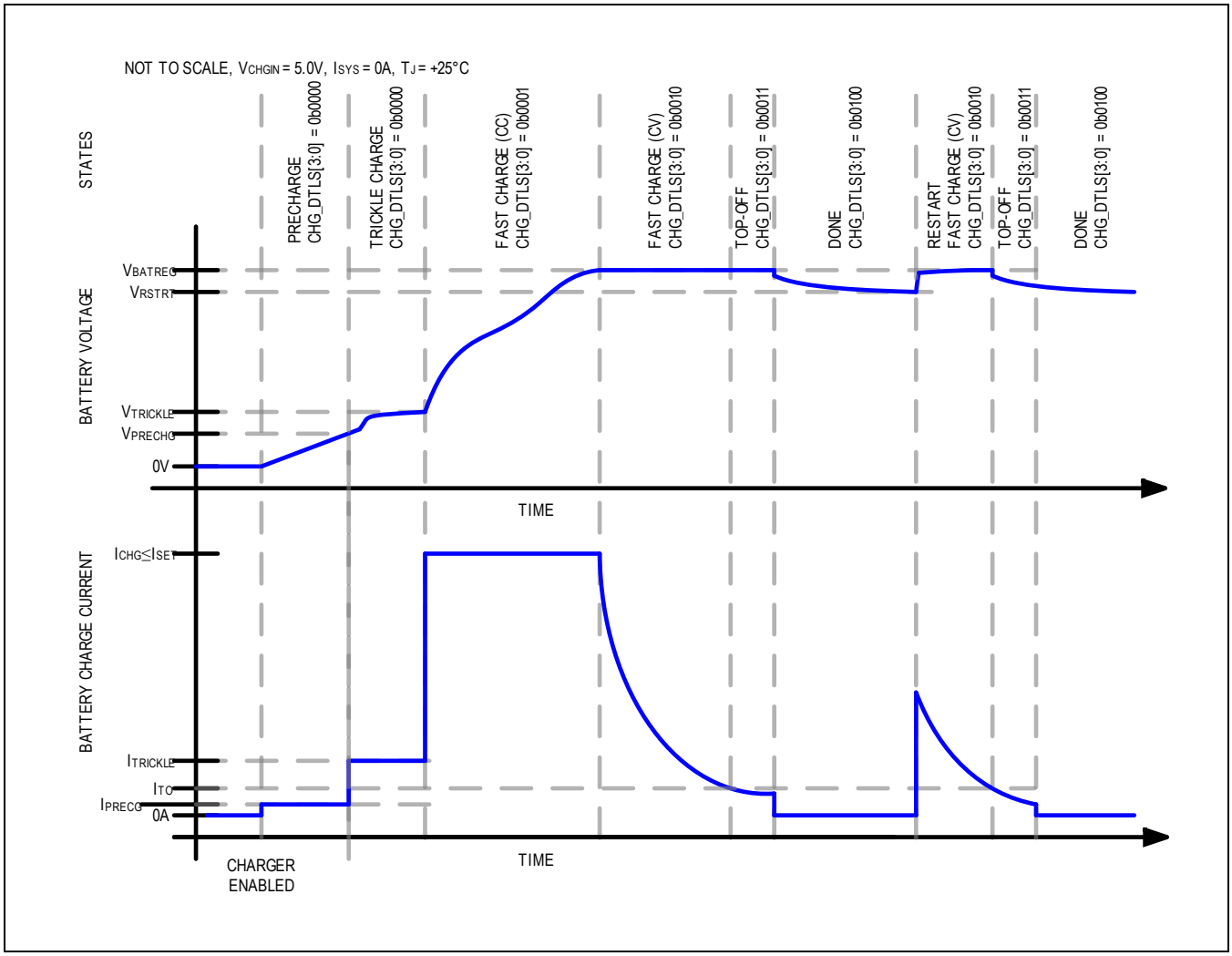


Figure 8. Li+/Li-Poly Charge Profile

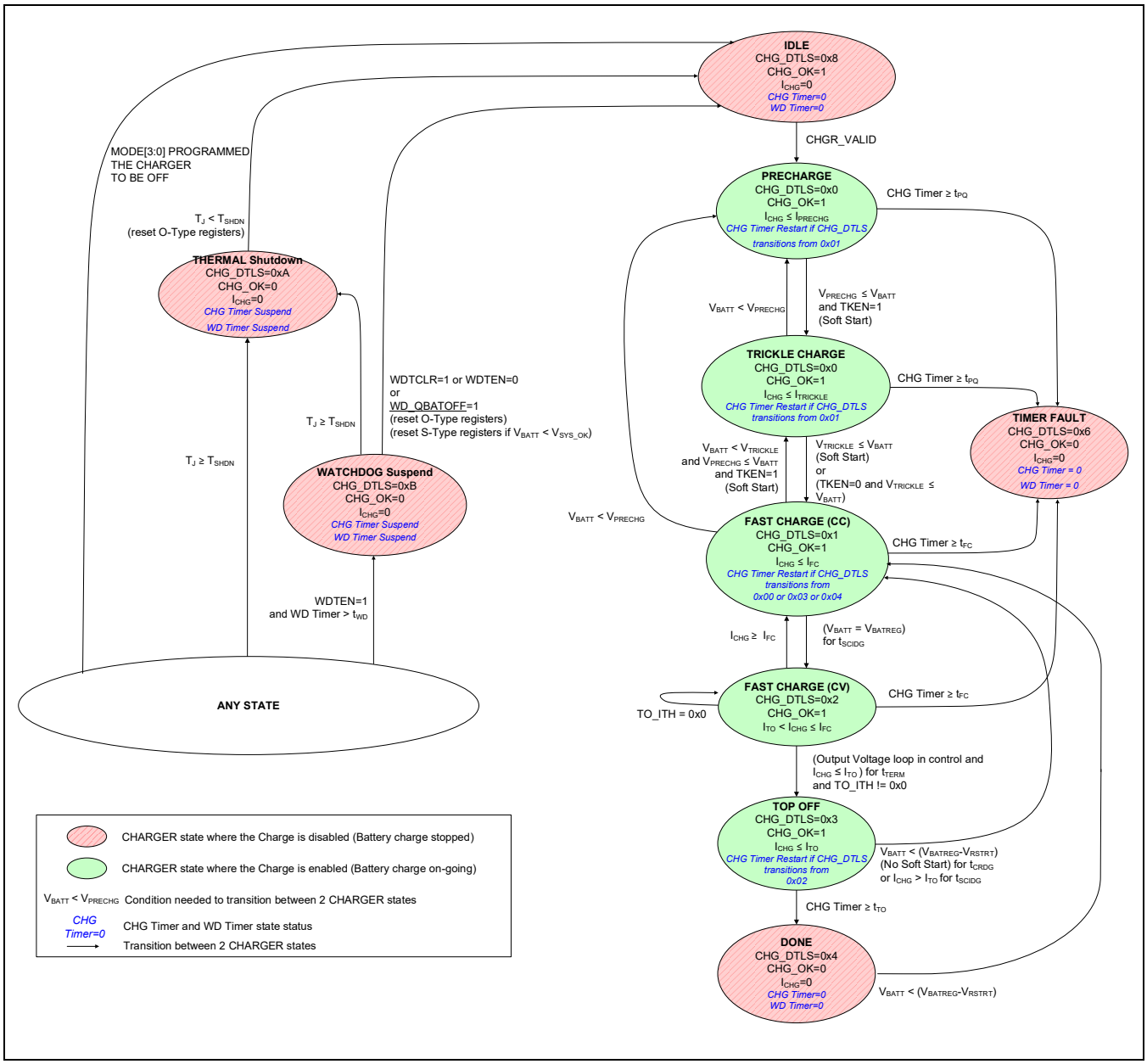


Figure 9. Charger State Diagram

No Input Power or Charge Idle State

While in the “no input power or charger idle” state, the charge current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power is available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the “no input power or charger idle” state, the charger input must be valid, and the charger must be enabled.

Precharge State

As shown in *Figure 8*, the precharge state occurs when the main battery voltage is less than V_{PRECHG}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS is set to 0x00. In the precharge state, the charge current into the battery is I_{PRECHG}.

The following events cause the state machine to exit this state:

- Main battery voltage rises above V_{PRECHG}, and the charger enters the next state in the charging cycle: “Trickle Charge”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced (see the *Watchdog Timer* section), the charger state machine transitions to the “Watchdog Suspend” state.

Note that the precharge state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically, a pack internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the precharge mode current flows into the 0V battery—this current raises the pack’s terminal voltage to the pointer where the internal pack protection switch closes.

Note that a normal battery typically stays in the precharge state for several minutes or less. Therefore, a battery that stays in the precharge for longer than t_{PQ} may be experiencing a problem.

Trickle Charge State

As shown in *Figure 8*, the trickle charge state occurs when $V_{BATT} > V_{PRECHG}$ and $V_{BATT} < V_{TRICKLE}$. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x00.

With TKEN = 1 and the IC in its trickle charge state, the current in the battery is less than or equal to $I_{TRICKLE}$. When TKEN = 0, the battery current is less than or equal to I_{FC}.

Charge current may be less than $I_{TRICKLE}/I_{FC}$ for any of the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Typical systems operate with TKEN = 1. When operating with TKEN = 0, the system’s software usually sets I_{FC} to a low value such as 450mA, and then monitors the battery voltage. When the battery exceeds a relatively low voltage such as 3.1V, then the system’s software usually increases I_{FC}.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{TRICKLE}$ or the PQEN bit is cleared, the charger enters the next state in the charging cycle: “Fast Charge (CC)”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less. Therefore, a battery that stays in trickle charge for longer than t_{PQ} may be experiencing a problem.

Fast-Charge Constant Current (CC) State

As shown in *Figure 8*, the fast-charge CC state occurs when the main-battery voltage is greater than the low-battery prequalification threshold and less than the battery regulation threshold ($V_{TRICKLE} < V_{BATT} < V_{BATTREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x01.

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current may be less than I_{FC} for any of the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback

- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle: “Fast Charge (CV)”.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced. See the *Thermal Foldback* section for more information.

Fast-Charge Constant Voltage (CV) State

As shown in *Figure 8*, the fast-charge CV state occurs when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x02.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to I_{FC}. As shown in *Figure 8*, the charger current decreases exponentially in this state as the battery becomes fully charged.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below I_{TO} for t_{TERM}, the charger enters the next state in the charging cycle: “TOP OFF” state.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Top-Off State

As shown in *Figure 8*, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x03. In the top-off state, the battery charger tries to maintain $V_{BATTREG}$ across the battery, and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time (t_{TO}), the charger enters the next state in the charging cycle: “DONE” state.
- If $V_{BATT} < V_{BATTREG} – V_{RSTRT}$, the charger goes back to the “FAST CHARGE (CC)” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Top-Off Current Shift in Skip Mode

When DISKIP = 0, the buck charger operates in the skip mode during light load. The skip mode operation makes a long-term ripple in the battery charging current and usually results in I_{TO} shifting down than the actual target. Approximately, if (I_{SYS} + I_{TO}) < I_{ULO_DET} x $V_{CHGIN}/V_{BATTREG}$ (let's call this "condition T") then the user may experience the I_{TO} shift.

To maintain I_{TO} accuracy, one of the following methods may be employed:

- MODE = 0x5, use higher I_{TO} and longer t_{TO}: For example, V_{CHGIN} = 15V, $V_{BATTREG}$ = 4.2, I_{SYS} = 0A, and I_{TO} = 200mA. It may show I_{TO} shifted down to around 100mA because it meets the condition T. In the case where the selected I_{TO} is 250mA or 300mA, then I_{TO} accuracy is maintained since the buck charger is still operating in non-skip mode.
- MODE = 0x5, set DISKIP = 1 only when V_{CHGIN} ≥ 15V && CHG_DTLS = 0x02 (CV mode) and set DISKIP = 0 when CHG_DTLS = 0x03 (Top-off state). The alternative condition could be V_{CHGIN} ≥ 15V && I_{BAT} = 50mA + I_{TO} for setting DISKIP = 1 assuming the system processor can read the battery current through the fuel gauge.
- MODE = 0x7, V_{SYS} is regulated by the BCKSYS register while QBAT operates as a linear charger to maintain I_{TO} accuracy.
- MODE = 0x1, V_{SYS} is supplied by an external converter while QBAT operates as a a linear charger to maintain I_{TO} accuracy.

Done State

As shown in *Figure 8*, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 0, and CHG_DTLS = 0x04.

The following events cause the state machine to exit this state:

- If V_{BATT} < $V_{BATTREG}$ – V_{RSTRT}, the charger goes back to the “FAST-CHARGE CC” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low, then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}), and the charger state machine transitions back into the fast-charge CV state. There is no soft-start (di/dt limiting) during the done-to-fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC & CV states is t_{FC} which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO} which is programmable with TO_TIME. Upon entering the timer fault state a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

In the timer fault state, the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and re-inserted to exit the timer fault state.

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The watchdog timer protects the battery from charging indefinitely if the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

If WD_QBATTOFF bit is set to 0 and the watchdog timer expires while the charger is in dead-battery prequalification, low-battery prequalification, fast-charge CC or CV, top-off, done, or timer fault, the charging stops, a CHG_I interrupt is generated only if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer has expired, the charger may be restarted by programming

WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer has expired.

If WD_QBATTOFF bit is set to 1 and the watchdog timer expires, MAX77785/MAX77786 turns off the buck, charger, and Q_{BATT} switch for 150ms. And then V_{SYS} voltage collapses and it resets all I^2C registers. The IC restarts as the initial power-up condition.

Thermal Shutdown State

The thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal-shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN} the charger folds back the charge current to 0A (see the *Thermal Foldback* section). Upon entering this state, CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state, the charger is off. The MODE register (CHG_CNFG_00[3:0]) is reset to its default value as well as all O-type registers.

Charger Interrupt Debounce Time

Table 2. Charger Interrupt Debounce Time

	DEBOUNCE TIME RISING	DEBOUNCE TIME FALLING
INTERRUPT	**Typ (ms)**	**Typ (ms)**
AICL_I	30	30
CHGIN_I	7.5	—
INLIM_I	30	30
BAT_I (Overvoltage T_{BATOV})	7.5	—
BYP_I (T_{OTG_I})	20	—
BYP_I (BST_I_{LIM})	30	—
BYP_I (Buck Neg I_{LIM})	0.5	—

The accuracy of the timer is defined by TACC.

Main-Battery Differential Voltage Sense

BATSP and BATSN are differential remote sense lines for the main battery. To improve accuracy and decrease charging times, the battery charger voltage sense is based on the differential voltage between BATSP and BATSN. Similarly, the thermistor voltage is interpreted with respect to BATSN.

A battery charger without the remote sensing function would typically measure the battery voltage between BATT and GND. In case a charge current of 1A measuring from BATT to GND leads to a V_{BATT} that is 40mV higher than the real voltage because of R_{PAR1} and R_{PAR7} (I_{CHG} x (R_{PAR1} + R_{PAR7}) = 1A x 40mΩ = 40mV). Since the charger thinks the battery voltage is higher than it is, it enters its fast-charge CV state sooner and the effective charge time may be extended by 10 minutes (based on real lab measurements). This charger with differential remote sensing does not experience this type of problem because BATSP and BATSN sense the battery voltage directly. To get the maximum benefit from these sense lines, connect them as close as possible to the main battery connector.

Reverse Boost Mode

The DC-DC converter topology of the IC allows it to operate as a forward buck converter or as a reverse boost converter. The modes of the DC-DC converter are controlled with MODE. When MODE = 0x09 or 0x0A, the DC-DC converter operates in reverse boost mode allowing it to source current to BYP. To allow current flow to CHGIN, set MODE = 0x0A. This mode allows current to be sourced from CHGIN and is commonly referred to as OTG mode.

When MODE = 0x0A, the DC-DC converter operates in reverse boost mode and regulates V_{BYP} to $V_{BYP.OTG}$ and the low ohmic ($R_{CHGIN2BYP}$) switch from BYP to CHGIN is closed. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM. The programmable OTG_ILIM options allow for supplying from 500mA to 3100mA to an external load. When the OTG mode is selected, the unipolar CHGIN transfer function measures the current going out of CHGIN. When OTG mode is not selected, the unipolar CHGIN transfer function measures the current going into CHGIN.

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$ current during a minimum time of T_{OTG_I} ms, then a BYP_I interrupt is generated. BYP_OK = 0 and BYP_DTLS[0] = 1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off T_{OTG_fault} after entering OTG_ILIM condition. If the overload at CHGIN persists, BYP_DTLS keeps continuing to report OTG_ILIM fault through BYP_DTLS[0] = 1.

If OTG_REC_EN bit = '1: other functions remain unaffected, i.e., BYP is supplied by reverse boost, and the BYP to CHGIN switch automatically retries after T_{OTG_retry}. If the overload at CHGIN persists, then the CHGIN switch toggles ON and OFF with T_{OTG_fault} ON time and T_{OTG_retry} OFF time.

If OTG_REC_EN bit = '0: the BYP to CHGIN switch remains off and the switcher is turned off until MODE is toggled. BYP_I exit interrupt is only generated on OTG load release such as $I_{OTG} < I_{CHGIN.OTG.ILIM}$ or FET opening. At that time, the BYP_I interrupt is generated. BYP_OK = 1 and BYP_DTLS[0] = 0.

Note: On OTG_ILIM debounce time out, BYP_DTLS[0] is latched until the BYP_DTLS register is read by AP. BYP_OK is matching BYP_DTLS[0] behavior.

Main-Battery Overcurrent Protection During System Power-Up

The “main-battery overcurrent protection during system power-up” feature limits the main battery to system current to I_{SYSPU} if V_{SYS} is less than V_{SYSPU_BAT}. This feature limits the surge current that typically flows from the main battery to the device’s low-impedance system bypass capacitors during a system power-up. System power-up is any time that energy from the battery is supplied to SYS when $V_{SYS} < V_{SYSPU}$. This “system power-up” condition typically occurs when a battery is hot-inserted into an otherwise unpowered device. Similarly, the “system power-up” condition can occur when the DISIBS bit is driven low.

When “system power-up” occurs due to hot insertion into an otherwise unpowered device, a small delay is required for this feature’s control circuits to activate. A current spike over I_{SYSPU_BAT} can occur during this time.

Main-Battery Overcurrent Protection Due to Fault

The IC protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur in a smartphone for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The main-battery overcurrent protection feature is enabled with B2SOVRC; disabling this feature reduces the main-battery current consumption by 2µA.

When the main-battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold (I_{BOVRC}) for at least t_{BOVRC}, a BAT_I interrupt is generated, BAT_OK is cleared, and BAT_DTLS reports an overcurrent condition. Typically, when the system’s processor detects this overcurrent interrupt it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent within t_{OCP}, then the IC disables the BATT to SYS discharge path (Q_{BATT} switch) and turns off the Buck. Under OCP fault condition, when SYS is low ($V_{SYS} < V_{SYSUP}$) for t_{OCP_RETRY}, the IC restarts on its own and attempts to pull up SYS again. If the fault condition remains, the whole cycle repeats until this fault condition is removed.

AP can also turn off the Q_{BATT} switch by driving the DISIBS bit to a logic high or pulling the DISQBAT pin high.

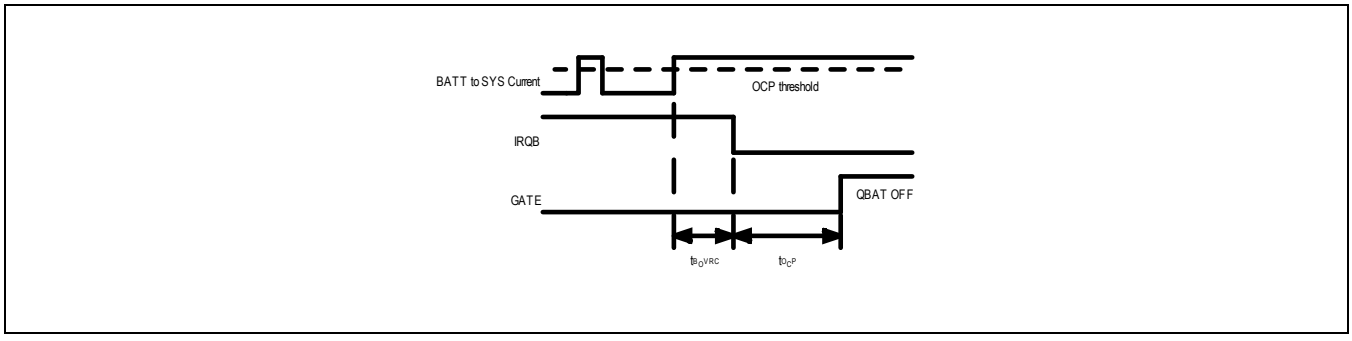


Figure 10. BATT to SYS Overcurrent Protection

There are different scenarios of how the ICs respond to the OCP event depending on the available power source and the state of the charger:

1) The IC is only powered by battery, then the OCP event occurs:

a. Q_{BATT} switch opens.

b. SYS collapses and is allowed to go to 0V.

c. If RECYCLE_EN = 1: After SYS is low (V_{SYS} < V_{SYSUP}) for t_{OCP_RETRY}, the IC restarts on its own and attempts to pull up SYS again. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section). If RECYCLE_EN = 0: The Q_{BATT} switch remains open. When a valid charger input is inserted, the Buck and Q_{BATT} switch turns on.

2) The IC is powered from BATT and CHGIN, buck is switching, charge is ON, then an OCP event occurs:

a. Buck is off and Q_{BATT} switch opens

b. SYS collapses and is allowed to go to 0V

c. Regardless of the RECYCLE_EN setting, the IC retries to bring up V_{SYS} above V_{SYSUP}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section). If V_{SYS} Power-up Failure happened during a retry, then valid charger input has to be inserted to turn on the Buck and Q_{BATT} switch (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section).

3) The IC is powered from CHGIN, the buck is switching, the charge is OFF, then an OCP event occurs:

a. Buck is off and Q_{BATT} switch opens

b. SYS collapses and is allowed to go to 0V

c. Regardless of the RECYCLE_EN setting, the IC retries to bring up V_{SYS} above V_{SYSUP}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section). If V_{SYS} Power-up Failure happened during a retry, then valid charger input has to be inserted to turn on the Buck and Q_{BATT} switch (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section).

Battery to SYS Q_{BATT} Switch Control (DISIBS)

To protect the system from unexpected and critical events (e.g., excessive battery discharge current), the AP can control the MAX77785/MAX77786 Q_{BATT} switch by driving the DISIBS bit to a logic high.

There are different scenarios of how the IC responds to setting the DISIBS bit high depending on the available power source and the state of the charger:

1) The IC is only powered from BATT and the DISIBS bit is set

a. Q_{BATT} switch opens

b. SYS collapses and is allowed to go to 0V

c. If RECYCLE_EN = 1, the IC self-recovers and restarts after t_{OCP_RETRY}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section). If RECYCLE_EN = 0, after t_{OCP_RETRY}, the IC does not recycle until a valid charger input is inserted.

2) The IC is powered from BATT, CHGIN is present, the charger buck is not switching, and the DISIBS bit is set:

a. Q_{BATT} switch opens

b. SYS collapses and is allowed to go to 0V

c. Regardless of the RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section).

3) The IC is powered from CHGIN, the buck is switching, the charge is OFF, and the DISIBS bit is set:

a. Q_{BATT} stays OFF (opened)

b. Turn off Buck

c. SYS collapses and is allowed to go to 0V

d. Regardless of the RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section).

4) The IC is powered from CHGIN, the buck is switching, the charge is ON, and the DISIBS bit is set:

a. Charge is disabled

b. Q_{BATT} turns off (opened)

c. Turn off Buck

d. SYS collapses and is allowed to go to 0V

e. Regardless of the RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}. If the fault condition is not removed by SYS collapsing to 0V, the IC may fail to bring up V_{SYS} above V_{SYSUP} (see the *V_{SYS} Power-Up Failure (PWRUPFAIL)* section).

HW Control of Battery to SYS Q_{BATT} Switch—DISQBAT

To protect the system from unexpected and critical events (e.g., excessive battery discharge current), the AP can control the ICs Q_{BATT} switch by driving the DISQBAT hardware pin. This pin can also be driven during factory test modes.

On DISQBAT low-to-high assertion, Q_{BATT} FET opens and any ongoing charge is disabled but the buck keeps switching (if allowed by MODE setting).

The IC supports a factory-boost mode to enter boost mode (through CHG_CNFG_00.MODE setting) and keep Q_{BATT} OFF even if boost mode is set.

This functionality is only enabled once the functional register CHG_CNFG_07.FMBST bit is set 1.

DISQBAT is an input control signal for Q_{BATT} FET with an external logic signal. If DISQBAT is driven by high, Q_{BATT} FET is truly disconnected. It has an internal 470kΩ pulldown resistor.

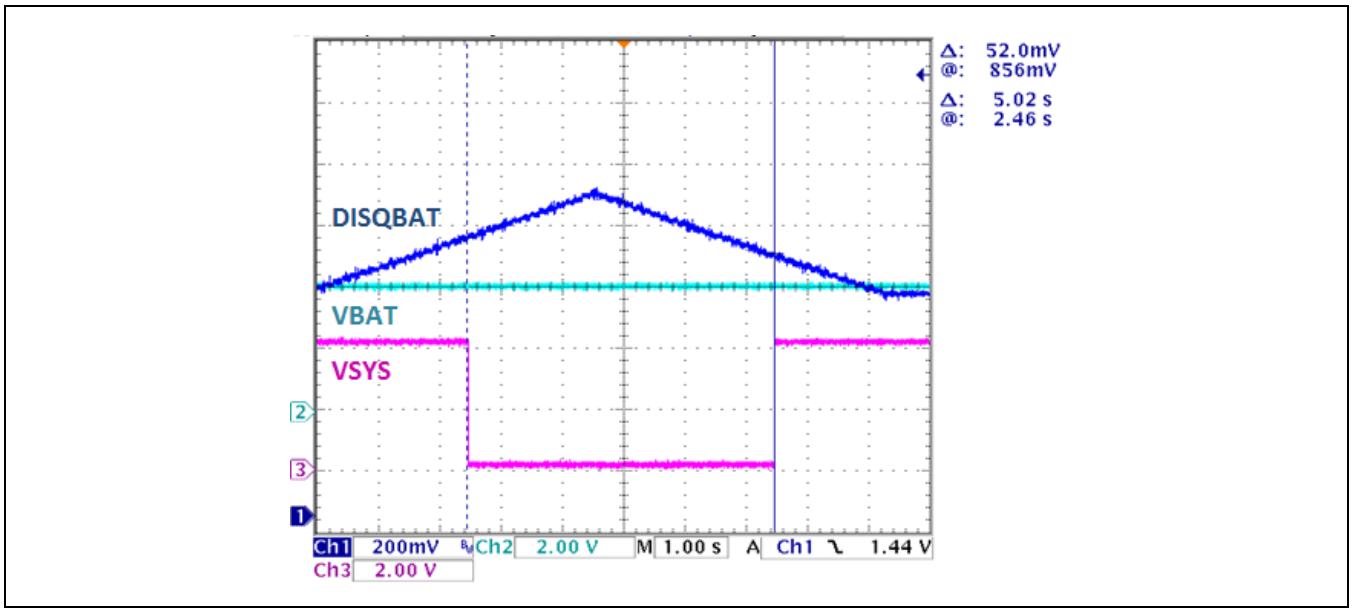


Figure 11. Hardware Control of Battery to SYS Switch

Thermal Management

The ICs charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the ICs junction temperature. When the die temperature exceeds the value programmed by REGTEMP (T_{REG}), a thermal limiting circuit reduces the battery charger's target current to regulate the ICs junction temperature to T_{REG}. The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current). When the thermal foldback loop changes state, a CHG_I interrupt is generated and the system's microprocessor may read the status of the thermal regulation loop through the T_{REG} status bit. Note that the thermal foldback loop being active is not considered to be an abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

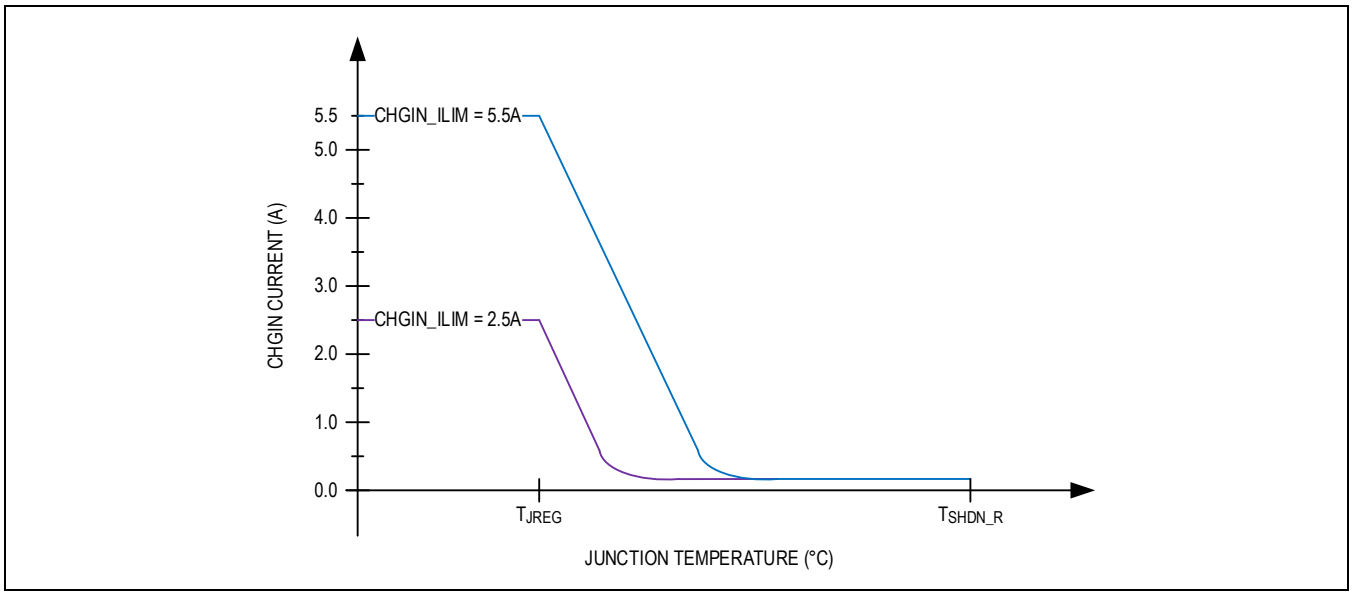


Figure 12. CHGIN Current vs. Junction Temperature

Thermistor Input (THM)

The thermistor input can be utilized to achieve functions such as charge suspension, JEITA-compliant charging, and battery removal detection. The thermistor monitoring feature can be disabled by connecting the THM pin to ground.

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature.

JEITA Compliant Charging

JEITA-compliant charging is available with JEITA_EN = 1.

Charging stops when the thermistor temperature is out of range ($T < T_{COLD}$ or $T > T_{HOT}$). The charge timers are reset and the CHG_DTLS[3:0], CHG_OK register bits report the charging suspension status, and CHG_I interrupt bit is set. When the thermistor comes back into range ($T_{COLD} < T < T_{HOT}$), charging resumes, and the charge timer restarts.

See the *JEITA Controlled Charging* section for more details.

Battery Removal Detection

With pullup connected between PVDD and THM, if the battery is removed, the thermistor is disconnected from THM; this event is detected as THM is pulled up to PVDD. Battery removal event prevents charging.

Disable Thermistor Monitoring

Connecting THM to GND disables the thermistor monitoring function, and JEITA-controlled charging is unavailable in this configuration. The IC detects an always-connected battery when THM is grounded, and charging starts automatically when a valid adapter is plugged in. In applications with removable batteries, do not connect THM to GND because the IC

is not able to detect battery removal when THM is grounded. Instead, connecting THM to the thermistor pin in the battery pack is recommended.

Since the thermistor monitoring circuit employs an external bias resistor from THM to PVDD, the thermistor is not limited only to 10kΩ (at +25ºC). Any resistance thermistor can be used as long as the value is equivalent to the thermistor's +25ºC resistance. For example, with a 10kΩ at RTB resistor, the charger enters a temperature suspend state when the thermistor resistance falls below 4.67kΩ (too hot) or rises above 30.3kΩ (too cold). This corresponds to the 0ºC to +45ºC range when using a 10kΩ NTC thermistor with a beta of 3610. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\{\beta\{\frac{1}{T+273^{\circ}C}-\frac{1}{298^{\circ}C}\}\}}$$

where:

R_T = The resistance in Ω of the thermistor at temperature T in Celsius

R_{25} = The resistance in Ω of the thermistor at +25ºC

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k

T = The temperature of the thermistor in °C

Some designs might prefer other thermistor temperature limits. Threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with a different β. For example, a +45ºC hot threshold and 0°C cold threshold can be realized by using a thermistor with a β to 4250 and connecting 120kΩ in parallel. Since the thermistor resistance near 0ºC is much higher than it is near +50ºC, a large parallel resistance lowers the cold threshold while only slightly lowering the hot threshold. Conversely, a small series resistance raises the hot threshold, while only slightly raising the cold threshold. Raising R_{TB}, lowers both the hot and cold threshold, while lowering R_{TB} raises both thresholds.

Thermistor bias current flows whenever P_{VDD} is enabled (CHGIN valid or BOOST enabled). When using a 10kΩ thermistor and a 10kΩ pullup to THM, this results in an additional 90µA load. This load can be reduced to 9µA by instead using a 100kΩ thermistor and 100kΩ pullup resistor.

Table 3. Trip Temperatures for Different Thermistors

THERMISTOR	R25 (Ω)	10000	10000	47000	100000
	Thermistor Beta (β)	3380	3610	4050	4250
	RTB (Ω)	10000	10000	47000	100000
	R15 (Ω)	14826	15223	75342	164083
	R45 (Ω)	4900	4671	19993	40781
TRIP TEMPERATURES	T_{COLD} (˚C)	-1.3	0.2	2.7	3.7
	T_{COOL} (˚C)	9.1	10.0	11.6	12.2
	T_{WARM} (˚C)	46.2	44.8	42.5	41.7
	T_{HOT} (˚C)	62.4	59.8	55.6	54.0

JEITA Controlled Charging

The MAX77785/MAX77786 safely charges Li+ batteries following JEITA specifications. The IC monitors the battery temperature with an NTC thermistor connected to the THM pin and automatically adjusts the fast-charge current and/or charge termination voltage as the battery temperature varies. JEITA controlled charging can be disabled by setting JEITA_EN to '0; if JEITA_EN = '0, thermistor input is not taken into account to determine charge state or charge current and voltage levels.

CHG_DTLS and THM_DTLS registers report JEITA controlled charging status.

The JEITA-controlled fast-charging current (I_{CHGCC_JEITA}) for $T_{WARM} < T < T_{HOT}$ is programmable with I^2C bit CHG_CC_WARM.

The JEITA-controlled charge termination voltage (V_{CHGCV_JEITA}) for $T_{COLD} < T < T_{COOL}$ is programmable with I2C bit CHG_CV_COOL.

The JEITA-controlled fast-charging current for $T_{COLD} < T < T_{COOL}$ is halved (to CHG_CC x 0.5) and the charge termination voltage for $T_{WARM} < T < T_{HOT}$ is reduced to (CHG_CV_PRM – CV_BCKOFF), as shown in *Figure 13*.

The JEITA-controlled charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

Temperature thresholds T_{COLD}, T_{COOL}, T_{WARM}, and T_{HOT} depend on the thermistor selection. See the *Thermistor Input (THM)* section for more details.

When the JEITA-controlled battery charge current is reduced by 50%, the charger timer is doubled.

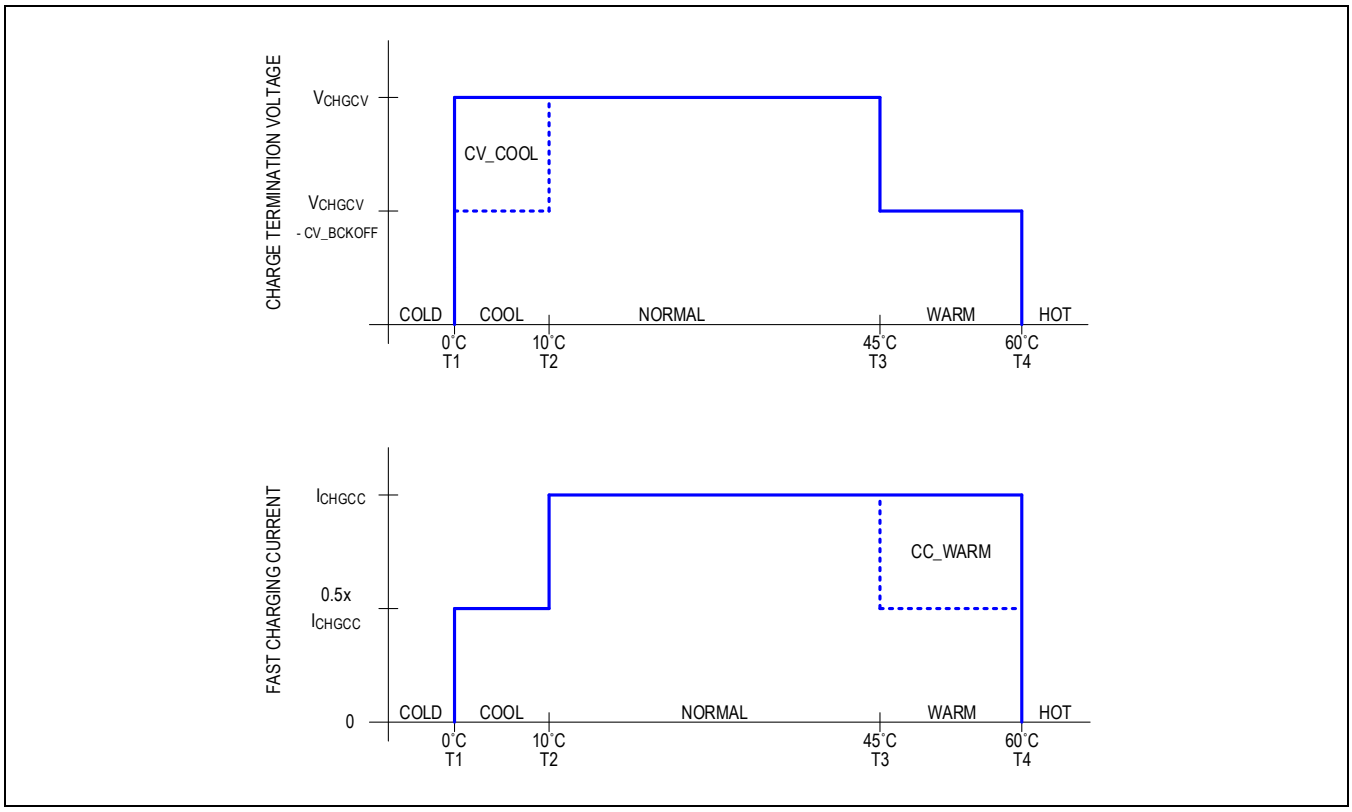


Figure 13. JEITA Controlled Charging

Analog Low-Noise Power PVDD and VDD

VDD is the 1.8V LDO output for the charger's analog circuitry. VDD takes its power from the higher voltage of CHGIN, BATT, and SYS. VDD has a bypass capacitance of 1µF.

PVDD is the 1.8V LDO output for internal power circuitry. PVDD has a bypass capacitance of 1µF + 0.1µF.

Factory-Ship Mode

The ICs support factory-ship mode.

Charger's CHG_CNFG_07 bit 0: FSHIP_MODE bit controls this mode.

When this bit is set to 1, the IC goes into factory-ship mode.

This mode can be exited by battery removal, on a valid charger input plug, or by pulling EXTSM low longer than t_{EXTSM_DEB} (programmable with EXTSM_T bit).

Factory-ship mode cannot be entered when a valid charger is present.

This feature minimizes battery leakage current when the factory ships battery-connected devices.

External Q_{BATT} Control I/O

QBEXT is an open-drain output that is driven low in Battery mode and high-impedance (pulled up externally) in non-battery mode.

The Q_{BATT} in MAX77785/MAX77786 has a very low R_{DSON} that equals 7.7mΩ. If the application requires a lower resistive discharging path then this output can be utilized to drive an external Q_{BATT} FET driver in parallel with internal Q_{BATT}. This output can be enabled or disabled by the QBEXT_CTRL bit.

Table 4. QBEXT Output in Different System Modes

SYSTEM MODE	USE CASE DETAILS	QBEXT OUTPUT
Battery Mode	All use cases except non-battery mode	Low
Non-Battery Mode	Valid adapter is present, and the buck is switching (whatever the charge status is) or MODE = 0x09 (Boost) or MODE = 0x0A (Boost + OTG)	Hi-Z (pulled-up)

The QBEXT pin also can be configured to an alternative function called $\overline{PGOOD}$. If a user writes UNPLUG_TH[5:0] with another than 0b00, then the QBEXT pin is working as $\overline{PGOOD}$ which is the comparator output of V_{BUS} unplug detection.

For the 5V unplug detection (CHGIN invalid), there are two cases as follows, the output goes high when V_{CHGIN} = AICL and I_{CHGIN} < I_{IULO_DET} with 1ms de-bounce time when AICL function is enabled. Or the output goes high when $V_{CHGIN2SYS}$ < 150mV or V_{CHGIN} < $V_{CHGIN\_UVLO\_F}$ when the AICL function is disabled.

For other unplug detection, the output goes high when V_{CHGIN} voltage comes across the threshold of V_{CHGIN_UNPLUG} with selectable de-bounce by the UNPLUG_DB bit.

Table 5. $\overline{PGOOD}$ Output State

V_{BUS}	BATTERY	MODE	$\overline{PGOOD}$
plugged, > programmed threshold	Yes/No	Normal	Low
plugged, < programmed threshold	Yes/No	Normal	Hi-Z
not plugged	Yes	Normal	Hi-Z
not plugged	Yes	Factory-ship mode	Hi-Z
not plugged	No	No Power	Hi-Z
plugged, > programmed threshold	Yes	Suspend	Low
plugged, < programmed threshold	Yes	Suspend	Hi-Z
don't care	Yes	Deep Suspend	Hi-Z
don't care	Yes	OTG (reverse boost)	Hi-Z

Charge Status LED Indication

Table 6. STAT_MODE = 0x0

CHG STATUS	LED	DUTY (%)
No DC input or Suspend or Buck operation	Off	0
Any Charging Timeout, Off by JEITA feature, Off by thermal shutdown	Blink in 2Hz	50
DBAT, Pre-Q, CC, CV	Blink in 1Hz	50
Top-off, Done, Restart	Solid on	100

Table 7. STAT_MODE = 0x1

CHG STATUS	LED	DUTY (%)
No DC input or Suspend or Buck operation	Off	0
Any Charging Timeout, Off by JEITA feature, Off by thermal shutdown	Off	0
DBAT, Pre-Q, CC, CV	Blink in 1Hz	50
Top-off, Done, Restart	Solid on	100

Audio Mode

When the Audio mode is enabled by writing AUDIO_MODE = 0b1, the bootstrap is intentionally refreshed with 64kHz so that the switch node frequency is higher than the audible frequency.

Spread Spectrum

The Buck can dither its switching frequency for noise-sensitive applications. The spread-spectrum function is activated only in Continuous Conduction Mode (CCM) and it is automatically deactivated when the Buck enters Discontinuous Conduction Mode (DCM). The spread-spectrum function can be disabled by SS_ENV[1:0] bits.

The modulation envelope (ΔFSS) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. The modulation envelope is programmable (±4%, ±8%, or ±16%) by the SS_ENV[1:0] bits and it controls 'how wide' the switching frequency dithers.

Modulation frequency (FSS_MOD) determines how often the switching frequency dithering cycle repeats.

Two modulation patterns are determined by the SS_PAT bit. One is triangular and the other is pseudo-random. In a triangular pattern, the modulation frequency is fixed at 2.133kHz. In pseudo-random, it is 4.267kHz.

When Audio_Mode is enabled, the modulation frequency is automatically changed to 133Hz for a triangular pattern and to 267Hz for a pseudo-random pattern.

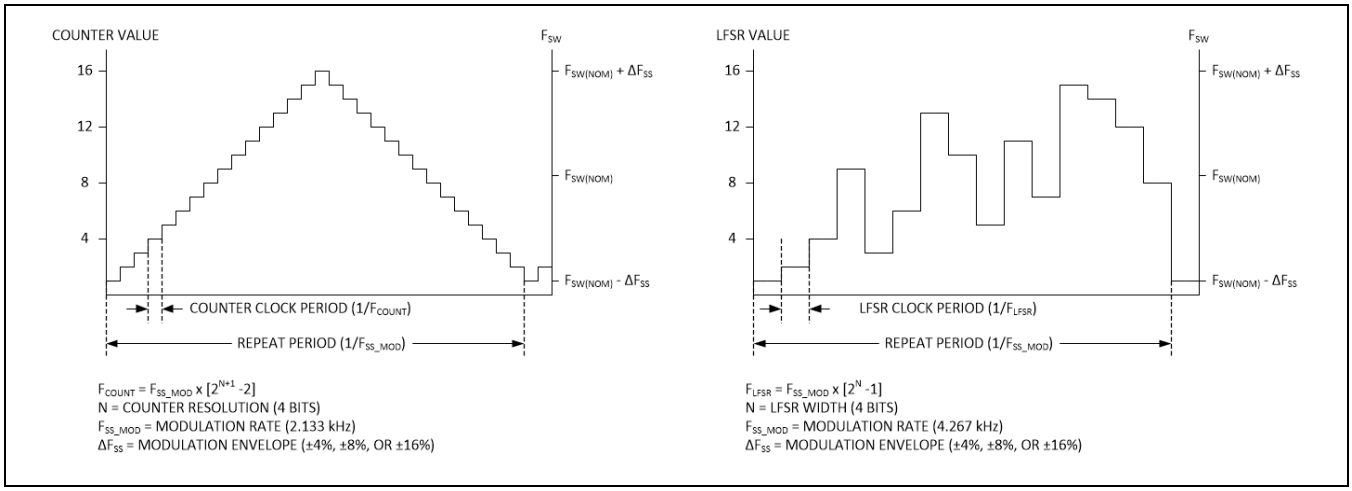


Figure 14. Spread Spectrum

Programmable Minimum System Voltage

Based on Battery chemistry, the CHG_CV_PRM selects to meet the target battery termination voltage ($V_{BATTREG}$). The V_{MINSYS} must be positioned between the minimum system operation voltage and the battery termination voltage. So MAX77785/MAX77786 supports programmable V_{MINSYS} (minimum system voltage) by MINSYS[2:0] value. It is recommended to position where the system minimum operating voltage < V_{MINSYS} ≤ $V_{BATTERM}$ voltage – 200mV condition can be met for proper operation.

Top System Management

Overview

This section discusses the top system of the MAX77785/MAX77786 and how the IC manages its bias, system faults, and turn-on and off events.

Main Bias

The main bias includes voltage and current references for all circuitry that runs from the V_{SYS} node.

System Faults

V_{SYS} Fault

The system monitors the V_{SYS} node for undervoltage and overvoltage events. The following describes the IC behavior if any of these events are to occur.

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

V_{SYS} undervoltage lockout prevents the regulators from being used when the input voltage is below the operating range. When the voltage from SYS to GND (V_{SYS}) is less than the undervoltage-lockout threshold ($V_{SYSUVLO}$), MAX77785/MAX77786 shuts down and resets "O" Type I^2C registers.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

V_{SYS} overvoltage lockout is a fail-safe mechanism and prevents the regulators from being used when the input voltage is above the operating range. The absolute maximum ratings state that the SYS node withstands up to 6V. The SYS OVLO threshold is set to 5.45V (typ)—ideally, V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed such that V_{SYS} never exceeds 5.2V (transient and steady state). If the V_{SYS} exceeds $V_{SYS\_OVLO\_R}$, the ICs shut down and reset "O" Type I^2C registers.

V_{SYS} Power-Up Failure ($P_{WRUPFAIL}$)

V_{SYS} power-up failure is a hardware diagnostic mechanism to detect failures affecting the system and preventing the platform from powering up. When a valid power source (battery V_{BATT} > SYS_UVLOB_R or charger with V_{CHGIN} > $V_{CHGIN\_UVLO\_R}$) is plugged, MAX77785/MAX77786 is expected to pull the SYS node up using one of the system power-up current sources (I_{SYSPU_BAT} or I_{SYSPU_BYP} respectively). If V_{SYS} does not rise above V_{SYSPU} due to a fault in the application (external to MAX77785/MAX77786) after a time-out elapses (t_{SYSPU_BAT} or t_{SYSPU_BYP} respectively) a power-up fault is asserted and an interrupt (PWRUP_FAIL_INT) is generated. Because the SYS node is down, the application software may not be able to service the interrupt; the interrupt can only be observed by pulling VIO up externally and serviced by taking control of the I^2C interface.

Thermal Fault

The ICs have one centralized thermal circuit that senses the temperature on the die. If temperature increases >155°C (T_{SHDN}) this constitutes a thermal shutdown event and the MAX77785/MAX77786 shuts down and resets "O" Type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature is reduced by 15°C, the thermal shutdown bus is deasserted and the IC can be enabled again. The main battery charger has an independent thermal control loop which does not cause a thermal shutdown event. If a charger thermal overload occurs, only the charger turns off.

System Faults Debounce Time

Applicable in charge or buck mode.

Table 8. System Faults Debounce Time Summary

	EDGE TO I/T		I/T TO FAULT		ACTION ON FAULT
	t_{DEB} (RISING)	t_{DEB} (FALLING)	t_{DEB} (RISING)	t_{DEB} (FALLING)	—
SYS UVLO	—	—	8ms	—	O-Type reset
SYS OVLO	-/5ms by I^2C*	—	—	—	O-Type reset
T_{SHDN}	175µs	—	—	—	O-Type reset
BATT OCP	t_{BOVRC}	—	t_{OCP}	—	Q_{BATT} opens
OTG OCP	t_{OTG_ALARM}	—	t_{OTG_FAULT} - t_{OTG_ALARM}	—	RBFET opens

(*) Depending on I^2C Bit SYSOVLO_DEB_EN

Fast Role Swap Implementation Considerations

With MAX77785/MAX77786, a system can implement the Fast Role Swap function as defined in the USB PD3.0 specification. The reverse boost operation is started immediately if it meets the following conditions:

- FAST_ROLE_SWAP_EN bit = 1
- $V_{CHGIN} < V_{safe5Vmax}$ (5.5V)
- Any MODE except MODE 0xA

MAX77785/MAX77786 has no CC pin, so the external PD controller or application processor must pull up the ENBST pin after the CC pin goes low within $t_{FRSwapRx}$.

After the reverse boost operation starts, the CHGIN_I interrupt is generated and the FRS_STS status bit is set. This feature overrides the MODE bit to expedite reverse boost operation. Then, it requires the application processor to match the actual operation status by writing 0x0A to MODE. After MODE is written 0x0A, the ENBST pin can be released, and the reverse boost operation continues.

To disable the boost operation, change the MODE to other than 0x0A or set FAST_ROLE_SWAP_EN to 0.

Keep the FAST_ROLE_SWAP_EN to 0 if the user application doesn't support FRS.

USB Switch with BC1.2 Detection

Features

- D+/D- Charging Signature Detector
- USB BC1.2 Compliant
- SDP, DCP, and CDP Detection
  - Apple 500mA, 1A, 2A, and 2.4A
  - Samsung 2A
  - 3A DCP

Description

The USB charger detection is USB BC1.2 compliant with the ability to automatically detect some common proprietary charger types. It detects SDP, CDP, and DCP types as well as a limited number of proprietary charger types (Apple and Samsung). It automatically sets the CHGIN input current limiting based on the charger type detection results. If charger type detection results are an unknown charger type, the input current limits are set to 500mA max.

The chgDetMan bit allows users to conduct the USB charger detection manually and the USB_SW_CTRL enables users to control the USB switch manually. After the USB cable is plugged out, the USB switch (B) remains on, so the application processor or system controller needs to turn both switches off by writing USB_SW_CTRL to 0b00 if preferred.

Also, a user can control HVDCP with dpDnMan, dpDrv, and dnDrv bits.

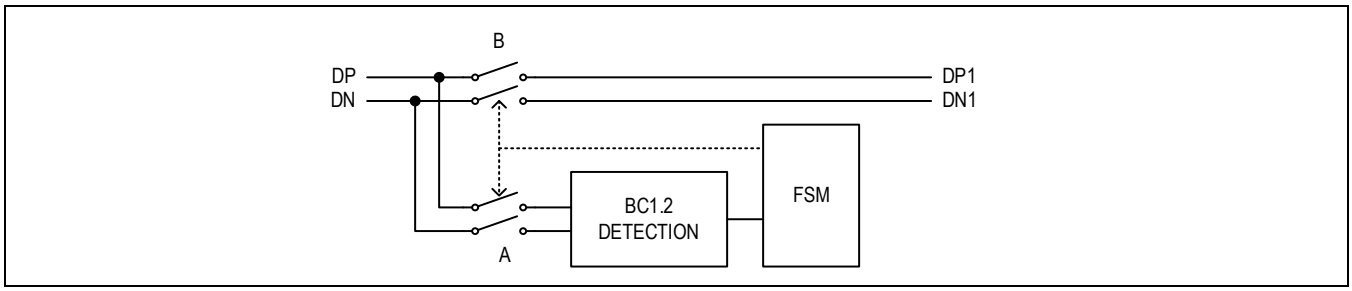


Figure 15. USB Switch with BC1.2 Detection

Table 9. BC1.2 Port Type

USB BC1.2 DETECTED PORT TYPE	
INPUT CURRENT LIMIT	**PORT DETECTED**
500mA	No CHGIN
500mA	SDP
1.5A	CDP
1.5A	DCP

Table 10. Proprietary Charger Type

DETECTED PROPRIETARY CHARGER TYPE	
500mA	Apple 0.5A
1A	Apple 1A
2A	Apple 2A
2.4A	Apple 2.4A (12W)
2A	Samsung
500mA	All others

S-Type and O-Type Registers

- S-Type registers include TOP_FUNC registers 0x0, 0x01, 0x02, 0x03, 0x04, 0x05, 0x51; CHARGER_FUNC 0x10, 0x12, 0x13, 0x14, 0x15, 0x27.
- O-Type registers include I2C_FUNC register 0x40, TOP_FUNC register 0x50; CHARGER_FUNC registers 0x11, all registers from 0x16 to 0x26 and 0x28 to 0x2C; BC1P2 all registers.

Charger Register Write Protection

CHARGER_FUNC registers (0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27) are protected to be written by I2C by default. To write to these registers, CHGPROT[1:0] has to be written as 0b11.

Write CHGPROT[1:0] with values other than 0b11 to prohibit these registers from being written.

I2C Interface Description

Main I2C Interface

The IC acts as a Slave Transmitter/Receiver and has the following slave addresses:
Slave Address (7 bit) 0x6B 110 1011
Slave Address (Write) 0xD6 1101 0110
Slave Address (Read) 0xD7 1101 0111

I2C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

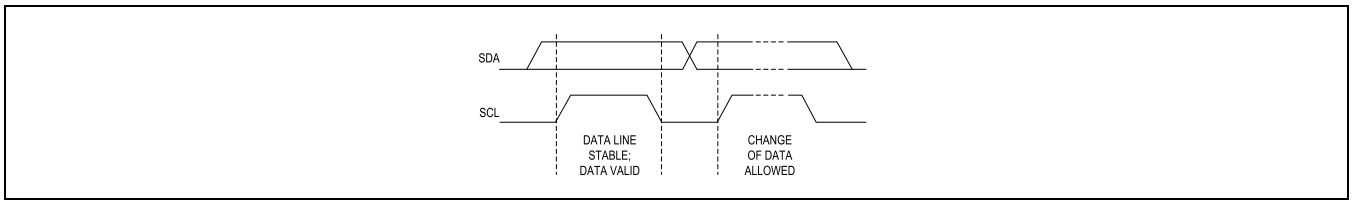


Figure 16. I2C Bit Transfer

I²C Start and Stop Conditions

Both SDA and SCL remain High when the bus is not busy. The Start (S) condition is defined as a high-to-low transition of the SDA while the SCL is high. The Stop (P) condition is defined as a low-to-high transition of the SDA while the SCL is high.

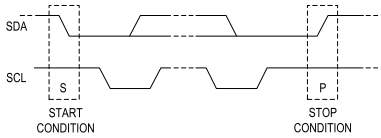


Figure 17. I²C Start and Stop

I²C System Configuration

A device on the I²C bus that generates a “message” is called a “Transmitter” and a device that receives the message is a “Receiver”. The device that controls the message is the “Master” and the devices that are controlled by the “Master” are called “Slaves”.

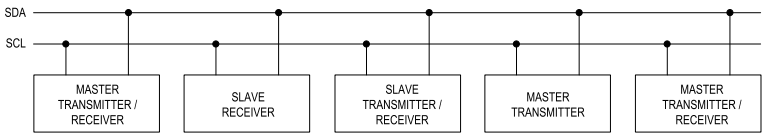


Figure 18. System Configurations

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited.

Each 8-bit byte is followed by an Acknowledge bit. The Acknowledge bit is a high-level signal put on SDA by the transmitter during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge-clock pulse so that the SDA line is stable and low during the high period of the acknowledge-clock pulse (setup and hold times must also be met). A master receiver must signal the end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

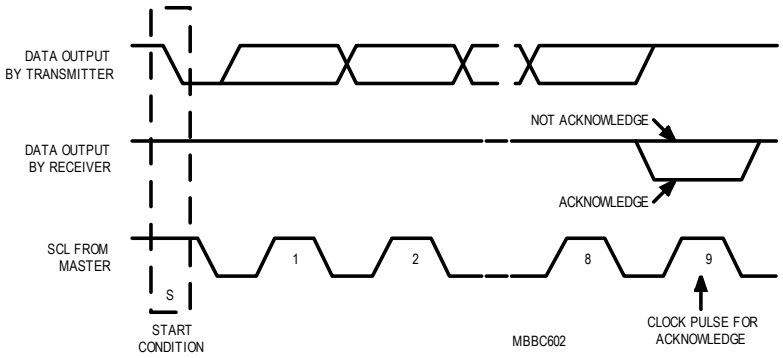


Figure 19. I²C Acknowledge

Master Transmits (Write Mode)

Use the following format when the master writes to the slave.

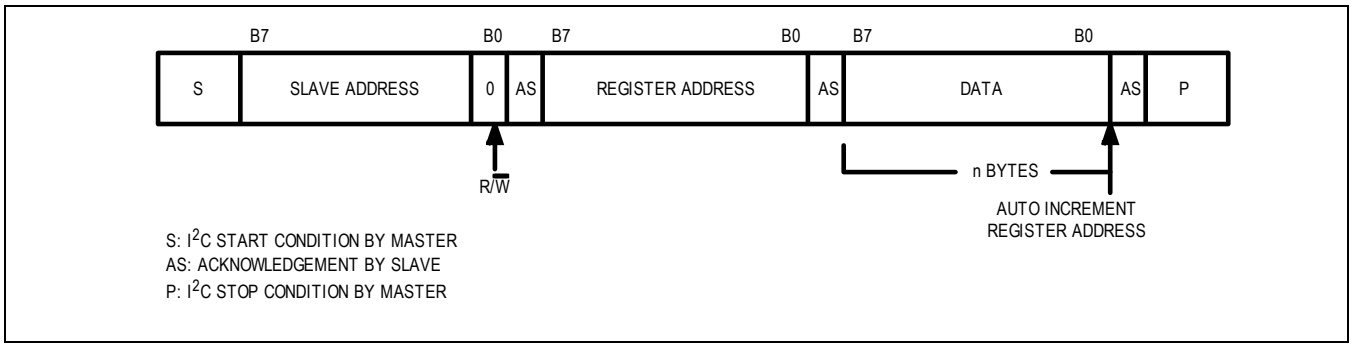


Figure 20. I²C Master Transmits

Master Reads after Setting Register Address (Write Register Address and Read Data)

Use the following format to read a specific register.

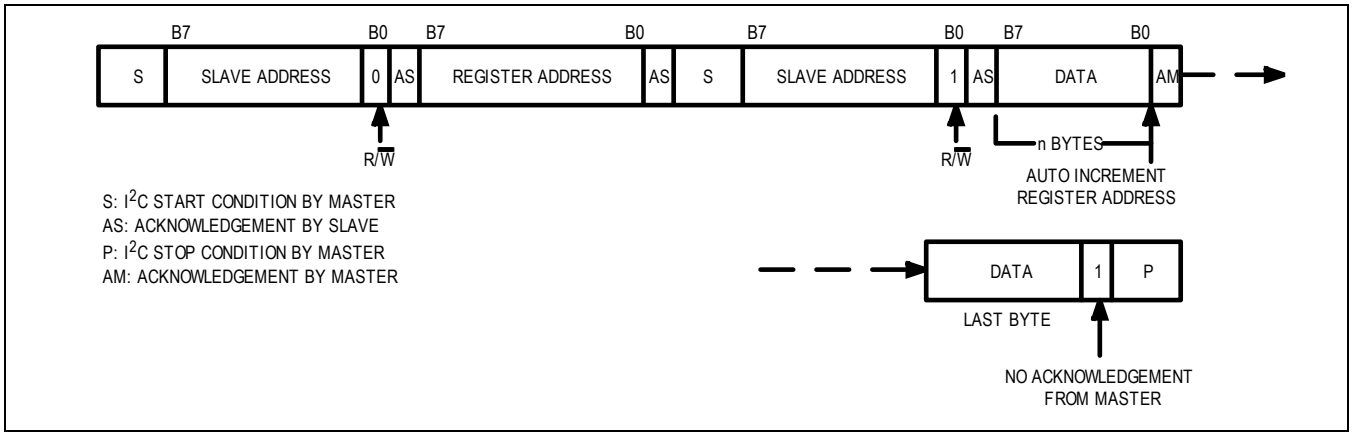


Figure 21. I²C Master Reads after Setting Register Address

Master Reads Register Data Without Setting Register Address (Read Mode)

Use the following format to read registers continuously starting from first address.

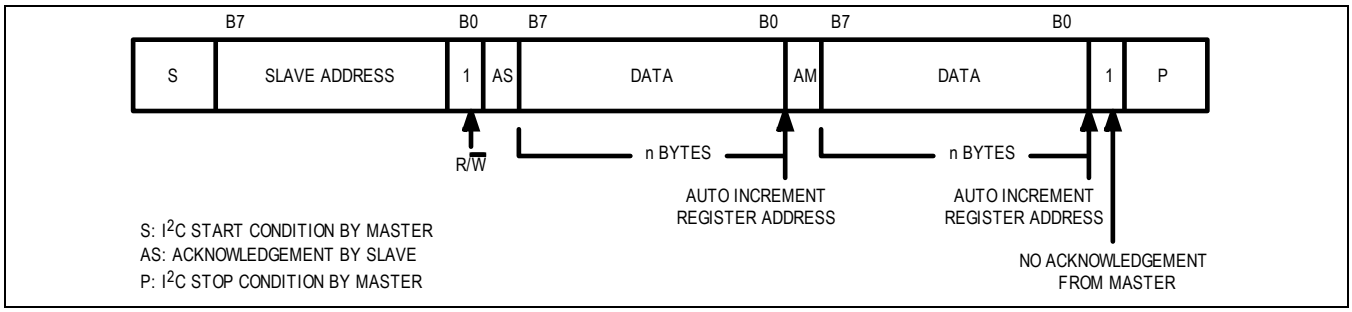


Figure 22. I²C Master Block Read

Register Map

TOP

I²C Slave Address

Slave Address (7 bit) 0x6B (7'b110 1011)
Slave Address (Write) 0xD6 (8'b1101 0110)
Slave Address (Read) 0xD7 (8'b1101 0111)

Functional Reset Conditions

The chip has different levels of reset as defined below:
• Type S: Registers are reset each time when: SYS < VDD (1.8V)
• Type O: Registers are reset each time when: SYS < VDD or SYS < SYS UVLO or SYS > SYS OVLO or die temp > T_{SHDN} or software reset (SW_RST)

ADDRESS	NAME	MSB							LSB
TOP_FUNC									
0x00	CHIP_ID[7:0]	ID[7:0]							
0x01	CHIP_REVISION[7:0]	VERSION[3:0]				REVISION[3:0]			
0x02	OTP_REVISION[7:0]	OTP_REV[7:0]							
0x03	TOP_INT[7:0]	TWARN_INT	TSHDN_INT	SYSOVLO_INT	SYSUVLO_INT	SPR_3_1[2:0]			PWRUP_FAIL_INT
0x04	TOP_INT_MASK[7:0]	TWARN_INT_M	TSHDN_INT_M	SYSOVLO_INT_M	SYSUVLO_INT_M	SPR_3_1[2:0]			PWRUP_FAIL_INT_M
0x05	TOP_CTRL[7:0]	–	SPR_6_4[2:0]			LPM	SYSOVLO_DIS	SYSOVLO_DEB_EN	TSHDN_DIS
0x50	SW_RESET[7:0]	SWR_RST[7:0]							
0x51	SM_CTRL[7:0]	SPR_7_1[6:0]							EXTSM_T
I2C_FUNC									
0x40	I2C_CNFG[7:0]	SPR_7	RSVD_6_5[1:0]		PAIR	SPR_3_1[2:0]			HS_EXT_EN

Register Details

CHIP_ID (0x0)

PMIC ID

BIT	7	6	5	4	3	2	1	0
Field	ID[7:0]							
Reset	0x86							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ID	7:0	ID of MAX77786/MAX77885	0x86: MAX77786 0x85: MAX77785

CHIP_REVISION (0x1)

PMIC revision

BIT	7	6	5	4	3	2	1	0
Field	VERSION[3:0]				REVISION[3:0]			
Reset	0xA				0x3			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VERSION	7:4	Version	0b1010: MAX77785/MAX77786 base 0b1011: For a variation
REVISION	3:0	Revision	0b001: PASS1 0b010: PASS2 0b011: PASS3 0b100: PASS4

OTP_REVISION (0x2)

BIT	7	6	5	4	3	2	1	0
Field	OTP_REV[7:0]							
Reset	0x0A							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP_REV	7:0	OTP Recipe Revision

TOP_INT (0x3)

Top SYS Interrupts

BIT	7	6	5	4	3	2	1	0
Field	TWARN_INT	TSHDN_INT	SYSOVLO_INT	SYSUVLO_INT	SPR_3_1[2:0]			PWRUP_FAIL_INT
Reset	0b0	0b0	0b0	0b0	0b000			0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All			Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
TWARN_INT	7	Thermal Alarm Interrupt (entering fault condition)	0b0: No interrupt. 0b1: Interrupt is detected.
TSHDN_INT	6	Thermal Shutdown Interrupt (entering fault condition)	0b0: No interrupt. 0b1: Interrupt is detected.
SYSOVLO_INT	5	SYSOVLO Interrupt (entering fault condition)	0b0: No interrupt. 0b1: Interrupt is detected.
SYSUVLO_INT	4	SYSUVLO Interrupt (entering fault condition)	0b0: No interrupt. 0b1: Interrupt is detected.
SPR_3_1	3:1		
PWRUP_FAIL_INT	0	Power-Up Fail Interrupt (entering fault condition)	0b0: No interrupt. 0b1: Interrupt is detected.

TOP_INT_MASK (0x4)

Top SYS Interrupt Mask

BIT	7	6	5	4	3	2	1	0
Field	TWARN_INT_M	TSHDN_INT_M	SYSOVLO_INT_M	SYSUVLO_INT_M	SPR_3_1[2:0]			PWRUP_FAIL_INT_M
Reset	0b1	0b1	0b1	0b1	0b111			0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TWARN_INT_M	7	Thermal Alarm Interrupt Mask	0b0: Unmasked 0b1: Masked
TSHDN_INT_M	6	Thermal Shutdown Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSOVLO_INT_M	5	SYSOVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSUVLO_INT_M	4	SYSUVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SPR_3_1	3:1		
PWRUP_FAIL_INT_M	0	Power-Up Fail Interrupt Mask	0b0: Unmasked 0b1: Masked

TOP_CTRL (0x5)

Main Control1

BIT	7	6	5	4	3	2	1	0
Field	–	SPR_6_4[2:0]			LPM	SYSOVLO_DIS	SYSOVLO_DEB_EN	TSHDN_DIS
Reset	–	0b000			0b0	0b0	0b0	0b1
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_6_4	6:4		
LPM	3	Low-Power Mode Cycling mode is allowed for SYS UVLO, SYS OVLO, and THERM comparators.	
SYSOVLO_DIS	2	SYSOVLO Disable	
SYSOVLO_DEB_EN	1	SYSOVLO Debounce (Rising 5ms)	
TSHDN_DIS	0	Internal Die Temperature Shutdown Disable Bit. In case a valid CHGIN is detected or MODE = 0x1, this bit has no effect and the Internal Die Temperature Comparator is permanently enabled.	0b0: T_{SHDN} comparator is enabled. 0b1: T_{SHDN} comparator is disabled unless a valid CHGIN is detected or MODE = 0x1.

SW_RESET (0x50)

SW-reset register

BIT	7	6	5	4	3	2	1	0
Field	SWR_RST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SWR_RST	7:0	Software Reset	0xA5: O-Type registers are reset.

SM_CTRL (0x51)

SW-reset register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_1[6:0]							EXTSM_T

Reset	0b0000000	0b0
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SPR_7_1	7:1	
EXTSM_T	0	External Ship Mode Timer

I2C_CNFG (0x40)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	RSVD_6_5[1:0]		PAIR	SPR_3_1[2:0]			HS_EXT_EN
Reset	0b0	0b00		0b0	0b000			0b0
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	
RSVD_6_5	6:5	Reserved	
PAIR	4	Pair Address Mode Option for Register Write Burst Operation	
SPR_3_1	3:1		
HS_EXT_EN	0	Enable HS-Mode Extension	0b0: HS-mode extension is disabled. (I^2C Rev. 4 Compliant) 0b1: HS-mode extension is enabled. HS-mode is enabled without HS-mode entrance code and keeps HS-mode during STOP condition.

CHARGER

ADDRESS	NAME	MSB							LSB
CHARGER_FUNC									
0x10	CHG_INT[7:0]	AICL_I	CHGIN_I	INLIM_I	CHG_I	BAT_I	SYSAICL_I	DISQBAT_I	BYP_I
0x11	CHG_INT_MASK[7:0]	AICL_M	CHGIN_M	INLIM_M	CHG_M	BAT_M	SYSAICL_M	DISQBAT_M	BYP_M

ADDRESS	NAME	MSB							LSB
0x12	CHG_INT_OK[7:0]	AICL_OK	CHGIN_OK	INLIM_OK	CHG_OK	BAT_OK	SYSAICL_OK	DISQBAT_OK	BYP_OK
0x13	CHG_DETAILS_0[7:0]	TWARN	CHGIN_DTLS[1:0]		SPR_4_3[1:0]		SPSN_DTLS[1:0]		SYS_REG_OK
0x14	CHG_DETAILS_1[7:0]	FRS_STS	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
0x15	CHG_DETAILS_2[7:0]	TREG	THM_DTLS[2:0]			BYP_DTLS[3:0]			
0x16	MODE_CNFG[7:0]	SPR_7_4[3:0]				MODE[3:0]			
0x17	INPUT_CNFG_0[7:0]	SPR_7	CHGIN_ILIM[6:0]						
0x18	INPUT_CNFG_1[7:0]	CHGIN_OVLO_DEB[1:0]		INLIM_CLK[1:0]		NO_AUTOIBUS	DIS_AICL	VCHGIN_REG[1:0]	
0x19	TRICKLE_CNFG[7:0]	TKEN	VTRICKLE[2:0]			SPR_3_0[3:0]			
0x1A	CC_CNFG[7:0]	SPR_7	CHG_CC[6:0]						
0x1B	CC_LNR_CNFG[7:0]	SPR_7_6[1:0]		CHG_CC_LNR[5:0]					
0x1C	CV_CNFG[7:0]	SPR_7	CHG_CV_PRM[6:0]						
0x1D	TOP_OFF_CNFG[7:0]	TO_TIME[2:0]			TO_ITH[4:0]				
0x1E	RESTART_CNFG[7:0]	WDTCLR[1:0]		CHG_RSTRT[1:0]		WDTEN	FCHGTIME[2:0]		
0x1F	JEITA_CNFG[7:0]	JEITA_EN	CV_BCKOFF	CHG_CV_COOL	CHG_CC_WARM	SPR_3	REGTEMP[2:0]		
0x20	QBAT_CNFG_0[7:0]	B2SOVRC_DTC	B2SOVRC_ALARM_ONLY	B2SOVRC_CTRL	RECYCLE_EN	B2SOVRC[3:0]			
0x21	QBAT_CNFG_1[7:0]	WD_QBATOFF	FMBST	DISIBS	SPSN_DET_EN	QBEXT_CTRL_EN	–	BATRMV_MSK	FSHIP_MODE
0x22	MINSYS_CNFG[7:0]	–	–	–	–	–	MINSYS[2:0]		
0x23	SYSAICL_CNFG[7:0]	SPR_7_6[1:0]		SYSAICL[5:0]					

ADDRESS	NAME	MSB							LSB
0x24	BCKSYS_CNFG[7:0]	SPR_7_6[1:0]		BCKSYS[5:0]					
0x25	BUCK_CNFG_0[7:0]	AUDIO_MODE	SPR_6_2[4:0]					FSW	DISKIP
0x26	BUCK_CNFG_1[7:0]	SPR_7_6[1:0]		SS_FREQ[1:0]		SS_PAT[1:0]		SS_ENV[1:0]	
0x27	LNR_CNFG[7:0]	–	–	–	–	–	–	–	EXT_SYS
0x28	WR_PROT[7:0]	SPR_7_2[5:0]						CHGPROT[1:0]	
0x29	RVS_BOOST_CNFG_0[7:0]	OTG_REC_EN	AUDIO_MODE	SPR_5	OTG_ILIM[4:0]				
0x2A	RVS_BOOST_CNFG_1[7:0]	SPR_7	VBYPSET[6:0]						
0x2B	UNPLUG_DET_CNFG[7:0]	UNPLUG_DB	SPR_6	UNPLUG_TH[5:0]					
0x2C	STAT_CNFG[7:0]	BYPDISCHG_EN	DEEP_SUSP_DIS	SPR_5_4[1:0]		STAT_CURR[1:0]		STAT_MODE	STAT_EN

Register Details

CHG_INT (0x10)

Interrupt status register for the charger block.

BIT	7	6	5	4	3	2	1	0
Field	AICL_I	CHGIN_I	INLIM_I	CHG_I	BAT_I	SYSAICL_I	DISQBAT_I	BYP_I
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_I	7	AICL Interrupt	0b0: The AICL_OK bit has not changed since the last time this bit was read. 0b1: The AICL_OK bit has changed since the last time this bit was read.
CHGIN_I	6	CHGIN Interrupt	0b0: The CHGIN_OK bit has not changed since the last time this bit was read. 0b1: The CHGIN_OK bit has changed since the last time this bit was read or FRS_STS bit has changed.

BITFIELD	BITS	DESCRIPTION	DECODE
INLIM_I	5	Input Current Limit Interrupt	0b0: The INLIM_OK bit has not changed since the last time this bit was read. 0b1: The INLIM_OK bit has changed since the last time this bit was read.
CHG_I	4	Charger Interrupt	0b0: The CHG_OK bit has not changed since the last time this bit was read. 0b1: The CHG_OK bit has changed since the last time this bit was read.
BAT_I	3	Battery Interrupt	0b0: The BAT_OK bit has not changed since the last time this bit was read. 0b1: The BAT_OK bit has changed since the last time this bit was read.
SYSAICL_I	2	SYS Interrupt for Linear Charger in Q_{BAT}	0x0: The SYS_OK bit has not changed since the last time this bit was read. Only works for MODE 1 and 7. 0x1: The SYS_OK bit has changed since the last time this bit was read. Only works for MODE 1 and 7.
DISQBAT_I	1	DISQBAT Interrupt	0b0: The DISQBAT_OK bit has not changed since the last time this was read. 0b1: The DISQBAT_OK bit has changed since the last time this was read.
BYP_I	0	Bypass Node Interrupt	0b0: The BYP_OK bit has not changed since the last time this bit was read. 0b1: The BYP_OK bit has changed since the last time this bit was read.

CHG_INT_MASK (0x11)

Mask register to mask the corresponding charger interrupts.

BIT	7	6	5	4	3	2	1	0
Field	AICL_M	CHGIN_M	INLIM_M	CHG_M	BAT_M	SYSAICL_M	DISQBAT_M	BYP_M
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_M	7	AICL Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGIN_M	6	CHGIN Interrupt Mask	0b0: Unmasked 0b1: Masked
INLIM_M	5	Input Current Limit Interrupt Mask	0b0: Unmasked 0b1: Masked
CHG_M	4	Charger Interrupt Mask	0b0: Unmasked 0b1: Masked
BAT_M	3	Battery Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSAICL_M	2	Battery Interrupt Mask	0x0: Unmasked 0x1: Masked
DISQBAT_M	1	DISQBAT Interrupt Mask	0b0: Unmasked 0b1: Masked
BYP_M	0	Bypass Interrupt Mask	0b0: Unmasked 0b1: Masked

CHG_INT_OK (0x12)

BIT	7	6	5	4	3	2	1	0
Field	AICL_OK	CHGIN_OK	INLIM_OK	CHG_OK	BAT_OK	SYSAICL_OK	DISQBAT_OK	BYP_OK
Reset	0b1	0b0	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_OK	7	AICL_OK Status	0b0: AICL mode 0b1: Not in AICL mode.
CHGIN_OK	6	CHGIN Input Status Indicator	0b0: The CHGIN input is invalid. CHGIN_DTLS ≠ 0x03 0b1: The CHGIN input is valid. CHGIN_DTLS = 0x03
INLIM_OK	5	Input Current Limit Status Indicator	0b0: The CHGIN input current has been reaching the current limit for at least 30ms. 0b1: The CHGIN input current has not reached the current limit.
CHG_OK	4	Charger Status Indicator	0b0: The charger has suspended charging or T_{REG} = 1. 0b1: The charger is okay or the charger is off.
BAT_OK	3	Battery Status Indicator	0b0: The battery has an issue or the charger has been suspended. BAT_DTLS ≠ 0x03, ≠0x04 and ≠0x07 0b1: The battery is okay. BAT_DTLS = 0x03, 0x04, or 0x07
SYSAICL_OK	2		0x0: The SYS input is invalid. SYS ≤ SYSAICL 0x1: The SYS input is valid. SYS > SYSAICL
DISQBAT_OK	1	DISQBAT Status Indicator	0b0: DISQBAT is high and Q_{BATT} is disabled. 0b1: DISQBAT is low and Q_{BATT} is not disabled.
BYP_OK	0	Bypass Status Indicator.	0b0: Something powered by the bypass node has hit the current limit. BYP_DTLS ≠ 0x00 0b1: The bypass node is okay. BYP_DTLS = 0x00

CHG_DETAILS_0 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	TWARN	CHGIN_DTLS[1:0]		SPR_4_3[1:0]		SPSN_DTLS[1:0]		SYS_REG_OK
Reset	0b0	0b00		0b00		0b00		0b1
Access Type	Read Only	Read Only		Read Only		Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TWARN	7	Temperature Regulation Status	0b0: The junction temperature is less than the thermal alarm threshold. 0b1: The junction temperature is greater than the thermal alarm threshold.
CHGIN_DTLS	6:5	CHGIN Details	0b00: V_{BUS} is invalid. V_{CHGIN} rising: $V_{CHGIN} < V_{CHGIN\_UVLO}$ V_{CHGIN} falling: $V_{CHGIN} < V_{CHGIN\_REG}$ (AICL) 0b01: V_{BUS} is invalid. $V_{CHGIN} < V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0b10: V_{BUS} is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0b11: V_{BUS} is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ and $V_{CHGIN} > V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} < V_{CHGIN\_OVLO}$

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_4_3	4:3		
SPSN_DTLS	2:1	SP/SN Remonte Sense Battery Line Connection Status	0b00: SPSN remote sense line is connected. 0b01: SP remote sense line detected as opened. 0b10: SN remote sense line detected as opened. 0b11: SP and SN remote sense lines are both detected as opened.
SYS_REG_OK	0	In MODE 4 only, indicating SYS is on regulation or not (do not use in other modes, always 0 in the other mode).	0b0: SYS is not regulation yet. 0b1: SYS is on regulation.

CHG_DETAILS_1 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	FRS_STS	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
FRS_STS	7	Fast Role Swap Status	0b0: ENBST pin driven low or FAST_ROLE_SWAP_EN bit is 0. 0b1: rvs boost operation initiated by ENBST driven high when FAST_ROLE_SWAP_EN bit is 1.
BAT_DTLS	6:4	Battery Details	0b000: Battery Removal A valid adpater is present and the battery is detached, detected on THM pin. 0b001: Battery Prequalification Voltage A valid adapter is present and the battery voltage is low: $V_{BATT} < V_{TRICKLE}$. **Note:** This condition is also reported in the CHG_DTLS as 0x00. 0b010: Battery Timer Fault A valid adapter is present and the battery has taken longer than expected to charge (exceeded t_{FC}). This could be due to high system currents, an old battery, a damaged battery, or something else. Charging has suspended and the charger is in timer-fault mode. **Note:** This condition is also reported in the CHG_DTLS as 0x06. 0b011: Battery Regular Voltage A valid adapter is present and the battery voltage is greater than the minimum system regulation level but lower than the overvoltage level: $V_{MINSYS} < V_{BATT} < V_{BATTREG} + V_{COV}$ V_{SYS} is approximately equal to V_{BATT}. Only valid with MODE = 0x5, ignore in the other Mode. 0b100: Battery Low Voltage A valid adapter is present and the battery voltage is lower than the minimum system regulation level but higher than prequalification voltage: $V_{TRICKLE} < V_{BATT} < V_{MINSYS}$ V_{SYS} is regulated at least equal to V_{SYSMIN}. Only valid with MODE = 0x5, ignore in the other Mode. 0b101: Battery Overvoltage A valid adapter is present and the battery voltage is greater than the battery-overvoltage threshold ($V_{BATTREG} + V_{COV}$) for the last 30ms.

BITFIELD	BITS	DESCRIPTION	DECODE
			Note: This flag is only generated when there is a valid input. 0b110: Battery Overcurrent The battery current has exceeded the battery-overcurrent threshold (I_{BOVRC}) for at least 3ms since the last time this register was read. 0b111: Battery Only, No Overcurrent No valid adapter is present and battery current is lower than battery-overcurrent threshold (I_{BOVRC}). The battery voltage and battery removal monitoring are not available. **Note:** In case of deep suspend, it is considered that no valid adapter is present.
CHG_DTLS	3:0	Charger Details	0x00: Charger is in dead-battery prequalification or low-battery prequalification mode. CHG_OK = 1 and $V_{BATT} < V_{PQLB}$ and $T_J < T_{SHDN}$ 0x01: Charger is in fast-charge constant current mode. CHG_OK = 1 and $V_{BATT} < V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x02: Charger is in fast-charge constant voltage mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x03: Charger is in top-off mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x04: Charger is in done mode. CHG_OK = 0 and $V_{BATT} > V_{BATTREG} - V_{RSTRT}$ and $T_J < T_{SHDN}$ 0x05: Reserved 0x06: Charger is in timer-fault mode. CHG_OK = 0 and if BAT_DTLS = 0b001 then $V_{BATT} < V_{PQLB}$ or $V_{BATT} < V_{PQDB}$ and $T_J < T_{SHDN}$ 0x07: Charger is suspended because Q_{BATT} is disabled (DISQBAT = H or DISIBS = 1). CHG_OK = 0 0x08: Charger is off, charger input invalid and/or charger is disabled. CHG_OK = 1 0x09: Reserved 0x0A: Charger is off and the junction temperature is > T_{SHDN}. CHG_OK = 0 0x0B: Charger is off because the watchdog timer expired. CHG_OK = 0 0x0C: Charger is suspended or charge current or voltage is reduced based on JEITA control. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0D: Charger is suspended because battery removal is detected on THM pin. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0E: Charger is suspended because SUSPEND pin is high. CHG_OK = 0 0x0F: Reserved

CHG_DETAILS_2 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	TREG	THM_DTLS[2:0]			BYP_DTLS[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	7	Temperature Regulation Status	0b0: The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 0b1: The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.
THM_DTLS	6:4	Thermistor Details	0b000: Low temperature and charging suspended (COLD). 0b001: Low temperature charging (COOL). 0b010: Normal temperature charging (NORMAL). 0b011: High temperature charging (WARM). 0b100: High temperaure and charging suspended (HOT). 0b101: Battery removal detected on THM pin. 0b110: Thermistor monitoring is disabled. 0b111: RSVD
BYP_DTLS	3:0	Bypass Node Details	0x0: The bypass node is okay. 0x1: OTG_ILIM when CHG_CNFG_00.MODE = 0xA or 0xE or 0xF The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. BYP_DTLS[0] status bit is latched until CHG_DETAILS_02 register read access is performed by AP. 0x2: BSTILIM The BYP reverse boost converter has hit its current limit and condition persisted for 30ms. 0x4: BCKNegILIM The BYP buck converter has hit the max negative demand current limit. BYP_DTLS[2] status bit is latched until CHG_DETAILS_02 register read access is performed by AP. 0x8: BST_SWON_DONE (This status bit is only available in CHG_CNFG_00.MODE = 0x9) The BYP reverse boost converter switch-on is done and V_{BYP} reached the V_{BYPSET} target.

MODE_CNFG (0x16)

Charger configuration 0

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_4[3:0]				MODE[3:0]			
Reset	0b0000				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_4	7:4	Reserved	
MODE	3:0	Smart Power Selector Configuration	0x0: Charger = off, OTG = off, buck = off, boost = off. The Q_{BATT} switch is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability. 0x1: Charger = off, OTG = off, buck = off, boost = off. The Q_{BATT} switch works as linear charger as well as allows the

BITFIELD	BITS	DESCRIPTION	DECODE
			battery to support the system. 0x2: Same as 0x0. 0x3: Same as 0x0. 0x4: Charger = off, OTG = off, buck = on, boost = off. When there is a valid input, the buck converter regulates the system voltage to be the maximum of (V_{BCKSYS} or V_{BATT} + V_{TRACK}). V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x5: Charger = on, OTG = off, buck = on, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{MINSYS} and ~V_{BATT} + I_{BATT} x RBAT2SYS. V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x6: Same as 0x5. 0x7: Charger = off, OTG = off, buck = on, boost = off. When there is a valid input, the buck converter regulates the system voltage to be the maximum of (V_{BCKSYS} or V_{BATT} + V_{TRACK}). The Q_{BATT} switch works as a linear charger as well as allows the battery to support the system. 0x8: Reserved 0x9: Charger = off, OTG = off, buck = off, boost = on. The Q_{BATT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. BYP voltage is regulated to V_{BYPSET}. Q_{CHGIN} is off. 0xA: Charger = off, OTG = on, buck = off, boost = on. The Q_{BATT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. BYP voltage is regulated to V_{BYPSET}. Q_{CHGIN} is on allowing it to source current up to ICHGIN.OTG.LIM. 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

INPUT_CNFG_0 (0x17)

Charger configuration 1

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	CHGIN_ILIM[6:0]						
Reset	0b0	0b0001001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	
CHGIN_ILIM	6:0	CHGIN Input Current Limit (mA) 7-Bit Adjustment: From 0.05A to 3.5A in 50mA steps (MAX77785A/B) From 0.05A to 5.5A in 50mA steps (MAX77786A/B)	0x00: 50 0x01: 50 0x02: 100 0x03: 150 0x04: 200 0x05: 250 0x06: 300 0x07: 350

BITFIELD	BITS	DESCRIPTION	DECODE
			0x08: 400 0x09: 450 0x0A: 500 0x0B: 550 0x0C: 600 0x0D: 650 0x0E: 700 0x0F: 750 0x10: 800 0x11: 850 0x12: 900 0x13: 950 0x14: 1000 0x15: 1050 0x16: 1100 0x17: 1150 0x18: 1200 0x19: 1250 0x1A: 1300 0x1B: 1350 0x1C: 1400 0x1D: 1450 0x1E: 1500 0x1F: 1550 0x20: 1600 0x21: 1650 0x22: 1700 0x23: 1750 0x24: 1800 0x25: 1850 0x26: 1900 0x27: 1950 0x28: 2000 0x29: 2050 0x2A: 2100 0x2B: 2150 0x2C: 2200 0x2D: 2250 0x2E: 2300 0x2F: 2350 0x30: 2400 0x31: 2450 0x32: 2500 0x33: 2550 0x34: 2600 0x35: 2650 0x36: 2700 0x37: 2750 0x38: 2800 0x39: 2850 0x3A: 2900 0x3B: 2950 0x3C: 3000 0x3D: 3050 0x3E: 3100 0x3F: 3150 0x40: 3200 0x41: 3250 0x42: 3300 0x43: 3350 0x44: 3400 0x45: 3450 0x46: 3500 0x47: 3550 0x48: 3600 0x49: 3650 0x4A: 3700 0x4B: 3750 0x4C: 3800 0x4D: 3850

BITFIELD	BITS	DESCRIPTION	DECODE
			0x4E: 3900 0x4F: 3950 0x50: 4000 0x51: 4050 0x52: 4100 0x53: 4150 0x54: 4200 0x55: 4250 0x56: 4300 0x57: 4350 0x58: 4400 0x59: 4450 0x5A: 4500 0x5B: 4550 0x5C: 4600 0x5D: 4650 0x5E: 4700 0x5F: 4750 0x60: 4800 0x61: 4850 0x62: 4900 0x63: 4950 0x64: 5000 0x65: 5050 0x66: 5100 0x67: 5150 0x68: 5200 0x69: 5250 0x6A: 5300 0x6B: 5350 0x6C: 5400 0x6D: 5450 0x6E: 5500

INPUT_CNFG_1 (0x18)

Charger configuration 2

BIT	7	6	5	4	3	2	1	0
Field	CHGIN_OVLO_DEB[1:0]		INLIM_CLK[1:0]		NO_AUTOIBUS	DIS_AICL	VCHGIN_REG[1:0]	
Reset	0b10		0b10		0b0	0b0	0b01	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_OVLO_DEB	7:6	CHGIN_OVLO Comparator Debounce Time	0b00: No debounce 0b01: 100µs 0b10: 5ms 0b11: 7ms
INLIM_CLK	5:4	Input Current Limit Soft-Start Clock (µsec per 50mA step)	0b00: 16 0b01: 512 0b10: 2048 0b11: 8192
NO_AUTOIBUS	3	CHGIN Current Control	0b0: CHGIN current limit controlled by BC1P2 detection. 0b1: CHGIN current limit controlled by CHGIN_ILIM.
DIS_AICL	2	AICL Disable Feature	0b0: AICL feature is not disabled. 0b1: AICL feature is disabled.

BITFIELD	BITS	DESCRIPTION	DECODE
VCHGIN_REG	1:0	CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment. The CHGIN to GND minimum turn-on threshold (V_{CHGIN_UVLO}) also scales with this adjustment.	0b00: V_{CHGIN_REG} = 4.5V and V_{CHGIN_UVLO} = 4.7V 0b01: V_{CHGIN_REG} = 4.6V and V_{CHGIN_UVLO} = 4.8V 0b10: V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 4.9V 0b11: V_{CHGIN_REG} = 4.9V and V_{CHGIN_UVLO} = 5.1V

TRICKLE_CNFG (0x19)

Charger configuration 3

BIT	7	6	5	4	3	2	1	0
Field	TKEN	VTRICKLE[2:0]			SPR_3_0[3:0]			
Reset	0b1	0b000			0b0000			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TKEN	7	Trickle Charge Enable	0b0: Trickle charge is disabled: When V_{BATT} is in trickle charge voltage range, charge current target level is I_{FC}. 0b1: Trickle charge is enabled: When V_{BATT} is in trickle charge voltage range, charge current target level is $I_{TRICKLE}$.
VTRICKLE	6:4	Trickle Charge Threshold	0x0: 2.8V 0x1: 2.9V 0x2: 3.0V 0x3: 3.1V 0x4: 3.2V 0x5: 3.3V 0x6: 3.4V 0x7: 3.5V
SPR_3_0	3:0	Reserved	

CC_CNFG (0x1A)

Charger configuration 4

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	CHG_CC[6:0]						
Reset	0b0	0b0001001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	
CHG_CC	6:0	Fast-Charge Current Selection (mA). When the charger is enabled, the charge current limit is set by	Value: Decode 0x00: 50 0x01: 50

BITFIELD	BITS	DESCRIPTION	DECODE
		these bits. Note that the thermal-foldback loop can reduce the battery charger's target current by ATJREG. From 0.05A to 3.5A in 50mA steps (MAX77785A/B) From 0.05A to 5.5A in 50mA steps (MAX77786A/B) Note that the first two codes are both 0.05A.	0x02: 100 0x03: 150 0x04: 200 0x05: 250 0x06: 300 0x07: 350 0x08: 400 0x09: 450 0x0A: 500 0x0B: 550 0x0C: 600 0x0D: 650 0x0E: 700 0x0F: 750 0x10: 800 0x11: 850 0x12: 900 0x13: 950 0x14: 1000 0x15: 1050 0x16: 1100 0x17: 1150 0x18: 1200 0x19: 1250 0x1A: 1300 0x1B: 1350 0x1C: 1400 0x1D: 1450 0x1E: 1500 0x1F: 1550 0x20: 1600 0x21: 1650 0x22: 1700 0x23: 1750 0x24: 1800 0x25: 1850 0x26: 1900 0x27: 1950 0x28: 2000 0x29: 2050 0x2A: 2100 0x2B: 2150 0x2C: 2200 0x2D: 2250 0x2E: 2300 0x2F: 2350 0x30: 2400 0x31: 2450 0x32: 2500 0x33: 2550 0x34: 2600 0x35: 2650 0x36: 2700 0x37: 2750 0x38: 2800 0x39: 2850 0x3A: 2900 0x3B: 2950 0x3C: 3000 0x3D: 3050 0x3E: 3100 0x3F: 3150 0x40: 3200 0x41: 3250 0x42: 3300 0x43: 3350 0x44: 3400 0x45: 3450 0x46: 3500 0x47: 3550

BITFIELD	BITS	DESCRIPTION	DECODE
			0x48: 3600 0x49: 3650 0x4A: 3700 0x4B: 3750 0x4C: 3800 0x4D: 3850 0x4E: 3900 0x4F: 3950 0x50: 4000 0x51: 4050 0x52: 4100 0x53: 4150 0x54: 4200 0x55: 4250 0x56: 4300 0x57: 4350 0x58: 4400 0x59: 4450 0x5A: 4500 0x5B: 4550 0x5C: 4600 0x5D: 4650 0x5E: 4700 0x5F: 4750 0x60: 4800 0x61: 4850 0x62: 4900 0x63: 4950 0x64: 5000 0x65: 5050 0x66: 5100 0x67: 5150 0x68: 5200 0x69: 5250 0x6A: 5300 0x6B: 5350 0x6C: 5400 0x6D: 5450 0x6E~0x7F: 5500

CC_LNR_CNFG (0x1B)

Charger configuration 5

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		CHG_CC_LNR[5:0]					
Reset	0b00		0b000010					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6	Reserved	
CHG_CC_LNR	5:0	Fast-Charge Current Selection (mA) for MODE 0x1 and 0x7	0x0: 50mA 0x1: 50mA 0x2: 100mA 0x3: 150mA 0x4: 200mA 0x5: 250mA 0x6: 300mA

BITFIELD	BITS	DESCRIPTION	DECODE
			0x7: 350mA 0x8: 400mA 0x9: 450mA 0xA: 500mA 0xB: 550mA 0xC: 600mA 0xD: 650mA 0xE: 700mA 0xF: 750ma 0x10: 800mA 0x11: 850mA 0x12: 900mA 0x13: 950mA 0x14: 1000mA 0x15: 1050mA 0x16: 1100mA 0x17: 1150mA 0x18: 1200mA 0x19: 1250mA 0x1A: 1300mA 0x1B: 1350mA 0x1C: 1400mA 0x1D: 1450mA 0x1E: 1500mA 0x1F: 1550mA 0x20: 1600mA 0x21: 1650mA 0x22: 1700mA 0x23: 1750mA 0x24: 1800mA 0x25: 1850mA 0x26: 1900mA 0x27: 1950mA 0x28: 2000mA 0x29: 2050mA 0x2A: 2100mA 0x2B: 2150mA 0x2C: 2200mA 0x2D: 2250mA 0x2E: 2300mA 0x2F: 2350mA 0x30: 2400mA 0x31: 2450mA 0x32: 2500mA 0x33~0x3F: clampled at 2.5A

CV_CNFG (0x1C)

Charger configuration 6

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	CHG_CV_PRM[6:0]						
Reset	0b0	0b1000110						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV_PRM	6:0		0x0: 3.50V 0x1: 3.51V 0x2: 3.52V 0x3: 3.53V 0x4: 3.54V 0x5: 3.55V 0x6: 3.56V 0x7: 3.57V 0x8: 3.58V 0x9: 3.59V 0xA: 3.60V 0xB: 3.61V 0xC: 3.62V 0xD: 3.63V 0xE: 3.64V 0xF: 3.65V 0x10: 3.66V 0x11: 3.67V 0x12: 3.68V 0x13: 3.69V 0x14: 3.70V 0x15: 3.71V 0x16: 3.72V 0x17: 3.73V 0x18: 3.74V 0x19: 3.75V 0x1A: 3.76V 0x1B: 3.77V 0x1C: 3.78V 0x1D: 3.79V 0x1E: 3.80V 0x1F: 3.81V 0x20: 3.82V 0x21: 3.83V 0x22: 3.84V 0x23: 3.85V 0x24: 3.86V 0x25: 3.87V 0x26: 3.88V 0x27: 3.89V 0x28: 3.90V 0x29: 3.91V 0x2A: 3.92V 0x2B: 3.93V 0x2C: 3.94V 0x2D: 3.95V 0x2E: 3.96V 0x2F: 3.97V 0x30: 3.98V 0x31: 3.99V 0x32: 4.00V 0x33: 4.01V 0x34: 4.02V 0x35: 4.03V 0x36: 4.04V 0x37: 4.05V 0x38: 4.06V 0x39: 4.07V 0x3A: 4.08V 0x3B: 4.09V 0x3C: 4.10V 0x3D: 4.11V 0x3E: 4.12V 0x3F: 4.13V 0x40: 4.14V 0x41: 4.15V 0x42: 4.16V 0x43: 4.17V 0x44: 4.18V 0x45: 4.19V

BITFIELD	BITS	DESCRIPTION	DECODE
			0x46: 4.20V 0x47: 4.21V 0x48: 4.22V 0x49: 4.23V 0x4A: 4.24V 0x4B: 4.25V 0x4C: 4.26V 0x4D: 4.27V 0x4E: 4.28V 0x4F: 4.29V 0x50: 4.30V 0x51: 4.31V 0x52: 4.32V 0x53: 4.33V 0x54: 4.34V 0x55: 4.35V 0x56: 4.36V 0x57: 4.37V 0x58: 4.38V 0x59: 4.39V 0x5A: 4.40V 0x5B: 4.41V 0x5C: 4.42V 0x5D: 4.43V 0x5E: 4.44V 0x5F: 4.45V 0x60: 4.46V 0x61: 4.47V 0x62: 4.48V 0x63: 4.49V 0x64: 4.50V 0x65: 4.51V 0x66: 4.52V 0x67: 4.53V 0x68: 4.54V 0x69: 4.55V 0x6A: 4.56V 0x6B: 4.57V 0x6C: 4.58V 0x6D: 4.59V 0x6E: 4.60V 0x6F~0x7F: clamped at 4.6V

TOP_OFF_CNFG (0x1D)

Charger configuration 7

BIT	7	6	5	4	3	2	1	0
Field	TO_TIME[2:0]			TO_ITH[4:0]				
Reset	0b011			0b00100				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TO_TIME	7:5	Top-Off Timer Setting (min)	0b000: 30sec 0b001: 10 0b010: 20 0b011: 30 0b100: 40 0b101: 50

BITFIELD	BITS	DESCRIPTION	DECODE
			0b110: 60 0b111: 70
TO_ITH	4:0	Top-Off Current Threshold (mA). The charger transitions from its fast charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME.	0x0: Disable 0x1: 50mA 0x2: 100mA 0x3: 150mA 0x4: 200mA 0x5: 250mA 0x6: 300mA 0x7: 350mA 0x8: 400mA 0x9: 450mA 0xA: 500mA 0xB: 550mA 0xC: 600mA 0xD: 650mA 0xE: 700mA 0xF: 750mA 0x10: 800mA 0x11: 850mA 0x12: 900mA 0x13: 950mA 0x14: 1000mA 0x15~0x1F: clamped at 1A

RESTART_CNFG (0x1E)

Charger configuration 8

BIT	7	6	5	4	3	2	1	0
Field	WDTCLR[1:0]		CHG_RSTRT[1:0]		WDTEN	FCHGTIME[2:0]		
Reset	0b00		0b10		0b0	0b011		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
WDTCLR	7:6	Watchdog Timer Clear Bit. Writing "01" to these bits clears the watchdog timer when the watchdog timer is enabled.	0b00: The watchdog timer is not cleared. 0b01: The watchdog timer is cleared. 0b10: The watchdog timer is not cleared. 0b11: The watchdog timer is not cleared.
CHG_RSTRT	5:4	Charger-Restart Threshold	0b00: 100mV below the value programmed by CHG_CV_PRM. 0b01: 150mV below the value programmed by CHG_CV_PRM. 10: 200mV below the value programmed by CHG_CV_PRM. 11: Disabled
WDTEN	3	Watchdog Timer Enable Bit	0b0: Watchdog timer disabled. 0b1: Watchdog timer enabled.
FCHGTIME	2:0	Fast-Charge Timer Setting (t_{FC}, hrs)	0b000: Disable 0b001: 3 0b010: 4 0b011: 5 0b100: 6 0b101: 7 0b110: 8 0b111: 10

JEITA_CNFG (0x1F)

Charger configuration 9

BIT	7	6	5	4	3	2	1	0
Field	JEITA_EN	CV_BCKOFF	CHG_CV_COOL	CHG_CC_WARM	SPR_3	REGTEMP[2:0]		
Reset	0b0	0b0	0b0	0b0	0b0	0b101		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
JEITA_EN	7	JEITA Enable	0x0: JEITA Disabled Fast charge current and charge termination voltage do not change based on thermistor temperature. 0x1: JEITA Enabled Fast charge current and charge termination voltage change based on thermistor temperature.
CV_BCKOFF	6	Battery Termination Voltage Back Off in JEITA Feature	0x0: -100mV 0x1: -150mV
CHG_CV_COOL	5	JEITA controlled battery termination voltage when thermistor temperature is between T_{COLD} and T_{COOL}.	0x0: Battery termination voltage is set by CHG_CV_PRM. 0x1: Battery termination voltage is set to CHG_CV_PRM - CV_BCKOFF.
CHG_CC_WARM	4	JEITA controlled battery fast charge current when thermistor temperature is between T_{WARM} and T_{HOT}.	0x0: Battery fast-charge current is set by CHG_CC. 0x1: Battery fast-charge current is to 50% of CHG_CC.
SPR_3	3	Reserved	
REGTEMP	2:0	Junction Temperature Thermal Regulation (ºC). The charger's target current limit starts to foldback and the T_{REG} bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x0: 86 0x1: 92 0x2: 98 0x3: 104 0x4: 110 0x5: 116 0x6: 122 0x7: 128

QBAT_CNFG_0 (0x20)

Charger configuration 10

BIT	7	6	5	4	3	2	1	0
Field	B2SOVRC_DTC	B2SOVRC_ALARM_ONLY	B2SOVRC_CTRL	RECYCLE_EN	B2SOVRC[3:0]			
Reset	0b0	0b0	0b0	0b0	0b1101			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
B2SOVRC_DTC	7	BATT to SYS Overcurrent Debounce to Q_{BATT} Clear Control	0x0: 105µs 0x1: 10ms
B2SOVRC_ALARM_ONLY	6	B2SOVRC Alarm Only Control	0x0: Alarm only is disabled: when tripping B2SOVRC, I/T is triggered and Q_{BATT} opens after T_{OCP}. 0x1: Alarm only is enabled: when tripping B2SOVRC, I/T is triggered but Q_{BATT} remains closed even after T_{OCP}.
B2SOVRC_CTRL	5	Battery Mode B2SOVRC Monitoring Control	0x0: Automatic mode 0x1: Continuous mode
RECYCLE_EN	4	B2S OCP or DISIBS Event Recycle Option	0b0: In case of B2S OCP **or** DISIBS events, buck is disabled (OFF) and Q_{BATT} FET is opened. System recycles after 150ms (min) only in case a valid charger is present. 0b1: In case of B2S OCP **or** DISIBS events, buck is disabled (OFF) and Q_{BATT} FET is opened. System recycles after 150ms (min).
B2SOVRC	3:0	BATT to SYS Overcurrent Threshold (A)	0x0: Disabled 0x1: 3.0 0x2: 3.5 0x3: 4.0 0x4: 4.5 0x5: 5.0 0x6: 5.5 0x7: 6.0 0x8: 6.5 0x9: 7.0 0xA: 7.5 0xB: 8.0 0xC: 8.5 0xD: 9.0 0xE: 9.5 0xF: 10.0

QBAT_CNFG_1 (0x21)

Charger configuration 11

BIT	7	6	5	4	3	2	1	0
Field	WD_QBATOFF	FMBST	DISIBS	SPSN_DET_EN	QBEXT_CTRL_EN	–	BATRMV_MSK	FSHIP_MODE
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WD_QBATOFF	7	Q_{BATT} FET Control Under Watchdog Condition	0b0: When watchdog timer expires, turn off only the charger. 0b1: When watchdog timer expires, turn off buck, charger, and Q_{BATT} switch for 150ms.
FMBST	6	Factory Mode Boost	0b0: When DISQBAT = high, any mode change is not possible.

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1: When DISQBAT = high, this bit makes mode change (Boost mode) possible.
DISIBS	5	BATT to SYS FET Disable Control	0b0: BATT to SYS FET is controlled by the power-path state machine. 0b1: BATT to SYS FET is forced off.
SPSN_DET_EN	4	SPSN Remote Sense Line Detection Enable. Enable SPSN remote sense line detection only when MODE = 0x0 (*detection is discarded if not*). End of SPSN detction triggers a BAT_I interrupt. Detection result available in dedicated status bit field SPSN_DTLS[1:0].	0b0: SPSN remote sense line detection disabled. 0b1: SPSN remote sense line detection enabled.
QBEXT_CTRL_EN	3		0b0: External Q_{BATT} control is disabled. 0b1: External Q_{BATT} control is enabled.
BATRMV_MSK	1	Battery Removal Detection Masking When masked, battery removal detection is ignored.	0b0: Unmasked 0b1: Masked
FSHIP_MODE	0	Factory-Ship Mode. When asserted to "1", system enters into factory-ship mode. This bit can be reset by battery removal or on a valid charger input plug.	0b0: Not factory-ship mode. 0b1: Factory-ship mode.

MINSYS_CNFG (0x22)

Charger configuration 12

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MINSYS[2:0]		
Reset	–	–	–	–	–	0b101		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MINSYS	2:0	Minimum System Regulation Voltage (V_{MINSYS}, V) The MINSYS should be lower than CHG_CV_PRM - 200mV so if it is set higher then the state machine forces to clamp MINSYS at CHG_CV_PRM - 200mV. In this case, users have the readback value of CHG_CV_PRM - 200mV, not the written value.	0x0: 3.0V 0x1: 3.1V 0x2: 3.2V 0x3: 3.3V 0x4: 3.4V 0x5: 3.5V 0x6: 3.6V 0x7: 3.7V

SYSAICL_CNFG (0x23)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		SYSAICL[5:0]					

Reset	0b00	0b001010
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6	Reserved	
SYSAICL	5:0	SYSAICL Level in MODE 1	0x0: 2.85V 0x1: 2.90V 0x2: 2.95V 0x3: 3.00V 0x4: 3.05V 0x5: 3.10V 0x6: 3.15V 0x7: 3.20V 0x8: 3.25V 0x9: 3.30V 0xA: 3.35V 0xB: 3.40V 0xC: 3.45V 0xD: 3.50V 0xE: 3.55V 0xF: 3.60V 0x10: 3.65V 0x11: 3.70V 0x12: 3.75V 0x13: 3.80V 0x14: 3.85V 0x15: 3.90V 0x16: 3.95V 0x17: 4.00V 0x18: 4.05V 0x19: 4.10V 0x1A: 4.15V 0x1B: 4.20V 0x1C: 4.25V 0x1D: 4.30V 0x1E: 4.35V 0x1F: 4.40V 0x20: 4.45V 0x21: 4.50V 0x22: 4.55V 0x23: 4.60V 0x24: 4.65V 0x25: 4.70V 0x26: 4.75V 0x27: 4.80V 0x28: 4.85V 0x29~0x3F: clamped at 4.85V

BCKSYS_CNFG (0x24)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		BCKSYS[5:0]					
Reset	0b00		0b001010					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6	Reserved	
BCKSYS	5:0	SYS Level in MODES 4, 7	0x0: 3.00V 0x1: 3.05V 0x2: 3.10V 0x3: 3.15V 0x4: 3.20V 0x5: 3.25V 0x6: 3.30V 0x7: 3.35V 0x8: 3.40V 0x9: 3.45V 0xA: 3.50V 0xB: 3.55V 0xC: 3.60V 0xD: 3.65V 0xE: 3.70V 0xF: 3.75V 0x10: 3.80V 0x11: 3.85V 0x12: 3.90V 0x13: 3.95V 0x14: 4.00V 0x15: 4.05V 0x16: 4.10V 0x17: 4.15V 0x18: 4.20V 0x19: 4.25V 0x1A: 4.30V 0x1B: 4.35V 0x1C: 4.40V 0x1D: 4.45V 0x1E: 4.50V 0x1F: 4.55V 0x20: 4.60V 0x21: 4.65V 0x22: 4.70V 0x23: 4.75V 0x24: 4.80V 0x25: 4.85V 0x26: 4.90V 0x27: 4.95V 0x28: 5.00V 0x29~0x3F: clamped at 5V **Note:** Do not set BCKSYS > CHGIN - 0.3V

BUCK_CNFG_0 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_MODE	SPR_6_2[4:0]					FSW	DISKIP
Reset	0b0	0b0000					0b1	0b0
Access Type	Write, Read	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_MODE	7	Audio Mode Control Bit	0x0: No Audio mode enabled. 0x1: Audio mode enabled.

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_6_2	6:2	Reserved	
FSW	1	Switching Frequency Options (MHz)	0b0: Do not use 0b1: 1.3
DISKIP	0	Charger Skip Mode Disable	0b0: Auto skip mode. 0b1: Disable skip mode.

BUCK_CNFG_1 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_6[1:0]		SS_FREQ[1:0]		SS_PAT[1:0]		SS_ENV[1:0]	
Reset	0b00		0b11		0b11		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_6	7:6	Reserved	
SS_FREQ	5:4	Spread Spectrum Pattern Frequency (FSS_MOD)	0x0: 3kHz 0x1: 5kHz 0x2: 7kHz 0x3: 25kHz
SS_PAT	3:2	Spread Spectrum Pattern Type	0x0: Triangular (Linear) pattern 0x1: Psuedo Random Pattern 1 repeats 0x2: Rsuedo Random Pattern 2 repeats 0x3: Psuedo Random Pattern 1 and 2 repeats
SS_ENV	1:0	Spread Spectrum Control Register Bits	0x0: Disabled 0x1: 4% modulation envelope 0x2: 8% modulation envelope 0x3: 16% modulation envelope

LNR_CNFG (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EXT_SYS
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
EXT_SYS	0	EXT_SYS flag to be set or cleared during MODE 1 entry (before applying external voltage to SYS) and exit sequence (after disabling external voltage to SYS). This flag is used internally to MAX77785/MAX77786 to avoid Q_{BAT} FET shorting BAT to SYS while SYS is driven by an external source.

WR_PROT (0x28)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_2[5:0]						CHGPROT[1:0]	
Reset	0b000000						0b00	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_2	7:2	Reserved	
CHGPROT	1:0	Charger Settings Protection Bit Writing "11" to these bits unlocks the write capability for the registers who are "Protected with CHGPROT". Writing any value besides "11" locks these registers.	0b00: Write capability locked. 0b01: Write capability locked. 0b10: Write capability locked. 0b11: Write capability unlocked.

RVS_BOOST_CNFG_0 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	OTG_REC_EN	AUDIO_MODE	SPR_5	OTG_ILIM[4:0]				
Reset	0b0	0b0	0b00	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OTG_REC_EN	7	OTG OCP Event Recycle Option	1b0: In case of OTG OCP, OTG FET is disabled (OFF = opened). System does not recycle OTG output. 1b1: In case of OTG OCP, OTG FET is disabled (OFF = opened). OTG recycles after T_{OTG}, retry.
AUDIO_MODE	6	USB Fast Role Swap Control Bit	0x0: FRS disabled 0x1: FRS enabled
SPR_5	5	Reserved	
OTG_ILIM	4:0	CHGIN OTG Output Current Limit (mA) When the boost-OTG mode (MODE = 0xA) is enabled, the OTG output current limit is set by these bits. These bits range from 0.50A (0x00) to 3.1A (0x1A) in 100mA steps. Note that the OTG output current limit is clamped at 2.4A from 0x13 to 0x1F in MAX77985.	Value: Decode 0x00: 500 0x01: 600 0x02: 700 0x03: 800 0x04: 900 0x05: 1000 0x06: 1100 0x07: 1200 0x08: 1300 0x09: 1400 0x0A: 1500 0x0B: 1600 0x0C: 1700

BITFIELD	BITS	DESCRIPTION	DECODE
			0x0D: 1800 0x0E: 1900 0x0F: 2000 0x10: 2100 0x11: 2200 0x12: 2300 0x13: 2400 0x14: 2500 0x15: 2600 0x16: 2700 0x17: 2800 0x18: 2900 0x19: 3000 0x1A: 3100 0x1B: 3100 0x1C: 3100 0x1D: 3100 0x1E: 3100 0x1F: 3100

RVS_BOOST_CNFG_1 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	VBYPSET[6:0]						
Reset	0b0	0b0000001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	
VBYPSET	6:0	V_{BYP} Target Output Voltage (V). Bypass target output voltage in boost mode. MODE = 0x9/0xA. 4.505V to 10.805V with 90mV step.	0x00: 4.505V 0x01: 4.595V 0x02: 4.685V 0x03: 4.775V 0x04: 4.865V 0x05: 4.955V 0x06: 5.045V 0x07: 5.135V 0x08: 5.225V 0x09: 5.315V 0x0A: 5.405V 0x0B: 5.495V 0x0C: 5.585V 0x0D: 5.675V 0x0E: 5.765V 0x0F: 5.855V 0x10: 5.945V 0x11: 6.035V 0x12: 6.125V 0x13: 6.215V 0x14: 6.305V 0x15: 6.395V 0x16: 6.485V 0x17: 6.575V 0x18: 6.665V 0x19: 6.755V 0x1A: 6.845V 0x1B: 6.935V

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1C: 7.025V 0x1D: 7.115V 0x1E: 7.205V 0x1F: 7.295V 0x20: 7.385V 0x21: 7.475V 0x22: 7.565V 0x23: 7.655V 0x24: 7.745V 0x25: 7.835V 0x26: 7.925V 0x27: 8.015V 0x28: 8.105V 0x29: 8.195V 0x2A: 8.285V 0x2B: 8.375V 0x2C: 8.465V 0x2D: 8.555V 0x2E: 8.645V 0x2F: 8.735V 0x30: 8.825V 0x31: 8.915V 0x32: 9.005V 0x33: 9.095V 0x34: 9.185V 0x35: 9.275V 0x36: 9.365V 0x37: 9.455V 0x38: 9.545V 0x39: 9.635V 0x3A: 9.725V 0x3B: 9.815V 0x3C: 9.905V 0x3D: 9.995V 0x3E: 10.085V 0x3F: 10.175V 0x40: 10.265V 0x41: 10.355V 0x42: 10.445V 0x43: 10.535V 0x44: 10.625V 0x45: 10.715V 0x46~0x7F: 10.805V

UNPLUG_DET_CNFG (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	UNPLUG_DB	SPR_6	UNPLUG_TH[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
UNPLUG_DB	7	V_{BUS} Unplug Detection Debounce Selection	0b0: No debounce 0b1: 2µs
SPR_6	6	Reserved	
UNPLUG_TH	5:0	V_{BUS} Unplug Detection Enabling and Threshold If written other value than 0b00, the QBEXT pin	0x0: Disabled (functions as QBEXT) 0x1: CHGIN_REG (AICL enabled) or $V_{CHGIN\_UVLO\_F}$ (AICL

BITFIELD	BITS	DESCRIPTION	DECODE
		works as an unplug detection active-low output (so called /PGOOD)	disabled) 0x2: 7.95V 0x3: 8.00V 0x4: 8.05V 0x5: 8.10V 0x6: 8.15V 0x7: **8.20V** 0x8: 8.25V 0x9: 8.30V 0xA: 8.35V 0xB: 8.40V 0xC: 8.45V 0xD: 8.50V 0xE: 8.55V 0xF: 8.60V 0x10: 8.65V 0x11: 8.70V 0x12: 8.75V 0x13: 8.80V 0x14: 8.85V 0x15: 8.90V 0x16: 8.95V 0x17: **9.00V** 0x18: 9.05V 0x19: 9.10V 0x1A: 9.15V 0x1B: 9.20V 0x1C: 9.25V 0x1D: 9.30V 0x1E: 9.35V 0x1F: 9.40V 0x20: 12.75V 0x21: 12.80V 0x22: 12.85V 0x23: 12.90V 0x24: 12.95V 0x25: 13.00V 0x26: 13.05V 0x27: **13.10V** 0x28: 13.15V 0x29: 13.20V 0x2A: 13.25V 0x2B: 13.30V 0x2C: 13.35V 0x2D: 13.40V 0x2E: 13.45V 0x2F: 13.50V 0x30: 17.50V 0x31~0x3F: Reserved

STAT_CNFG (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	BYPDISCHG_EN	DEEP_SUSP_DIS	SPR_5_4[1:0]		STAT_CURR[1:0]		STAT_MODE	STAT_EN
Reset	0b0	0b0	0b00		0b00		0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BYPDISCHG_EN	7	Boost BYP Discharge after Overshoot When enabled, if BYP is seen to be above target, a soft pulldown is activated to discharge BYP back to target, even if auto-skip mode is active.	0b0: Disabled 0b1: Enabled
DEEP_SUSP_DIS	6	When SUSPND pin pulls high or in MODE 0, input FET is enabled or disabled by this bit.	0b0: Input FET disabled 0b1: Input FET Enabled
SPR_5_4	5:4	Reserved	
STAT_CURR	3:2	STAT LED Driving Current (mA)	0b00: 5 0b01: 10 0b10: 15 0b11: 20
STAT_MODE	1	STAT LED Behaviour Selection Bit	0b0: LED MODE 1 0b1: LED MODE 2
STAT_EN	0	STAT Charging Status Indication LED Enable Bit	0x0: Disable 0x1: Enable

USB

ADDRESS	NAME	MSB							LSB
BC1P2									
0x30	ALERT1[7:0]	–	USB_OVPInt	dnVdatRefInt	chgTypRunFInt	chgTypRunRInt	prChgTypInt	dcdTmoInt	chgTypInt
0x31	ALERT_MASK1[7:0]	–	MSK_USB_OVP	MSK_dnVDatRef	MSK_chgTypRunF	MSK_chgTypRunR	MSK_PrchgTyp	MSK_dcdTmo	MSK_chgTyp
0x32	BC_STATUS1[7:0]	–	ChgTypRun	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
0x33	BC_STATUS2[7:0]	dnDebOk	–	dnVlgc	dnVdatRef	dpDebOk	–	dpVlgc	dpVdatRef
0x34	OVP_STATUS[7:0]	–	–	–	–	–	–	USBDP_OVP	USBDN_OVP
0x35	BC_CTRL1[7:0]	dcdCpl	–	noBcComp	DCP3ADetEn	–	–	chgDetMan	ChgDetEn
0x36	BC_CTRL2[7:0]	dpMonEn	–	dnMonEn	dpDnMan	dpDrv[1:0]		dnDrv[1:0]	
0x37	USBSW_CTRL[7:0]	–	–	–	–	–	–	USB_SW_CTRL[1:0]	

Register Details

ALERT1 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	USB_OVPInt	dnVdatRefInt	chgTypRunFInt	chgTypRunRInt	prChgTypInt	dcdTmoInt	chgTypInt
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
USB_OVPInt	6	DP/DN Over Voltage Interrupt	0x0: No Interrupt 0x1: New DP/DN Over Voltage Interrupt
dnVdatRefInt	5	DN Vdat_ref Interrupt	0x0: No Interrupt 0x1: New DN Vdat_ref interrupt
chgTypRunFInt	4	Charger Detection Running Falling Edge Interrupt	0x0: No Interrupt 0x1: New Charger Detection Running falling edge interrupt
chgTypRunRInt	3	Charger Detection Running Rising Edge Interrupt	0x0: No Interrupt 0x1: New Charger Detection Running rising edge interrupt
prChgTypInt	2	BC1.2 Proprietary Charger Type Interrupt	0x0: No Interrupt 0x1: New Proprietary Charger Type Interrupt
dcdTmoInt	1	Data Contact Detect Interrupt	0x0: No Interrupt 0x1: New Data Contact Detect Interrupt
chgTypInt	0	BC1.2 Charger Type Interrupt	0x0: No Interrupt 0x1: New Charger Type Interrupt

ALERT_MASK1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	MSK_USB_OVP	MSK_dnVDatRef	MSK_chgTypRunF	MSK_chgTypRunR	MSK_PrchgTyp	MSK_dcdTmo	MSK_chgTyp
Reset	–	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_USB_OVP	6	DP/DN Over Voltage Interrupt Mask	0x0: Unmasked 0x1: Masked
MSK_dnVDatRef	5		0x0: Unmasked 0x1: Masked
MSK_chgTypRunF	4	Charger Detection Running Falling Edge Interrupt Mask	0x0: Unmasked 0x1: Masked
MSK_chgTypRunR	3	Charger Detection Running Rising Edge Interrupt Mask	0x0: Unmasked 0x1: Masked

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_PrchgTyp	2	Proprietary Charger Type Interrupt Mask	0x0: Unmasked 0x1: Masked
MSK_dcdTmo	1	Data Contact Detect Interrupt Mask	0x0: Unmasked 0x1: Masked
MSK_chgTyp	0	Charger Type Interrupt Mask	0x0: Unmasked 0x1: Masked

BC_STATUS1 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	–	ChgTypRun	PrChgTyp[2:0]			DCDTmo	ChgTyp[1:0]	
Reset	–	0b0	0b000			0b0	0b00	
Access Type	–	Read Only	Read Only			Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
ChgTypRun	6	Charger Detection Running Status	0x0: Not running 0x1: Running
PrChgTyp	5:3	Proprietary Charger Type	0x0: Not proprietary charger 0x1: Samsung 2A 0x2: Apple 500mA 0x3: Apple 1A 0x4: Apple 2A 0x5: Apple 2.4A 0x6: 3A DCP (If enabled AND chgTyp = DCP) 0x7: Reserved
DCDTmo	2	DCD Detection Timeout	0x0: No timeout or detection has not run. 0x1: DCD timeout occured
ChgTyp	1:0	Output of Charger Detection	0x0: Nothing attached 0x1: SDP 0x2: CDP 0x3: DCP

BC_STATUS2 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	dnDebOk	–	dnVlgc	dnVdatRef	dpDebOk	–	dpVlgc	dpVdatRef
Reset	0b0	–	0b0	0b0	0b0	–	0b0	0b0
Access Type	Read Only	–	Read Only	Read Only	Read Only	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
dnDebOk	7	When high, DN debouncer are stable.
dnVlgc	5	DN_VLGC Status

BITFIELD	BITS	DESCRIPTION
dnVdatRef	4	DN_VDATRef Status
dpDebOk	3	When high, DP debouncer are stable.
dpVlgc	1	DP_VLGC Status
dpVdatRef	0	DP_VDATRef Status

OVP_STATUS (0x34)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	USBDP_OVP	USBDN_OVP
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
USBDP_OVP	1	Current Value of DP OVP	0x0: DP < V_{OVDX_THF} 0x1: DP > V_{OVDX_THR}
USBDN_OVP	0	Current Value of DN OVP	0x0: DN < V_{OVDX_THF} 0x1: DN > V_{OVDX_THR}

BC_CTRL1 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	dcdCpl	–	noBcComp	DCP3ADetEn	–	–	chgDetMan	ChgDetEn
Reset	0b1	–	0b0	0b0	–	–	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dcdCpl	7	Data Contact Detection Wait Time	0x0: 2000ms 0x1: 800ms
noBcComp	5	BC1.2 Compatibility	0x0: BC1.2 compliant, continuously source VDP_SRC while in state DCP_END 0x1: Not BC1.2 compliant, do not source VDP_SRC while in state DCP_END
DCP3ADetEn	4	Enable Detection of DCP 3A Charger	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
chgDetMan	1	Force Manual Run of Charger Detection—Bit Auto Resets to 0	0x0: Not enabled 0x1: Request manual run of charger detection, run when $V_{BUS} > V_{CHGIN\_UVLO}$.
ChgDetEn	0	Enable Charger Detection	0x0: Not enabled 0x1: Enabled, charger detection runs every time CHGIN > V_{CHGIN_UVLO} (rising).

BC_CTRL2 (0x36)

Control DP/DN analog resources when CHGIN is present

BIT	7	6	5	4	3	2	1	0
Field	dpMonEn	–	dnMonEn	dpDnMan	dpDrv[1:0]		dnDrv[1:0]	
Reset	0b0	–	0b0	0b0	0b00		0b00	
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
dpMonEn	7	Enable Monitor of D+ Line with the VDATREF Comparator	0x0: Disabled 0x1: Enabled
dnMonEn	5	Enable Monitor of D- Line with the VDATREF Comparator	0x0: Disabled 0x1: Enabled
dpDnMan	4		0x0: Resources on DP and DN are controlled by charger detection FSM. 0x1: Drive voltages on DP and DN according to DPDrv and DNDrv.
dpDrv	3:2		0x0: 20K pd to ground 0x1: 0.6V 0x2: 3.0V 0x3: Open
dnDrv	1:0	Force Voltage on DP	0x0: 20K pd to ground 0x1: 0.6V 0x2: 3.0V 0x3: Open

USBSW_CTRL (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	USB_SW_CTRL[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
USB_SW_CTRL	1:0	USB Switch Control Bits After the detection done, if an SDP or CDP are detected, then DP/DN automatically connect to DP1/DN1. Writing to the USB_SW_CTRL register while charger detection is running does not have any effect. Any new charger detection makes the USB switch control back to automatic.	0b00: DP/DN open 0b01: DP/DN connected to DP1/DN1 0b10: DP-DN connected to BC1.2 charger detection (read-only, cannot be forced) 0b11: Reserved

Components Recommendation

Capacitor Recommendation

All capacitors should be X5R dielectric or better. *Table 11* shows the recommended capacitors after operating voltage derating consideration.

Table 11. Capacitor Recommendation

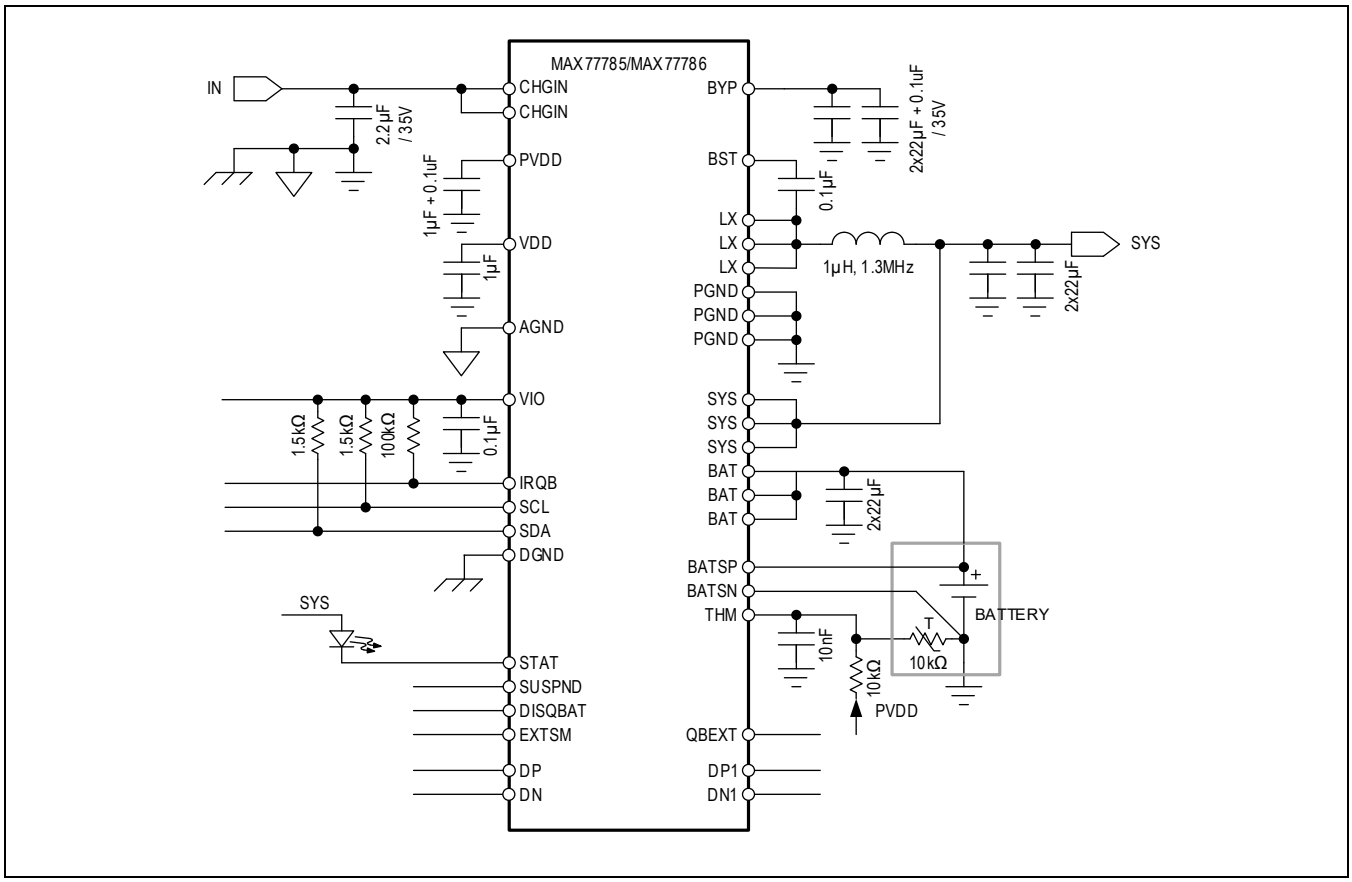
PIN	CAPACITORS
CHGIN Capacitor	2.2µF/35V
BYP Capacitor	2x22µF/35V or 4x10µF/35V + 0.1µF/50V
SYS Capacitor	2x22µF/16V
BATT Capacitor	2x22µF/16V
BST Capacitor	0.1µF/10V
VDD Capacitor	1µF/10V
PVDD Capacitor	1µF/10V + 0.1µF/10V
VIO Capacitor	0.1µF/10V

Inductor Recommendation

Table 12. Inductor Recommendation

SWITCHING FREQUENCY (MHz)	MANUFACTURER	PART NUMBER	INDUCTANCE (µH)	I_{SAT} (TYP) (A)	I_{RMS} (TYP) (A)	DCR (TYP) (mΩ)	SIZE (L x W x T) (mm)
1.3MHz	PULSE ELECTRONICS	PA5002.102NLT	1.0µH	12.8	10.5	12	5.5 x 5.3 x 1.8
1.3MHz	VISHAY DALE	IHLP2020CZER1R0M01	1.0µH	12	9.2	13.1	5.18 x 5.18 x 3.0

Typical Application Circuits



Layout Guidelines

1) Place CHGIN, BYP, SYS, and BATT bypass capacitors as close as possible to the IC pins and connect them to the power ground plane on the PCB top layer. Ensure the connection between the BYP capacitor ground and the SYS capacitor ground is as direct, short, and wide as possible. If possible, reinforce the connection between the BYP capacitor ground and the SYS capacitor ground in other layers.
2) Place the PVDD and VDD bypass capacitors as close as possible to the IC. This can reduce the loop area between the bypass capacitor and the IC.
3) Use wide and short traces for high-current connections such as CHGIN, BYP, LX, SYS, and BATT.
4) Use kelvin sensing for BATSP and BATSN to the interface of the battery. Connect as close as possible to the battery terminal so that the battery voltage is sensed correctly. Kelvin sensing traces should not be shared with other circuits.
5) Do not connect AGND directly with the top layer PGND. Allocate ground isolation between AGND and PGND. This can be done by connecting AGND to the system ground plane near the input capacitor. Usually, the input source's ground plane is more stable. Refer to the MAX77785/MAX77786 EV kit as an example.

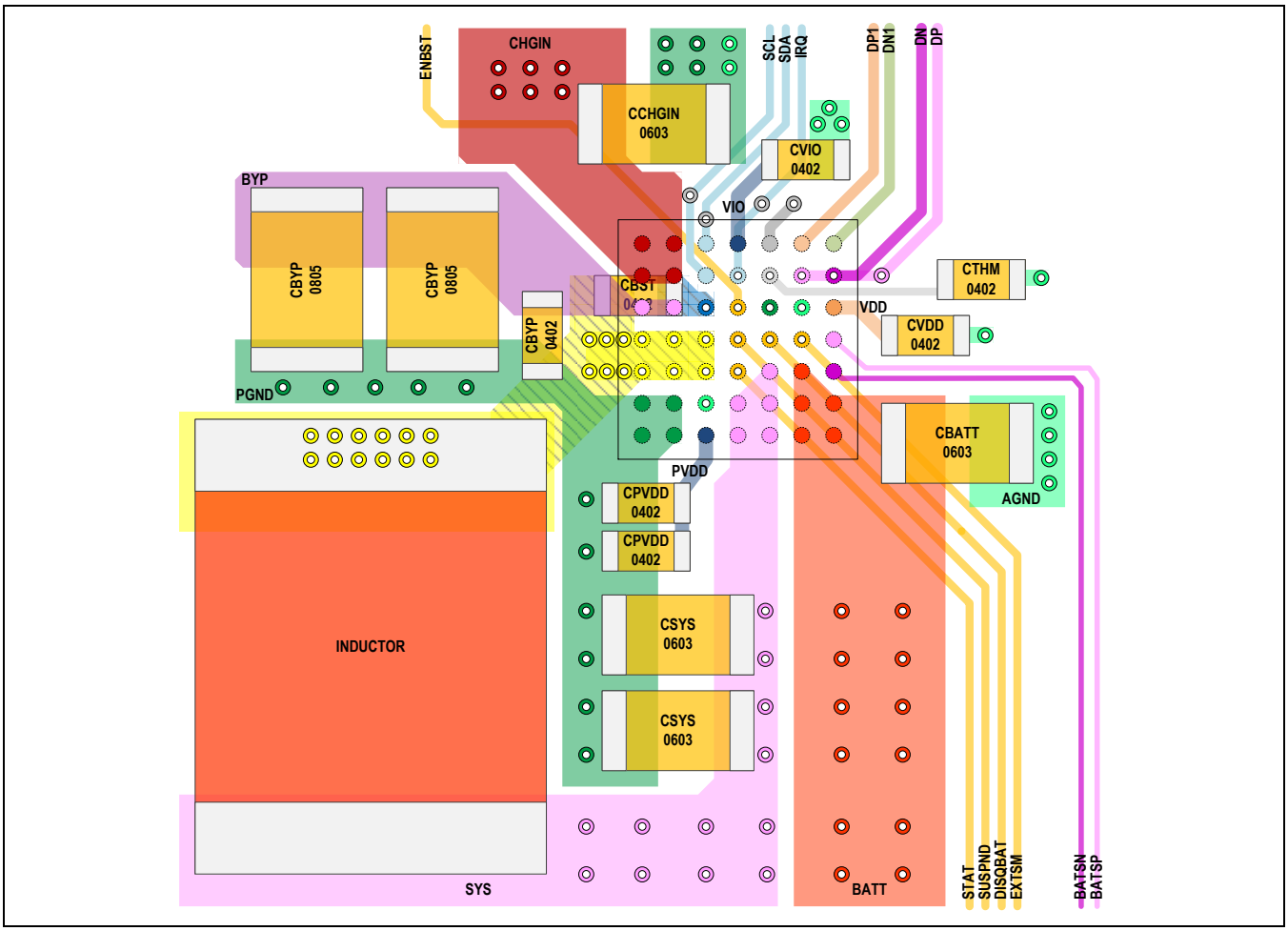


Figure 23. Recommended Placement and Layout

Ordering Information

PART NUMBER	TEMP RANGE	MAX FAST-CHARGE CURRENT (A)	INDUCTOR CURRENT LIMIT (A)	REVERSE BOOST POWER CEILING (W)	PIN-PACKAGE	DEFAULT MODE[3:0]
MAX77785EWJ+	-40°C to +85°C	3.5	8.3	10.8	7 x 7 WLP, 0.4mm pitch. 2.96mm x 2.96mm	0X4
MAX77785EWJ+T	-40°C to +85°C	3.5	8.3	10.8	7 x 7 WLP, 0.4mm pitch. 2.96mm x 2.96mm	0X4
MAX77786EWJ+	-40°C to +85°C	5.5	11.1	16.2	7 x 7 WLP, 0.4mm pitch. 2.96mm x 2.96mm	0X4
MAX77786EWJ+T	-40°C to +85°C	5.5	11.1	16.2	7 x 7 WLP, 0.4mm pitch. 2.96mm x 2.96mm	0X4

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/24	Release for Market Intro	—

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX77785EWJ+T MAX77786EWJ+T MAX77786EVKIT# MAX77785EVKIT# MAX77785EWJ+ MAX77786EWJ+