

SCOPE: MICROPROCESSOR SUPERVISORY CIRCUITS

<u>Device Type</u>	<u>Generic Number</u>
01	MAX705(x)/883B
02	MAX706(x)/883B
03	MAX707(x)/883B
04	MAX708(x)/883B
05	MAX813L(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM SMD			
JA P	GDIP1-T08 or CDIP2-T08	8 LEAD CERDIP	J08
LP 2	CQCC1-N20	20 Pin Leadless Chip	L20

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)

V_{CC} -0.3V to +6.0V

All other Inputs $\frac{1}{2}$ -0.3V to ($V_{CC}+0.3V$)

Input Current

V_{CC} 10mA

GND 10mA

Output Current (all outputs) 10mA

Lead Temperature (soldering, 10 seconds) +300°C

Storage Temperature -65°C to +160°C

Continuous Power Dissipation $T_A=+70^\circ\text{C}$

8 lead CERDIP(derate 8.0mW/°C above +70°C) 640mW

20 lead LCC(derate 9.1mW/°C above +70°C) 727mW

Junction Temperature T_J +150°C

Thermal Resistance, Junction to Case, Θ_{JC} :

Case Outline 8 lead CERDIP 55°C/W

Case Outline 20 leadless Chip carrier 20°C/W

Thermal Resistance, Junction to Ambient, Θ_{JA} :

Case Outline 8 lead CERDIP 125°C/W

Case Outline 20 leadless Chip carrier 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) -55°C to +125°C

Supply Voltage Range (V_{CC}) +1.2V to +5.5V

NOTE 1: The input voltage limits on PFI and MR may be exceeded if the input current is less than 10mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min 3/	Limits Max 3/	Units
		-55 °C ≤ T _A ≤ +125°C 2/ Unless otherwise specified					
Operating Voltage Range	V _{CC}		1,2,3	All	1.2	5.5	V
Supply Current	I		1,2,3	All		500	μA
RESET AND WATCHDOG TIMER							
Reset Threshold	V _{RT}		1,2,3	01,03,05	4.5	4.75	V
				02,04	4.25	4.5	
RESET Output Voltage	V _{RSTL}	I _{SOURCE} =800μA	1,2,3	01,02,03,04	V _{CC} -1.5		V
		I _{SINK} =3.2mA				0.4	
		I _{SINK} =100μA, V _{CC} =1.2V				0.3	
RESET Output Voltage	V _{RSTH}	I _{SOURCE} =800μA	1,2,3	03,04,05	V _{CC} -1.5		V
		I _{SINK} =1.2mA		03,04		0.4	
		I _{SOURCE} =4μA, V _{CC} =1.2V		05	0.9		
		I _{SINK} =3.2mA				0.4	
WDI Input Threshold Logic Low	WD _{VIL}	V _{CC} =5V	1,2,3	01,02,05		0.8	V
WDI Input Threshold Logic High	WD _{VIH}	V _{CC} =5V	1,2,3	01,02,05	3.5		V
WDI Input Current	WD _{IIN}	WDI=V _{CC}	1,2,3	01,02,05		150	μA
		WDI=0V			-150		
WDO Output Voltage	WDO _{VOH}	I _{SOURCE} =800μA	1,2,3	01,02,05	V _{CC} -1.5		V
	WDO _{VOL}	I _{SINK} =1.2mA				0.4	
Reset Pulse Width	t _{RS}		9,10,11	All	140	280	ms
Watchdog Timeout Period	t _{WD}		9,10,11	01,02,05	1.0	2.25	s
WDI Pulse Width	t _{WP}	V _{IL} =0.4V, V _{IH} =(V _{CC})(0.8)V	9,10,11	01,02,05	50		ns
MANUAL RESET							
MR Pull-up Current	MR _{IPU}	MR=0V	1,2,3	All	100	600	μA
MR Input Threshold Logic Low	MR _{VIL}		1,2,3	All		0.8	V
MR Input Threshold Logic High	MR _{VIH}		1,2,3	All	2.0		V

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min 3/	Limits Max 3/	Units
		-55 °C ≤ T _A ≤ +125 °C 2/ Unless otherwise specified					
MR to Reset Out Delay	t _{MD}	NOTE 4	9,10,11	All		250	ns
MR Pulse Width	t _{MR}		9,10,11	All	150		ns
POWER-FAIL DETECTOR							
PFI Input Threshold	PFI _{VTH}	V _{CC} =5V	1,2,3	All	1.2	1.3	V
PFI Input Current	PFI _{IN}		1,2,3	All	-25	+25	nA
PFO Output Voltage	PFO _{VO}	I _{SOURCE} =800μA I _{SINK} =3.2mA	1,2,3	All	V _{CC} -1.5	0.4	V

NOTE 2: For device types 01, 03, and 05, V_{CC}=4.75V to 5.5V unless otherwise specified and for device 02, 04, V_{CC}=4.5V to 5.5V unless otherwise specified.

NOTE 3: The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum is used for these limits. Negative current shall be defined as conventional current flow out of a device terminal.

NOTE 4: Applies to both RESET in device types 03-05 and RESET in device types 01 and 04.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	8 pin Cerdip	MAX705MJA/883B	5962-9326701MPA
01	20 pin LCC	MAX705MLP/883B	5962-9326701M2C
02	8 pin Cerdip	MAX706MJA/883B	5962-9326702MPA
02	20 pin LCC	MAX706MLP/883B	5962-9326702M2C
03	8 pin Cerdip	MAX707MJA/883B	5962-9326703MPA
03	20 pin LCC	MAX707MLP/883B	5962-9326703M2C
04	8 pin Cerdip	MAX708MJA/883B	5962-9326704MPA
04	20 pin LCC	MAX708MLP/883B	5962-9326704M2C
05	8 pin Cerdip	MAX813LMJA/883B	5962-9326705MPA
05	20 pin LCC	MAX813LMLP/883B	5962-9326705M2C

TERMINAL CONNECTIONS:

	MAX705/706	MAX705/706	MAX707/708	MAX707/708	MAX813L	MAX813L
	J8	L20	J8	L20	J8	L20
1	$\overline{\text{MR}}$	NC	$\overline{\text{MR}}$	NC	$\overline{\text{MR}}$	NC
2	V _{CC}	$\overline{\text{MR}}$	V _{CC}	$\overline{\text{MR}}$	V _{CC}	$\overline{\text{MR}}$
3	GND	NC	GND	NC	GND	NC
4	PFI	NC	PFI	NC	PFI	NC
5	$\overline{\text{PFO}}$	V _{CC}	$\overline{\text{PFO}}$	V _{CC}	$\overline{\text{PFO}}$	V _{CC}
6	WDI	NC	NC	NC	WDI	NC
7	$\overline{\text{RESET}}$	GND	$\overline{\text{RESET}}$	GND	RESET	GND
8	$\overline{\text{WDO}}$	NC	RESET	NC	$\overline{\text{WDO}}$	NC
9		NC		NC		NC
10		PFI		PFI		PFI
11		NC		NC		NC
12		$\overline{\text{PFO}}$		$\overline{\text{PFO}}$		$\overline{\text{PFO}}$
13		NC		NC		NC
14		NC		NC		NC
15		WDI		NC		WDI
16		NC		NC		NC
17		$\overline{\text{RST}}$		$\overline{\text{RST}}$		RST
18		NC		NC		NC
19		NC		NC		NC
20		$\overline{\text{WDO}}$		RST		$\overline{\text{WDO}}$

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1, 9

* PDA applies to Subgroup 1 only.

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