*Click **here** to ask an associate for production status of specific part numbers.*

MAX30210

±0.1°C Accurate, Ultra-Small, Low-Power I²C Digital Temperature Sensor

General Description

The MAX30210 operates from 1.7V to 2.0V supply voltage, and is a low-power, high-accuracy digital temperature sensor with ±0.1°C accuracy from +20°C to +50°C and ±0.15°C accuracy from -20°C to +85°C. The MAX30210 has a 16-bit resolution (0.005°C).

The device uses a standard I²C serial interface to communicate with a host controller. There are four functional I/Os. Those functions include a dedicated interrupt pin, a shared external convert and power-down functional pin, and two target address select pins.

The MAX30210 includes a 64-word FIFO for the temperature data and also includes high and low threshold digital temperature alarms along with FIFO full alert. The device is available in a 0.968mm x 0.968mm x 0.5mm, 9-pin WLP package.

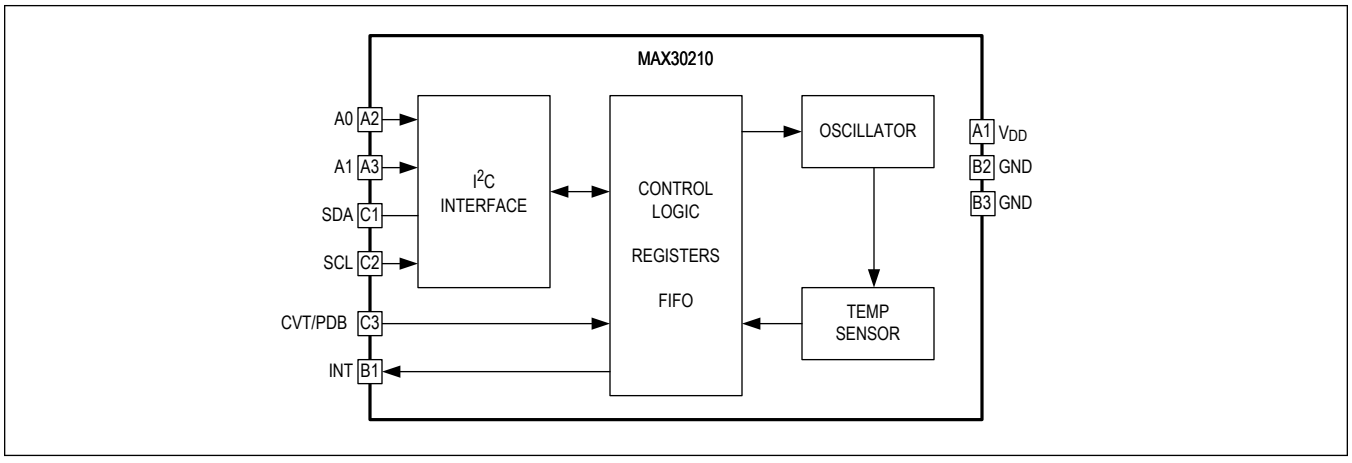
Applications

- Wearable Devices for Fitness, Wellness, and Medical Applications
- Medical Thermometers
- Hearing Aids
- Smart Clothing

Benefits and Features

- High Accuracy and Precision
  - ±0.1°C Accuracy from +20°C to +50°C
  - ±0.15°C Accuracy from -20°C to +85°C
- Low-Power Consumption
  - 1.7V to 2.0V Operating Voltage
  - 61µA Operating Current during Measurement
  - 0.75µA Standby Current
  - 10nA Power-Down Current
  - 8ms Integration Time
- Safety and Compliance
  - High and Low Temperature Alarms
- Digital Interface
  - Shared External Convert Temperature and Power-Down Input Pin
  - Dedicated Interrupt Output Pin
  - Autonomous Conversion Mode
  - 16 Different I²C Target Address Options
  - 48-Bit Unique ROM IDs Allow Device to be NIST Traceable

Simplified Block Diagram



Ordering Information appears at end of data sheet.

19-101474; Rev 0; 12/22

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Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +2.2V
SDA, SCL, A0, A1, CVT/PDB, INT to GND ..... -0.3V to +6.0V
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s).....+260°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

9-Pin WLP

Package Code	N90A0+1
Outline Number	21-100600
Land Pattern Number	Refer to the *Application Note 1891: Wafer-Level Packaging (WLP) and Its Applications*.
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	94°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 1.8V, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TEMPERATURE SENSOR							
Temperature Measurement Error		+20°C to +50°C	post reflow, 3 sigma	-0.1		+0.1	°C
		-20°C to +85°C	post reflow, 3 sigma	-0.15		+0.15	
Resolution		16-Bit			0.005		°C
Repeatability		V_{DD} = 1.8V, 1sps, 120 samples			0.008		°C RMS
Integration Time	t_{INT}				8		ms
Long-Term Stability		Mounted, T_A = 70°C, 0% RH			0.015		°C/ 1000hrs
Supply Voltage	V_{DD}			1.7	1.8	2.0	V
DC Power-Supply Rejection Ratio (PSRR)	PSRR	T_A = +25°C, 1.7V < VDD <2.0V			0.015		°C/V
Operating Current		During Conversion	V_{DD} = 1.8V		61	80	µA
Standby Current (Note 2a)		V_{DD} = 1.8V, T_A = +25°C			0.75	1.5	µA
		V_{DD} = 1.8V				3.0	
Power-Down Current (Note 2b)		V_{DD} = 1.8V, T_A = +25°C			0.01	0.15	µA
		V_{DD} = 1.8V				0.3	

Electrical Characteristics (continued)

(V_{DD} = 1.8V, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-On Reset Threshold		Rising Edge			1.530		V
		Falling Edge			1.465		
DIGITAL I/O CHARACTERISTICS							
Input Voltage High	V_{IH}	SDA, SCL, A0, A1, and CVT/PDB pins only		1.4			V
Input Voltage Low	V_{IL}	SDA, SCL, A0, A1, and CVT/PDB pins only				0.4	V
Input Hysteresis	V_{HYS}	SDA, SCL, A0, A1, and CVT/PDB pins only			200		mV
Input Leakage Current	I_{IN}	SDA, SCL, A0, A1, and CVT/PDB pins only	0V < V_{IN} < 5.5V, T_A = 25°C	- 0.1		+ 0.1	µA
Input Capacitance	C_{IN}	SDA, SCL, A0, A1, and CVT/PDB pins only			10		pF
Input Low-Pulse Width		CVT/PDB pin only		5			µs
Output Voltage High	V_{OH}	INT pin only	I_{SOURCE} = 2mA	V_{DD}-0.4			V
Output Voltage Low	V_{OL}	INT pin only	I_{SINK} = 2mA			0.4	V
Open-Drain Output Low Voltage	V_{OL_OD}	SDA and INT pins only	I_{SINK} = 6mA			0.4	V
I²C TIMING CHARACTERISTICS (Note 3)							
Serial Clock Frequency	f_{SCL}			0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
Hold Time START and Repeat START Condition	t_{HD_STA}			0.6			µs
SCL Pulse-Width Low	t_{LOW}			1.3			µs
SCL Pulse-Width High	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition	t_{SU_STA}			0.6			µs
Data Hold Time	t_{HD_DAT}			0		900	ns
Data Setup Time	t_{SU_DAT}			100			ns
Setup Time for STOP Condition	t_{SU_STO}			0.6			µs
Pulse Width of Suppressed Spike	t_{SP}					50	ns
Bus Capacitance	C_B					400	pF
SDA and SCL Receiving Rise Time	t_R			20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F			20 + 0.1C_B		300	ns

Electrical Characteristics (continued)

(V_{DD} = 1.8V, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Transmitting Fall Time	t_{TF}		20 + 0.1C_B		300	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated bench or proprietary automated test equipment (ATE) characterization.

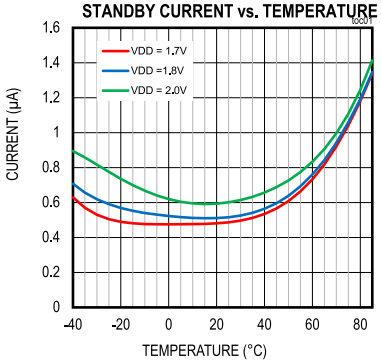
Note 2: a) CVT/PDB = V_{DD} and EXT_CVT_EN = 0 or EXT_CVT_EN = 1 and CVT/PDB = V_{DD} or EXT_CVT_EN = 1 and CVT/PDB = GND
b) CVT/PDB = GND and EXT_CVT_EN = 0

Note 3: Guaranteed by design and characterization. Not tested in production.

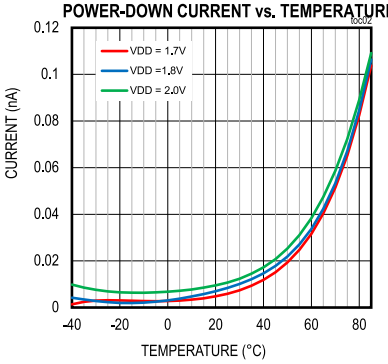
Typical Operating Characteristics

(V_{DD} = +1.8V, T_A = 25°C, unless otherwise noted.)

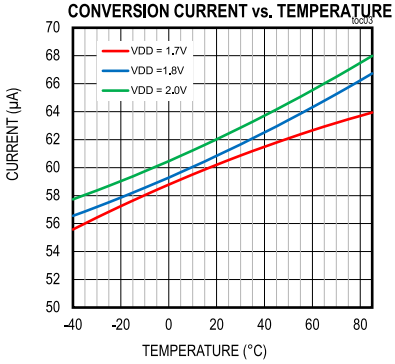
STANDBY CURRENT vs. TEMPERATURE



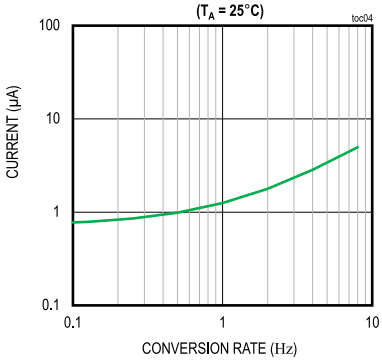
POWER-DOWN CURRENT vs. TEMPERATURE



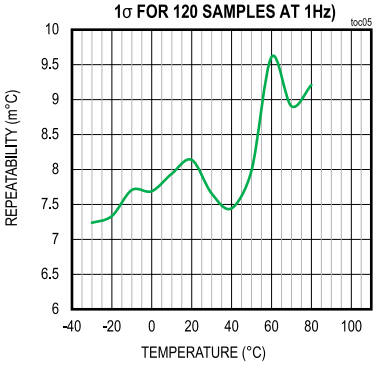
CONVERSION CURRENT vs. TEMPERATURE



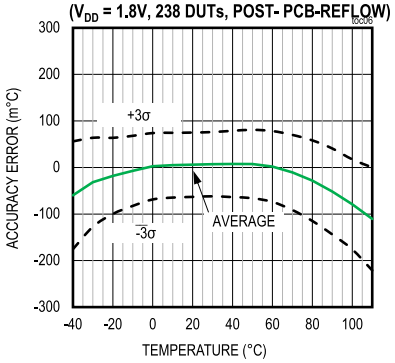
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (T_A = 25°C)



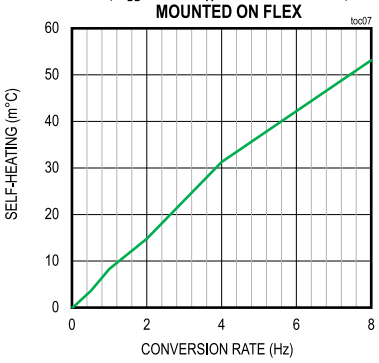
SAMPLE-TO-SAMPLE REPEATABILITY (V_{DD} = 1.8V, 32 DUTs, 1σ FOR 120 SAMPLES AT 1Hz)



ACCURACY ERROR vs. TEMPERATURE (V_{DD} = 1.8V, 238 DUTs, POST- PCB-REFLOW)

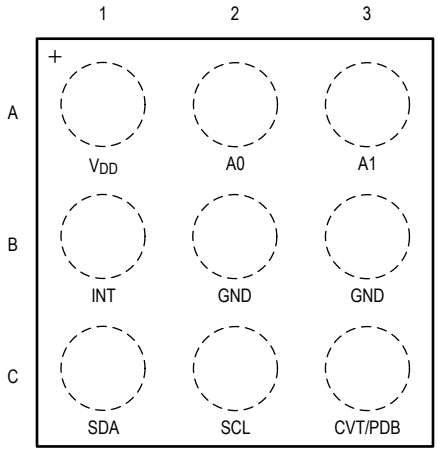


SELF-HEATING vs. CONVERSION RATE (V_{DD} = 1.8V, T_A = 25°C, STILL AIR) MOUNTED ON FLEX



Pin Configuration

MAX30210



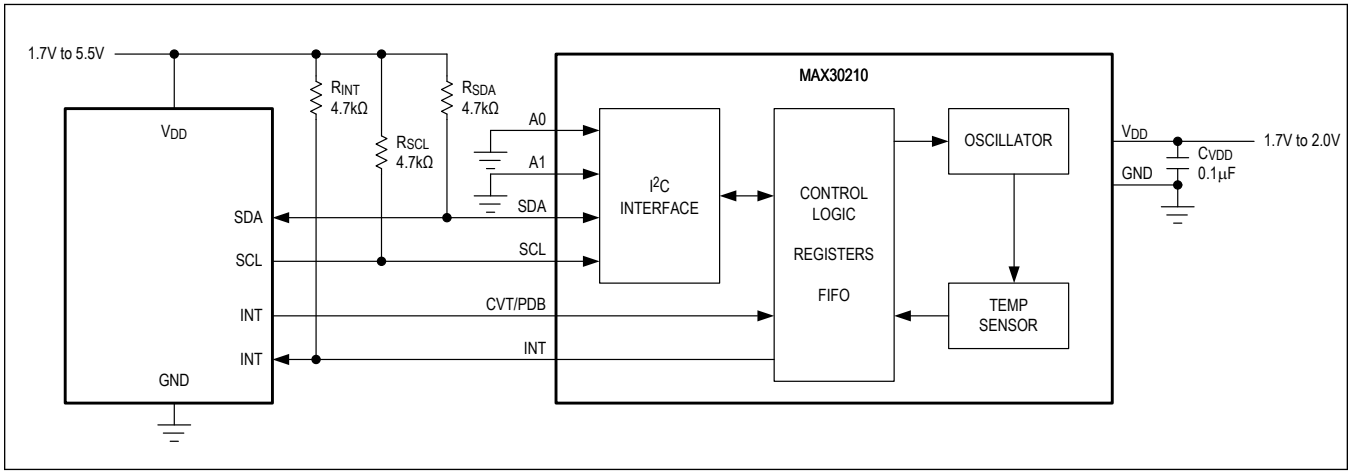
TOP VIEW (BUMPS FACING DOWN)
WLP 0.968mm x 0.968mm x 0.5mm, 0.3mm PITCH

Pin Description

PIN	NAME	FUNCTION
A1	V_{DD}	+1.7V to +2.0V Power Supply. Bypass to GND with a 0.1µF capacitor as close to the bump as possible.
A2	A0	Address select pin A0. Connect to GND, V_{DD}, SDA, or SCL.
A3	A1	Address select pin A1. Connect to GND, V_{DD}, SDA, or SCL.
B1	INT	Interrupt/Alert Output Pin.
B2, B3	GND	Ground Reference.
C1	SDA	I2C Data Input and Output.
C2	SCL	I2C Clock.
C3	CVT/PDB	Convert Input Pin/Power-Down Pin.

Functional Diagrams

Diagram 1



Detailed Description

The MAX30210 temperature sensor measures temperature with ±0.1°C accuracy over a +20°C to +50°C temperature range and ±0.15°C accuracy over a -20°C to +85°C temperature range. The device communicates over a standard I2C interface with serial data (SDA) and serial clock (SCL) lines to read the FIFO, which contains up to 64, 2-byte temperature readings from a 16-bit ADC measurement. The device operates properly over a -40°C to +85°C temperature range without any damage. There are multiple ways to take a temperature measurement including single-shot mode, autonomous conversion mode, and using an external trigger through the CVT/PDB pin. In the autonomous conversion mode, the MAX30210 performs temperature conversions based on a programmable rate and stores the temperature result into the FIFO at the end of every active conversion. Once the data fills up the FIFO, the memory-mapped register contains a FIFO full alarm to be able to save all the data collected. The memory-mapped registers contain programmable high-alarm and low-alarm trigger registers as well. The Alarm High, Alarm Low, and Setup registers are volatile, and do not retain data when the device is powered down. The MAX30210 has four additional pins where three are of fixed function and the fourth is a shared functional pin. Two of the pins (A0, A1) are dedicated for the I2C target address which can be tied to V_{DD}, SCL, SDA, and GND and provide up to 16 different I2C target address options. The final two pins are for interrupt (INT) and convert/power-down (CVT/PDB). The interrupt (INT) pin wakes up the microcontroller unit (MCU) during a qualified event and the convert/power-down (CVT/PDB) pin allows for either an external source to toggle the pin to start a conversion or power-down the part.

Measuring Temperature

The device powers up in a low-power standby state. There are three different ways to initiate a temperature measurement:

- Controller writes a '1' to CONVERT_T[0](0x2A) register.
- Falling/Rising edge trigger on CVT/PDB pin input (EXT_CVT_EN[7](0x12) = 1).
- Turn on autonomous conversion mode after setting up the registers.

In any of these methods, sampling should not exceed 20Hz to limit possible self-heating. Following the conversion, which takes 8ms (typ), the resulting temperature data is stored in the FIFO and the device returns to the standby state. CONVERT_T automatically clears to ‘0’ after the measurement is taken.

The output temperature data is calibrated in degrees Celsius. The temperature data is stored as a left-justified, 16-bit sign-extended two’s complement number in the FIFO Data register (see Table 1). The data is two’s complement where the most significant bit (MSB) determines the sign of the temperature with an MSB of 1 indicating a negative temperature and an MSB of 0 indicating a positive temperature.

To calculate the temperature from the measurement result, convert the two’s complement value to the decimal value and use the following equation.

T = Decimal Value × 0.005

For example, if the result is 0x1CE8, convert to decimal to get 7400, then T = 7400 × 0.005 or 37°C. Table 1 gives examples of digital output data and the corresponding temperature reading.

Table 1. FIFO Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hexadecimal)	DIGITAL OUTPUT (Decimal)
+70	0011 0110 1011 0000	36B0	14000
+50	0010 0111 0001 0000	2710	10000
+41	0010 0000 0000 1000	2008	8200
+37	0001 1100 1110 1000	1CE8	7400
+35.8	0001 1011 1111 1000	1BF8	7160
+25	0001 0011 1000 1000	1388	5000
+15	0000 1011 1011 1000	0BB8	3000

Table 1. FIFO Data Format (continued)

+0.04	0000 0000 0000 1000	0008	8
+0.02	0000 0000 0000 0100	0004	4
+0.01	0000 0000 0000 0010	0002	2
+0.005	0000 0000 0000 0001	0001	1
0	0000 0000 0000 0000	0000	0
-0.005	1111 1111 1111 1111	FFFF	-1
-1	1111 1111 0011 1000	FF38	-200
-10	1111 1000 0011 0000	F830	-2000
-40	1110 0000 1100 0000	E0C0	-8000

External Convert Pin/Power-Down Input

The MAX30210 features a pin that is used for both an external conversion input (CVT) and powering down (PDB) the part to reduce current in between temperature conversions. The CVT input offers the ability to trigger a conversion by either a rising or falling edge. There are more details of the timing in the *Start-Up Timing* section in Figure 9 and Figure 10. To enable the CVT feature, set EXT_CVT_EN[7](0x12) = 1 and set the EXT_CVT_ICFG[6](0x12) bit to set the input active edge. The settings for both the CVT and the PDB features are listed in Table 2. Note, when PDB is brought high from Power Down to Power Up, all register contents restore to the power on reset values.

Table 2. CVT/PDB Pin Function

EXT_CVT_EN	EXT_CVT_ICFG	CVT/PDB	FUNCTION
0	X	GND	Power Down
0	X	V_{DD}	Power Up
1	0	Pulse	Power Up, CVT On, Falling Edge Conversion
1	1	Pulse	Power Up, CVT On, Rising Edge Conversion

Autonomous Conversion Mode

When the AUTO[1](0x2A) is set to 1, the MAX30210 operates in autonomous conversion mode. The MAX30210 continuously performs temperature conversions in this mode based on the TEMP_PERIOD[3:0](0x29) settings and the resulting temperature measurement data is stored in the FIFO at the end of every active conversion. Every conversion cycle consists of an active conversion followed by a standby period. The device typically consumes 61µA during active conversion and 750nA in standby mode. Table 3 shares the corresponding bit settings and the sample rate.

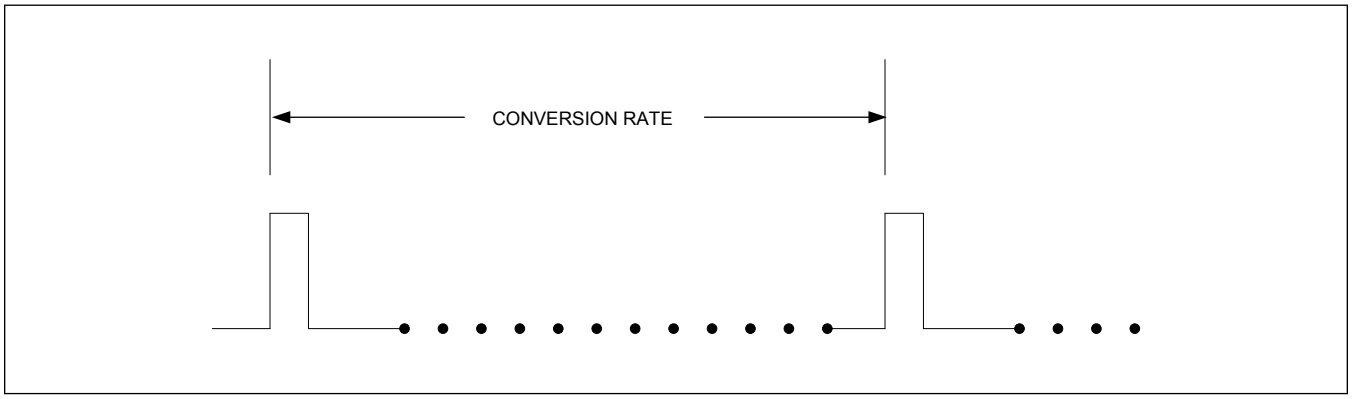


Figure 1. Conversion Sample Period

Table 3. Temperature Sample Rate

TEMP_PERIOD	SAMPLE RATE (Hz)	SAMPLE PERIOD (sec)
0x0	0.015625	64
0x1	0.03125	32
0x2	0.0625	16
0x3	0.125	8
0x4	0.25	4
0x5	0.5	2
0x6	1	1
0x7	2	0.5
0x8	4	0.25
0x9 to 0xF	8	0.125

MCU Interrupt Modes

High/Low Alarm

After the device performs a temperature conversion, the temperature value is compared with the user-defined two's complement alarm trigger values stored in the 2-byte ALARM_HI[15:0](0x22, 0x23) and 2-byte ALARM_LO[15:0](0x24,0x25) registers (see Figure 2). The default value for ALARM_HI is 0x7FFF (+163.835°C) and the default value for ALARM_LO is 0x8000 (-163.840°C). The MSB indicates if the value is positive or negative; for positive numbers the MSB is 0 and for negative numbers the MSB is 1. If the measured temperature is lower than ALARM_LO or higher than ALARM_HI, an alarm condition exists and corresponding status bit, TEMP_LO[3](0x00) or TEMP_HI[2](0x00) is set in the Status register. When the alarm condition is detected and the corresponding interrupt enable bit, TEMP_LO_EN[3](0x02) or TEMP_HI_EN[2](0x02) is set in the Interrupt Enable register and a hardware interrupt asserts on the INT pin, then the status bits, the alarm flag, and the hardware interrupt stay asserted until the Status register is read using the serial interface. The alarm flag only clears when STATUS is read. If the alarm flag is set and the next result does not trip the flag, then the flag remains set.

If the alarm settings change while the device is under an alarm condition, the alarm status must be cleared and another temperature conversion executed to update the alarm condition.

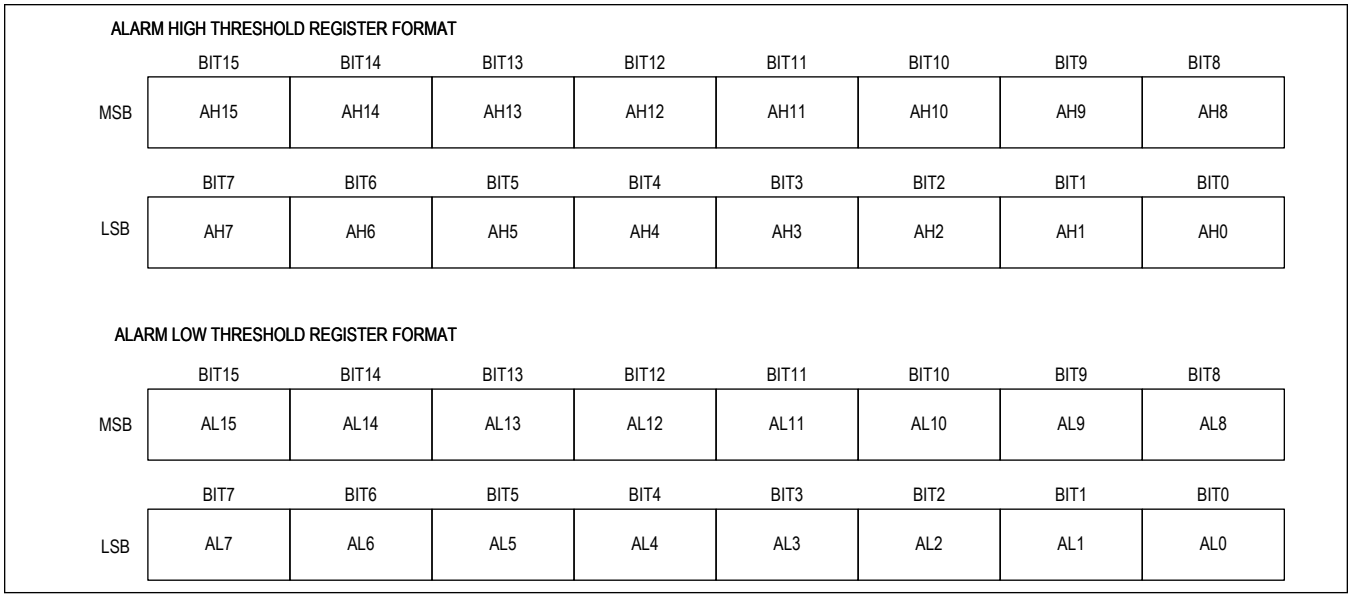


Figure 2. High/Low Alarm Threshold Register Format

Interrupt Mode

When the alert mode bit is set to 0 and autonomous conversion mode is enabled, the MAX30210 is set for interrupt mode alerts. In this mode, the MAX30210 sends an interrupt to the MCU when the temperature passes either the high temperature threshold or the low temperature threshold value. The alerts are cleared once the I2C read occurs. Figure 3 shows how the mode works.

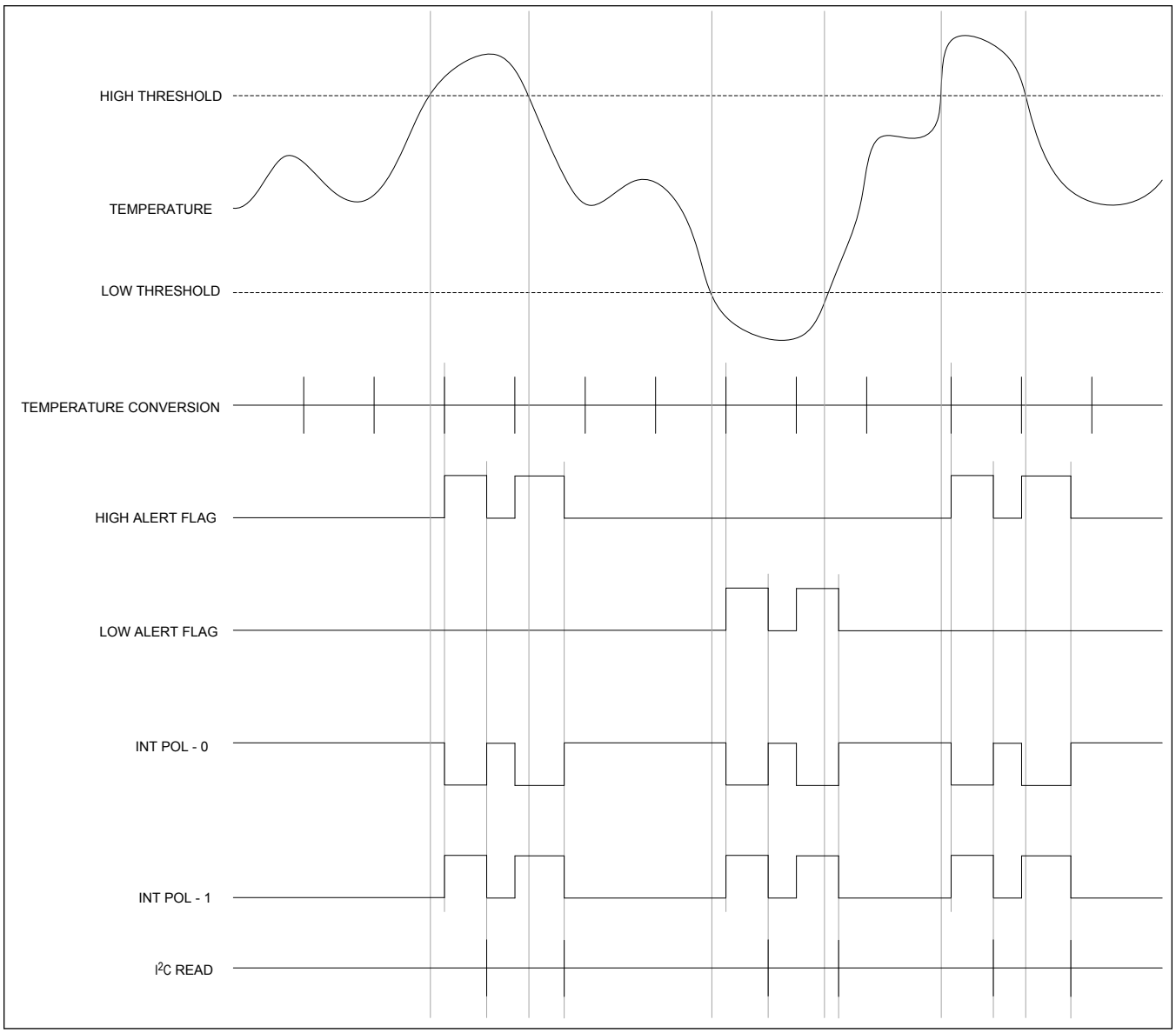


Figure 3. Interrupt Mode Timing Diagram

Comparator Mode

When the alert mode bit is set to 1 and autonomous conversion mode is enabled, the MAX30210 is set for comparator mode alerts. In this mode, the MAX30210 sends an interrupt to the MCU when the temperature is measured higher than the high temperature threshold. Both the high alert register and the interrupt pin stay asserted until the temperature falls below the set low temperature threshold value. The low alert flag is disabled and always read 0 in this mode. No alerts are cleared once the I2C read occurs. Figure 4 shows how the mode works.

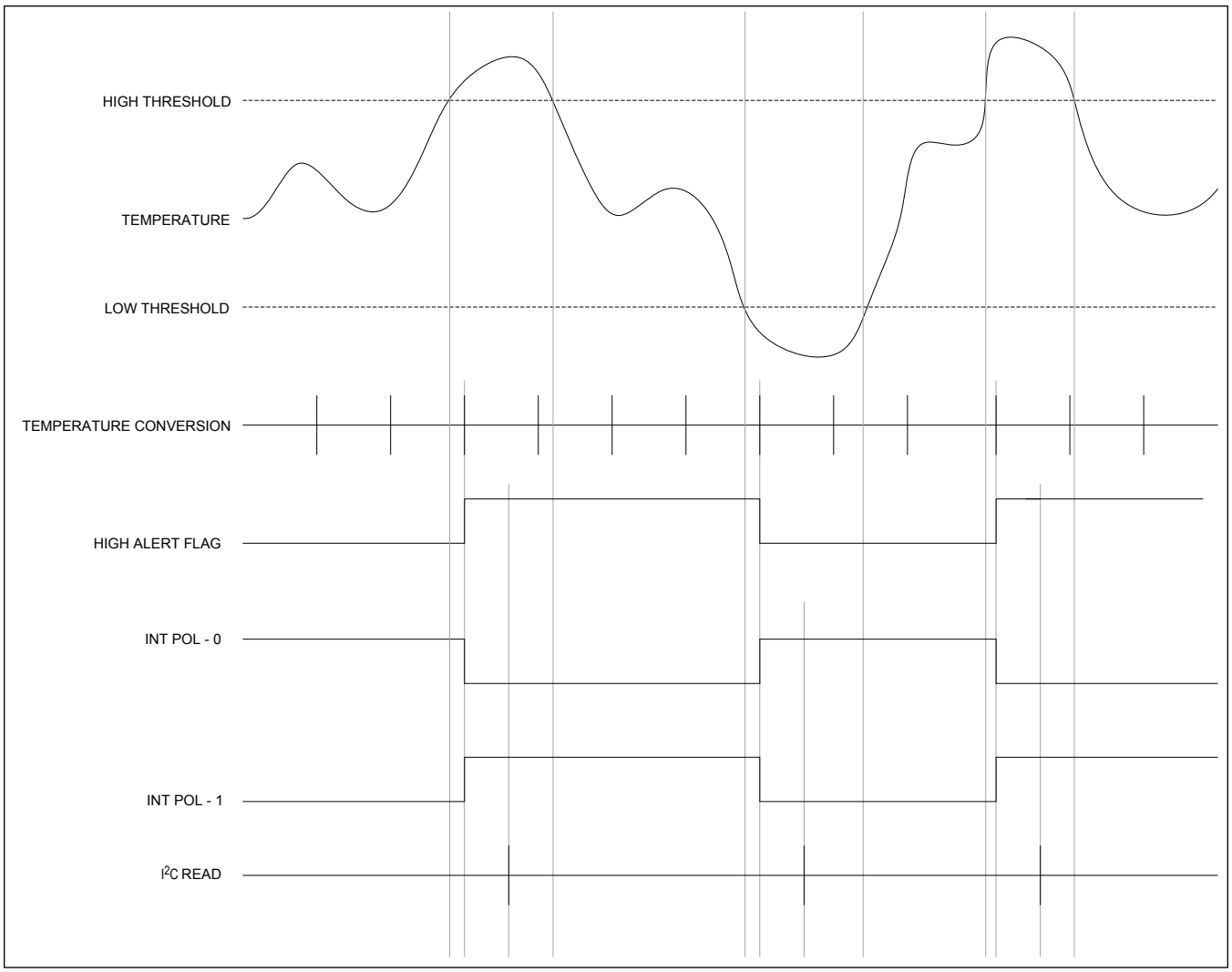


Figure 4. Comparator Mode Timing Diagram

Rate-of-Change Alarm

An on-chip filter, when enabled, measures the slope of the previous N samples, is available after N samples have been collected and then updated for each additional sample. In the following example, N is set to 5. If the slope exceeds the setting in TEMP_INC_THRESH[7:0](0x26), an interrupt is asserted. Likewise, if the slope is less than the setting in TEMP_DEC_THRESH[7:0](0x27), an interrupt is set. Figure 5 shows measured data with eight sequential slope measurements.

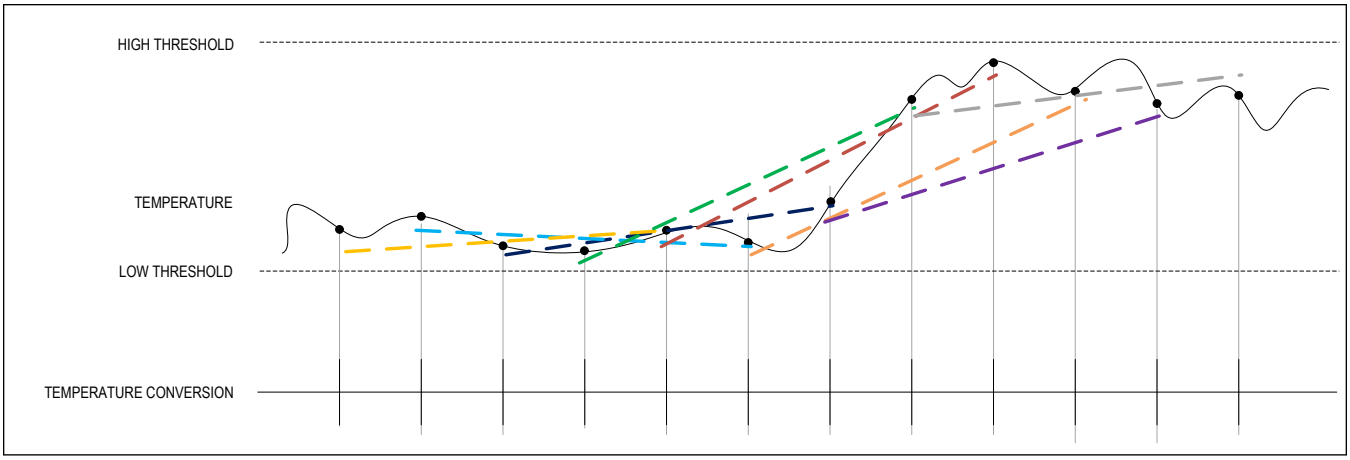


Figure 5. Rate-of-Change Filter Applied to Temperature Measurements

When autonomous mode is enabled (AUTO[1](0x2A) = 1) and CHG_DET_EN[3](0x28) is set to 1, the MAX30210 enables a rate-of-change mode. The mode is also enabled when CHG_DET_EN is set to 1 and EXT_CVT_EN[7](0x12) is set to 1. Table 4 summarizes how the mode is set.

Table 4. Rate-of-Change Alarm Mode

AUTO	EXT_CVT_EN	CHG_DET_EN	RATE OF CHANGE MODE
0	0	X	Disabled
X	1	0	Disabled
1	0	0	Disabled
X	1	1	Enabled
1	0	1	Enabled

When the rate-of-change mode is enabled, the MAX30210 provides a slope value based on a set number of temperature measurement samples (m°C/Sample) and stores the 2's compliment value in the TEMP_SLOPE[8:0](0x2D, 0x2E) registers. This value is compared to a user settable slope increase threshold TEMP_INC_THRESH[7:0](0x26) and the slope decrease threshold TEMP_DEC_THRESH[7:0](0x27). If the slope value is higher than the value in the TEMP_INC_THRESH, the TEMP_INC_FAST[4](0x00) bit is asserted. Likewise, if the slope value is lower than the value in the TEMP_DEC_THRESH, the TEMP_DEC_FAST[5](0x00) bit is asserted in the status register. There are interrupt options to send an interrupt to the INT pin if either the TEMP_DEC_FAST or the TEMP_INC_FAST bit is asserted by setting 1 to the TEMP_DEC_FAST_EN[5](0x02) or TEMP_INC_FAST_EN[4](0x02) bit, independently. One could choose to interrupt only on an increase slope threshold, a decrease slope threshold or choose to be interrupted by both. All interrupts and status bits are cleared upon I2C read.

These settings are dependent on the filter set in the RATE_CHG_FILTER[2:0](0x28) register. This register sets the length of the change in temperature FIR filter. The slope value is calculated based on the number of samples selected in this register and is stored in the TEMP_SLOPE registers as described above. No slope value is stored until the number of samples in the RATE_CHG_FILTER register has been taken. The user needs to set the appropriate number of samples to fit the application needs.

Table 5. Rate-of-Change Filter Settings

RATE_CHG_FILTER	TEMPERATURE SAMPLES
0x0	2
0x1	3
0x2	5
0x3	9

Table 5. Rate-of-Change Filter Settings (continued)

RATE_CHG_FILTER	TEMPERATURE SAMPLES
0x4	17
0x5	33
0x6	65
0x7	65

The TEMP_INC_THRESH setting is based on a positive slope in units of 5m°C*N/SAMPLE(S) where N = (0 to 255). Likewise, the TEMP_DEC_FAST_THRESH setting is based on a negative slope in units of 5m°C*N/SAMPLE(S) where N = (0 to 255).

Table 6. Change in Temperature Threshold Settings

VALUE	CHANGE IN TEMPERATURE/SAMPLE (m°C/SAMPLE)
0x0	0
0x1	5
0x2	10
0x3	15
0x4	20
---	---
0xFF	N*5 where N={0 to 255}

To set the expected threshold, the slope needs to be set based on the configured sample rate. Here are some examples sharing how the calculation is completed.

Table 7. Rate of Change Alarm Examples

SAMPLE RATE (SPS)	TEMPERATURE SAMPLES	CHANGE IN TEMPERATURE/ SAMPLE (m°C/sample)	CHANGE IN TEMPERATURE (m°C)	TIME PERIOD (SEC)	DESCRIPTION
8	9 [0x3]	5	5*(9-1) = 40	(9-1)/8 = 1	40m°C slope increase threshold over a 1-second time period.
8	65 [0x6, 0x7]	5	5*(65-1) = 320	(65-1)/8 = 8	320m°C increase over an 8-second time period
1	5 [0x2]	50	50*(5-1) = 200	(5-1)/1 = 4	200m°C slope increase threshold over a 4-second time period
1	17 [0x4]	50	50*(17-1) = 800	(17-1)/1 = 16	800m°C increase over a 16-second time period
0.0625	3 [0x1]	200	200*(3-1) = 400	(3-1)/0.0625 = 32	400m°C slope increase threshold over a 48-second time period
0.0625	9[0x3]	200	200*(9-1) = 1600	(9-1)/0.0625 = 128	1600m°C slope increase threshold over a 128-second time period

Start-Up Timing

The start-up timing and delays for the MAX30210 are shown in the waveform below. Figure 6 shows the typical time taken for the MAX30210 to wake up and be ready for I2C communication.

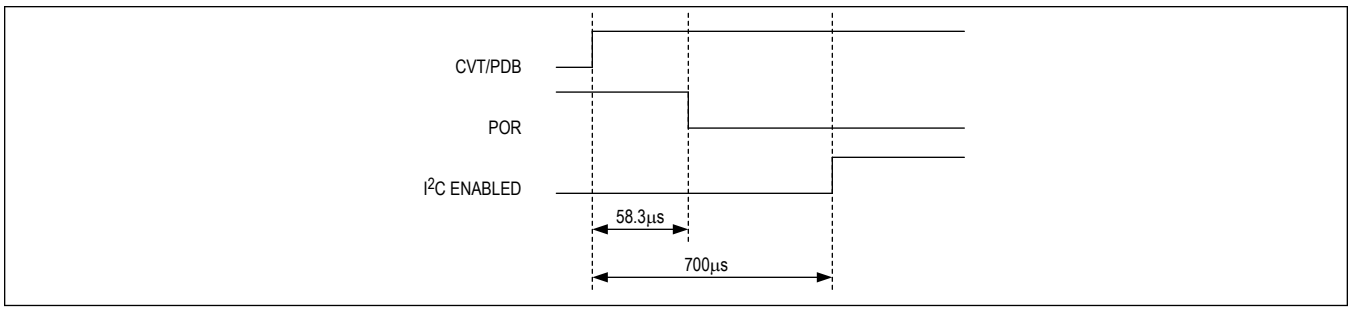


Figure 6. Power-Up Timing

Figure 7 shows the typical start-up delay when the MAX30210 is used in autonomous mode.

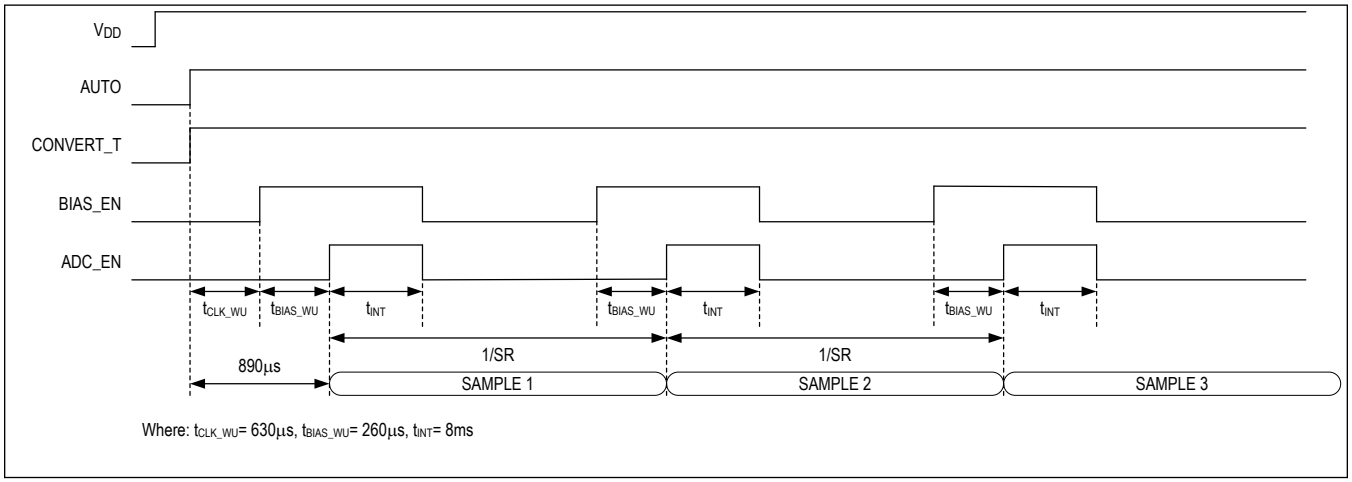


Figure 7. Autonomous Conversion Mode

Figure 8 shows the typical start-up delay when the MAX30210 is used in single-shot mode initiated through I2C.

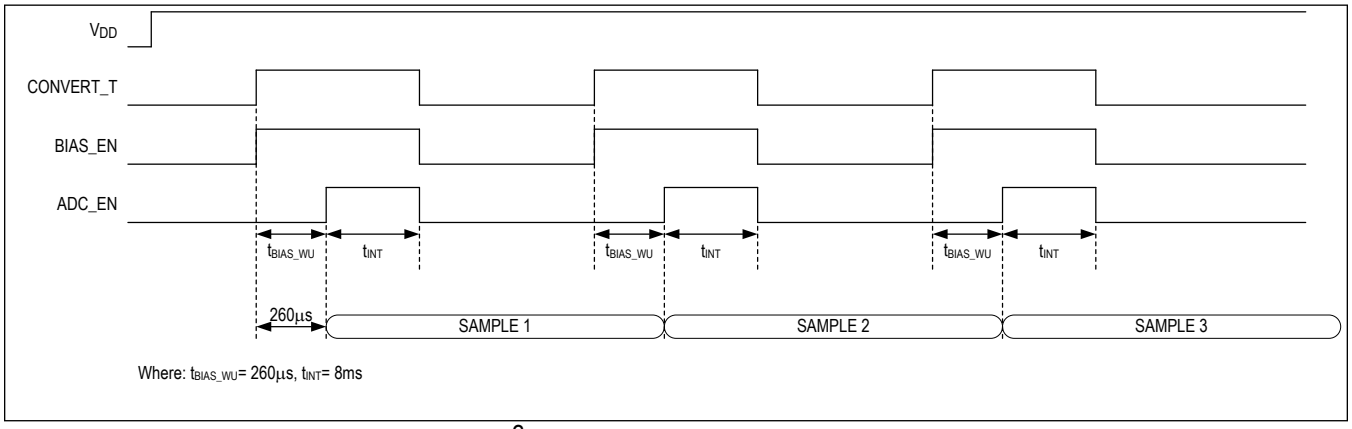


Figure 8. Single-Shot Conversion Mode - through I2C

Figure 9 shows the typical start-up delay when the MAX30210 is used in single-shot mode initiated through the CVT pin.

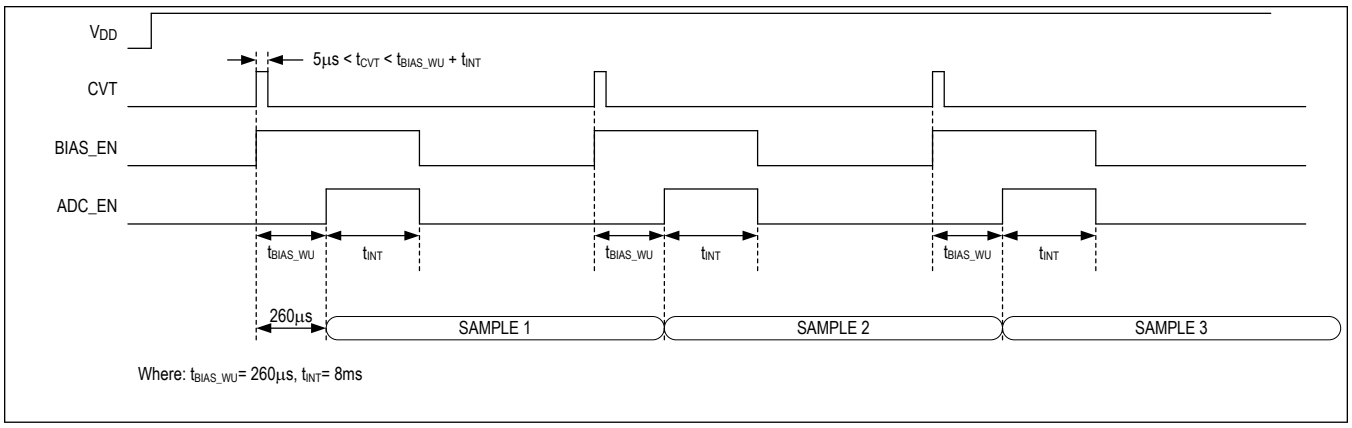


Figure 9. Single-Shot Conversion Mode - through CVT

When using the CVT pin to initiate a conversion the pulse width of the CVT pin must meet the minimum requirements shown in Figure 10.

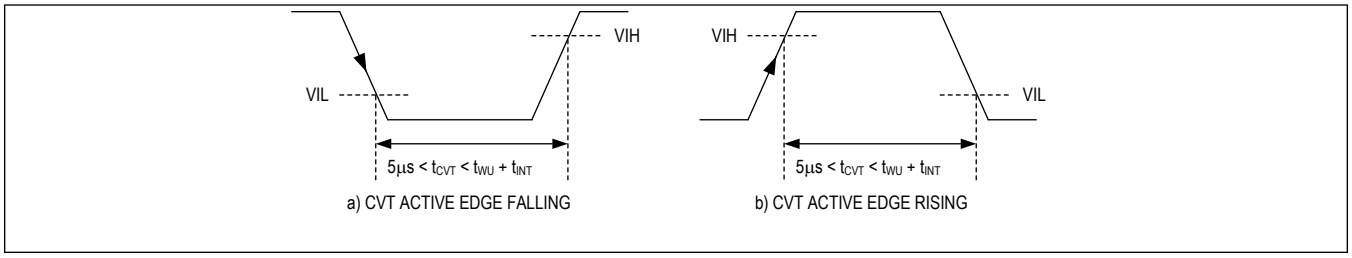


Figure 10. CVT Pulse Width Timing

FIFO Description

FIFO Data Format

The FIFO is 64 samples deep and is designed for 16-bit temperature data. The controller does a burst read of three bytes starting at register 0x08 to read one 16-bit temperature sample, referred to as a word, from the FIFO. The data read from the FIFO has an 8-bit tag and a 16-bit temperature data as shown in Table 8. The controller reads 3N bytes from the FIFO to get N samples.

When the rate change is too fast, a 9-bit temperature slope is saved in the FIFO along with the R[1:0] bits which indicate if the temperature rise or fall is too fast.

Table 8. FIFO Data and Tags

	TAG[23:16]								DATA[15:0]															
Data Type	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	0	0	0	0	0	0	0	0	RESERVED															
Temperature	0	C[1:0]		R[1:0]		T[1:0]		1	TEMP_DATA[15:0]															
Marker	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Invalid data	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

C[1:0]	Conversion Type
00	Internal Manual
01	Internal Auto

1x	External

R[1:0]	Rate of Change of Temperature
0x	Temperature change is normal
10	Temperature increase is too fast
11	Temperature decrease is too fast

T[1:0]	Temperature Data
0x	Temperature is normal
10	Temperature below low threshold
11	Temperature above high threshold

FIFO Configuration Registers

There are seven registers (address 0x04 to 0x0A) that control how the FIFO is configured and read out. Details of these registers are given as follows:

FIFO_WR_PTR (address 0x04), Write Pointer

FIFO_WR_PTR[5:0] points to the FIFO location where the next word is written. This pointer advances for each word pushed on to the FIFO by the internal conversion process. The write pointer is updated from a 6-bit counter and wraps around to count 0x00 from count 0x3F.

FIFO_RD_PTR (address 0x05), Read Pointer

FIFO_RD_PTR[5:0] points to the location where the next word of the FIFO is read using the I2C interface. This advances each time a word is read from the FIFO. The read pointer is updated from a 6-bit counter and wraps around to count 0x00 from count 0x3F.

OVF_COUNTER (address 0x06), Overflow Counter

OVF_COUNTER[5:0] logs the number of words lost if new words are written after the FIFO is full. This counter saturates at count value 0x3F. Each time a complete word is popped from the FIFO, the OVF_COUNTER is reset to zero. The counter is useful as a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

FIFO_DATA_COUNT (address 0x07), FIFO Data Counter

FIFO_DATA_COUNT[6:0] is a read-only register, which holds the number of words available in the FIFO for the controller to read. This increments when a new word is pushed to the FIFO, and decrements when the controller reads a word from the FIFO.

FIFO_DATA (address 0x08), FIFO Data

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the word from the FIFO. Each word is three bytes. Burst reading three bytes from the FIFO_DATA register advances the FIFO_RD_PTR by one.

FIFO_A_FULL (address 0x09), FIFO Almost Full

The FIFO_A_FULL[5:0] register sets the watermark for the FIFO and determines when the A_FULL[7](0x00) bit in the Status register is asserted. The A_FULL bit is set when the FIFO contains 64 minus FIFO_A_FULL[5:0] words. For example, when FIFO_A_FULL is set to 2, the flag is set when the 62nd word is written to the FIFO. When the FIFO almost full condition is met, the A_FULL bit is asserted in the Status register. If the A_FULL_EN[7](0x02) bit in the Interrupt Enable register is set and INT_OCFG[1:0](0x12) and INT_FCFG[3:2](0x12) are set in the Pin Configuration register, then the interrupt is asserted on the INT pin. This condition should prompt the applications processor to read samples from the FIFO before it fills.

The application processor reads the OVF_COUNTER[5:0](0x06) and FIFO_DATA_COUNT[6:0](0x07) registers, to

determine how many data items are in the FIFO.

Alternatively, if the application always responds much faster than the selected sample rate, it could read 64 minus FIFO_A_FULL[5:0] number of data items every time it gets an A_FULL interrupt and be assured that all data from the FIFO are read. This is the preferred way to minimize the traffic on the serial interface. FIFO_WR_PTR, FIFO_RD_PTR, FIFO_DATA_COUNT and OVF_COUNTER registers are available for debug purposes, if needed.

FIFO_RO (address 0x0A), FIFO Rollover

The FIFO_RO[1] bit in the FIFO Configuration 2 register determines whether a sample is pushed onto the FIFO or discarded when it is full. If FIFO_RO is enabled when FIFO is full, old samples are overwritten. If FIFO_RO is not set, the new sample is discarded and the FIFO is not updated.

A_FULL_TYPE (address 0x0A),Almost Full Type

The A_FULL_TYPE[2] bit defines the behavior of the A_FULL status bit. If the A_FULL_TYPE bit is set low, the A_FULL[7](0x00) status bit is asserted when the A_FULL condition is detected and cleared by a STATUS register read, then reasserts for every sample if the A_FULL condition persists. If the A_FULL_TYPE bit is set high, the A_FULL status bit is asserted only when a new A_FULL condition is detected. The status bit is cleared by a STATUS register read and does not reassert for every sample until a new A_FULL condition is detected.

FIFO_STAT_CLR (address 0x0A), FIFO Status Clear

The FIFO_STAT_CLR[3] bit defines whether the A_FULL[7](0x00) and TEMP_RDY[6](0x00) status bits should clear by a FIFO_DATA[7:0](0x08) register read. If FIFO_STAT_CLR is set low, A_FULL and TEMP_RDY status bits are not cleared by a FIFO_DATA register read but are cleared by Status register read. If FIFO_STAT_CLR is set high, A_FULL and TEMP_RDY status bits are cleared by a FIFO_DATA register read or a STATUS register read.

FLUSH_FIFO (address 0x0A)

The FLUSH_FIFO[4] bit is used for flushing the FIFO. The FIFO becomes empty and the FIFO_WR_PTR[5:0](0x04), FIFO_RD_PTR[5:0](0x05), FIFO_DATA_COUNT[6:0](0x07) and OVF_COUNTER[5:0](0x06) are reset to zero. FLUSH_FIFO is a self-clearing bit.

Serial Interface

I2C Target Address

The device responds to its own I2C target address, which is selected using the A0 and A1 pins for the MAX30210. A0 and A1 can be connected to the supply voltage, ground, SDA, or SCL. This provides up to 16 unique addresses for the MAX30210 as shown in Table 9.

Table 9. I2C Target Address

A1	A0	ADDR
GND	GND	0x80
GND	V_{DD}	0x82
GND	SCL	0x84
GND	SDA	0x86
V_{DD}	GND	0x88
V_{DD}	V_{DD}	0x8A
V_{DD}	SCL	0x8C
V_{DD}	SDA	0x8E
SCL	GND	0x90
SCL	V_{DD}	0x92
SCL	SCL	0x94
SCL	SDA	0x96

Table 9. I2C Target Address (continued)

A1	A0	ADDR
SDA	GND	0x98
SDA	V_{DD}	0x9A
SDA	SCL	0x9C
SDA	SDA	0x9E

I2C/SMBus Compatible Serial Interface

The MAX30210 features an I2C/SMBus-compatible, 2-wire serial interface consisting of an SDA and SCL. The SDA and SCL facilitate communication between the MAX30210 and the controller at clock rates up to 400kHz. Figure 11 shows the 2-wire interface timing diagram. The controller generates SCL and initiates data transfer on the bus. The controller device writes data to the MAX30210 by transmitting the proper target address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX30210 is 8-bit long and is followed by an acknowledge clock pulse. A controller reading data from the MAX30210 transmits the proper target address followed by a series of nine SCL pulses. The MAX30210 transmits data on SDA in sync with the controller-generated SCL pulses. The controller acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. The SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL operates only as an input. A pullup resistor is required on SCL if there are multiple controllers on the bus, or if the single controller has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX30210 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

Detailed I2C Timing Diagram

The detailed timing diagram is shown in Figure 11.

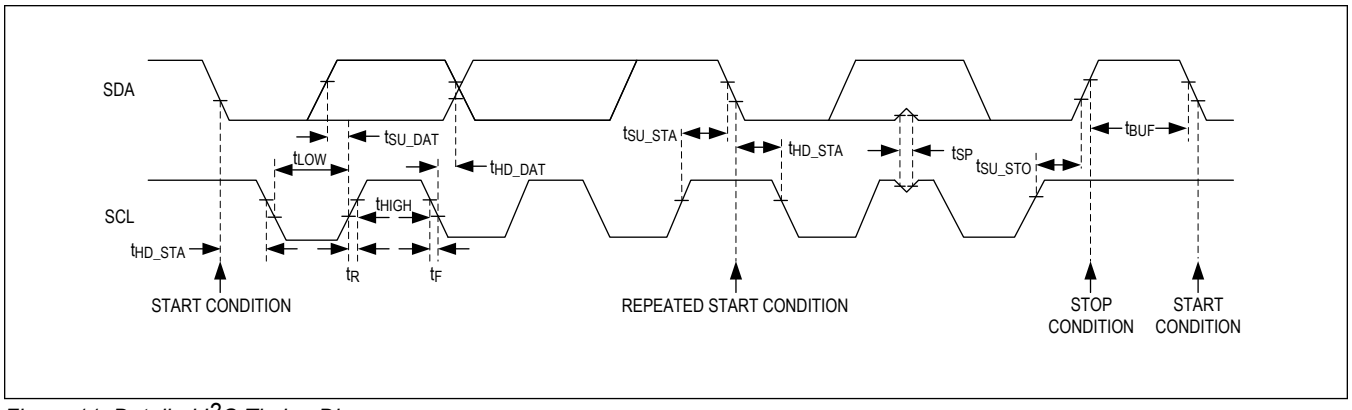


Figure 11. Detailed I2C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

The SDA and SCL idle high when the bus is not in use. A controller initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 12). A START condition from the controller signals the beginning of a transmission to the MAX30210. The controller terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX30210 uses to handshake receipt of each byte of data when in write mode (Figure 13). The MAX30210 pulls down SDA during the entire controller-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller retries communication. The controller pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX30210 is in read mode. An acknowledge is sent by the controller after each read byte to allow data transfer to continue. A not acknowledge is sent when the controller reads the final byte of data from the MAX30210 followed by a STOP condition.

I2C Write Data Format

A write to the MAX30210 includes transmission of a START condition, the target address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 14 illustrates the proper frame format for writing one byte of data to the MAX30210. Figure 15 illustrates the frame format for writing n-bytes of data to the MAX30210.

The controller first sends the target address with the R/$\overline{W}$ bit set to 0. This indicates that the controller intends to write data to the MAX30210. The MAX30210 acknowledges receipt of the address byte during the controller-generated 9th SCL pulse.

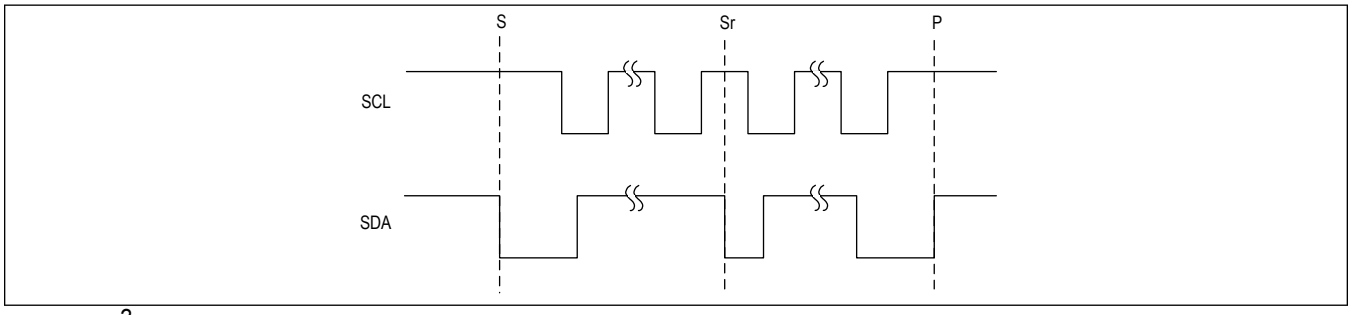


Figure 12. I2C Start (S), Stop (P), and Repeated Start (Sr) Conditions

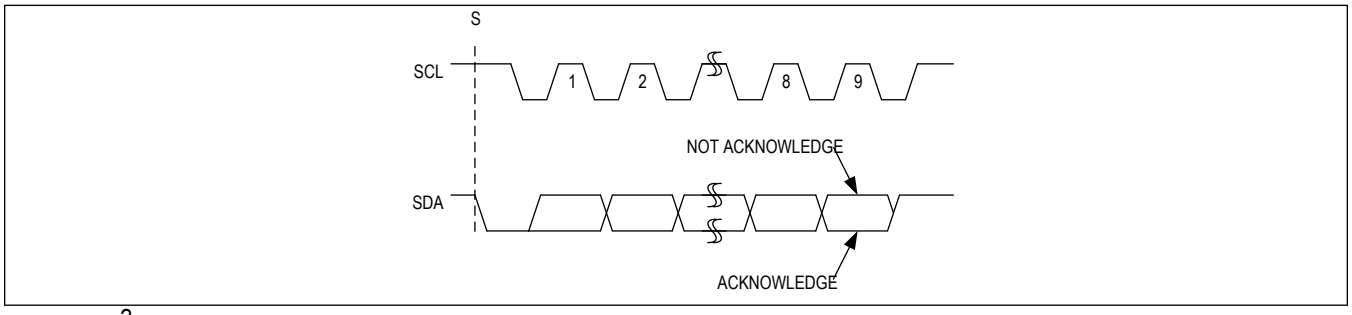


Figure 13. I2C Acknowledge Bit

The second byte transmitted from the controller configures the MAX30210's internal register address pointer. The pointer tells the MAX30210 where to write the next byte of data. An acknowledge pulse is sent by the MAX30210 upon receipt of the address pointer data.

The third byte sent to the MAX30210 contains the data that is written to the chosen register. An acknowledge pulse from the MAX30210 signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a controller to write to sequential registers within one continuous frame. The controller signals the end of transmission by issuing a STOP condition. The auto-increment feature is disabled when there is an attempt to write to the FIFO_DATA[7:0] (0x08) register.

I2C Read Data Format

The controller sends the target address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX30210 acknowledges receipt of its target address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

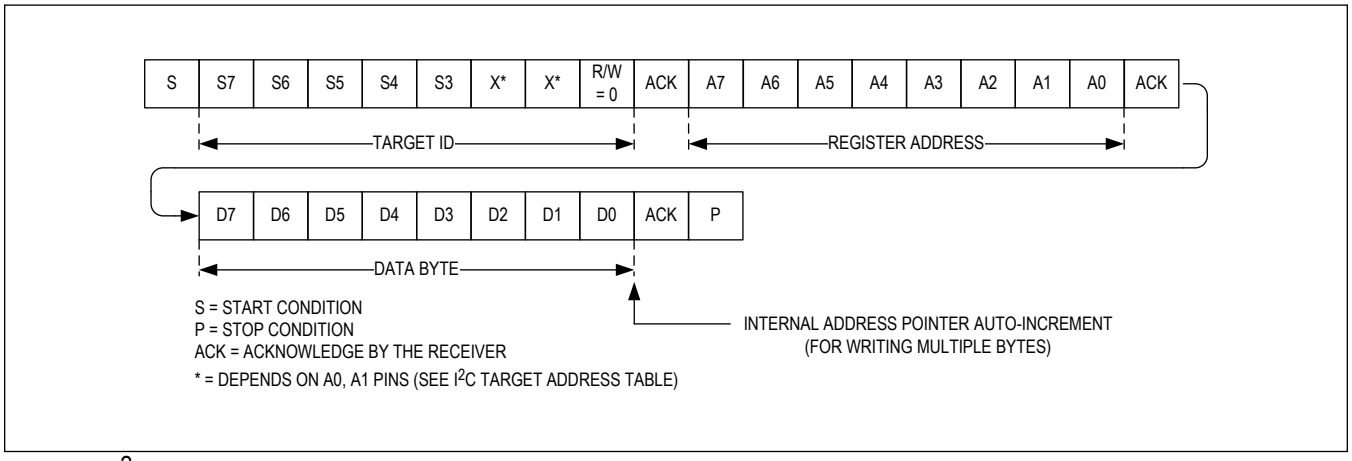


Figure 14. I2C Single Byte Write Transaction

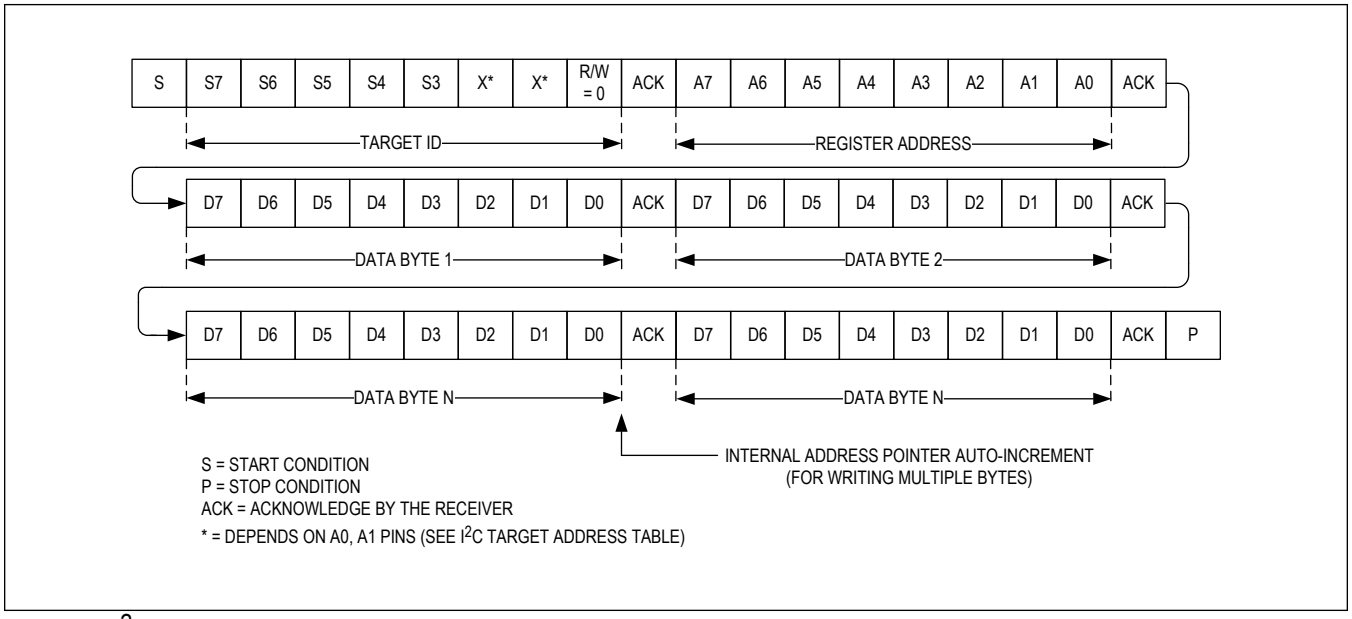


Figure 15. I2C Multi-Byte Write Transaction

The first byte transmitted from the MAX30210 contains the data in register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto-increment feature is disabled when there is an attempt to read from the FIFO_DATA[7:0](0x08) register, and this allows for burst reading of the FIFO_DATA register. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00. The address pointer can be preset to a specific register before a read command is issued. The controller presets the address pointer by first sending the MAX30210 target address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the target address with the R/$\overline{W}$ bit set to 1. The MAX30210 then transmits the contents of the specified

register. The address pointer auto-increments after transmitting the first byte.

The controller acknowledges receipt of each read byte during the acknowledge clock pulse. The controller must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the controller and then a STOP condition. Figure 16 illustrates the frame format for reading one byte from the MAX30210. Figure 17 illustrates the frame format for reading multiple bytes from the MAX30210.

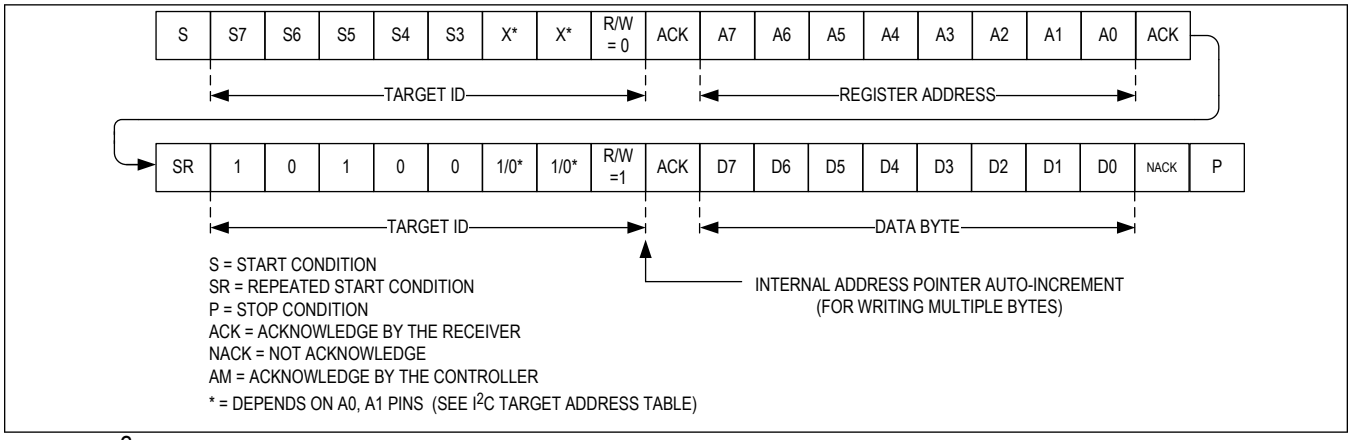


Figure 16. I2C Single Byte Read Transaction

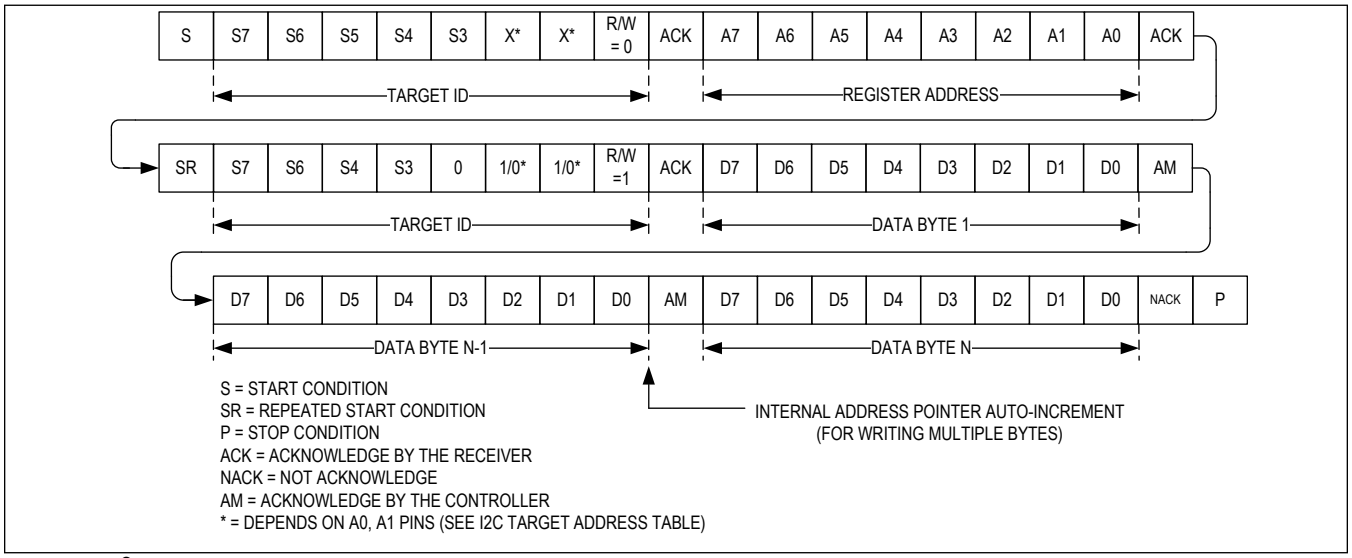


Figure 17. I2C Multi-Byte Read Transaction

Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	Status[7:0]	A_FULL	TEMP_RDY	TEMP_DEC_FAST	TEMP_INC_FAST	TEMP_LO	TEMP_HI	–	PWR_RDY
Interrupt Enables									
0x02	Interrupt Enable[7:0]	A_FULL_EN	TEMP_RDY_EN	TEMP_DEC_FAST_EN	TEMP_INC_FAST_EN	TEMP_LO_EN	TEMP_HI_EN	–	–
FIFO									
0x04	FIFO Write Pointer[7:0]	–	–	FIFO_WR_PTR[5:0]					
0x05	FIFO Read Pointer[7:0]	–	–	FIFO_RD_PTR[5:0]					
0x06	FIFO Counter 1[7:0]	–	–	OVF_COUNTER[5:0]					
0x07	FIFO Counter 2[7:0]	–	FIFO_DATA_COUNT[6:0]						
0x08	FIFO Data[7:0]	FIFO_DATA[7:0]							
0x09	FIFO Configuration 1[7:0]	–	–	FIFO_A_FULL[5:0]					
0x0A	FIFO Configuration 2[7:0]	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
SYSTEM CONTROL									
0x11	SYSTEM CONFIGURATION[7:0]	–	–	–	–	–	–	–	RESET
0x12	PIN CONFIGURATION[7:0]	EXT_CVT_EN	EXT_CVT_ICFG	–	–	INT_FCFG[1:0]		INT_OCFG[1:0]	
TEMPERATURE									
0x20	TEMP ALARM HIGH SETUP[7:0]	TEMP_HI_DET_CNTR[2:0]			–	TEMP_HI_TRIP	TEMP_HI_TRIP_CNT[1:0]		TEMP_RST_HI_CNTR
0x21	TEMP ALARM LOW SETUP[7:0]	TEMP_LO_DET_CNTR[2:0]			–	TEMP_LO_TRIP	TEMP_LO_TRIP_CNT[1:0]		TEMP_RST_LO_CNTR
0x22	TEMP ALARM HIGH MSB[7:0]	ALARM_HI[15:8]							
0x23	TEMP ALARM HIGH LSB[7:0]	ALARM_HI[7:0]							
0x24	TEMP ALARM LOW MSB[7:0]	ALARM_LO[15:8]							
0x25	TEMP ALARM LOW LSB[7:0]	ALARM_LO[7:0]							
0x26	TEMP_INC_FAST_THRESH[7:0]	TEMP_INC_THRESH[7:0]							
0x27	TEMP_DEC_FAST_THRESH[7:0]	TEMP_DEC_THRESH[7:0]							

ADDRESS	NAME	MSB							LSB
0x28	TEMP CONFIGURATION 1[7:0]	–	–	–	–	CHG_DET_EN	RATE_CHG_FILTER[2:0]		
0x29	TEMP CONFIGURATION 2[7:0]	ALERT_MODE	–	–	–	TEMP_PERIOD[3:0]			
0x2A	TEMP CONVERT[7:0]	–	–	–	–	–	–	AUTO	CONVERT_T
0x2B	TEMP DATA MSB[7:0]	TEMP_DATA[15:8]							
0x2C	TEMP DATA LSB[7:0]	TEMP_DATA[7:0]							
0x2D	TEMP SLOPE MSB[7:0]	–	–	–	–	–	–	–	TEMP_SLOPE[8]
0x2E	TEMP_SLOPE LSB[7:0]	TEMP_SLOPE[7:0]							
UNIQUE ID									
0x30	UNIQUE ID1[7:0]	UNIQUE_ID_1[7:0]							
0x31	UNIQUE ID2[7:0]	UNIQUE_ID_2[7:0]							
0x32	UNIQUE ID3[7:0]	UNIQUE_ID_3[7:0]							
0x33	UNIQUE ID4[7:0]	UNIQUE_ID_4[7:0]							
0x34	UNIQUE ID5[7:0]	UNIQUE_ID_5[7:0]							
0x35	UNIQUE ID6[7:0]	UNIQUE_ID_6[7:0]							
IDENTIFIERS									
0xFF	PART IDENTIFIER[7:0]	PART_ID[7:0]							

Register Details

Status (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	TEMP_RDY	TEMP_DEC_FAST	TEMP_INC_FAST	TEMP_LO	TEMP_HI	–	PWR_RDY
Reset	0	0	0	0	0	0	–	1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION
A_FULL	7	A_FULL is set to 1 when the FIFO has reached the threshold programmed in the FIFO_A_FULL[5:0](0x09). This is a read-only bit. This bit is cleared when the Status Register is read. It is also cleared when FIFO_DATA[7:0](0x08) register is read, if FIFO_STAT_CLR[3](0x0A) = 1.
TEMP_RDY	6	TEMP_RDY is asserted when a temperature sensor measurement has completed and new data is available to be read by the controller. This bit is cleared when the Status Register is read. It is also cleared when FIFO_DATA[7:0](0x08) register is read, if FIFO_STAT_CLR[3](0x0A) = 1.
TEMP_DEC_FAST	5	TEMP_DEC_FAST is asserted when the temperature decreases too fast. This is a read-only bit and it is cleared after the STATUS register is read.

BITFIELD	BITS	DESCRIPTION
TEMP_INC_FAST	4	TEMP_INC_FAST is asserted when the temperature increases too fast. This is a read-only bit and it is cleared after the STATUS register is read.
TEMP_LO	3	TEMP_LO is asserted when the latest temperature sensor measurement is less than what is programmed in the Temperature Sensor Alarm Low (0x24,0x25) register. This is a read-only bit and it is cleared after the STATUS register is read. TEMP_LO is not used when ALERT_MODE[7](0x29) is set for Comparator mode.
TEMP_HI	2	TEMP_HI is asserted when the latest temperature sensor measurement is greater than what is programmed in the Temperature Sensor Alarm High (0x22, 0x23) register. This is a read-only bit. When this bit is asserted and if the TEMP_HI_EN bit is set to 1 then it asserts the interrupt on the INT pin. The controller needs to read the status register to determine if the interrupt was asserted by the TEMP_HI status. When ALERT_MODE[7](0x29) is set for Interrupt mode, TEMP_HI and the interrupt are cleared after the STATUS register is read. When ALERT_MODE is set for Comparator mode, TEMP_HI does not clear on STATUS register read, but the interrupt clears on STATUS register read. TEMP_HI remains asserted until the latest temperature sensor measurement goes lower than what is programmed in the Temperature Sensor Alarm Low (0x24, 0x25) register.
PWR_RDY	0	PWR_RDY is set to 1 when V_{DD} goes below POR threshold, which is nominally 1.42V. If this condition occurs, all registers are reset to their POR state. This bit is not triggered by a soft reset. This is a read-only bit and it is cleared when the Status register is read. PWR_RDY is a non-maskable interrupt, so it gets asserted on INT pin.

Interrupt Enable (0x02)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	TEMP_RDY_EN	TEMP_DEC_FAST_EN	TEMP_INC_FAST_EN	TEMP_LO_EN	TEMP_HI_EN	–	–
Reset	0	0	0	0	0	0	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION
A_FULL_EN	7	Enables A_FULL[7](0x00) status bit to be output to the INT output pin.
TEMP_RDY_EN	6	Enables TEMP_RDY[6](0x00) status bit to be output to the INT output pin.
TEMP_DEC_FAST_EN	5	Enables TEMP_DEC_FAST[5](0x00)status bit to be output to the INT output pin.
TEMP_INC_FAST_EN	4	Enables TEMP_INC_FAST[4](0x00) status bit to be output to the INT output pin.

BITFIELD	BITS	DESCRIPTION
TEMP_LO_EN	3	Enables TEMP_LO[3](0x00) status bit to be output to the INT output pin.
TEMP_HI_EN	2	Enables TEMP_HI[2](0x00) status bit to be output to the INT output pin. Note that when ALERT_MODE[7](0x29) = 1 and AUTO[1](0x2A) = 1, if TEMP_HI_EN needs to be set to 1, no other interrupts should be enabled.

FIFO Write Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_WR_PTR[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
FIFO_WR_PTR	5:0	FIFO_WR_PTR points to the location where the next sample will be written. This pointer advances for each sample pushed on to the circular FIFO. FIFO_WR_PTR is a read-only register. See the FIFO Description section for details.

FIFO Read Pointer (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_RD_PTR[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
FIFO_RD_PTR	5:0	FIFO_RD_PTR points to the location from where the processor gets the next sample from the FIFO via the serial interface. This advances each time a sample is popped from the circular FIFO. FIFO_RD_PTR is a read-only register. See the FIFO Description section for details.

FIFO Counter 1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	–	OVF_COUNTER[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
OVF_COUNTER	5:0	When FIFO is full any new samples will result in new or old samples getting lost depending on FIFO_RO[1](0x0A). OVF_COUNTER counts the number of samples lost. It saturates at 0x3F. This is a read-only register. See the FIFO Description section for details.

FIFO Counter 2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	–	FIFO_DATA_COUNT[6:0]						
Reset	–	0x00						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
FIFO_DATA_COUNT	6:0	FIFO_DATA_COUNT is a read-only register which holds the of the number of items available in the FIFO for the host to read. See the FIFO Description section for details.

FIFO Data (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FIFO_DATA	7:0	FIFO_DATA is a read-only register and is used to get data from the FIFO. See the FIFO Description section for details.

FIFO Configuration 1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_A_FULL[5:0]					
Reset	–	–	0x1F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
FIFO_A_FULL	5:0	FIFO_A_FULL indicates how many new samples can be written to the FIFO before the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there is 15 empty space left (49 entries), and so on. **FIFO_A_FULL** / **FREE SPACE BEFORE INTERRUPT** / **NUMBER OF SAMPLES IN FIFO** 0x0 / 0 / 64 0x1 / 1 / 63 0x2 / 2 / 62 0x3 / 3 / 61 ---- / ---- / ---- 0x3E / 62 / 2 0x3F / 63 / 1 See the FIFO Description section for details.

FIFO Configuration 2 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	–	0	0	0	0	–
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION
FLUSH_FIFO	4	When FLUSH_FIFO bit is set to ‘1’, the FIFO gets flushed, FIFO_WR_PTR[5:0](0x04) and FIFO_RD_PTR[5:0](0x05) are reset to zero and FIFO_DATA_COUNT[6:0](0x07) becomes 0. The contents of the FIFO are lost. FLUSH_FIFO is a self-clearing bit. See the FIFO Description section for details.
FIFO_STAT_CLR	3	See the FIFO Description section for details.
A_FULL_TYPE	2	See the FIFO Description section for details.

BITFIELD	BITS	DESCRIPTION
FIFO_RO	1	FIFO_RO bit controls the behavior of the FIFO when the FIFO becomes completely filled with data. Push to FIFO is enabled when FIFO is full if FIFO_RO = 1 and old samples are lost. Both FIFO_WR_PTR[5:0](0x04) and FIFO_RD_PTR[5:0](0x05) increment for each sample after the FIFO is full. Push to FIFO is disabled when FIFO is full if FIFO_RO = 0 and new samples are lost. FIFO_WR_PTR and FIFO_RD_PTR do not increment for each sample after the FIFO is full. If temperature conversion is in AUTO mode or in External Trigger mode and if CHG_DET_EN[3](0x28) is set to 1, FIFO_RO is ignored and the FIFO always rolls on full. See the FIFO Description section for details.

SYSTEM CONFIGURATION (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RESET
Reset	–	–	–	–	–	–	–	0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	DESCRIPTION
RESET	0	Setting this bit to 1 resets all register settings to default values. This is a self-clearing bit.

PIN CONFIGURATION (0x12)

BIT	7	6	5	4	3	2	1	0
Field	EXT_CVT_EN	EXT_CVT_ICFG	–	–	INT_FCFG[1:0]		INT_OCFG[1:0]	
Reset	0	0	–	–	0x1		0x0	
Access Type	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
EXT_CVT_EN	7	When EXT_CVT_EN is set to 0, external temperature conversion command is disabled. The CVT/PDB pin is used for powering down the part to low power mode. When EXT_CVT_EN is set to 1, CVT/PDB pin is used for external temperature conversion command. AUTO[1](0x2A) and CONVERT_T[0](0x2A) bits are ignored. If a convert command is initiated while temperature conversion is in progress, the current command is ignored.
EXT_CVT_ICFG	6	EXT_CVT_ICFG bit sets the input active edge of the convert input signal on the CVT pin. Active edge is the edge for which the convert input responds.
INT_FCFG	3:2	INT_FCFG sets the functional configuration of the INT pin. This interrupt can be configured to be disabled, cleared on status byte read or to self-clear after two optional prescribed times. See table below for options.

BITFIELD	BITS	DESCRIPTION
INT_OCFG	1:0	INT_OCFG selects the output drive type for the INT pin, as shown in the table below. **INT_OCFG** / **DECODE** 0x0 – Open drain, up to 6V compliant, active low output 0x1 – Active drive to V_{DD} & GND, the active level is a high output. 0x2 – Active drive to V_{DD} & GND, the active level is a low output. 0x3 – Not defined

TEMP ALARM HIGH SETUP (0x20)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_HI_DET_CNTR[2:0]			–	TEMP_HI_TRIP	TEMP_HI_TRIP_CNT[1:0]		TEMP_RST_HI_CNTR
Reset	0x0			–	0	0x0		0
Access Type	Read Only			–	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
TEMP_HI_DET_CNTR	7:5	TEMP_HI_DET_CNTR is a read-only register which holds the count for the number of times the temperature sensor ADC data went above the temperature alarm high threshold after the counter was cleared.
TEMP_HI_TRIP	3	TEMP_HI_TRIP = 0: Programs the alarm high trip type to be consecutive. When the trip type is consecutive, the number of trips programmed with the TEMP_HI_TRIP_CNT[1:0] needs to be consecutive to assert the TEMP_HI[2](0x00) status bit. TEMP_HI_TRIP = 1: Programs the alarm high trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with TEMP_HI_TRIP_CNT[1:0] does not need to be consecutive to assert the TEMP_HI status bit. If ALERT_MODE[7](0x29) = 1 (Comparator Mode), nonconsecutive trip type is not supported.
TEMP_HI_TRIP_CNT	2:1	The TEMP_HI_TRIP_CNT bits program the number of trip counts required to assert the TEMP_HI[2](0x00) status bit. See the table below for the programmable temperature sensor alarm high trip counts. TEMP_HI_TRIP_CNT / TRIP COUNT 0x0 – 1 0x1 – 2 0x2 – 3 0x3 – 4
TEMP_RST_HI_CNTR	0	TEMP_RST_HI_CNTR is a self clearing bit. When set to 1, it clears the count in TEMP_HI_DET_CNTR[2:0] and is cleared itself.

TEMP ALARM LOW SETUP (0x21)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_LO_DET_CNTR[2:0]			–	TEMP_LO_TRIP	TEMP_LO_TRIP_CNT[1:0]		TEMP_RST_LO_CNTR
Reset	0x0			–	0	0x0		0
Access Type	Read Only			–	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
TEMP_LO_DET_CNTR	7:5	TEMP_LO_DET_CNTR is a read only register that holds the count for the number of times the temperature sensor ADC data went below the temperature alarm low threshold after the counter was cleared.
TEMP_LO_TRIP	3	TEMP_LO_TRIP = 0: Programs the alarm low trip type to be consecutive. When the trip type is consecutive, the number of trips programmed with TEMP_LO_TRIP_CNT[1:0] needs to be consecutive to assert the TEMP_LO[3](0x00) status bit. TEMP_LO_TRIP = 1: Programs the alarm low trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with TEMP_LO_TRIP_CNT[1:0] does not need to be consecutive to assert the TEMP_LO status bit. If ALERT_MODE = 1[7](0x29) (Comparator Mode), nonconsecutive trip type is not supported.
TEMP_LO_TRIP_CNT	2:1	The TEMP_LO_TRIP_CNT bits program the number of trip counts required to assert the TEMP_LO[3](0x00) status bit. See the table for the programmable temperature sensor alarm low trip counts. TEMP_LO_TRIP_CNT / TRIP COUNT 0x0 / 1 0x1 / 2 0x2 / 3 0x3 / 4
TEMP_RST_LO_CNTR	0	TEMP_RST_LO_CNTR is a self clearing bit. When set to 1, it clears the count in TEMP_LO_DET_CNTR[2:0] and is cleared itself.

TEMP ALARM HIGH MSB (0x22)

BIT	7	6	5	4	3	2	1	0
Field	ALARM_HI[15:8]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ALARM_HI	7:0	The ALARM_HI[15:8] bits are the most significant byte of the 16-bit temperature sensor alarm high threshold, ALARM_HI[15:0]. The default for the Alarm High threshold is 0x7FFF, which is the highest temperature setting and also disables the alarm.

TEMP ALARM HIGH LSB (0x23)

BIT	7	6	5	4	3	2	1	0
Field	ALARM_HI[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ALARM_HI	7:0	The ALARM_HI[7:0] bits are the least significant byte of the 16-bit temperature sensor alarm high threshold. See ALARM_HI[15:8] for details.

TEMP ALARM LOW MSB (0x24)

BIT	7	6	5	4	3	2	1	0
Field	ALARM_LO[15:8]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ALARM_LO	7:0	The ALARM_LO[15:8] bits are the most significant byte of the 16-bit temperature sensor alarm low threshold, ALARM_LO[15:0]. The default for the Alarm Low threshold is 0x8000, which is the lowest temperature setting and also disables the alarm.

TEMP ALARM LOW LSB (0x25)

BIT	7	6	5	4	3	2	1	0
Field	ALARM_LO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ALARM_LO	7:0	The ALARM_LO[7:0] bits are the least significant byte of the 16-bit temperature sensor alarm low threshold. See ALARM_LO[15:8] for details.

TEMP_INC_FAST_THRESH (0x26)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_INC_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TEMP_INC_THRESH	7:0	TEMP_INC_THRESH sets the positive change-in-temperature slope threshold in units of 5mºC/SAMPLE. It is unsigned. TEMP_INC_THRESH = 5mºC*N/SAMPLE where N={0 to 255}.

TEMP_DEC_FAST_THRESH (0x27)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_DEC_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TEMP_DEC_THRESH	7:0	TEMP_DEC_THRESH sets the negative change-in-temperature slope threshold in units of 5mºC/SAMPLE. It is unsigned. TEMP_DEC_THRESH = 5mºC*N/SAMPLE where N={0 to 255}.

TEMP CONFIGURATION 1 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CHG_DET_EN	RATE_CHG_FILTER[2:0]		
Reset	–	–	–	–	0	0x0		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHG_DET_EN	3	When CHG_DET_EN is set to 0, temperature change detection is disabled, and therefore TEMP_DEC_FAST[5](0x00) and TEMP_INC_FAST[4](0x00) status bits and corresponding interrupts are disabled. Change detection is also disabled atumatically, when EXT_CVT_EN[7](0x12) is set to 0 and AUTO[1](0x2A) is set to 0. When AUTO is set to 1 or if EXT_CVT_EN is set to 1, change detection may be enabled by setting CHG_DET_EN to 1. Note that when EXT_CVT_EN is set to 1, the external convert pulses are expected to be periodic. If the convert pulses are not periodic, change detection is not meaningful, and therefore CHG_DET_EN must be set to 0.
RATE_CHG_FILTER	2:0	RATE_CHG_FILTER selects the length of the change-in-temperature FIR filter.

RATE_CHG_FILTER	NUMBER OF TEMPERATURE SAMPLES
0x0	2
0x1	3
0x2	5
0x3	9
0x4	17
0x5	33
0x6	65
0x7	65

TEMP CONFIGURATION 2 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	ALERT_MODE	–	–	–	TEMP_PERIOD[3:0]			
Reset	0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ALERT_MODE	7	When the ALERT_MODE is set to 0 if autonomous conversion mode is enabled, the MAX30210 is set for interrupt mode alerts. In this mode, the MAX30210 will send an interrupt to the MCU when the temperature passes either the high temperature threshold or the low temperature threshold value. The TEMP_LO[3](0x00) and TEMP_HI[2](0x00) alerts are cleared once the I2C read occurs. When the ALERT_MODE is set to 1 if autonomous conversion mode is enabled, the MAX30210 is set for comparator mode alerts. In this mode, if TEMP_HI_EN[2](0x02) is set to 1, the MAX30210 will send an interrupt to the MCU when the temperature is measured higher than the high temperature threshold. Both the TEMP_HI status and the interrupt pin will stay asserted until the temperature falls below the set low temperature threshold value. The TEMP_LO status is disabled and will always read 0 in this mode. No alerts are cleared once the I2C read occurs. In this mode, TEMP_HI_TRIP[3](0x20) and TEMP_LO_TRIP[3](0x21) are ignored, and only consecutive trip type is supported.	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>TEMP_PERIOD</td><td>3:0</td><td>TEMP_PERIOD sets the sample period for temperature conversion when AUTO[1](0x2A) is set to 1.
<table>
<tr><th>TEMP_PERIOD</th><th>SAMPLE RATE (Hz)</th><th>SAMPLE PERIOD (sec)</th></tr>
<tr><td>0x0</td><td>0.015625</td><td>64</td></tr>
<tr><td>0x1</td><td>0.03125</td><td>32</td></tr>
<tr><td>0x2</td><td>0.0625</td><td>16</td></tr>
<tr><td>0x3</td><td>0.125</td><td>8</td></tr>
<tr><td>0x4</td><td>0.25</td><td>4</td></tr>
<tr><td>0x5</td><td>0.5</td><td>2</td></tr>
<tr><td>0x6</td><td>1</td><td>1</td></tr>
<tr><td>0x7</td><td>2</td><td>0.5</td></tr>
<tr><td>0x8</td><td>4</td><td>0.25</td></tr>
<tr><td>0x9 to 0xF</td><td>8</td><td>0.125</td></tr>
</table></td><td>0x0: 64
0x1: 32
0x2: 16
0x3: 8
0x4: 4
0x5: 2
0x6: 1
0x7: 0.5
0x8: 0.25
0x9 to 0xF: 0.125</td></tr>
</table>

TEMP CONVERT (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUTO	CONVERT_T
Reset	–	–	–	–	–	–	0	0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
AUTO	1	Set AUTO is set to 1 for autonomous mode. In this mode, When CONVERT_T is set to 1, the temperature conversions are continuous at the rate determined by TEMP_PERIOD[3:0](0x29) register. When AUTO is set to 0, one temperature conversion is initiated by the CONVERT_T bit. AUTO bit is ignored if the CVT pin is used for initiating a temperature conversion. See EXT_CVT_EN[7](0x12) description.

BITFIELD	BITS	DESCRIPTION
CONVERT_T	0	Set CONVERT_T = 1 to start temperature data conversions. This bit stays high while conversion is in progress and is set to zero when the conversion completes. For manual mode with AUTO = 0, the conversion is considered complete after one conversion. For auto mode with AUTO = 1, the conversions are continuous at the sample rate programmed in TEMP_PERIOD[3:0](0x29) register, and will not stop until CONVERT_T bit is deasserted. Set CONVERT_T = 0 to immediately abort any conversion in progress. When writing 0 to CONVERT_T bit, it is important to write 0 to AUTO bit as well. So for auto mode, the conversion is considered complete when AUTO and CONVERT_T bits are set to 0. Writing 1 to the CONVERT_T bit is ignored, if temperature conversion is in progress. CONVERT_T bit is ignored if the CVT pin is used for initiating a temperature conversion. See EXT_CVT_EN[7](0x12) description.

TEMP DATA MSB (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_DATA[15:8]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TEMP_DATA	7:0	TEMP_DATA[15:8] is a read-only register that holds the most significant byte of the 16-bit temperature TEMP_DATA[15:0]. TEMP_DATA[15:0] holds the temperature data from the last temperature conversion. This is useful when AUTO[1](0x2A) is set to 0, and CONVERT_T[0](0x2A) is used for initiating a temperature conversion, and the application does not need to read the FIFO. The data is also saved in the FIFO. TEMP_DATA[15:8] and TEMP_DATA[7:0] registers must be read in a single burst using the serial interface, to ensure that the two bytes correspond to the same sample.

TEMP DATA LSB (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TEMP_DATA	7:0	TEMP_DATA[7:0] is a read-only register that holds the least significant byte of the 16-bit temperature TEMP_DATA[15:0]. See TEMP_DATA[15:8] for details.

TEMP SLOPE MSB (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	TEMP_SLOPE[8]
Reset	–	–	–	–	–	–	–	0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
TEMP_SLOPE	0	TEMP_SLOPE[8] is a read-only register and has the most significant bit of the 9-bit temperature slope, TEMP_SLOPE[8:0]. The lower 8 bits are in TEMP_SLOPE[7:0] register. TEMP_SLOPE[8:0] is a 2's compliment number which represents the slope value calculated (0.005C per sample per LSB) for a set of temperature measurements as programmed in the RATE_CHG_FILTER[2:0](0x28) register. TEMP_SLOPE[8] and TEMP_SLOPE[7:0] registers must be read in a single burst using the serial interface, to ensure that the two bytes correspond to the same slope. See Detailed Description section for more information.

TEMP_SLOPE LSB (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_SLOPE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TEMP_SLOPE	7:0	TEMP_SLOPE[7:0] is a read-only register and has the lower byte of the 9-bit temperature slope. The most significant bit is in TEMP_SLOPE[8] register. See TEMP_SLOPE[8] register for details.

UNIQUE ID1 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_1[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_1	7:0	Factory set to unique ID.

UNIQUE ID2 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_2[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_2	7:0	Factory set to unique ID.

UNIQUE ID3 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_3	7:0	Factory set to unique ID.

UNIQUE ID4 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_4[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_4	7:0	Factory set to unique ID.

UNIQUE ID5 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_5[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_5	7:0	Factory set to unique ID.

UNIQUE ID6 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	UNIQUE_ID_6[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNIQUE_ID_6	7:0	Factory set to unique ID.

PART IDENTIFIER (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x45							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PART_ID	7:0	This register stores the part identifier for the chip.

Typical Application Circuits

MAX30210 Single-Point Temperature Sensing

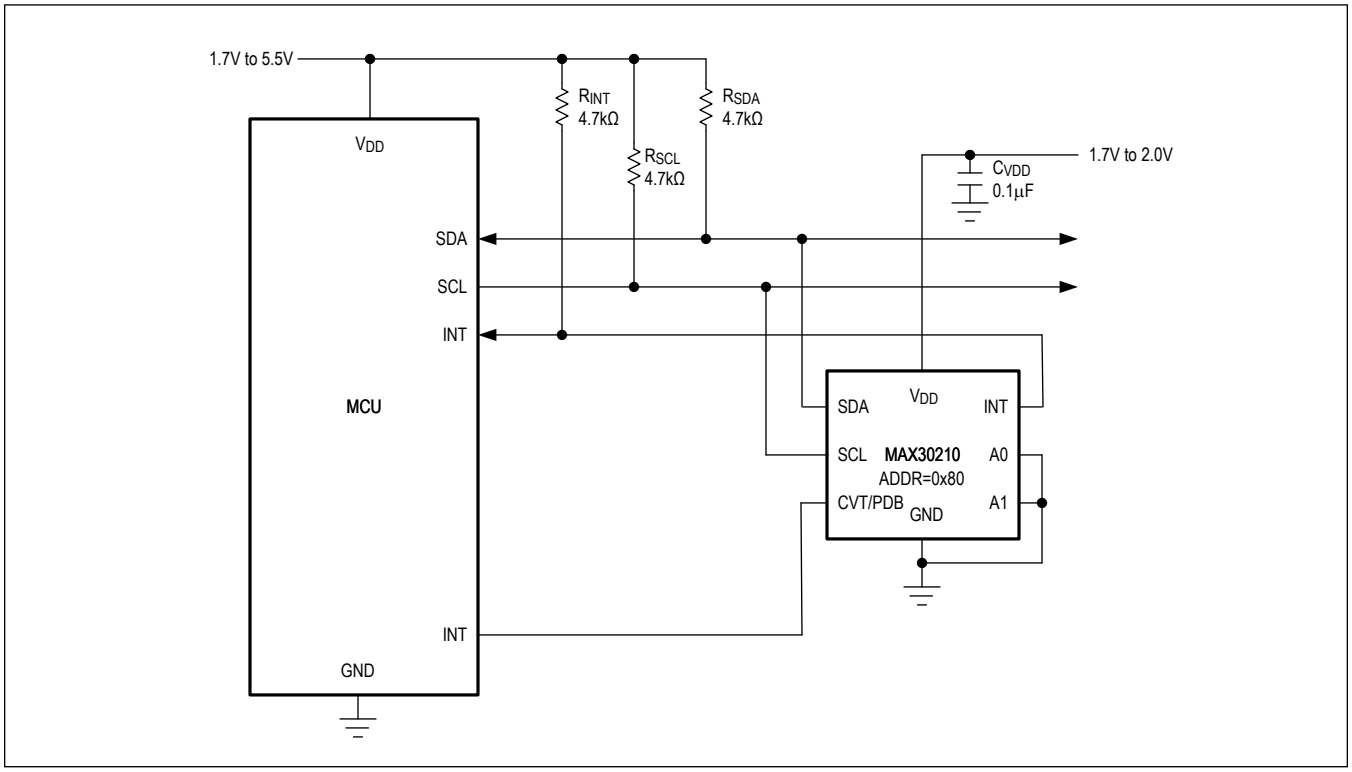


Figure 18. Single-Point Temperature Sensing

Typical Application Circuits (continued)

MAX30210 Multi-Point Temperature Sensing with up to 16 I2C Addresses

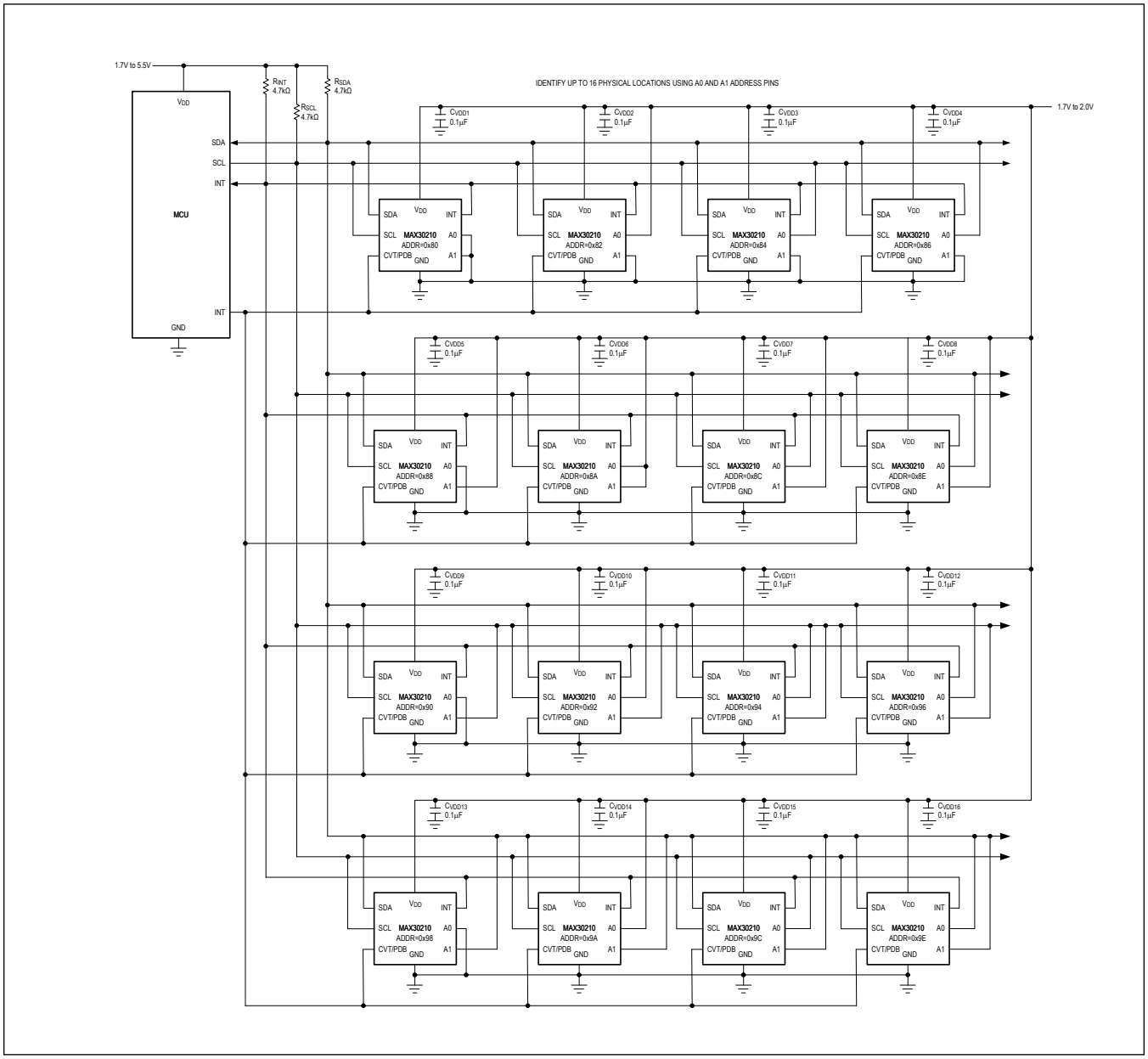


Figure 19. Multi-Point Temperature Sensing

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX30210ENL+	-40°C to +85°C	9 WLP
MAX30210ENL+T	-40°C to +85°C	9 WLP

+Denotes lead(Pb)-free/RoHS compliance.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/22	Release for Market Intro	—

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX30210ENL+T MAX30210ENL+