MAX22516

IO-Link Data Link Controller with Transceiver and Integrated DC-DC

General Description

The MAX22516 IO-Link data link controller integrates a 24V C/Q transceiver, an auxiliary digital input and output, an integrated DC-DC, 5V and 3.3V linear regulators, and a full-feature IO-Link data link controller.

Once configured, the MAX22516 data link controller operates the IO-Link transceiver and requires no intervention from the external microcontroller during normal operation. Alternatively, the IO-Link transceiver can be controlled using the UART interface (TXEN, TX, and RX) directly, or through the serial-peripheral interface (SPI). The data link controller supports and includes, receive and transmit buffers for IO-link communication. Buffers for maximum size process data, ISDU, event, and page data reduce the need for time-critical microcontroller intervention, which allows the microcontroller to focus on the application layer task.

The MAX22516 features extensive integrated protection to ensure robust communication in harsh industrial environments. All IO-Link interface pins (V_{24}, C/Q, DO, DI, and GND), are reverse voltage protected, short-circuit protected, and feature integrated ±1kV/500Ω surge protection.

The MAX22516 is available in a tiny WLP package (3.53mm x 3.16mm) or 40-pin TQFN-EP package (5mm x 5mm) and operates over the -40°C to +125°C temperature range.

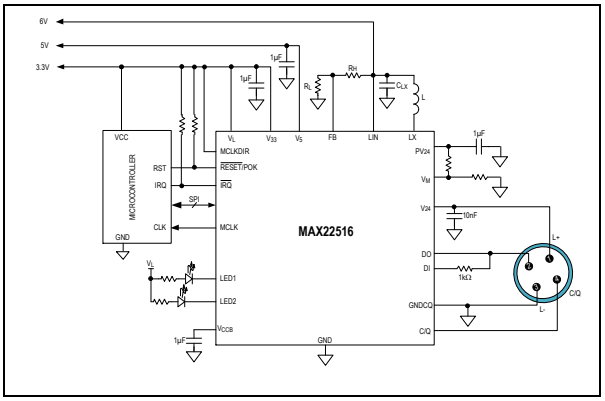
Key Applications

- IO-Link Sensor and Actuator Devices
- Industrial Sensors

Benefits and Features

- Easily Enhance IO-Link Communication
  - COM3: 400µs (min) Cycle Time Support
  - Data Link Controller Autonomously Answers All Master Message Requests
  - Deterministic Device Answer Delay
- Highly Integrated Solution
  - Complete Data Link Layer Includes
    - Message Handler
    - ISDU Handler
    - Page Handler
    - Event Handler
    - Mode Handler
    - Startup Handler
  - 15MHz SPI with Burst Mode
  - High Efficiency 200mA DC-DC with Adjustable Output
  - High Accuracy 3.3V and 5V Linear Regulators
- Flexible Application
  - Transparent (TX, RX, TXEN) Mode Option
  - LED Drivers with Programmable Sequence
  - COM1, COM2, and COM3 Data Rates
- Robust and Reliable Design
  - Integrated ±1kV/500Ω Surge Protection
- Optimized for Small Sensor Designs
  - Available in Small WLP (3.53mm x 3.16mm) and 40-pin TQFN-EP (5mm x 5mm) Packages

Simplified Application Diagram



***Ordering Information* appears at end of data sheet.**

19-101758; Rev 2; 3/24

Absolute Maximum Ratings

All voltages referenced to GND, unless otherwise noted.

POWER

V_{24} (Continuous) ..... -36V to +36V

V_{24} (Peak, 100µs) ..... -52V to +65V

PV_{24} (Continuous) ..... -0.3V to +36V

PV_{24} (Peak, 100µs) MAX(-0.3V, V_{24} - 52V) to MIN(+52V, V_{24} + 52V)

V_5, V_L, V_M, FB, V_{CCB} ..... -0.3V to +6V

V_{33} ..... -0.3V to (V_5 + 0.3V)

LX ..... -0.3V to (PV_{24} + 0.3V)

LIN (Continuous) ..... MAX(-0.3V, V_5 - 0.3V) to +36V

LIN (Peak, 100µs) ..... MAX(-0.3V, V_5 - 0.3V) to +52V

24V I/O

C/Q, DO (Continuous) MAX(-36V, V_{24} - 36V) to MIN(+36V, V_{24} + 36V)

C/Q, DO (Peak, 100µs) MAX(-52V, V_{24} - 60V) to MIN(+52V, V_{24} + 60V)

CQGND ..... -0.3V to +0.3V

DI (Continuous) ..... -36V to +36V

DI (peak 100µs) ..... -52V to +52V

LOGIC INPUTS

$\overline{CS}$, SCLK, SDI, TX, TXEN, LO, CRCEN, MCLKDIR -0.3V to (V_L + 0.3V)

LOGIC OUTPUTS

SDO, RX, MCLK, LI ..... -0.3V to (V_L + 0.3V)

$\overline{IRQ}$, $\overline{WU}$/HEART, LED1, LED2, $\overline{CRCERR}$, $\overline{WDG}$, $\overline{RESET}$/POK ..... -0.3V to +6V

GPIO1, GPIO2 ..... -0.3V to (V_L + 0.3V)

CURRENT

Continuous Current into V_{24}, LX, GND, or GNDCQ ..... ±1A

Continuous Current into PV_{24} ..... ±200mA

Peak Current into PV_{24} (100µs) ..... ±1A

Continuous Current into C/Q ..... ±500mA

Continuous Current into Any Other Pin ..... ±50mA

CONTINUOUS POWER DISSIPATION

40-pin TQFN-EP (T_A = +70°C, derates at 28mw/°C above +70°C) 2857mW

42-bump WLP (T_A = +70°C, derates at 27.5mw/°C above +70°C) 1510mW

TEMPERATURE

Operating Temperature Range ..... -40°C to +125°C

Maximum Junction Range ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (Reflow) (TQFN only, soldering 10 sec) ..... +300°C

Bump Reflow Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

40 TQFN-EP

Package Code	T4055+1C
Outline Number	*21-0140*
Land Pattern Number	*90-0016*
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	45°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	28°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

42 WLP

Package Code	W423H3+1
Outline Number	*21-100631*
Land Pattern Number	Refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	36.38°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{24} = 7V to 36V, V_5 = 4.85V to 5.5V, V_L = 2.5V to 5.5V, V_{GNDCQ} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are = at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
POWER SUPPLY							
V_{24} Supply Voltage	V_{24}			8		36	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising		7	7.5	8	V
		V_{24} falling		6.3	6.9	7.5	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}				530		mV
V_{24} Supply Current	I_{24}	No load on C/Q, DO, V_5 powered externally, DC-DC disabled, MCLK disabled	C/Q, DO disabled, V_{33} enabled	0.01	0.05	0.10	mA
			C/Q, DO in push-pull, and is high or low	0.42	0.6	0.75	
		V_5 powered externally, DC-DC enabled, MCLK enabled	C/Q, DO in push-pull and is high or low	0.60	0.75	0.95	
V_5 Supply Voltage	V_5	V_5 supplied externally		4.85		5.5	V
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 rising		3.15	3.27	3.40	V
		V_5 falling		3.10	3.22	3.35	
V_5 Supply Current	I_5	V_5 powered externally, DC-DC disabled, MCLK disabled, V_{33} enabled, no load on V_{33}	C/Q, DO disabled	1.5	2.4	3.0	mA
			C/Q, DO in push-pull mode, no load on C/Q, DO	2.1	3	3.7	
		V_5 powered externally, DC-DC enabled, MCLK enabled and set to 29.48MHz, C/Q in push-pull and is high or low		2.9	4	5	
V_L Logic Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}	V_L rising				1.35	V
		V_L falling		0.45			
V_L Logic Level Supply Current	I_L	All logic inputs at GND or V_L, no load on any logic outputs, MCLK disabled				10	µA
DC-DC SWITCHING REGULATOR							
Input Voltage Range	V_{24_DC}	V_{24} is the input to the DC-DC		7		36	V
DC-DC Turn-on Delay	t_{DC_ON}	Delay from V_{24} crossing V_{24UVLO} threshold until the DC-DC regulator finishes soft-start and $\overline{RESET}$/POK rises			2.22		ms
Switching Frequency	f_{DC_H}	BuckSS = 0		1.140	1.229	1.330	MHz
	f_{DC_HSPRD}	BuckSS = 1			1.229		
Spread Spectrum	Δf_{DC_SPRD}	BuckSS = 1		-11.5		+13.5	%
Feedback (FB) Regulation Voltage	V_{DC_FB}			0.8865	0.9	0.9135	V

(V_{24} = 7V to 36V, V_5 = 4.85V to 5.5V, V_L = 2.5V to 5.5V, V_{GNDCQ} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are = at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Accuracy	ACC_{DCFB}		-1.5	0	+1.5	%
Feedback (FB) OK Threshold	V_{DC_FBOK}		92	95	98	$\%V_{DC\_FB}$
Feedback (FB) Low Threshold	$V_{DC\_FBTHLOW}$		61	65	70	$\%V_{DC\_FB}$
LX On-Resistance (High Side)	R_{DC_HS}	From V_{24} to LX, LX is sinking current (Note 2)		2.2	3.9	Ω
LX On-Resistance (Low Side)	R_{DC_LS}	From LX to GND (Note 2)		1.3	2.8	Ω
Active Diode On-Resistance	R_{DC_ACT}	DC current (Note 2)		3.0	5.5	Ω
Maximum Peak Current into Active Diode	I_{DC_ACTMAX}		300			mA
Maximum LX Current Ripple	ΔI_{DC_LX}			100		%
High-Side Peak Current Limit	I_{DC_HSLIM}		+350	+390	+440	mA
Low-Side Current Limit	I_{DC_LSMAX}		-240	-190	-150	mA
DC-DC Autoretry Period	$t_{DCRETRY}$			22		ms
External Capacitance on PV_{24}	C_{DC_PV24}			1		µF
LX Leakage Current	I_{LX_LKG}	$0V < V_{LX} < 36V$	-1		+1	µA
FB Input Bias Current	I_{FB_LKG}	$0 \le V_{FB} \le 1V$, T_A = 25°C	-100		+100	nA
FB Threshold for POK Assertion	V_{FBOK_F}	V_{FB} falling	89	92	95	$\%V_{FB}$
		V_{FB} rising	92	95	98	
FB Undervoltage Trip Threshold	V_{FB_LOW}		61	64.5	70	$\%V_{FB}$
LX Minimum On-Time	t_{LX_MINON}	(Note 2)		64	92	ns
LX Minimum Off-Time	t_{LX_MINOFF}	(Note 2)		32	60	ns
V_{CCB} LINEAR REGULATOR (V_{CCB})						
V_{CCB} Output Voltage	V_{CCB}	$8V \le V_{PV24} \le 36V$, $0mA \le I_{LOAD} \le 5mA$	4.85	5	5.15	V
V_{CCB} Current Limit	I_{CCB_MAX}	V_{PV24} = 8V	10			mA
5V LINEAR REGULATOR (V_5)						
V_5 Input Supply Voltage	V_{LIN}		6		36	V
V_5 Output Voltage	V_5	$6V \le V_{LIN} \le 36V$, no load on V_5	4.85	5	5.15	V
V_5 Load Regulation	$\Delta V5_{LDR}$	V_{LIN} = 24V, $1mA \le I_{LOAD} \le 50mA$		0.6	2.0	%
V_5 Line Regulation	$\Delta V5_{LNR}$	$6V \le V_{LIN} \le 36V$, I_{LOAD} = 1mA		0.05	0.2	mV/V
V_5 Load Capacitance	C_{V5}	External capacitance on V_5		1		µF
3.3V LINEAR REGULATOR (V_{33})						
V_{33} Output Voltage	V_{33}	No load	3.15	3.3	3.45	V
V_{33} Load Regulation	ΔV_{33_LR}	$1mA \le I_{LOAD} \le 100mA$, LIN and V_5 shorted	0	0.9	3	%
V_{33} Load Capacitance	C_{V33}	External capacitance on V_{33}		1		µF
C/Q, DO DRIVERS						

(V_{24} = 7V to 36V, V_5 = 4.85V to 5.5V, V_L = 2.5V to 5.5V, V_{GNDCQ} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are = at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q, DO Driver High-Side On-Resistance	R_{CQOH}	High-side enabled, CQ_CL[1:0] or DO_CL[1:0] = 01, I_{LOAD} = +150mA (Note 2)			2.4	4.4	Ω
C/Q, DO Driver Low-Side On-Resistance	R_{CQLO}	Low-side enabled, CQ_CL[1:0] or DO_CL[1:0] = 01, I_{LOAD} = -150mA (Note 2)			2.0	4.0	Ω
C/Q, DO Driver Current Limit	I_{CL}	V_{DROP} = 3V (Note 3)	CQ_CL[1:0] or DO_CL[1:0] = 00	50	60	70	mA
			CQ_CL[1:0] or DO_CL[1:0] = 01	100	120	140	
			CQ_CL[1:0] or DO_CL[1:0] = 10	200	230	260	
			CQ_CL[1:0] or DO_CL[1:0] = 11	250	289	330	
C/Q Leakage Current	I_{LEAK_CQ}	V_{24} = 24V, (V_{24} - 36V) ≤ $V_{C/Q, DO}$ ≤ 36V, Driver disabled, C/Q receiver disabled	C/Q driver	-32		+40	µA
DO Leakage Current	I_{LEAK_DO}	V_{24} = 24V, (V_{24} - 36V) ≤ V_{DO} ≤ 36V, Driver disabled	DO driver	-22		+4	µA
C/Q, DO Output Reverse Current	I_{REV_CQ}	Driver enabled and in push-pull, $V_{C/Q, DO}$ = (V_{24} + 5V) or (V_{GND} - 5V)		-90		+375	µA
C/Q, DO Weak Pull-Down Current	I_{CQPD}	Driver disabled, $V_{C/Q, DO}$ > 5V, CQ_PD = 1 or DO_PD = 1, CQ_PU = 0 or DO_PU = 0, CQPu2mA = 0 or DOPu2mA = 0		-220	-193	-160	µA
C/Q, DO Weak Pull-Up Current	I_{CQPU}	Driver disabled, $V_{C/Q, DO}$ = (V_{24} - 5V), CQ_PD = 0 or DO_PD = 0, CQ_PU = 1 or DO_PD = 1, CQPu2mA = 0 or DOPu2mA = 0		+160	+200	+260	µA
C/Q, DO 2mA Pull-Down Current	I_{CQPD2}	Driver disabled, $V_{C/Q, DO}$ > 5V, CQ_PD = 1 or DO_PD = 1, CQ_PU = 0 or DO_PU = 0, CQPu2mA = 1 or DOPu2mA = 1		-2.5	-2.2	-2.0	mA
C/Q, DO 2mA Pull-Up Current	I_{CQPU2}	Driver disabled, $V_{C/Q, DO}$ = (V_{24} - 5V), CQ_PD = 0 or DO_PD = 0, CQ_PU = 1 or DO_PU = 1, CQPu2mA = 1 or DOPu2mA = 1		2.0	2.2	2.5	mA
C/Q, DI RECEIVERS							
Input Voltage Range	V_{RIN}	For valid RX /LI logic		V_{24} - 36V		36	V
Input Threshold High	V_{THR}	Receiver enabled	V_{24} ≥ 18V	11		12.5	V
			V_{24} < 18V	54		80	%V_{24}
Input Threshold Low	V_{TLR}	Receiver enabled	V_{24} ≥ 18V	9		10.5	V
			V_{24} < 18V	45		68.1	%V_{24}
Input Hysteresis	V_{HYSR}	Receiver enabled	V_{24} ≥ 18V		2		V
			V_{24} < 18V		11		%V_{24}

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C/Q Input Threshold High (TTL Mode)	V_{TH_TTL}	C/Q driver disabled, RXTTL = 1	2.10		3.45	V
C/Q Input Threshold Low (TTL Mode)	V_{TL_TTL}	C/Q driver disabled, RXTTL = 1	1.1		1.8	V
Input Hysteresis (TTL Mode)	V_{HYSTTL}	Driver disabled, RXTTL = 1		1.38		V
C/Q Receiver Input Capacitance	C_{IN_CQ}	Driver disabled, CQ_PD = 0, CQ_PU = 0, f = 100kHz		35		pF
DI Receiver Input Capacitance	C_{IN_DI}			2		pF
VOLTAGE MONITOR INPUT						
V_M Voltage Range	V_M		0		5.5	V
V_M Threshold Voltage	V_{M_R}	Rising	0.87	0.9	0.93	V
	V_{M_F}	Falling	0.83	0.86	0.89	
V_M Threshold Hysteresis	V_{M_HYS}			0.04		V
V_M Input Current	I_M		-1		+1	µA
RESET/POWER OK ($\overline{RESET}$/POK)						
$\overline{RESET}$/POK Input Voltage Low	V_{RSTIL}		0.4			V
$\overline{RESET}$/POK Input Voltage High	V_{RSTIH}				1.3	V
$\overline{RESET}$/POK Output Voltage Low	V_{POKLOW}	I_{LOAD} = -5mA			+0.12	V
$\overline{RESET}$/POK High Impedance Leakage Current	I_{RST_OD}	$\overline{RESET}$/POK not asserted	-1		+1	µA
LOGIC INPUTS ($\overline{CS}$, SCLK, SDI, TX, TXEN, LO, GPIO1, GPIO2, MCLK, MCLKDIR, CRCEN)						
Logic Input Voltage Low Threshold	V_{IL}				0.31 x V_L	V
Logic Input Voltage High Threshold	V_{IH}		0.68 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
GPIO_ Pull-Up Resistance	R_{GPIO_UP}		200	330	460	kΩ
GPIO_ Pull-Down Resistance	R_{GPIO_DN}		200	330	460	kΩ
LOGIC OUTPUTS ($\overline{WU}$/HEART, $\overline{IRQ}$, SDO, RX, LI, MCLK, GPIO1, GPIO2, LED1, LED2, $\overline{CRCERR}$, $\overline{WDG}$)						
Logic Output Voltage Low	V_{OL}	I_{LOAD} = -5mA			0.4	V
Logic Output Voltage High	V_{OH}	SDO, RX, LI, MCLK, GPIO1, GPIO2; I_{LOAD} = +5mA	V_L - 0.4			V
Open-Drain High Impedance Leakage Current	I_{LK_OD}	$\overline{IRQ}$, $\overline{WU}$/HEART, $\overline{CRCERR}$, LED1 and LED2, not asserted	-1		+1	µA
SDO Leakage Current	I_{LK_SDO}	$\overline{CS}$ = high	-1		+1	µA
RX Leakage Current	I_{LK_RX}	RX = GND or V_L	-1		+1	µA

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL THERMAL SENSOR							
Programmable Thermal Warning Threshold Range	T_{WRN_RNG}	Typical range		-15		+174	°C
Programmable Thermal Warning Threshold Step	T_{WRN_LSB}	1 LSB			3		°C
Thermal ADC Resolution	T_{WRN_RES}				6		bit
Thermal ADC Accuracy	ΔT_{PREC_25C}	T_J = 25°C (Note 2)		-8	0	+8	°C
	ΔT_{PREC_125C}	T_J = 125°C (Note 2)		-7	3	+12	
Thermal ADC Conversion Time	t_{ADC_CONV}				450		µs
THERMAL PROTECTION							
C/Q, DO Driver Shutdown Temperature	T_{SHUT_DRV}	Driver temperature rising, driver fault bit is set and driver is disabled			+165		°C
C/Q, DO Driver Shutdown Hysteresis	T_{SHUT_DHYS}	Driver temperature falling, driver is automatically re-enabled, TSHOFFEN = 0			9		°C
IC Thermal Warning Threshold	T_{WRN}	Die temperature rising, ThW and ThWInt bits are set			+135		°C
IC Thermal Warning Threshold Hysteresis	T_{WRN_HYS}	Die temperature falling, ThW bit is cleared			9		°C
IC Thermal Shutdown Threshold	T_{SHUT_IC}	Die temperature rising, ThShd bit set			+175		°C
IC Thermal Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature falling, ThShd bit is cleared			26		°C
AC ELECTRICAL CHARACTERISTICS							
C/Q, DO DRIVERS							
C/Q, DO Driver Low-to-High Propagation Delay	t_{PDLH_PP}	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00, Figure 1	Push-pull or PNP mode	0.32	0.61	0.90	µs
	t_{PDLH_OC}	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00, Figure 1	NPN mode		1		
C/Q, DO Driver High-to-Low Propagation Delay	t_{PDHL_PP}	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00, Figure 1	Push-pull or NPN mode	0.41	0.65	0.92	µs
	t_{PDHL_OC}	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00, Figure 1	PNP mode		1		
C/Q, DO Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00		-0.2		+0.2	µs
C/Q, DO Driver Rise Time	t_{RISE}	Push-pull or PNP mode, V_{24}(max) = 30V, Figure 1	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00	0.2	0.36	0.56	µs

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Push-pull or PNP mode, V_{24}(max) = 30V, *Figure 1*	CQ_SLEW[1:0] = 01 or DO_SLEW[1:0] = 01	0.38	0.69	1.04	
			CQ_SLEW[1:0] = 10 or DO_SLEW[1:0] = 10	0.80	1.63	2.65	
			CQ_SLEW[1:0] = 11 or DO_SLEW[1:0] = 11	2.2	6.3	11.5	
C/Q, DO Driver Fall Time	t_{FALL}	Push-pull or NPN mode, V_{24}(max) = 30V, *Figure 1*	CQ_SLEW[1:0] = 00 or DO_SLEW[1:0] = 00	0.18	0.32	0.50	µs
		Push-pull or NPN mode, V_{24}(max) = 30V, *Figure 1*	CQ_SLEW[1:0] = 01 or DO_SLEW[1:0] = 01	0.38	0.63	1.00	
			CQ_SLEW[1:0] = 10 or DO_SLEW[1:0] = 10	1	1.56	2.5	
			CQ_SLEW[1:0] = 11 or DO_SLEW[1:0] = 11	4	7.32	12	
C/Q, DO Driver Enable Time High	t_{ENH}	Push-pull or PNP mode, *Figure 3*		0.35	0.64	0.94	µs
C/Q, DO Driver Enable Time Low	t_{ENL}	Push-pull or NPN mode, *Figure 2*		0.27	0.43	0.67	µs
C/Q, DO Driver Disable Time High	t_{DISH}	Push-pull or PNP mode, *Figure 3*		1.2	1.8	2.4	µs
C/Q, DO Driver Disable Time Low	t_{DISL}	Push-pull or NPN mode, *Figure 2*		1.2	1.93	2.6	µs
C/Q, DI RECEIVERS							
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH}	*Figure 4*	RXFilter = 1	0.83	1.28	1.8	µs
			RXFilter = 0	0.27	0.39	0.51	
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL}	*Figure 4*	RXFilter = 1	0.75	1.16	1.7	µs
			RXFilter = 0	0.18	0.28	0.38	
DI Receiver Low-to-High Propagation Delay	t_{PRLH}	*Figure 4*	RXFilter = 1	0.97		2.30	µs
			RXFilter = 0	0.45		1.05	
DI Receiver High-to-Low Propagation Delay	t_{PRHL}	*Figure 4*	RXFilter = 1	0.85		2.05	µs
			RXFilter = 0	0.35		0.78	
WAKE-UP DETECTION (*Figure 5*)							
Wake-Up Input Minimum Pulse Width	t_{WUMIN}	C/Q load capacitance = 3nF		60	66	70	µs

(V_{24} = 7V to 36V, V_5 = 4.85V to 5.5V, V_L = 2.5V to 5.5V, V_{GNDCQ} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are = at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Wake-Up Input Maximum Pulse Width	t_{WUMAX}			85	95	110	µs
$\overline{WU}$/HEART Output Low Time	t_{WUL}	Valid wake-up condition on C/Q, $\overline{WU}$/HEART configured as Wake-up output		150	200	250	µs
MCLK CLOCK							
MCLK Output Frequency	f_{MCLK}	MCLKDIR = high	ClkDiv[2:0] = 000	3.55	3.684	3.81	MHz
			ClkDiv [2:0] = 001	7.10	7.37	7.62	
			ClkDiv [2:0] = 010	14.1	14.71	15.3	
			ClkDiv [2:0] = 011	28	29.4	31	
			ClkDiv [2:0] = 100	1.78	1.843	1.91	
SPI TIMING ($\overline{CS}$, SCLK, SDI, SDO) (*Figure 6*)							
Maximum SCLK Frequency	f_{SPI_MAX}	With 50% duty cycle on SCLK				15	MHz
SCLK Clock Period	t_{CH+CL}			40			ns
SCLK Pulse Width High	t_{CH}			8			ns
SCLK Pulse Width Low	t_{CL}			32			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}			9			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			11			ns
SDI Hold Time	t_{DH}			6			ns
SDI Setup Time	t_{DS}			8			ns
SDO Output Data Propagation Delay	t_{DO}					20	ns
SDO Rise and Fall Times	t_{FT}				0.5	4	ns
Minimum $\overline{CS}$ Pulse	t_{CSW}				20		ns
EMC TOLERANCE							
ESD Protection (V_{24}, C/Q, DO, DI Pins to GND)		IEC 61000-4-2 contact discharge			±3		kV
ESD Protection (All Other Pins)		Human body model			±2		kV
Surge Protection (V_{24}, C/Q, DO, DI Pins)	V_{SRG}	500Ω 8/20µs surge to ground			±1.2		kV

Note 1: All devices 100% production tested at T_A = 25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Not production tested. Guaranteed by design.

Note 3: V_{DROP} is measured as the voltage from the driver output to GND (V_{DRIVER} - V_{GND}) when measuring the low-side driver current limit and as (V_{24} - V_{DRIVER}) when measuring the high-side current limit.

Timing Diagrams

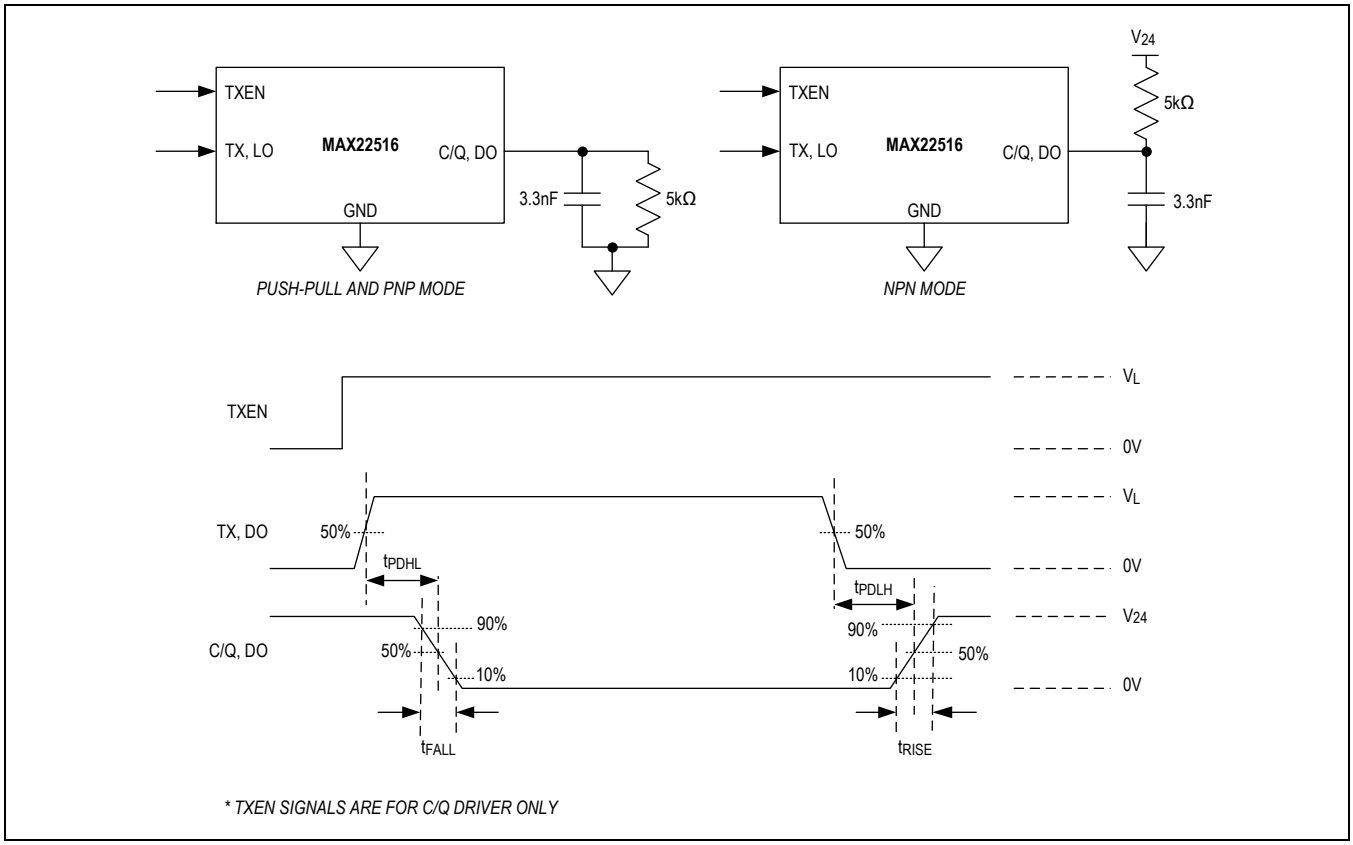


Figure 1. C/Q Driver Propagation Delays

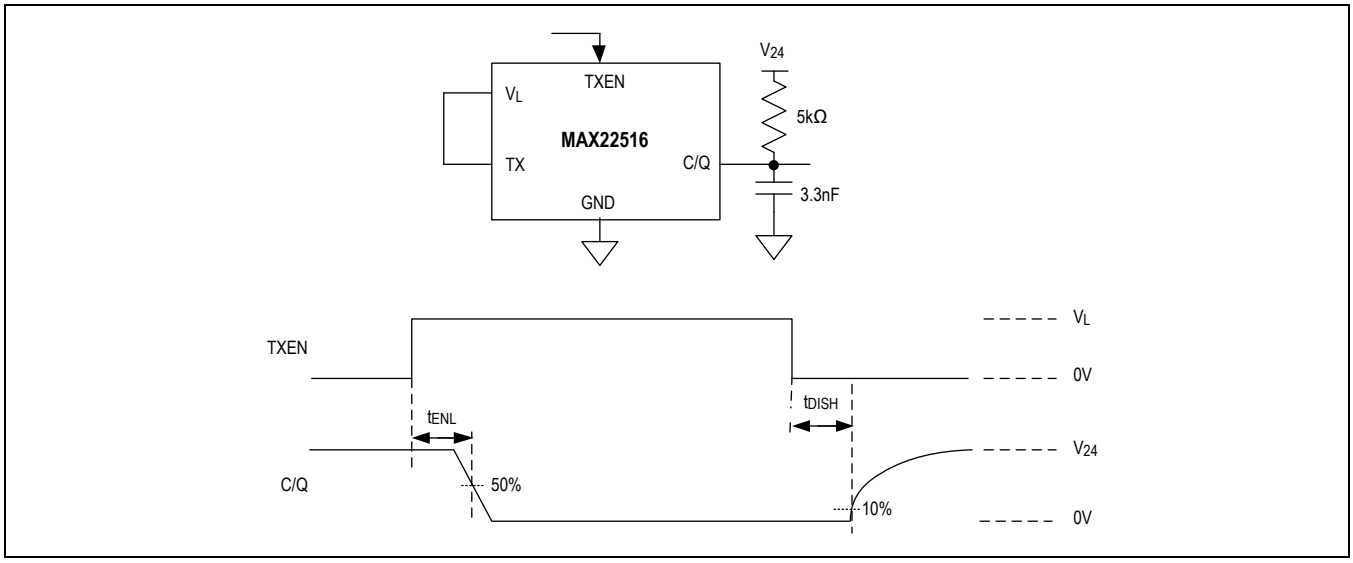


Figure 2. C/Q Driver Enable Low and Disable High Timing

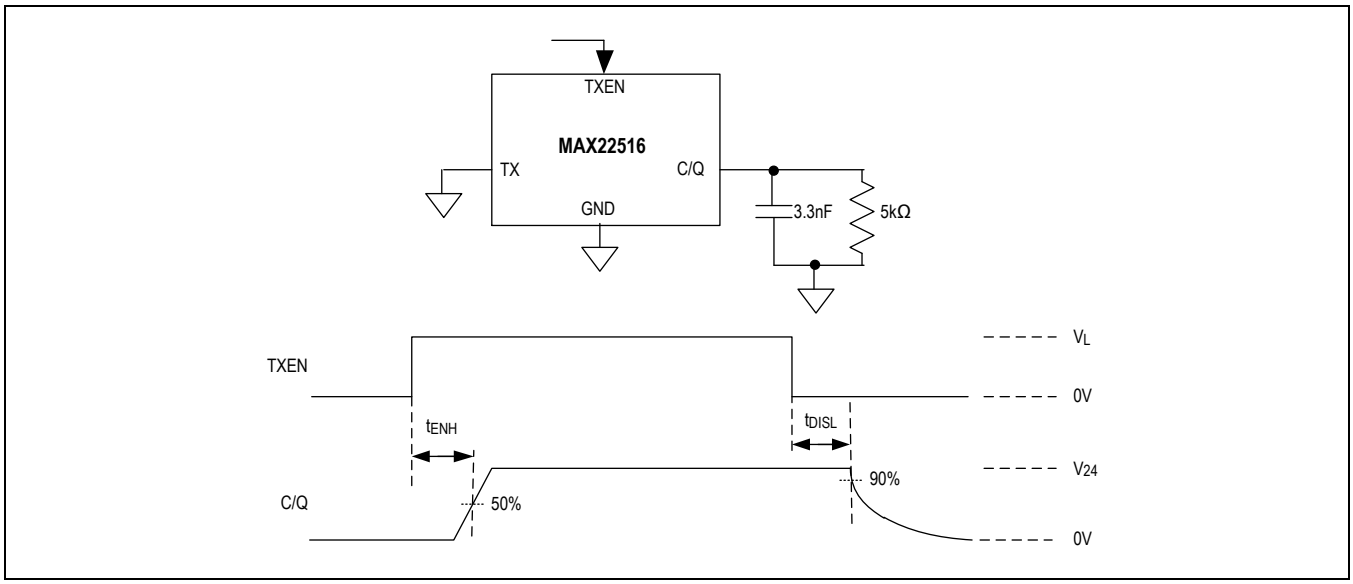


Figure 3. C/Q Driver Enable High and Disable Low Timing

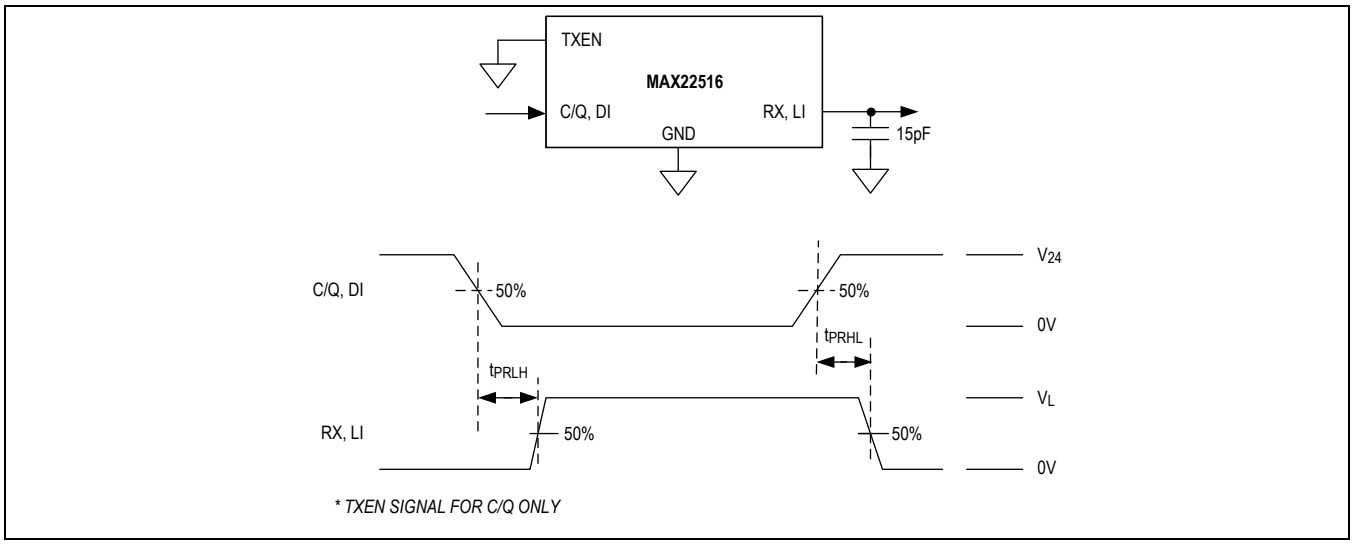


Figure 4. C/Q Receiver Timing

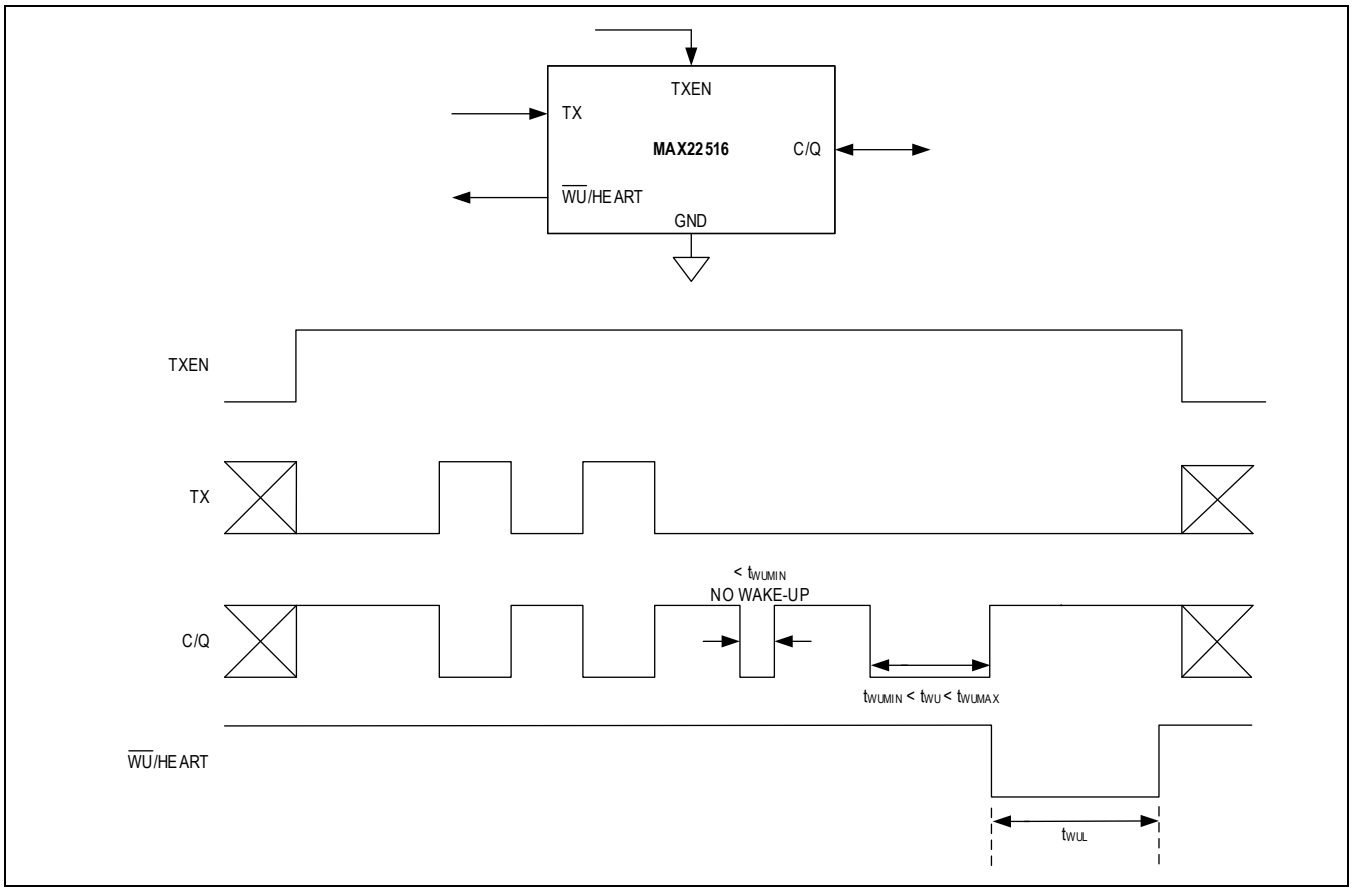


Figure 5. Wake-Up Detection

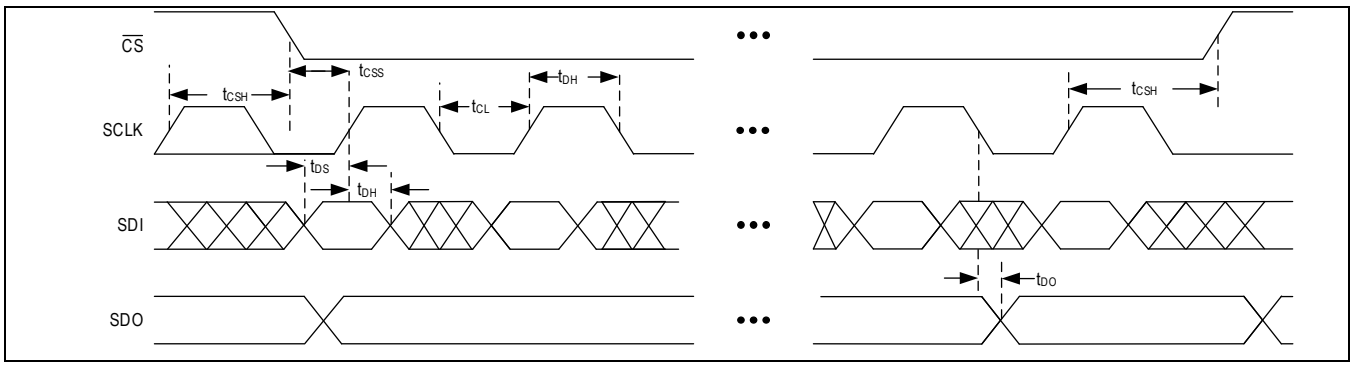
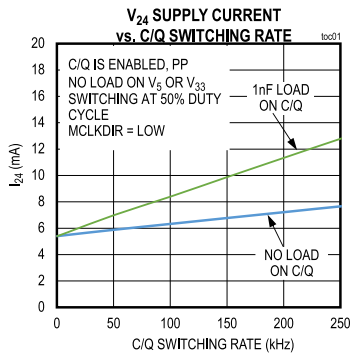
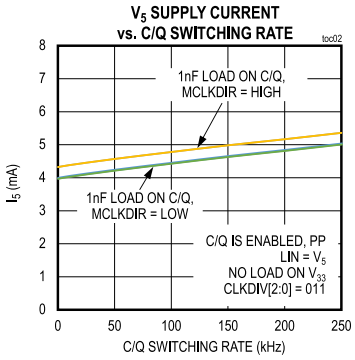


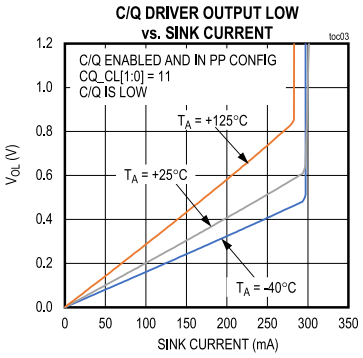
Figure 6. SPI Timing Diagram

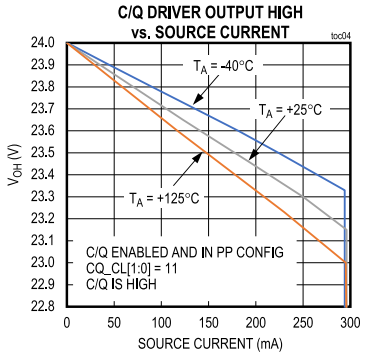
Typical Operating Characteristics

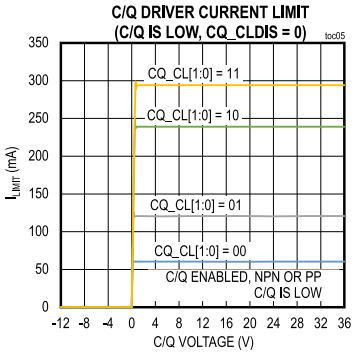
V_{24} = 24V, LIN = DC-DC output = 6V, V_L = V_{33}, T_A = 25°C, unless otherwise noted.

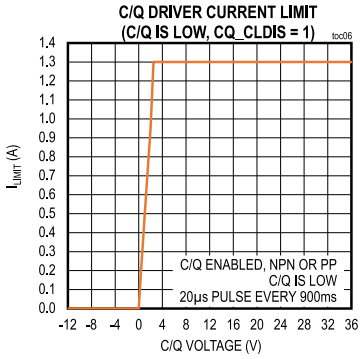


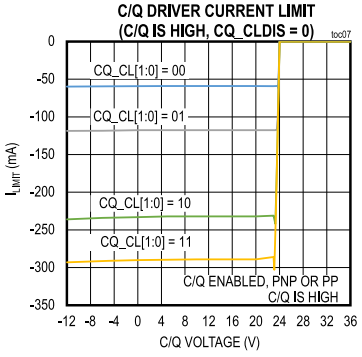


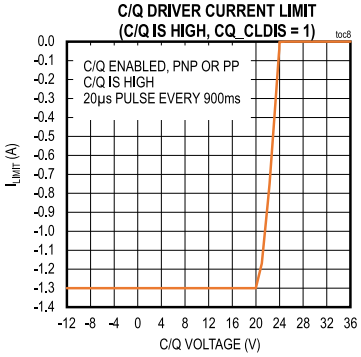


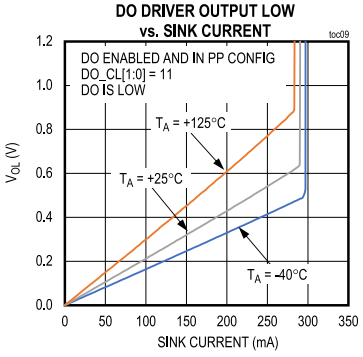












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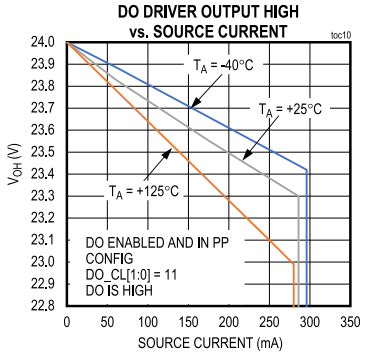
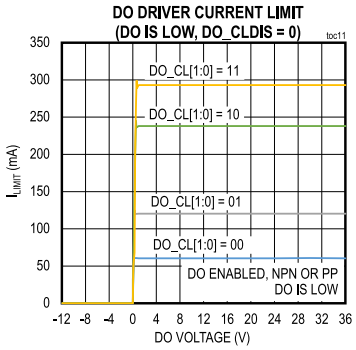
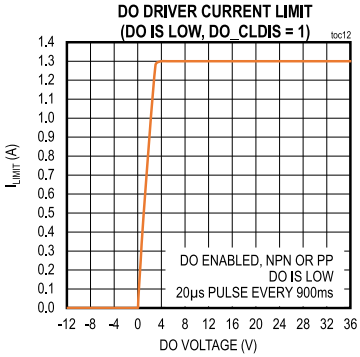
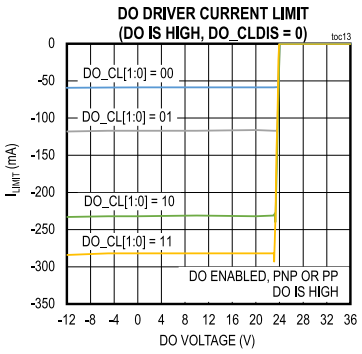
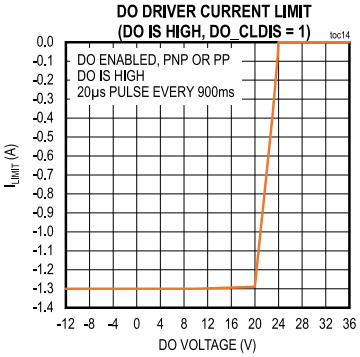
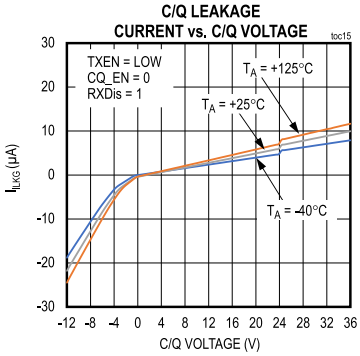


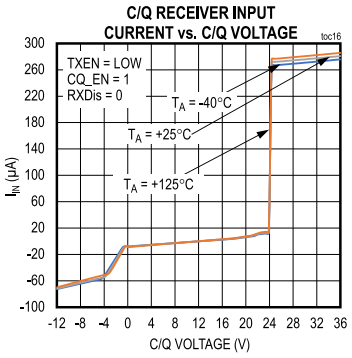


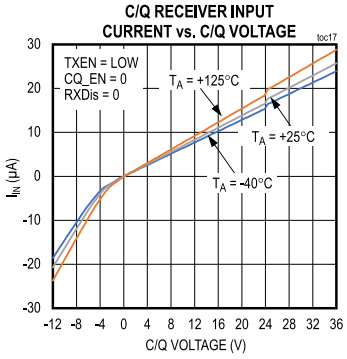


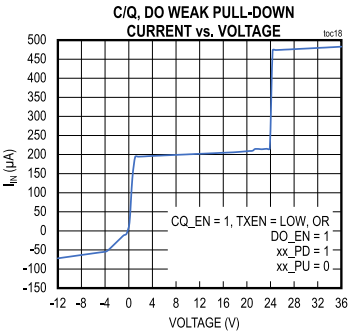




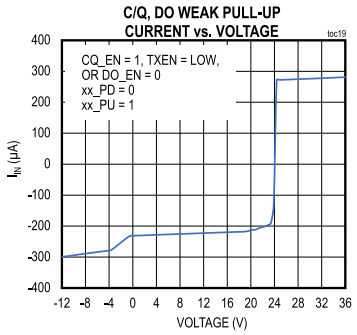


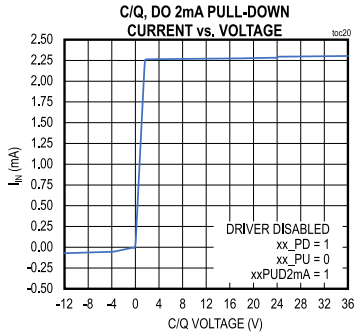


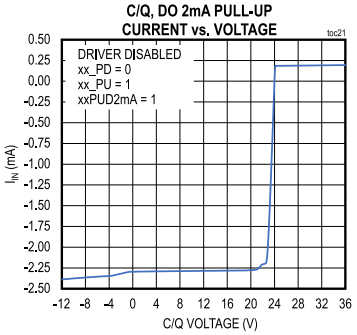


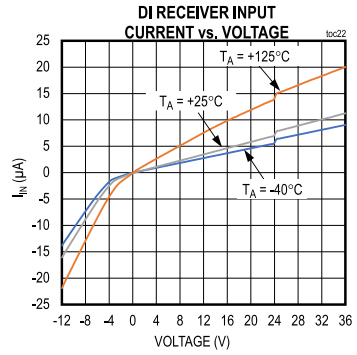


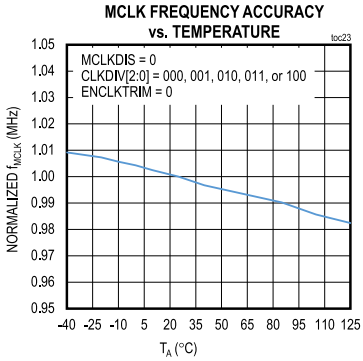
V_{24} = 24V, LIN = DC-DC output = 6V, V_L = V_{33}, T_A = 25°C, unless otherwise noted.

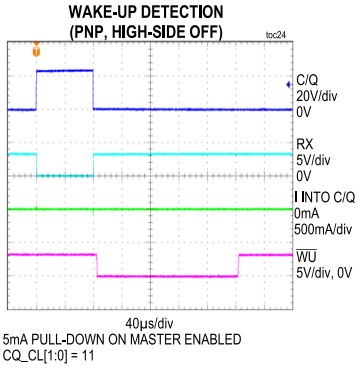


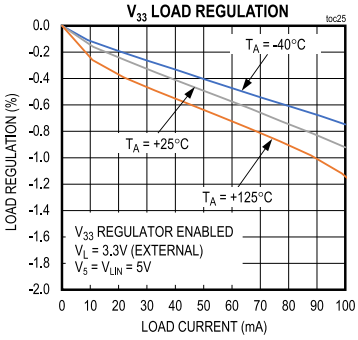


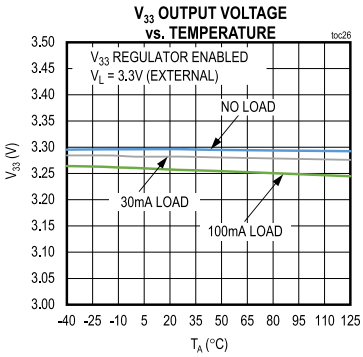


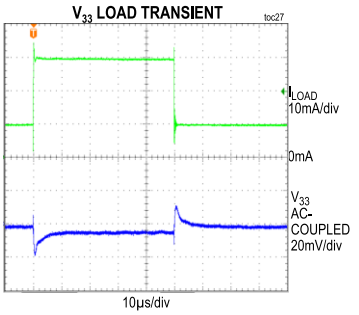




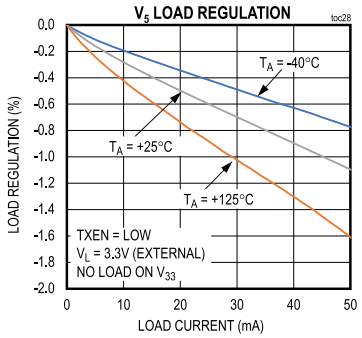


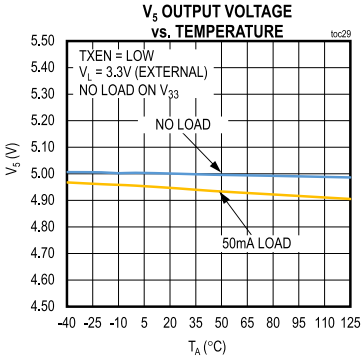


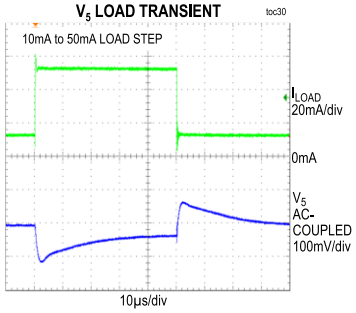


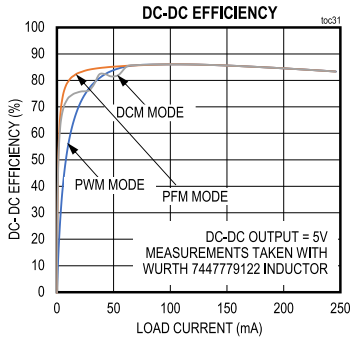


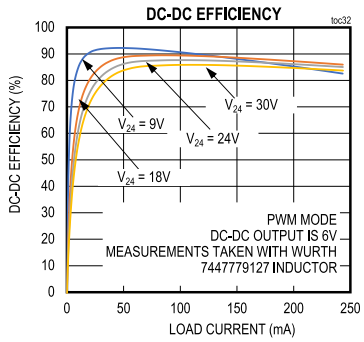
V_{24} = 24V, LIN = DC-DC output = 6V, V_L = V_{33}, T_A = 25°C, unless otherwise noted.

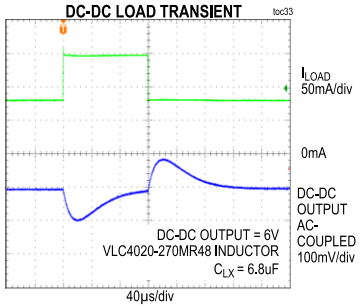


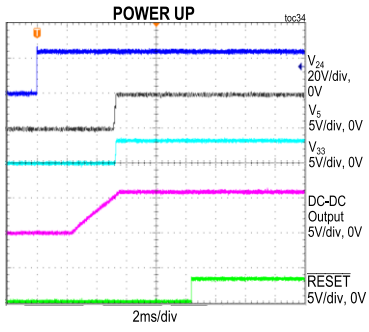


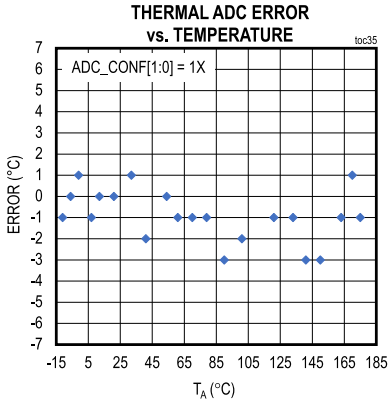




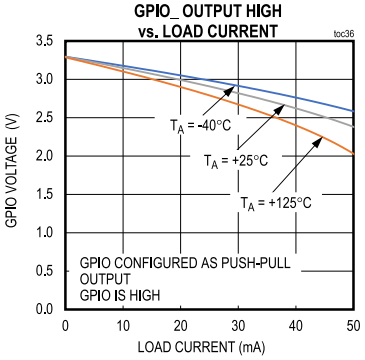


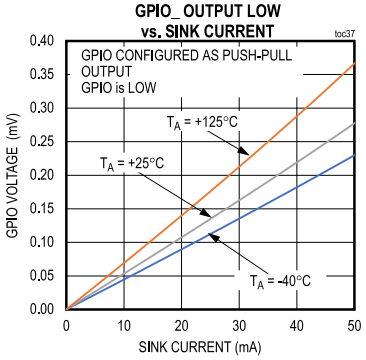




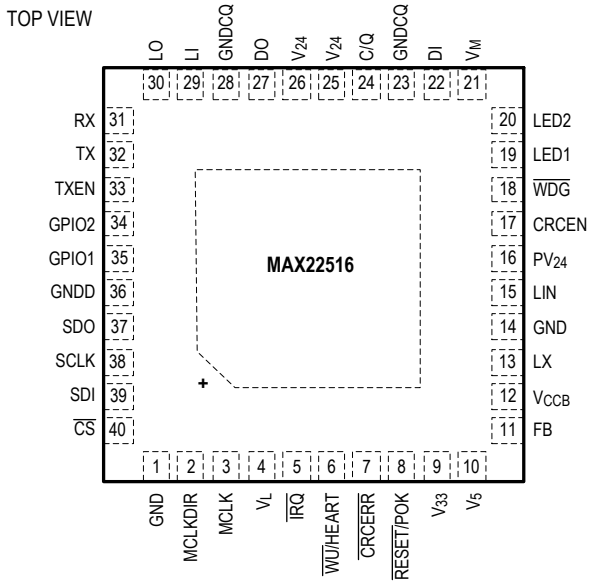


V_{24} = 24V, LIN = DC-DC output = 6V, V_L = V_{33}, T_A = 25°C, unless otherwise noted.

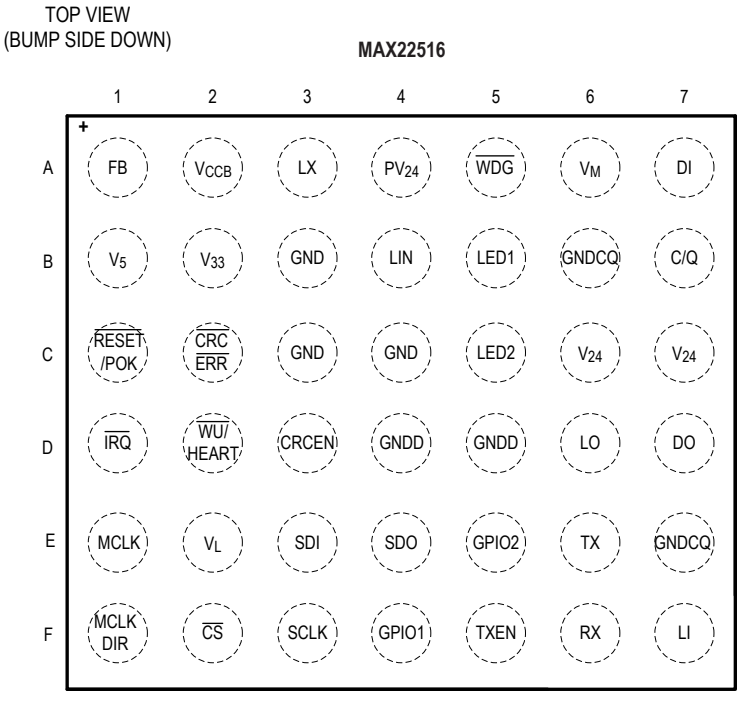




Pin Configurations



TQFN
5mm x 5mm



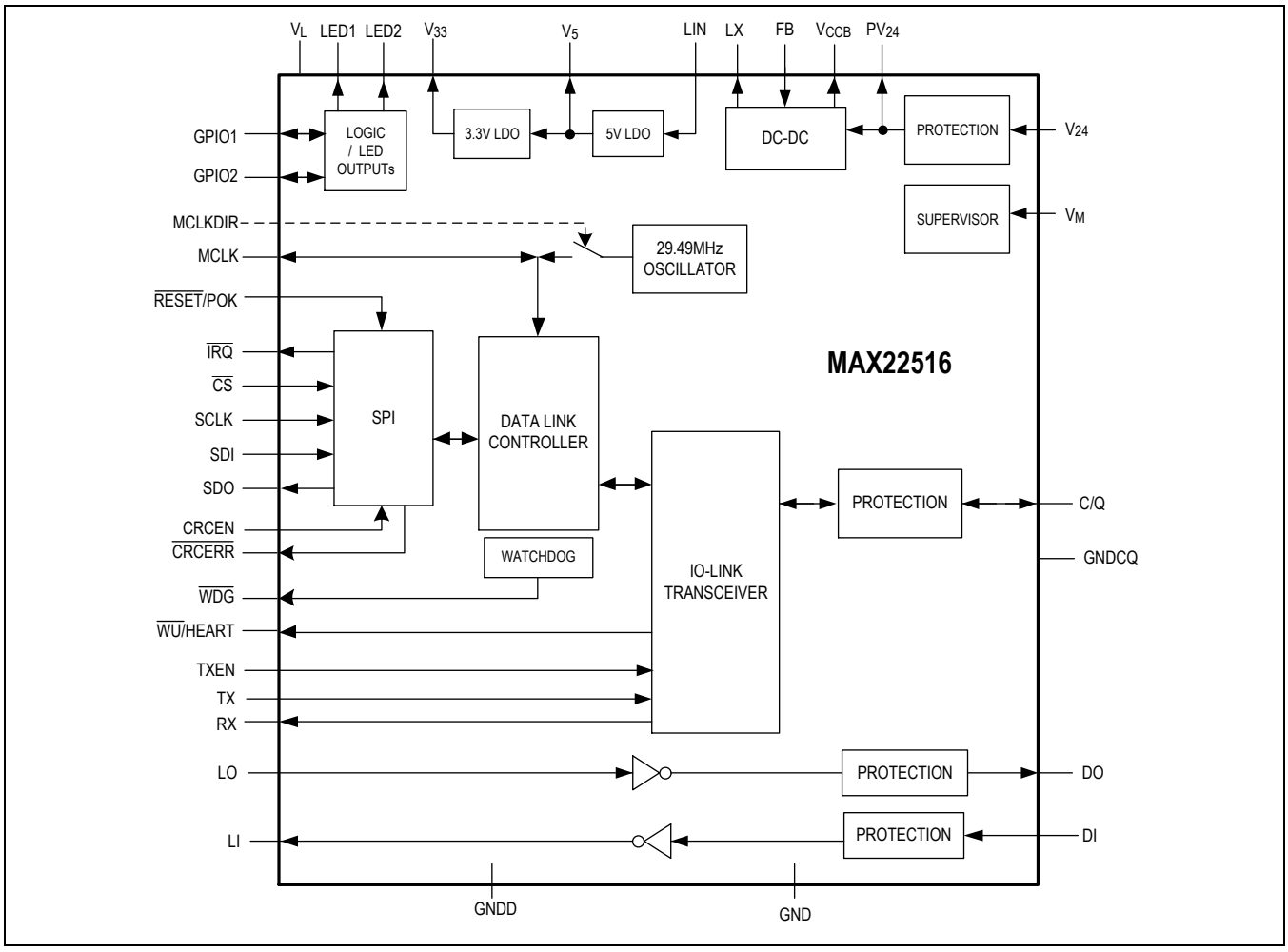
WLP
(3.53mm x 3.16mm)

Pin Descriptions

PIN		NAME	FUNCTION
TQFN	WLP		
POWER			
12	A2	V_{CCB}	Internal 5V Supply Regulator Output. Bypass V_{CCB} to GND with a 1µF capacitor as close to the device as possible. V_{CCB} can supply an external load up to 5mA.
16	A4	PV_{24}	Active Diode Output and DC-DC Input. Bypass PV_{24} with an external 1µF capacitor as close to the device as possible.
15	B4	LIN	5V Linear Regulator Input. Connect LIN to the output of the DC-DC circuit, to the PV_{24} supply, or to an external supply between 6V and 36V. Bypass LIN to GND with a 1µF capacitor. Connect LIN to V_5 to disable the 5V linear regulator.
10	B1	V_5	5V Linear Regulator Output/ Supply Input. V_5 is the output of the internal 5V linear regulator. Bypass V_5 to GND with a 1µF capacitor as close to the device as possible. To disable the 5V linear regulator, connect LIN to V_5. 5V is required on V_5 for normal operation. If the 5V regulator is disabled, apply an external 5V power supply to V_5.
25, 26	C6, C7	V_{24}	Supply Voltage Input. Connect all V_{24} pins together. Connect V_{24} to the L+ terminal of the IO-Link connector, or to an external supply. Bypass V_{24} to GND with a 10nF capacitor as close to the device as possible.
23, 28	B6, E7	GNDCQ	C/Q Driver IO-Link Ground. Connect GNDCQ to the L- terminal of the IO-Link connector and to GND. For more information, see the *Layout and Grounding* section.
4	E2	V_L	Logic IO Supply Input. Bypass V_L to GND with a 1µF capacitor as close to the device as possible. V_L sets the logic levels for all logic signals. Connect V_L to V_{33}, V_5, or to an external voltage between 2.5V and 5.5V.
1, 14	B3, C3, C4	GND	Ground. Connect GND to GNDCQ. All GND pins must be connected. For more information, see the *Layout and Grounding* section.
36	D4, D5	GNDD	Digital Ground. Connect GNDD to GND. All GND pins must be connected. For more information, see the *Layout and Grounding* section.
9	B2	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND with a 1µF capacitor as close to the device as possible. A bypass capacitor is not required for applications where V_{33} is disabled.
EP	-	EP	Exposed Pad. Connect EP to GND. For more information, see the Layout and Grounding section.
DC-DC REGULATOR			
13	A3	LX	Switching Output of the Integrated DC-DC Converter. Connect an inductor between LX and the output capacitor to generate a voltage with the DC-DC circuit. For more information, see the *Integrated DC-DC Regulator* section.
11	A1	FB	DC-DC Buck Regulator Feedback Input. Connect FB to the tap of a resistor divider between the output of the DC-DC and GND. For more information, see the *Integrated DC-DC Regulator* section. Connect FB to V_{CCB} if the DC-DC is not used.
24V I/O LINE INTERFACE			
24	B7	C/Q	C/Q IO-Link Transceiver Input/ Output. Drive TXEN high and set CQ_EN = 1 to enable the C/Q driver. The logic on C/Q is the logic inverse of the signal on TX and RX, by default.
27	D7	DO	DO Auxiliary Driver Output. Set DO_EN = 1 to enable the DO driver output. DO is the logic inverse of the LO input. DO is high impedance when DO_EN = 0.
22	A7	DI	Auxiliary Digital Input. LI is the logic inverse of the signal on the DI input. The DI receiver is always enabled. Connect a 1kΩ series resistor between the signal and DI pin.
AUXILIARY DI/DO LOGIC INTERFACE			
30	D6	LO	DO Driver Logic Input. DO is the logic inverse of the signal on LO when DO is enabled.

29	F7	LI	DI Receiver Logic Output. LI is the logic inverse of the signal on the DI input. LI is always enabled.
SPI INTERFACE			
37	E4	SDO	Serial Data Output. Connect SDO on the MAX22516 to the serial data input on the SPI host controller. SDO is high impedance when $\overline{CS}$ is high.
38	F3	SCLK	Serial Clock Input.
39	E3	SDI	Serial Data Input. Connect SDI on the MAX22516 to the serial data output on the SPI host controller.
40	F2	$\overline{CS}$	SPI Chip-Select Input. Drive $\overline{CS}$ low to start a read/write cycle. The cycle ends when $\overline{CS}$ is driven high.
17	D3	CRCEN	CRC Enable for SPI interface. Connect CRCEN to V_L to enable the CRC for the SPI interface.
7	C2	$\overline{CRCERR}$	Open-Drain SPI CRC Error Output. $\overline{CRCERR}$ asserts low when a CRC error has been detected in the last SPI communication.
VOLTAGE MONITOR			
21	A6	V_M	Voltage Monitor Input. Connect a resistor divider between the monitored supply voltage (for example, PV_{24}) and GND to define the power-OK threshold for the monitored voltage. For more information, see the *Voltage Monitor Input* section.
INTERRUPTS AND INDICATORS			
5	D1	$\overline{IRQ}$	Active-Low Open-Drain Interrupt Request Output. $\overline{IRQ}$ asserts low when a bit is set in the IOLInt, DEVInt, and/or ISDUInt registers, if enabled.
6	D2	$\overline{WU}$/HEART	Open-Drain IO-Link Wake-Up Request/Heart Output. Set the HEART_WU bit in the MISC_CTRL register to program the functionality for the $\overline{WU}$/HEART pin.
8	C1	$\overline{RESET}$/POK	Open-Drain Dual Function Active-Low Reset Input and Power-OK (POK) Output. Drive $\overline{RESET}$/POK low to set the MAX22516 in reset mode. The MAX22516 asserts $\overline{RESET}$/POK low when any of the V_{24}, V_5, or DC-DC output voltages are below their respective undervoltage lockout (UVLO) thresholds. Connect $\overline{RESET}$/POK to V_{CCB} or V_L with a 10kΩ (typ) resistor for normal operation. For more information, see the *Reset Input/ Power OK Output ($\overline{RESET}$/POK)* section.
18	A5	$\overline{WDG}$	Open-Drain Watchdog Timeout Output. $\overline{WDG}$ asserts low when the watchdog timer counter limit is reached.
IO-LINK UART INTERFACE			
31	F6	RX	C/Q Receiver Logic Output. By default, RX is the logic inverse of C/Q.
33	F5	TXEN	C/Q Driver Enable Logic Input.
32	E6	TX	C/Q Driver Logic Input.
CLOCK INPUT/OUTPUT			
2	F1	MCLKDIR	MCLK Input/Output Direction Select. Drive MCLKDIR high to use the internal oscillator for the UART and MCLK as clock source. Drive MCLKDIR low to disable the internal clock. Connect an external clock to the MCLK pin for UART communication when MCLKDIR is low.
3	E1	MCLK	Microcontroller Clock Input/Output. Drive MCLKDIR high to use MCLK as a clock source. Drive MCLKDIR low to use MCLK as a clock input pin. Connect an external clock source to MCLK when MCLKDIR is low.
GENERAL PURPOSE I/Os AND LED OUTPUTS			
35	F4	GPIO1	General Purpose Logic Input/Output 1. Configure and control GPIO1 with the GPIO1CTRL register.
34	E5	GPIO2	General Purpose Logic Input/Output 2. Configure and control GPIO2 with the GPIO2CTRL register.
19	B5	LED1	Open-Drain LED Output 1. Set the LED1 output on/off with the LED1CTRMSB and LED1CTR LSB registers.
20	C5	LED2	Open-Drain LED Output 2. Set the LED2 output on/off with the LED2CTRMSB and LED2CTR LSB registers.

Functional Diagram



Detailed Description

The MAX22516 IO-Link data link controller integrates a 24V C/Q transceiver, an auxiliary digital input and output, an integrated DC-DC, 5V and 3.3V linear regulators, and a full-feature IO-Link data link controller.

Once configured, the MAX22516 data link controller operates the IO-Link transceiver and requires no intervention from the external microcontroller during normal operation. Alternatively, the IO-Link transceiver can be controlled using the UART interface (TXEN, TX, and RX) directly, or through the SPI interface. The data link controller supports and includes, receive and transmit buffers for IO-link communication. Buffers for maximum size process data, ISDU, event, and page data reduce the need for time-critical microcontroller intervention, which allows the microcontroller to focus on the application layer tasks.

24V Interface I/O (V_{24}, C/Q, DO, DI, and GNDCQ)

The MAX22516 features an IO-Link transceiver interface capable of operating with DC voltages up to 36V. This 24V industrial standard interface includes the C/Q communication line, the auxiliary digital input (DI) and output (DO), the V_{24} supply, and ground.

C/Q and DO Drivers

The C/Q and DO switching drivers are programmable for PNP, NPN, or push-pull operation. Each driver features an independently programmable current limit, slew rate, and pull-up/pull-down currents.

C/Q operates over all of the COM1, COM2, and COM3 IO-Link data rates.

When using the data link layer, the UART pins (TXEN, TX, and RX) do not need to be controller or monitored. For applications that require UART pin control, the C/Q driver can be enabled and operated with the TXEN and TX pins, or through the SPI interface. Ensure that CQDrvSel = 0 in the TX_CTRL register to control the C/Q output with the TXEN and TX pins. In pin mode, drive TXEN high and set CQ_EN = 1 in the CQ_CTRL1 register to enable the C/Q driver. C/Q is the logic inverse of the TX input and RX output by default. Set the CQ_INV = 1 in the CQ_CTRL1 register to align the TX, C/Q, and RX logic states.

Set CQDrvSel = 1 in the TX_CTRL register to control the C/Q output with the CQTx and CQTxEn bits. C/Q is the logic inverse of the CQTx bit by default, and RX is the same logic as the CQTx bit. Set the CQ_INV = 1 in the CQ_CTRL1 register to align the CQTx, C/Q, and RX logic states.

The CQ_EN bit in the CQ_CTRL1 register must be set to enable the C/Q output for either CQDrvSel = 0 or 1. For more information, see *Table 1.*

Table 1. C/Q Driver Control

CQ_EN BIT	CQDrvSel BIT	TXEN PIN	TX PIN	CQTxEn BIT	CQTx BIT	CQ_INV BIT	C/Q DRIVER		
							NPN MODE	PNP MODE	PP MODE
0	X	X	X	X	X	X	C/Q driver disabled, C/Q receiver enabled		
1	0	L	X	X	X	X	Z	Z	Z
		H	L	X	X	0	Z	H	H
				X	X	1	L	Z	L
			H	X	X	0	L	Z	L
				X	X	1	Z	H	H
	1	X	X	0	X	X	Z	Z	Z
		X	X	1	0	0	Z	H	H
		X	X			1	L	Z	L
		X	X		1	0	L	Z	L
		X	X			1	Z	H	H

X = Do not care, Z = High Impedance

The DO driver can be operated with the LO pin or through the SPI interface. Ensure that DODrvSel = 0 in the TX_CTRL register to control the DO output with the LO pin. In pin mode, set DO_EN = 1 in the DO_CTRL1 register to enable the DO driver. DO is the logic inverse of the LO input by default. Set the DO_INV = 1 in the DO_CTRL1 register to align the LO and DO logic states.

Set DODrvSel = 1 in the TX_CTRL register to control the DO output with the DOTx bit. DO is the logic inverse of the DOTx bit, by default. Set the DO_INV = 1 in the DO_CTRL1 register to align the DOTx and DO logic states.

The DO_EN bit in the DO_CTRL1 register must be set to enable the DO output for either DODrvSel = 0 or 1. For more information, see *Table 2*.

Table 2. DO Driver Control

DO_EN BIT	DODrvSel BIT	LO PIN	DOTx BIT	DO_INV BIT	DO DRIVER		
					NPN MODE	PNP MODE	PP MODE
0	X	X	X	X	DO driver disabled		
1	0	L	X	0	Z	H	H
			X	1	L	Z	L
		H	X	0	L	Z	L
			X	1	Z	H	H
	1	X	0	0	Z	H	H
				1	L	Z	L
		X	1	0	L	Z	L
				1	Z	H	H

X = Do not care, Z = High Impedance

The DO output can be configured to track, or follow, the C/Q output. Set the CQDOPar bit in the TX_CTRL register to enable the DO output to track C/Q. Set CQDOPar = 1 and DO_AV = 1 so that DO tracks C/Q with inverted logic. DO_AV is ignored when CQDOPar = 0.

Driver Current Limit

The C/Q and DO drivers feature independently programmable current limits using the CQ_CTRL2 register and DO_CTRL2 register, respectively. Driver current-limit thresholds can be set to 50mA (min), 100mA (min), 200mA (min), and 250mA (min). When the load attempts to draw more current than the current-limit threshold setting, the affected driver actively limits the load current to the threshold level.

Set the C/Q current limit by setting the CQ_CL bits[1:0] in the CQ_CTRL2 register.

Set the DO current limit by setting the DO_CL[1:0] bits in the DO_CTRL2 register.

Driver Continuous Current Limit with Blanking Time

Large inrush currents are common for large capacitive loads and incandescent lamps and can trigger faults. The programmable current-limit blanking time on the C/Q and DO drivers allows for improved fault and thermal management while driving a large capacitive load or turning on an incandescent lamp.

When the driver current exceeds the programmed current-limit threshold for longer than the programmed blanking time, the associated driver fault bit is set. When an overcurrent event occurs on C/Q, the CQFltInt bit in the DEVInt register is set. When an overcurrent event occurs on DO, the DOFltInt in the IOLInt register is set. When the interrupt is enabled, (CQFltIntEn = 1 in the DEVIntEn register, and/or DOFltIntEn = 1 in the IOLIntEn register), the $\overline{IRQ}$ output also asserts.

The blanking time for the C/Q and DO drivers can be independently programmed. Select the C/Q driver blanking time by setting the CQ_CLBL[1:0] bits in the CQ_CTRL2 register. Select the DO driver blanking time by setting the DO_CLBL[1:0] bits in the DO_CTRL2 register. Programmable blanking time options are 128µs (typ), 500µs (typ), 1ms (typ), or 5ms (typ). If autoretry is enabled for the affected driver (CQ_AutoRtryEn = 1 in the CQ_CTRL2 register and/or DO_AutoRtryEn = 1 in the DO_CTRL2 register), the driver is disabled following the programmed blanking time.

If autoretry is not enabled (CQ_AutoRtryEn = 0 in the CQ_CTRL2 register and/or DO_AutoRtryEn = 0 in the DO_CTRL2 register), the driver is not disabled after the blanking time. When autoretry is not enabled, the associated driver fault bit (CQFltInt bit in the DEVInt register, and/or DOFltInt in the IOLInt register) is set when the overcurrent condition begins and the driver continues to operate until either the fault condition is removed, or the driver enters thermal shutdown.

Driver Autoretry

The MAX22516 features an autoretry function on the C/Q and DO drivers that allows for improved thermal management during overload conditions or events.

Autoretry functionality can be independently set and configured for the C/Q and DO drivers. Set the CQ_AutoRtyEn = 1 in the CQ_CTRL2 register to enable autoretry functionality for the C/Q driver. Set the DO_AutoRtyEn = 1 in the DO_CTRL2 register to enable autoretry functionality for the DO driver.

When autoretry is enabled, the MAX22516 disables the driver after the current-limit threshold has been exceeded for the selected blanking time. The driver is disabled for the programmed fixed off-time and is then automatically reenabled. If the overcurrent condition persists, the driver remains on for the blanking time and is then re-disabled. This autoretry cycle continues until the overcurrent condition is removed.

Select the blanking time and fixed off-time for the C/Q driver by setting the CQ_CLBL[1:0] and CQ_AutoRtyTime[1:0], respectively, in the CQ_CTRL2 register. Select the blanking time and fixed-off time for the DO driver by setting the DO_CLBL[1:0] and DO_AutoRtyTime[1:0] bits, respectively, in the DO_CTRL2 register.

Driver Thermal Shutdown

The C/Q and DO drivers are monitored individually and can be turned off when the driver junction temperature exceeds the +175ºC (typ) driver thermal shutdown threshold. The associated driver fault bits (CQFltInt, DOFltInt) in the DEVInt and IOLInt registers are set when a driver enters thermal shutdown. If the interrupt is enabled (__FltIntEn = 1), $\overline{IRQ}$ is asserted after the programmed blanking time has elapsed. The driver is automatically re-enabled when the driver junction temperature falls at least 26ºC (typ).

Internal Pull-Up/Pull-Down Currents

The MAX22516 features two pull-up or pull-down currents that can be enabled/disabled on C/Q and DO: a 300µA weak current, and a 2mA (typ) current.

Configure and enable the current on C/Q by setting the CQ_PD and CQ_PU bits in the CQ_CTRL1 register and by setting the CQPUD2mA bit MISC_CTRL register.

Similarly, configure and enable the current on DO by setting the DO_PD and DO_PU bits in the DO_CTRL1 register and by setting the DOPUD2mA bit MISC_CTRL register. For more information, see *Table 3*.

Table 3. C/Q and DO Pull-Up/-Down Current Configuration

CQ_PU, DO_PU	CQ_PD, DO_PD	CQPUD2mA, DOPUD2mA	C/Q OUTPUT OR DO OUTPUT
0	0	0	No pull-up or pull-down current enabled.
0	1	0	300µA (typ) pull-down current enabled.
		1	2mA (typ) pull-down current enabled.
1	0	0	Weak 300µA (typ) pull-up current enabled.
		1	2mA (typ) pull-up current enabled.

C/Q Wake-up Detection

The IO-Link standard defines a wake-up condition as a combination of a current and a voltage event on the C/Q line when the driver is enabled in PNP or push-pull mode. A wake-up event occurs when an IO-Link master forces a level on the C/Q line that is opposite to the set level of the C/Q driver for 80µs (typ).

Set the WU_HEART = 0 bit in the MISC_CTRL register to assert the $\overline{WU}$/HEART output low for 200µs (typ) when a wake-up event is detected.

The WUInt bit in the IOLInt register is set when a valid wake-up has been detected. If enabled by setting WUIntEn = 1 in the IOLIntEn register, $\overline{IRQ}$ also asserts when WUInt is set.

Similar to the PNP and push-pull modes, the MAX22516 can also detect a wake-up when configured in NPN mode. In NPN mode, a wake-up pulse is detected when C/Q is shorted from low-to-high when the low-side switch is enabled (TX = high). When the low-side switch is disabled in NPN mode, ensure that C/Q is pulled-high and shorted from high-to-low to properly detect a wake-up pulse. The MAX22516 cannot detect a wake-up pulse in NPN mode when the low-side switch is disabled and C/Q is shorted from low-to-high during the wake-up pulse.

The MAX22516 automatically ignores false wake-up events that can sometimes occur as a consequence of driving large capacitive or lamp loads where the time constant of charging up is around 80µs.

C/Q and DI Receivers

Although the IO-Link standard defines device/sensor operation for a supply ranging between 18V to 30V, industrial sensors in the field commonly operate with supply voltages as low as 9V. The MAX22516 operates with a supply voltage between 8V and 36V. When the V_{24} supply voltage is above 18V, the C/Q and DI receivers support the standard IO-Link receiver thresholds. When V_{24} is less than 18V, the C/Q and DI receiver thresholds are scaled, which allows receiver functionality down to the lowest supply voltage.

The C/Q receiver can also be configured to detect TTL signal levels. Set the RXTTL bit in the RX_CTRL register to enable TTL thresholds on the C/Q receiver. By default, RXTTL is 0.

V_{CCB} Output

V_{CCB} is the output of an internal regulator powered by V_{24} or V_5. V_{CCB} is powered by V_{24} until the V_5 voltage exceeds 3V. V_{CCB} is powered by V_5 when the V_5 voltage exceeds 3V. As V_5 is rising, V_{CCB} may drop below 5V until V_5 reaches its steady state voltage.

Reset Input/ Power OK Output ($\overline{RESET}$/POK)

The $\overline{RESET}$/POK pin is a dual function open-drain logic input/output, functioning as a reset input and a power-OK (POK) output.

Drive $\overline{RESET}$/POK low to put the MAX22516 in reset mode. The C/Q driver is disabled and the registers are reset to their default state when $\overline{RESET}$/POK is driven low. SPI communication is not available while $\overline{RESET}$/POK is low. If the DC-DC is disabled in the registers (BuckDis = 1 in the MISCCfg register), the device deasserts $\overline{RESET}$/POK 4ms (typ) after $\overline{RESET}$/POK is released and all power supplies are valid. If the DC-DC is enabled but lightly loaded, the delay between power up and when $\overline{RESET}$/POK deassert can be up to 10ms (typ).

The MAX22516 asserts $\overline{RESET}$/POK low when the V_{24} or V_5 voltage falls below their respective UVLO thresholds, or when the DC-DC output voltage falls below 95% of the set voltage (typ). The C/Q driver is disabled and the registers are reset to their default state when $\overline{RESET}$/POK is low. The MAX22516 deasserts $\overline{RESET}$/POK 4ms (typ) after all power supplies are valid. Note that the SPI is not available when $\overline{RESET}$/POK is low.

Connect a pull-up resistor between $\overline{RESET}$/POK and V_L or V_{CCB} for normal operation. Connect $\overline{RESET}$/POK to the reset input of a microcontroller to use it as a reset signal.

Voltage Monitor Input (V_M)

The MAX22516 features a flexible voltage comparator. This comparator monitors the voltage at the V_M input. When the V_M input voltage is below the 900mV (typ) threshold, the VMInt bit in the DEVInt register is set. If enabled (VMErrIntEn = 1 in the DEVIntEn register), $\overline{IRQ}$ is asserted when VMErrInt is set. Note that the VMErrInt interrupt bit is not cleared when the DEVInt register is read while the V_M voltage is below the comparator threshold. This bit is cleared only if the V_M voltage exceeds the threshold voltage during the DEVInt register read.

V_M can be used to supervise the voltage on V_{24}, PV_{24}, or any other pin. Ensure that the absolute maximum ratings for V_M do not exceed during transient events for the voltage monitored.

To monitor the PV_{24}, for example, use a resistor divider between PV_{24}, V_M, and GND to set the minimum PV_{24} voltage threshold (*Figure 7*). Calculate the monitored voltage power-OK threshold (V_{POK}) as:

$$V_{OK} = V_{TH\_M} \times [(R_1 + R_2)/R_2]$$

Select the resistor values to ensure that V_M does not exceed the 5.5V maximum voltage.

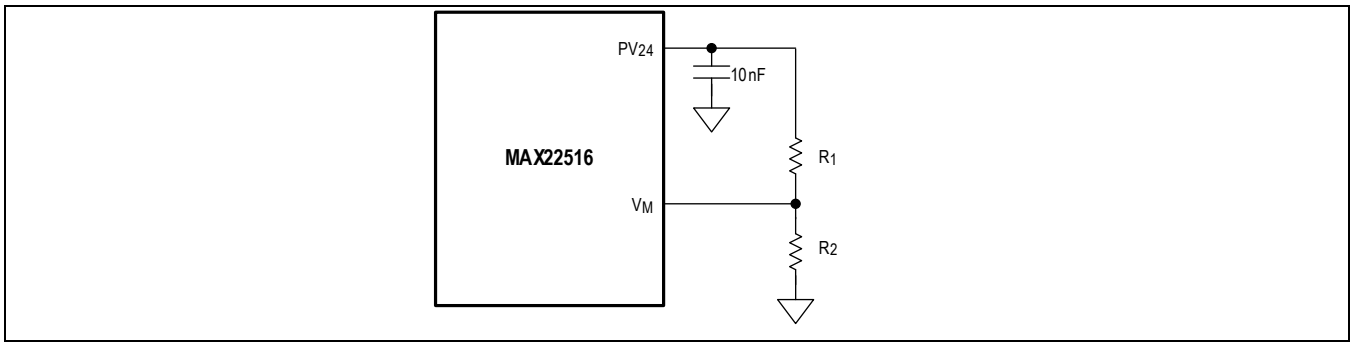


Figure 7. Monitored Voltage Input

Integrated DC-DC Regulator

Overview

The MAX22516 features an integrated high-efficiency synchronous DC-DC buck regulator with active diode reverse protection, current overload protection, soft-start, spread spectrum operation, and an adjustable output voltage. The DC-DC regulator operates with a fixed 1.229MHz (typ) frequency during normal operation. The regulator operates in pulse-width modulation mode (PWM), pulse frequency modulation (PFM) mode, or discontinuous conduction mode (DCM) during normal operation. Select the operating mode by setting the BuckDCM or BuckPFM mode bits in the MISCCfg register. The regulator is enabled by default but can be disabled through the serial interface. The DC-DC regulator is supplied from the PV_{24} voltage to protect against supply inversion. Bypass PV_{24} to GND with a 1µF capacitor to ensure proper operation for the DC-DC regulator.

Startup and Soft-Start

The MAX22516 DC-DC buck regulator features soft-start to slowly raise the output voltage when the device is powered up.

When the V_{24} voltage exceeds the 7.5V (typ) UVLO threshold, the DC-DC regulator is turned on, operating in DCM mode. DCM mode allows the DC-DC output to soft-start whether the output voltage is unpowered or pre-biased. Internal circuitry slowly ramps the output voltage to 95% of the set voltage within 2.2ms (typ) of the V_{24} voltage exceeding the UVLO threshold, ending the soft-start sequence.

Once soft-start has ended, the regulator switches from DCM mode to the selected mode for normal operation. By default, normal operation is PWM mode. Set the BuckPFM and/or the BuckDCM bits in the MISCCfg register to select another operating mode of the DC-DC regulator.

Maximum DC-DC Output Current

The MAX22516 integrated DC-DC buck regulator can drive loads up to 200mA (typ). The internal reverse-protection active diode between V_{24} and PV_{24} has a 300mA average current capability to supply the DC-DC input. Under certain conditions, the internal active diode between the V_{24} supply and PV_{24} may reduce the efficiency or reduce the maximum load current. If load currents are such that the current through the active diode exceeds 300mA, connect a Schottky diode between V_{24} and PV_{24} to bypass the internal active diode. When a Schottky diode is used, a transient voltage suppressor (TVS) or varistor on V_{24} may be necessary to survive hot-plug events.

Selecting the Mode of Operation

Pulse-Width Modulation (PWM)

A PWM DC-DC regulator switches at a fixed frequency, which adjusts the duty cycle of the pulses depending on the output power requirements. The maximum duty cycle on the DC-DC regulator is near 100%. Switching noise is easily filtered in PWM mode. The DC-DC regulator operates in PWM mode by default (BuckDCM = 0 and BuckPFM = 0 in the MISCCfg register).

Pulse Frequency Modulation (PFM)

In PFM mode, the DC-DC converter switches LX with a peak current set to be at least 200mA. LX stops switching when the output voltage exceeds 103% of set value and starts switching again when the DC-DC output voltage drops to 101% of the set value. Because the switching frequency changes in PFM mode, switching noise is more difficult to filtering,

typically resulting in a higher ripple on the output. PFM mode has the highest efficiency when driving low loads. Set BuckPFM = 1 and BuckDCM = 0 in the MISCCfg register to enable PFM mode on the DC-DC regulator.

Discontinuous Conduction Mode (DCM)

In DCM mode, the inductor current of the DC-DC regulator can reach zero for a short period during each switching cycle. In this mode, the output voltage is dependent on the input voltage, the inductance in the DC-DC regulator, the switching frequency, and the load. Use DCM mode for low output ripple and high efficiency under light load conditions. The MAX22516 DC-DC regulator operates in DCM mode during soft-start. Set BuckDCM = 1 in the MISCCfg register (in this case, the BuckPFM bit is ignored) to enable DCM functionality for normal operation.

Enabling/Disabling the DC-DC

The integrated DC-DC buck regulator on the MAX22516 is enabled by default, but can be disabled through the serial interface. Set the BuckDis bit in the MISCCfg register to disable the DC-DC. If the DC-DC regulator is not used, leave the LX unconnected and connect FB to V_{CCB}.

DC-DC Component Selection

Setting the Output Voltage

The output voltage of the DC-DC regulator can be programmed from 2.5V to 12V. Set the output voltage by connecting a resistor divider from the output to FB to GND (see *Figure 8*). Calculate the resistor values for the desired output voltage using the following equation:

$$R_H = R_L \times (V_{OUT}/0.9 - 1)$$

Ensure that R_H || R_L ≤ 66kΩ and use ±1% resistors for best accuracy.

The R_H resistor controls the load regulation on the load step and can also affect the value of the output capacitor to ensure stability of the DC-DC regulator.

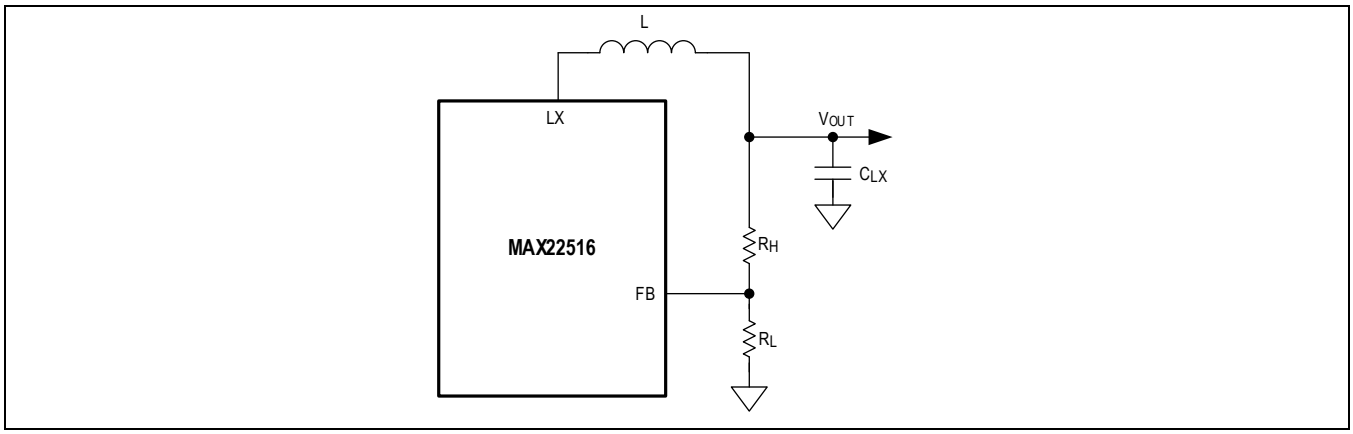


Figure 8. Setting the DC-DC Output Voltage

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough ensure that saturation cannot occur below the 440mA maximum current-limit value. Under lower load conditions, smaller inductors may be used.

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended to use with the MAX22516 DC-DC regulator. The output capacitor has the following two functions:

1. Filter the square wave generated by the device along with the output inductor.
2. Stabilize the device's internal control loop.

Capacitor selection depends on the operating conditions and the value of R_H and may affect the stability of the DC-DC regulator.

Typical External Components

Table 4 shows the recommended component values for the DC-DC buck regulator for a wide range of typical operating conditions (*Figure 8*). Recommended values in the table are designed for <±3% load regulation on a 50% load current step and with minimum inductance. A ±30% tolerance on inductance and a ±20% tolerance on capacitance is expected due to C-V dependence.

Table 4. Typical DC-DC Component Selection

V_{24} (V)		OUTPUT VOLTAGE (V)	MAX OUTPUT CURRENT (mA)	L [µH]	MIN C_{LX} OUTPUT CAPACITANCE [µF]	MAX C_{LX} OUTPUT CAPACITANCE [µF]	R_H [kΩ]	R_L [kΩ]
MIN	MAX							
8	36	3.3	200	15	4.7	27	226	84.5
8	36	5	200	22	3.3	17	348	75
8	36	6	200	27	3.3	14	412	73.2
9	36	7	190	33	2.7	12	499	73.2
10	36	8	190	33	2.2	11	562	71.5
10	36	9	170	33	1.8	9	634	69.8
12	36	10	180	39	1.8	8	698	69.8
12	36	11	160	39	1.5	8	768	68.1
14	36	12	180	39	1.2	7	845	68.1

DC-DC Spread Spectrum

The DC-DC regulator uses an internal clock synchronized with the main on-board oscillator that is used to generate other signals and timing. To reduce electromagnetic compatibility (EMC) emission peaks and/or reduce interference between the DC-DC switching circuitry and analog circuitry, the MAX22516 features a selectable spread-spectrum functionality for the DC-DC clock. When enabled, the DC-DC clock is randomly changed with a maximum frequency deviation of ±10% (typ). By default, DC-DC spread spectrum is disabled. Set the BuckSS bit in the MISCCfg register to enable spread spectrum for the DC-DC.

DC-DC Protection and Diagnostics

DC-DC Overcurrent and Runaway Protection

The DC-DC regulator includes integrated circuitry to protect the regulator during a current overload condition to avoid runaway. When the high-side current exceeds the 400mA (typ) high-side peak current limit (I_{DC_HSLIM}), the high-side switch is disabled.

Similarly, when the low-side current exceeds the 200mA (typ) low-side current-limit threshold (I_{DC_LSMAX}), the low-side switch is turned off and LX is floating until the next clock cycle, when switching begins again.

Hiccup Mode (Autoretry)

The DC-DC regulator features an autoretry sequence (hiccup mode) to protect against fault conditions on the output. After soft-start, if the output voltage of the DC-DC regulator falls below 92% of the set threshold, the regulator is disabled for 22ms (typ) and the BuckFault bit in the DEVStat register is set. Following the autoretry period, the DC-DC is restarted with soft-start.

If the fault on the output persists, the DC-DC is disabled and the autoretry sequence begins again. If the output voltage rises to 95% of the expected voltage, the DC-DC exits hiccup mode and operates normally.

DC-DC Power Diagnostics

The BuckFault and BuckOK bits in the DEVStat register indicate the state of the DC-DC output. Use these bits to monitor the regulator during operation.

The BuckOK bit is set when the output voltage is above 95% of the set voltage and the regulator is operating normally. When the DC-DC output voltage falls below 95% of the set voltage, $\overline{\text{RESET}}$/POK asserts and the BuckOK bit is set to 0.

The BuckFault bit is set when the regulator is in a fault condition. Fault conditions include the output voltage falling below 62% of the set threshold, current overload, and/or when the regulator is operating in hiccup mode. The BuckFault bit is cleared automatically when the regulator returns to normal operation.

Temperature Measurements

The MAX22516 monitors the die temperature during normal operation. This temperature can be read through the SPI interface and can be configured to generate a high temperature warning when the temperature rises above a set threshold. This threshold is user programmable.

The MAX22516 uses the same thermal sense circuitry to monitor the die temperature for the default thermal warning and when the programmable thermal warning methods are used. The default thermal warning system features a reduced precision, but faster response times. The programmable thermal ADC features a higher precision but slower functionality.

The high temperature warning can be disabled completely by setting the ADCCfg[1:0] bits in the ThADCCfg register.

High Temperature Warning

To protect against thermal damage, the IC monitors the die temperature during operation. The MAX22516 compares the die temperature to two different thresholds: the warning and the thermal shutdown threshold. By default, the high temperature warning threshold is +135°C.

Programmable Thermal Warning

Enable the programmable thermal warning threshold by setting the ADCCfg[1:0] bits in the ThADCCfg register to 01. Program the warning threshold by setting the ThWarn[5:0] bits in the ThADCThd register. The ThWarn[5:0] bits are binary-coded, with 1 LSB = 3°C and ThWarn = 00 000 at -15°C (typ). For more information, see *Table 5*.

Table 5. Thermal ADC Conversion

DIE TEMPERATURE (°C)	ThWarn[5:0]
0	00 0101 (5d)
27	00 1110 (14d)
84	10 0001 (33d)
126	10 1111 (47d)

The ThWInt bit in the DEVInt register and the ThW bit in the DEVStat2 register are set when the die temperature exceeds the thermal warning threshold. If enabled (ThWIntEn = 1 in the DEVIntEn register), $\overline{IRQ}$ asserts when the ThWInt bit is set. ThWInt is cleared when the DEVInt register is read, but ThW is not cleared until the temperature falls below the thermal warning threshold hysteresis. No hysteresis is available for the programmable warning threshold mode.

Thermal ADC

Set the ADCCfg[1:0] bits in the ThADCCfg register to 10 or 11 to enable ADC thermal monitoring to allow the die temperature to be read over the SPI interface.

Set the ADCStart bit in the ThADCCfg register to start the thermal ADC measurement. The ADCStart bit is cleared and the ADCEOC bit in the ThADCRes register is set after the manual ADC thermal measurement is completed after 450µs (typ). Measurement results are stored in the ThVal[5:0] bits in the ThADCRes register. Measurements are binary-coded, 1 LSB = 3°C (typ) and THVAL = 0 at -15°C (typ). Thermal ADC measurements range from -15°C to 174°C. For more information, see *Table 5*.

Thermal warning functionality is disabled when manual ADC thermal monitoring is enabled. Ignore the ThW bit in the DEVStat2 register and disable the thermal warning interrupt (ThWIntEn = 0 in the DEVIntEn register).

Protection

Reverse Polarity Protection

The MAX22516 is internally protected against reverse polarity miswiring on the V_{24}, C/Q, DO, DI, and GNDCQ pins. Any combination of these pins can be connected to a DC voltage in the range of -36V to +36V. Shorts to these voltages result in a current flow of less than 500µA. Note that the maximum voltage between any pins may not exceed the absolute maximum ratings.

Thermal Shutdown

The MAX22516 enters thermal shutdown when the average die temperature exceeds the +175°C (typ) thermal shutdown threshold. The C/Q and DO drivers, the DC-DC regulator, and the V_5 and V_{33} regulators are disabled when the device is in thermal shutdown. All registers are reset, and the SPI interface is not available when the device enters thermal shutdown.

The MAX22516 exits thermal shutdown when the average die temperature falls below the 20°C (typ) thermal shutdown hysteresis.

Thermal shutdown is present regardless of the method of high temperature warning utilized and cannot be disabled.

SPI Controller Interface

The MAX22516 supports full-duplex SPI communication at speeds up to 15MHz, which includes single-byte read and write, and burst read and write operations. The master must generate clock and data signals in SPI MODE0 (clock polarity CPOL = 0 and clock phase CPHzHHHz0) to communicate with the MAX22516. The SPI interface is not available when V_5 falls below 4.25V or when V_L is below 2.5V.

Figure 9 shows a single-cycle SPI write command and *Figure 10* shows a single-cycle SPI read command.

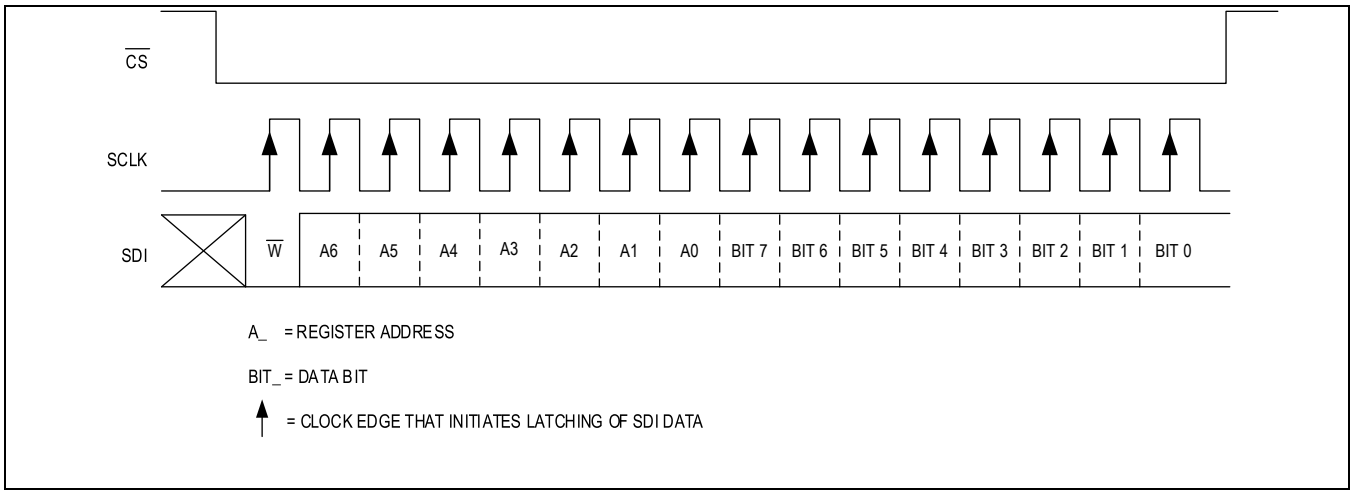


Figure 9. SPI Write Byte

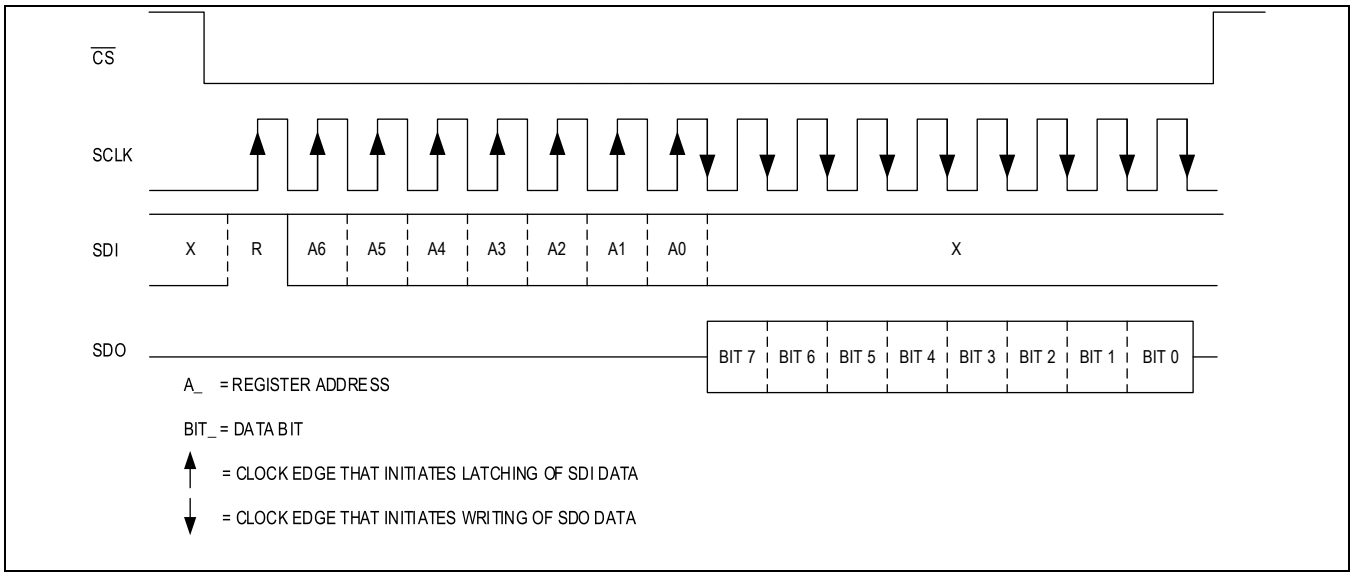


Figure 10. SPI Read Byte

SPI Burst Access

Burst access allows writing or reading in one block, by only defining the initial register address in the SPI command byte. Once the initial SPI address is received, the MAX22516 automatically increments the register after each SPI data byte. Drive $\overline{CS}$ low during the whole burst write or read cycle. The SPI clock must continue clocking throughout the burst access cycle. The burst cycle ends when the SPI master pulls $\overline{CS}$ high.

Note that do not use CRC error checking when using burst access.

SPI Cyclic Redundancy Check (CRC)

The MAX22516 supports a cyclic redundancy check (CRC) on SPI transactions to ensure data integrity across the SPI interface. Drive the CRCEN pin high or set the CRCEn bit in the IOLCfg register to enable CRC for the SPI interface.

The IC uses an 8-bit CRC frame check sequence (FCS) to check data integrity during transfers between the MAX22516 and the microcontroller. For write operations, the SPI master must append the CRC FCS byte as the last byte of communication. For read operations, the MAX22516 appends the CRC FCS data as the last byte of communication. CRC uses the following polynomial:

$$G(x) = x^8 + x^2 + x + 1$$

The CRC seed value is 0x52.

SPI Write to the MAX22516 with CRC Enabled

The external microcontroller must append the 8-bit CRC as the last byte of communication when CRC is enabled. The CRC frame check sequence (FCS) is calculated using the register address and data byte written to the MAX22516.

For example, assume a microcontroller sends a write command of 01h to register 21h. Data on the SDI line is as follows: [0x21] [0x01] [0xBC], where [0x21][0x01] is the write command to the register, with the data byte, and [0xBC] is the calculated 8-bit CRC.

When the write sequence has been completed, the MAX22516 verifies that the received bytes generate the expected CRC value. The write operation is considered as successful if the calculated CRC matches the value sent by the microcontroller, and the MAX22516 completes the received commands

If the CRC values do not match, however, the CRCErrInt bit in the DEVInt register is set, the $\overline{CRCERR}$ pin asserts low, and the write operation is ignored. If enabled (CRCErrIntEn in the DEVIntEn register is set), $\overline{IRQ}$ asserts when the CRCErrInt bit is set. The CRC fault is not cleared, and the $\overline{CRCERR}$ pin remains low, until a valid write command sequence is received.

SPI Read from the MAX22516 with CRC Enabled

When a read command is received, and CRC is enabled, the MAX22516 calculates and appends the 8-bit CRC to the end of the read data transmitted to the external microcontroller. The CRC checksum is calculated using the SPI command byte and the read data.

For example, assume that the microcontroller sends a command to read register 0x21, which has a data value of 0x01. Then the SPI data are:

SDI (from the microcontroller to MAX22516): [0xA1] [0x00] [0x00]

SDO (from MAX22516 to microcontroller): [zz] [0x01] [0x0A]

0xA1 is the read command of register 0x21, and 0x01 in the SDO stream is the read data from the register. 0x0A is the calculated 8-bit CRC using the read command (0xA1) and the read data (0x01).

IO-Link Communication

The MAX22516 integrates a fully functional IO-Link device data link layer as is required for IO-Link communication. Integrated state machines include an ISDU handler, a command handler, an event handler, process data handlers, an on-request data handler, a DL-mode handler, and a message handler. All integrated state machines are capable of handling cyclic and acyclic data transmission types, as outlined in the IO-Link standard.

SIO Mode

By default, the MAX22516 operates in SIO mode when powered up, or after a hardware or software reset. In SIO mode, the C/Q output is controlled by the UART interface pins: TXEN, TX, and RX, or by the TX_CTRL register bits: CQTxEn and CQTx. C/Q is configurable for NPN, PNP, or push-pull operation and features a programmable current limit and slew rate.

Once the MAX22516 is powered up and stabilized, the microcontroller should configure it by setting bits in the register map. When the MAX22516 registers are configured, set the ConfDone bit (in the IOLCfg register) to allow the device to proceed through the establish-communication sequence after a valid wake-up pulse is detected. The IC ignores incoming wake-up pulses and remains in SIO mode while the ConfDone bit is 0.

DL-Mode Handler

The DL-mode handler is responsible for detecting a wake-up request and for establishing communication. When a command is received from the IO-Link master, the integrated DL-mode handler synchronizes with the IO-Link master DL-mode handler states (STARTUP, PREOPERATE, and OPERATE) and manages other handlers as appropriate.

The DL-mode handler returns to the reset state, putting the device in SIO mode, after each power-up or reset.

Wake-Up and Establish COM

The wake-up sequence is the prerequisite for placing an IO-Link device in PREOPERATE and OPERATE modes. A wake-up condition is detected when the IO-Link master shorts the C/Q line to the opposite logic polarity for 80µs (typ).

The MAX22516 must be configured, and ready for communication, before a wake-up pulse is received by the IO-Link master. Configure the MAX22516 for establish-communication sequence by setting the IO-Link device communication rate to COM1, COM2, or COM3 by setting the COMx bits in the IOLCfg register. Set the required minimum cycle time for IO-Link communication by programming the PAGE1_BYTE02 register and configure other Direct Page 1 registers as needed. Enable the C/Q driver (CQ_EN = 1 and TXEN = high or CQTxEn = 1) to enable the driver output. Set the ConfDone bit in the IOLCfg register once all of the configuration settings have been programmed.

When a valid wake-up pulse is detected on the C/Q line, the MAX22516 sets the WUInt bit and, if enabled (WUIntEn in the IOLIntEn register is set), $\overline{IRQ}$ asserts. If configured for wake-up detection (WU_HEART = 0), the $\overline{WU}$/HEART pin also asserts low for 200µs (typ). After a valid wake-up pulse has been detected, configure the C/Q output for communication.

An integrated IO-Link establish-communication sequencer autonomously performs the IO-Link EstablishCom sequence after a valid wake-up pulse has been detected (*Figure 11*), if ConfDone = 1.

The DLMode bits in the IOLStat register indicate the current state of the DL-mode handler during the power-up and establish-communication sequence. When the DL-mode changes state, the DLModeInt bit in the IOLInt register is set. If enabled (DLModeIntEn in the IOLIntEn register is set), $\overline{IRQ}$ also asserts.

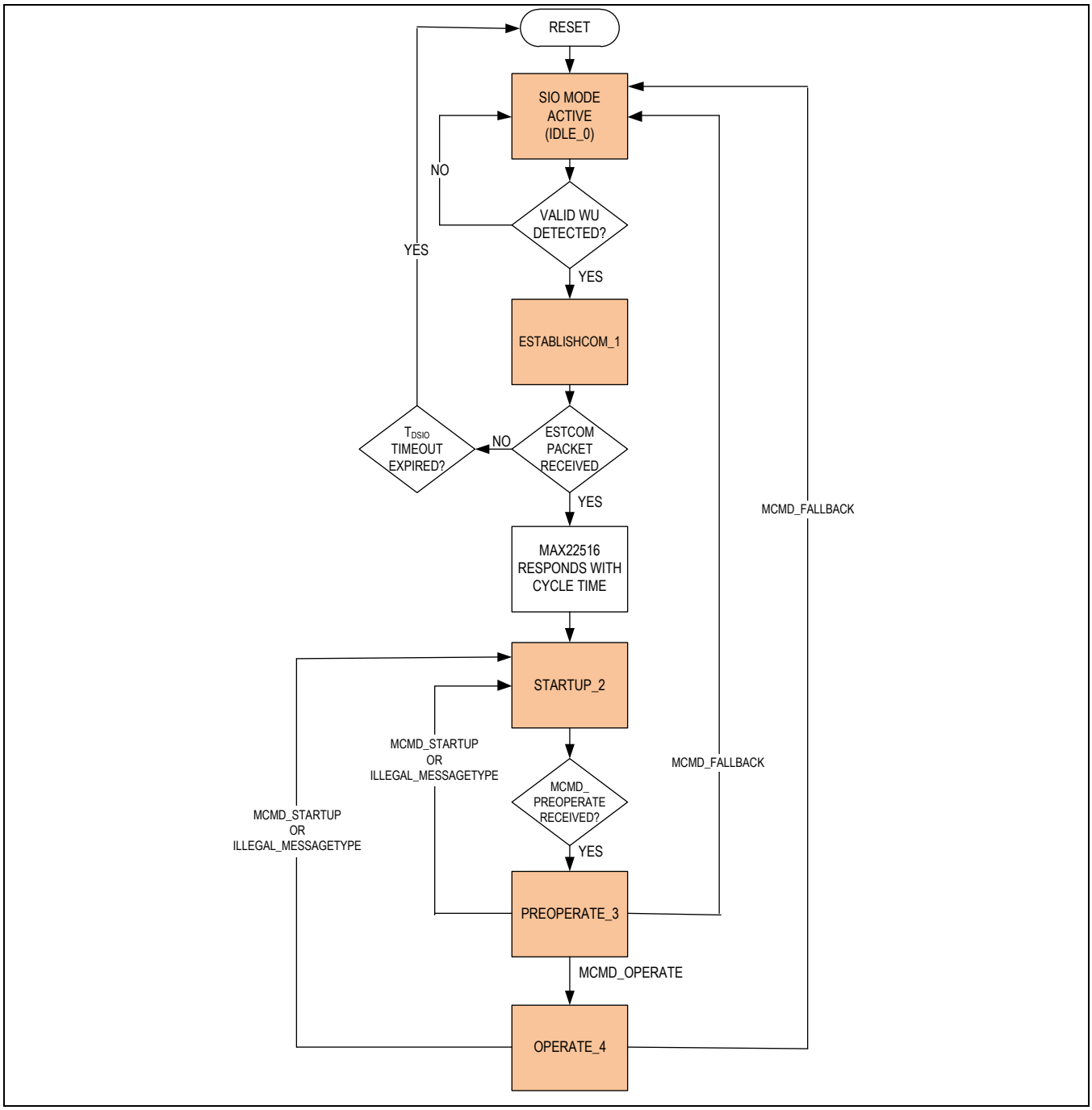


Figure 11. DL-Mode Handler Flowchart

Fallback Procedure

The MAX22516 returns to SIO mode within 420ms (typ) after receiving a fallback command from an IO-Link master.

It is also possible to reset the MAX22516 to SIO mode with the external microcontroller. Set the SIOForce bit in the IOLCfg register to force the device to return to SIO mode. There is no delay when switching to SIO mode once the SIOForce bit is set.

Process Data Transfers

Output Process Data (PDOut)

The MAX22516 autonomously handles the tasks supporting output Process Data (PDOut) from the IO-Link master to the PDOut buffer and features a process data architecture that supports up to 32-bytes of IO-Link PDOut.

The MAX22516 only receives the number of PDOut bytes declared in the MSequenceCapability and ProcessDataOut bytes in the PAGE1_BYTE02 and PAGE1_BYTE06 registers, respectively. If the IO-Link master transmits the wrong number of output process data bits, the data packet is ignored and the MAX22516 returns to the IO-Link STARTUP state. The microcontroller must read PDOut data with a single SPI burst read from the PDOUTFIFO register. Data read from the PDOUTFIFO register is always the latest received data.

Note that the MAX22516 cannot be used for partial output process data reads.

The PDOutDatRxInt bit in the IOLInt register is set after the MAX22516 has received new output process data. If enabled (PDOutDatRxIntEn = 1 in the IOLIntEn register), $\overline{IRQ}$ asserts when the PDOutDatRxInt bit is set.

Input Process Data (PDIn)

The MAX22516 handles all real-time tasks related to transmitting input Process Data (PDIn) to the IO-Link master and features a process data architecture that supports up to 32-bytes of IO-Link PDIn data.

The MAX22516 transmits the number of PDIn bytes declared in the MSequenceCapability and ProcessDataIn bytes in the PAGE1_BYTE03 and PAGE1_BYTE05 registers, respectively. Once loaded, the microcontroller must write the input process data bytes to the PDINFIFO register with a single SPI burst write. The MAX22516 automatically transmits data in the PDINFIFO to the IO-Link master in the next IO-Link cycle, which ensures minimal PDIn data delay to the IO-Link master. If not overwritten, data in the PDINFIFO is resent at the next IO-Link cycle.

Ensure that the PDStatus bit in the PDINDataRdy register is 0 once the PDIn data has been transferred to the PDINFIFO register. The MAX22516 transmits the data in the PDINFIFO to the IO-Link master when PDStatus = 0. When PDStatus = 1, the PD status bit in CKS/status byte of the process data packet is set and 0x00 is transmitted as the PDIn data.

ISDU Transfers

The MAX22516 handles the real-time tasks to support ISDU data transfer in both IN (that is, from the IO-Link device to the IO-Link master) and OUT (that is, from the IO-Link master to the device) directions. The MAX22516 integrates a 256-bytes ISDU buffer for both IN and OUT directions, allowing full-length ISDU transfers.

The MAX22516 detects that the ISDU data transmission is complete when the IO-Link master sends an ISDU idle command (IDLE), an ISDU abort command (ABORT), or a new ISDU request.

ISDU Receive

When the IO-Link master sends an ISDU request to the device, the MAX22516 decodes the length of the ISDU structure and verifies the ISDU checksum (CHKPDU). If the ISDU data is valid, the ISDUPckInt interrupt bit in the ISDUInt register is set.

If the received data is invalid (that is, the CHKPDU is incorrect), the ISDUPckInt interrupt bit is set, which indicates the received packet, but the CHKPDUErrInt error interrupt is also set. The invalid data is held in the ISDUOUTFIFO until the IO-Link master overwrites it. Clear the ISDUPckInt to allow ISDU communication to proceed.

The recommended ISDU receive sequence is as follows once the ISDUPckInt interrupt has been generated:

- Read the ISDUInt register to see if the CHKPDUErrInt bit is set.
- Clear the interrupt flags in the ISDUInt register.
- Read the ISDUOUTFIFO completely (burst access) or in chunks, as the microcontroller has time to process it. For more information on reading the ISDU FIFO in chunks, see the *Read/Write ISDUs in Multiple Chunks* section.

The MAX22516 autonomously responds to the IO-Link master with an ISDU busy message until the ISDU response is loaded into the ISDU out FIFO.

ISDU Transmit

The recommended ISDU transmit sequence is as follows:

- Write the ISDU into the ISDUINFIFO completely (burst access) or in chunks. For more information on writing the ISDU FIFO in chunks, see the *Read/Write ISDUs in Multiple Chunks* section.

- Set the ISDUINDataRdy bit in the ISDUDataRdy register to begin transmitting the ISDU event information to the IO-Link master.

Once transmission is complete, the MAX22516 sets the ISDUIdleInt bit in the ISDUInt register and the ISDUINFIFO register data is cleared.

Read/Write ISDUs in Multiple Chunks

Every SPI read command that the device microcontroller requests from the ISDUOUTFIFO register starts at the beginning of the received structure plus the value programmed in the ISDU_OFFSET register. For long ISDU communication, when the device is not able to read/write the entire ISDU in one cycle, it is recommended to read the ISDUOUTFIFO in multiple chunks – reading a limited number of bytes at a time. Read the required number of bytes and program the ISDUOFFSET register value to set the starting point for the next read. Repeat this cycle until the ISDU FIFO is completely read.

Similarly, for long ISDU write commands from the microcontroller, it is recommended to write to the ISDUINFIFO in multiple chunks, using the ISDUOFFSET register to set the starting point for each write. The process is the same as for an ISDU read.

Events

IO-Link device Events are transmitted using acyclic transfers and are reported using three levels of severity: notification, warning, and error, as outlined in the IO-Link standard.

The MAX22516 uses 4 bytes to compose an Event structure with details including the Status Code, the EventQualifier1, and the EventCode1 (MSB and LSB). For more information, see *Table 6*.

Table 6. Event Message Bytes

REGISTER ADDRESS	REGISTER NAME	DESCRIPTION
0x2C	STATUS_CODE	Summary of status and error information.
0x2D	EVENT_QUALIFIER	Event type, mode, and source.
0x2E	EVENT_CODE1MSB	16-bit EventCode of the Event.
0x2F	EVENT_CODE1LSB	

The microcontroller writes the Event information to the STATUS_CODE, EVENT_QUALIFIER, EVENT_CODE1MSB, and EVENT_CODEL1LSB registers and then sets the EventFlag bit in the EVENT_FLAG register to signal an event to the IO-Link master. Setting the EventFlag bit corresponds to the EventFlag bit in the IO-Link checksum/status (CKS) byte.

Once the microcontroller sets the EventFlag bit, data in the STATUS_CODE, EVENT_QUALIFIER, EVENT_CODE1MSB, and EVENT_CODE1LSB registers are locked until the current event has been processed by the IO-Link master. Because the Event Details bit is set, the IO-Link master reads the details of the Event indicated in the StatusCode from the event memory. The MAX22516 only supports one EventQualifier and EventCode at a time.

The IO-Link master writes to the StatusCode bits in the STATUS_CODE register to indicate the end of event processing. The MAX22516 autonomously handles the IO-Link handshake of an event. The EventFlag is automatically cleared and the ClrEvnFlgInt bit in the IOLInt register is set when the event processing is completed.

Note that the MAX22516 does not mask the event memory when EventFlag = 0. Similarly, the MAX22516 does not automatically clear the event memory when event processing is complete.

Watchdog IO-Link Cycle Counter

The MAX22516 features a configurable watchdog counter to monitor IO-Link activity and ensure that process data is updated regularly. *Table 7* shows the registers associated with the watchdog functionality.

Table 7. Watchdog Counter Registers

REGISTER ADDRESS	REGISTER NAME	DESCRIPTION
0x08	IOLInt	The WDInt bit is set when the watchdog counter reaches the maximum watchdog counter threshold.
0x09	IOLIntEn	Enable or mask watchdog interrupt bit (WDInt).
0x15	WDGTmr	This register stores the watchdog end-of-count value.
0x16	WDGClr	The WDClr bit configures the way that the watchdog counter is cleared.
0x2A	WDG_EVENT	This register holds the event code to be sent to the IO-Link master when configured to do so.
0x30	EVENT_FLAG	The WDGEvent bit can be used to configure the MAX22516 to send the data written in the WDGEvent register when the watchdog counter expires.

The watchdog counter can be configured for one of two modes of operation: standard watchdog or event watchdog modes.

In standard watchdog mode, set the watchdog counter limit by programming the counter limit (n) in the WDGTmr register. The watchdog counter is incremented after each transmission of the CKS byte. The watchdog output ($\overline{WDG}$) asserts low when the number of successful IO-Link transfers reaches the watchdog counter limit. The watchdog is reset to the watchdog value after a watchdog reset or a successful PDIN update (depending on WDClear bit in WDGClr register).

In standard watchdog mode, the MAX22516 falls back into SIO mode when the watchdog counter reaches the programmed limit. Additionally, $\overline{WDG}$ asserts low and the WDInt bit in the IOLInt register is set. If enabled (WDIntEn = 1 in the IOLIntEn register), $\overline{IRQ}$ asserts low. $\overline{WDG}$ and $\overline{IRQ}$, if enabled, are deasserted after writing 1 to the WDInt bit in the IOLInt register.

In event watchdog mode, set the watchdog counter limit by programming the counter threshold value (n) in the WDGTmr register. The watchdog counter is incremented after each transmission of the CKS byte. Program a byte into the WDG_EVENT register. Additionally, set the WDGEvent bit (WDGEvent = 1) in the EVENT_FLAG register. In this mode, data in the WDG_EVENT register is copied into the STATUS_CODE register, overwriting any data in that register, when the watchdog counter expires, and the EventFlag bit is set (EventFlag = 1). The MAX22516 notifies the IO-Link master of an Event and processes data in the STATUS_CODE register as a normal Event (for more information, see the *Events* section). Communication continues normally after the event is processed.

Ensure that the microcontroller updates the PDIn data and clears the watchdog counter before the watchdog counter limit is reached. The MAX22516 offers two methods of clearing the watchdog counter, as configured in the WDGClr register. Set the WDClear bit in the WDGClr register (WDClear = 1) to reset the watchdog counter when new PDIn data is loaded into the PDIn buffer. Clear the WDClear bit (WDClear = 0) to reset the watchdog counter after an SPI write into the WDGTmr register. When WDClear = 0, write any value to the WDGTmr register to clear it.

The watchdog counter is disabled by setting the WDGTmr register to 0x00. The watchdog counter is not active in SIO and EST_COM modes.

LEDs: Status and Diagnostic Indicators

The MAX22516 integrates two logic outputs for controlling LEDs (LED1 and LED2). These pins can be used as indicators of active SDCI communication and are controlled by setting bits in the LED1CTRMSB, LED1CTRLSB, LED2CTRMSB, and LED2CTRLSB registers.

Set the 16-bit LED control sequence for each LED by setting the bits in the corresponding LED_CTRMSB and LED_CTRLSB registers. The LED status (ON or OFF) is set according to the configuration in these registers. In sequence, a bit in the registers (MSB to LSB) is sampled every 63ms and the 16-bit pattern is repeated about every second. *Table 8* shows an example of an LED control sequence.

Write to both the LED_CTRMSB and LED_CTRLSB registers when setting the LED bits.

Table 8. LED1 Program Example

	LED1CTRMSB								LED1CTRLSB							
REGISTER BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
BIT LOGIC	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0
LED1 STATUS	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF

General Purpose I/Os (GPIO1, GPIO2)

The MAX22516 includes two integrated general purpose I/O pins, GPIO1 and GPIO2. GPIO1 and GPIO2 are independently configurable as inputs, outputs, or as process data (PDIn and PDOut) indicators. Configure GPIO1 using the GPIO1CTRL register and configure GPIO2 with the GPIO2CTRL register.

Integrated pull-up/-down resistors can be enabled for GPIO1 and GPIO2 when configured as inputs. By default, both GPIO1 and GPIO2 are configured as inputs with the internal pull-down enabled.

GPIO1 and GPIO2 can be configured as either open-drain or push-pull outputs. Individually set each GPIO output high or low by programming the GPIO_DOut bit in the associated GPIO control register. Integrated pull-up/-down settings are ignored when a GPIO is configured as an output.

GPIOs as Process Data Indicators (PDIn/PDOut)

Process data exchanges allow for regular cyclic transmission between a device and an IO-Link master. GPIO1 and GPIO2 can be configured to aid in this transfer.

Set GPIO1IO = 0 and GPIO1_TO_PDIN = 1 in the GPIO1CTRL register to configure GPIO1 as a PDIn bit. In this configuration, the status of GPIO1 is inserted into bit[0] of all of the PDIn bytes sent to the IO-Link master. The status of GPIO1 is sampled just before each PDIn byte is transmitted as shown in *Table 9* and *Table 10*.

Table 9. GPIO1 to PDIn Functionality (GPIO1IO = X, GPIO1_TO_PDIN = 0)

	GPIO1_TO_PDIN CONFIG BIT	PDIn[7:0]
BYTE 0	0	From buffer
BYTE 1		From buffer
BYTE 2		From buffer
…		…
BYTE n		From buffer

X = Do not care

Table 10. GPIO1 to PDIn Functionality (GPIO1IO = 0, GPIO1_TO_PDIN = 1)

	GPIO1_TO_PDIN CONFIG BIT	PDIn[7:1]	PDIn[0]
BYTE 0	1	0b0000000	GPIO1
BYTE 1		0b0000000	GPIO1
BYTE 2		0b0000000	GPIO1
…		…	
BYTE n		0b0000000	GPIO1

Similarly, GPIO2 can be configured to reflect the status of PDOut data received from the IO-Link master. When GPIO2IO = 1 and PDOUT_TO_GPIO2 = 1, GPIO2 is set high or low by bit 0 of the PDOut data received.

For more information, see *Table 11* and *Table 12*. When more than one PDOut byte is received from the IO-Link master, the status of GPIO2 is overwritten for every byte received.

All PDOut data bits are stored in the PDOUT buffer, regardless of the status of the PDOUT_TO_GPIO2 bit.

Table 11. PDOut to GPIO2 Functionality (GPIO2IO = X, PDOUT_TO_GPIO2 = 0)

	PDOUT_TO_GPIO2 CONFIG BIT	PDOut[7:0]	GPIO2
BYTE 0	0	To buffer	Configured and set in GPIO2CTRL register.
BYTE 1		To buffer	Configured and set in GPIO2CTRL register.
BYTE 2		To buffer	Configured and set in GPIO2CTRL register.
…		…	…
BYTE n		To buffer	Configured and set in GPIO2CTRL register.

X = Do not care

Table 12. PDOut to GPIO2 Functionality (GPIO2IO = 1, PDOUT_TO_GPIO2 = 1)

	PDOUT_TO_GPIO2 CONFIG BIT	PDOut Buffer	GPIO2
BYTE 0	1	PDOut[7:0]	PDOut[0]
BYTE 1		PDOut[7:0]	PDOut[0]
BYTE 2		PDOut[7:0]	PDOut[0]
…		…	
BYTE n		PDOut[7:0]	PDOut[0]

Register Map

MAX22516 REGISTER TABLE

ADDRESS	NAME	MSB							LSB
ID REGISTERS									
0x00	CHIP_ID[7:0]	CHIPID[7:0]							
0x01	REV_ID[7:0]	–	–	–	–	REVID[3:0]			
STATUS REGISTERS									
0x02	IOLStat[7:0]	–	–	–	–	–	DLMode[2:0]		
0x03	DEVStat1[7:0]	–	–	BuckFault	BuckOk	–	–	RXLvl	LILvl
0x04	DEVStat2[7:0]	–	ExtClkFail	DOFlt	CQFlt	V24Err	VMErr	ThW	–
0x05	ISDUStat[7:0]	–	–	–	–	–	–	–	ISDU_BAV
0x06	IOLErrCnt[7:0]	IOLinkErrCnt[7:0]							
0x07	FRMErrCnt[7:0]	FrmErrCnt[7:0]							
INTERRUPT REGISTERS									
0x08	IOLInt[7:0]	WDInt	DOFltInt	PDOutDatRxInt	ClrEvnFlgInt	WUInt	MCmdInt	DirPage1Int	DLModeInt
0x09	DEVInt[7:0]	CRCErrInt	FrmErrCntInt	IOLinkErrCntInt	CQFltInt	V24ErrInt	VMErrInt	ThWInt	–
0x0A	ISDUInt[7:0]	-	–	ISDU_BAVInt	CHKPDUErrInt	NewISDUWriteStartInt	ISDUAbrtInt	ISDUIdleInt	ISDUPckInt
INTERRUPT TO IRQ ENABLE									
0x0E	IOLIntEn[7:0]	WDIntEn	DOFltIntEn	PDOUTDatRxIntEn	ClrEvnFlgIntEn	WUIntEn	MCmdIntEn	DirPage1IntEn	DLModeIntEn
0x0F	DEVIntEn[7:0]	CRCErrIntEn	FrmErrCntIntEn	IOLinkErrCntIntEn	CQFltIntEn	V24ErrIntEn	VMErrIntEn	ThWIntEn	–
0x10	ISDUIntEn[7:0]	-	–	ISDU_BAVIntEn	CHKPDUErrIntEn	NewISDUWriteStartIntEn	ISDUAbrtIntEn	ISDUIdleIntEn	ISDUPckIntEn
CONFIGURATION REGISTERS									
0x14	IOLCfg[7:0]	DeviceAnsDelay[1:0]		ConfDone	CRCEn	COMx[1:0]		Page1Inh	SIOForce
0x15	WDGTmr[7:0]	Watchdog[7:0]							

ADDRESS	NAME	MSB							LSB
0x16	WDGClr[7:0]	–	–	–	–	–	–	–	WDClear
0x17	MISCCfg[7:0]	LDO33Dis	–	IOLDly[1:0]		BuckDCM	BuckPFM	BuckSS	BuckDis
0x18	CLKCfg[7:0]	EnClkTrim	ExtClk	–	–	ClkDiv[2:0]			MCLKDis
0x19	CLKTrim[7:0]	–	–	ClkTrim[5:0]					
DIRECT PAGE 1 REGISTERS									
0x1A	PAGE1_BYTE00[7:0]	MasterCommand[7:0]							
0x1B	PAGE1_BYTE01[7:0]	MasterCycleTime[7:0]							
0x1C	PAGE1_BYTE02[7:0]	MinCycleTime[7:0]							
0x1D	PAGE1_BYTE03[7:0]	MSequenceCapability[7:0]							
0x1E	PAGE1_BYTE04[7:0]	RevisionID[7:0]							
0x1F	PAGE1_BYTE05[7:0]	ProcessDataIn[7:0]							
0x20	PAGE1_BYTE06[7:0]	ProcessDataOut[7:0]							
0x21	PAGE1_BYTE07[7:0]	VendorID1[7:0]							
0x22	PAGE1_BYTE08[7:0]	VendorID2[7:0]							
0x23	PAGE1_BYTE09[7:0]	DeviceID1[7:0]							
0x24	PAGE1_BYTE0A[7:0]	DeviceID2[7:0]							
0x25	PAGE1_BYTE0B[7:0]	DeviceID3[7:0]							
0x26	PAGE1_BYTE0C[7:0]	FunctionID1[7:0]							

ADDRESS	NAME	MSB							LSB
0x27	PAGE1_BYTE0D[7:0]	FunctionID2[7:0]							
0x28	PAGE1_BYTE0E[7:0]	Page1Reserved1[7:0]							
0x29	PAGE1_BYTE0F[7:0]	Page1Reserved2[7:0]							
EVENT REGISTERS									
0x2A	WDGEvent[7:0]	WDGCode[7:0]							
0x2B	STATUS_CODE_DEF[7:0]	StatusCodeDefault[7:0]							
0x2C	STATUS_CODE[7:0]	StatusCode[7:0]							
0x2D	EVENT_QUALIFIER[7:0]	EventQualifier1[7:0]							
0x2E	EVENT_CODE1MSB[7:0]	EventCode1MSB[7:0]							
0x2F	EVENT_CODE1LSB[7:0]	EventCode1LSB[7:0]							
0x30	EVENT_FLAG[7:0]	–	–	–	–	–	–	WDGEvent	EventFlag
PROCESS DATA REGISTERS									
0x35	PDINFIFO[7:0]	PDINData[7:0]							
0x36	PDINDataRdy[7:0]	–	–	–	–	–	–	–	PDStatus
0x37	PDOUTFIFO[7:0]	PDOUTData[7:0]							
ISDU REGISTERS									
0x3F	ISDU_OFFSET[7:0]	ISDU_OFFSET[7:0]							
0x40	ISDUINFIFO[7:0]	ISDUINData[7:0]							
0x41	ISDUDataRdy[7:0]	–	–	–	–	–	–	–	ISDUINDataRdy
0x42	ISDUOUTFIFO[7:0]	ISDUOUTData[7:0]							

ADDRESS	NAME	MSB							LSB
0x43	ISDU_LEVEL[7:0]	ISDU_LEVEL[7:0]							
PIN CONFIGURATION REGISTERS									
0x50	LED1CTRMSB[7:0]	LED1CtrMsb[7:0]							
0x51	LED1CTRLSB[7:0]	LED1CtrLsb[7:0]							
0x52	LED2CTRMSB[7:0]	LED2CtrMsb[7:0]							
0x53	LED2CTRLSB[7:0]	LED2CtrLsb[7:0]							
0x54	GPIO1CTRL[7:0]	GPIO1Din	–	GPIO1_TO_PDIN	GPIO1OD	GPIO1Dout	GPIO1IO	GPIO1PUEn	GPIO1Res
0x55	GPIO2CTRL[7:0]	GPIO2Din	–	PDOUT_TO_GPIO2	GPIO2OD	GPIO2Dout	GPIO2IO	GPIO2PUEn	GPIO2Res
TRANSCEIVER CONTROL REGISTERS									
0x56	CQ_CTRL1[7:0]	CQ_SLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	CQ_INV	CQ_EN
0x57	CQ_CTRL2[7:0]	CQ_CL[1:0]		–	CQ_CLBL[1:0]		CQ_AutoRtyTime[1:0]		CQ_AutoRtyEn
0x58	DO_CTRL1[7:0]	DO_SLEW[1:0]		DO_PD	DO_PU	DO_NPN	DO_PP	DO_INV	DO_EN
0x59	DO_CTRL2[7:0]	DO_CL[1:0]		–	DO_CLBL[1:0]		DO_AutoRtyTime[1:0]		DO_AutoRtyEn
0x5A	TX_CTRL[7:0]	CQTx	CQTxEn	CQDrvSel	DOTx	DODrvSel	–	CQDOPar	DO_AV
0x5B	RX_CTRL[7:0]	–	RXTTL	RXDIS	RXFilter	–	–	–	DIFilter
0x5C	MISC_CTRL[7:0]	HEART_WU	–	–	–	–	–	CQPUD2mA	DOPUD2mA
THERMAL ADC CONTROLS									
0x5D	ThADCCfg[7:0]	ADCStart	–	–	–	–	–	ADCCfg[1:0]	
0x5E	ThADCThd[7:0]	–	–	ThWrn[5:0]					
0x5F	ThADCRes[7:0]	ADC_EOB	–	ThVal[5:0]					

Register Details

CHIP_ID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	CHIPID[7:0]							
Reset	0x16							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CHIPID	7:0	The ChipID register identifies the MAX22516 die type (RX46).

REV_ID (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REVID[3:0]			
Reset	–	–	–	–	0x02			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
REVID	3:0	The RevID bits identify the revision of the MAX22516.	0x0: N/A 0x1: Pass 1 0x2: Pass 2

IOLStat (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DLMode[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DLMode	2:0	Data Link Layer Mode of Operation These bits indicate the DL-Mode of communication.	000 = IDLE_0 001 = EstablishCom_1 010 = Startup_2 011 = PreOperate_3

BITFIELD	BITS	DESCRIPTION	DECODE
			100 = Operate_4 No other codes permitted.

DEVStat1 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BuckFault	BuckOk	–	–	RXLvl	LILvl
Reset	–	–			–	–	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BuckFault	5	DC-DC Fault Bit DC-DC fault conditions include output overcurrent/overload, the output voltage falls below 70% of the set voltage, and when the regulator is in hiccup mode.	0 = The DC-DC is operating normally. No fault conditions are present. 1 = A fault condition is present on the DC-DC regulator.
BuckOk	4	DC-DC Power-OK	0 = The DC-DC regulator is not ready or has a fault condition. 1 = The DC-DC regulator is operating normally in the steady state condition and is ready to be used.
RXLvl	1	RX Output Level Status Bit	0 = RX output is low. 1 = RX output is high. The logic level of the RX output is defined by the level of the C/Q pin, RXTTL bit, and the CQ_INV bit. RXLvl is always 0 when RXDis = 1.
LILvl	0	LI Output Level Status Bit	0 = LI output is low. 1 = LI output is high. The logic state of the LI output is defined by the state of the DI pin.

DEVStat2 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	ExtClkFail	DOFlt	CQFlt	V24Err	VMErr	ThW	–
Reset	–		0b0	0b0	0b0	0b0	0b0	–
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
ExtClkFail	6	External Clock Fail Bit This bit is set when the part MCLK is programmed as an input (MCLKDIR is low and ExtClk = 1) and there is no clock, or an incorrect clock frequency on the MCLK pin.	0 = No clock issues detected/internal clock used. 1 = Missing or incorrect clock at MCLK input.
DOFlt	5	DO Fault Status Bit	0 = No fault on DO driver. 1 = Overcurrent or thermal overload fault on DO driver.
CQFlt	4	C/Q Fault Status Bit	0 = No fault on C/Q driver. 1 = Overcurrent or thermal overload fault on C/Q driver.
V24Err	3	V_{24} Undervoltage Status Bit	0 = V_{24} is above the 7V (typ) rising undervoltage lockout (UVLO) threshold. 1 = V_{24} is below the 6V (typ) falling UVLO threshold.
VMErr	2	Monitored Input Status Bit	0 = V_M is above the 900mV (typ) threshold. 1 = V_M is below the 900mV (typ) threshold.
ThW	1	Thermal Warning Status Bit	0 = The die temperature is below the warning threshold temperature. 1 = The die temperature is above the warning threshold temperature.

ISDUStat (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ISDU_BAV
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ISDU_BAV	0	ISDU Buffer Activity Status Bit	0 = The ISDU buffer is not available to be over SPI. 1 = The ISDU buffer is available to be read.

IOLErrCnt (0x6)

BIT	7	6	5	4	3	2	1	0
Field	IOLinkErrCnt[7:0]							
Reset	0x00							

Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
IOLinkErrCnt	7:0	IO-Link Communication Error Counter The IOLinkErrCnt[7:0] bits increment every time an error occurs in the IO-Link communication. Possible causes of communication errors can include wrong check type octect (CKT) and wrong number of bytes from the IO-Link master. The MAX22516 can record up to 255 errors in this register before it is cleared. Clear the IOLinkErrCnt[7:0] bits by writing any value to the IOLErrCnt register.

FRMErrCnt (0x7)

BIT	7	6	5	4	3	2	1	0
Field	FrmErrCnt[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FrmErrCnt	7:0	IO-Link Communication Frame Parity Error Bit The FrmErrCnt[7:0] bits increment every time a frame parity error is detected in the IO-Link communications from the master. The MAX22516 can record up to 255 errors in this register before it is cleared. Clear the FrmErrCnt[7:0] bits by writing any value to the FRMErrCnt register.

IOLInt (0x8)

BIT	7	6	5	4	3	2	1	0
Field	WDInt	DOFltInt	PDOutDatRxInt	ClrEvnFlgInt	WUInt	MCmdInt	DirPage1Int	DLModeInt
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDInt	7	Watchdog Cycle Counter Interrupt The MAX22516 monitors the watchdog timeout and	0 = Watchdog time has not expired since bit was last cleared.

BITFIELD	BITS	DESCRIPTION	DECODE
		sets the WDInt bit when the timeout expires. Write a 1 to this bit to clear it.	1 = Watchdog timer has expired since bit was last cleared.
DOFltInt	6	DO Fault Interrupt DO fault conditions can include overcurrent/overload and/or driver thermal shutdown events. Write a 1 to this bit to clear it.	0 = No fault has occurred on DO fault since bit was last cleared. 1 = A fault has been detected on DO since the bit was last cleared.
PDOutDatRxInt	5	PDOUT Data Received Interrupt Write a 1 to this bit to clear it.	0 = No new PDOUT data has been received since this bit was last cleared. 1 = New PDOUT data has been received since this bit was last cleared.
ClrEvnFlgInt	4	Master Clears Event Flag Interrupt This bit is set when the IO-Link master writes to the StatusCode[7:0] bits in the STATUS_CODE register to complete the event processing. This clears the event flag. Write a 1 to this bit to clear it.	0 = No Event process has been completed since this bit was last cleared. 1 = Event process has been completed since this bit was last cleared.
WUInt	3	Valid Wake-up Detection Interrupt A valid wake-up pulse has been detected. Note that a valid wake-up pulse is detected only in Idle_0. Write a 1 to this bit to clear it.	0 = A valid wake-up pulse has not been detected since this bit was last cleared. 1 = A valid wake-up pulse has been detected since this bit was last cleared.
MCmdInt	2	Master Command Interrupt This bit is set every time a valid IO-Link master command (MC) is received, or the IO-Link master writes to Direct Page 1 byte 0x00. Write a 1 to this bit to clear it.	0 = No valid master command has been received since this bit was last cleared. 1 = A valid master command has been received since this bit was last cleared.
DirPage1Int	1	Direct Page 1 Content Changed by IO-Link Master Interrupt This bit is set whenever the IO-Link master changes anything writable in Direct Page 1 locations (1Ah - 29h). Write a 1 to this bit to clear it.	0 = Direct Page 1 content has not been changed by the master since this bit was last cleared. 1 = Direct Page 1 content has been changed By the master since this bit was last cleared.
DLModeInt	0	DL-Mode Interrupt Bit	0 = DLMODE[2:0] bits have changed since this bit was last cleared.

BITFIELD	BITS	DESCRIPTION	DECODE
		This bit is set when the DL-Mode status has been changed in the DLMode[2:0] bits. For more information, see the IOLStat register. Write a 1 to this bit to clear it.	1 = DLMODE[2:0] bits have changed since this bit was last cleared.

DEVInt (0x9)

BIT	7	6	5	4	3	2	1	0
Field	CRCErrInt	FrmErrCntInt	IOLinkErrCntInt	CQFltInt	V24ErrInt	VMErrInt	ThWInt	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRCErrInt	7	CRC Error Interrupt When CRC detection is enabled, the MAX22516 monitors SPI communication and calculates the CRC for each SPI communication. This bit indicates when a mismatch occurs between the received and computed CRC at the end of an SPI write cycle. Write a 1 to this bit to clear it.	0 = No CRC error detected. 1 = CRC error detected.
FrmErrCntInt	6	IO-Link/UART Frame Error Interrupt This bit indicated a parity or frame error is detected on IO-link line. The FrmErrCnt[7:0] in the FRMErrCnt register are incremented when an IO-Link/UART frame error occurs. Write a 1 to this bit to clear it.	0 = No IO-Link/UART frame error detected. 1 = IO-Link/UART frame error detected.
IOLinkErrCntInt	5	IO-Link Communication Error Interrupt This bit is set when an IO-Link communication error occurs. Possible causes of IO-Link communication errors include wrong CKT, an incorrect number of bytes, and any issue that might cause the MAX22516 to not send the CKS packet back to the IO-Link master. The IOLinkErrCnt[7:0] bits also increment every time an error occurs in the IO-Link communication.	0 = No IO-Link error detected. 1 = IO-Link error detected.

BITFIELD	BITS	DESCRIPTION	DECODE
		Write a 1 to this bit to clear it.	
CQFltInt	4	C/Q Fault Interrupt This bit is set when a fault occurs on C/Q. Fault conditions include an overcurrent fault and a driver thermal fault. Write a 1 to this bit to clear it.	0 = No C/Q fault detected. 1 = C/Q fault detected.
V24ErrInt	3	V_{24} Undervoltage Interrupt This bit is set when V_{24} falls below the UVLO threshold. Write a 1 to this bit to clear it.	0 = V_{24} has not fallen below the UVLO threshold. 1 = V_{24} has fallen below the UVLO threshold.
VMErrInt	2	Monitor Voltage, V_M, undervoltage Interrupt. This bit is set when the monitored voltage, V_M, falls below the threshold. Write a 1 to this bit to clear it.	0 = V_M has not fallen below the threshold. 1 = V_M has fallen below the threshold.
ThWInt	1	Thermal Warning Interrupt This bit is set when the die temperature rises above the thermal warning threshold. Write a 1 to this bit to clear it.	0 = The IC junction temperature has not exceeded the thermal warning threshold. 1 = The IC junction temperature has exceeded the thermal warning threshold.

ISDUInt (0xA)

BIT	7	6	5	4	3	2	1	0
Field	-	–	ISDU_BAVInt	CHKPDUErrInt	NewISDUWriteStartInt	ISDUAbrtInt	ISDUIdleInt	ISDUPckInt
Reset		–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	–	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
-	7	Reserved	
ISDU_BAVInt	5	ISDU Buffer Available Interrupt This bit is set when the ISDU buffer is available to	0 = ISDU buffer is not available to SPI interface. 1 = ISDU buffer is available to SPI interface.

BITFIELD	BITS	DESCRIPTION	DECODE
		be accessed by SPI. Write a 1 to this bit to clear it.	
CHKPDUErrInt	4	CHKPDU Error Interrupt This bit is set when the CHKPDU packet at the end of an ISDU out transfer is incorrect. Write a 1 to this bit to clear it.	0 = Correct CHKPDU received. 1 = Incorrect CHKPDU received.
NewISDUWriteStartInt	3	New ISDU Out Cycle Write Start Interrupt This bit is set when the IO-Link master sends a 0x70 command, triggering the beginning of a new ISDU transfer. Write a 1 to this bit to clear it.	0 = No new ISDU out cycle started. 1 = A new ISDU out cycle has started.
ISDUAbrtInt	2	ISDU ABORT Command Received Interrupt This bit is set when an ISDU abort (ABORT) command (0xFF) is received from the IO-Link master. Write a 1 to this bit to clear it.	0 = No ISDU abort command has been received. 1 = ISDU abort command has been received.
ISDUIdleInt	1	ISDU IDLE Command Received Interrupt This bit is set when a first ISDU IDLE IO-Link master command is received after a completed ISDU request. ISDU IDLE command is 0b1111 xxxx, excluding the cases where xxxx=0000 and xxxx=1111. Write a 1 to this bit to clear it.	0 = No ISDU IDLE command received. 1 = ISDU IDLE command received.
ISDUPckInt	0	ISDU Packet Received Interrupt. This bit is set when a complete ISDU packet has been received from the IO-Link master, regardless of whether the CHKPDU is correct or wrong. Before reading out the ISDU data, the controller must complete the following steps: 1) Clear this bit by writing a 1 to it. 2) Wait for the ISDU buffer to be available, by polling the ISDU_BAV status bit (ISDUStat[0]) or by waiting for the interrupt bit ISDu_BAVInt (ISDUInt[5]) to go high.	0 = No ISDU packet received. 1 = Complete ISDU packet received.

BITFIELD	BITS	DESCRIPTION	DECODE
		Write a 1 to this bit to clear it.	

IOLIntEn (0xE)

BIT	7	6	5	4	3	2	1	0
Field	WDIntEn	DOFltIntEn	PDOUTDatRxIntEn	ClrEvnFlgIntEn	WUIntEn	MCmdIntEn	DirPage1IntEn	DLModeIntEn
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDIntEn	7	Watchdog Cycle Counter Interrupt (WDInt) Enable Set this bit to assert the IRQ output when the WDInt bit is set (IOLInt[7] = 1).	0 = IRQ does not assert when WDInt = 1. 1 = IRQ asserts when WDInt = 1.
DOFltIntEn	6	DO Fault Interrupt (DOFltInt) Enable Set this bit to assert the IRQ output when the DOFltInt bit is set (IOLInt6] = 1).	0 = IRQ does not assert when DOFltInt = 1. 1 = IRQ asserts when DOFltInt = 1.
PDOUTDatRxIntEn	5	PDOUT Data Received Interrupt (PDOUTDatRxInt) Enable Set this bit to assert the IRQ output when the PDOUTDatRxInt bit is set (IOLInt[5] = 1).	0 = IRQ does not assert when PDOUTDatRxInt = 1. 1 = IRQ asserts when PDOUTDatRxInt = 1.
ClrEvnFlgIntEn	4	IO-Link Master Clears Event Flag Interrupt (ClrEvnFlgInt) Enable Set this bit to assert the IRQ output when the ClrEvnFlgInt bit is set (IOLInt[4] = 1).	0 = IRQ does not assert when ClrEvnFlgInt = 1. 1 = IRQ asserts when ClrEvnFlgInt = 1.
WUIntEn	3	Wake-Up Detection Interrupt (WUInt) Enable Set this bit to assert the IRQ output when the WUInt bit is set (IOLInt[3] = 1).	0 = IRQ does not assert when WUInt = 1. 1 = IRQ asserts when WUInt = 1.
MCmdIntEn	2	IO-Link Master Command Interrupt (MCmdInt) Enable Set this bit to assert the IRQ output when the MCmdInt bit is set (IOLInt[2] = 1).	0 = IRQ does not assert when MCmdInt = 1. 1 = IRQ asserts when MCmdInt = 1.
DirPage1IntEn	1	Direct Page 1 Content Changed by IO-Link Master Interrupt (DirPage1Int) Enable	0 = IRQ does not assert when DirPage1Int = 1. 1 = IRQ asserts when DirPage1Int = 1.

BITFIELD	BITS	DESCRIPTION	DECODE
		Set this bit to assert the IRQ output when the DirPage1Int bit is set (IOLInt[1] = 1).	
DLModeIntEn	0	DL-Mode Interrupt (DLModeInt) Enable Set this bit to assert the IRQ output when the DLModeInt bit is set (IOLInt[0] = 1).	0 = IRQ does not assert when DLModeInt = 1. 1 = IRQ asserts when DLModeInt = 1.

DEVIntEn (0xF)

BIT	7	6	5	4	3	2	1	0
Field	CRCErrIntEn	FrmErrCntIntEn	IOLinkErrCntIntEn	CQFltIntEn	V24ErrIntEn	VMErrIntEn	ThWIntEn	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRCErrIntEn	7	CRC Error Interrupt (CRCErrInt) Enable Set this bit to assert the IRQ output when the CRCErrInt bit is set (DEVInt[7] = 1).	0 = IRQ does not assert when CRCErrInt = 1. 1 = IRQ asserts when CRCErrInt = 1.
FrmErrCntIntEn	6	IO-Link/UART Frame Error Interrupt (FrmErrCntInt) Enable Set this bit to assert the IRQ output when the FrmErrCntInt bit is set (DEVInt[6] = 1).	0 = IRQ does not assert when FrmErrCntInt = 1. 1 = IRQ asserts when FrmErrCntInt = 1.
IOLinkErrCntIntEn	5	IO-Link Communication Error Interrupt (IOLinkErrCntInt) Enable Set this bit to assert the IRQ output when the IOLinkErrCntInt bit is set (DEVInt[5] = 1).	0 = IRQ does not assert when IOLinkErrCntInt = 1. 1 = IRQ asserts when IOLinkErrCntInt = 1.
CQFltIntEn	4	C/Q Fault Interrupt (CQFltInt) Enable Set this bit to assert the IRQ output when the CQFltInt bit is set (DEVInt[4] = 1).	0 = IRQ does not assert when CQFltInt = 1. 1 = IRQ asserts when CQFltInt = 1.
V24ErrIntEn	3	V_{24} Undervoltage Interrupt (V24ErrInt) Enable Set this bit to assert the IRQ output when the V24ErrInt bit is set (DEVInt[3] = 1).	0 = IRQ does not assert when V24ErrInt = 1. 1 = IRQ asserts when V24ErrInt = 1.
VMErrIntEn	2	VM Error Interrupt (VMErrInt) Enable	0 = IRQ does not assert when VMErrInt = 1. 1 = IRQ asserts when VMErrInt = 1.

BITFIELD	BITS	DESCRIPTION	DECODE
		Set this bit to assert the IRQ output when the VMErrInt bit is set (DEVInt[2] = 1).	
ThWIntEn	1	Thermal Warning Interrupt (ThWInt) Enable Set this bit to assert the IRQ output when the ThmWrnInt bit is set (DEVInt[1] = 1).	0 = IRQ does not assert when ThWInt = 1. 1 = IRQ asserts when ThWInt = 1.

ISDUIntEn (0x10)

BIT	7	6	5	4	3	2	1	0
Field	-	–	ISDU_BAVIntEn	CHKPDUErrIntEn	NewISDUWriteStartIntEn	ISDUAbrtIntEn	ISDUIdleIntEn	ISDUPckIntEn
Reset		–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
-	7	This bit is reserved.	
ISDU_BAVIntEn	5	ISDU Buffer Available Interrupt (ISDU_BAVInt) Enable Set this bit to assert the IRQ output when the ISDU_BAVInt bit is set (ISDUInt[5] = 1).	0 = IRQ does not assert when ISDU_BAVInt = 1. 1 = IRQ asserts when ISDU_BAVInt = 1.
CHKPDUErrIntEn	4	CHKPDU Error Interrupt (CHKPDUErrInt) Enable Set this bit to assert the IRQ output when the CHKPDUErrInt bit is set (ISDUInt[4] = 1).	0 = IRQ does not assert when CHKPDUErrInt = 1. 1 = IRQ asserts when CHKPDUErrInt = 1.
NewISDUWriteStartIntEn	3	New ISDU Out Cycle Write Start Interrupt (NewISDUWriteStartInt) Enable Set this bit to assert the IRQ output when the NewISDUWriteStartInt bit is set (ISDUInt[3] = 1).	0 = IRQ does not assert when NewISDUWriteStartInt = 1. 1 = IRQ asserts when NewISDUWriteStartInt = 1.
ISDUAbrtIntEn	2	ISDU ABORT Command Received Interrupt (ISDUAbrtInt) Enable Set this bit to assert the IRQ output when the ISDUAbrtInt bit is set (ISDUInt[2] = 1).	0 = IRQ does not assert when ISDUAbrtInt = 1. 1 = IRQ asserts when ISDUAbrtInt = 1.
ISDUIdleIntEn	1	ISDU IDLE Command Received Interrupt (ISDUIdleInt) Enable	0 = IRQ does not assert when ISDUIdleInt = 1. 1 = IRQ asserts when ISDUIdleInt = 1.

BITFIELD	BITS	DESCRIPTION	DECODE
		Set this bit to assert the IRQ output when the ISDUIdleInt bit is set (ISDUInt[1] = 1).	
ISDUPckIntEn	0	ISDU Packet Received Interrupt (ISDUPckInt) Enable Set this bit to assert the IRQ output when the ISDUPckInt bit is set (ISDUInt[0] = 1).	0 = IRQ does not assert when ISDUPckInt = 1. 1 = IRQ asserts when ISDUPckInt = 1.

IOLCfg (0x14)

BIT	7	6	5	4	3	2	1	0
Field	DeviceAnsDelay[1:0]		ConfDone	CRCEn	COMx[1:0]		Page1Inh	SIOForce
Reset	0b00		0b0	0b0	0b00		0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DeviceAnsDelay	7:6	Device Answer Delay These bits set the delay between the end of the IO-Link master message received and the beginning of the response from the MAX22516 to the masterr.	00 = 2 bit times 01 = 4 bit times 10 = 6 bit times 11 = 8 bit times
ConfDone	5	Map Configuration Complete Set this bit when the Register Map configuration has been completed after power-up. Note that the MAX22516 does not exit from SIO mode when this bit is 0.	0 = Register map configuration is not complete. 1 = Register map configuration is complete.
CRCEn	4	SPI CRC Enable Set this bit, or drive the CRCEN pin high, to enable CRC for SPI communication.	0 = CRC status depends on the CRCEN pin: SPI CRC is disabled if CRCEN is low. SPI CRC is enabled if CRCEN is high. 1 = CRC is enabled.
COMx	3:2	IO-Link Communication Speed Set these bits to select the COM rate for IO-Link communication between the MAX22516 and the IO-Link master.	00 = COM3 (230.4kbps) 01 = COM2 (38.4kbps) 10 = COM1 (4.8kbps) 11 = COM3 (230.4kbps)
Page1Inh	1	PAGE 1 Inhibit for IO-Link Master Writes Set this bit to reject IO-Link master writes to the RevisionID, DeviceID1, DeviceID2, and DeviceID3	0 = Master can overwrite RevisionID, DeviceID1, DeviceID2, and DeviceID3 in PAGE 1. 1 = Master cannot overwrite the contents of the RevisionID, DeviceID1, DeviceID2, and DeviceID3

BITFIELD	BITS	DESCRIPTION	DECODE
		parameters in PAGE 1. Writes to these parameters are rejected when this bit is set.	registers in PAGE 1. Writes to these registers are rejected.
SIOForce	0	Force SIO Mode Set this bit to reset the DL-Mode Handler state machine and force the MAX22516 into SIO mode.	0 = Do not force the MAX22516 to SIO mode. 1 = MAX22516 is forced to SIO mode.

WDGTmr (0x15)

BIT	7	6	5	4	3	2	1	0
Field	Watchdog[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Watchdog	7:0	Watchdog Counter This register records the number of successful IO-Link cycles, after which the MAX22516 goes automatically into SIO mode and WDInt is set. The watchdog is not active in SIO and ESTCOM modes. When this register is 0x00, the watchdog cycle counter is disabled. Periodically clear this register. The method to clear the register depends on the WDClear bit setting in the WDGClr register.

WDGClr (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	WDClear
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDClear	0	Watchdog Clear	0 = Watchdog[7:0] bits in the WDGTmr register are cleared after a SPI write into the WDGTmr register. If the WDG output is asserted, write a 1 to the WDInt bit in the

BITFIELD	BITS	DESCRIPTION	DECODE
			IOLInt register to clear the interrupt and deassert WDG. 1 = Watchdog[7:0] bits are cleared after loading PDIn data.

MISCCfg (0x17)

BIT	7	6	5	4	3	2	1	0
Field	LDO33Dis	–	IOLDly[1:0]		BuckDCM	BuckPFM	BuckSS	BuckDis
Reset		–						
Access Type	Write, Read	–	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO33Dis	7	V_{33} Linear Regulator Disable Use this register toe disable the V_{33} linear regulator output. The regulator is enabled by default.	0 = V_{33} linear regulator is enabled. 1 = V_{33} linear regulator is disabled
IOLDly	5:4	IO-Link Interpacket Delay Select Set these bits to select the interpacket delay during IO-Link communication. Delay is set in Tbit intervals.	00 = Delay is 1 Tbit times. 01 = Delay is 2 Tbit times. 10 = Delay is 3 Tbit times. 11 = Delay is 4 Tbit times.
BuckDCM	3	DC-DC Regulator DCM Mode Select The integrated DC-DC regulator operates in PWM mode by default. Set this bit to operate the DC-DC in DCM mode. See The BuckPFM bit to operate the DC-DC regulator in PFM mode instead of DCM or PWM mode.	0 = The DC-DC regulator operates in PFM mode (BuckPFM = 1) or PWM mode (BuckPFM = 0) after soft-start is complete. 1 = The DC-DC regulator operates in DCM mode after soft-start is complete.
BuckPFM	2	DC-DC Regulator PFM Mode Select The integrated DC-DC regulator operates in PWM mode by default. Set this bit to operate the DC-DC in PFM mode. See The BuckDCM bit to operate the DC-DC regulator in DCM mode instead of PFM or PWM mode.	0 = The DC-DC regulator operates in PWM mode (BuckDCM = 0) or DCM mode (BuckDCM = 1) after soft-start is complete. 1 = The DC-DC regulator operates in PFM mode after soft-start is complete.
BuckSS	1	DC-DC Spread Spectrum Enable	0 = Spread spectrum operation is not enabled on the DC-DC regulator.

BITFIELD	BITS	DESCRIPTION	DECODE
		Set this bit to enable the spread spectrum of the clock of the DC-DC regulator.	1 = Spread spectrum operation is enabled on the DC-DC regulator.
BuckDis	0	DC-DC Regulator Enable The integrated DC-DC regulator is enabled by default. Set this bit to disable the DC-DC.	0 = DC-DC regulator is enabled. 1 = DC-DC regulator is disabled.

CLKCfg (0x18)

BIT	7	6	5	4	3	2	1	0
Field	EnClkTrim	ExtClk	–	–	ClkDiv[2:0]			MCLKDis
Reset			–	–				
Access Type	Write, Read	Write, Read	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EnClkTrim	7	MCLK Trimming Enable Set this bit to enable fine trimming of the MCLK output frequency. For more information, see the CLKTrim register. MCLKDIR must be high to enable fine trimming.	0 = Fine trimming of the MCLK frequency is disabled. 1 = Fine trimming of the MCLK frequency is enabled.
ExtClk	6	External Clock Input Enable The internal oscillator is used for UART communication by default. Set this bit to use the external clock supplied at MCLK for the UART communication. This bit is ignored when the MCLKDIR pin is high.	0 = Internal oscillator is used for UART communication. 1 = External clock from MCLK is used for UART communication. For more information, see the ClkDiv bits.
ClkDiv	3:1	MCLK Frequency Select MCLK is an input when MCLKDIR is low. MCLK is an output when MCLKDIR is high. Set the CLKDIV:2:0] bits to set the MCLK frequency.	MCLKDIR is low or high: 000 = MCLK frequency is 3.686MHz (typ). 001 = MCLK frequency is 7.373MHz (typ). 010 = MCLK frequency is 14.74MHz (typ). 011 = MCLK frequency is 29.49MHz (typ). MCLKDIR is low (MCLK is an input): 10x = MCLK frequency is 1.843MHz (typ). 11x = MCLK frequency is 921.5kHz (typ). MCLKDIR is high (MCLK is an output): 100 = MCLK frequency is 1.843MHz (typ). 101 or 11x = MCLK is halted.

BITFIELD	BITS	DESCRIPTION	DECODE
MCLKDis	0	MCLK Disable The MCLK oscillator is enabled by default. Set this bit to disable MCLK. This bit is ignored when the MCLKDIR pin is low.	0 = MCLK is enabled. 1 = MCLK is disabled. MCLK is high when disabled.

CLKTrim (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ClkTrim[5:0]					
Reset	–	–						
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
ClkTrim	5:0	MCLK Trim Setting The ClkTrim[5:0] bits are used to trim the internally generated clock frequency. The bits are binary coded, centered to 0 from -5% for -32 to +6.7% for +31.

PAGE1_BYTE00 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	MasterCommand[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MasterCommand	7:0	Last Master Command Received This register contains the last IO-Link master command to the MAX22516 to switch operating states. This register can be read from microncontroller for debug purposes.

PAGE1_BYTE01 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	MasterCycleTime[7:0]							

Reset	0x00
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
MasterCycleTime	7:0	IO-Link Master Cycle Duration This register contains the actual cycle duration used by the IO-Link master to address the MAX22516. This register can be used as a parameter to monitor Process Data transfer.

PAGE1_BYTE02 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	MinCycleTime[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MinCycleTime	7:0	Device Minimum Cycle Time This register hold the minimum cycle duration supported by the MAX22516. The minimum cycle time is a performance feature of the IO-Link device. The microcontroller must write the minimum cycle time to the MAX22516 while the transceiver is being configured.

PAGE1_BYTE03 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	MSequenceCapability[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSequenceCapability	7:0	M-Sequency Capability This register contains information about implemented options related to M-sequences and physical configuration for the device.

PAGE1_BYTE04 (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	RevisionID[7:0]							
Reset	0x03							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RevisionID	7:0	Device Protocol Revision This register contains the revision of the protocol version used implementation of the device.

PAGE1_BYTE05 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	ProcessDataIn[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ProcessDataIn	7:0	Process Data In (PDIn) This register contains the type and length of the Input Process Data (process data from the device to the IO-Link master).

PAGE1_BYTE06 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	ProcessDataOut[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ProcessDataOut	7:0	Process Data Out (PDOut)

BITFIELD	BITS	DESCRIPTION
		This register contains the type and length of output data (process data from the IO-Link master to the device).

PAGE1_BYTE07 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	VendorID1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VendorID1	7:0	Unique Vendor Identification (MSB) Each IO-Link device vendor has a unique vendor identification number. This vendor identification must be communicated to the IO-Link master when establishing communication. Write the MSB of the unique vendor identification of the Device vendor using VendorID1 (MSB) and VendorID2 (LSB) in the PAGE1_BYTE07 and PAGE1_BYTE08 registers, respectively.

PAGE1_BYTE08 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	VendorID2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VendorID2	7:0	Unique Vendor Identification (LSB) Each IO-Link device vendor has a unique vendor identification number. This vendor identification must be communicated to the IO-Link master when establishing communication. Write the MSB of the unique vendor identification of the Device vendor using VendorID1 (MSB) and VendorID2 (LSB) in the PAGE1_BYTE07 and PAGE1_BYTE08 registers, respectively.

PAGE1_BYTE09 (0x23)

BIT	7	6	5	4	3	2	1	0

Field	DeviceID1[7:0]
Reset	0x00
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
DeviceID1	7:0	Unique Vendor-Allocated Device Indentification (Octet 2, MSB) Each IO-Link device has a unique device idenfication number allocated by the device vendor. Write the unique device identification number of the device using the DeviceID1 (MSB), DeviceID2, and DeviceID3 (LSB) in the PAGE1_BYTE09, PAGE1_BYTE0A, and PAGE1_BYTE0B registers, respectively.

PAGE1_BYTE0A (0x24)

BIT	7	6	5	4	3	2	1	0
Field	DeviceID2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DeviceID2	7:0	Unique Vendor-Allocated Device Indentification (Octet 1) Each IO-Link device has a unique device idenfication number allocated by the device vendor. Write the unique device identification number of the device using the DeviceID1 (MSB), DeviceID2, and DeviceID3 (LSB) in the PAGE1_BYTE09, PAGE1_BYTE0A, and PAGE1_BYTE0B registers, respectively.

PAGE1_BYTE0B (0x25)

BIT	7	6	5	4	3	2	1	0
Field	DeviceID3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DeviceID3	7:0	Unique Vendor-Allocated Device Indentification (Octet 0, LSB)

BITFIELD	BITS	DESCRIPTION
		Each IO-Link device has a unique device idenfication number allocated by the device vendor. Write the unique device identification number of the device using the DeviceID1 (MSB), DeviceID2, and DeviceID3 (LSB) in the PAGE1_BYTE09, PAGE1_BYTE0A, and PAGE1_BYTE0B registers, respectively.

PAGE1_BYTE0C (0x26)

BIT	7	6	5	4	3	2	1	0
Field	FunctionID1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FunctionID1	7:0	MSB (Reserved)

PAGE1_BYTE0D (0x27)

BIT	7	6	5	4	3	2	1	0
Field	FunctionID2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FunctionID2	7:0	LSB (Reserved)

PAGE1_BYTE0E (0x28)

BIT	7	6	5	4	3	2	1	0
Field	Page1Reserved1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Page1Reserved1	7:0	Reserved

PAGE1_BYTE0F (0x29)

BIT	7	6	5	4	3	2	1	0
Field	Page1Reserved2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
Page1Reserved2	7:0	Reserved

WDGEvent (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	WDGCode[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WDGCode	7:0	Watchdog Event Code It is possible to send a designated data octet to the StatusCode register when the watchdog timer expires. Write the required watchdog event code to WDGCode[7:0]. Data in the STATUS_CODE register is replaced with the WDGCode[7:0] bits when the watchdog timer expires and WDGEvent = 1.

STATUS_CODE_DEF (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	StatusCodeDefault[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
StatusCodeDefault	7:0	IO-Link Device Status Code Default Write the required default device status code to this register. When the IO-Link master issues a command to read from device Event memory address 0x00, and EventFlag = 0 in the EVENT_FLOW register, the contents of this register are transmitted to the IO-Link master. When the IO-Link master issues a command to read from device Event memory address 0x00, and EventFlag = 1 in the EVENT_FLOW register, the contents of the STATUS_CODE register are transmitted to the IO-Link master.

STATUS_CODE (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	StatusCode[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
StatusCode	7:0	IO-Link Device Status Code Write the device status code to this register. When the IO-Link master issues a command to read from device event memory address 0x00, and EventFlag = 1 in the EVENT_FLOW register, the contents of the STATUS_CODE register are transmitted to the IO-Link master.

EVENT_QUALIFIER (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	EventQualifier1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
EventQualifier1	7:0	Event Qualifier Octet Diagnosis information for a device is transmitted to the IO-Lionk master through events,

BITFIELD	BITS	DESCRIPTION
		which consist of EventQualifiers and EventCodes. Write EventQualifier codes to the EVENT_QUALIFIER register for IO-Link master event transmissions.

EVENT_CODE1MSB (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	EventCode1MSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
EventCode1MSB	7:0	Event Code Octet 1 (MSB) Diagnosis information for a device is transmitted to the IO-Link master through events, which consist of EventQualifiers and EventCodes. Write EventCodes to the EVENT_CODE1MSB and EVENT_CODE1LSB registers IO-Link master event transmissions.

EVENT_CODE1LSB (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	EventCode1LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
EventCode1LSB	7:0	Event Code Octet 2 (LSB) Diagnosis information for a device is transmitted to the IO-Link master through events, which consist of EventQualifiers and EventCodes. Write EventCodes to the EVENT_CODE1MSB and EVENT_CODE1LSB registers IO-Link master event transmissions.

EVENT_FLAG (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	WDGEvent	EventFlag

Reset	–	–	–	–	–	–		0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDGEvent	1	Watchdog Event Flag It is possible to send a designated data octect to the StatusCode register when the watchdog timer expires. Write the desired watchdog event code to WDGCode[7:0] and set WDGEvent = 1 to transmit this data when the timer expires.	0: Contents of the STATUS_CODE register are not overwritten and EventFlag is not set when the watchdog timer expires. 1: Contents of the STATUS_CODE register are overwritten with the contents of the WDG_EVENT register, and EventFlag is set, when the watchdog timer expires.
EventFlag	0	Event Flag Bit The checksum/status octet (CKS) is part of the reply message from a device to the IO-Link master. The event flag bit indicates to the IO-Link master if an event has occurred. Set the EventFlag bit high to indicate to the IO-Link master that an event has occurred. when an event has occurred. This bit is cleared upon receiving a write access to the STATUS_CODE register by the IO-Link master.	0 = No Event has occurred. 1 = Event has occurred.

PDINFIFO (0x35)

BIT	7	6	5	4	3	2	1	0
Field	PDINData[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
PDINData	7:0	Input Process Data (PDIn) FIFO Data written to the PDINFIFO register is automatically loaded in to the PDINFIFO. An SPI burst write to this register address write to the PDIn buffer only. The SPI address does not increment during the burst write.

PDINDataRdy (0x36)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PDStatus

Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PDStatus	0	Process Data Status Bit (PDStatus) The PDStatus bit sets the PDStatus bit in the CKS packet and indicates whether the validity of the Process data from the device. Write a 1 to this bit if the PDIn data is not valid. Clear this bit as soon as there is valid PD data to send to the master. PDIn data transmitted to the master is forced to 0x00 when PDStatus = 1. Note that, when GPIO1_TO_PDIN = 1 in the GPIO1CTRL register, PDIn follows GPIO1 as normal, regardless of the state of the PDStatus bit.	0 = Process data is valid. 1 = Process data is not valid.

PDOUTFIFO (0x37)

BIT	7	6	5	4	3	2	1	0
Field	PDOUTData[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PDOUTData	7:0	Output Process Data (PDOut) FIFO The microcontroller can read the process data from the PDOUTFIFO register during PDOut transfers. An SPI burst read of this register address read the PDOut buffer. The SPI address does not increment during the burst read.

ISDU_OFFSET (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	ISDU_OFFSET[7:0]							
Reset	0x00							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
ISDU_OFFSET	7:0	ISDU Data Offset The value in this register is the first address from which the ISDU data is written or read out through SPI. Both single and Burst Mode are allowed. Clear this register before setting bit the ISDUINDataRdy bit in the ISDUDataRdy register.

ISDUINFIFO (0x40)

BIT	7	6	5	4	3	2	1	0
Field	ISDUINData[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
ISDUINData	7:0	ISDU Data In FIFO Data written to this location are automatically loaded to ISDU FIFO. The ISDU buffer can be accessed only when the the IsduPckInt in the ISDU register is 1. An SPI burst write to this address write to the ISDU buffer only. The SPI address does not increment during the burst write.

ISDUDataRdy (0x41)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ISDUINDataRdy
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ISDUINDataRdy	0	ISDU FIFO Data Ready Bit Set this bit after writing data to the ISDUINFIFO	0 = Any request from the IO-Link master for an ISDU read is responded with ISDU BUSY.

BITFIELD	BITS	DESCRIPTION	DECODE
		register to begin the IO-Link transfer. Ensure that IsduPckInt = 0 in the ISDUInt register and NewISDUWriteStartInt must be low. ISDUINDataRdy is automatically cleared when the IO-Link master sends the DL_ISDU-ABORT or ISDU_IDLE commands.	1 = The byte loaded into the ISDUINData FIFO is ready to be transmitted to IO-Link master.

ISDUOUTFIFO (0x42)

BIT	7	6	5	4	3	2	1	0
Field	ISDUOUTData[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ISDUOUTData	7:0	ISDU Data Out FIFO The microcontroller can read the ISDU data from the ISDUOUTFIFO register during ISDU out transfers. The ISDU buffer can be accessed only when the the IsduPckInt in the ISDU register is 1. An SPI burst read from this address read from the ISDU buffer only. The SPI address does not increment during the burst read.

ISDU_LEVEL (0x43)

BIT	7	6	5	4	3	2	1	0
Field	ISDU_LEVEL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ISDU_LEVEL	7:0	ISDU FIFO Fill Level Data written to the ISDU_LEVEL register is the expected fill level of the ISDU FIFO after the end of an ISDU out transfer initiated by the IO-Link master.

BITFIELD	BITS	DESCRIPTION
		Calculate the fill level using the value of the ISDU header (that is, the first byte, or first two bytes) of the ISDU FIFO.

LED1CTRMSB (0x50)

BIT	7	6	5	4	3	2	1	0
Field	LED1CtrMsb[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LED1CtrMsb	7:0	LED1 Control Sequence MSB The LED1 output is enabled (low) for each '1' in this register. LED1 is disabled (high impedance) for each '0' in this register. Each bit is sampled with a 63ms period clock. Write to both the LED1CTRMSB and LED1CTRLSB registesr to change or update LED funcitonality.

LED1CTRLSB (0x51)

BIT	7	6	5	4	3	2	1	0
Field	LED1CtrLsb[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LED1CtrLsb	7:0	LED1 Control Sequence LSB The LED1 output is enabled (low) for each '1' in this register. LED1 is disabled (high impedance) for each '0' in this register. Each bit is sampled with a 63ms period clock. Write to both the LED1CTRMSB and LED1CTRLSB registesr to change or update LED funcitonality.

LED2CTRMSB (0x52)

BIT	7	6	5	4	3	2	1	0
Field	LED2CtrMsb[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LED2CtrMsb	7:0	LED2 Control Sequence MSB The LED2 output is enabled (low) for each '1' in this register. LED2 is disabled (high impedance) for each '0' in this register. Each bit is sampled with a 63ms period clock. Write to both the LED2CTRMSB and LED2CTRLSB registesr to change or update LED funcitonality.

LED2CTRLSB (0x53)

BIT	7	6	5	4	3	2	1	0
Field	LED2CtrLsb[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LED2CtrLsb	7:0	LED2 Control Sequence LSB The LED2 output is enabled (low) for each '1' in this register. LED1 is disabled (high impedance) for each '0' in this register. Each bit is sampled with a 63ms period clock. Write to both the LED2CTRMSB and LED2CTRLSB registesr to change or update LED funcitonality.

GPIO1CTRL (0x54)

BIT	7	6	5	4	3	2	1	0
Field	GPIO1Din	–	GPIO1_TO_PDIN	GPIO1OD	GPIO1Dout	GPIO1IO	GPIO1PUEn	GPIO1Res

Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO1Din	7	GPIO1 Data In Bit This bit reflects the state of the GPIO1 pin when configured as an input (GPIO1HiZ = 1). Ignore this bit when GPIO1 is configured as an output.	0 = GPIO1 pin is low. 1 = GPIO1 pin is high.
GPIO1_TO_PDIN	5	GPIO1 Input/Output Configuration Bit When GPIO1 is configured as an input, and GPIO1_TO_PDIN = 1, GPIO1 sets the LSB of the PDIn bytes sent to the IO-Link master. When GPIO1 is high, the LSB of the PDIn data is 0. When GPIO1 is low, the LSB of the PDIn data is 1.	0 = GPIO1 does not set the LSB of the PDIn bytes. 1 = GPIO1 sets the LSB of the PDIn bytes sent to the master.
GPIO1OD	4	GPIO1 Configuration Bit Use this bit to configure GPIO1 as either an open-drain output or a push-pull output. This bit is ignored when GPIO1 is an input (GPIO1IO = 0).	0 = GPIO1 is a push-pull output. 1 = GPIO1 is an open-drain output.
GPIO1Dout	3	GPIO1 Logic Output State GPIO1Dout reflects the logic state of the GPIO1 pin. When GPIO1 is configured as an input, GPIO1 can be read to determine the state of the GPIO1 pin. When GPIO1 is configured as an output, set this bit to set the logic state of GPIO1.	0 = GPIO1 is low. 1 = GPIO1 is high.
GPIO1IO	2	GPIO1 Input/Output Enable Bit GPIO1 is an input by default. Set this bit to configure GPIO1 as an output.	0 = GPIO1 is an input. 1 = GPIO1 is an output.
GPIO1PUEn	1	GPIO1 Pull-up Enable Bit When GPIO1 is configured as an input, an internal pull-up or pull-down resistor can be enabled on GPIO1 using the GPIO1PUEn and GPIO1Res bits. Set GPIO1Res = 0 and GPIO1PUEn = 1 to enable the internal 330kΩ (typ) pull-up on GPIO1. Set	0 = GPIO1 input pull-down enabled (GPIO1Res = 1). 1 = GPIO1 input pull-up enabled (GPIO1Res = 1).

BITFIELD	BITS	DESCRIPTION	DECODE
		GPIO1Res = 0 and GPIO1PUEn = 0 to enable the internal 330kΩ (typ) pull-down on GPIO1. This bit is ignored if GPIO1IO = 1 or GPIO1Res = 1.	
GPIO1Res	0	GPIO1 I/O Resistor Enable Bit When GPIO1 is configured as an input, an internal pull-up or pull-down resistor can be enabled on GPIO1 using the GPIO1PUEn and GPIO1Res bits.	0 = GPIO1 input resistor is enabled. 1 = GPIO1 input resistor is disabled.

GPIO2CTRL (0x55)

BIT	7	6	5	4	3	2	1	0
Field	GPIO2Din	–	PDOUT_TO_GPIO2	GPIO2OD	GPIO2Dout	GPIO2IO	GPIO2PUEn	GPIO2Res
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO2Din	7	GPIO2 Data In Bit This bit reflects the state of the GPIO2 pin when configured as an input (PDOUT_TO_GPIO2 = 1). Ignore this bit when GPIO2 is configured as an output.	0 = GPIO2 pin is low. 1 = GPIO2 pin is high.
PDOUT_TO_GPIO2	5	GPIO2 Input/Output Configuration Bit Set PDOUT_TO_GPIO2 = 1 to configure GPIO2 as an output. When configured as an output, the logic state of GPIO2 reflects the LSB of each received PDOut byte.	0 = GPIO2 is an input. 1 = GPIO2 is an output. GPIO2 reflects the LSB of the received PDOut bytes.
GPIO2OD	4	GPIO2 Configuration Bit Use this bit to configure GPIO2 as either an open-drain output or a push-pull output. This bit is ignored when GPIO2 is an input (GPIO2IO = 0).	0 = GPIO2 is a push-pull output. 1 = GPIO2 is an open-drain output.

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO2Dout	3	GPIO2 Logic Output State GPIO2Dout reflects the logic state of the GPIO2 pin. When GPIO2 is configured as an input, GPIO2 can be read to determine the state of the GPIO2 pin. When GPIO2 is configured as an output, set this bit to set the logic state of GPIO2.	0 = GPIO2 is low. 1 = GPIO2 is high.
GPIO2IO	2	GPIO2 Input/Output Enable Bit GPIO2 is an input by default. Set this bit to configure GPIO2 as an output.	0 = GPIO2 is an input. 1 = GPIO2 is an output.
GPIO2PUEn	1	GPIO2 Pull-up Enable Bit When GPIO2 is configured as an input, an internal pull-up or pull-down can be enabled on GPIO2 using the GPIO2PUEn and GPIO2Res bits. Set GPIO2Res = 0 and GPIO2PUEn = 1 to enable the internal 330kΩ (typ) pull-up on GPIO2. Set GPIO2Res = 0 and GPIO2PUEn = 0 to enable the internal 330kΩ (typ) pull-down on GPIO2. This bit is ignored if GPIO2IO = 1 or GPIO2Res = 1.	0 = GPIO2 input pull-down enabled (GPIO2Res = 1). 1 = GPIO2 input pull-up enabled (GPIO2Res = 1).
GPIO2Res	0	GPIO2 I/O Resistor Enable Bit When GPIO2 is configured as an input, an internal pull-up or pull-down resistor can be enabled on GPIO2 using the GPIO2PUEn and GPIO2Res bits.	0 = GPIO2 input resistor is enabled. 1 = GPIO2 input resistor is disabled.

CQ_CTRL1 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	CQ_SLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	CQ_INV	CQ_EN
Reset								
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CQ_SLEW	7:6	C/Q Driver Slew Rate Select	00 = 310ns (typ) 01 = 610ns (typ)

BITFIELD	BITS	DESCRIPTION	DECODE
		Set the CQ_SLEW[1:0] bits to program the typical rising and falling slew rates on the C/Q driver. CQ_SLEW[1:0] are ignored when the CQ_CLDIS bit is set.	10 = 1.5µs (typ) 11 = 6.3µs (typ)
CQ_PD	5	C/Q Weak Pull-Down Enable Enable/disable the weak pull-down current on C/Q.	0 = The 300µA (typ) weak pull-down current on C/Q is disabled. 1 = The 300µA (typ) weak pull-down current on C/Q is enabled.
CQ_PU	4	C/Q Weak Pull-Up Enable Enable/disable the weak pull-up current on C/Q.	0 = The 300µA (typ) weak pull-up current on C/Q is disabled. 1 = The 300µA (typ) weak pull-up current on C/Q is enabled.
CQ_NPN	3	C/Q Driver NPN Mode Select Set this bit to configure the C/Q driver in NPN mode when CQ_PP = 0. This bit is ignored when CQ_PP = 1 or when C/Q is configured in IO-Link mode.	0 = The C/Q driver is in PNP mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1). 1 = The C/Q driver is in NPN mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1).
CQ_PP	2	C/Q Driver Push-Pull Mode Select Set this bit to configure the C/Q driver in push-pull mode. This bit is ignored when C/Q is configured in IO-Link mode. C/Q is forced to push-pull mode in IO-Link mode.	0 = The C/Q driver is in PNP mode (CQ_NPN = 0) or NPN mode (CQ_NPN = 1). 1 = The C/Q driver is in push-pull mode.
CQ_INV	1	C/Q Receiver/Driver Logic Invert By default, C/Q is the logic inverse of the signals at the TX and RX pins. Set this bit to invert the C/Q signal so that the C/Q logic matches the signals on Tx and RX.	0 = C/Q logic is inverted compared to TX and RX. 1 = C/Q logic is the same as TX and RX.
CQ_EN	0	C/Q Driver Enable	0 = C/Q driver is disabled. 1 = C/Q driver is enabled.

CQ_CTRL2 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	CQ_CL[1:0]		–	CQ_CLBL[1:0]		CQ_AutoRtyTime[1:0]		CQ_AutoRtyEn
Reset	0b000		–	0b00		0b00		0b0
Access Type	Write, Read		–	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CQ_CL	7:6	C/Q Driver Current Limit Setting Set the CQ_CL[1:0] bits to select the active current limit level for the C/Q driver when CQ_CLDIS = 0.	00 = 50mA (min) 01 = 100mA (min) 10 = 200mA (min) 11 = 250mA (min)
CQ_CLBL	4:3	C/Q Driver Current Limit Blanking Time Set the CQ_CLBL[1:0] to program the blanking time for the C/Q driver: An interrupt is generated, and the C/Q driver is disabled, when the load current exceeds the C/Q driver current threshold for longer than the programmed blanking time.	00 = 128µs (typ) 01 = 500µs (typ) 10 = 1ms (typ) 11 = 5ms (typ)
CQ_AutoRtyTime	2:1	C/Q Driver Fix Off-Time Set the CQ_AutoRtyTime[1:0] bits to select the fixed off-time for the C/Q driver after a fault has been generated and auto-retry functionality is enabled (CQ_AutoRtyEn = 1). The driver is automatically re-enabled after the fixed off-delay.	00 = 50ms (typ) 01 = 100ms (typ) 10 = 200ms (typ) 11 = 500ms (typ)
CQ_AutoRtyEn	0	C/Q Driver Autoretry Enable When a fault is signaled on the C/Q driver, and CQ_AutoRtyEn = 1, the driver is disabled for the programmed fixed off time (CQ_AutoRtyTime[1:0]) and then automatically reenabled.	0 = Autoretry is disabled on the C/Q driver. 1 = Autoretry is enabled on the C/Q driver.

DO_CTRL1 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	DO_SLEW[1:0]		DO_PD	DO_PU	DO_NPN	DO_PP	DO_INV	DO_EN
Reset								
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DO_SLEW	7:6	DO Driver Slew Rate Select Set the DO_SLEW[1:0] bits to program the typical rising and falling slew rates on the DO driver. DO_SLEW[1:0] are ignored when the DO_CLDIS bit is set.	00 = 310ns (typ) 01 = 610ns (typ) 10 = 1.5µs (typ) 11 = 6.3µs (typ)

BITFIELD	BITS	DESCRIPTION	DECODE
DO_PD	5	DO_PD Weak Pull-Down Enable Enable/disable the weak pull-down current on DO.	0 = The 300µA (typ) weak pull-down current on DO is disabled. 1 = The 300µA (typ) weak pull-down current on DO is enabled.
DO_PU	4	DO Weak Pull-Up Enable Enable/disable the weak pull-up current on DO.	0 = The 300µA (typ) weak pull-up current on DO is disabled. 1 = The 300µA (typ) weak pull-up current on DO is enabled.
DO_NPN	3	DO Driver NPN Mode Select Set this bit to configure the DO driver in NPN mode when DO_PP = 0. This bit is ignored when DO_PP = 1.	0 = The DO driver is in PNP mode (DO_PP = 0) or push-pull mode (DO_PP = 1). 1 = The DO driver is in NPN mode (DO_PP = 0) or push-pull mode (DO_PP = 1).
DO_PP	2	DO Driver Push-Pull Mode Select Set this bit to configure the DO driver in push-pull mode.	0 = The DO driver is in PNP mode (DO_NPN = 0) or NPN mode (DO_NPN = 1). 1 = The DO driver is in push-pull mode.
DO_INV	1	DO Driver Logic Invert By default, DO is the logic inverse of the signal at the LO pin. Set this bit to invert the DO signal so that the DO logic matches the signal on LO.	0 = DO logic is inverted compared to LO. 1 = DO logic is the same as LO.
DO_EN	0	DO Driver Enable	0 = DO driver is disabled. 1 = DO driver is enabled

DO_CTRL2 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	DO_CL[1:0]		–	DO_CLBL[1:0]		DO_AutoRtyTime[1:0]		DO_AutoRtyEn
Reset	0b000		–	0b00		0b00		0b0
Access Type	Write, Read		–	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DO_CL	7:6	DO Driver Current Limit Setting Set the DO_CL[1:0] bits to select the active current limit level for the C/Q driver when DO_CLDIS = 0.	00 = 50mA (min) 01 = 100mA (min) 10 = 200mA (min) 11 = 250mA (min)
DO_CLBL	4:3	DO Driver Current Limit Blanking Time Set the DO_CLBL[1:0] to program the blanking	00 = 128µs (typ) 01 = 500µs (typ)

BITFIELD	BITS	DESCRIPTION	DECODE
		time for the DO driver: An interrupt is generated, and the DO driver is disabled, when the load current exceeds the DO driver current threshold for longer than the programmed blanking time.	10 = 1ms (typ) 11 = 5 ms (typ)
DO_AutoRtyTime	2:1	DO Driver Fix Off-Time Set the DO_AutoRtyTime[1:0] bits to select the fixed off-time for the DO driver after a fault has been generated and auto-retry functionality is enabled (DO_AutoRtyEn = 1). The driver is automatically re-enabled after the fixed off-delay.	00 = 50ms (typ) 01 = 100ms (typ) 10 = 200ms (typ) 11 = 500ms (typ)
DO_AutoRtyEn	0	DO Driver Autoretry Enable When a fault is signaled on the DO driver, and DO_AutoRtyEn = 1, the driver is disabled for the programmed fixed off time (AutoRtyTime[1:0]) and then automatically reenabled.	0 = Autoretry is disabled on the DO driver. 1 = Autoretry is enabled on the DO driver.

TX_CTRL (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	CQTx	CQTxEn	CQDrvSel	DOTx	DODrvSel	–	CQDOPar	DO_AV
Reset	0b0	0b0	0b0	0b0	0b0	–		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CQTx	7	C/Q Driver Logic Control Bit Set CQDrvSel = 1 to configure the CQTxEn and CQTx bits to control the C/Q driver. This bit is ignored when CQDrvSel = 0.	0 = C/Q is high (CQDrvSel = 1, CQTxEn = 1, CQ_EN = 1). 1 = C/Q is low (CQDrvSel = 1, CQTxEn = 1, CQ_EN = 1). C/Q logic states are inverted when CQ_INV = 1.
CQTxEn	6	C/Q Driver Enable Control Bit Set CQDrvSel = 1 to configure the CQTxEn and CQTx bits to control the C/Q driver. This bit is ignored when CQDrvSel = 0.	0 = C/Q driver is disabled (CQDrvSel = 1, CQ_EN = 0 or 1). 1 = C/Q driver is enabled (CQDrvSel = 1, CQ_EN = 1)
CQDrvSel	5	C/Q Driver Input Select The C/Q driver can be enabled and driven using either the TXEN and TX pins, or by setting the CQTxEn and CQTx bits. C/Q is driven by the TXEN and TX inputs by default.	0 = C/Q is driven by the TXEN and TX input pins. 1 = C/Q is driven by the CQTxEcn and CQTx bits. The TXEN and TX pins are ignored.

BITFIELD	BITS	DESCRIPTION	DECODE
		Set CQDrvSel = 1 to configure the CQTxEn and CQTx bits to control the C/Q driver. TXEN and TX are ignored when this bit is set.	
DOTx	4	DO Driver Logic Control Bit Set DODrvSel = 1 to configure the DOTx bit to control the DO driver. This bit is ignored when DODrvSel = 0.	0 = DO is high (DODrvSel = 1, DO_EN = 1). 1 = DO is low (DODrvSel = 1, DO_EN = 1). DO logic states are inverted when DO_INV = 1.
DODrvSel	3	DO Driver Input Select The DO driver can be enabled and driven using either the LO pin, or by setting the DoTx bit. DO is driven by LO by default. Set DODrvSel = 1 to configure the DOTx bit to control the DO driver. The LO pin is ignored when this bit is set.	0 = DO output driven by the LO input pin. 1 = DO is driven by the DoTx bit. The LO pin is ignored.
CQDOPar	1	C/Q and DO Tracking Enable Set CQDoPar = 1 to enable tracking of the C/Q and DO outputs. In this configuration, DO tracks C/Q and both drivers switch as a function of the TX input or/and the CQTx bit. CQDOPar must be set when DO_AV=1.	0 = The DO driver operates independently of C/Q. 1 = The DO driver tracks the C/Q driver.
DO_AV	0	C/Q and DO Antivalent Select CQDOPar must be set to enable this functionality. Set DO_AV = 1 to enable antivalent operation of the C/Q and DO outputs. When CQDOPar = 1 and DO_AV = 0, both C/Q and DO switch as a function of the TX input pin or/and the CQTx bit, but with opposite logic. When CQDOPar = 1 and DO_AV = 1, both C/Q and DO switch as a function of the TX input pin and/or the CQTx bit, but with the same logic. This bit is ignored when CQDOPar = 0.	0 = C/Q and DO switch with normal (inverted logic) polarity of the TX pin or CQTx bit. 1 = C/Q and DO follow the same logic as the TX pin or CQTx bit.

RX_CTRL (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	RXTTL	RXDIS	RXFilter	–	–	–	DIFilter
Reset	–				–	–	–	
Access Type	–	Write, Read	Write, Read	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RXTTL	6	RX TTL Threshold Enable Use this bit to select the C/Q receiver thresholds. By default, threshold voltages are set to 11V (min) and 13V (max) for normal IO-Link functionality. Set this bit to select TTL thresholds for the C/Q receiver, instead.	0 = IO-Link receiver thresholds enabled for C/Q receiver. 1 = TTL receiver thresholds enabled for C/Q receiver.
RXDIS	5	RX Output Disable Set this bit to disable the RX output. RX is high impedance when disabled and the the C/Q input current is reduced when RXDIS = 1.	0 = RX logic output is enabled. 1 = RX logic output is disabled.
RXFilter	4	C/Q Receiver Glitch Filter Enable	0 = The 1µs (typ) glitch filter on the C/Q receiver is disabled. 1 = The 1µs (typ) glitch filter on the C/Q receiver is enabled.
DIFilter	0	DI Receiver Glitch Filter Enable	0 = The 1µs (typ) glitch filter on the DI receiver is disabled. 1 = The 1µs (typ) glitch filter on the DI receiver is enabled.

MISC_CTRL (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	HEART_WU	–	–	–	–	–	CQPUD2mA	DOPUD2mA
Reset		–	–	–	–	–		
Access Type	Write, Read	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HEART_WU	7	HEART/WU (Heart or Wake-Up) Function Select HEART/WU is a dual function pin. Set this bit to operat this pin as a wake-up indicator or an IO-Link cycle indicator.	0 = Wake-up (WU) functonality selected. HEART/WU is driven low when a valid wake-up is detected. 1 = IO-Link cycle indicator (HEART) functionality selected. HEART/WU is driven low every IO-Link cycle.
CQPUD2mA	1	C/Q 2mA Pull-up/Pull-Down Enable For more information, see Table 3.	0 = 2mA (typ) current on C/Q is disabled. 1 = 2mA (typ) current on C/Q is enabled.
DOPUD2mA	0	DO 2mA Pull-up/Pull-Down Enable For more information, see Table 3.	0 = 2mA (typ) current on DO is disabled. 1 = 2mA (typ) current on DO is enabled.

ThADCCfg (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	ADCStart	–	–	–	–	–	ADCCfg[1:0]	
Reset		–	–	–	–	–		
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ADCStart	7	Manual Thermal ADC Conversion Start Bit Set ADCCfg[1:0] = 10 or 01 to enable manual thermal ADC conversion and set ADCStart = 1 to begin the conversion. Results of the thermal conversion are stored in the ThADCRes register once the conversion is complete.	0 = No manual thermal ADC conversion. 1 = Start new manual thermal ADC conversion.
ADCCfg	1:0	Thermal ADC Configuration Set these bits to configure the thermal warning threshold (for example, default or programmable) or to enable manual thermal ADC conversion.	00 = Internal/Default thermal warning threshold and response time is enabled. 01 = Programmable thermal warning threshol is enabled. 1x = Manual thermal ADC is enabled. Thermal warning is disabled in this mode.

ThADCThd (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ThWrn[5:0]					
Reset	–	–						
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ThWrn	5:0	Programmable Thermal Warning Threshold Set ADCCfg[1:0] bits in the ThADCCfg register to enable the programmable thermal warning threshold. Program the ThWrn[5:0] bits to set the thermal warning threshold. Scaling is the same as for the ThVal[5:0] bits in the ThADCRes register. The ThWInt and ThW bits in are set when the die temperature exceeds this threshold. There is no	These bits are only valid when ADCCfg[1:0] = 01. Bits are binary coded with 1LBS = 3°C and ThWrn = 0 at -15°C. For more information, see the Temperature Measurements section.

BITFIELD	BITS	DESCRIPTION	DECODE
		hysteresis when the programmable thermal warning threshold is enabled.	

ThADCRes (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	ADC_EOB	–	ThVal[5:0]					
Reset		–						
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_EOB	7	Manual Thermal ADC End of Conversion Indicator Set the ADCCfg[1:0] = 10 or 11 to enable manual thermal ADC conversion. This bit is set when a thermal ADC conversion is complete.	0 = Thermal ADC conversion is complete and ThVal[5:0] bits hold the latest thermal ADC conversion value. 1 = Thermal ADC conversion is running. Value in the ThVal[5:0] bits is not valid.
ThVal	5:0	Manual Thermal ADC Conversion Results	This register holds the results of the latest thermal conversion. Bits are binary coded with 1LBS = 3°C and ThVal = 0 at -15°C. For more information, see the Temperature Measurements section.

Applications Information

MCLK Microcontroller Clocking

The MCLK output produces a clock that can be used for clocking a microcontroller (when MCLKDIR pin is high).

Select the frequency of the MCLK output by setting the ClkDiv bits in the CLKCfg register. Available MCLK frequencies are 1.843MHz (typ), 3.686MHz (typ), 7.373MHz (typ), 14.74MHz (typ), and 29.49MHz (typ). The MCLK frequency can be further adjusted by setting the EnClkTrim bit in the CLKCfg register and writing the ClkTrim bits in the CLKTrim register.

MCLK is enabled by default and the switching frequency is 3.686MHz (typ). MCLK voltage output levels are referenced to the V_L logic supply.

EMC Protection

The MAX22516 features integrated surge protection of ±1kV/500Ω for 8µs/20µs surge on the C/Q, DO, and V_{24} pins to ground. No external protection is required on these pins to meet the ESD and burst requirements in the IO-Link standard. External TVS diodes are required to meet higher levels of surge protection. Ensure that the TVS diode peak clamping voltage is within the absolute maximum voltage ratings.

For all applications, a resistor greater or equal to 1kΩ should be use for safe operation on DI.

For applications where DI is connected to DO, a low-power 1kΩ resistor may be used. A standard 0603 is suitable for this configuration.

For applications where DI used, but is not connected to DO, there are two options. The first option is to use a series pulse resistor rated to withstand the surge energy. The RPC2512 is an example of a suitable resistor for this configuration. The second option, which can result in a smaller overall footprint, is to use a low-power resistor in combination with an external TVS diode. The TVS should be connected at the line side of the series resistor and must be able to absorb the surge energy. The TVS has the function of limiting the peak voltage so that the resistor sees a low differential voltage during the surge transient. Suitable TVS include the SPT02-236 and PDFN3-32.

Layout and Grounding

Layout for the MAX22516 is important to ensure that all parts operate normally and with minimal interference.

The MAX22516 features three ground pins: analog ground (GND), digital ground (GNDD), and IO-Link ground (GNDCQ).

Bypass all supply pins for the IC (V_5, V_L, and PV24) to the GND pin and connect directly to a ground plane. Bypass capacitors should be placed as close to the IC as possible. Connect the GNDD pins directly to the GND plane under the exposed pad of the IC for the TQFN or at the C4, D4, and D5 pads on the WLP.

The V_{24}, C/Q, DO, DI and GNDCQ pins are connected directly to the IO-Link connector. Connect all bypass capacitors and other components on this line directly to the GNDCQ. Connect the GNDCQ to the ground layer at the IC (at the exposed pad for the TQFN or under pad B3, C3, and C4 on the WLP package).

Keep the component loop for the DC-DC buck regulator as small as possible. Ensure that the feedback resistor divider is not near the inductor. Connect the ground terminal of the DC-DC output capacitor to the ground plane with multiple vias.

For a sample layout, refer to the MAX22516 EV kit.

Ordering Information

PART NUMBER	TEMP. RANGE	PIN-PACKAGE
MAX22516ATL+	-40°C to +125°C	40 TQFN-EP*
MAX22516ATL+T	-40°C to +125°C	40 TQFN-EP*
MAX22516AWO+	-40°C to +125°C	42 WLP
MAX22516AWO+T	-40°C to +125°C	42 WLP

*Exposed Pad

+T Tape and Reel

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Release for market intro	—
1	1/24	Removed all TQFN package from General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Pin Configuration, Pin Description, Layout and Grounding sections, and the Ordering Information table	1, 2, 3, 17, 18, 83
2	3/24	Add TQFN package from General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Pin Configuration, Pin Description, Layout and Grounding sections, and the Ordering Information table, Update EC Table	1-5, 9, 17, 18, 83

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

MAX22516AWO+ MAX22516AWO+T