19-2520; Rev 5; 1/09

EVALUATION KIT AVAILABLE

2.4GHz SiGe Linear Power Amplifier

General Description

The MAX2247 low-voltage, three-stage linear power amplifier (PA) is optimized for 802.11b/g wireless LAN (WLAN) applications in the 2.4GHz ISM band. The device is integrated with an adjustable bias control, power detector, and shutdown mode. The MAX2247 features 29dB of power gain and delivers up to +24dBm of linear output power at 24% efficiency from a single +3.3V supply. It achieves less than -32dBc first-side lobe suppression and less than -55dBc second-side lobe suppression under 802.11b modulation. In addition, the device can be matched for optimum efficiency and performance at output power levels from +10dBm to +24dBm. Its high +28dBm saturated output power also allows the device to meet the requirements of 802.11g OFDM modulation.

The MAX2247 features an external bias-control pin that allows the supply current of the device to be dynamically throttled back at lower output power levels, thus improving efficiency while maintaining sufficient side-lobe suppression. Proprietary internal bias circuitry maintains stable device performance over temperature and voltage-supply variations. An additional power-saving feature is a logic-level shutdown pin that reduces supply current to 0.5µA and eliminates the need for an external supply switch. The integrated shutdown function also allows guaranteed device ramp-on and ramp-off times.

The MAX2247 integrates a power detector with 20dB dynamic range and ±0.8dB accuracy at the highest output power level. The detector provides a buffered DC voltage proportional to the output power of the device, saving cost and space by eliminating a coupler and op amp usually required to implement a power detector function. The device is packaged in the tiny 3 × 4 chip-scale package (UCSP™), measuring only 1.5mm × 2mm, making it the ideal solution for radios built in small form factors.

Applications

IEEE 802.11b DSSS WLAN

IEEE 802.11g OFDM WLAN

HomeRF™

2.4GHz Cordless Phones

2.4GHz ISM Radios

UCSP is a trademark of Maxim Integrated Products, Inc.
HomeRF is a trademark of HomeRF Working Group.

Features

- **2.4GHz to 2.5GHz Operating Range**
- **Up to +24dBm Linear Output Power (ACPR of Less than -32dBc First-Side Lobe and Less than -55dBc Second-Side Lobe)**
- **24% PAE at +24dBm Linear Output Power, 3.3V**
  24% PAE at +21dBm Linear Output Power, 3.0V
- **29dB Power Gain**
- **On-Chip Power Detector with Buffered Output**
- **Internal 50Ω Input Matching**
- **External Bias Control for Current Throttleback**
- **Integrated Bias Circuitry**
- **+2.7V to +4.2V Single-Supply Operation**
- **0.5µA Shutdown Mode**
- **Tiny Chip-Scale Package (1.5mm × 2mm)**

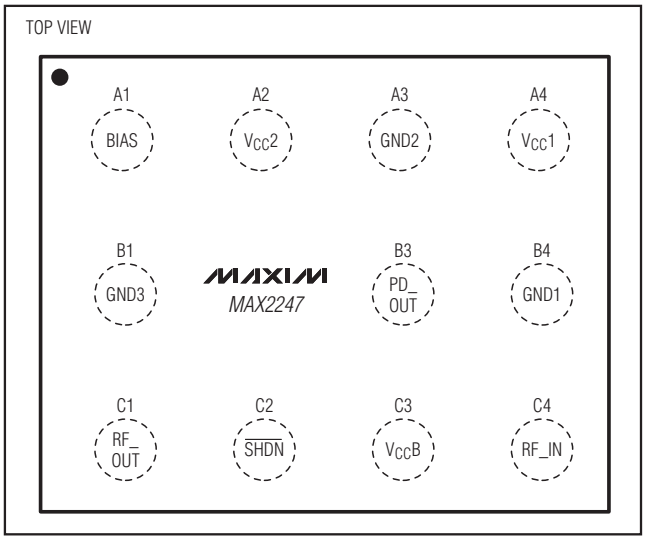
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX2247EBC-T	-40°C to +85°C	4 x 3 UCSP*	AAW
MAX2247EWC+T	-40°C to +85°C	12 WLP	+AAX

**Requires special solder temperature profile in the Absolute Maximum Ratings Sections.*
-Denotes a package containing lead(Pb).
+Denotes a lead(pB)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

Pin Configuration



2.4GHz SiGe Linear Power Amplifier

ABSOLUTE MAXIMUM RATINGS

$V_{CC}1$, $V_{CC}2$, $V_{CC}B$, RF_OUT to GND.....-0.3V to +4.5V
$\overline{SHDN}$, BIAS, PD_OUT .....-0.3V to $V_{CC\_}$ + 0.3V
RF Input Power (50Ω source).....+5dBm
RF_IN Input Current.....±1mA
Maximum VSWR Without Damage 10:1
Maximum VSWR for Stable Operation, P_{OUT} < +25dBm.....5:1
Continuous Power Dissipation (T_A = +70°C)
4 × 3 UCSP, 12 WLP
(derate 28.5mW/°C above +70°C).....1.3W
Thermal Resistance (Note 1).....35°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +125°C
UCSP Bump Temperature (soldering) (Note 2)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C
WLP Bump Soldering Temperature .....+250°C
Continuous Operating Lifetime.....$10yrs \times 0.92^{(T_A - 60°C)}$
(For Operating Temperature, $T_A \geq +60°C$)

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits the use of only the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not recommended.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2247 EV kit, $V_{CC\_}$ = +2.7V to +4.2V, $\overline{SHDN}$ = V_{CC}, RF_IN and RF_OUT terminated to 50Ω, T_A = -40°C to +85°C. Typical values are at +3V and T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			2.7		4.2	V
Supply Current (Notes 4, 5)	Idle current = 250mA with V_{CC} = 3.3V	P_{OUT} = +24dBm, $V_{CC\_}$ = 3.3V		317	350	mA
		P_{OUT} = +25dBm, $V_{CC\_}$ = 4.2V		345		
		P_{OUT} = +23dBm, $V_{CC\_}$ = 3.0V		305		
	P_{OUT} = +21dBm with optimized output-matching circuit. Refer to the MAX2247 EV kit for details.			175		
	P_{OUT} = +18dBm with optimized output-matching circuit. Refer to the MAX2247 EV kit for details.			120		
	P_{OUT} = +15dBm with optimized output-matching circuit. Refer to the MAX2247 EV kit for details.			85		
Shutdown Supply Current	$\overline{SHDN}$ = 0, no RF signal applied			0.5	10	µA
Digital Input Logic High			2			V
Digital Input Logic Low					0.8	V
Digital Input Current High			-1		+5	µA
Digital Input Current Low			-1		+1	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2247 EV kit, $V_{CC\_}$ = +3V, f_{RF} = 2.45GHz, $\overline{SHDN}$ = V_{CC}, 50Ω RF system impedance, T_A = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency Range (Notes 5, 7)				2.4 to 2.5		GHz
Power Gain (Notes 3, 5, 9)	$V_{CC\_}$ = 3V, P_{OUT} = +23dBm	T_A = +25°C	26	29.5		dB
		T_A = -40°C to +85°C	25			
	$V_{CC\_}$ = 3.3V, P_{OUT} = +24dBm			29.5		
	$V_{CC\_}$ = 4.2V, P_{OUT} = +25dBm			30.5		
Gain Variation Over Supply Voltage (Note 5)	V_{CC} = 3.0V to 3.6V			±0.5		dB
Output Power Over Temperature (Notes 5, 9)	ACPR: First-side lobe < -32dBc, second-side lobe < -55dBc	$V_{CC\_}$ = 3V	22	23		dBm
		$V_{CC\_}$ = 3.3V		24		
		$V_{CC\_}$ = 4.2V		25		
Saturated Output Power	P_{IN} = +5dBm			27.8		dBm
Harmonic Output (2f, 3f, 4f)				-45		dBc
Input VSWR	Over full P_{IN} range			1.8:1	2.5:1	
Output VSWR	Over full P_{OUT} range			2:1	2.5:1	
Power Ramp Turn-On Time (Note 8)				0.8	1.5	µs
Power Ramp Turn-Off Time (Note 10)				0.8	1.5	µs
RF Output Detector Response Time				0.9		µs
RF Output Detector Voltage (Note 11)	P_{OUT} = +23dBm			1		V
	P_{OUT} = +15dBm			0.6		
	P_{OUT} = +7dBm			0.47		

Note 3: Characteristics are production tested at T_A = +25°C. DC specifications over temperature are guaranteed by design and characterization.

Note 4: Idle current is controlled by external DAC for best efficiency over the entire output power range.

Note 5: Parameter is measured with RF modulation based on IEEE 802.11b standard.

Note 6: Minimum and maximum specifications are guaranteed by design and characterization.

Note 7: Operation outside this range is possible but not guaranteed.

Note 8: The total turn-on time required for PA output power to settle to within 0.5dB of the final value.

Note 9: Specification is corrected for PC board loss of approximately 0.3dB, on the output of the MAX2247 EV kit.

Note 10: Total turn-off time required for PA supply current to fall below 10µA.

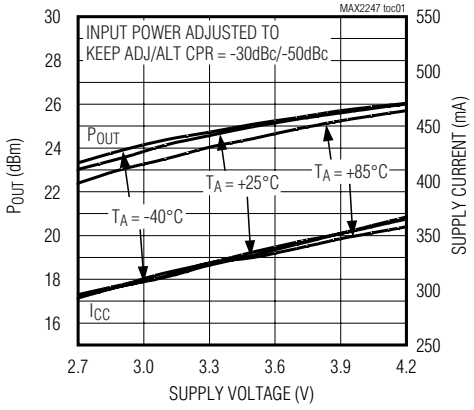
Note 11: See the *Typical Operating Characteristics* for statistical variation.

2.4GHz SiGe Linear Power Amplifier

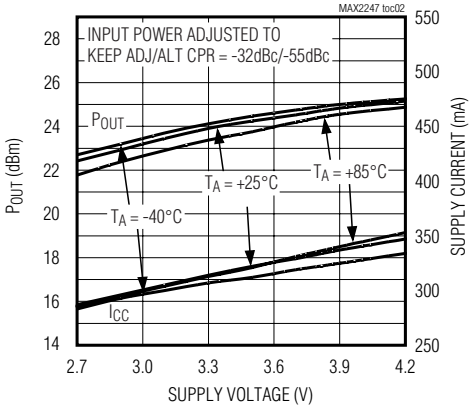
Typical Operating Characteristics

($V_{CC\_}$ = 3V, f_{RF} = 2.45GHz, with MAX2247 EV kit optimized for P_{OUT} = +23dBm. T_A = +25°C, unless otherwise noted.)

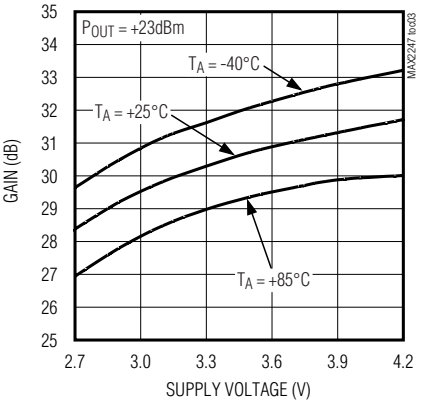
OUTPUT POWER, SUPPLY CURRENT vs. SUPPLY VOLTAGE



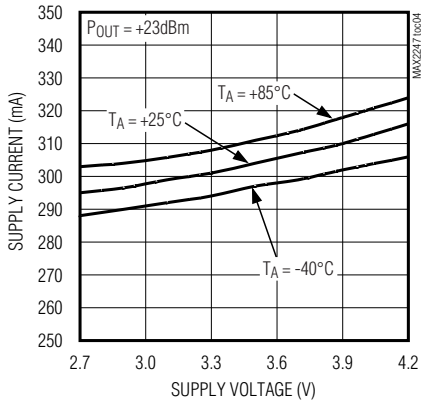
OUTPUT POWER, SUPPLY CURRENT vs. SUPPLY VOLTAGE



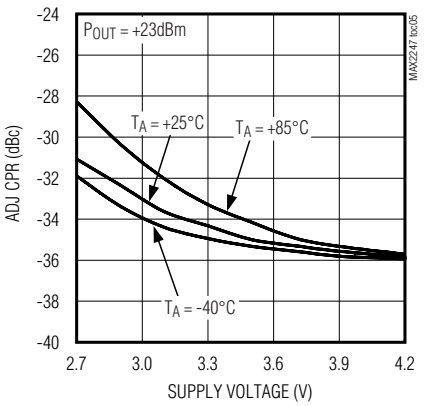
GAIN vs. SUPPLY VOLTAGE



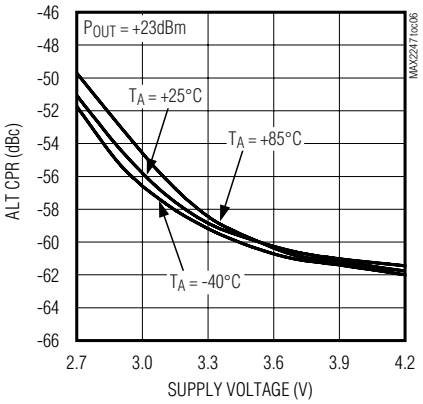
SUPPLY CURRENT vs. SUPPLY VOLTAGE



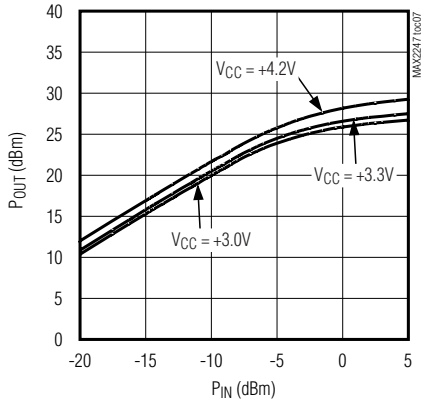
ADJ CPR vs. SUPPLY VOLTAGE



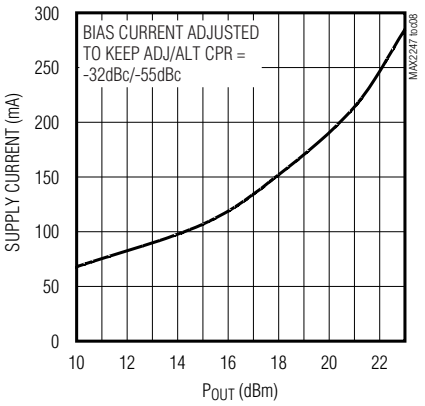
ALT CPR vs. SUPPLY VOLTAGE



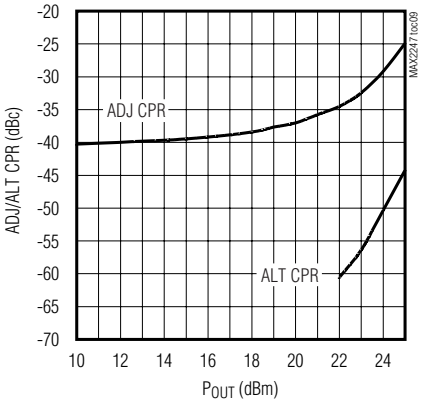
OUTPUT POWER vs. INPUT POWER



SUPPLY CURRENT vs. OUTPUT POWER



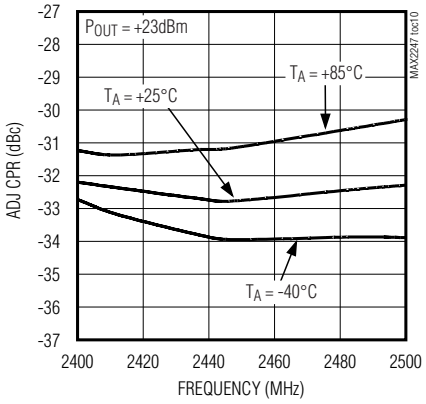
ADJ/ALT CPR vs. OUTPUT POWER



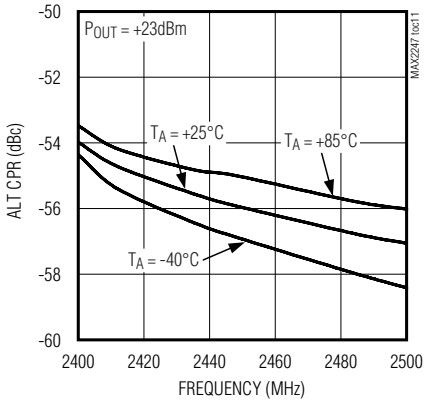
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 3V, f_{RF} = 2.45GHz, with MAX2247 EV kit optimized for P_{OUT} = +23dBm. T_A = +25°C, unless otherwise noted.)

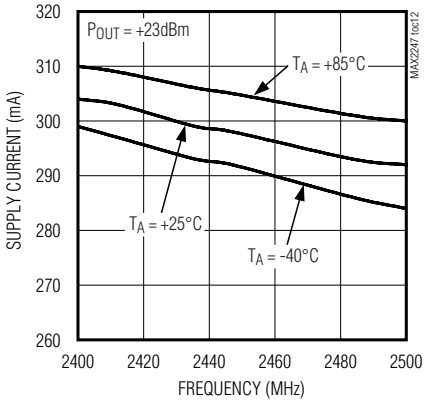
ADJ CPR vs. FREQUENCY



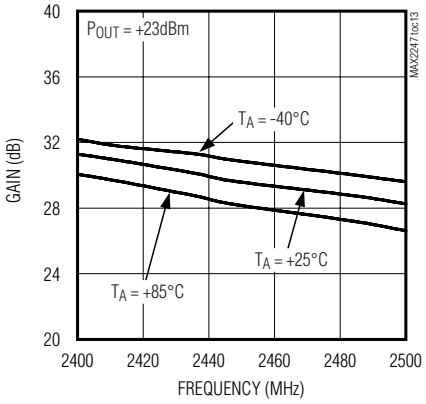
ALT CPR vs. FREQUENCY



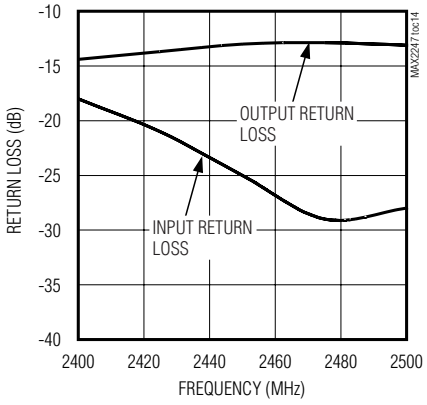
SUPPLY CURRENT vs. FREQUENCY



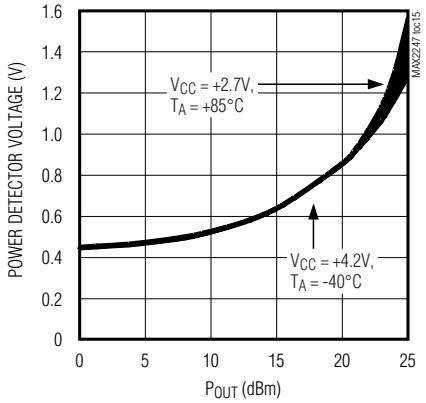
GAIN vs. FREQUENCY



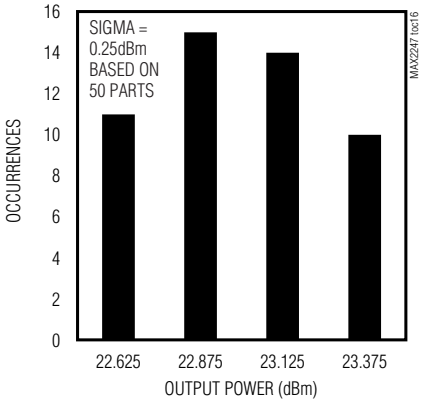
INPUT/OUTPUT RETURN LOSS vs. FREQUENCY



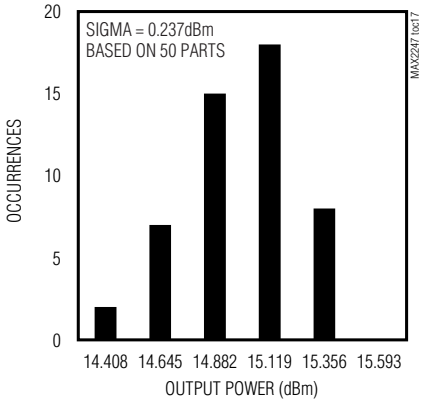
POWER DETECTOR VOLTAGE vs. OUTPUT POWER



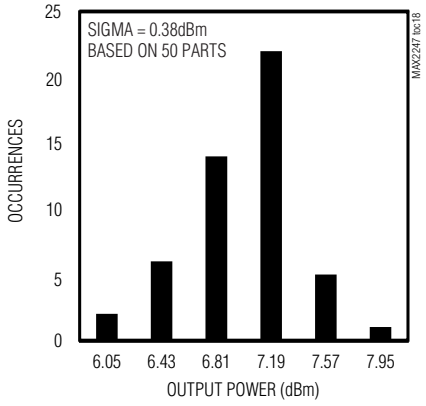
OUTPUT POWER HISTOGRAM AT FIXED 1V POWER DETECTOR VOLTAGE



OUTPUT POWER HISTOGRAM AT FIXED 0.6V POWER DETECTOR VOLTAGE



OUTPUT POWER HISTOGRAM AT FIXED 0.47V POWER DETECTOR VOLTAGE

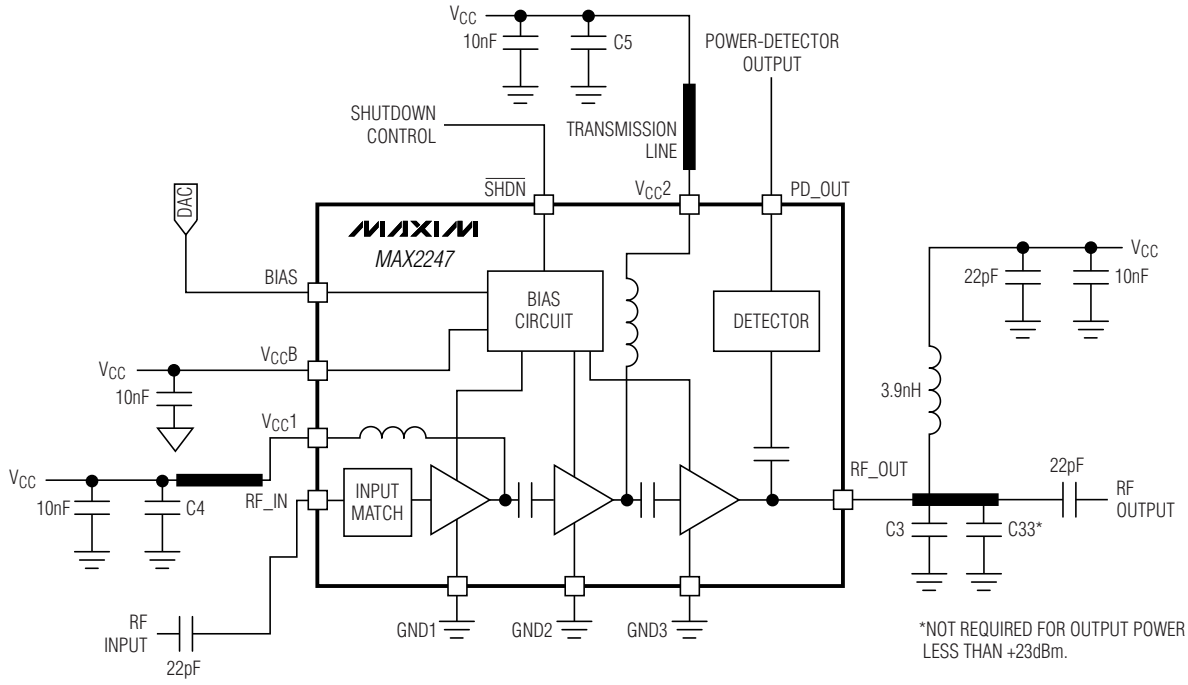


2.4GHz SiGe Linear Power Amplifier

Pin Description

BUMP	NAME	DESCRIPTION
A1	BIAS	Bias Control. The overall current is set by the current sourced through the bias pin. See the *Bias Circuitry* section.
A2	$V_{CC}2$	Second-Stage DC Supply Voltage. Sets the bias and external matching for the second amplifier stage. Requires a small inductance. Bypass to ground using the configuration in the *Typical Operating Circuit.*
A3	GND2	Second-Stage Ground. See the *Applications Information* section for detailed layout information.
A4	$V_{CC}1$	First-Stage DC Supply Voltage. Sets the bias and external matching for the first amplifier stage. Requires a small inductance. Bypass to ground using the configuration in the *Typical Operating Circuit*.
B1	GND3	Third-Stage Ground. See the *Applications Information* section for detailed layout information.
B3	PD_OUT	Power-Detector Output. This output is a DC voltage indicating the PA output power.
B4	GND1	First-Stage and Bias-Control Circuit Ground
C1	RF_OUT	RF Output. Open-collector output. Requires a pullup inductor, which is part of the matching network.
C2	$\overline{SHDN}$	Shutdown Input. Drive logic low to place the device in shutdown mode. Drive logic high for normal operation.
C3	$V_{CC}B$	Bias Circuit DC Supply Voltage. Bypass to ground using the configuration in the *Typical Operating Circuit.*
C4	RF_IN	RF Input. Internally matched to 50Ω. Requires an external DC-blocking cap.

Functional Diagram/Typical Operating Circuit



REFER TO THE MAX2247 EV KIT FOR LAYOUT AND DESIGN DETAILS.

Detailed Description

The MAX2247 linear power amplifier (PA) offers a wide variety of features incorporated into a tiny UCSP package. The device includes internal bias circuitry, an integrated power detector with buffered output, low-power shutdown mode, and internal input matching. The MAX2247 output power can be optimized for +15dBm to +24dBm by adjusting the output, first-stage, and second-stage matching network (see the *Typical Operating Circuit*) while exceeding 802.11b ACPR requirements. In addition, external bias control allows dynamic throttle-back of the supply current to increase efficiency.

The MAX2247's performance can be optimized for lower output power levels. Go to the Maxim website, www.maxim-ic.com, for MAX2247 application notes covering performance at +21dBm, +18dbm, and +15dBm.

Bias Circuitry

To improve efficiency at lower output levels, a bias pin is offered to allow dynamic current control. An external current DAC or resistor network can be used to throttle-back current at lower output powers while still maintaining ACPR requirements. By including an internal voltage regulator along with the bias circuitry, no external bias voltage is necessary. The internal voltage regulator maintains stable performance of the bias circuitry over temperature and supply variations.

The overall current of the MAX2247 is set by the current sourced through the bias pin. The overall current is 540 times the bias current. An internal bandgap reference provides +1.2V to each bias stage (see Figure 1). An external resistor to ground can be placed at the bias pin to set the bias current (refer to the MAX2247 evaluation kit).

An external current DAC can be connected directly to the bias pin to adjust the bias current of the MAX2247. Figure 2 shows the MAX2247 connected to the MAX2820 zero-IF transceiver, which includes a 4-bit DAC.

Shutdown Mode

The MAX2247 features a low-power shutdown mode to further reduce current consumption. The MAX2247 responds to logic-level signals at the $\overline{SHDN}$ pin. A logic-level high enables all circuitry, while a logic-level low places the device in low-power shutdown mode and reduces supply current to 0.5µA (typ). Power-ramp turn-on and turn-off times are guaranteed to be less than 1.5µs.

Power Detector

This device includes a power detector that samples the peak voltage of the output and generates a voltage proportional to the output power. The detector is fully temperature compensated and allows the user to set the detector bandwidth with an external capacitor.

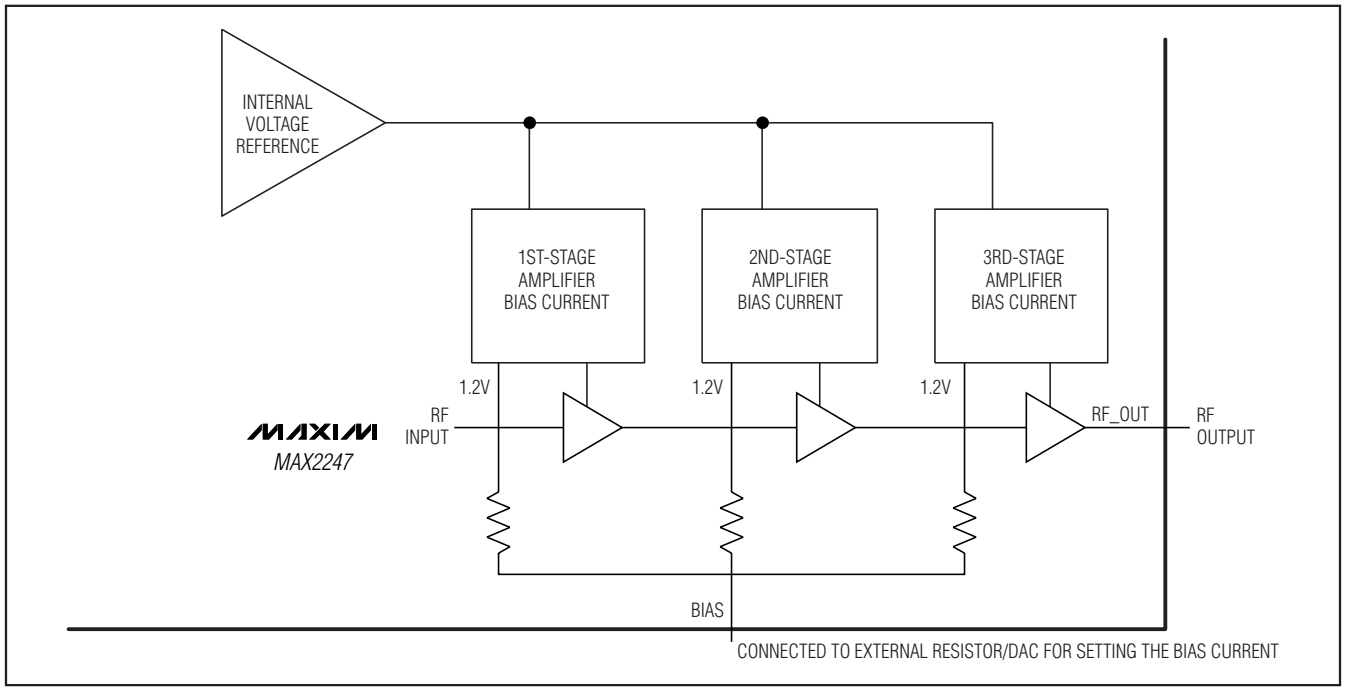


Figure 1. Internal Bias Circuitry

2.4GHz SiGe Linear Power Amplifier

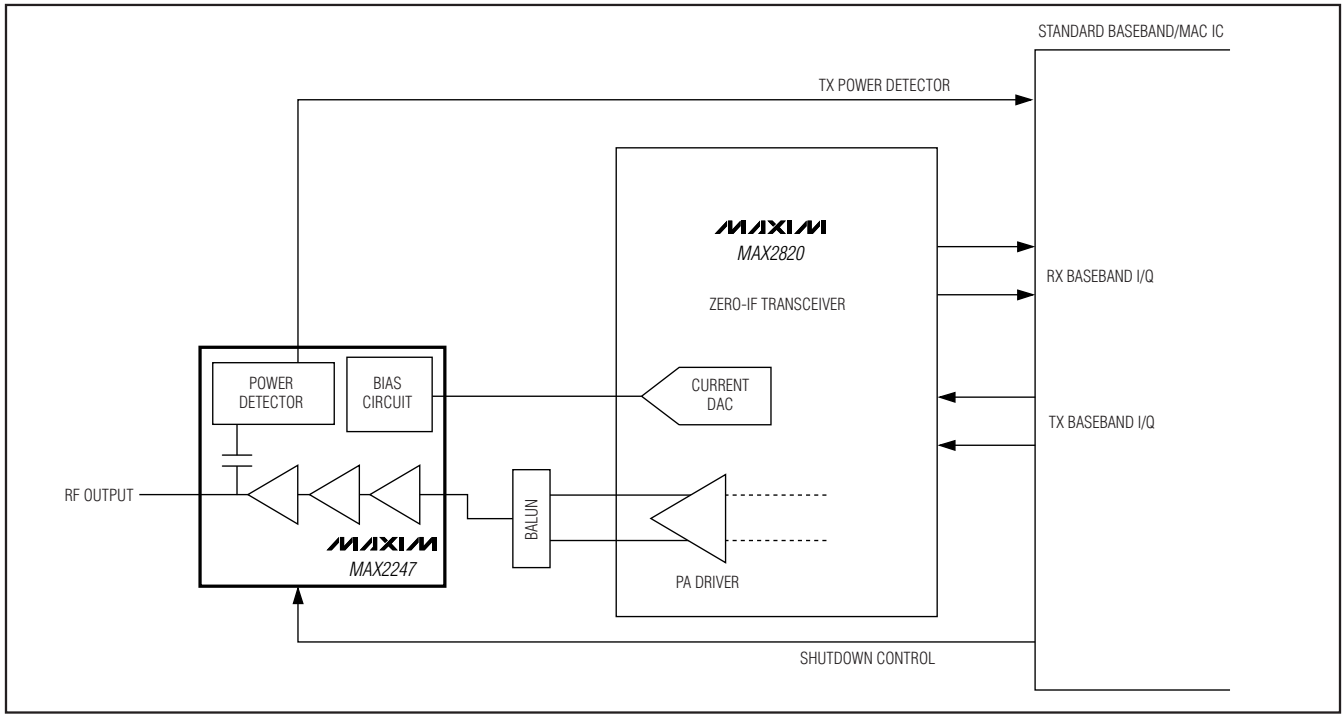


Figure 2. The MAX2247 Connected to the Current DAC of the MAX2820 for Bias Control

Applications Information

The MAX2247 is a three-stage amplifier that requires special attention to board layout and grounding for optimum output power, gain, efficiency, and side-lobe suppression. For ease of implementation, the MAX2247 evaluation (EV) kit layout should be used as a model. Gerber files are available from Maxim upon request. Follow the recommendations below to optimize performance when adapting the layout to your board.

Interstage Matching and Bypassing

$V_{CC}1$ and $V_{CC}2$ provide DC bias to the open-collector outputs of the first- and second-stage amplifiers and are also part of the interstage matching networks required to optimize performance among the three amplifier stages. The MAX2247 must have a small amount of inductance on the V_{CC} lines in addition to the inductance already provided on-chip. See the *Typical Application Circuit* for the lumped and discrete component values used on the MAX2247 EV kit for optimum interstage matching and RF bypassing.

In addition to RF bypass capacitors on each bias line, a global bypass capacitor of 4.7µF is necessary to filter any noise on the supply line. Route separate V_{CC} bias paths from the global bypass capacitor (using a star topology) to avoid coupling between PA stages. Use the MAX2247 EV kit PC board layout as a guide.

Input Matching

The MAX2247 includes internal input matching to 50Ω, so no external matching network is required. A DC-blocking capacitor is required at the input to the device.

Output Matching

The RF_OUT port is an open-collector output that must be pulled to V_{CC} through an RF choke for proper biasing (see the *Typical Operating Circuit*). A shunt 22pF capacitor to ground is required at the supply side of the inductor. In addition, a matching network is required for optimum gain, efficiency, ACPR, and output power. The EV kit should serve as a good starting point for your layout. However, optimum performance is layout dependent, and some component optimization may be required. It is important to leave room on your board for tuning/optimization.

Ground Vias

To achieve optimum gain, output power, thermal performance, and ACPR performance, ground vias should be properly placed throughout the layout. Each ground pin requires its own through-hole via (diameter = 10mils) placed as near as possible to the device pin. This reduces ground inductance, thermal resistance, and feedback between stages. Use the MAX2247 EV kit PC board layout as a guide.

UCSP Reliability

The tiny chip-scale package (UCSP) represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. Operating life test and moisture resistance remains uncompromised, as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSP solder-joint contact integrity must be considered because the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Users should also be aware that as with any interconnect system there are electromigration-based current limits that, in this case, apply to the maximum allowable current in the bumps. Reliability is a function of this current, the duty cycle, lifetime, and bump temperature. See the *Absolute Maximum Ratings* section for any specific limitations listed under Continuous Operating Lifetime. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com/1st_pages/UCSP.htm.

Chip Information

TRANSISTOR COUNT: 1425

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
4 x 3 UCSP	B12-8	**21-0104**
12 WLP	W121B2+2	**21-0009**

2.4GHz SiGe Linear Power Amplifier

Revision History

REVISION NUMBER	REVISION DATE		PAGES CHANGED
4	8/03	—	—
5	1/09	Added MAX2247EWC+T to *Ordering Information*, added WLP package information	1, 2, 9

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX2247EBC+T MAX2247EBC-T MAX2247EBC-T10 MAX2247EBC+TW